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FEUP FACULDADE DE ENGENHARIA
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IMPLANTE PARA ESTIMULAÇÃO ELÉTRICA NERVOSA

ELECTRONIC IMPLANT FOR NERVOUS STIMULATION

RENATO FERREIRA BORGES

DISSERTAÇÃO DE MESTRADO APRESENTADA
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FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO

Implante para Estimulação Elétrica Nervosa

Electronic Implant for Nervous Stimulation

Renato Ferreira Borges

WORKING VERSION

DISSERTAÇÃO

Supervisor: Professor José Machado da Silva

3 de julho de 2016

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Resumo

Nesta dissertação é apresentado um dispositivo implantável para estimulação elétrica neuromuscular (NMES) local do ligamento cruzado anterior ou posterior, depois deste ter sido submetido a uma cirurgia de reconstrução. O objectivo da estimulação é o fortalecimento do ligamento para proporcionar estabilidade do joelho e assim promover uma mais rápida recuperação e retorno à atividade desportiva.

Este implante foi desenvolvido numa tecnologia CMOS de 180 nm e apresenta um funcionamento semi-ativo, pois não tem fonte de alimentação própria permanente, que é assegurada por uma interface por acoplamento indutivo. Este acoplamento é usado também para estabelecer uma comunicação $half-duplex$ entre um controlador externo e o implante, utilizando um esquema de modulação binária por comutação de fase (BPSK). O controlador externo permite que o terapeuta possa alterar os parâmetros de estimulação. Esta é bifásica com balanceamento de cargas de modo a evitar a acumulação de carga elétrica nas interfaces elétrodo - tecido nervoso. No circuito implantado, um circuito de *front-end* de baixo consumo de energia, composto por um retificador e um regulador linear, regula a tensão contínua de 2,5 V para alimentar o circuito do micro-estimulador e uma outra de 1,8 V para alimentar os restantes circuitos analógico/digitais: o desmodulador BPSK, a máquina de estados de leitura dos comandos, e os conversores digital/analógico dos circuitos de configuração dos parâmetros de estimulação. O desmodulador BPSK deteta o sinal modulado recebido e recupera o sinal de relógio e os dados de programação do circuito micro-estimulador. Estes são a duração do estímulo, a intensidade/amplitude, e a frequência e largura de pulso da onda de estimulação. Os impulsos elétricos serão aplicados ao ligamento por meio de elétrodos de garra, que serão colocados e amarrados em torno do novo ligamento para promover uma estimulação eficiente.

Abstract

This dissertation presents the design of an implantable device within a CMOS technology of 180 nm, for in-situ neuromuscular electrical stimulation (NMES) of the new cruciate ligament, after a posterior or anterior cruciate ligament reconstruction surgery. The goal of the stimulation is to strengthen the ligament to provide knee stability and to promote a faster recovery and return to sports. An inductive interface is used to power the implant, as well as, to establish a half-duplex communication between an external controller and the implant, using a binary phase shift keying (BPSK) modulation scheme. The external controller is used to allow the doctor or the physician to change the stimulation parameters. At the receiver side, a low-power fully-integrated 13,56 MHz CMOS RF front-end circuit was designed. It comprises a rectifier that converts the incoming BPSK signal into a non-regulated DC voltage, a linear regulator that provides two regulated DC voltages, 2,5 V voltage to power the micro-stimulator circuit and 1,8 V to power the remaining analogue/digital circuits, a BPSK demodulator that detects the modulated data and recovers the clock and data that will program the micro-stimulator circuit for stimulus duration, intensity/amplitude, and frequency and pulse width of the charge-balanced biphasic stimulating waveform. The electric impulses will be delivered to the ligament via cuff electrodes that will be placed and tied around the new ligament to insure an efficient stimulation.

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First of all, and as it should be, I would like to thank Prof. José Machado da Silva, my mentor of dissertation, for the the permanent demonstrated availability, crucial to the realization of this thesis. The numerous meetings with him and Prof. Dr. Jorge Marinho, as well as, the discussions and recommendations given by other, revealed to be essential guidelines for the realization of this project. Secondly, I would like to thank the staff of the Microelectronics and Bioelectronics group in the Electrical Engineering department of the Delft University of Technology (TU Delft), where I spent 5 months in an internship during which I learned the basis of analogue and digital CMOS design, IC fabrication and to use the Cadence Virtuoso software. In particular, I am grateful to Prof. Ir. Wouter Serdijn, leader of Bioelectronics group, and to Gustavo Campos Martins, my co-supervisor in TU Delft, for the constant help and availability that they always shown to teach and help me. Last but not the least, I want to leave here a very special thanks to my close relatives and friends for the constant presence next to me and support when I needed.

Renato Ferreira Borges

Contents

List of Figures

List of Tables

Abreviaturas e Símbolos

ACL, PCL	Anterior and Posterior Cruciate Ligament
NMES	Neuromuscular Electrical Stimulation
BPSK	Binary Phase-shift Keying
RF	Radio-Frequency
WPT	Wireless Power Transfer
PMOS, NMOS	P and N-channel Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complementary Metal-Oxide-semiconductor
OTA	Operational Transconductance Amplifier
PSRR	Power-Supply Rejection Ratio
UGF	Unity-gain Frequency
SIPO	Serial-in and Parallel-out
DAC	Digital to Analog Converter
VCO	Voltage Controlled Oscilaltor
PA	Power Amplifier
k	Coupling Factor
n	Inductance ratio
a.c.	Alternating current (which means a non-zero signal frequency)
d.c.	Direct current (which refers to a zero frequency signal)
R_{load2}	Equivalent a.c. resistor of the rectifier connected to the loaded regulator
Z_{eq}	The equivalent impedance of the secondary transformed to the primary
R_{eq}	Z_{eq} that become real at the phase-resonance frequency of the secondary
n_1, n_2	Number of turns in the primary and secondary coil
L_{S2}, R_{S2}	Secondary coil inductance and resistance
C_2	Resonance capacitor for the secondary
L_{S1}, R_{S1}	Primary coil inductance and resistance
C_{1res}	Resonance capacitor in a (semi-) resonant class-E driver
$Q_{L_{S1}}$, $Q_{L_{S2}}$	Primary and secondary coil quality factor
C_{1ser}	Primary series capacitor in a class-E driver
C_{1par}	Primary parallel capacitor in a class-E driver
R^*_{S1}	Series resistance of the primary coil coupled to the secondary circuit
V_{prim}, V_{sec}	a.c. link input and output (= voltage across R_{load2}) voltage

Chapter 1

Introduction

1.1 Background and Objectives

Injuries related to torn anterior and posterior cruciate ligaments (ACL/PCL) are among the most common ones in the world of sports. Their reconstruction by means of surgical operation followed by physical rehabilitation, takes a long time until the athlete can return to sport activities [1], [2]. As these injuries may require long recovery times, specialists have investigated several procedures that allow for reducing those times.

Electrical muscle stimulation has received increased attention in the last few years because of its potential to serve as a strengthening training tool for healthy subjects and athletes, a rehabilitation and preventive tool for partially or totally immobilized patients, a testing tool for evaluating the neural and/or muscular function *in-vivo*, and a post-exercise recovery tool for athletes [3]. Neuromuscular electrical stimulation, or NMES, which is one of the types of electrical stimulation used in the orthopedic procedures to strengthen or rehabilitate muscles, has received increased attention due to its capability to induce muscle activation and provide muscular strengthening to increase knee stability after the replacement of the injured cruciate ligament [2]. Several systems of neuromuscular electrical stimulation [4], [5], [6] for quadriceps and hamstrings, aiming at overcoming weakness and to protect the graft, are currently available.

The interest for implantable medical devices to provide electrical stimulation has been growing in many clinical applications during recent years, due to the proven therapeutic and rehabilitative effects of electrical stimulation [7], [8]. Advanced implantable smart stimulator devices must satisfy requirements such as high reliability, high degree of programmability, small size and long life-time. The availability of precise and user-friendly external means to control their operation, to define or calibrate stimulation parameters, is also a desirable feature [9]. Hereupon, an externally controlled implantable stimulator device was thought and discussed with medical staff to provide in-situ electrical stimulation to the new cruciate ligament in an early post-operative phase after surgery to strength and protect the graft, at the same time as enhance knee stability.

Several externally powered and controlled implants have been designed for different neuromuscular stimulation applications, such as, rehabilitation of voluntary bladder voiding [10], [11],

functional neuromuscular stimulation (FNS) [12], [13], and cochlear prostheses [14]. To the best of our knowledge, this new approach of direct stimulation of the new ligament, moves away from the nowadays existing techniques of neuromuscular electrical stimulation on quadriceps or hamstrings to overcome muscle strength deficits and knee instability after anterior/posterior cruciate ligament reconstruction surgery [15].

The main goal of this dissertation is to develop a wireless powered and controlled implantable device that directly applies neuromuscular electrical stimulation via electrodes to the new ligament that replaces the injured ACL/PCL, with the purpose of giving more strength, induce growth, and improve knee stability. Data and power can be transmitted from a portable external source placed in the leg above the knee to the biomedical implant embedded in the graft via an inductive link between two coils (one external and other internal to the body) operating at a carrier frequency of 13,56 MHz, since the power loss in the surrounding tissues can be ignored at this frequency and this is one of the frequencies internationally selected for Industrial, Scientific and Medical (ISM) applications. The external controller, which is meant to be used by the doctor, is able to trigger the stimulation and to change functional parameters according to the stage of the recovery process. The system is intended to be safe, efficient, comfortable and must not affect the functionality and the integrity of the knee, specially the new cruciate ligament.

1.2 Structure of the Dissertation

The present dissertation is composed of five chapters, of which this is the first one and where the underlining motivation, objectives and scientific background are described. The chapter ends with the description of the overall structure of the dissertation and of the contents of the different chapters.

Chapter 2 describes in more detail the motivation behind the development of this implantable stimulator device. It starts with an overview on the anterior/posterior cruciate ligament injury and of the surgery procedure and rehabilitation protocol. A review of the effects of the neuromuscular electrical stimulation after ACL/PCL reconstruction based on relevant literature, along with a description of the developed system, is then is presented.

In chapter 3 the general block diagram of the implant meant to be inserted inside the graft and the details followed to design the corresponding circuits, are presented. The design of the low-power CMOS front-end containing the rectifier, regulator and demodulator along with the programmable micro-stimulator are fully detailed.

Chapter 4 describes system and the design of the external device circuit, to be used to power and send the stimulation parameters to the implant. A strategy procedure is presented. First, the design of the transmitter coils is discussed, and then the step-by-step design optimization procedure (based on the set of recommended design equations) that was followed to achieve maximal link efficiency is described. This approach provides the values for the components of the circuit that ensures the wireless powering and data transfer system.

Finally, in chapter 5, the conclusions of this dissertation are highlighted with a summary and critical discussion on the most important obtained results. A vision for future work to be carried out in order to create a more flexible and efficient system, is also presented.

Chapter 2

In-Situ Neuromuscular Electrical Stimulator for Post ACL/PCL Repair

Injuries related to torn cruciate ligaments are among the most common ones in the world of sports and may require long recovery times after reconstruction surgery. The reducing of the recovery time after the ligament reconstruction is important for both patient and doctor and, thus, the use of electrical muscle stimulation has received increasing attention because of its potential to induce muscle activation and provide muscular strengthening to increase knee stability after the replacement of the injured cruciate ligament [2].

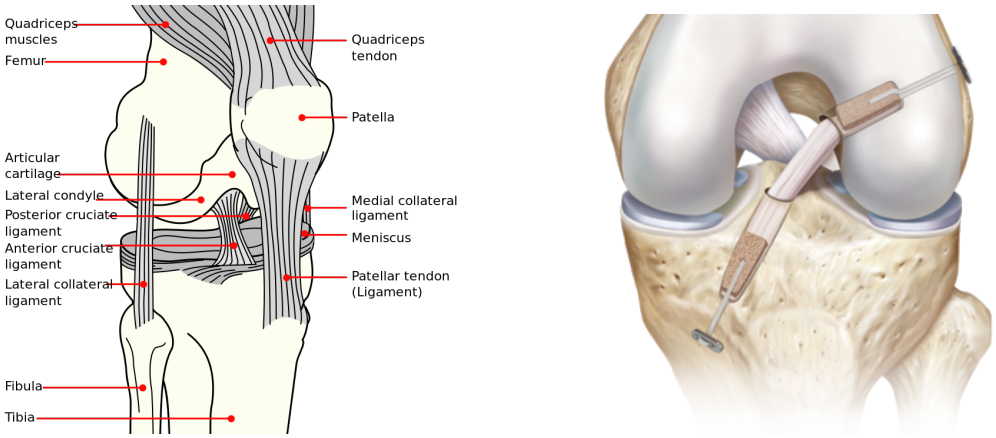
2.1 Anterior/Posterior Cruciate Ligament Injuries, Surgery and Rehabilitation

The anterior and posterior cruciate ligaments (ACL/PCL) are a pair of ligaments present in the human knee, arranged in a crossed formation that connect the base of the femur to the top of the tibia (Figure 2.1a). These ligaments prevent the knee from excessive forward and backward movements, as well as twisting movements in either direction. The mean length of these ligaments is 32 mm, the average width is 11 mm and the average cross-sectional area is around 41 mm^2 [2].

ACL/PCL tear are the most common ligament injury in the world of sports and may require long recovery times or could even end with an athlete's career. Athletes who participate in high demand sports like soccer, basketball or tennis are more likely to suffer these injuries. Studies [1] reveal that female athletes have higher incidence of ACL injury than their male mates, being this related to differences in physical conditioning and muscular strength since the stronger the quadriceps muscles, the larger and hence stronger the cruciate ligaments. The sprain or tear of the ligaments can occur due to [1]:

- Changing direction rapidly;
- Stopping suddenly;
- Landing from a jump incorrectly;
- Direct contact or collision, such as a soccer tackle;

In some cases, when the ligament is not completely torn and the knee is still stable or if the patient no longer wishes to participate in strenuous physical activities, the surgery can be avoided and the injury can be treated with strengthening and rehabilitation. However, surgery remains the treatment of choice in almost all athletes who want to remain active, but, unfortunately, surgery is not always successful. In arthroscopic ACL/PCL reconstruction the surgeon makes two or three small incisions in order to remove the torn ligament and clean all the area. After that, surgical drills are inserted through other small incisions. The surgeon drills small holes into the upper and lower leg bones where these bones come close together at the knee joint. The holes form tunnels through which the new ligament will be anchored. For this new ligament auto-grafts, such as the tendon of the kneecap (patellar tendon) or one of the hamstring tendons, are used. Then, the graft is pulled through the two tunnels that were drilled in the upper and lower leg bones. The surgeon secures the graft with screws or staples and closes the incisions with stitches or tape [2]. A reconstructed ACL is shown in Figure 2.1b.



(a) (b)

Figure 2.1: (a) Knee anatomy and (b) ACL reconstruction.

After reconstruction surgery, patients are often plagued with quadriceps femoris weakness, which may result in serious functional deficits and limitations, such as, slower walking speeds, longer stair-climbing times, and increased risk of falls [16]. The goals of post operative rehabilitation are to restore normal joint motion and strength to the reconstructed knee, while protecting the graft. The strengthening of the surrounding muscles (hamstrings and quadriceps) gradually increases the stress across the ligament. Physical therapy using exercises to increase the range of movement, strengthening of the quadriceps and hamstrings, and proprioception can help many people regain motion and strength in their knee.

The rehabilitation and recovery process usually takes 6 to 8 months after surgery and then the athlete can return to the normal sports activities. Since the source of the quadriceps femoris weakness is voluntary activation deficits in early stages after ACL/PCL reconstruction, at this stage voluntary exercise programs have had limited success in restoring quadriceps strength and, thus new procedures using electrical muscle activation has seen to have the potential to override

muscle activation deficits [16] and to complement physical rehabilitation in order to reduce the recovery times. It should be noted that the decision to return to sports must be a medical decision based on the functional assessment of the knee joint, because too early return to sports may result in graft failure [2].

2.2 Literature Review of Neuromuscular Electrical Stimulation

The electrical muscle stimulation (EMS) is the elicitation of muscle contraction (beyond motor threshold) using electric impulses that can be used as a training [17], for pain therapy, and as a therapeutic tool [7],[8]. Nowadays, the neuromuscular electrical stimulation (one of the types of electrical stimulation), also known as NMES, which is applied to the muscle in static conditions, has received increasing attention in the last few years, because of its potential to serve as therapeutic tool for muscle strengthening, maintenance of muscle mass and strength during prolonged periods of immobilization after musculoskeletal injuries [3], such as ACL/PCL injury. Postoperative weakness, muscle atrophy and instability of the knee are common following ACL/PCL reconstruction. In some studies [8], [15], [7], [18], neuromuscular electrical stimulation for clinical rehabilitation, was applied to the quadriceps/hamstrings in order to overcome its strength and function deficits after ACL/PCL reconstructions. With the training of these muscles also the knee stability and the strength of the graft for the new ACL/PCL are significantly improved. The electrical impulses are generated by a device and delivered through electrodes on the skin in direct proximity to the muscles to be stimulated, as shown in Figure 2.2. The impulses mimic the action potential coming from the central nervous system, causing muscles to contract and because of that it is necessary to carefully specify the NMES parameters in order to seeking effective treatments for patients following ACL/PCL reconstruction. A variability of these parameters may have impact on the clinical outcomes of the treatment [15].

Figure 2.2: Neuromuscular electrical stimulation on the quadriceps and hamstrings.

It has been referred in [7] that augmentation of muscle strength with NMES occurs in a similar manner to augmentation of muscle strength with voluntary exercise, and also that the muscle strengthening seen following NMES training results from a reversal of voluntary recruitment order with a selective augmentation of type II muscle fibres, because type II fibres (fast-twitch) have

a higher specific force than type I fibres. Also, selective augmentation of type II muscle fibres will increase the overall strength of the muscle and result in an improved functional performance. However, the spatially fixed recruitment implies that, as the same motor units are repeatedly activated, muscle fatigue may result and that represents the major limitation of NMES. This fatigue may also result in muscle damage [3].

Some reviews [19], [20] indicate that NMES with exercise is more effective than exercise alone in improving isometric knee extension strength. NMES has the potential to override muscle activation deficits by activating a greater proportion of type II muscle fibers when compared to volitional exercise at a comparable intensity. They also suggests that the incorporation of NMES treatment sessions along with exercise, is warranted in the treatment of patients recovering from ACL/PCL reconstruction, and treatment should be initiated within the first week and continued through at least the fourth postoperative week. The effectiveness of NMES was observed for a low number of repetitions with high external loads and a high intensity of muscle contraction [7].

From here, the procedure that allows for a quick complete recovery from ACL/PCL surgery and a faster return to sports is a combination of both exercises and NMES stimulation. The rehabilitation with only exercises may take up to 6 to 8 months to restore normal joint motion and strength to the reconstructed knee, but nowadays the more realistic is 10 to 14 weeks [18]. The effect outcome is to have more motor fibers recruited using electrical stimulation and volitional exercises than one would have with solely volitional exercising [7],[15].

Unfortunately, the utility of the NMES for sport application still remains controversial. For example, it is true that many research studies find muscle strength and recovery after physical effort significantly improved by NMES [21], [22], [23], but other few do not [24], [25]. It is also unclear whether the NMES is completely safe. Some authors maintain that NMES could induce muscle damage or influence on function and biomechanics of the near articulations of the stimulated muscles [26].

The neuromuscular electrical stimulation procedure applied to quadriceps femoris combined with physical therapy, has been applied in recent years to patients after ACL/PCL reconstruction using different types of stimulators [4] and strategies of stimulation [5], and their outcomes and benefits have been studied. Differences in quadriceps muscle-torque generating capacity between a clinical console device (VersaStim 380 - Figure 2.3a) whose power source is provided by an electrical outlet and a portable electrical muscle stimulator (Empi 300PV - Figure 2.3b) were tested with a non-pathological group of subjects under the same assessment conditions. The results advocate the use of the portable stimulator since it produces comparable levels of average peak torque at comparable levels of discomfort to those produced by the clinical stimulator, and it also has better safety in use, and is more comfortable for the patient [4].

As far as the stimulation strategy is concerned, different waveforms produce different results. The ability to generate isometric contractions of the quadriceps femoris muscles along with muscle fatigue caused by repeated contractions induced by 3 different waveforms was compared. In [5], a clinical stimulator was used to generate a 2,500 Hz alternating current (polyphasic waveform) and a portable battery-operated stimulator was used to generate either a monophasic or biphasic

rectangular waveform. The results indicated that biphasic waveforms have an advantage over the polyphasic waveform, since they generated contractions with greater torque and were also less fatiguing.

(a) (b)

Figure 2.3: (a) Clinical NMES stimulator plugged to an outlet and (b) small, battery-operated and portable NMES stimulator.

2.3 System Description

As it will be described in section 2.2, it is known that NMES applied to quadriceps and hamstrings significantly improves quadriceps muscle mass and strength, which consequently increases the stress across the ligament and thus knee stability. But here, we address a new type of NMES for post ACL/PCL reconstruction that consists in a direct application of electrical impulses to the graft that replaces the injured ligament. With this, it is expected to accelerate the healing and to strength the ligament and, thus improve knee stability within a short recovery time.

In this dissertation, we present a first prototype of an in-situ implantable neuromuscular electrical stimulator wirelessly powered and controlled by an external controller via inductive coupling. It permits to produce flexible and precise biphasic current stimulation waveforms where the intensity of stimulation, pulse width, frequency of stimulation and on and off times of the stimulus are externally controlled. At the receiver side, to recover the transmitted data and power via BPSK signals, a low-power RF front-end circuit, that includes a rectifier, a linear regulator, a BPSK demodulator to recover the clock and programming data, is needed. The implantable stimulator will be located inside the new cruciate ligament and will provide the electrical impulses via cuff electrodes placed around the ligament. Figure 2.4 shows the block diagram of the proposed medical system for neuromuscular stimulation.

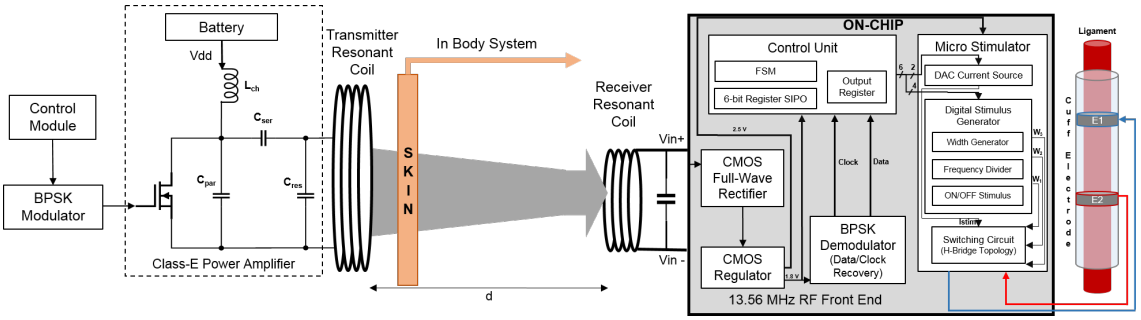


Figure 2.4: Block diagram of the implemented system.

The first and the main block of this device is the wireless power transfer system which is supplied by a battery and delivers the power and stimulation data to the implantable electronics from the transmitter to the receiver coil via a inductive link. Data is encoded and modulated at the carrier frequency of 13,56 MHz and, then transmitted to the body following the same principle. At the implantable side, a receiver coil captures the magnetic flux lines and a low power 13,56 MHz CMOS RF front-end circuit is used to recover the transmitted power and data which includes a rectifier, a regulator and a demodulator. A control unit receives the data for the stimulation parameters from the exterior and controls the stimulation waveform pattern and intensity in the micro-stimulator to proper stimulate the new ligament.

2.4 Conclusion

From the literature review is known that cruciate ligaments are one of the most common injuries and one that takes longer to complete recovery from injury and return to sports. NMES has already been applied to the quadriceps and hamstrings and the results are satisfactory, since using devices that can provide electrical stimulation via surface electrodes, muscle contraction is achieved without making any effort by the patient. With this procedures already being applied the recovery time was slightly reduced below 6 months. However, this external NMES stimulation only strengthens the thigh muscles and thus indirectly increases the stress across the new ligament. From here, it was thought to use an implantable device for applying directly stimulating ligament, in order to further increase the voltage across it, in order to give more strength and thus achieve a recovery time even lower. For the design of this implantable device we focused in the characteristics of the available devices for external NMES that reveals better results in reducing recovery time and it effectiveness.

Chapter 3

Design of Implantable Device

This chapter delves into the design of the implantable device in order to both fit inside the new cruciate ligament, as well as, to show an efficient operation to receive the power and data from the external controlling device. The design of the SoC (System on Chip) integrated circuit is divided in the description and design of each one of the comprises blocks, i. e., the RF front-end circuit that implements the receiver of the signal conveying the stimulation parameters and that regulates the power coming from the exterior, the power supply voltage regulators that ensure a stable power supply voltage, the data decoder that recovers the wirelessly transmitted commands, and the programmable micro-stimulator circuit that produces the electric impulses to be applied to the ligament in a safe and efficient manner.

3.1 Implant Dimensions and Shape

Figure 3.1a illustrates the external aspect foreseen for the implant, whose block diagram was presented in Figure 2.4. For the design of the receiver coil the main constraint is its dimensions, once these need to be adapted to the limited dimensions of the implant and this has to be quite smaller than the size of the new ligament where the implantable device will be located. Hereupon, as the average dimensions of the ligament are already known from Section 2.1, it is possible to foresee how the implantable micro-stimulation device will look like. A device with a cylindrical shape with length of 10 mm and radius of 2,5 mm, is expected to fit the implant dimensions. So, the size of the receiver coil will be limited to these dimensions, but the coil size has more length constraints in order to save space for the power conditioning and micro-stimulation integrated circuits. On the other hand, the radius of the coil should be as large as possible, in order to capture more magnetic flux lines that come from the primary coil. Thus, a single layer long solenoid shape with 6 mm of length and 2 mm of radius are the chosen dimensions for the receiver coil, which will be embedded in the implantable device, as shown in Figure 3.1b.

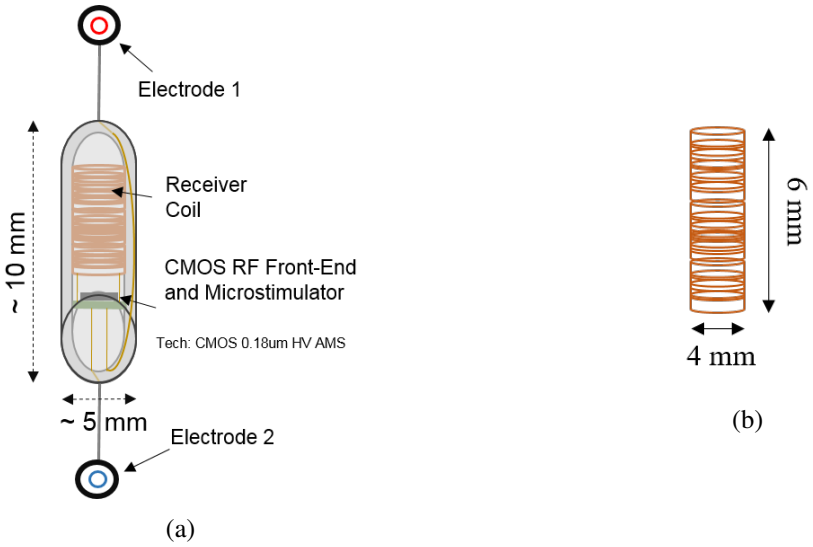


Figure 3.1: (a) Aspect of the implantable device and (b) of the receiver coil.

3.2 Low-Power Fully-Integrated 13,56 MHz CMOS RF Front-End Circuit

The fully integrated front-end block diagram of the implant proposed in [27] has been adopted here. It is composed of a full-wave bridge rectifier, two linear regulators and a BPSK demodulator to extract the clock and data.

3.2.1 CMOS Full-Wave Bridge Rectifier with Low-Substrate Leakage

The rectifier circuit acts as a a.c./d.c. voltage converter, being the full-wave rectifier preferred over the alternative simpler half-wave counter part because it uses both phases (positive and negative) of the signal and consequently there is a better usage of the input energy [28]. Thus, in the rectifier design a CMOS full-wave bridge rectifier with low substrate leakage was implemented using medium-voltage transistors, as shown in Figure 3.2. From [27], it is known that this configuration gives a better conversion efficiency than a conventional CMOS full-wave bridge rectifier [29] due to the reduced substrate leakage current.

According to the technical characteristics of the 0.18 μm 1P6M CMOS process adopted here, an N-well can be used to separate the NMOS rectifying transistors and an isolated P-well can be fabricated on a deep N-well process. As working principle, the rectifying transistors M_{p2} and M_{n2} conduct as soon as the voltage drop $V_{in-} - V_{in+} > |V_{THp2}|$ or $V_{in-} - V_{in+} > |V_{THn2}|$ occurs. The current is then delivered from the coil and via the load to ground. Similarly, the rectifying transistors M_{p1} and M_{n1} conduct when $V_{in+} - V_{in-} > |V_{THp1}|$ or $V_{in+} - V_{in-} > |V_{THn1}|$, and in contrast, the current is absorbed from the ground to the coil [27]. The additional auxiliary transistors M_{p3} to M_{p6} and (M_{n3} to M_{n6}) dynamically control the substrate voltage of M_{p1} and M_{p2} (M_{n1} and M_{n2}) to reduce the leakage current [29].

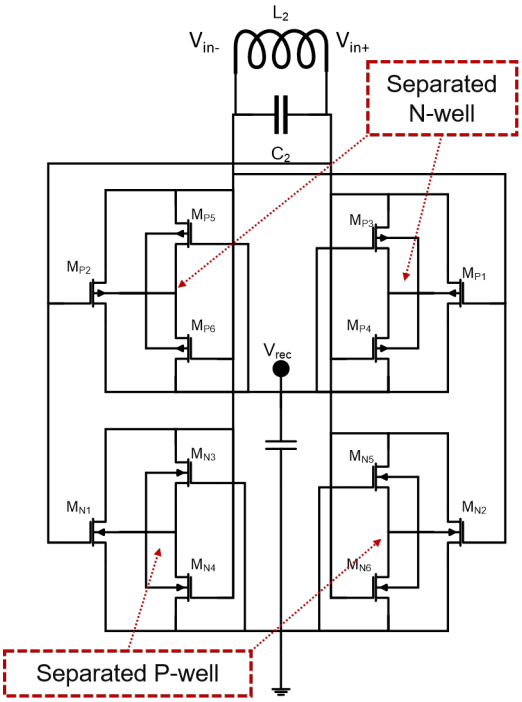


Figure 3.2: Proposed CMOS full-wave rectifier implemented in a 0.18 μm CMOS process.

Comparing with the work proposed in [27] and with the conventional rectifier [29] without leakage reduction, the simulation results in Figure 3.3, show that the implemented circuit can achieve higher output voltage and higher output current. An output rectifying capacitor C_{out} of 300 pF was chosen to be possible its integration on-chip. The simulations were performed under the same conditions as the previous works. The schematic of the implemented rectifier is shown in Figure A.3.

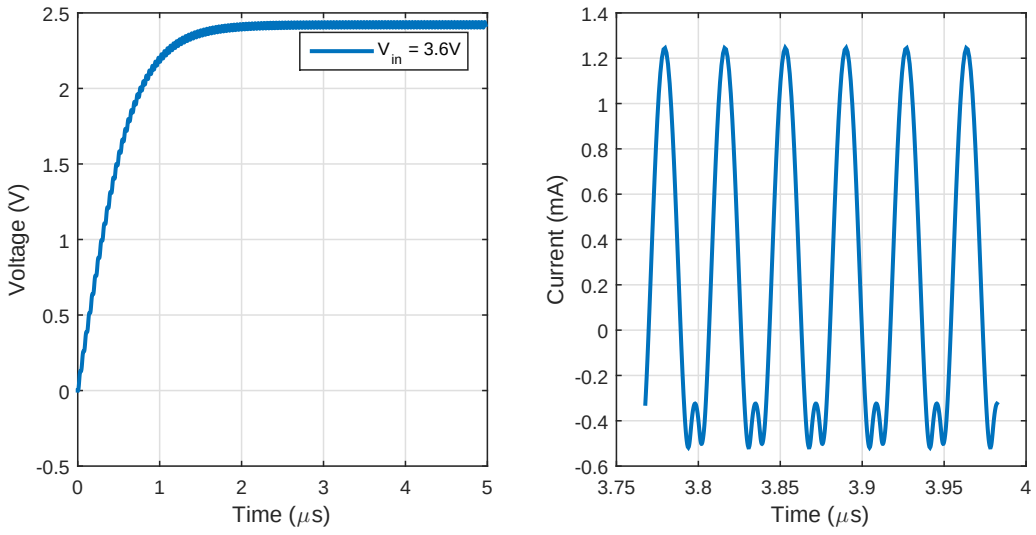


Figure 3.3: Performance of the implemented rectifying circuit.

This rectifier achieves a rectified voltage (V_{rec}) of 2,42 V with a ripple of 35,12 mV and an output current of 1,23 mA, with a settling time of 3 μs for an input voltage of 3,6 V. The performance summary and the comparison with previous works are shown in Table 3.1.

Table 3.1: Performance and comparison summary.

References	**[13]**	**[14]**	**Work**	**This Work**
Process (CMOS) [μm]	0,18μm	0,5	0,18	0,18
Carrier Frequency [MHz]	13,56	13,56	13,56	13,56
Input Voltage Range [V]	0,8	3,8	3,6 - 4.8	4,2 - 8
Output Voltage Range [V]	1,8	3,12	2,3 - 3	2,8 - 5,3
Loading Resistance [Ω]	270	50	10k	10k
Power Conversion Efficiency [%]	54,9	80,2	70 - 87	69 - 85

3.2.2 Low-Power CMOS Linear Voltage Regulator

This d.c./d.c. converter circuit is designed to automatically regulate the variable output voltage of the rectifier stage (V_{rec}) to a stable voltage for the load (V_{DD}). A linear low-dropout (LDO) regulator, was preferred over a switching regulator because of the lower noise and smaller implementation area [28]. As small area is an important challenge in biomedical implants a linear regulator can be designed based on unconditional stability without the output capacitor implemented within the 0.18 μm CMOS process. This block was built using medium voltage transitors. The designed linear regulator, shown in Figure 3.4, includes a bias circuit, an error amplifier, a voltage buffer, a pole-zero tracker, a power MOS transistor, and Miller compensation stage as a feedback. The design of all these blocks will be described in the next sections. The implemented circuit comprises two similar blocks of the LDO in order to regulate the input voltage (V_{rec}) to two different output levels (V_{DD1} and V_{DD2}). V_{DD1} is a low-voltage supply of 1,8 V that will be used to supply the analogue/digital circuitry, excluding the microstimulator circuit that will be powered by V_{DD2} with 2,5 V. A detailed schematic is shown Figure A.1.

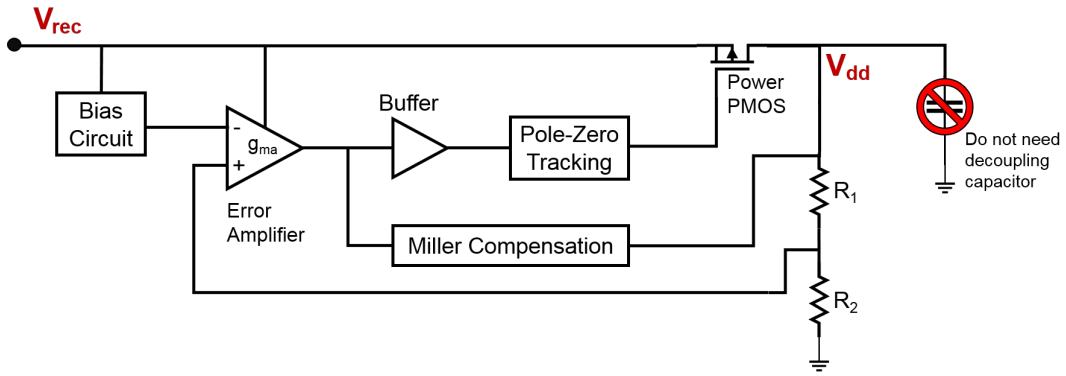


Figure 3.4: Block diagram of the capacitor-free LDO regulator.

3.2.2.1 Voltage Reference and Bias Circuit

A voltage reference circuit is required specifically to provide a voltage reference for the embedded low dropout (LDO) regulator. In this system, the power supply voltage variations are more important due to knee/leg movement than temperature variations because the device is implanted in the knee, thus a high-PSRR (Power Supply Rejection Ratio) low-power CMOS voltage reference based on the difference between weighted gate-to-source voltages (V_{gs}) of MOS transistors operating in the subthreshold region proposed in [30] was implemented. The present circuit does not have any passive element for scaling V_{gs} voltages as the resistors branch is replaced by at least another MOS transistor to weight one of the V_{gs} voltages, as shown in Figure 3.5. This method reduces the power consumption and improves the PSRR.

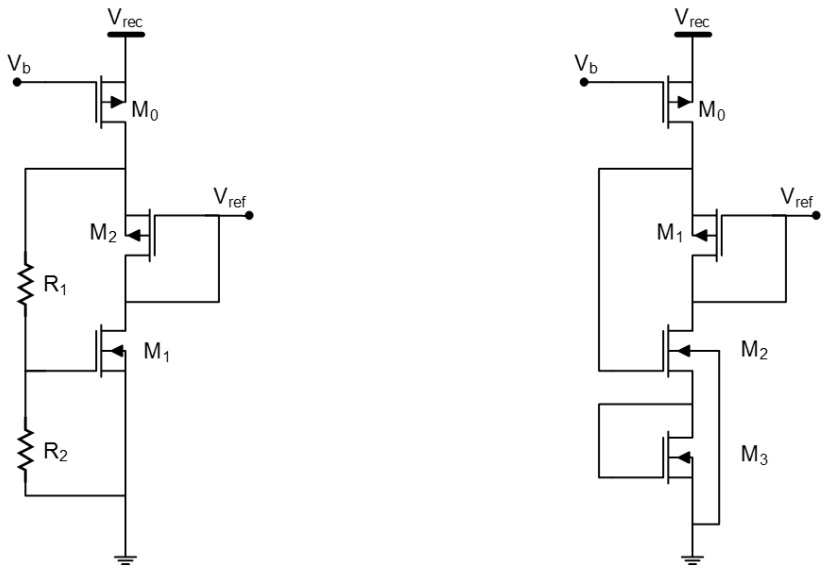


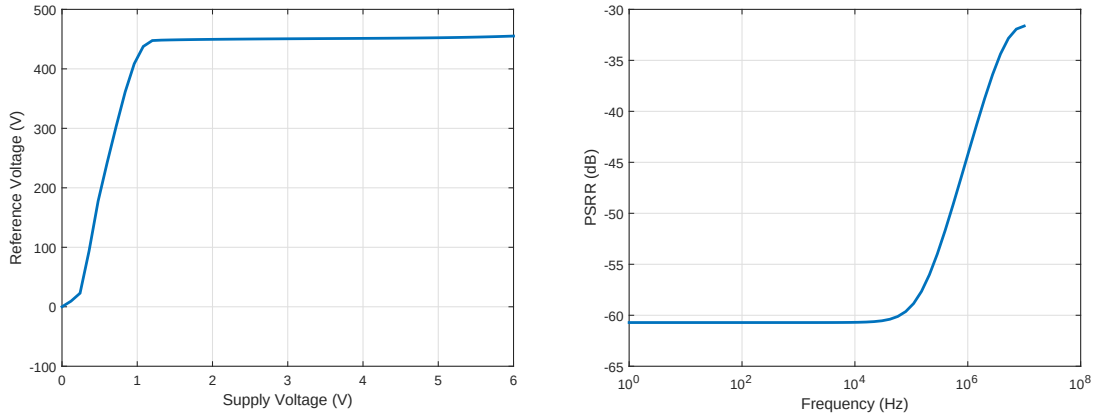
Figure 3.5: Simplified circuit of (a) the conventional and (b) the proposed voltage reference circuit.

The transistor M_0 delivers adequate biasing current to the circuit and V_b is generated by a biasing circuitry. The diode-connected transistor M_3 in series with M_1 and M_2 provides a weighting factor for V_{gs} for NMOS transistors without the resistive branch. The reference voltage is given by:

$$V_{ref} = V_{gs3} + V_{gs2} - |V_{gs1}| \tag{3.1}$$

The schematic of the implemented voltage reference circuit, including the bias section and start-up circuit, drawn in Cadence Virtuoso environment is shown in Figure A.4. Some circuit simulations were performed in order to evaluate its operation.

The transfer characteristic of the reference voltage V_{ref} generator, as a function of the supply voltage, is shown in Figure 3.6a. It can be seen that for a variation of the input voltage in the range 2,8 to 5,3 V, the average reference voltage is 451,4 mV, with only a difference of 2,5 mV in all range of the supply voltage variation. The power supply rejection ratio of this voltage reference is shown in Figure 3.6b.



(a) (b)

Figure 3.6: (a) Transfer characteristic of the reference voltage generator and (b) its power supply rejection ratio.

3.2.2.2 Folded Cascode OTA as an Error Amplifier

The design of the feedback error amplifier is based on a folded cascode operational transconductance amplifier. This circuit is intended to sample the output voltage of the voltage regulator that is fed back and compared with the reference voltage, in order to control the gate of the power PMOS pass transistor to maintain a specified constant voltage at the output of the regulator. The chosen configuration is the folded cascode, as show in Figure 3.7a, due to its high gain, high bandwidth performance and high input and output swing [31].

To understand the operation of the folded cascode OTA, one can see that the input stage comprises a differential stage consisting of PMOS transistors M_1 and M_2, followed by a cascode Wilson current mirror as the active load. Transistors M_{11} and M_{12} provide the d.c. voltages to properly bias the M_7-M_{10} transistors [31].

The unity-gain frequency of the OTA is given by [32]:

$$UGF = \frac{g_{m1}}{I_D} \cdot \frac{I_D}{C_L} = \frac{g_{m1}}{C_L} \tag{3.2}$$

The open-loop voltage gain of the amplifier, taking into account the complementarity between transistors M_6 and M_8 (g_{m6}=g_{m8}) is given by [32]:

$$A_v = \frac{g_{m1} \cdot g_{m6} \cdot g_{m8}}{I_D^2 \left(g_{m6}.\lambda_P^2 + g_{m8}.\lambda_N^2\right)} = \frac{g_{m1}}{I_D} \cdot \frac{g_{m6}}{I_D} \cdot \frac{1}{\left(\lambda_P^2 + \lambda_N^2\right)} \tag{3.3}$$

where g_{m1}, g_{m6} and g_{m8} are the transconductances of transistors M_1, M_6 and M_8, respectively, I_D is the bias current, C_L is the load capacitance, λ_P and λ_N are the channel length modulation coefficients of, respectively, PMOS and NMOS transistors.

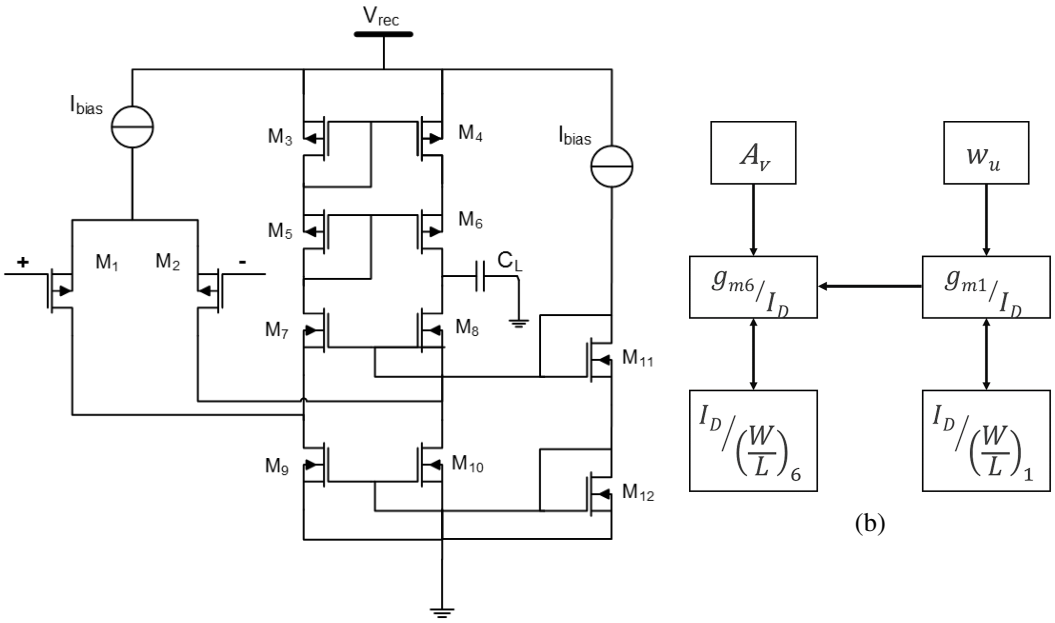


Figure 3.7: (a) Folded Cascode OTA schematic and (b) design flow for sizing algorithm.

In the folded cascode OTA design methodology, the aim is to determine values of the design parameters (e.g., transistor aspect ratios, bias currents and other component values) that optimize an objective feature, whereas satisfying the specifications. Figure 3.7b presents a top-down design flow methodology for CMOS OTA architectures [32] which follows a synthesis procedure based on the g_m/I_D methodology [33]. It starts by fixing the specifications to be optimized (Table 3.2) in order to determine the unknowns, i. e., the MOS transistors aspect ratios.

Table 3.2: Specifications.

Specifications	Values
I_D (nA)	700
A_v (dB)	80
UGF (MHz)	35
C_L (pF)	0,4
V_{rec} (V)	3
Channel length (μm)	0,5

Table 3.3: OTA design parameters.

Parameters	Values
$g_{m\,1,2}\,/\,I_D$ (V^{-1})	20
$I_D\,/\,(W/L)_{1,2}$ (nA)	48,6
$g_{m\,6}\,/\,I_D$ (V^{-1})	20
$I_D\,/\,(W/L)_6$ (nA)	140
$W_{1,2}$ (μm)	7,2
$W_{1,2}$ (μm)	7,2
$W_{3,4,5,6}$ (μm)	2,5
$W_{7,8,9,10,11,12}$ (μm)	7,5

After applying this design strategy, the computed parameters are obtained and summarized in Table 3.3. The transistors are biased in the saturation mode and operated close to weak inversion

(moderate inversion) to take advantage of the higher transconductance, larger gain with smaller current, low thermal noise and lower power consumption.

In order to evaluate the performance of this error amplifier, circuit simulations were carried out within the Cadence Virtuoso tool, using the circuit shown in Figure A.5. Figure 3.8 shows the open loop transfer characteristic of the error amplifier when one of the inputs is defined as a reference voltage of 450 mV and the other input is changed. The output changes from 0 V to V_{rec} when the input is higher than the reference. It can bee seen that the input voltage offset is very small — a value of 0,3 mV could be observed.

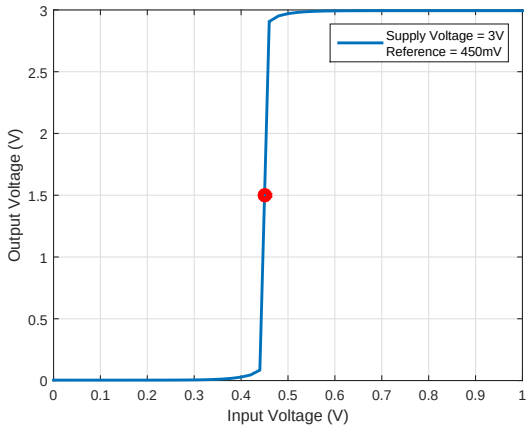


Figure 3.8: OTA transfer characteristic.

In Figure 3.9 the open loop phase and gain of the error amplifier are presented. From these it is possible to see that the error amplifier is stable because the phase and gain margin are, respectively, 60,7º and 22,9dB. The module of the gain response also reveals a d.c. gain of 87 dB and a unity-gain frequency of 30 MHz.

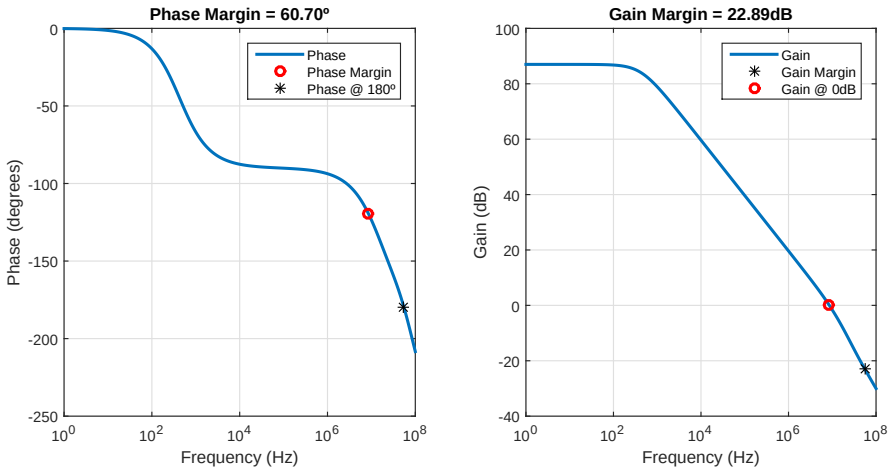


Figure 3.9: Open-loop phase and gain of the OTA.

3.2.2.3 Unconditional Frequency Stability without Output Capacitor

Figure 3.10 shows the conventional configuration of a linear regulator [27]. It can be seen that the loop gain is dominated by two poles and one zero given by Equations 3.4, 3.5 and 3.6. Is known that a larger output capacitor is usually required to ensure stability but, on the other hand, this implies larger implementation area, what is not suitable for this biomedical implantable device. Therefore, to optimize frequency stability, three frequency compensation techniques (Voltage Buffer, Pole-Zero Tracking and Miller Compensation) were evaluated to retain the frequency response independent of the load current and output capacitor [27].

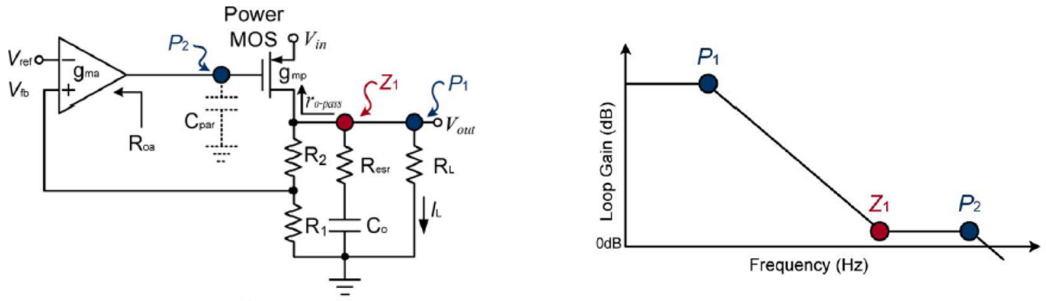


Figure 3.10: Typical poles and zero location of the loop gain of a conventional linear regulator.

$$P_1 = \frac{1}{[(R_L // r_{o-pass} // (R_1 + R_2)) + R_{esr}] \cdot C_o} \tag{3.4}$$

$$P_2 = \frac{1}{R_{oa} \cdot C_{par}} \tag{3.5}$$

$$Z_1 = \frac{1}{R_{esr} \cdot C_o} \tag{3.6}$$

where R_{oa} is the output resistance of the error amplifier, r_{o-pass} and C_{par} are the output resistance and the input capacitance of the p-type power MOS, respectively, R_1 and R_2 are two resistors in the voltage feedback network, C_o and R_{esr} are the output filtering capacitor and the equivalent series resistance, respectively, and R_L is the output load.

CMOS Source Follower as a Voltage Buffer

In order to reduce the size of the output capacitor C_o, the conventional regulator was improved with a voltage buffer implemented using a PMOS transistor in source-follower configuration, which is interposed between the output of the error amplifier and the gate of the PMOS pass transistor [34]. This technique decomposes the original pole P_2 in two higher-frequency poles P_{21} and P_{22} given by Equations 3.7 and 3.8, respectively. Thus, the unity-gain frequency (UGF) of the linear regulator could be increased (Figure 3.11). This is because the input capacitance and output resistance of the voltage buffer are much smaller than the input capacitance of the large power PMOS and than the output resistance of the error amplifier. Moreover, the value of C_{par} is usually quite large (due to the input capacitance of the power PMOS), therefore P_{21} is lower than P_{22} [35].

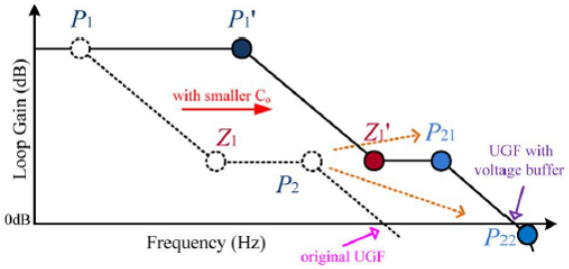


Figure 3.11: Poles and zero location of the loop gain with the voltage buffer.

$$P_{21} = \frac{1}{R_{buf} \cdot C_{par}} \tag{3.7}$$

$$P_{21} = \frac{1}{R_{oa} \cdot C_{buf}} \tag{3.8}$$

where C_{buf} and R_{buf} are the input capacitance and output resistance of the voltage buffer, respectively.

Pole-Zero Tracking

Linear regulators with poor frequency response performance, show limited load current (I_L) operation range due to their stability problem which deteriorates the transient response. The dominant pole P_1 has a strong relation with the load current, as it is shown in Equation 3.9 and, thus, the frequency response is weakened with decreased loading current. By introducing a tracking zero technique to cancel out the dominant pole P_1, the frequency response of the feedback loop becomes load current independent and, thus, the regulator performance is optimized over a larger load current range [36].

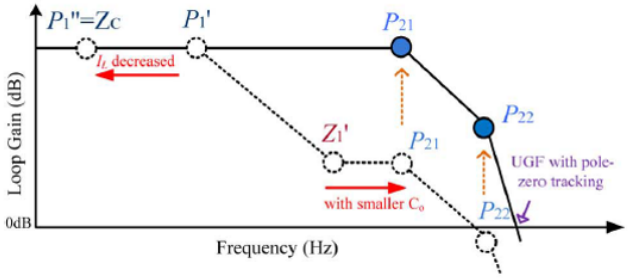


Figure 3.12: Poles and zero location of the loop gain with the pole-zero tracking.

$$P_1'' = \frac{\lambda \cdot I_L}{C_o} \tag{3.9}$$

where λ is the channel length parameter.

The concept of this technique is to move the series RC network used for compensation into the output node of the error amplifier. In order to have pole-zero cancellation, the position of the output pole P_1 and the compensation zero Z_c (given by Equation 3.10) should match each other [36].

$$P_1'' = \frac{1}{r_{o-pass} \cdot C_o} = \frac{1}{R_c \cdot C_c} = Z_c \tag{3.10}$$

where R_c is the internal resistor and C_c is generally an on-chip MIM capacitor in CMOS process, and their values are given by setting the relationships in equation 3.11.

$$R_c = r_{o-pass} \cdot K, \quad C_c = \frac{C_o}{K} \tag{3.11}$$

Being K a constant, the equality in equation 3.10 holds.

Miller Compensation

The application of the pole-zero tracking technique results in poor phase margin and it should be overcome by Miller compensation with a feedback capacitor C_m. Since the amplifier does have a two-pole behavior, this compensation is done by spliting the two poles (P_{21} and P_{22}) in order to impose the amplifier gain to drop at 20 dB/decade from the corner frequency down to 0 dB gain, or even lower. With this unconditional stability of the regulator is achieved by losing some accuracy.

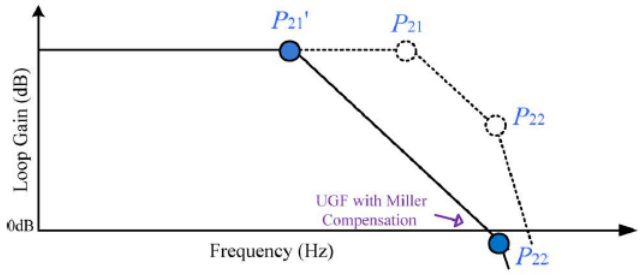


Figure 3.13: Poles and zero location of the loop gain with the Miller compensation.

3.2.3 BPSK Demodulation

The wireless neuromuscular stimulation micro-system receives a 13,56 MHz carrier waveform with the BPSK signal that powers the implantable device and conveys the modulated data to control the micro-stimulator circuit. A BPSK demodulator is implemented to detect the received BPSK signal from the internal coil and to translate the recovered clock and data to the system controller of the micro-stimulator circuit.

A BPSK demodulator based on a squaring loop architecture, as shown in Figure 3.14, featuring an asynchronous design requiring low circuit area and lower power consumption, fundamental requirements of a battery-less implantable device like this one, was implemented. The delay T is applied to lock the carrier signal $A_c \cdot cos(\omega t)$ from the input BPSK modulated signal $A_m \cdot m(t) \cdot$

$cos(\omega t)$. After, the mixer and the low-pass filter (LPF) can extract the demodulated signal $m(t)$ containing the data information.

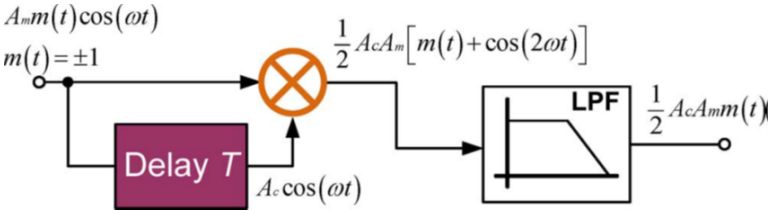


Figure 3.14: Block diagram of the BPSK demodulator with a squaring loop architecture.

Firstly, a voltage divider may be necessary to reduce the voltage levels of the received BPSK signal in order to fit the voltage limit imposed by the supply for the operation of the demodulator. At the input of the BPSK demodulator, a Schmitt trigger S_3 with adjustable hysteresis formats the received BPSK signal into a digital bit stream data. Next, a phase detector and a delay cell (DL_A) with $3T_1/4$ delay are employed to lock the carrier clock. The XNOR gate mixes the inverted digital input data and the carrier clock from the phase detector to extract the demodulated signal. As the input signal of the XNOR gate are asynchronous, a jitter occurs at the output. To prevent the jitter from deteriorating the function of the bi-phase signal in the output of the filter (DFF_3), a delay cell (DL_B) with $T_1/8$ delay controls the clock of the D flip-flop (DFF_3) to extract the bi-phase signal containing the data information. The recovered clock (from node 3) and data will serve as input of the FSM and of the shift register that will control the stimulation. The block diagram of the BPSK circuit is shown in Figure 3.15.

The delay times of the delay cells (DL_A and DL_B) are determined by adjusting the respective R and C values using the relationship shown in equation 3.12.

$$V_{iH} = V_{DD1}\left(1 - e^{-t/RC}\right) \tag{3.12}$$

where $t = 3T_1/4$ for the DL_A and $t = T_1/8$ for DL_B, T_1 is the period of the clock frequency of 13,56 MHz, V_{DD1} is the supply voltage of 1,8 V, and V_{iH} is the low to high threshold voltage of the Schmitt trigger, and therefore

$$RC = \frac{-t}{ln\left(1 - \frac{V_{iH}}{V_{DD1}}\right)} \tag{3.13}$$

The Table 3.4 presents the sizes of the transistors in the delay cells as well as the values for the resistors and capacitors. A detailed schematic of the BPSK demodulator is shown Figure A.7 and the simulation results of this block is shown in 3.14.

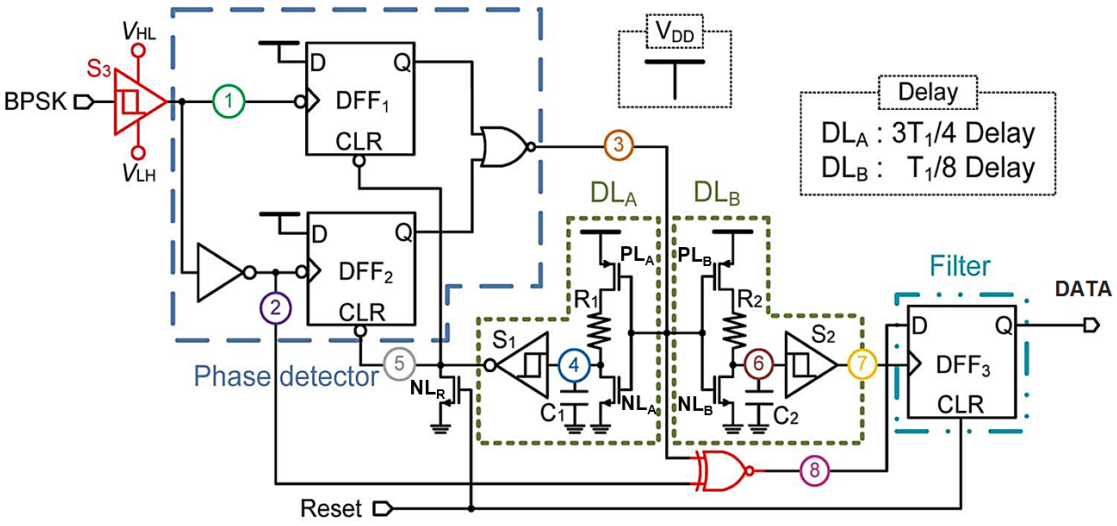


Figure 3.15: BPSK demodulator circuit diagram.

Table 3.4: Design parameters of the BPSK demodulator.

Parameter	Value
$(W/L)_{PL_A}$ (μm)	6 / 0,18
$(W/L)_{NL_A}$ (μm)	2 / 0,18
$(W/L)_{PL_B}$ (μm)	1,5 / 0,18
$(W/L)_{NL_B}$ (μm)	0,5 / 0,18
$(W/L)_{NL_R}$ (μm)	0,5 / 0,18
R_1 (kΩ)	7,7
C_1 (pF)	12
R_2 (kΩ)	1
C_1 (pF)	1

3.2.4 Simulation Results

The implemented LDO regulator, incorporating the three frequency compensation techniques, shows unconditional stability and at the same time wideband characteristics. This gives two stable levels of output voltages (V_{DD1}=1.8 V and V_{DD2}=2,5 V) regardless of the variation of the input voltage (V_{rec}) in the 2,8 V and 5,3 V range, or variations of the load current from 0 mA to 1 mA. The simulations were performed in Cadence Virtuoso and the schematic is shown in Figure A.6.

Figure 3.16 shows the open loop frequency response of the LDO for an output voltage of 1,8 V, using the referred frequency compensation techniques. From here, it can be seen that the regulator is stable since it shows a phase margin of 60º and a gain margin of 37 dB. The line and load transient responses depicted in Figures 3.17 and 3.18 show that the implemented LDO provides stable output voltages (2,5 V and 1,8V) regardless of the changes in the input voltage (V_{rec}) from 3 V to 5,5 V, or the deviation in the load current from 0 mA to 1 mA. Figure 3.19 shows the power supply rejection ratios for the two output voltages.

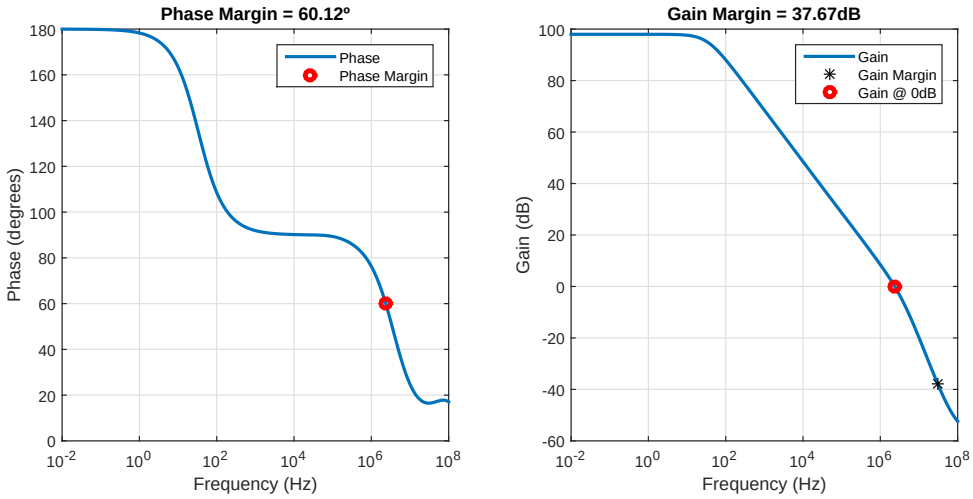
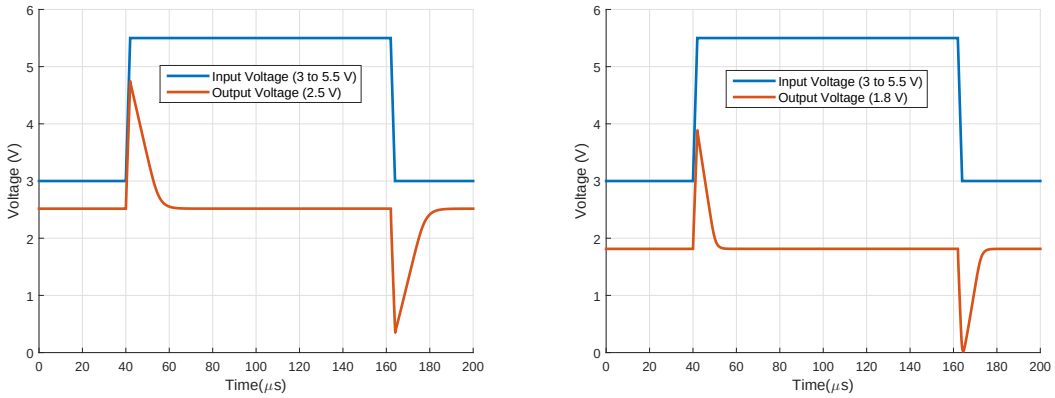
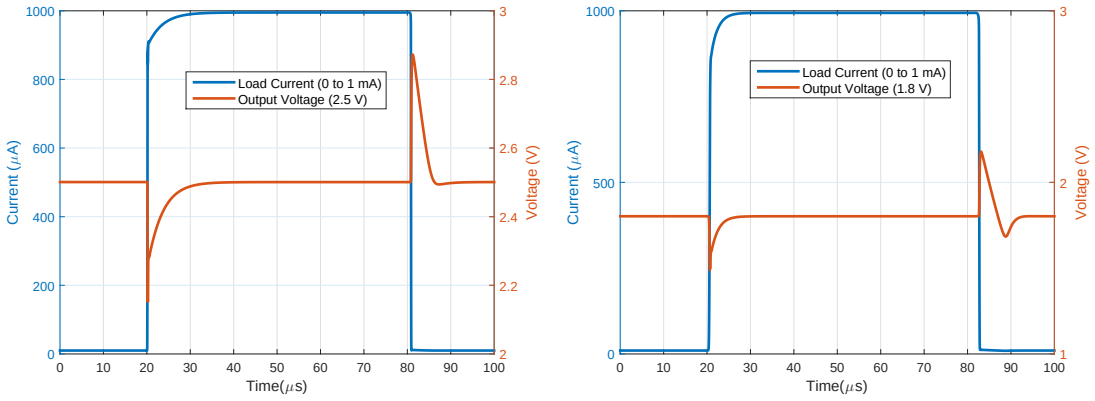


Figure 3.16: Loop response of the implemented LDO.



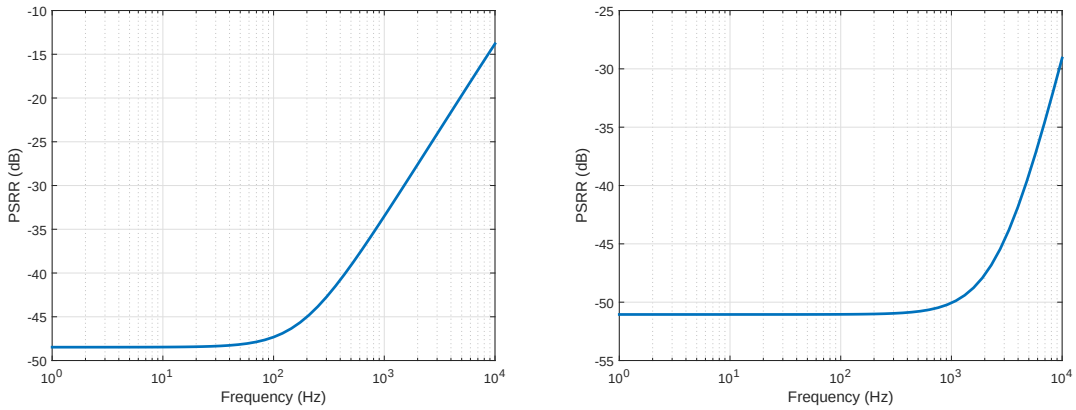
(a) (b)

Figure 3.17: Line transient response for a regulator output voltage of (a) 2,5 V and (b) 1,8 V.



(a) (b)

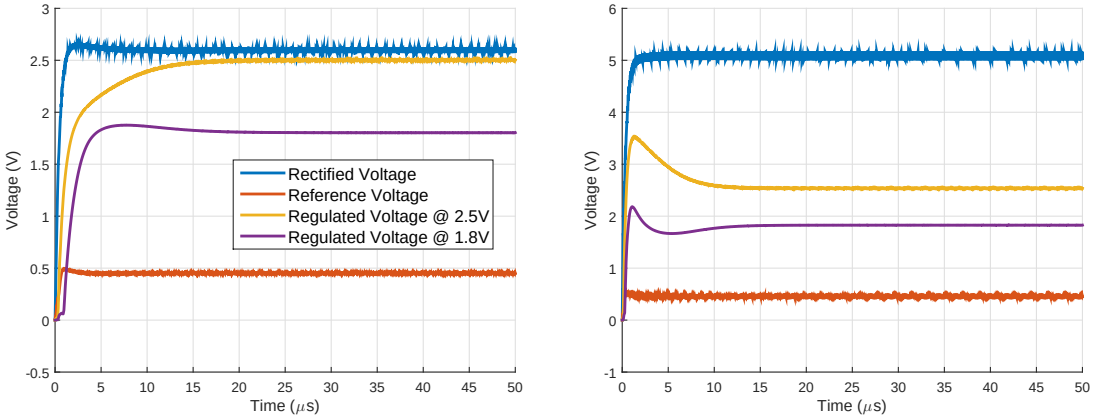
Figure 3.18: Load transient response for a regulator output voltage of (a) 2,5 V and (b) 1,8 V.



(a) (b)

Figure 3.19: Power supply rejection ratio for the regulator output voltage of (a) 2,5 V and (b) 1,8 V.

Figure 3.20 shows the overall system operation (rectifier and two regulators) for the range of input voltages of the rectifier from the secondary coil of 4,2 V_{pp} to 8 V_{pp}. It is possible to observe that the regulator maintains the output voltages constant in 2,5 V and 1,8 V despite the supply voltage variations. This system has also a fast settling time of only 20 μs for the minimum input voltage in the receiver coil.



(a) (b)

Figure 3.20: Operation of the power supply circuit — rectifier and voltage regulators — for two voltage levels at the secondary coil (a) 4.2 V_{pp} and (b) 8 V_{pp}.

The Figure 3.21 shows the overall operation of the BPSK demodulator implemented in Cadence software (Figure A.7) to recover the clock and data to control the implantable microstimulator circuit.

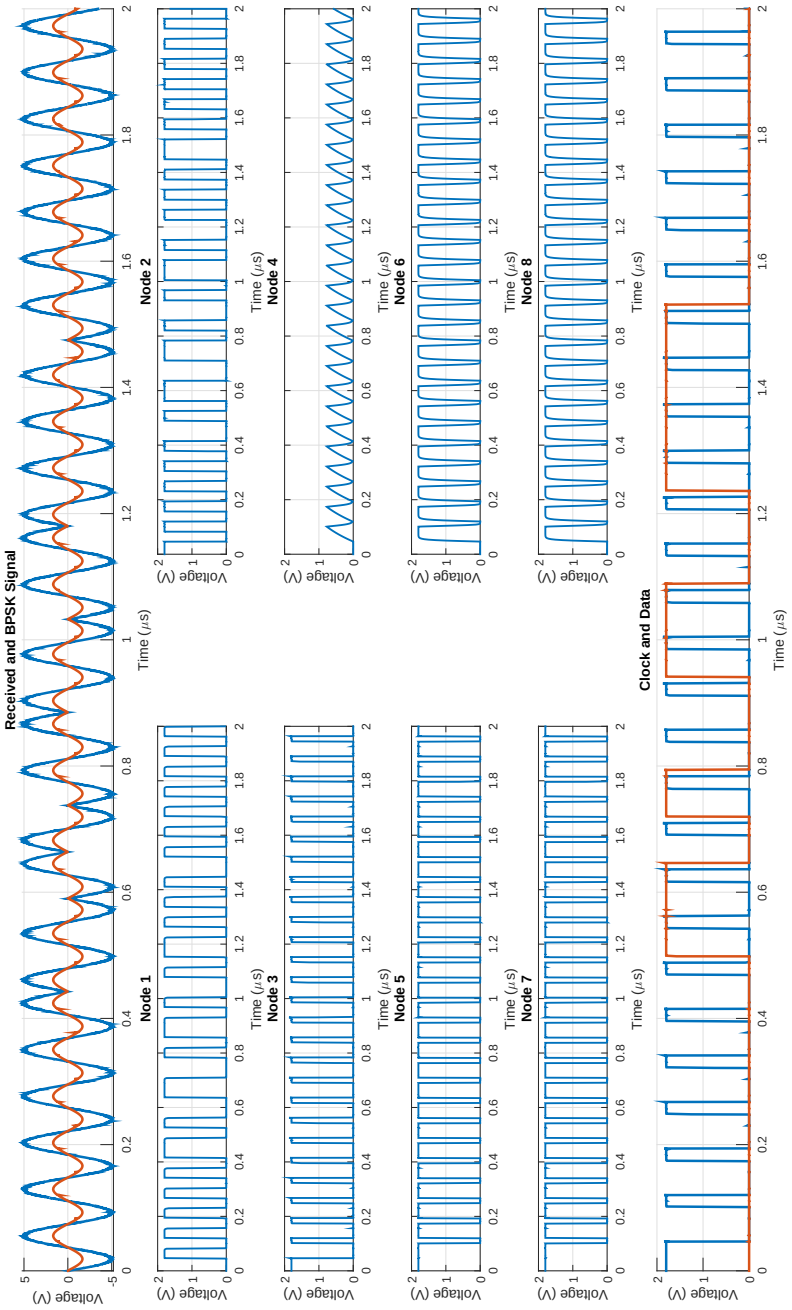


Figure 3.21: Circuit operation of the BPSK demodulator circuit (Figure 3.15).

3.3 Micro-stimulator Circuit

3.3.1 Stimulation Strategy

The stimulation strategy being followed here is based on the neuromuscular stimulation approach adopted for the quadriceps and hamstrings to recover from cruciate ligaments reconstruction [6]. As this work is a novel method of directly stimulation of the new ligament through an implantable device, this work will follow the same stimulation pattern of the other devices for NMES on quadriceps/hamstrings with a small adjustment on stimulation intensity.

According to [5], the use of monophasic and biphasic waveforms, instead of polyphasic (Russian stimulation) waveform, reveals greater quadriceps femoris muscle torque and also less fatigue. Taking into account both stimulation waveforms, the charge balanced biphasic with interphase delay stimulation waveform, as shown in Figure 3.22, was chosen. In biphasic pulsing, the stimulating (first) phase, is used to elicit the desired physiological effect and the reversal (second) phase is used to reverse electrochemical processes occurring during the stimulating pulse, in order to ensure that there is zero net charge transfer at the end of each stimulation cycle. Biphasic waveform is more efficient than monophasic in preventing tissue damage, thanks to the reverse of the electrochemical processes [37]. An open circuit inter-phase delay (ID) of 50 μs is interposed between the phases in order to give more time to the tissue to remain depolarized, and thus to increase the stimulation effects.

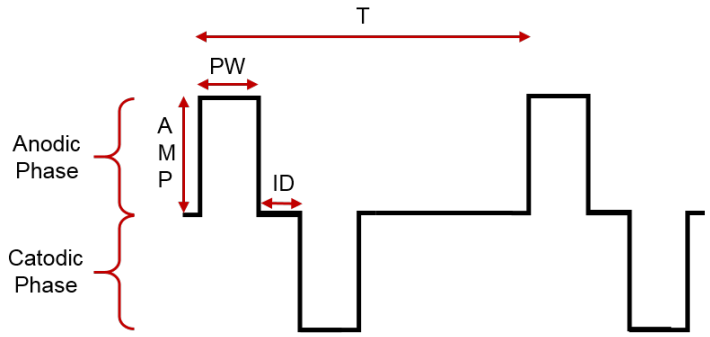


Figure 3.22: Proposed stimulation waveform.

Despite of the stimulation waveform, there are some stimulation parameters, such as intensity/amplitude (AMP), pulse width (PW), stimulation period (T) and stimulus duration (T_{ON} and T_{OFF}), that can be adjusted to produce different effects. These stimulation parameters are programmed by a 6-bit word coming from the external device, which is handled by the doctor. As the main concern here is to recover a patient or athlete as fast as possible from the ligament reconstruction, adjusting the parameters of stimulation will depend on the recovery phase the patient is at the moment. In early stages of the rehabilitation, lower stimulation pulses (200 μs) at low stimulation frequencies (20 Hz) should be used for muscle endurance of the weakened muscles, as they produce low force. At the end of the rehabilitation, higher stimulation pulses (400 μs) at higher stimulation frequencies (40-50 Hz) are required to produce stronger contractions for

muscular strengthening. The stimulus duty-cycle (on and off stimulus times) is related to muscle fatigue, thus larger rest time proportion (1/8) are advised for weaker muscles to allow stimulation with minimal change of fatigue, afterwards rest time could be reduced [7]. The aspect of the stimulus wave train that will flow through the tissue is presented in Figure 3.23.

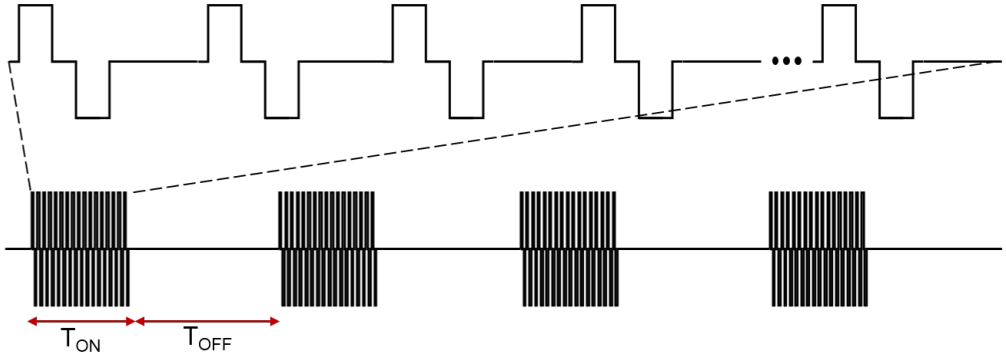


Figure 3.23: Stimulus wave train.

3.3.2 Electrode-Ligament Interface

Concerning the load of the stimulator, the electrode-ligament tissue interface (ETI) can be modelled using the equivalent electrical circuit shown in Figure 3.24.

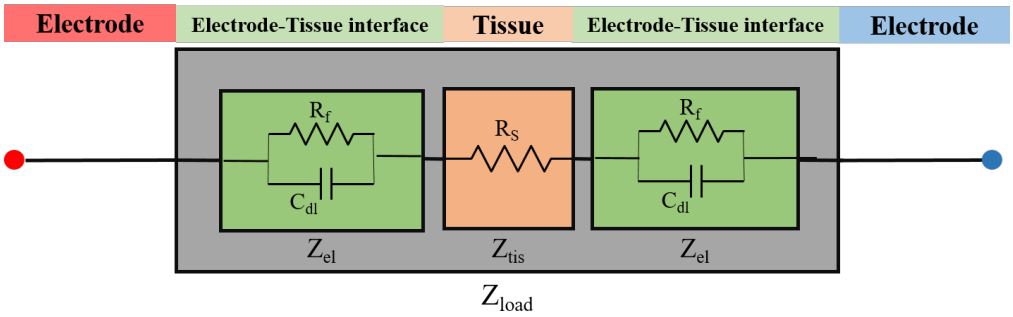


Figure 3.24: Equivalent electrical model of the electrodes and nerve (or tissue) interface.

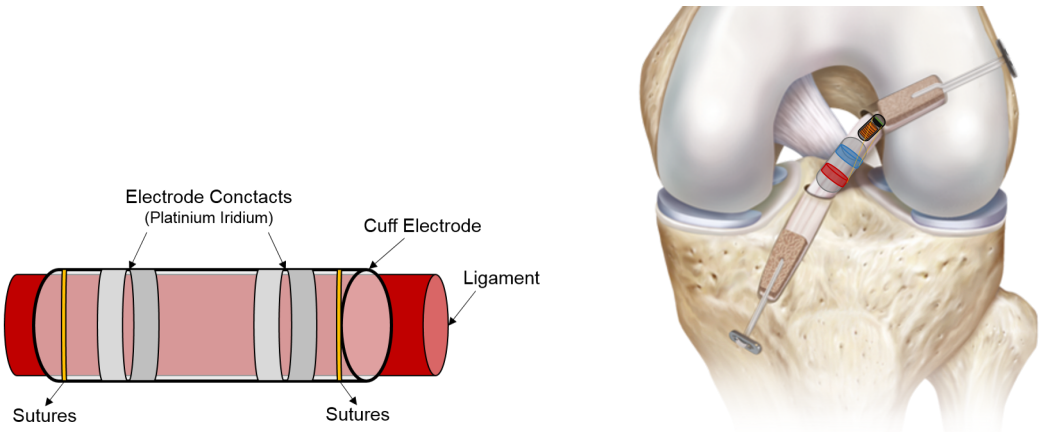
At the ETI, two types of interactions take place between the electrons in the electrodes and the ions in the tissue: charge accumulation and electrochemical reactions, which can be represented by the equivalent electrical model after changing the values of the components.

The ETS is characterized by two mechanisms. Firstly, reversible (non-faradaic) currents are characterized by the fact that they store charge at the interface (no charge is transferred between the electrode and tissue), but the stored charge can be recovered by reversing the electrical current, and this process is modeled with a capacitor C_{dl}. Secondly, irreversible (faradaic) currents are characterized by the electrochemical (oxidation and reduction) reactions in which the reaction products cannot be reversed, and this process is modeled with a charge transfer resistor R_f [38], [37]. The values of C_{dl} and R_f highly depend on the size, geometry and materials used for

electrodes. Besides the electrode size, the tissue impedance also depends on the tissue properties. In many cases the tissue is simply modeled using only a resistor R_s. In electrical stimulation of excitable tissue, it is desirable to have a large reversible charge storage capacity so that a relatively large amount of charge may be injected (being thus efficient for stimulation) prior to the onset of irreversible faradaic reactions (which may be deleterious to the tissue being stimulated or to the electrode itself) [37].

3.3.2.1 Design of the Electrodes

Evaluating all the available electrodes configurations, the cuff electrode adopting bipolar configuration with two contacts, shown in Figure 3.25a, was chosen as the best configuration to deliver the stimulus pulses to the tissue, since they can be placed and tied around the ligament with sutures achieving better stimulation efficiency and not affecting the functionality of the ligament. The placement of the cuff electrodes and the implantable device in the graft after surgical operation is shown in Figure 3.25b.



(a) (b)

Figure 3.25: (a) Cuff electrodes with two Platinum-Iridium contacts, (b) Placement of the electrodes and the implantable stimulator device in the graft.

The cuff electrode must respect size constraints (mean length of 15 mm and width of 9 mm [2]), which is the average dimensions of the graft that is not attached to any of the bones (i. e., that stands in free space inside the knee), thus has to be customized with a length of 10 mm and diameter of 10 mm of diameter. Electrode contacts made of platinum will be used due to the large reversible charge storage capacity of this material and thus to reduce the likeness of the onset of irreversible faradaic reactions. In this application, bipolar stimulation will be followed and thus during the cathodic phase of biphasic stimulation current is sourced through the working electrode while simultaneously sunk through the counter electrode and vice-versa in the anodic phase. It has the advantage of the voltage swing range across the physiological medium is V_{dd2}.

3.3.2.2 Load Impedance

Based on several studies [39], [40], [41], the impedance that models the ETI and tissue of the two-electrode system for this type of applications could be estimated to be in the range between 500 Ω and 5 kΩ. For simplicity, is assumed that R_f has a large value (>1MΩ) during stimulation and can be neglated and thus the load Z_{load} can be modeled as a RC series impedance in the range of R_s=0.5∼3kΩ, C_{dl}=20∼50nF. Thus, a voltage supply (V_{DD2}) of 2,5 V is needed to accommodate the maximum stimulation current required (140 μA) through the maximum load expected.

3.3.3 Stimulation Control Unit

The single-channel stimulator can be programmed by a frame of 6 bits, that defines stimulation amplitude/intensity (2 bits), stimulation frequency (2 bits), pulse width (1 bit) and “on” and “off” stimulus times (1 bit). This frame is sent associated to other four bits to automatically synchronize the demodulator and a 8-bit message (header) to establish communication with the external controller, resulting in a 18-bit message word, as shown in Figure 3.26, sent by the external device. When the complete programming word is received, the stimulation is triggered. In normal operation the external programmer sends only the carrier to power the implant while stimulating the new ligament via electrodes. The micro-stimulator comprises six main blocks: 1) a finite-state machine (FSM) that detects the beginning of the data communication; 2) a serial to parallel data converter; 3) registers and frequency dividers; 4) a digital stimulus generator (DSG); 5) a bipolar programmable current source; and 6) a switching circuit (SC). The bipolar programmable current source and the switching circuit will be powered with a supply V_{DD2} of 2,5 V and the other circuitry will be powered with a low-voltage supply V_{DD1} of 1,8 V.

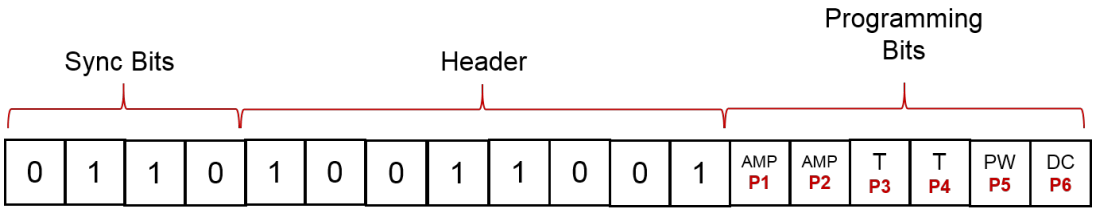


Figure 3.26: 18-bit message word.

The global controller of the stimulator circuit is composed by an FSM, shown in Figure 3.27, that controls all the operation of the stimulator, from the receiving of the stimulation parameters to the generation of stimulus to be applied to the tissue. Data is sent in 18-bit message words as shown before in Figure 3.26.

In the design of this FSM, JK flip-flops (FF) were used in order to reduce the associated logic circuit, since the number of logic gates used are reduced compared to when using the D type FF. From the FSM diagram depicted above a state table with JK FF excitations was elaborated. Resorting to Karnaugh maps the circuit for the FSM was implemented. The Karnaugh maps for the JK FF and for the output variable ’ENB’ are shown in logic Equations 3.14, 3.15, 3.16, 3.17, 3.18, 3.19.

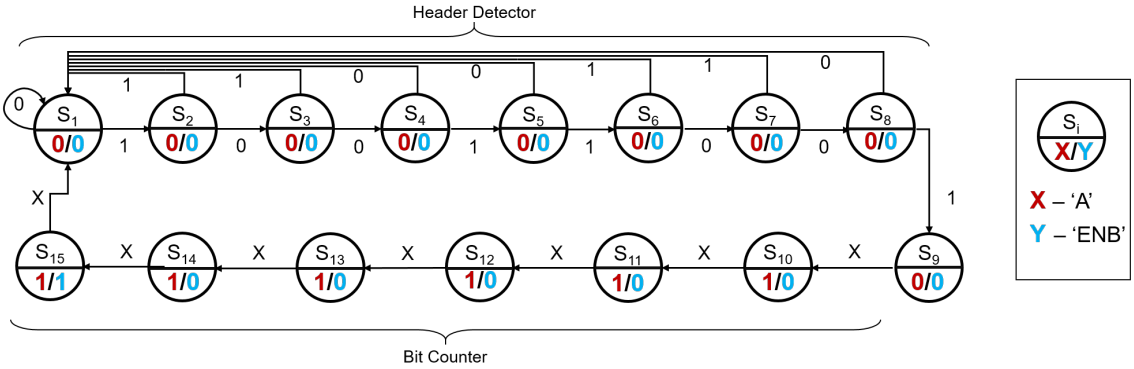


Figure 3.27: Finite state machine.

$$\begin{cases} J_A = B \cdot C \cdot D \cdot I \\ K_A = B \cdot C \end{cases} \tag{3.14}$$

$$\begin{cases} J_B = C \cdot D \cdot I + A \cdot C \cdot D \\ K_B = C \cdot I + C \cdot D + A \cdot C \cdot + \bar{A} \cdot D \cdot I + \bar{A} \cdot \bar{C} \cdot \bar{D} \cdot \bar{I} \end{cases} \tag{3.15}$$

$$\begin{cases} J_C = D \cdot \bar{I} + A \cdot D \\ K_C = D + \bar{A} \cdot I + A \cdot B \end{cases} \tag{3.16}$$

$$\begin{cases} J_D = \bar{C} \cdot I + A \cdot \bar{B} + A \cdot \bar{C} + \bar{A} \cdot C \cdot \bar{I} \\ K_D = 1 \end{cases} \tag{3.17}$$

$$ENB = A \cdot B \cdot C \cdot \bar{D} \tag{3.18}$$

$$A = A \cdot \bar{B} \cdot D + A \cdot C \cdot \bar{D} + A \cdot B \cdot \bar{C} \tag{3.19}$$

The optimized FSM implemented here receives the data and clock extracted by the demodulator in the RF front-end and comprises two block sequences, an header detector and a 3-bit counter. When data is sent, the FSM detects the header (10011001) that activates the communication between the exterior and the implant. Once the header is detected the FSM activates the output ('A') and the serial data received is converted into parallel data by means of a 6-bit shift register SIPO, as shown in Figure 3.28. A 3-bit counter is used to count the number of programmable bits and when the sixth bit is detected a pulse ('ENB') is sent to latch the data to an output register, being these values kept constant till new data is received. The outputs of the register are connected to a 2-bit current source and to the DSG that generates the control signals to be applied to the switching array in order to produce the desired stimulation pattern.

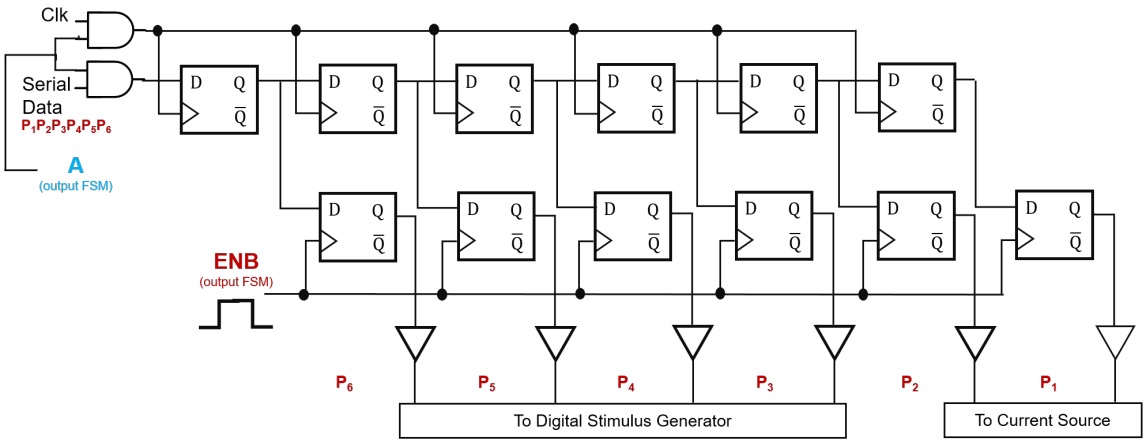


Figure 3.28: 6-Bit shift register with output latches.

3.3.4 Programmable Current Source

A current mode stimulator was preferred over a voltage stimulator because the amount of charge injected into the tissue can easily be defined by the current amplitude and the duration of the pulses ($Q_{injected} = I_{stim} * t_{PW}$), since the action potential is initiated when the charge injected goes over a certain threshold [37]. In order to ensure a charge-balanced stimulation during every stimulation cycle, a single current source from a single supply is adopted here. A switch array is used to reverse the current direction and generate the biphasic stimulation waveform.

Several current mode stimulators based on a current mirror circuit and wide-swing and regulated cascode current mirror have been reported, but they show limitations on the voltage compliance. The implemented current source, shown in Figure 3.29, includes a 2-bit current mode digital-to-analogue converter (DAC) employing double-loop negative feedback, which increases the output impedance of the current generator, maximizes the voltage compliance of the output transistor (PM_1), and achieves more voltage headroom (V_L) at the tissue which represents more charge that can be conveyed into the tissue [42].

The first feedback loop of this current source is used to force the drain terminals of PM_1 and PM_2 to be equal, resulting in a high precision down scaling of the current ($I_{fb} = I_{stim}/m$). The amplifier A_v was implemented using a standard differential amplifier with an active load as depicted in Figure 3.30, and an offset voltage source was interposed between the output of the amplifier and the gate of PM_3 in order to bias it properly. The current I_{fb} is compared with I_{DAC} resulting in an error current (Equation 3.20) that flows into the transimpedance amplifier (Z_m) that converts the current error into the voltage needed at the gate of PM_1 to produce I_{stim}.

$$I_e = \frac{I_{stim}}{m} - I_{DAC} \tag{3.20}$$

where,

$$I_{DAC} = n \cdot I_{ref} \tag{3.21}$$

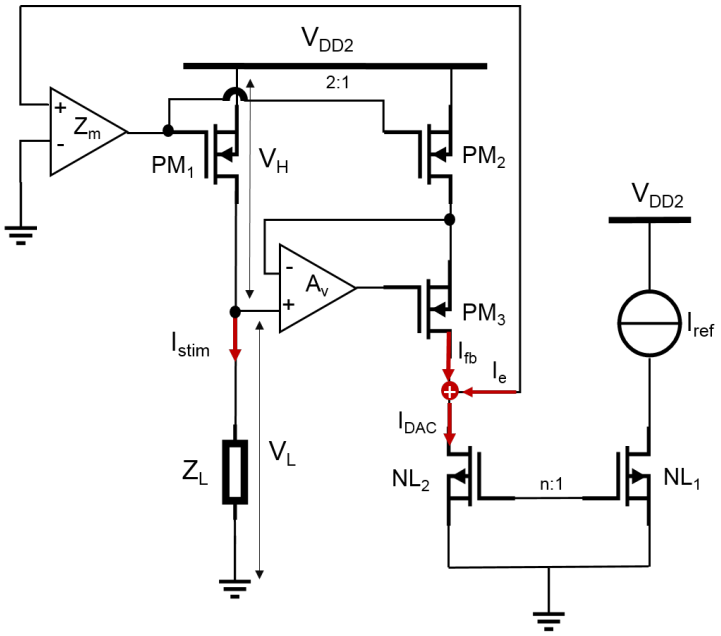


Figure 3.29: Implemented current source.

A large Z_m is required to set a large loop gain and, thus, I_e will be forced to be zero, creating a relationship of Equation 3.22. A large Z_m is the main part that we can play to make the loop gain as large as possible, so it defines the accuracy of this current source.

$$I_{stim} = m \cdot n \cdot I_{ref} \tag{3.22}$$

The amplitude of the current source (I_{stim}) is defined by scaling a reference current (I_{ref}) by a factor of n of NL_2 and then by a factor of m which is constant and equal to 2. To make the factor n programmable, NL_2 is programmable using a binary-weighted current-steering DAC scheme. The current source delivers a minimum of 20 μA and a maximum of a 140 μA stimulation current with a resolution of 40 μA. The reference current (I_{ref}) and the current source I_s were set to 5μA and 2μA, respectively, and these bias sources can be switched off when stimulation is not active, yielding very low static power consumption. The voltage supply (V_{DD2}) for the stimulation circuit is set to 2,5 V in order to give enough voltage headroom to accommodate the maximum current required (140 μA) through the maximum expected load (5 kΩ) and the voltage drop in the switching array of about 500 mV. The circuit diagram of the implemented stimulator is shown in Figure 3.30. This requires the use of medium-voltage transistors (NM_x and PM_x) combined with low-voltage transistors (NL_x and PL_x).

The aspect ratio of the transistors and the values of the voltages and current sources used in the implemented current source are presented in Table 3.5.

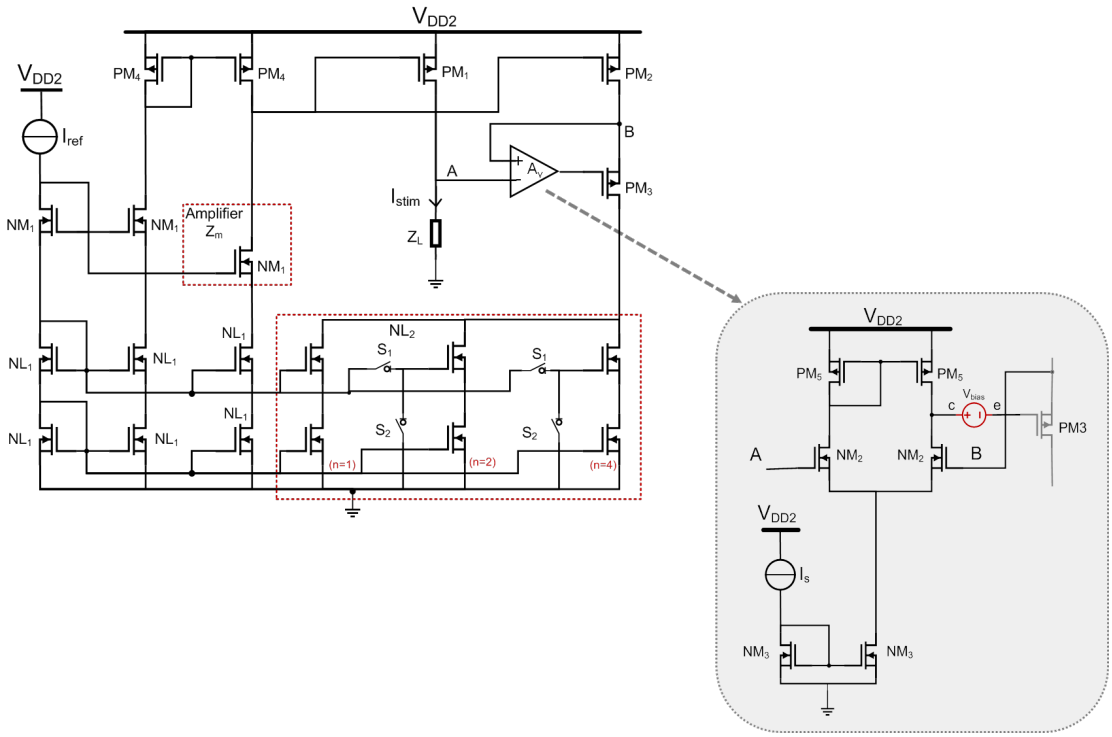


Figure 3.30: Circuit diagram of the implemented programmable current source.

Table 3.5: Design parameters of the 2-bit programmable current source.

Parameter	Value
$(W/L)_{NL_1}$ (μm)	0,5 / 0,18
$(W/L)_{NL_2}$ (μm)	1 / 0,18
$(W/L)_{NM_1, NM_3, PM_2, PM_3, PM_4}$ (μm)	6 / 0,7
$(W/L)_{PM_1}$ (μm)	11 / 0,7
$(W/L)_{PM_5}$ (μm)	4 / 5
$(W/L)_{NM_2}$ (μm)	5 / 5
I_{ref} (μA)	5
I_S (μA)	2
V_{bias} (V)	0,45
V_{DD2} (V)	2,5

3.3.5 Clock Generation

A global clock (Clk_0) of 10 kHz, generated using a CMOS current-starved VCO with several stages of inverters and with a capacitor (C_L) at the output of each stage was implemented [43], as shown schematically in Figure 3.31. MOSFETs PL_{inv} and NL_{inv} operate as an inverter while PL_{bias} and NL_{bias} operate as current sources limiting the current available to the inverter. This circuit was implemented using low-voltage transistors (NL_x and PL_x) in order to minimize circuit area and power consumption. This topology was chosen in order to generate a low frequency clock, since the current that flows to each inverter is voltage controlled by Vp_{bias} and Vn_{bias} and, thus, lowering the current increases the propagation time between each stage. The addition of the capacitor C_L

at the output of each stage also raises the propagation delay, but here there is a trade-off between increasing the propagation time and the increase of circuit area imposed by larger capacitances. The propagation delay is inversely proportional to the current that flows in the inverter (I_{inv}) and directly proportional to the value of C_L, as shown by Equation 3.25 [43], [44]. The aspect ratios of the transistors may have also to be taken into account. The circuit parameters and width of the transistors are presented in Table 3.6. All the transistors have the minimum length of 180 nm.

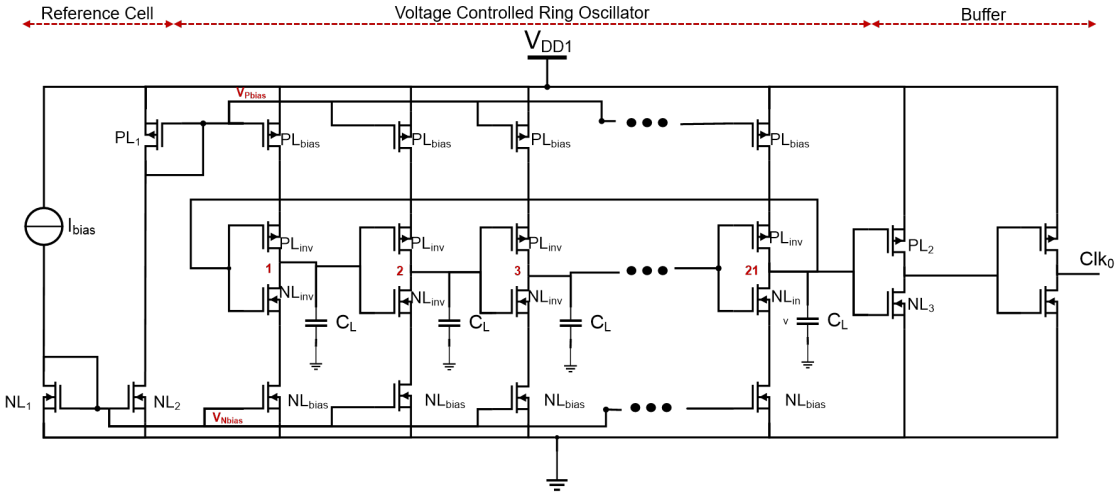


Figure 3.31: CMOS current starved ring oscillator.

Table 3.6: Design parameters of the current-starved ring oscillator.

Parameter	Value
W_{NL_1} (μm)	20
W_{NL_2} (μm)	0,5
W_{PL_1} (μm)	3
$W_{PL_{bias}}$ (μm)	1,5
$W_{NL_{bias}}$ (μm)	0,5
$W_{PL_{inv}}$ (μm)	6
$W_{NL_{inv}}$ (μm)	2
C_L (pF)	0,1
I_{bias} (μA)	1
V_{DD1} (V)	1,8

The total capacitance on the drains of PL_{inv} and NL_{inv} is given by:

$$C_{tot} = C_{out} + C_{in} + C_L = \left(\frac{5}{2} \cdot C'_{ox} \cdot (W_p L_p + W_n L n)\right) + C_L \tag{3.23}$$

The propagation delay of each inverter is simply the sum of t_1 (the time it takes to charge C_{tot}) and t_2 (the time it takes to discharge C_{tot}). So, the oscillation frequency of the current-starved VCO for N (odd number) of stages is given by [44]:

$$f_{osc} = \frac{1}{N \cdot (t_1 + t_2)} = \frac{I_{inv}}{N \cdot C_{tot} \cdot V_{dd1}} \tag{3.24}$$

where

$$t_1 + t_2 = \frac{N \cdot C_{tot} \cdot V_{dd1}}{I_{inv}} \tag{3.25}$$

For a total capacitance C_{tot} of about 185 ff and a current (I_{inv}) of 75 nA passing for each inverter stage, the optimal number of stages in order to get at the output a frequency of 10 kHz is 21, according to Equation 3.25. At the end of the ring oscillator, a buffer is interposed to force a square wave for the Clk_0 [43].

3.3.6 Digital Stimulus Generator (DSG)

This circuit is programmable with the four remaining bits of the command word in order to control the stimulation waveform parameters such as the stimulation frequency (f_{stim}), the width of the stimulation pulse (PW) and the duration of the stimulus (t_{ON} and t_{OFF}) applied to the tissue.

The stimulation frequency can be programmed, using two bits (P3 and P4) of the programming word (Figure 3.26), from 20 Hz to 50 Hz in steps of 10 Hz. The remaining two bits, P5 and P6, are used to control the pulse width (which is the same in both phases) that can be either 200 μs or 400 μs and the duration of the stimulus (stimulation duty-cycle) that can be 1/8 (with 8 sec. on and 52 sec. off) or 1/4 (with 15 sec. on and 45 sec. off), respectively. The logic circuit diagram, shown in Figure 3.32, generates three digital signals (W_1, W_2 and W_3) that will be applied to the switching circuit in order to generate the biphasic charge-balanced stimulation waveform with the required stimulation parameters according to the received data. A frequency divider stage was used to produce different clock frequencies (Table 3.7) to be used as the inputs of the DSG.

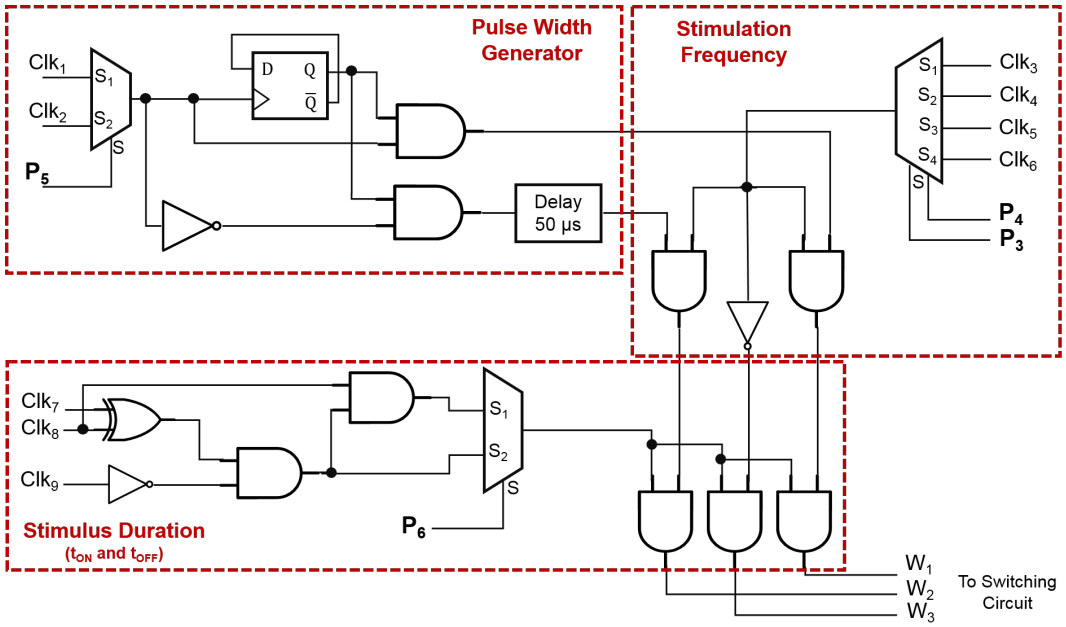


Figure 3.32: Logic circuit diagram of the DSG.

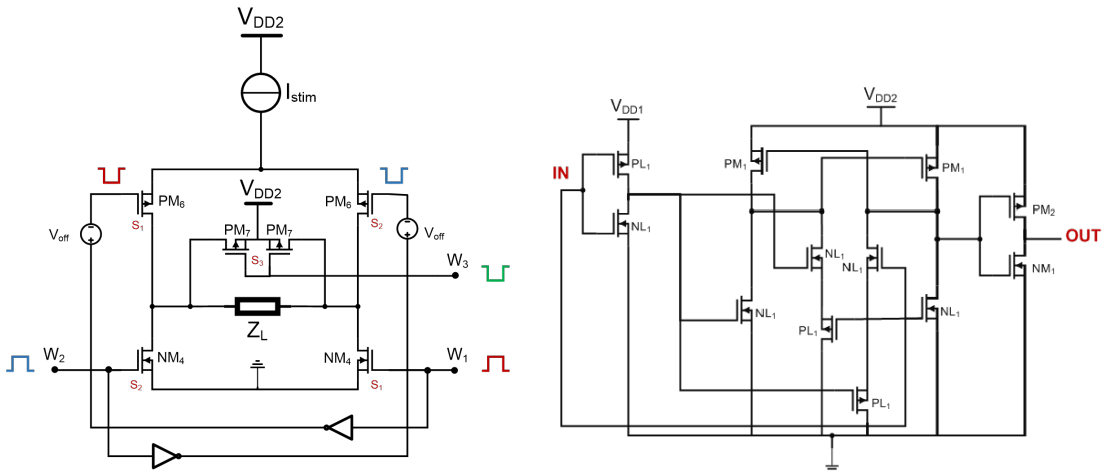
Table 3.7: Frequencies of the input signals of DSG.

Denomination	Clk_1	Clk_2	Clk_3	Clk_4	Clk_5	Clk_6	Clk_7	Clk_8	Clk_9
Frequency (Hz)	2,5k	1,25k	20	30	40	50	62,5m	31,3m	15,6m

3.3.7 Switching Circuit (SC)

The switching circuit is configured as an H-bridge topology in order to allow reversing the current in the load with an array of four transistors (two upper PMOS and two lower NMOS), as shown in Figure 3.33a. This topology has the advantage of needing only one power supply to generate a charge-balanced biphasic waveform [42], [38]. A power supply voltage (V_{DD2}) of 2,5 V is being used to accommodate the variable voltage drop in the nerve and electrode-tissue contact impedance load, as well as signals that come from the DSG to control S_1, S_2 and S_3 switches.

The switches S_1 and S_2 are driven by the control signals W_1 and W_2, respectively, that control the timing and direction of the current. Switch S_3, driven by W_3, is used to passively discharge the tissue by shortening the two electrodes. Switch S_3 is implemented using back-to-back PMOS to allow for current flowing in both directions. In order to drive the gate of the transistors in the array, a voltage level converter (Figure 3.33b) is used to convert low-voltage (V_{DD1} = 1,8 V) control signals from the DSG into medium-voltage (V_{DD2}= 2,5 V) control signals [45]. A voltage offset (V_{off}) of 2,5 V is interposed when the control signals are inverted to drive the PMOS.



(a) (b)

Figure 3.33: a) H-Bridge switch array and b) voltage level converter.

The transistor aspect ratios for the level converter and for the switch array are depicted in Table 3.8.

Table 3.8: Design parameters of the voltage level converter and of the switch array (H-bridge).

Parameters	**Values**
$(W/L)_{PL_1}$ (μm)	1,5 / 0,18
$(W/L)_{PM_1}$ (μm)	1 / 0,5
$(W/L)_{PM_2}$ (μm)	3 / 0,7
$(W/L)_{NL_1}$ (μm)	0,5 / 0,18
$(W/L)_{NM_1}$ (μm)	1 / 0,7
$(W/L)_{PM_6}$ (μm)	40 / 0,7
$(W/L)_{NM_4}$ (μm)	15 / 0,7
$(W/L)_{PM_7}$ (μm)	15 / 0,7

The control signals and the output stimulus waveforms are presented in Figure 3.34.

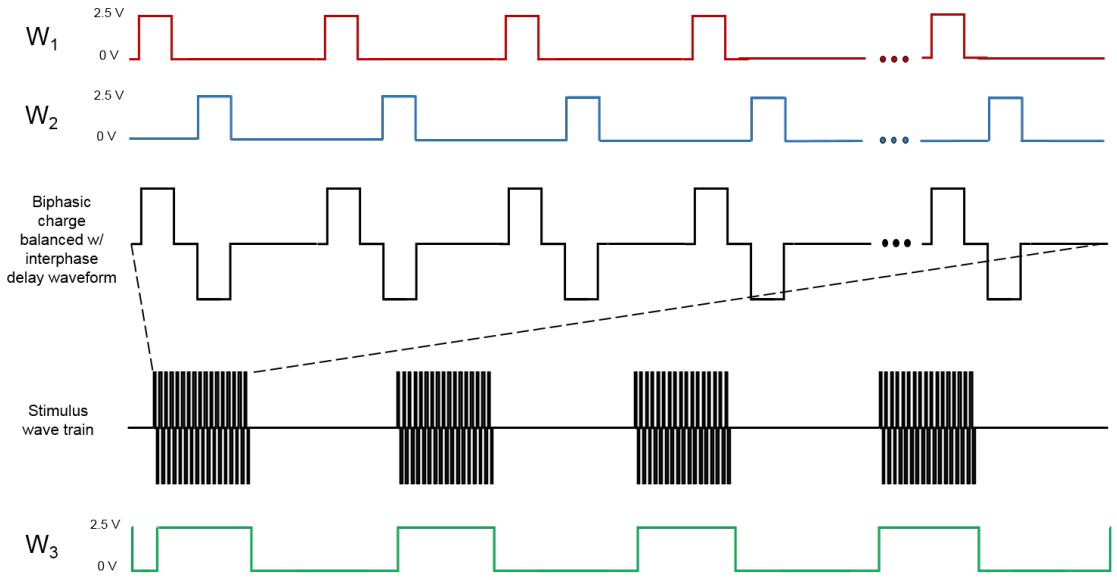


Figure 3.34: Generation of the stimulation waveform and stimulus wave train by the control signals.

3.3.8 Simulation Results

The simulations were performed in Cadence Virtuoso software using the design kit of a 180 nm CMOS technology. The frame sent from the exterior and used in this simulation to validate the operation of the circuits is shown in Figure 3.35.

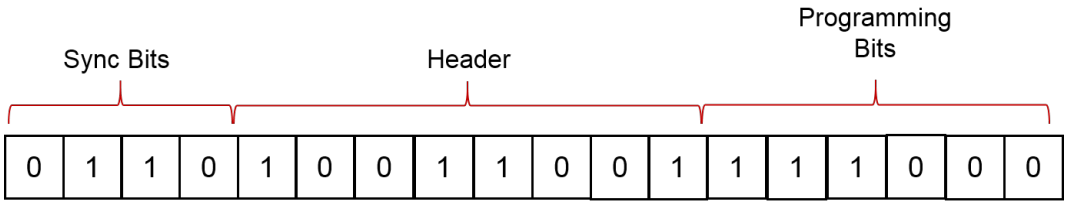


Figure 3.35: 18-bit message word used in the simulation test.

The stimulation strategy is programmed using six programming bits that were sent from the external device and recovered by the demodulator. The control of this process of applying the extracted data to the micro-stimulator, is done by the stimulation control unit which consists of a FSM and a shift-register with output registers (Figure A.8). The Figure 3.36 shows the operation of the FSM which detects correctly the header and that after six clock cycles sends an enable signal to lock the values in the output register. In the shift-register only enters the clock and data corresponding to the six programming bits.

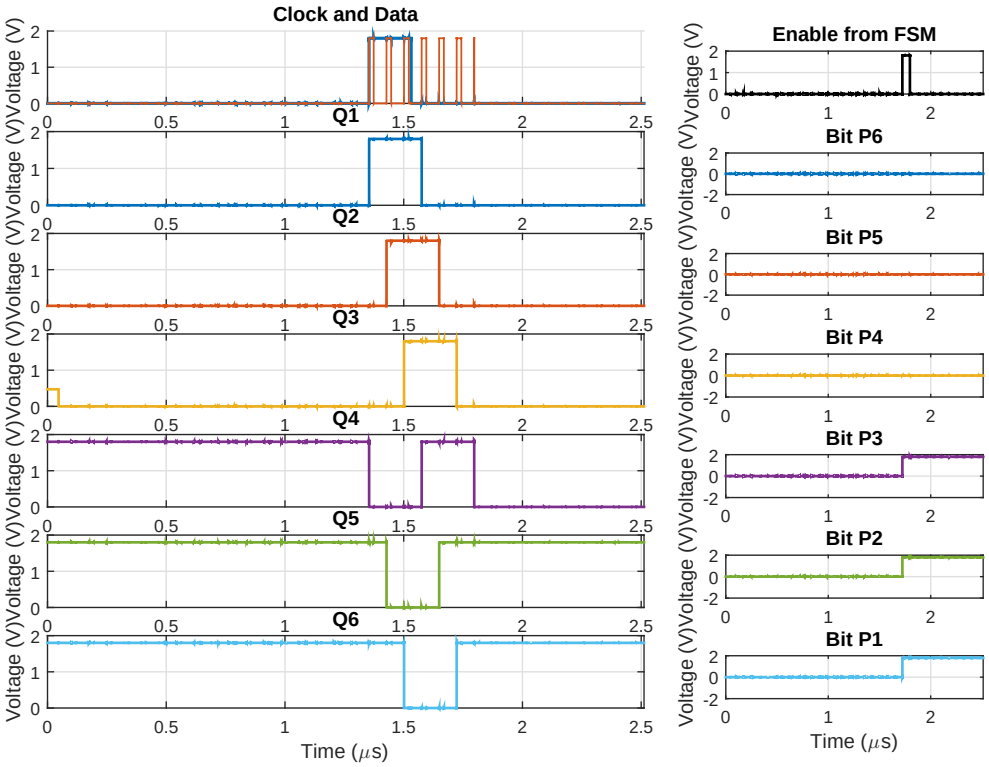


Figure 3.36: Finite state machine and 6-bit shift-register with output registers circuit operation.

The global clock (10 kHz) used to supply the frequency divider stage for the DSG is produced using a CMOS current starved ring oscillator. Figure 3.37 shows the waveform observed before and after the buffer which validates the design discussed before.

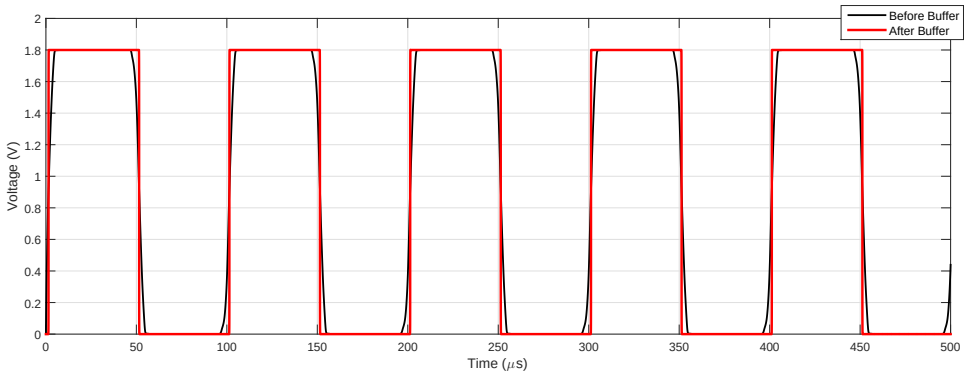


Figure 3.37: A 10 kHz clock signal for the DSG circuit.

The 2-bit programmable current source produces different stimulation currents depending on the programming bits values (P1 and P2) of the command word (Figure 3.26). From simulation results, the obtained stimulation currents (I_{stim}) depending on the programming bits and the load impedance (Z_{load}) are presented in Table 3.9.

Table 3.9: Theoretical versus simulated current values for the programmable current source.

Programing bits		**Expected Current**	**Obtained Current**		
P1	P2	I_{stim} (μA)	I_{DAC} (μA)	I_{stim} (μA) @ 0.5kΩ	I_{stim} (μA) @ 5kΩ
'0'	'0'	20	9,99	19,81	19,70
'0'	'1'	60	30,40	60,07	59,29
'1'	'0'	100	50,34	100,30	98,27
'1'	'1'	140	70,66	142,60	140,36

The output current of the stimulator versus the output voltage at the four levels of stimulation intensity were simulated ranging the output voltage from 0 to 2,5 V in steps of 0,1 V. The output characteristic is shown in Figure 3.38. The current source shows an output resistance of 500kΩ and 14,5 MΩ and a voltage headroom is about 1,3 V and 1,95 V at maximum and minimum stimulation current, respectively.

According to the command word (Figure 3.35) used for simulation, the produced biphasic waveform has a pulse width of 200μs with a period of 800μs. The design of the stimulator was set to handle a stimulator load between 500 Ω and 5 kΩ and a simulation using two different stimulation intensities (60μA and 140μA) was performed in order to evaluate the voltage seen between the electrodes for a 3kΩ (Figure 3.39a) and a 3kΩ+20nF load (Figure 3.39b).

The DSG produces the required control signals (W1, W2 and W3) to be applied to the switching array (Figure 3.33a) in order to produce a symmetrical rectangular biphasic stimulation current with a pulse width of 200 μs, a frequency stimulation of 40 Hz, and a stimulus duty-cycle of 25 % (15 seconds on and 45 seconds off). Figure 3.40 shows the correct operation for the received bits.

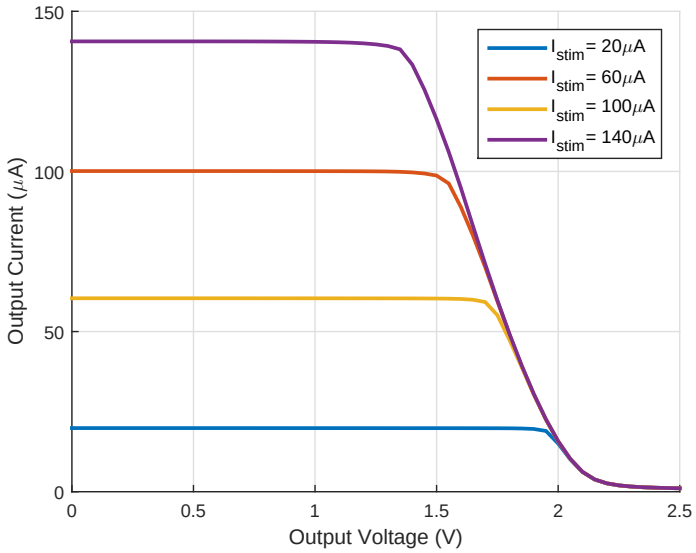


Figure 3.38: Simulated output characteristic of the stimulator.

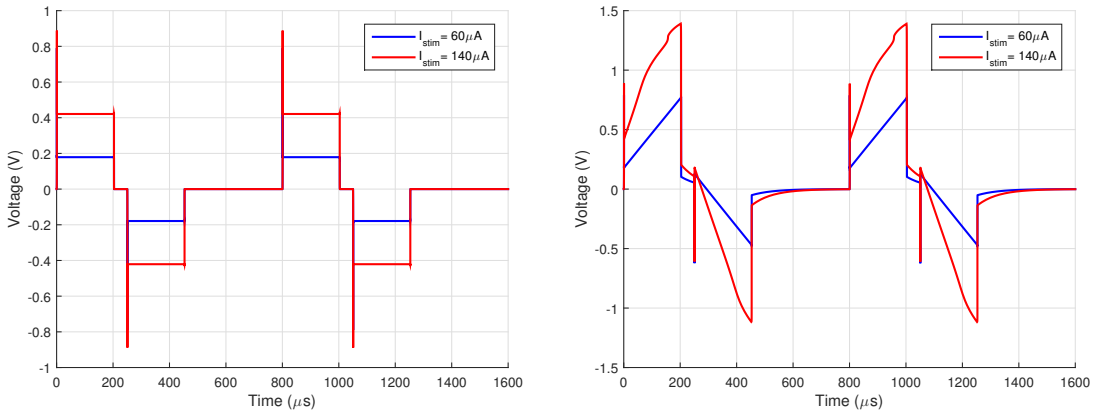


Figure 3.39: Biphasic output voltage for a a) 3kΩ load and b) 3kΩ+20nF load.

3.4 Conclusions

Simulation results show that the RF front-end and micro-stimulator circuits performs its tasks for which it was designed. The RF front-end circuit has as main feature the fact that consumes low power by designing a extremely power efficient full-wave rectifier and using a asynchronous design for the BPSK demodulator thus saving power and circuit area. As shown before the rectifier reveals good efficiency converting the a.c. power coming from the receiver coil to d.c. power to power the remote electronics of the implantable circuit, the regulator shows a good performance in stabilize the d.c. power (2,5 V and 1,8 V) to be independent of power and load variations and it has the feature of not needing a big capacitance at it output to achieve stability, thus saving circuit area, thanks to the three frequency compensation techniques employed here, and finally, the demodula-

tor can exactly extract the clock and data sent from the exterior using a low-area and low-power circuit. The micro-stimulator circuit generates a charge-balanced symmetrical biphasic stimulation waveform according with a 6-bit programming word. The stimulation is controlled by a FSM that detects the communication with the external device and receives the stimulation parameters in order to produce the required control signals by the DSG to be applied to the switching circuit is order to generate the expected stimulation pattern. The micro-stimulator circuit could deliver a maximum current of 140 μA over a range of 500 to 5kΩ load tissue impedance. In terms of power consumption the stimulation circuit consumes 250 μA at maximum stimulation current with a quiescent current of 36 μA, the power conditioning circuit (rectifier and regulator) consumes 200 μA, the BPSK demodulator consumes 450 μA and the other circuitry consumes 50 μA. Since during the programming phase the stimulation circuit is off, the total power consumption is 700 μA and during the stimulation phase the BPSK demodulator is switched off, thus leading to a maximum power consumption of 450 μA.

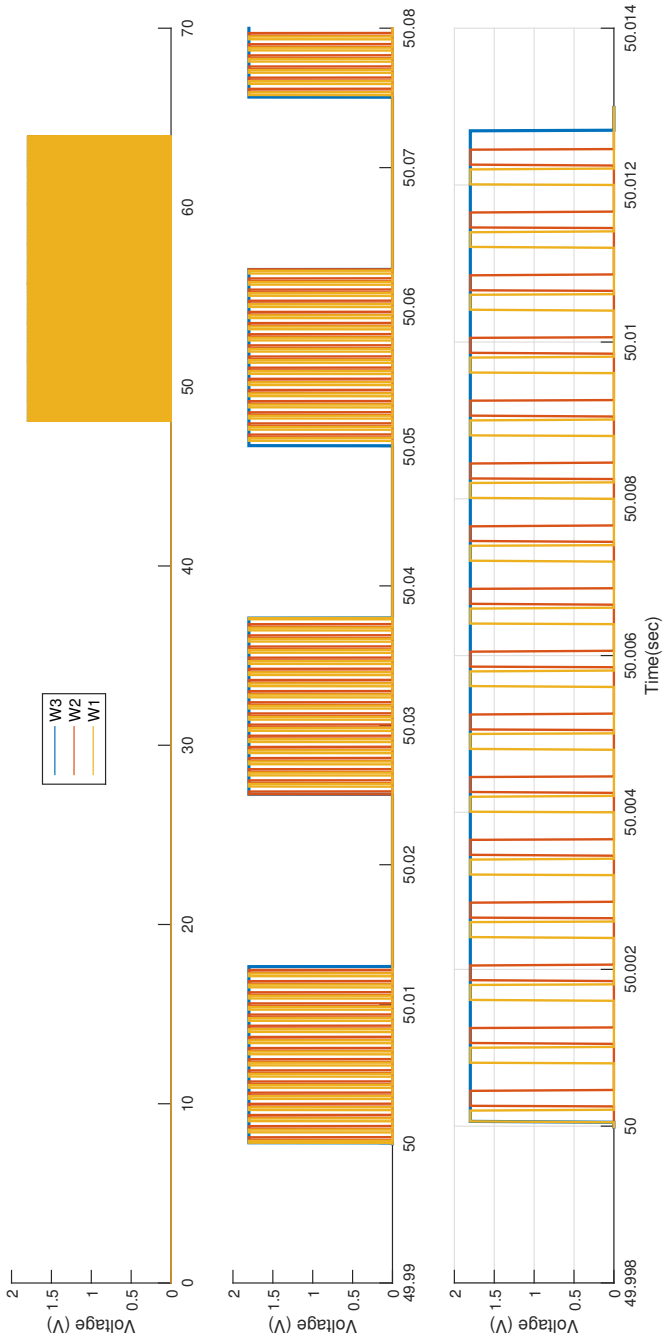


Figure 3.40: Control signals (outputs of DSG) used to control the SC in order to produce the desired electrical impulses.

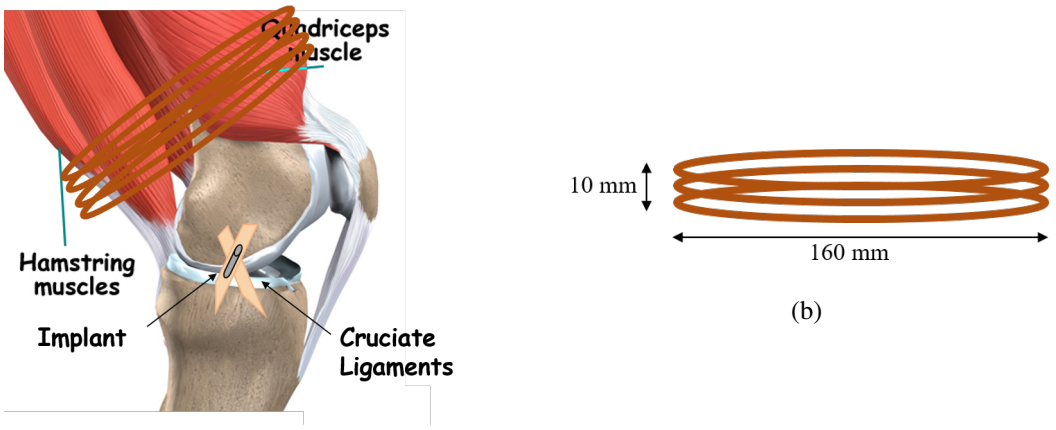
Chapter 4

Design of the External Device

This chapter addresses the design of the external device that establishes an inductive link with the implantable device to send data and power to provide proper operation of the neuromuscular stimulation system. Here, a design optimization procedure for the inductive link and power amplifier with respect to the external device, taking into account the power and geometry constraints of the implant will be followed. The design of the BPSK transmitting modulator that allows data transmission to the implant will be also discussed here.

4.1 External Stimulation Inductor

On the transmitter side there is much more freedom in the design of the primary coil and thus different possible designs are possible. After wondering about the best configuration for the transmitter coil, in order to maximize the link efficiency, the configuration presented in Figure 4.1a was chosen. In this configuration, the transmitter coil is expected to be rounded around the leg and in the final product could be embedded in a compression thigh. With this design it is expected that almost all of the the magnetic flux will drive through the leg to the implantable device. It is also likely the most comfortable configuration for the transmitter coil from the patient's point of view. The shape of the coil is a single layer short solenoid and its dimensions could vary a little to fit to different people, but the average dimensions defined for the coil are a length of 10 mm and a radius of 80 mm, as shown in Figure 4.1b.



(a) (b)

Figure 4.1: (a) Configuration of the inductive link and (b) design of the transmitter (primary) coil.

4.2 Wireless Power Transfer System

The main goal of the wireless power transfer (WPT) system is to deliver power to the implantable device from a external source of energy, such as a battery. The optimization procedure followed here, and presented in [46], takes into account powering and geometric constraints of the implantable device and also the coupling between the external and internal coils.

4.2.1 Secondary Tank of Inductive Link

The secondary tank of the inductive link is constituted by the secondary coil and a capacitor that could be placed in series or in parallel with the secondary coil for tuning into resonance. The power consumption of the remote electronics, including the rectifier, voltage regulator, demodulator and micro-stimulator circuit are often represented by an equivalent load a.c. resistor R_{load2} connected to the inductive link [46]. This subsection therefore derives a set of equations, over the entire coupling range, for optimized power transmission efficiency. The equations for the link components (coils and capacitors) and performance are calculated in the following order.

4.2.1.1 Optimization for Maximal System Efficiency

The possible six inductive link combinations are shown in the Figure 4.2, but in this work only the inductive links with a parallel-resonant secondary and a parallel-resonant primary coil are studied [46]. The only assumption is that the link operates at the phase-resonance frequency of the secondary tank.

In the inductive links with a parallel-resonant secondary, the secondary circuit is reduced to an equivalent secondary impedance Z_{eq}, in series with the primary coil, to find an operation mode where the coupling and load variations have a minimal effect on the tuning of primary circuits [46]. According to Figure 4.2, the equivalent representation indicates that:

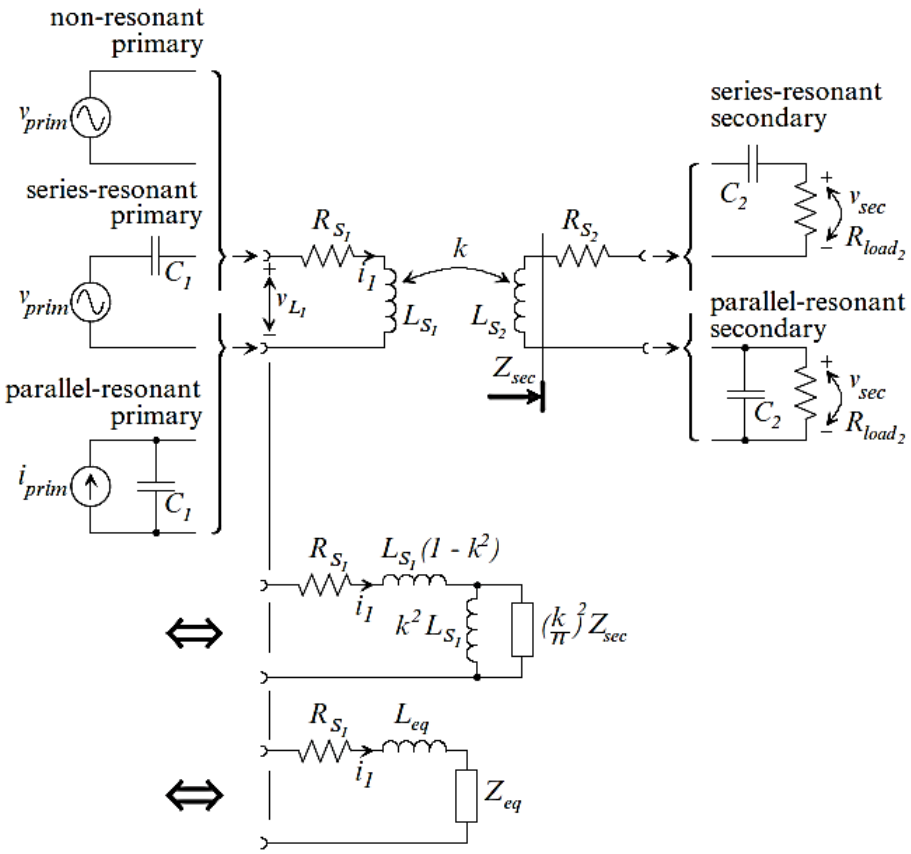


Figure 4.2: All inductive link combinations. Retrieved from [46]

$$Z_{eq} = \frac{1}{\frac{1}{j\omega \cdot k^2 \cdot L_{S1}} + \frac{1}{\left(\frac{k}{n}\right)^2 \cdot Z_{\text{sec}}}} - j\omega \cdot k^2 \cdot L_{S1} \tag{4.1}$$

where,

$$Z_{\text{sec}} = R_{S2} + \frac{1}{\frac{1}{j\omega \cdot C_2} + \frac{1}{R_{load2}}} \tag{4.2}$$

The equivalent secondary impedance Z_{eq} is real at the phase-resonance frequency of the loaded secondary tank circuit if it was not coupled to the primary coil [46], which is given by equation 4.3.

$$\omega_{resP} = \sqrt{\frac{1}{L_{S2} \cdot C_2} - \frac{1}{R_{load2}^2 \cdot C_2^2}} \tag{4.3}$$

Running an inductive link at the frequency ω_{resP} has the major advantage that Z_{eq} remains purely resistive regardless variations in coil coupling or the secondary power consumption. The equivalent resistance R_{eq} in that condition is given by

$$R_{eq} = Z_{eq} @ \omega_{resP} = k^2 \cdot L_{S1} \cdot \omega_{resP} \cdot \frac{\alpha \cdot Q_{L_{S1}}}{\alpha + Q_{L_{S2}}} \tag{4.4}$$

where α corresponds to the ratio of a.c. load R_{load2} to the reactance of the capacitor C_2, and is given by

$$\alpha \equiv \omega_{resP} \cdot C_2 \cdot R_{load2} \tag{4.5}$$

The total link efficiency is the product of the primary and the secondary link efficiencies. The primary link efficiency is defined as the ratio of the power that reaches the secondary circuit to the power put into the inductive link, and is given by [46]:

$$\eta_{primary} = \frac{k^2 \cdot Q_{L_{s1}} \cdot Q_{L_{S2}}}{1 + \frac{Q_{L_{S2}}}{\alpha} + k^2 \cdot Q_{L_{S1}} \cdot Q_{L_{S2}}} \tag{4.6}$$

The secondary link efficiency is defined as the ratio of the useful power dissipated in the a.c. load to the power that reaches the secondary circuit from the primary tank, and is given by [46]:

$$\eta_{secondary} = \frac{Q_{L_{S2}}}{\alpha + Q_{L_{S2}}} \tag{4.7}$$

Thus, the total link efficiency for inductive links only with parallel-resonant secondary and regardless whether the primary coil is tuned or not, is given by:

$$\eta_{link} = \eta_{primary} \cdot \eta_{secondary} \tag{4.8}$$

The total efficiency of the driven inductive link is the main component but is not equal to the overall efficiency because here also the driver, rectifier and regulator efficiencies have to be considered, and is given by:

$$\eta_{total} = \eta_{driver} \cdot \eta_{link} \tag{4.9}$$

The link gain is defined as the ratio of the a.c. voltage V_{sec} across the a.c. load R_{load2} to the a.c. link input voltage V_{prim} across the primary coil and its resonance capacitor, as shown in Figure 4.2. Once the parallel-resonant primaries are fed by current-type drivers, the link gain is better expressed as a transimpedance r_{stp} [46], which is the ratio of the a.c. voltage V_{sec} and the primary current I_{prim}.

The transimpedance then finally becomes:

$$r_{stp} = \omega_{resP} \cdot L_{S1} \cdot A_{stp} = \omega_{resP} \cdot L_{S1} \cdot \frac{k \cdot n \cdot Q_{L_{S1}} \cdot Q_{L_{S2}} \cdot \sqrt{\alpha^2 + 1}}{\alpha \cdot k^2 \cdot Q_{L_{S1}} \cdot Q_{L_{S2}} + \alpha \cdot Q_{L_{S2}}} \tag{4.10}$$

where A_{stp} represents the voltage link gain between V_{sec} and V_{prim}.

The link optimization involves the derivation of an optimal α to yield maximal efficiency. Optimizing α for a given a.c. load R_{load2} and transfer frequency ω_{resP}, corresponds to matching C_2 an L_{S2} to the load [46]. The optimal α that corresponds to maximal link efficiency is expressed as:

$$\alpha_{\eta_{link_{\max}}} = \frac{Q_{L_{S2}}}{\sqrt{1 + X}} \tag{4.11}$$

where,

$$X = k^2 \cdot Q_{L_{S1}} \cdot Q_{L_{S2}} \tag{4.12}$$

resulting in the maximal link efficiency given by:

$$\eta_{link_{\max}} = \frac{X}{\left(1+\sqrt{1+X}\right)^2} \tag{4.13}$$

As the link efficiency is directly proportional to the value of X, it is easy to understand from equation 4.12 that optimizing a coil set involves the maximization of the coil coupling and the coil factors. Thus, it is now possible matching the C_2 and L_{S2} to the a.c. load for maximum link efficiency through equations 4.14 and 4.15 [46].

$$L_{S2_{opt}} = \frac{R_{load2}}{\omega_{resP}} \cdot \left(\frac{\alpha_{\eta_{link_{\max}}}}{\alpha^2_{\eta_{link_{\max}}} + 1} \right) \tag{4.14}$$

$$C_{2_{opt}} = \frac{\alpha_{\eta_{link_{\max}}}}{\omega_{resP} \cdot R_{load2}} \tag{4.15}$$

4.2.2 Primary Tank of Inductive Link

It is known from the previous subsection that an inductive powering system should include the primary coil driver. There are different power amplifiers for this purpose, however in many wireless power transfer systems, class-E amplifiers have been utilized to create large a.c. currents in primary coil to produce the magnetic field for inductive powering [47]. As the system needs to operate at a specific frequency it is possible to tune out the primary inductance into resonance by adding a series/parallel capacitor in order to have a more effective use of the available a.c. voltage [46]. The driver frequency ω is always assumed to be equal to the secondary phase-resonance frequency ω_{resP} for improving the link efficiency. Primary coil drivers act as d.c. to a.c. power converts which take the d.c. energy from the supply and converts it as efficiently as possible into a.c. energy to power the primary coil. The primary coil drivers are not linear amplifiers because the output signal is a sinusoidal voltage across or current through primary coil, whereas the input signals are pulses [46]. Along this subsection, the class-E power amplifier operation is described and the amplifier design equations for driving weakly coupled links are presented.

4.2.2.1 Class-E Power Amplifiers

High efficiency power amplifiers (PA's) are commonly realized using switch-mode operation, such as Class-D, Class-F, Class-J, and Class-E PA's, which are very important for modern wireless communications systems to achieve low-cost and highly reliable transmitters [48]. The Class-E PA is the most suitable power amplifier as an element driver for transmitter coil because of its high

efficiency about 90-95% and the production of a stable sinusoidal signal to drive the inductive link [49]. This high efficiency comes from the switching mode operation because in that way the losses in the transistor (active element of PA) are practically zero since the circuit operation is determined by the switch when on and by the transient response of the load network when the switch is off. The higher efficiency of Class-E PA's is achievable thanks to tuned LC tanks, low-resistance switches and meticulous switch timing. The conventional Class-E PA topology is depicted in Figure 4.3. For this PA circuit, the inductor choke (L_{ch}) reduces the ripples and provides a constant current from the power supply V_{cc}. The transistor is considered as a switch and a shunt capacitor (C_{1par}) is connected in parallel to remove harmonics and ensure zero-voltage switching of the non-ideal switch. This capacitor is tuned to the carrier frequency to achieve a constant current from the supply source and converts the input signal to a stable sinusoidal output without d.c. offset [50].

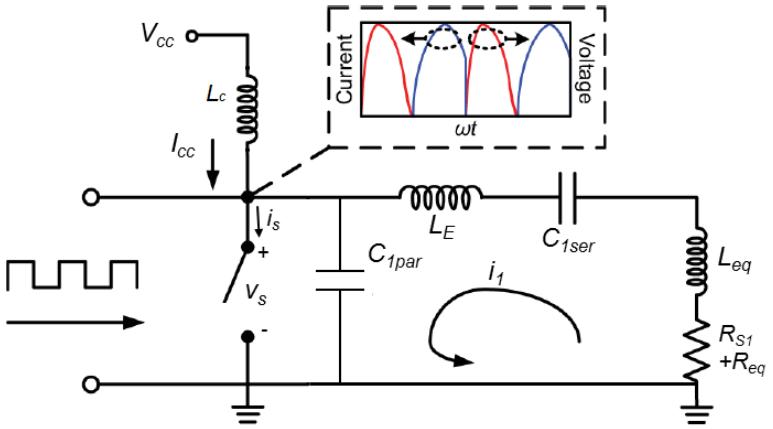


Figure 4.3: Class-E PA topology. Retrieved from [48].

If the transistor is turned on, the current flows entirely through the switch and the voltage is zero. When the switch is turned off, the current flows into the capacitor, which is charged simultaneously, and the switch voltage is non-zero. The two states of the PA are shown in the figure above, which depicts the voltage and the current status waveforms in switching time. The supply voltage is found as the average voltage across the switch [46]. The switch voltage and current are given by:

$$\begin{cases} v_{s_{OFF}}(\theta) = \frac{I_{cc}}{\omega \cdot C_{1par}} \left[y - \frac{\pi}{2} + \theta + g \cdot (\sin(\phi - y) + \cos(\phi + \theta)) \right] \\ i_{s_{OFF}}(\theta) = 0 \end{cases} \tag{4.16}$$

and

$$\begin{cases} v_{s_{ON}}(\theta) = 0 \\ i_{s_{ON}}(\theta) = I_{cc} \cdot [1 - g \cdot \sin(\phi + \theta)] \end{cases} \tag{4.17}$$

The high efficiency of the Class-E PA can be achieved by reducing the transistor switching

losses. For example, if a non-zero capacitor voltage is present at the turn-on instant, the switch discharges that voltage to zero dissipating the stored energy. This situation must be avoid in order to guarantee high efficiency of the driver, so loss-free operation requires that the switch voltage is zero at turn-on. The circuit equations for the Class-E design flow presented below are written in terms of the primary coil inductance for the optimization procedure. Some of the used terms result from the secondary optimization.

$$V_{prim} = V_{\text{sec}} \cdot A_{stp} \tag{4.18}$$

$$I_{prim} = V_{\text{sec}} \cdot r_{stp} \tag{4.19}$$

$$R_{s1}^{*} = R = \frac{\omega^2 \cdot L_{eq}^2 + (R_{s1} + R_{eq})^2}{R_{s1} + R_{eq}} \tag{4.20}$$

$$y = \pi \cdot (1 - D) \tag{4.21}$$

$$\phi = \arctan\left[\frac{\frac{\sin(y)}{y} - \cos(y)}{\frac{\zeta \cdot y}{\pi} \cdot \cos(y) - \left(1 + \frac{\zeta}{\pi}\right) \cdot \sin(y)}\right] \tag{4.22}$$

$$g = \frac{y}{\cos(\phi) \cdot \sin(y)} \tag{4.23}$$

$$\tan(\psi) = \frac{q1 \cdot \sin(\phi) + q2 \cdot \cos(\phi) + q3 \cdot \cos(2\phi) + g \cdot y}{q2 \cdot \sin(\phi) + q3 \cdot \sin(2\phi) - q1 \cdot \cos(\phi)} \tag{4.24}$$

$$\begin{cases} q1 \equiv -2g \cdot \sin(\phi - y) \cdot \sin(y) - 2y \cdot \sin(y) \\ q2 \equiv 2y \cdot \cos(y) - 2. \sin(y) \\ q3 \equiv -\frac{g}{2} \cdot \sin(2y) \end{cases} \tag{4.25}$$

$$C_{1par} = \frac{2y^2 + 2y \cdot g \cdot \sin(\phi - y) - 2g \cdot \sin(\phi) \cdot \sin(y)}{\omega \cdot \pi \cdot g^2 \cdot R_{s1}^{*}} \tag{4.26}$$

$$C_{1ser} = \frac{L_{eq}}{\omega^2 \cdot L_{eq}^2 + (R_{s1} + \mathrm{R}_{eq})^2} \tag{4.27}$$

$$I_{cc} = \frac{V_{prim}}{g \cdot \omega L_{eq}} \tag{4.28}$$

$$R_{cc} = \frac{g^2 \cdot R_{s1}^{*}}{2} \tag{4.29}$$

$$V_{cc} = R_{cc} \cdot I_{cc} \tag{4.30}$$

$$Infinite\ Choke \Leftrightarrow \omega \cdot L_{choke} \gg R_{cc} \tag{4.31}$$

$$\eta_{class-E} = \frac{p_R}{1 + p_{R_{ON}} + p_{V_{Sat}} + p_{t_F} + p_{t_R} + p_{L_S}} \tag{4.32}$$

$$\begin{cases} p_R \equiv \frac{P_R}{P_{V_{cc}}} = 1 \\ p_{R_{ON}} \equiv \frac{P_{R_{ON}}}{P_{V_{cc}}} = \frac{R_{ON}}{\pi \cdot R_{s1}^*} \left[\left(1 + \frac{2}{g^2}\right) \cdot (\pi - y) + \frac{4}{g} \cdot \sin(y) \cdot \cos(\phi) - \frac{\sin(2y) \cdot \cos(2\phi)}{2} \right] \\ p_{V_{SSat}} \equiv \frac{P_{V_{SSat}}}{P_{V_{cc}}} = \frac{V_{SSat}}{V_{cc}} \\ p_{t_F} \equiv \frac{P_{t_F}}{P_{V_{cc}}} = \frac{I_{OFF}^2 \cdot t_F^2}{24 C_{1par}} \cdot f, \quad where \quad I_{OFF} = I_{cc} \cdot [1 - g \cdot \cos(\phi - y)] \\ p_{t_R} \equiv \frac{P_{t_R}}{P_{V_{cc}}} = \frac{I_{ON}^2 \cdot t_R^2}{24 C_{1par}} \cdot f, \quad where \quad I_{ON} = I_{cc} \cdot [1 - g \cdot \cos(\phi + y)] \\ p_{L_S} \equiv \frac{P_{L_S}}{P_{V_{cc}}} = \frac{L_S \cdot I_{OFF}^2}{2} \cdot f \end{cases} \tag{4.33}$$

$$V_{cc}^* = \frac{V_{cc}}{\eta_{driver}} \tag{4.34}$$

$$\begin{cases} v_{S_{\max}} = v_{S_{OFF}} @ \theta_{\max}, \quad where \quad \theta_{\max} = \arcsin\left(\frac{1}{g}\right) - \phi \\ if \quad (y - \pi < \phi) \quad then \quad i_{S_{\max}} = I_{cc} \cdot (1 + g) \quad else \quad i_{S_{\max}} = I_{OFF} \end{cases} \tag{4.35}$$

It is completely different driving a well-coupled link and a weakly coupled link, because it leaves the driver in a sort of free-wheeling, whereas the driver of a well coupled link is appropriately loaded, since the secondary power consumption adds a considerable resistance to the primary coil, even for a high-Q primary [46]. Only the Class-E PA topology can deal with the demands of weakly coupled links. An ideal solution would be to raise the resistive driver load without increasing the coil inductance (to keep the circuit voltages low) or reducing its quality factor (to maintain the link efficiency). This is done by applying a capacitor C_{1res} in parallel to the primary coil and tuning it into resonance [46] (Figure 4.4). This parallel tank behaves like a resistor because it is resonating, but it exhibits a higher resistance than the coil itself. In fact, the link coil and the parallel capacitor form an impedance transformer.

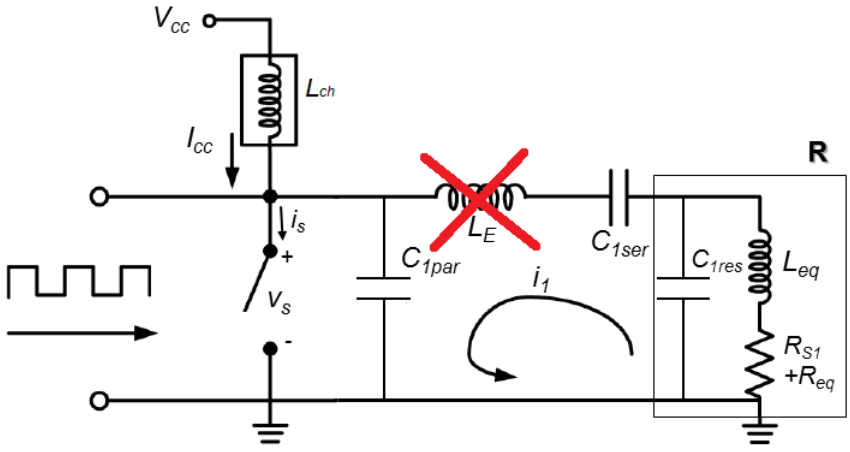


Figure 4.4: The class-E driver with a parallel-resonant primary coil.

The parallel resonance dissolves the inductance L_{eq} in the Class-E series branch turning that part to act like a resistor R, an extra coil L_E needs to be added. However, this technique has

the drawback that there is an additional coil in series branch. So, it is possible to overcome this situation choosing the semi-resonance operation mode for class-E design and by this way the use of the coil L_E is avoided. With this operation mode it is not necessary to tune the parallel capacitor and the link primary into full resonance to obtain a resistance increase [46]. For the design of the class-E PA it is necessary to choose a frequency ω_0 (slightly above the operation frequency ω) in order to run the tank somewhat below resonance to obtain a resistance increase. In this operation mode, the apparent resistance and inductance are given by:

$$R \approx \frac{R_{S1} + R_{eq}}{\left[1 - \left(\frac{\omega}{\omega_0}\right)^2\right]^2} \tag{4.36}$$

$$L \approx \frac{L_{eq}}{1 - \left(\frac{\omega}{\omega_0}\right)^2} \tag{4.37}$$

The calculations for the class-E driver follow the equations from 4.18 to 4.35, but replacing L_{eq} by L and R^*_{S1} by R.

In conclusion, driving weakly coupled links is difficult due to the high quality factors involved, which compromise Class-E efficiency since they lead to low circuit voltages and high currents. In these cases, this type of PA operates better at duty cycles (δ) shorter than 50%, since reducing the duty cycle cuts down $V_{S_{sat}}$ and R_{ON} losses and it increases the supply voltage and reduces the switch current.

4.2.3 Circuit Optimization Procedure

A step-by-step procedure aiming at optimizing a driven inductive link in order to get a maximum overall efficiency was proposed in [46] and discussed in [51]. The optimization procedure algorithm was implemented in MATLAB (see Appendix B), in which its output data are the circuit component values of the driven inductive link. This procedure is divided in two parts (design of the secondary and primary circuits) as shown in Figure 4.5.

The power losses in the surrounding tissue can be ignored if the operating frequency is chosen below 20 MHz [46], a frequency (f_{resP}) of 13,56 MHz was chosen for operating this system, since this is one of the frequencies internationally selected for Industrial, Scientific and Medical (ISM) applications and it is supposed to allow for some power applications without disturbing potential surrounding communications.

The design procedure of the secondary link follows the flowchart shown in Figure 4.5. The procedure starts with a realistic guess of the a.c. load R_{load2} of 5 kΩ from the powering demands of the remote implantable electronics of the secondary and also a realistic guess for the coil quality

factors (600 for the primary and 90 for the secondary coil). For the coupling factor, a value in the worst-case scenario taking into account possible angular or lateral misalignment between the coils of 0,5% is assumed. Then, the a.c. load is combined with the coupling factor to calculate the inductance that matches the a.c. load for maximum link efficiency, giving an optimum number of turns (n_2) of 26, an inductance for the secondary coil (L_{S2}) of 1,384 μH [52] with a series resistance R_{S2} of 2,096 Ω [53], and a matching capacitor C_2 for resonance of 97,254 pF. The quality factor of the secondary coil ($Q_{L_{S2}}$) is 56,26.

After finishing the inductive link design of the secondary, the circuit design of the primary link which follows the flow chart in Figure 4.5 starts by choosing a driver topology and afterwards its components, efficiency, supply specifications and maximum switching signals are expressed as a function of primary coil L_{S1}. A voltage of 5 V at the secondary side (V_{sec}) was specified as the target for the implantable device.

A Class-E Power Amplifier was the chosen topology for the power amplifier because it is the best topology when the coupling is weak and due to its excellent efficiency. The weakly coupling leaves the driver sort of a free-wheeling, whereas the driver of a well-coupled is appropriately loaded. So, in order to raise the resistive driver load, a capacitor is applied to the primary coil and tuned into resonance [46]. However, is not necessary to tune it into full resonance to obtain a resistance increase. Thus, a Class-E with a semi-resonant primary with a resonance frequency of 15 MHz was applied. The optimal coil which gives the best driver efficiency was found to have an inductance of 5,891 μH [52] with 4 windings and a series series resistance of R_{S1} of 0,922 Ω [53] with a parallel capacitor C_{1res} of 19,11 pF. The selected driver transistor is the n-channel Power MOSFET Si1555DL [54] because it handles a maximum voltage of 20 V and a maximum drain current of 500 mA (continuous), has high transition speeds (t_F=10ns and t_R=16ns), and shows low gate capacitance and on-resistance. A choke inductor (L_{choke}) with a minimum of 100 μH is used to force a constant supply current (I_{cc}) in order to fed the class-E driver. A series capacitor (C_{1ser}) of 4,37 pF is used to separate the switch transistor from the primary coil and it represents the residual capacitance from resonance. A shunt capacitance (C_{1par}) of 26 pF is added to the transistor output capacitance (around of 52 pF) in order to ensure zero voltage at turn-on and thus reducing the power dissipation on the transistor. The driver is expected to achieve an efficiency of 75,4%.

The algorithm output with the circuit components values for the driven inductive link shown in Figure 4.6, is listed in Table 4.2, along with the full properties of both coils in the WPT system in Table 4.1.

4.2.4 Designed System for Wireless Power Transfer

The performance of the circuit designed for the WPT system is described later taking into account simulation results. These circuit simulations are intended to validate the design procedure followed in the previous section and its equations.

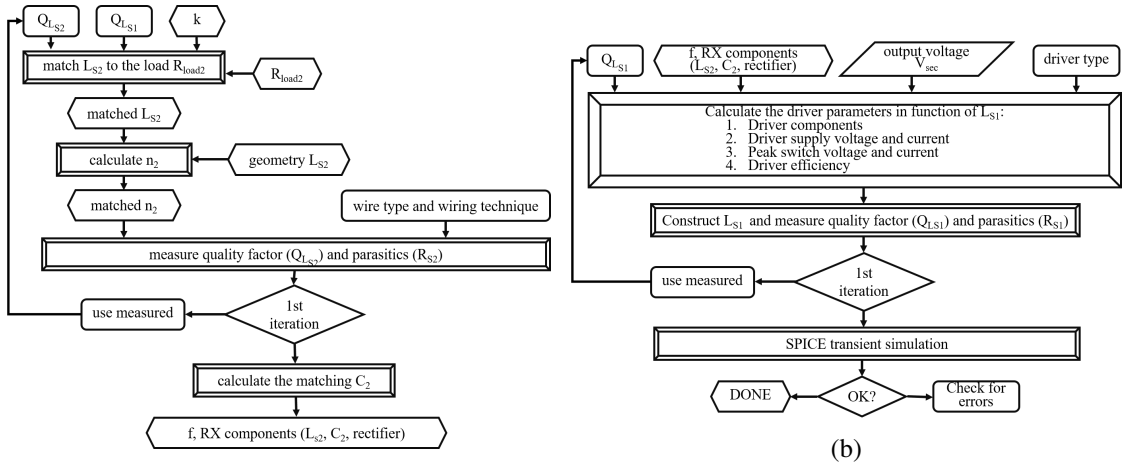


Figure 4.5: Design flow of the (a) secondary and (b) primary circuits.

Table 4.1: Properties of transmitter and receiver coils.

Parameter	Primary Coil	Secondary Coil
Length (mm)	10	6
Radius (mm)	80	2
Coil Inductance (μH)	5,891	1,384
Wire Type	Enamelled Copper (18 AWG)	Enamelled Copper (38 AWG)
Series Resistance (Ω)	0,922	2,097
Number of Turns	4	26
Quality Factor	544,60	56,26

Table 4.2: WPT circuit component values.

Parameter	Value
MOSFET	SI1555DL
Driver	3V @ 13.56MHz Square-Wave (Duty-Cycle=40%)
R_G (Ω)	25
V_{cc} (V)	2,06
L_{choke} (μH)	500
C_{1par} (pF)	26
C_{1ser} (pF)	4,37
C_{1res} (pF)	19,11
L_{S1} (μH)	5,89
R_{S1} (Ω)	0,92
L_{S2} (μH)	1,38
R_{S2} (Ω)	2,096
C_2 (pF)	97,25
R_{load2} (kΩ)	5
k (%)	0,5

The values presented in Table 4.2 are the exact values for the components, but it is obvious that when it is implemented in printed circuit board using discrete components these will not have these exact values but approximate standard values instead. With regards to the battery to be used, two rechargeable batteries (NiMH) of 1,2V with a capacity of 2450 mAh performing 2,4 V are used, because there are no batteries of 2 V available in the market. Thus, the circuit operation could change a little with respect to the designed system.

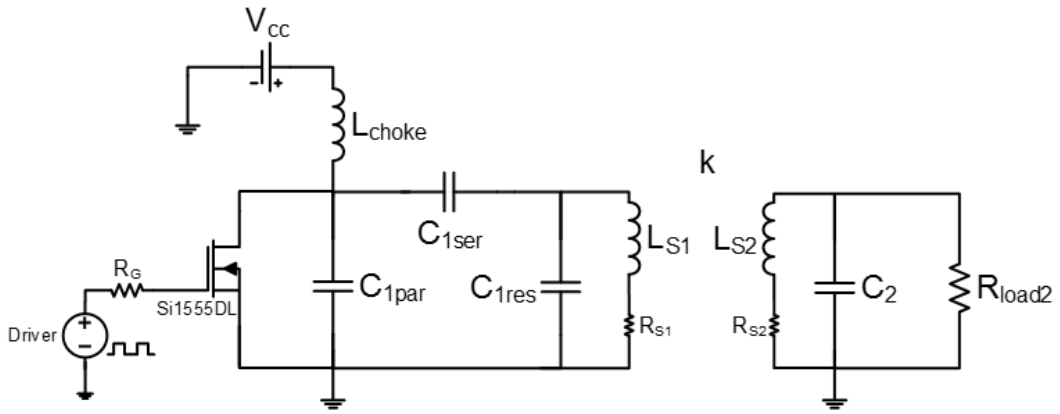


Figure 4.6: Designed system for wireless power transfer.

4.3 BPSK Modulation

The transmission of data to configure the operation of the implant is carried out after modulating the operation of the power class-E PA. For that purpose, the external device provides a controller that helps the physician/doctor to change the stimulation parameters (stimulation pulse width, frequency, amplitude and duration) and to trigger the stimulation. This controller could be a simple Arduino connected via Bluetooth to a PC that selects the stimulation parameters based on doctor's decision. The controller will receive the selection of the parameters and, then, generates the programming digital data that modulates the RF carrier.

In wirelessly connected systems, when the time base for the transmitter and the receiver are independent, a small difference between the clocks could cause errors due to sampling of the data at wrong time. The best solution for this problem is the combination of data and clock in the transmitter with a technique called Manchester coding, that provides strong timing information by providing a transition for every bit (zero or one).

At the transmitter side, data (stimulation parameters) are encoded by a Manchester encoder (XOR logic gate) and, then, the Manchester encoded data signal M(t)={+1,-1} that comes from a digital port of the controller is fed to the gate of the NMOS power transistor of the class-E PA. Thus, the data are modulated by binary phase shift keying (BPSK) with a carrier frequency of 13,56 MHz and then transmitted via BPSK signals through the primary coil L_{S1}, as shown in Figure 4.7. Since size constraints in the external device is not a concern, the circuit for the BPSK modulator and the power telemetry can be implemented using discrete components in a small board attached to the controller [55].

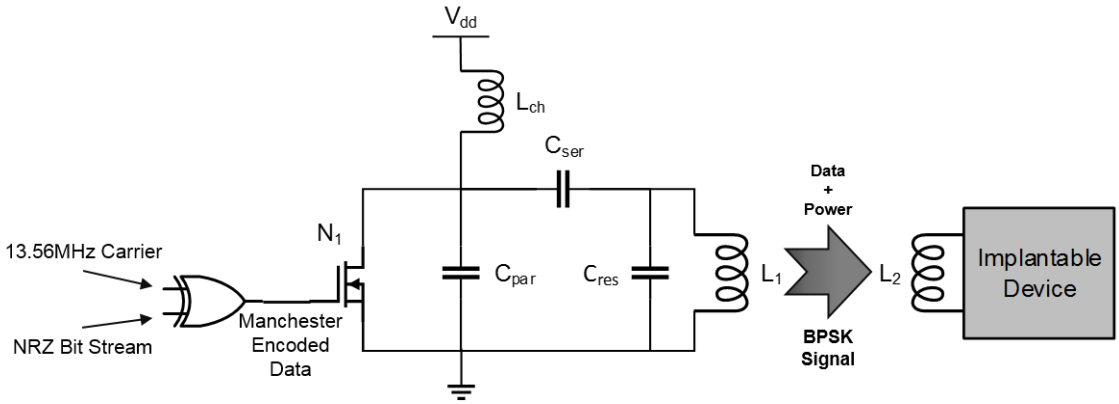


Figure 4.7: BPSK modulator and power telemetry unit.

4.4 Simulation Results

The simulation results presented below were obtained using the (LTSpice IV) simulation software. Figure 4.8 shows the operation of the Class-E power amplifier. From here it is possible to understand how the driver controls the switching operation of the transistor by applying a 3 V square wave at 13,56 MHz with a duty-cycle of 40% at the gate of n-channel power MOSFET. A small resistance, R_g has been used between the output of the driver and the gate of the MOSFET in order for minimizing the sharp current glitches in the switching transients. When the gate voltage is 0 V, the transistor is off and a voltage appears between the drain and source and when the gate voltage is in high-state (3 V) the transistor is on and the current flows from the network to the transistor. As shown in Figure 4.8 the class-E PA operation reveals a non-ideal operation resulting in power losses mainly due to non-zero voltage and current at same time.

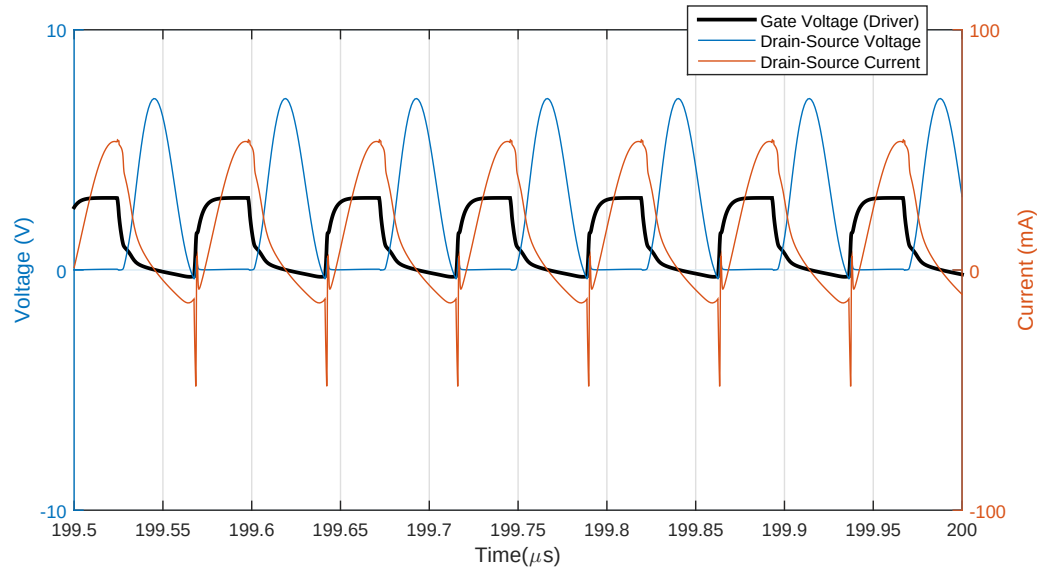


Figure 4.8: Class-E power amplifier operation.

The WPT system was designed for a worst case scenario of 0,5% of coupling factor and an a.c. load (R_{load_2}) of 5kΩ, but when these parameters are changed the system has the ability to adapt to the new conditions and thus is almost insensitive to those changes. Varying the coupling factor (k) from 0,5% to 5% the voltage at the secondary does not exceed 8,5 V. For coupling factors above 5%, the performance of the system and its functionality is greatly affected. Increasing the value of the a.c. load (reducing the available current for the implantable circuitry) to 1 MΩ raises the secondary voltage to 8 V.

Figure 4.9 shows the waveforms of the inductive link input and output voltages and currents for a worst case scenario of coupling factor of 0,5%. In the design procedure a target of 5 V at the secondary side was established, but stimulation results are even better since they show a 5,5 V at secondary.

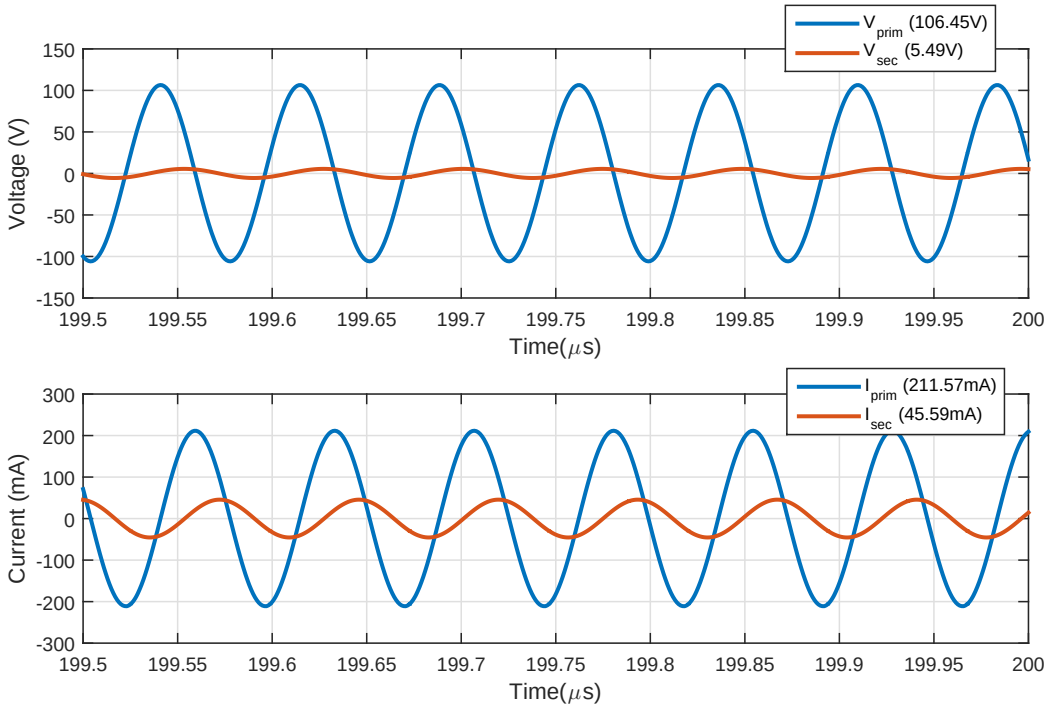


Figure 4.9: Voltages (V_{prim} , V_{sec}) and currents (I_{prim} , I_{sec}) in the primary and secondary coil.

From simulations experiments, a battery is simulated as a voltage source (V_{cc}) delivers a output voltage of 2,06 V and a d.c. current produced by the choke inductor (I_{cc}) is 14,1 mA, thus the power delivered by the battery (P_{in}) is equal to 28,9 mW. In the class-E power amplifier operation, essentially due to non-ideal effects of the switching transistor, there is a power dissipation (P_{driver}) of 8,3 mW, resulting in an driver efficiency (η_{driver}) of 72 %. The power put into the inductive link ($P_{link_{in}}$) is about 21 mW and the power that reaches the secondary circuit (P_{sec}) is 5,11 mW, resulting in a primary link efficiency ($\eta_{primary}$) of 24,3 %. From the power that reaches the secondary, a portion of 2,97 mW is dissipated in the a.c. load ($P_{link_{out}}$) and other portion of 2,14 mW is lost in the parasitic resistance ($P_{R_{S2}}$), which results in a secondary link efficiency ($\eta_{secondary}$) of 58,1

%, thus the link efficiency (η_{link}) is about 14 %. The overall efficiency of the designed wireless power transfer system (η_{total}) is 10 %, which is a good efficiency considering the low coupling factor between the two inductive interfaces.

4.5 Conclusions

Simulation results show that the wireless power and data transfer system using BPSK modulation scheme performs its tasks for which it was designed. The wireless power transfer was designed taking in account mainly the power requirements of the implantable circuitry and the design of the implantable and receiver coils in order to achieve an efficient and comfortable system. Basing in some requirements the system was design using an algorithm in which it outputs gives the optimal circuit component values and the simulations validated the algorithm. Due to low coupling factor and the need of the system to be portable was necessary to introduce a efficient power amplifier supplied by a battery in order to produce even higher magnetic fields. Using a 2 V battery and a efficient class-E power amplifier was achieved a voltage of 5 V at the secondary side (implant) delivering a current of 1 mA, in a worst case scenario, over a a.c. load of 5kΩ. The BPSK modulation was performed by changing the phase of the carrier RF signal that powers the implant and it was achieved by applying a Manchester encoded data at the gate of the power MOSFET that is used for the power amplifier.

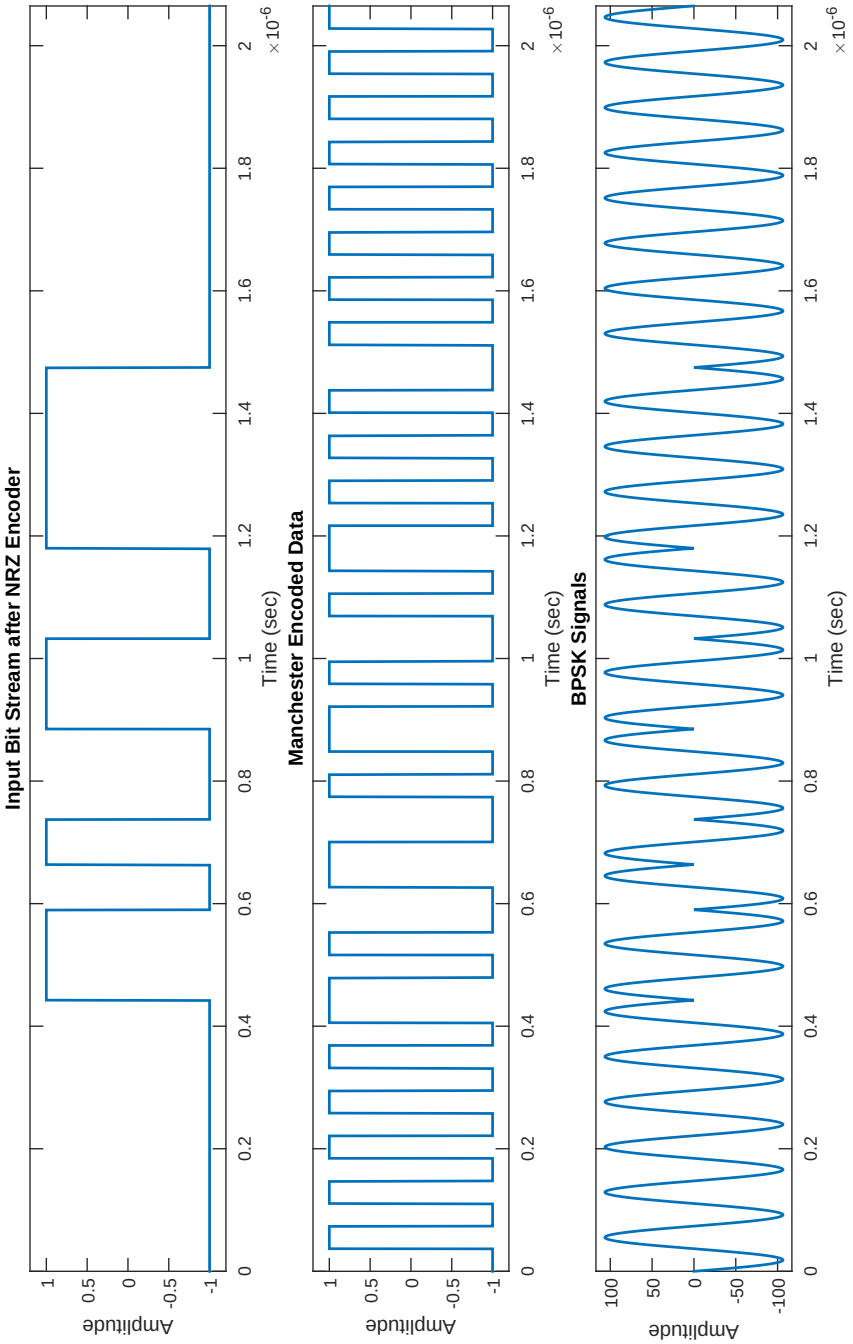


Figure 4.10: BPSK Modulator

Chapter 5

Conclusions

This is the final chapter of this dissertation. Here, a global analysis of all the work that was developed is carried out first and the main conclusions attained from the achieved results are highlighted. Finally, the future work still needed to build a fully optimized *in-situ* implantable device, including its powering and communication external system, in order for this device to be ready for the first prototype evaluation, is addressed.

5.1 Summary and main conclusions

The work developed in this dissertation addresses the design of a first prototype of an *in-situ* implantable neuromuscular electrical stimulator wirelessly powered and controlled by an external controller via inductive coupling, which aims at delivering electrical impulses via cuff electrodes placed around the ligament. To the best of our knowledge it is a totally new approach of *in-situ* stimulation of the new cruciate ligament in order to strengthen it. The stimulation pattern of the impulses can be programmed in amplitude, pulse width, frequency of stimulation and stimulus duration, by means of a 6-bit word received from the external device. The implantable device will be placed inside the new cruciate ligament that replaces the injured one after reconstruction surgery. It is expected that the electrical impulses with a suitable pattern (taking into account the recovery phase of the patient) delivered from the implantable stimulator will strengthen the new ligament and thus give more stability to the knee providing a reduction in the recovery time and a quickly return to sports.

The dissertation started with a comprehensive literature review of the anterior/posterior cruciate ligaments injury, its rehabilitation processes, the role that neuromuscular electrical stimulation (NMES) plays in training and strengthening the new ACL/PCL, how it can be improved by directly stimulating the ligament rather than stimulating the quadriceps and hamstrings to fortify the new ligament, and of what is the best stimulation pattern in terms of effectiveness (Chapter 2). A wireless power transfer system (WPT) with a BPSK modulation scheme was designed to not only provide power but also to establish a half-duplex communication between the stimulator and the

exterior that sends the programming data modulating the carrier wave. As the implantable device is so small, the coupling factor between the coils that builds the inductive interface for WPT is really low (order of 0,5 %), and the need for the system to be portable imposes the use of a power amplifier in the external device. The modulation is performed by combining data and clock at the gate of the power MOSFET of the power amplifier. Simulation results show that with a battery of 2,4 V the system achieves a 5 V at the receiver implanted coil (in the worst case scenario) and an overall efficiency for the WPT of 10 %. The modulation scheme does not affect this efficiency.

In order to build a so small implantable device to fit the size constraints of the graft (new ligament) the electronics needs to be implemented with a very large scale of integration. This integrated circuit comprises an RF front-end circuit for power conditioning and to extract the clock and data that comes from the exterior and a programmable micro-stimulator to deliver the required electrical impulses to the target tissue (graft). The proposed circuit was designed in a 0.18 μm CMOS technology. According to the simulation results, all the modular blocks that are integral part of this implantable SoC device operate in accordance with the specifications of low-power consumption and circuit area and with the expected behaviour. The full-wave rectifier works according to the design parameters and reveals a good efficiency. Two linear regulators ensure stable DC voltages, independently of power and load variations, providing 2,5 V to the micro-stimulator circuit and 1,8 V to the remaining analogue and digital circuits. The BPSK demodulator performs its function since it is able to extract correctly the data and clock from the BPSK RF signals. A header is sent along with the programming word in order to establish communication and inform the micro-stimulator circuit when data to configure stimulation parameters is being sent. A finite state machine (FSM) was implemented to detect the header and to send an enable signal after counting the six bits of the programming word, in order to lock the bit values in the output registers. Simulation results allowed us to confirm that the FSM performs correctly. The stimulation intensity can be programmed in four levels (from 20 μA to 140 μA) using a 2-bit programmable current source that can handle in perfect conditions with the switching array (in H-Bridge topology) and with the expected stimulator load whose impedance can vary from 500 Ω to 5kΩ.

The other stimulation configuration parameters, which configure the digital signal generator (DSG), are defined using the remaining four bits of the programming word. These define the control signals needed to generate the required stimulation waveform, i.e., to control the H-bridge switching array that drives the load (tissue) with a symmetrical biphasic and charge balanced stimulation waveform.

Chapter 3 presents simulation results obtained within the Cadence Virtuoso platform in order to validate the operation of the designed circuits. It could be concluded that all the blocks perform their tasks correctly.

5.2 Future Work

As mentioned before the work carried out in this dissertation is only a first approach to design the prototype of a medical device that is expected to be launched in the market in a couple of years and so further work is still needed to be done. Firstly, it is necessary to conclude the design with the layout and tape-out of the implantable chip, to bring this prototype from virtual to real. Using the circuits designed and simulated here the next step is making the layout of the chip with all types of post-layout simulations before sending it for fabrication. Once the prototype system is built it is necessary to conduct $in-vivo$ experiments in order to test the effectiveness of the neuromuscular stimulation. After the experimental operation is validated, the next step must be the design of a final prototype with a high degree of re-programmability, that is extremely safe and efficient and that, eventually, could establish a full-duplex communication in order to send back information about the effectiveness of the stimulation and about the condition of the ligament.

Appendix A

Appendix A

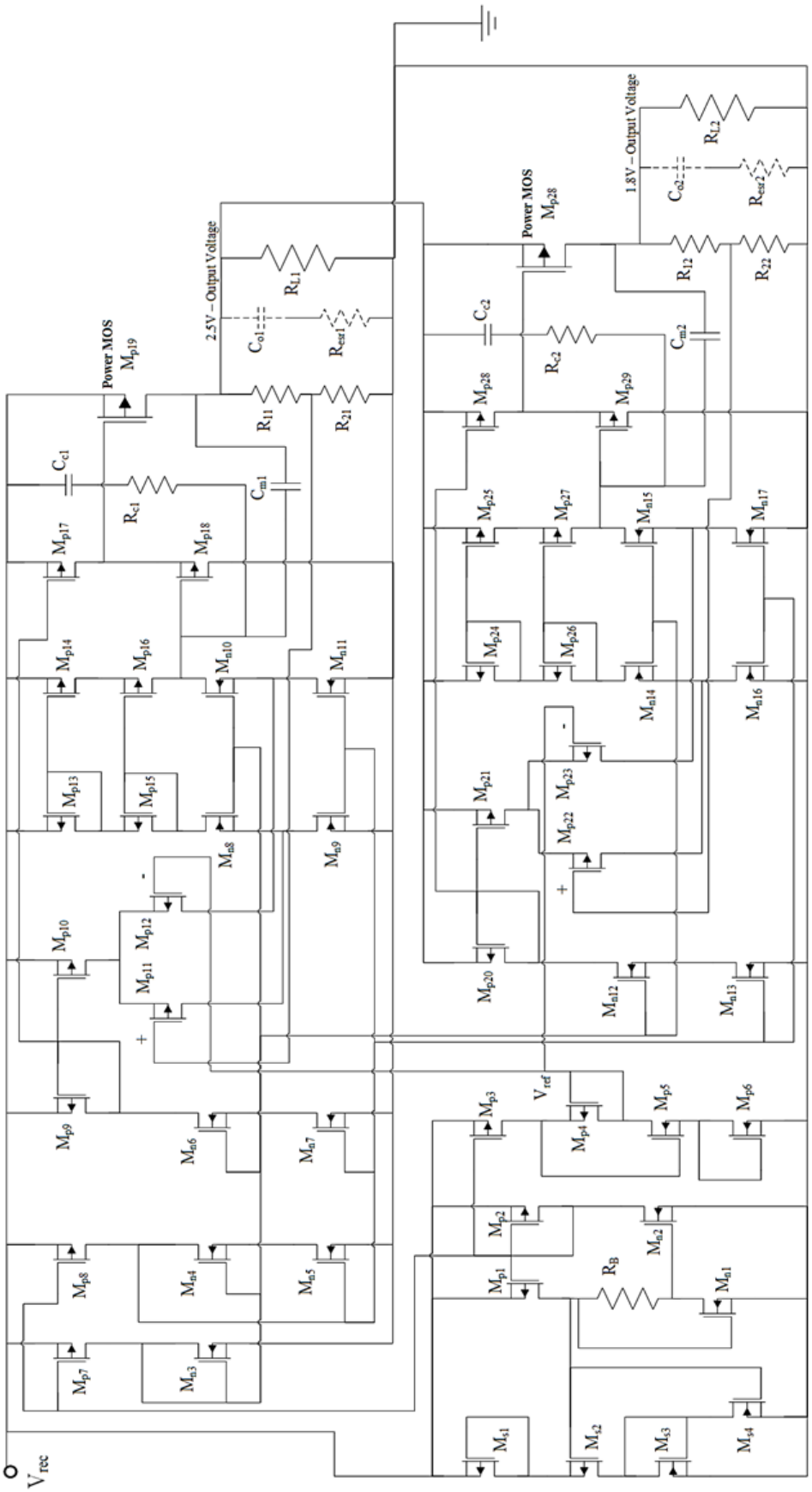


Figure A.1: Circuit Structure of the proposed linear regulator.

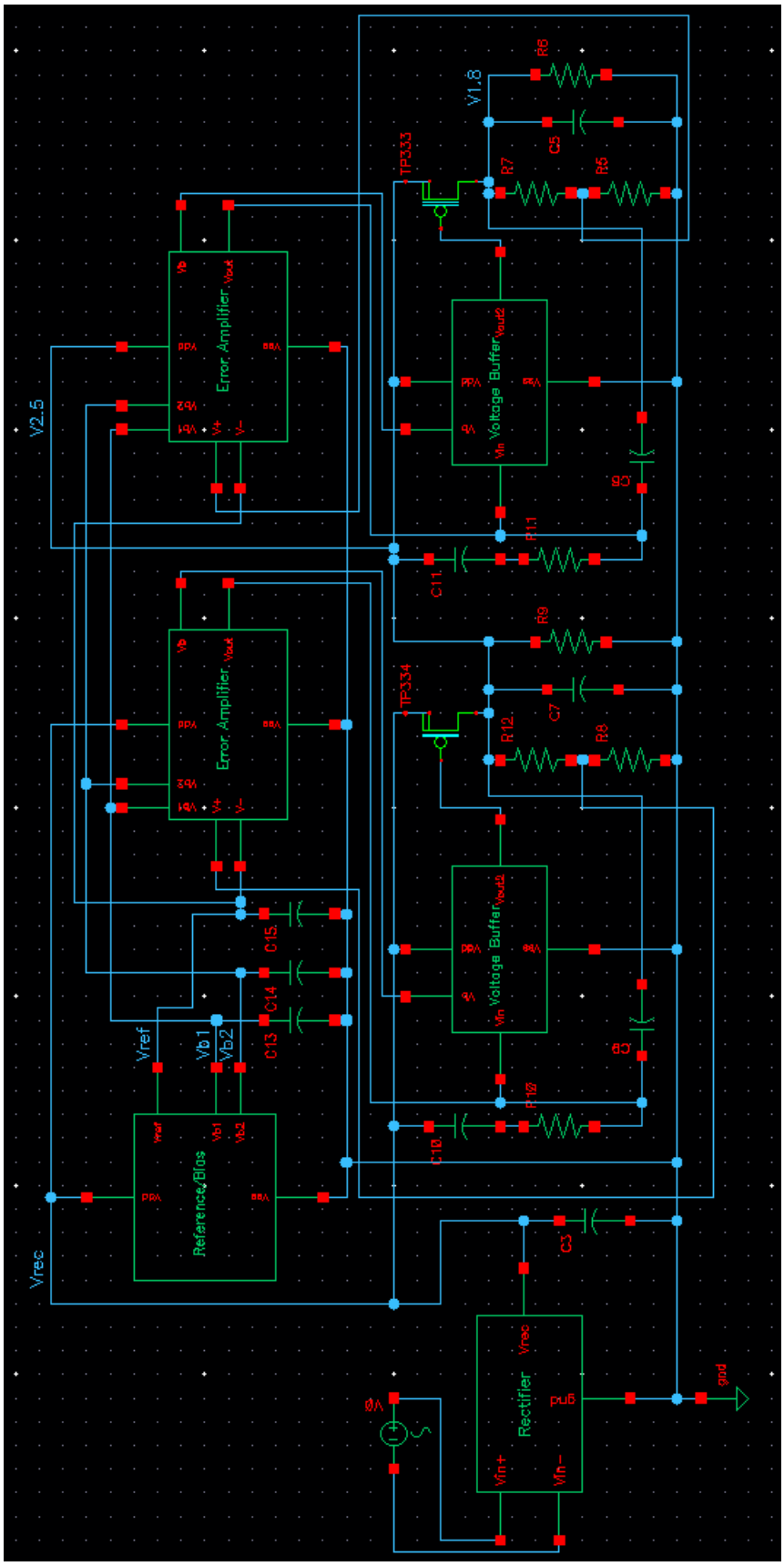


Figure A.2: Power conditioning circuit schematic implemented in Cadence Virtuoso.

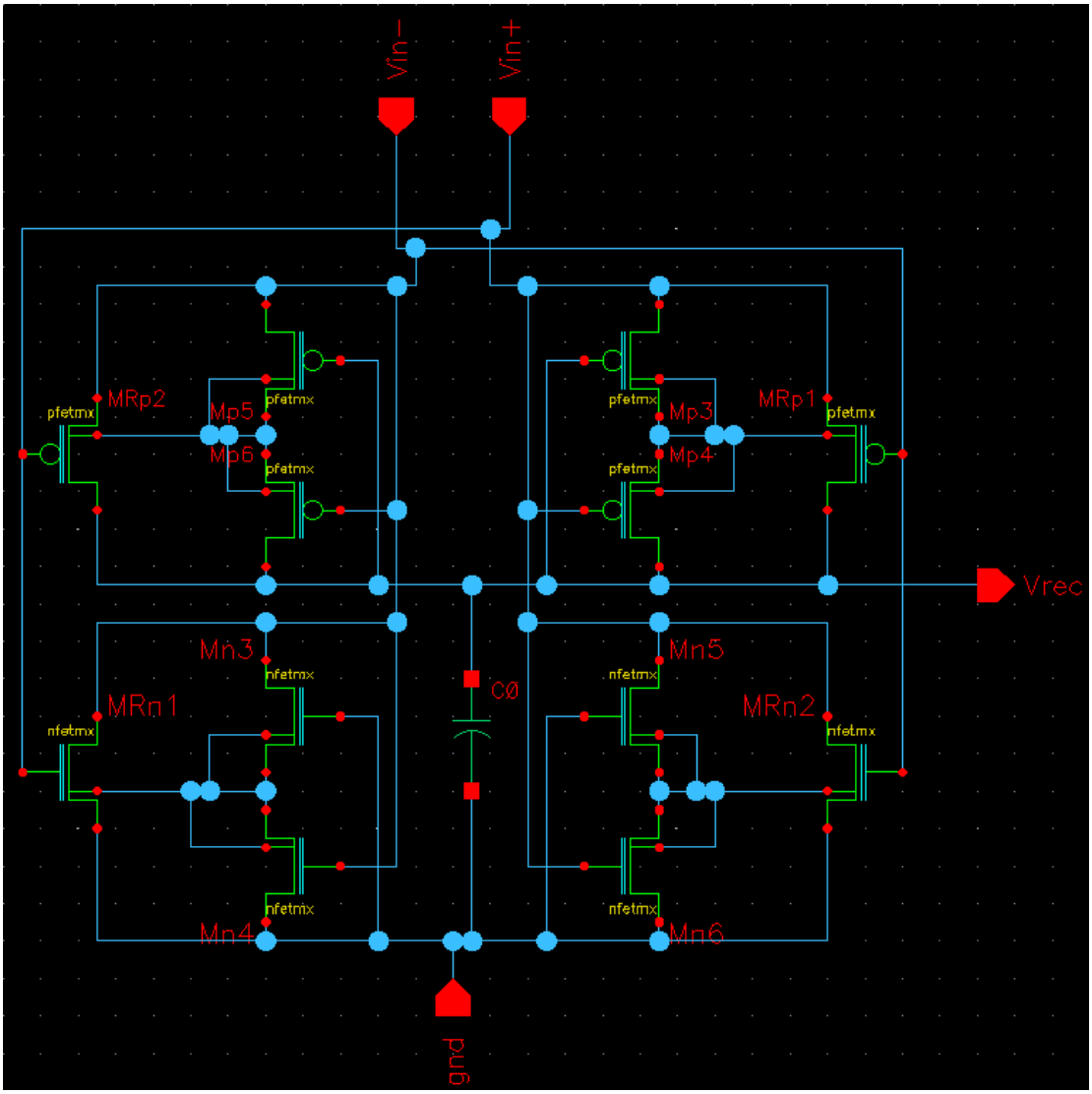


Figure A.3: Full-Wave rectifier with substrate leakage reduction implemented in Cadence Virtuoso.

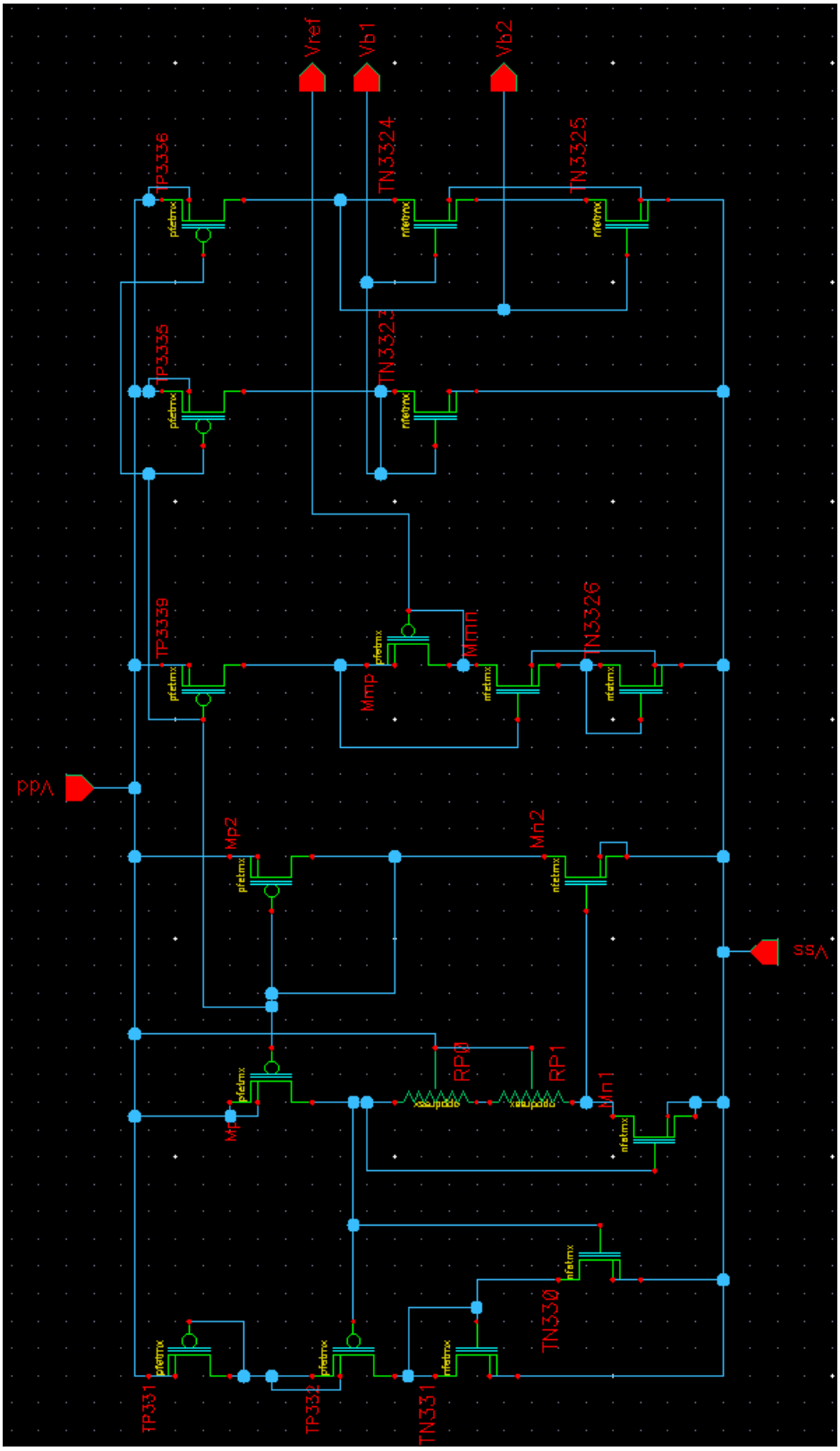


Figure A.4: Voltage reference and bias circuit schematic implemented in Cadence Virtuoso.

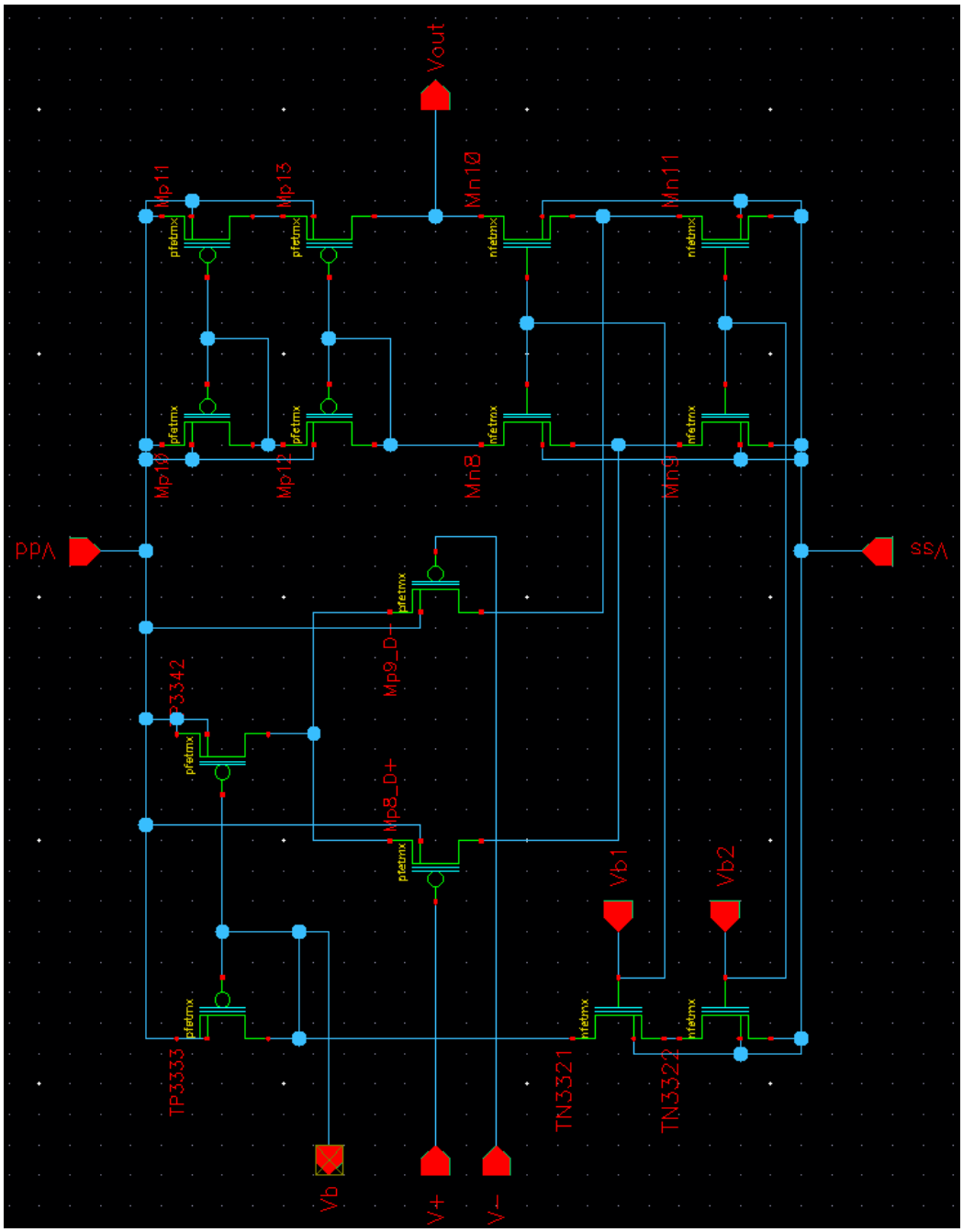


Figure A.5: Folded cascode OTA as a error amplifier circuit schematic implemented in Cadence Virtuoso.

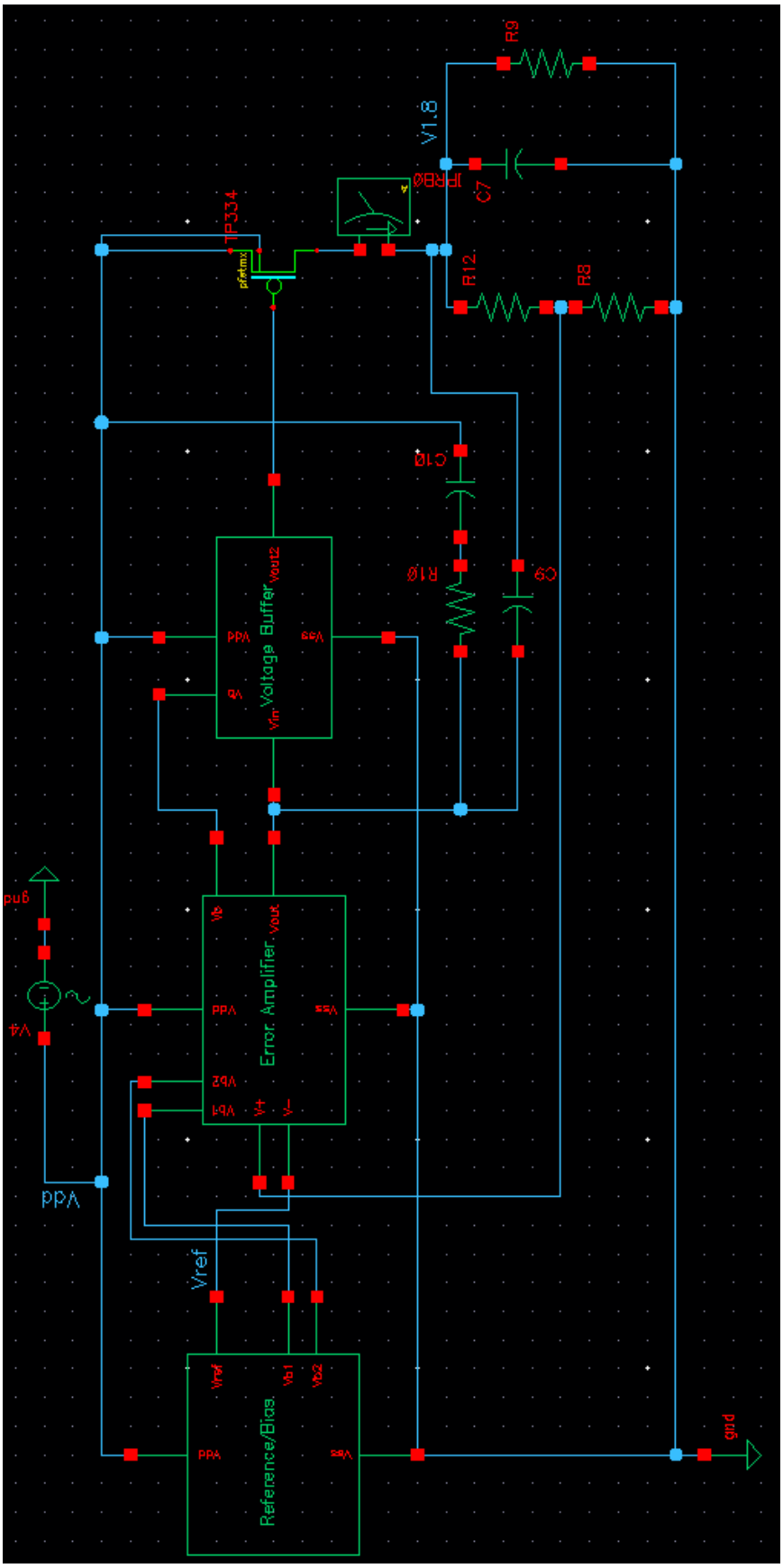


Figure A.6: LDO regulator circuit schematic implemented in Cadence Virtuoso.

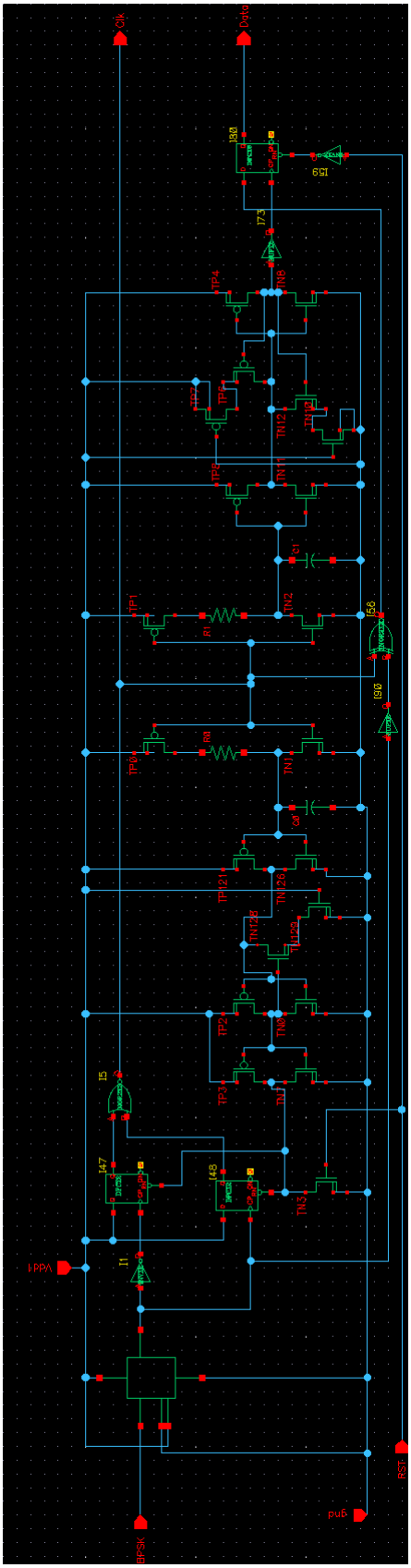


Figure A.7: BPSK demodulator circuit implemented in Cadence Virtuoso.

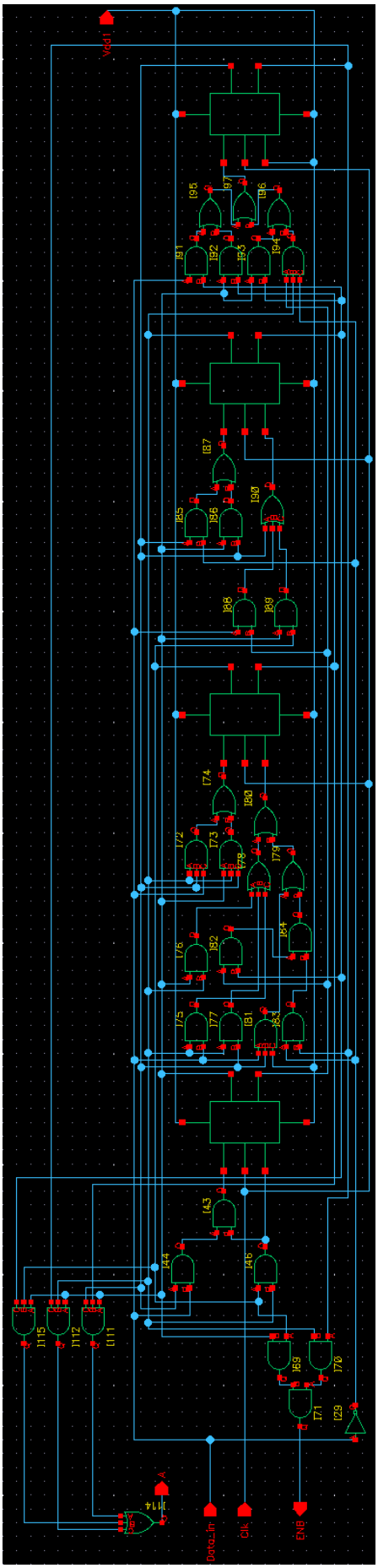


Figure A.8: Finite state machine using JK flip-flops implemented in Cadence Virtuoso.

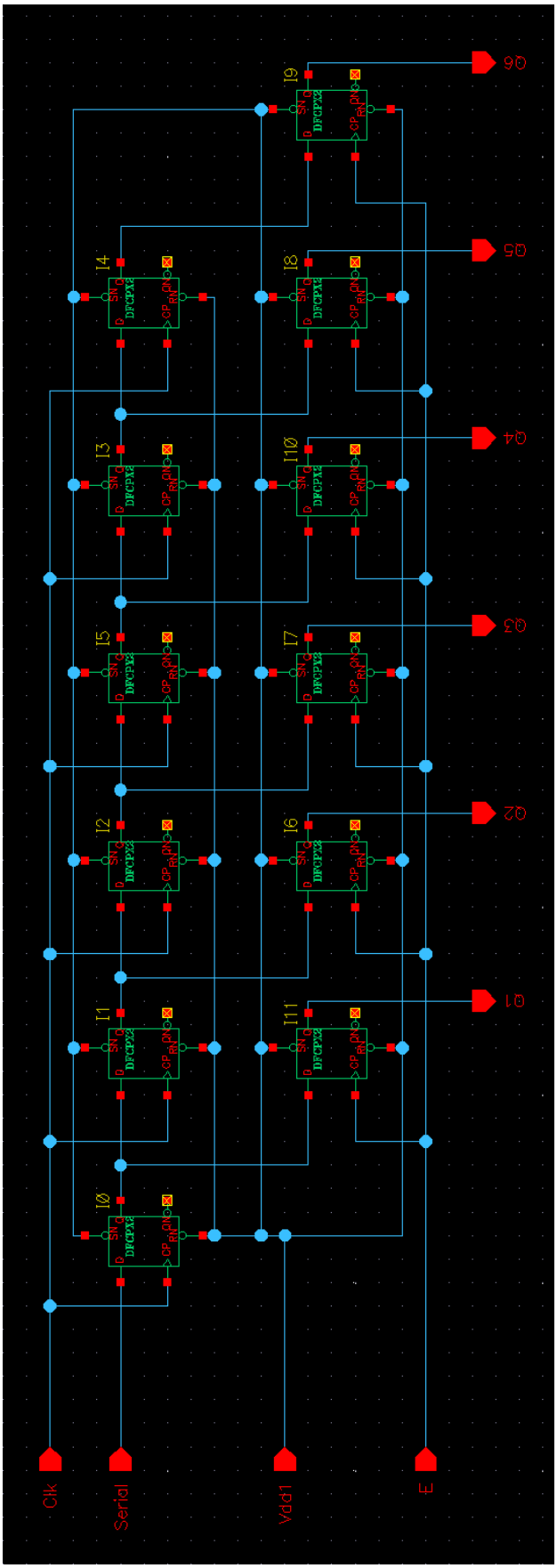


Figure A.9: Serial-in Parallel-ou 6-bit shift register with output registers implemented in Cadence Virtuoso.

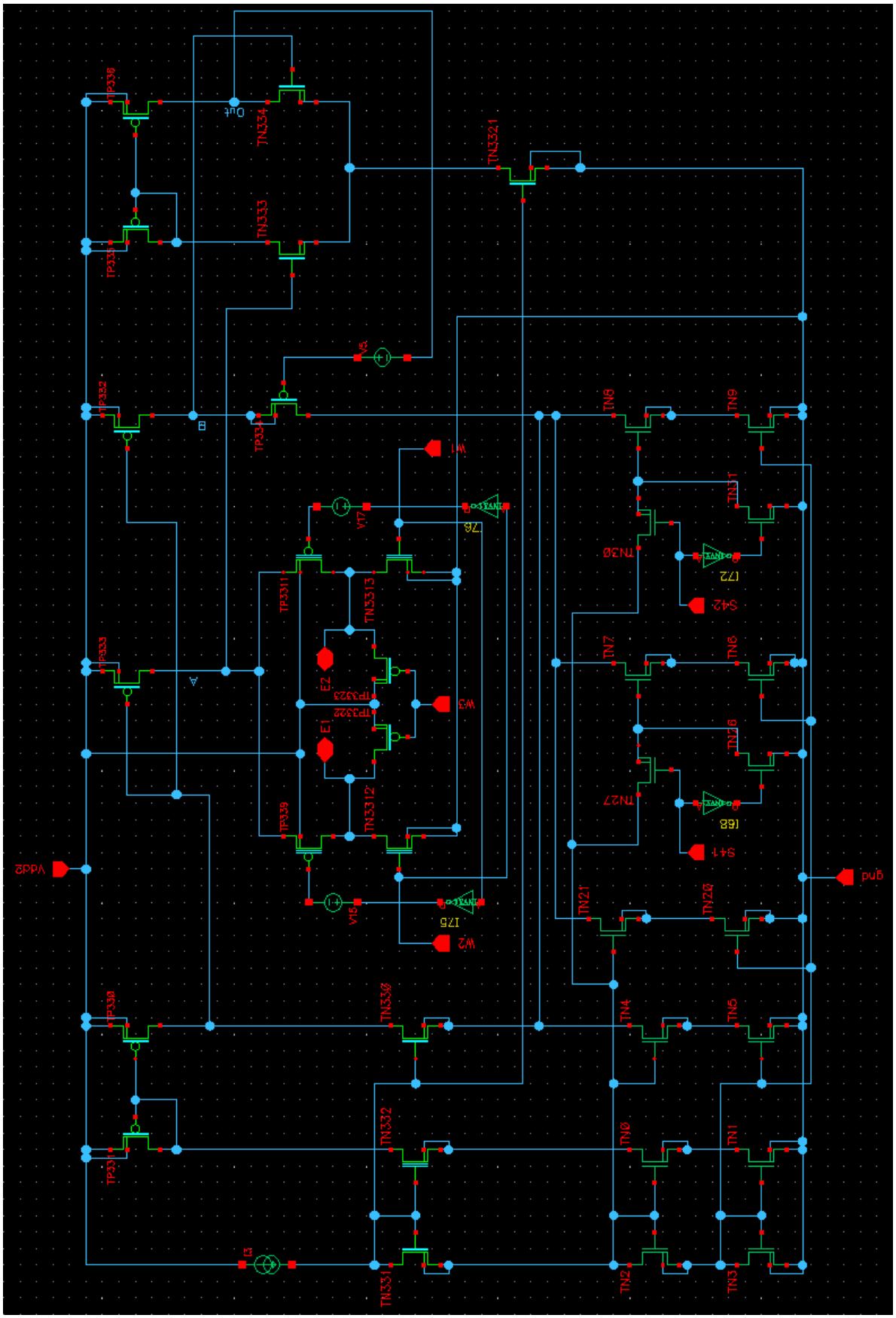


Figure A.10: Programmable 2-bit current source circuit implemented in Cadence Virtuoso.

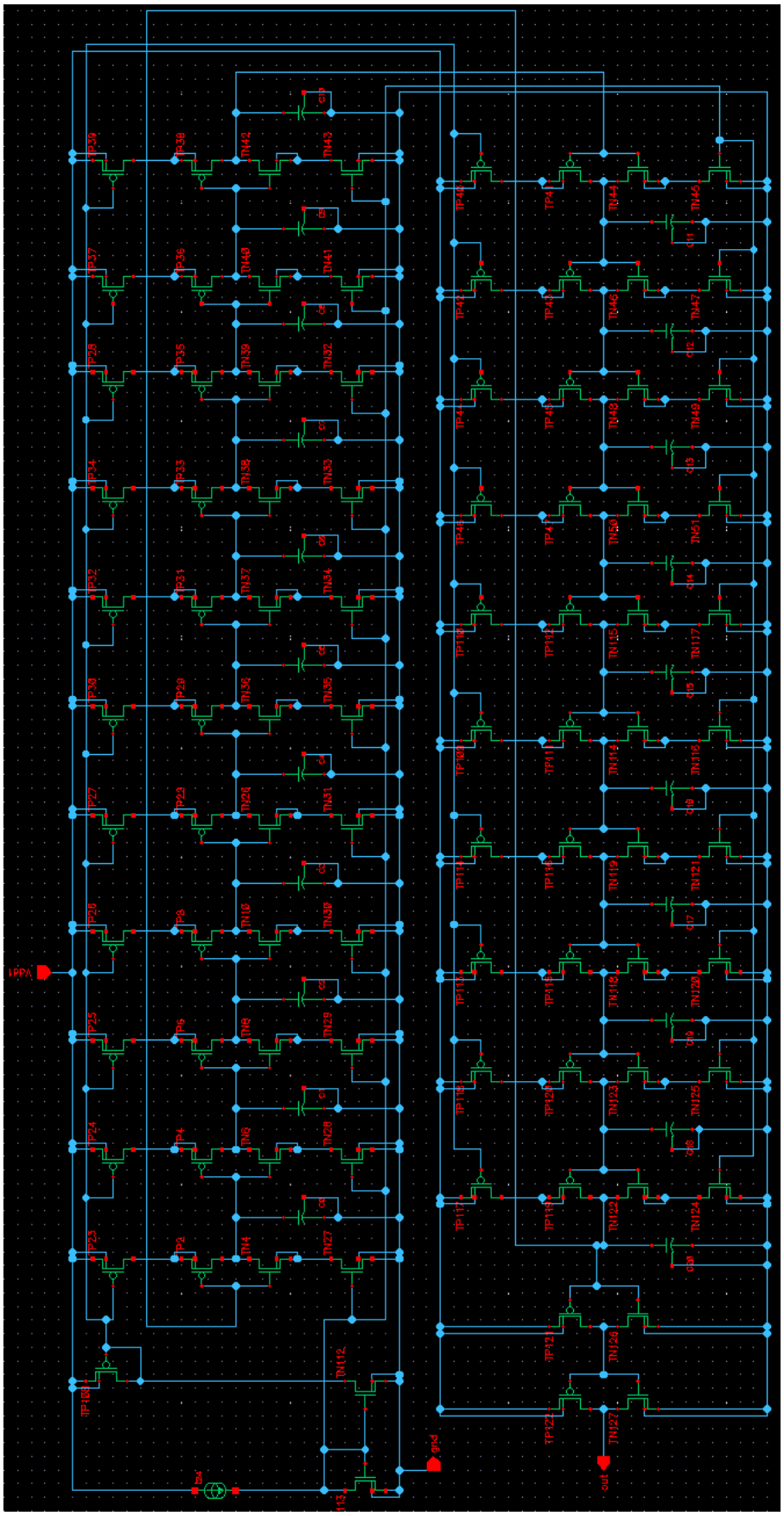


Figure A.11: CMOS current starved ring oscillator circuit implemented in Cadence Virtuoso.

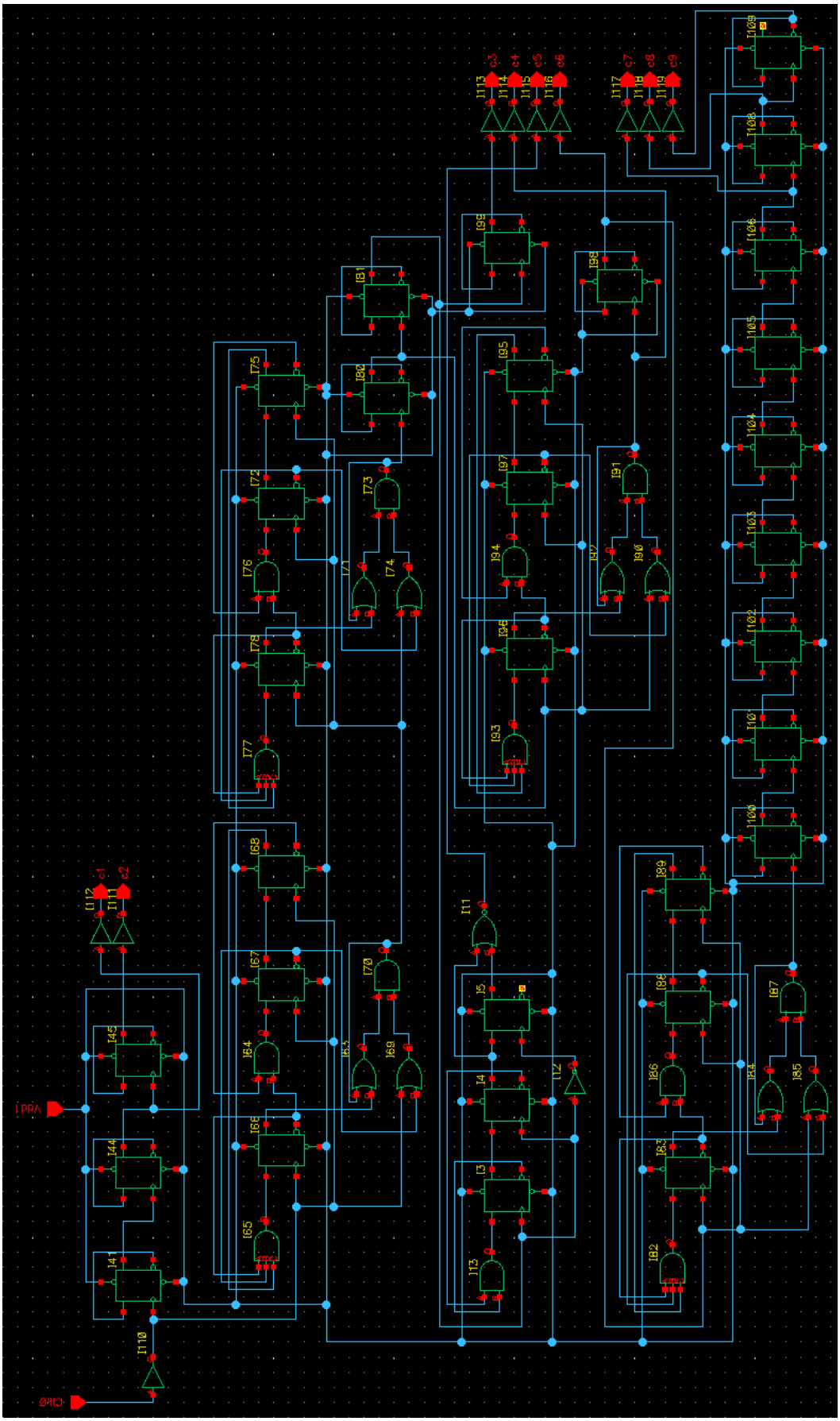


Figure A.12: Circuit able to generate clock signals with different frequencies implemented in Cadence Virtuoso.

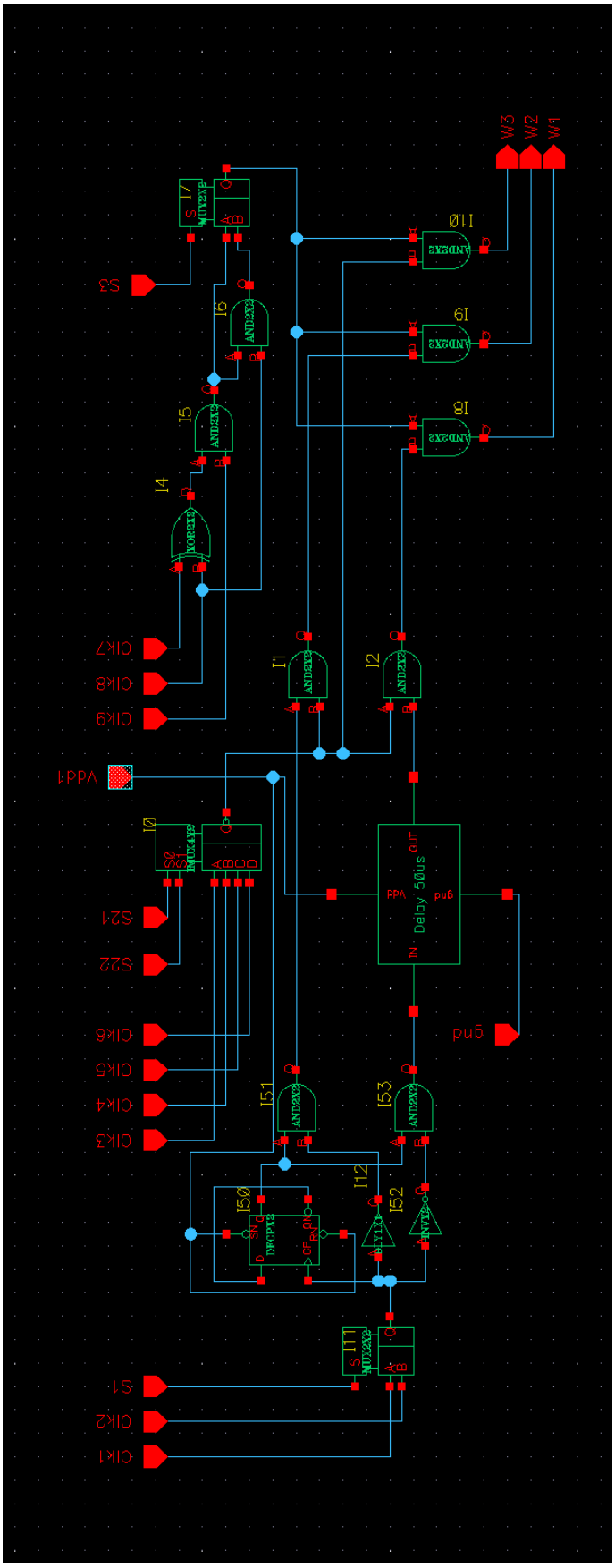


Figure A.13: Digital stimulus generation circuit implemented in Cadence Virtuoso.

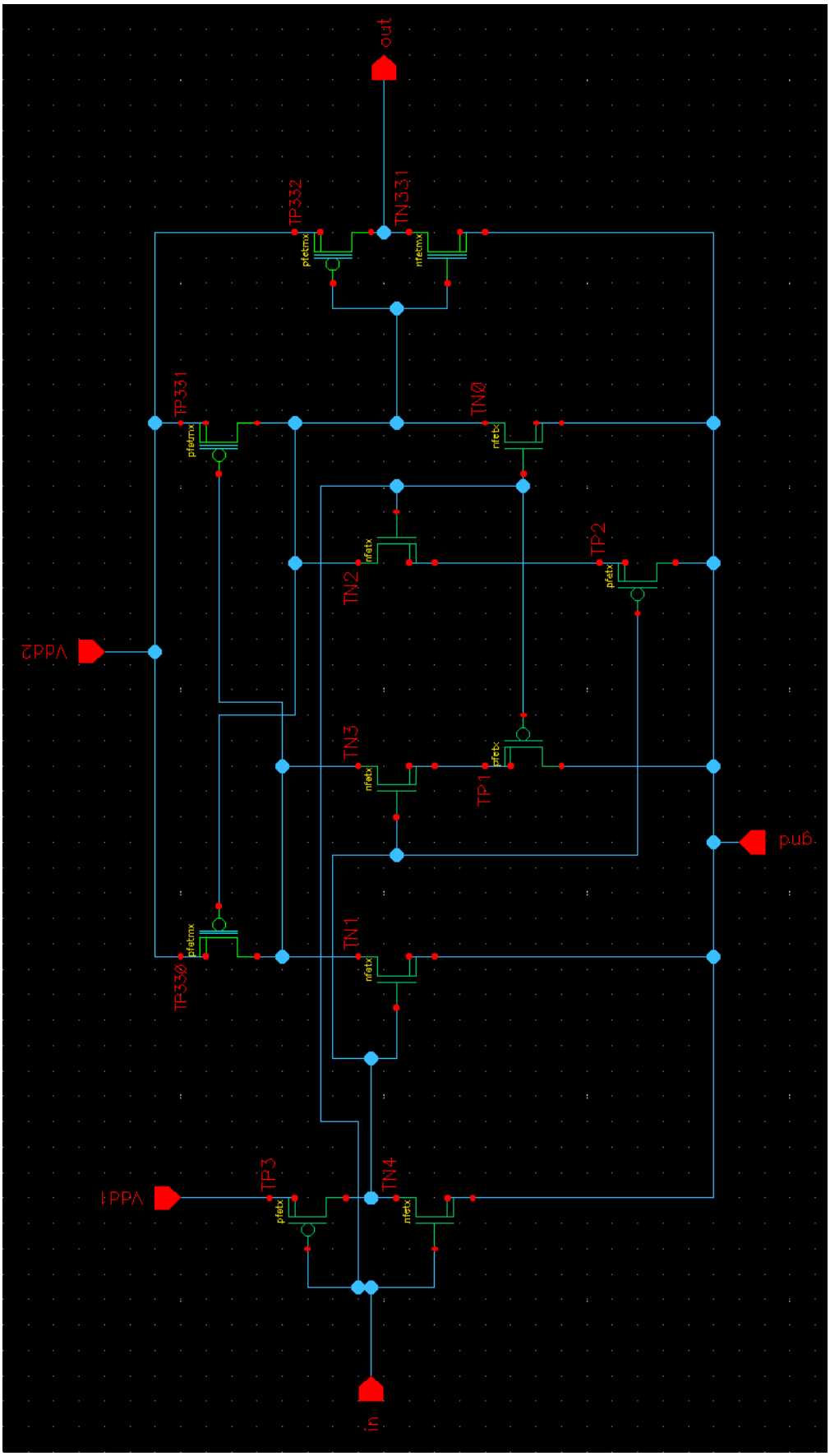


Figure A.14: Voltage level converter from low (1.8 V) to medium-voltage (2.5 V) implemented in Cadence Virtuoso.

Appendix B

Appendix B

B.1 Optimization Strategy

```
%% Optimization Strategy
% Renato Borges, up201406848@fe.up.pt
% Master Thesis – 2016
close all; clear all; clc;

    f = 13.56e6; % Operating Frequency

%% Electronic Design
% Calculation of the transfer frequency and the secondary circuit
% components (coil, capacitors, rectifier and regulator)
% Determination of the primary circuit (including the driver)
% Verification of the electronic design by Spice simulations
    [L20,Q20,R20ac,R20dc] = SecondaryCoil(1);
    k = 0.005;      % WCS for the coupling factor

%% Electronic Design of the Secondary Link Circuit
    RL = 5e3;
    [secondary_data] = ED_SecondaryLink(RL,L20,k,f);
    clearvars -except secondary_data k f

%% Electronic Design of the Primary Link Circuit
    V2  = 5;        % targeted voltage at secondary
    Nt1 = 4;        % number of turns of primary coil
    f0  = 15e6;     % semi-resonance frequency
    DC  = 0.4;      % duty-cyle
    [primary_data] = ED_PrimaryLink (secondary_data,f,f0,DC,V2,Nt1);
    clearvars -except secondary_data primary_data

%% Overall Efficiency
n_overall     = ((secondary_data{10,2}/100)*(primary_data{17,2}/100))*100;

```

```
%% Table Write
labels = [primary_data(:,1);secondary_data(:,1);{'Overall'}];
calculations = [cell2mat(primary_data(:,2));cell2mat(secondary_data(:,2));n_overall];
Table_data = table(calculations,'RowNames',labels);
writetable(Table_data,'ResultsData.xls','WriteRowNames',true)
```

B.2 Design of the Secondary Coil

```
function [L2,Q2,R2ac,R2dc] = SecondaryCoil(Nt2)
    f = 13.56e6;                            % Operating Frequency
    y = 0.0177047;                          % Skin-depth (mm)
    R = 2.18*(1+0.00393*(40-20));           % Resistivity - Ohm/m
    mm2in = 0.0393701;

%% Implantable Coil (Receiver) - Single Layer - Enameled Copper Wire (38 AWG)
    AWG = 38;
    dw = 0.127*(92^((36-AWG)/39));  % mm
    rw = dw/2;  % mm
    ow = pi*((dw/2)^2);             % mm2
    r2 = 2; l2 = 6;                 % radius and length of the coil (mm)
% Inductance - single layer very long solenoid (ideal) - l>>2R
    F = 0.013;      % diameter/lenght (4/6)
    L2 = F*(Nt2^2)*2*r2*mm2in*(10^(-6));
% Resistance
    lw = 1.6*(2*pi*r2*Nt2);     % mm
    R2dc = R*(lw/1000);         % DC resistance
    R2ac = R2dc*((rw/(2*y))+0.25+(3/64)*((2*y)/rw)); % AC resistance
% Unloaded Quality Factor
    Q2 = (2*pi*f*L2)/R2ac;
end
```

B.3 Electronic Design of the Secondary Link

```
function [secondary_data] = ED_SecondaryLink(RL,L20,k,f)
    Q2 = 90; % realistic guess of secondary quality factor

for i=1:8
    Q1 = 600;
%% Calculation of ALFA_opt for Maximal Link Efficiency - Step 2
% Solution at Maximal Link Efficiency
    X           = (k^2)*Q1*Q2;
    ALFA_opt    = Q2/sqrt(1+X);
%% Match L2 to the load R_load2, resulting in matched L2(f)
```

```
% Optimizing ALFA for a givem A.C. Load R_load2 and transfer frequency
% w_resP, corresponds to matching C2 and L2 to the load R_load2
    L2_opt = (RL/(2*pi*f))*(ALFA_opt/((ALFA_opt^2)+1));

%% Calculate N2 using the geometry L2, resulting in matched N2(f)
    n2 = round(sqrt(L2_opt/L20));    % optimal number of windings
    [L2,Q2,R2ac,R2dc] = SecondaryCoil(n2);
i=i+1;
end

% Calculate the matching C2
    C2_opt  = ALFA_opt/(2*pi*f*RL);     % Capacitor for resonance
% Link gains at maximal Efficiency
    X               = (k^2)*Q1*Q2;                  % Abbreviation for k^2*Q1*Q2
    ef_link_max     = (X/((1+sqrt(1+X))^2))*100;    % Maximal Link Efficiency
    ALFA            = 2*pi*f*C2_opt*RL;
    ef_primary      = ((k^2)*Q1*Q2)/(1+(Q2/ALFA)+((k^2)*Q1*Q2));
    ef_secondary    = Q2/(ALFA+Q2);
    ef_link         = (ef_primary*ef_secondary)*100;

%% Optimized Parameters
    names   = {'R_load2 ';'k       ';'X        ';'ALFA_opt';'L_s2    '; ...
        'n2      ';'R_ac2   ';'Q_Ls2   ';'C2     ';'n_link  '};
    values  = {RL; k; X; ALFA_opt; L2; n2; R2ac; Q2; C2_opt; ef_link};
    secondary_data = [names,values];
end
```

B.4 Design of the Primary Coil

```
function [L1,Q1,R1ac,R1dc] = PrimaryCoil(Nt1)
    f = 13.56e6;                    % Operating Frequency
    O = 0.0177047;                  % Skin-depth (mm)
    mm2in = 0.0393701;

%% External Coil (Transmitter) - Enameled Copper Wire (18 AWG)
    AWG = 18;
    dw = 0.127*(92^((36-AWG)/39));  % mm
    rw = dw/2;  % mm
    ow = pi*((dw/2)^2);     % mm2
    r1 = 80; l1 = 10;       % radius and length of the coil (mm)
% Inductance - single layer short solenoid
    F = 0.05845; % diameter/lenght (160/10)
    L1 = F*(Nt1^2)*2*r1*mm2in*10^(-6);
% Resistance
    lw = 1.5*(2*pi*r1*Nt1); % mm
    R = (1.71*10^(-8))/(ow*10^(-6));                    % Resistivity - Ohm/m
```

```
    R1dc = R*(lw/1000);                                    % DC resistance
    R1ac = R1dc*((rw/(2*O))+0.25+(3/64)*((2*O)/rw));       % AC resistance
% Unloaded Quality Factor
    Q1 = (2*pi*f*L1)/R1ac;
end
```

B.5 Electronic Design of the Primary Link

```
function [primary_data] = ED_PrimaryLink (secondary_data,f,f0,DC,V2,Nt1)
    ALFA    = secondary_data{4,2};  % ALFA for maximal link efficiency
    Q2      = secondary_data{8,2};  % Quality Factor
    X       = secondary_data{3,2};
    L2      = secondary_data{5,2};
    k       = secondary_data{2,2};
    w       = 2*pi*f;

%% Primary Coil
    [L1,Q1,Rs1,R1dc] = PrimaryCoil(Nt1);

%% Calculate the Driver Parameters in function of L1 (pg.138)- Step 1
% Compute Req and the link gain A
    R_eq    = (k^2)*L1*w*((ALFA*Q2)/(ALFA+Q2));
    A_stp   = (k*sqrt(L2/L1)*Q1*Q2*sqrt((ALFA^2)+1))/(ALFA*(k^2)*Q1*Q2+ALFA+Q2);
    r_m_ptp = w*L1*A_stp;      % Transimpedance for Parallel Resonant Prim
% Compute Req and the link gain A @ MAXEFICIENCY
    R_eq_opt    = Rs1*(X/(1+sqrt(1+X)));
    A_stp_opt   = ((k*sqrt(L2/L1)*Q1)/(1+sqrt(1+X)))*(sqrt((1+X+(Q2^2))/(1+X)));
    r_m_ptp_opt = w*L1*A_stp_opt;

%% Semi-Resonant Primary
    w0 = 2*pi*f0;
    w  = 2*pi*f;
    C1_res  = L1/((w0^2)*(L1^2)+((Rs1+R_eq)^2));
    R = (Rs1+R_eq)/((1-((w/w0)^2))^2);
    L = L1/(1-((w/w0)^2));
        Leq     = L;
        Rs1_r   = R;

%% Design Flow
    [V1, I1, Vcc, Vcc_real, Icc, L_ch, C1_par, C1_ser, vs_MAX, is_MAX, ...
        ef_classE] = ClassE_DesignFlow(f, DC, V2, Rs1_r, Leq, A_stp);

%% Optimized Parameters
    names   = {'Ls1       ';'n1        ';'R_ac1     ';'Q_Ls1     ';'C1        ';...
        'Vcc       ';'Vcc_real  ';'Icc       ';'V_prim    ';'vs_max    ';...
        'I_prim    ';'is_max    ';'C_1par    ';'C_1ser    ';'Lchoke_min';...
```

```
        'D          ';'n_driver  ';};
    values  = {L1; Nt1; Rs1; Q1; C1_res; Vcc; Vcc_real; Icc; V1; vs_MAX; ...
        I1; is_MAX; C1_par ;C1_ser; L_ch; DC; ef_classE;};
    primary_data = [names,values];

end
```

B.6 Class-E Design Flow

```
function [V1,I1,Vcc,Vcc_real,Icc,L_choke,C1_par,C1_ser,vs_MAX,...
is_MAX,ef_classE] = ClassE_DesignFlow(f,DC,V2,Rs1_real,Leq,A_stp)

%% The Class-E Design Flow - pg.134
    w       = 2*pi*f;
    [T] = transistor(DC);

    V1      = V2*A_stp;             % A.C. Link input Voltage
    I1      = V1/(w*Leq);           % A.C. Link input Current
    y       = pi*(1-DC);            % Half off-time (radians)
    yy      = (sin(y)/y)-cos(y);
    xx      = (((T{10,2}*y)/pi)*cos(y))-((1+(T{10,2}/pi))*sin(y));
    fi      = atan(yy/xx);
    g       = y/(cos(fi)*sin(y));
    q1      = -2*g*sin(fi-y)*sin(y)-(2*y*sin(y));
    q2      = 2*y*cos(y)-(2*sin(y));
    q3      = -0.5*g*sin(2*y);
    tanW    = (q1*sin(fi)+q2*cos(fi)+q3*cos(2*fi)+g*y)...
        /(q2*sin(fi)+q3*sin(2*fi)-q1*cos(fi));
% Driver Components in function of L1
    C1_par  = (2*(y^2)+2*y*g*sin(fi-y)-(2*g*sin(fi)*sin(y)))...
        /(w*pi*(g^2)*Rs1_real);         % Parallel Cap in ClassE
    C1_ser  = 1/(w*(w*Leq-(Rs1_real*tanW)));    % Series   Cap in ClassE
% Driver Supply Voltage and Current in function of L1
    Icc     = V1/(g*w*Leq);         % D.C Supply Current of Primary Coil Driver
    Rcc     = ((g^2)*Rs1_real)/2;
    Vcc     = Rcc*Icc;              % D.C Supply Voltage of Primary Coil Driver
    L_choke = (Rcc/w)*50;           % Minimum Value
% Peak Switch Voltage and Current in function of L1
    teta_max = asin(1/g)-fi;
    vs_MAX   = (Icc/(w*C1_par))*(y-(pi/2)+teta_max+...
        g*(sin(fi-y)+cos(fi+teta_max)));    % v_sMAX = v_sOFF @ teta_max
    if ((y-pi)<fi)
        is_MAX = Icc*(1+g);
    else
        is_MAX = 0;     % i_sMAX = i_sOFF
    end
```

```
    I_ON     = Icc*(1-g*cos(fi+y));
    I_OFF = Icc*(1-g*cos(fi-y));
% Driver Efficiency in function of L1
    p_R      = 1;
    p_R_ON   = (T{3,2}/(pi*Rs1_real))*((1+(2/(g^2)))*(pi-y)+...
    ((4/g)*sin(y)*cos(fi))-((sin(2*y)*cos(2*fi))/2));
    p_V_Sat  = T{11,2}/Vcc;
    p_t_F    = (((I_OFF^2)*(T{7,2}^2))/(24*C1_par))*f;
    p_t_R    = (((I_ON^2)*(T{8,2}^2))/(24*C1_par))*f;
    p_L_S    = ((T{6,2}*(I_OFF^2))/2)*f;

    ef_classE  = (p_R/(1+p_R_ON+p_V_Sat+p_t_F+p_t_R+p_L_S));
    Vcc_real = Vcc/ef_classE;
end
```

B.7 Switch Transistor Specifications

```
function [T] = transistor(Dcycle)
% Transistor Si155DL
    V_Sat            = 20;          % Maximum Drain-Source Voltage
    Vsat             = 0.3;
    I_max            = 0.7;         % Maximum Drain Current
    R_ON             = 0.5;         % On Resistance
    C_G              = 20e-12;      % Gate Capacitance (Input)
    C_DS             = 13e-12;      % Drain Source Capacitance (Output)
    L_S              = 10e-9;       % Parasitic Inductance of BS170 (table 5.3)
    t_F              = 10e-9;       % switch fall times
    t_R              = 16e-9;       % switch rise times
% Class-E parameters
    D                = Dcycle;       % Duty-Cycle
    C                = 0;            % Normalized turn-on slope

    names    = {'V_Sat';'I_max'; 'R_ON ';'C_G  ';'C_DS  ';'L_S  ';'t_F  ';...
        't_R  ';'D    ';'C     ';'Vsat '};
    values   = {V_Sat; I_max; R_ON; C_G;  C_DS; L_S; t_F; t_R; D; C; Vsat};
    T = [names,values];
end
```

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