FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO

Inductorless DC-DC Converter

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FINAL VERSION

Mestrado Integrado em Engenharia Eletrotécnica e de Computadores

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July 27, 2016

Resumo

Assim que a eletricidade se tornou um bem essencial, trouxe consigo a necessidade de conversão de energia. Os conversores CC-CC fazem parte desta classe e desempenham a tarefa de converter um sinal de tensão constante e estável, num sinal de outro nível. A forma de cumprir este objetivo mudou com o decorrer dos tempos. Anteriormente ao aparecimento dos semicondutores de potência, converter um nível de tensão constante noutro passava por primeiro converter esse sinal num sinal AC, converter o seu nível com um transformador e retificar a onda para obter novamente um sinal CC. Até aos dias de hoje continua-se a investigar nesta área porque os desafios assim o exigem e as ferramentas tecnológicas, mais poderosas, também assim o permitem. Os conversores CC-CC são usados em dispositivos portáteis, alimentados a bateria, que podem conter em si subsistemas a operar com diferentes níveis de tensão, sendo também commumente utilizados em sistemas de captação de energia.

O uso de indutores sempre foi uma componente forte na construção de conversores CC-CC, no entanto, a dado momento surgiram alternativas usando apenas condensadores. O principio de funcionamento passa sempre por armazenar energia em componentes eletrónicos capazes disso, como é o caso do indutor e do condensador, e comuta-los através de dispositivos semicondutores, libertando a energia armazenada a um nível de tensão diferente. Mas quando se fala de circuitos integrados, o indutor torna-se pouco desejável pois é origem de interferência eletromagnética, é caro, espaçoso, mas acima de tudo, difícil de integrar. A alternativa aos indutores passa por usar o *Charge Pump*, um tipo de circuito de condensadores comutados que permite obter uma tensão a um nível diferente da alimentação, abdicando do uso de indutores.

Este trabalho apresenta um circuito *Charge Pump* que cumpre determinados objetivos de desempenho e que é projetado para suportar variações de alimentação, de processo e temperatura. As especificações que serão almejadas são, nomeadamente: a tensão de entrada e sua variação admitida e tensão de saída e variação tolerada. Utiliza *Charge Pumps* auxiliares para implementar técnicas de *gate-boostrapping* para elevar o sinal de comando da comutação acima da alimentação, diminuindo a resistência dos interruptores, causando menos perdas e permitindo aumentar a frequência o que poupa no tamanho dos condensadores. Para regular a saída apresenta-se uma proposta de *Pulse-Skipping*, juntamente com PWM, que pode ser realizada com comparadores e lógica simples. Este trabalho é realizado em ambiente empresarial, na Synopsys - Portugal.

Abstract

DC-DC converters are an area of interest since electricity emerged as a common utility. They perform the task of converting a constant and stable voltage signal into another of different level. The way to achieve this goal has changed over time. Before power semiconductors were available, converting a constant level of voltage into another would demand converting the DC voltage into AC first, then the amplitude adjusted with the help of a transformer followed by a rectifier, that would recover the DC voltage to a different level. Even today, investigation still continues on these matters, because the challenges so requires and technological tools, more powerful,also allows it. DC-DC converters are used in portable devices that are battery powered, which can contain in themselves subsystems operating at different voltage levels, and are also commonly used in energy harvesting systems.

The use of inductors has always been a strong component in the construction of DC-DC converters, however, alternatives have emerged using solely capacitors. The operating principle always consists in storing energy in electronic components capable of such, as it is the case of the inductor and capacitor, and switching them through semiconductor devices, releasing the stored energy at a different voltage level. But when it comes to integrated circuits, the inductor becomes undesirable as it is a source of electromagnetic interference, it is expensive, spacious but above all, difficult to integrate. Charge Pumps have become a viable alternative to the use of inductors, a type of switched capacitor circuit that enables a voltage conversion avoiding the use of inductors.

This work presents a Charge Pump circuit that meets certain performance goals and is designed to support changes in process, voltage and temperature. Auxiliary Charge Pumps implement gate-boostrapping techniques that raises the switching command voltage above the power supply, in order to reduce the equivalent resistance of the switches, causing lower losses, allowing increased frequency operation, thus saving capacitor size. To adjust the output a Pulse-Skipping Control is proposed along with PWM control, which can be realized with comparators and simple logic. This work is carried out in a business environment, more specifically at Synopsys - Portugal.

Acknowledgements

Firstly I thank my parents for supporting me in all my academic and non-academic decisions. Also I am very thankful for the sacrifices they made throughout the years in order for me to have a good education.

To my girlfriend that supported me for most my university years and for her understanding towards my reduced availability during the elaboration of this thesis.

To all my friends at FEUP that shared with me these five years of friendship, study and laughs.

To the analogue team at Synopsys for the support with the complex tools, the good work environment, the afternoon snacks and above all for the constant reminder of having a Thesis to do.

To my supervisors Joaquim Machado and Prof. Vítor Grade Tavares for allays finding time, in their busy schedules, for me and contributing with very valuable ideas for this work.

Fábio Pascoal

"Study hard what interests you the most in the most undisciplined, irreverent and original manner possible."

Richard Feynman

Contents

List of Figures

List of Tables

Abbreviations, Acronyms and Symbols

AC	Alternate Current
CMOS	Complementary Metal-Oxide-Semiconductor
CTS	Charge Transfer Switch
DC	Direct Current
IC	Integrated Circuit
NMOS	N-type Metal-Oxide-Semiconductor
OLED	Organic Light-Emitting Diode
PMOS	P-type Metal-Oxide-Semiconductor
PWM	Pulse Width Modulation
PVT	Process Voltage Temperature

Hz	Hertz
nm	nanometre
V_{ov}	Overdrive Voltage
V_{th}	Threshold Voltage

Chapter 1

Introduction

DC-DC converters have been the aim of much research and attention throughout time. Recently, with the increase in importance of portable devices, DC-DC converters became even more relevant. This is true because portable devices are battery supplied and batteries show varying voltage levels as they discharge, additionally subsystems of a device can have different energy requirements from what is made available by the main supply. Frequent solutions for DC-DC conversion involve inductors, however, for chip applications this is not desirable, since integrating inductors can be even impossible if above a few nano-Henrys and also they cause electromagnetic interference. First proposed by Cockcroft-Walton [1] Charge Pump circuits make DC-DC conversion possible using only capacitors switched in a controlled fashion through semiconductor devices. Later an integrated version was proposed by J. F. Dickson [2]. This work aims at researching existing topologies, evaluating them and designing a circuit architecture, in a 28nm process, with validation of performance parameters and robust to manufacturing imperfections, temperature and supply variation. Some contributions of this work include switches controlled with above supply levels, techniques to achieve such levels, and Pulse-Skipping plus Pulse Width control scheme to regulate the output to the target specifications. Also, challenges and solutions relating with full-corner validation are included, which is rarely occurring in most literature.

In short, the challenge is to design a Charge Pump based DC-DC converter fulfilling certain performance goals, mentioned later and with full-corner and monte-carlo validation. Techniques that focus on efficiency and area reduction are also used.

1.1 Motivation

Power management is a fundamental issue in electronics. Devices can contain sub-systems that operate at specific voltages for which there isn't available supplies. This generalization includes a huge range of devices from industrial to domestic. Electronic devices that operate plugged-in into the grid may have transformers that change the voltage level of the AC supply to whatever is needed and then rectify the wave. But transformers are heavy and expensive and if different parts of the systems need different voltages it is much easier to use higher frequency switched DC-DC

converters, because the higher frequencies allows for smaller and lighter transformers or inductors. With regard to on chip applications, this problem is even more important because inductors are hard to integrate and are limited to very low inductances. Furthermore, electronic devices such as laptops, cellphones and portable media players operate from batteries, which present a decaying voltage level as they discharge, along with having to supply sub-circuits with different voltage requirements. Charge Pumps offer the possibility to have DC-DC converters operating only with capacitors and semiconducting elements. Charge pump DC-DC converters have recently been applied in OLED displays [6], solar energy harvesting [7, 8] and even thermoelectric harvesting [9]. Also some others have been allowing the possibility of having multi-mode conversion capabilities in systems [10]. A few authors had objectives more similar to this work, such as avoiding inductors and using above supply gate signals in the operation of switches [11, 5]. The circuit that this work aims to achieve should be able to convert 0.8V to a stable 1.2V supply using a 28nm CMOS process. Moreover, it should be validated for all corner operation.

1.2 Challenges and proposed solution

Challenges of this work involve choosing an adequate topology, keeping in mind the performance goals, which requires the understanding of the nuances of the different topologies and their trade-offs. As to be seen later, a big challenge to face is to adequately control the switches. These switches can be realized in different ways but turning them *on* and *off* in precise times is challenging. Their resistance, when conducting, is limited, requiring gate bootstraping techniques to achieve the goals. Gate bootstrapping is a technique that consists in using voltages higher than the supply at the gate of the transistor.

Ensuring that the circuit is robust to process, temperature and supply variations, is hard to accomplish since semiconductors' behaviour varies highly with these variables. Not all circuits will be able to handle such variations. A robust architecture that can deal with such variations will become a crucial factor in the design development.

Assuring an output as desired, a crucial factor for a DC-DC converter, when a load is unknown and can vary greatly requires some kind of close-loop control. A Pulse-Skipping with Pulse-Width-Modulation control will be used.

1.3 Objectives

The objective of this work is to design a converter fulfilling certain performance goals and validate the design for full corner operation. The goal is to convert a 0.8V ($\pm$10%) to a stable 1.2V ($\pm$5%) output able to supply a current up to 20mA.

1.4 Dissertation Structure

The document is organized as follows:

- Chapter 2 is intended to present the way Charge Pumps are typically made. The first Charge Pump known is presented, the Cockcroft-Walton Charge Pump. The Dickson Charge Pump in which a lot of Charge Pumps, to this day, are still based is mentioned. The CTS based Charge Pump that innovated the way Charge Pumps were made and is of particular importance to this work will be also presented. Finally, more recent topologies are presented. Throughout this chapter, there are references to articles and works devoted to the same aspects mentioned in the chapter. In short, this chapter exposes how Charge Pumps were developed throughout the literature, giving the reader tools to understand later different aspects of the present work.

- Chapter 3 explains the different steps taken during the design of the Charge Pump. It starts by giving the performance goals. Then it explains the operation of a Charge Pump and reflects on the topology choice. The requirement for the conception of the Bi-level converters, a crucial auxiliary circuit in the elaboration of the final circuit, is explained in this chapter. The way parameters are chosen and optimized as well as how the regulation of the output is achieved can also found here.

- Chapter 4 shows the final proposal and simulation results. Performance parameters will be simulated, such as, average output voltage, voltage ripple and efficiency. Many situations will be tested, including temperature extremes, process and mismatch deviations and variations of the input voltage.

- Chapter 5, the final chapter, presents some conclusions about this work and how this work can be improved further.

Chapter 2

Background and Bibliographical Review

This chapter has two objectives: to present how Charge Pump based DC-DC converters were forged throughout time, explaining and commenting the advantages and problems of each version. The second objective is to give the reader tools to better understand the decisions taken in the design and also some working principles involved with it.

As a certain topology is discussed, bibliographical references will be presented, working principles will be explained and some aspects will be commented in what concerns their applicability.

2.1 DC-DC converters

Electronic energy conversion consists in transforming electrical energy from one form to another, and the problem of how to make it efficiently and effectively as been posed to Engineers since electricity became a utility. The conversion may be concerned with voltage level adjustment, but may have to do with frequency conversion and also AC to DC or DC to AC are frequent needs. DC-DC converters are a subset of these in which only the voltage level is transformed. Throughout time this has been done in different ways. Before semiconductors, DC-DC conversion was achieved by first converting a DC supply to an AC voltage, changing the voltage level of the AC voltage with a transformer and only then to DC again. This, was possible because of the Vibrator [12], an electrical-mechanical device that allowed DC-AC and AC-DC conversion. The use of this primitive, but creative, DC-DC converter was mainly targeted for automobile radios and rural applications, where AC distribution was not present. Automobile radios needed high voltages to bias vacuum tubes used in radios and batteries were not able to offer such a high voltage. After the appearance of power semiconductors, this fell in disuse. DC-DC conversion is based on the principle of using energy storing elements, like inductors and capacitors, together with semiconductors, to produce a voltage level higher than the supply.

Figure 2.1 presents a basic DC-DC conversion topology using an inductor.

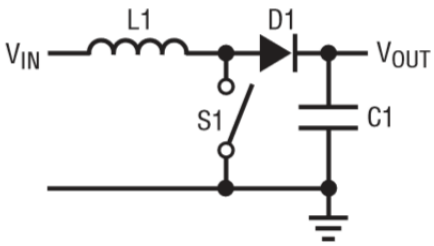

Figure 2.1: DC-DC converter using an inductor.

This is a typical DC-DC converter, an inductor is exposed to a source and energy is stored in its magnetic field. Later, when the switch opens, this energy is used to charge the capacitor through a diode. The rate of conversion (voltage level) can be controlled by the duty cycle of the switch. Although, not exactly like this, many circuits have been proposed that are inductor based [6, 7, 13, 14, 15], even though interesting, from a technological point of view, this type of converter will not be discussed beyond this, since it is inductor-based and out of the scope of this work.

2.2 Cockcroft-Walton Charge Pump

The first time a voltage multiplier was proposed that only used capacitors and semiconductors, seemed to be by Cockcroft and Walton in a work published in 1932 [1]. An interesting side-note is that Cockcroft and Walton were not trying to create a new capacitor based voltage multiplier, they were building a particle accelerator and a 800kV steady supply was needed. Its design can be seen in figure 2.2.

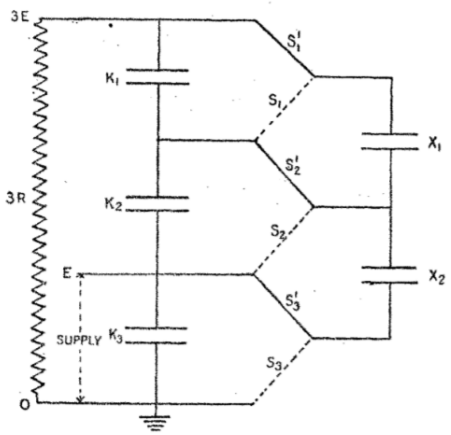

Figure 2.2: Cockcroft-Walton Charge pump, taken from [1].

The reason for building such a circuit, instead of other alternatives, like using a transformer to change the electrical distribution grid voltage into a higher voltage and then rectifying, is that they were trying to build this at reasonable cost and with ordinary laboratory equipment, as they said.

It consists of three capacitors in series and two other capacitors that are connected in a way that varies with the state of switches S_1, S_2 and S_3. There are two phases, Phase 1 corresponds to the full lines S_1', S_2', and S_3' being connected and phase 2 corresponds to the dotted lines S_1, S_2 and S_3 being connected. In the first phase the input supply charges K_3 to potential E. Then, in the second phase, X_2 is also charged by the supply. In the second phase 1, X_2 shares its charge with K_2, and both will be charged to E/2 if their capacitance is equal. Following that, in the second phase 2, K_2 will give half of its charge to X_1 and both will have E/4. At the same time X_2 is being charged to E, again. So, charge will gradually move through the capacitors until K_1, K_2 and K_3 will have voltage E. At that point the output will be 3E. It also becomes obvious that adding more capacitors and switches will increase the multiplying factor and also that this principle is reversible meaning that if a supply of 3E is connect to what we currently consider the output, K_1 will eventually have voltage E at its terminals. The way this is done no single capacitor withstands more that the voltage E at its terminals, and this is important because the voltage that capacitors are able to withstand is limited. It guaranties that no special higher voltage capacitor is needed. This was an important factor for them.

A doubling version of this, which is closer to what this works aims, can be seen in figure 2.3.

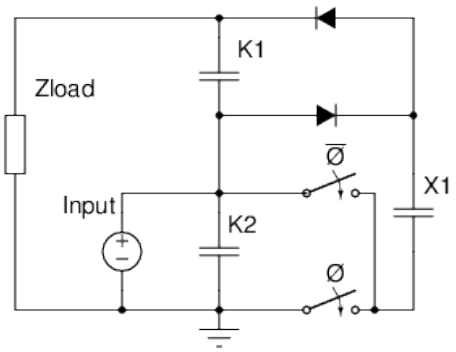

Figure 2.3: Double Cockcroft-Walton Charge Pump.

Capacitor K_2 is in parallel with the source, as such it can be suppressed for boosting purposes, it serves only to highlight that if instead of where the load is connected a source was connected, capacitor K_2 would finish with half the source's voltage (assuming both capacitors have the same capacitance). As Cockcroft and Walton, mentioned only two switches are necessary, besides S_3 and S_3' in figure 2.2 the other switches can be replaced by diodes. The working principle can be extended to whatever integer multiplication value is needed. When supplying a load a ripple exists, the charge of K_1 drops $\delta \times V/R$, being R the resistance of the load and δ the duration of charge supplied by K_1. In the next phase, X_1 must be able to recharge K_1 and supply the load during that period; so, if both phases have the same duration X_1 drains $\delta \times VE/R$ from the load. Of course, this only works if the diodes allow the transfer of such charge in the existing time frame.

Although this a design is old, many of its principles can be extended to all charge pumps. In figure 2.4 it is possible to see how the circuit looks during phase 1, i.e. $\Phi = 0$, the top diode does not conduct. If one defines Q as the charge that the load absorbs during half period, X_1 gains 2Q,

K_1 loses Q and K_2 loses 3Q. Whatever charges are lost by the capacitors must be replenish during the next phase.

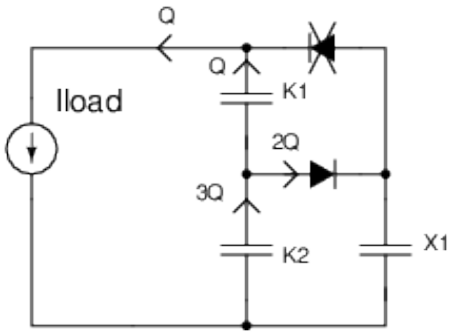

Figure 2.4: Phase 1 of the operation of the Cockcroft-Walton converter.

During phase 2 the circuit has the topology shown in figure 2.5. The load continues to absorb Q, X_1 loses the 2Q that gained during the previous phase, K_1 is recharged by Q, and K_2 further discharges Q. This is the steady state operation of this circuit and naturally a ripple exists because K_1's voltage is increasing in phase 2 and decreases during phase 1. K_2 is put in parallel with a source, so it is being constantly replenished. The reason K_2 is a capacitor and not just the source is suppose to be for two reasons: to highlight the fact the conversion works in both directions (if diodes are replaced by switches), and that at a certain point the source can be turned off without the converter stopping its operation. Of course the voltage will decreases through time but that may acceptable depending on the context.

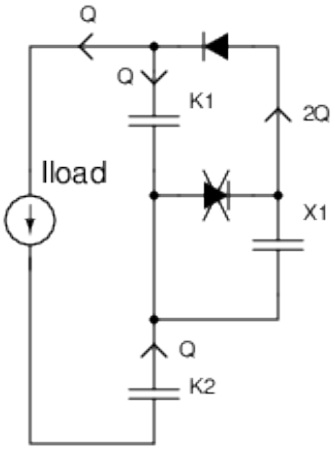

Figure 2.5: Phase 2 of the operation of the Cockcroft-Walton converter.

In short, this topology opened a precedent for circuits that followed, at least some are loosely based on it. In comparison with other topologies more used in recent time, it has the advantage of limiting the voltage for each individual capacitor to the source's voltage. However, this topology becomes inefficient if implemented in a monolithic integrated form [3], this is because of the on-chip parasitic capacitance and also the output impedance increases rapidly with the number of multiplying stages.

2.3 Dickson Charge Pump

Another big step in Charge Pump history was made by John F. Dickson [2], he proposed an improved voltage multiplying configuration, for purposes of being integrated, known today as the Dickson Charge Pump and is shown in figure 2.6. The main difference between Dickson's Charge Pump and the Cockcroft-Walton are:

1. In Dickson's Charge Pump individual capacitors have to withstand the full voltage developed along the chain. If maximum voltages for the process are respected this is not a problem.

2. The capacitors are coupled to the input via capacitors in parallel instead of in series. When in series, as Cockcroft-Walton, the effect of stray capacities is more dramatic.

Respectively, in figures 2.7 and 2.6 are represented the Cockcroft-Walton topology and Dickson's topology, each with their stray capacitances C_s.

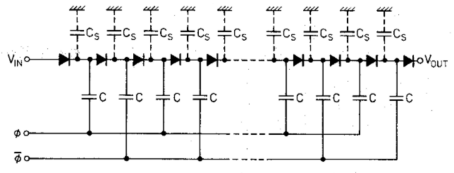

Figure 2.6: Dickson Charge Pump with stray capacities, taken from [2].

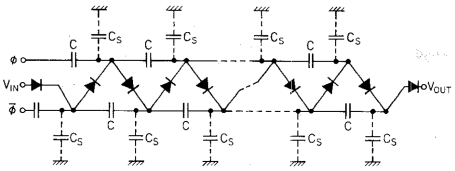

Figure 2.7: Cockcroft-Walton Charge Pump with stray capacities, taken from [2].

Dickson argued that analysis of the Cockcroft-Walton circuit with stray capacitances is very complex but in practice, because of the stray capacitances, it is hard to obtain more than a doubler.

The configuration uses diodes, capacitors and two complementary squares waves to achieve its goals. The complementary signals are represented as Φ and $\bar{\Phi}$ in the figure. At the beginning of the operation when Φ is low, the first capacitor C is charged to $V_{in} - V_d$, where V_d is the diode voltage drop. When Φ becomes high the second capacitor is exposed to the voltage $V_{in} - V_d + V_\Phi$ and it charges. Charge is pumped along the diode chain from the input to the output. Eventually the output reaches:

$$V_{out} = V_{in} + N(V_\Phi - V_d) - V_d \tag{2.1}$$

As pointed out in [4] if the stray capacitance C_s is considered, it reduce V_Φ by a factor of $C/(C+C_s)$ and also the presence of a load that draws I_{out} reduces the output voltage by $N \cdot Iout/((C+C_s) \cdot f_{osc})$, where f_{osc} is the operating frequency of the circuit, the output becomes:

$$V_{out} = V_{in} + N \cdot \left(\frac{C}{C+C_s} V_\Phi - V_d - \frac{I_{out}}{(C+C_s) f_{osc}} \right) - V_d \tag{2.2}$$

As Dickson pointed out: $V_{out} = V_o - I_{out}.R_s$ where $R_s = C/((C+C_s).f_{osc})$ and $V_o = V_{in} - V_d + N \cdot C/(C+C_s) \cdot V_\Phi - V_d$

There is also a ripple associated with the operation of this circuit. When the last diode is not conducting, the the output capacitor is supplying the load and therefore it is discharging. In the next phase this capacitor is recharged. So the peak-to-peak ripple is:

$$V_{ripple} = \frac{I_{out}}{f \cdot C_{out}} \tag{2.3}$$

The equivalent circuit is represented in figure

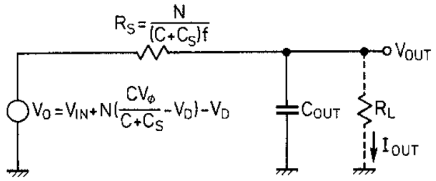

Figure 2.8: Cockcroft-Walton Charge Pump with stray capacities, taken from [2].

The clock that Dickson used to apply to the capacitor was an oscillator with NMOS clock drivers, which does not allow for significant current delivery.

Dickson charge pump can be implemented in practice using diode-connected NMOS transistors, where the voltage drop V_d is the MOS threshold voltage V_{th}. This same voltage drop V_{th} makes it difficult for the Dickson topology perform charge operation at low voltages. Addressing this problem Wu [3] proposed a new version of the Dickson charge pump using static charge transfer switches (CTS), as discussed next.

2.4 CTS based Charge pumps

With Wu, Charge Pumps took yet another step forward, mainly concerned with low voltage operation, Wu proposed a way to eliminate voltage drops through diodes, that are present in Dickson's Charge Pump. Later in the text there will be a subsection devoted into looking at the topology proposed by Wu applied to this work, which holds testament to how significant this is for the study of Charge Pumps. The main idea behind the technique is to use MOS switches with precise on/off characteristics avoiding the forward voltage drop at each node. This can be observed in figure 2.9.

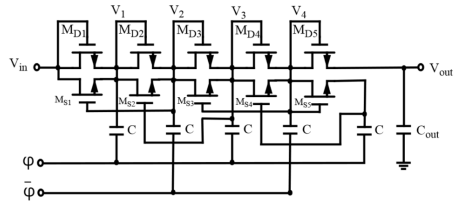

Figure 2.9: Static CTS based Charge Pump, taken from [3].

With the Dickson pump, the difference between the high level of two subsequent stages is:

$$G_v = V_\Phi \cdot \frac{C}{C+C_s} - Io \cdot \frac{C}{f \cdot (C+C_s)} - Vth. \tag{2.4}$$

This is called the pumping gain, and it reduces as V_{th} increases, as it does because of the body effect throughout the chain as V_{sb} voltage increases. So, this imposes a practical limit to the multiplication that can be achieved, due to the decreasing of the pumping gain.

Instead of the unavoidable voltage drop of the diode-connected MOS transistor, now the newly added transistors M_s 1-5 have gate signals previously charged to make possible a fully charge of the output capacitor of a particular stage to the max voltage of the previous stage. Now the lowest voltage of stage n is the highest voltage of the $n-1$ and the voltage drop V_{th} disappears. The pumping gain defined as the difference between successive pump stages is $G_v = V_2 - V_1 = \Delta V$ in which:

$$\Delta V = \frac{C}{C+C_s} \cdot V_\Phi - \frac{I_{out}}{(C+C_s) \cdot f_{osc}}. \tag{2.5}$$

However, this configuration has a problem, as pointed out by Wu himself, let us consider Φ is low so nodes 2 and 3 are at $2 \cdot \Delta V$ above node 1. This makes V_{gs} of M_{s2} be $2 \cdot \Delta V$ which is above V_{th} (if it was not the charge pump would not work) so this transistor is not completely *off* and charge sharing in the reverse direction will occur. This was also addressed by Wu. By including pass transistors, NMOS and PMOS, it will be able to turn completely *off* the CTSs (charge transfer switches). This can be observed in figure 2.10.

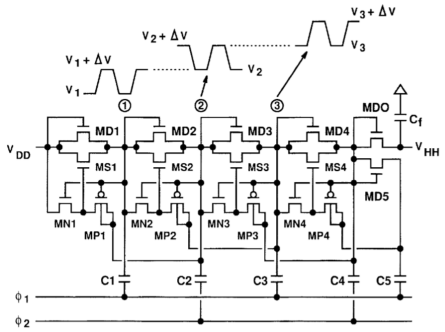

Figure 2.10: Dynamic CTS based Charge Pump, taken from [3].

For this configuration to work two conditions have to be satisfied

$$2\Delta V > V_{tp} \tag{2.6}$$

and

$$2\Delta V > V_{tn} \tag{2.7}$$

As of the realization of the clock itself, Wu was more concerned in boosting its voltage than increasing its ability to deliver current. The converter he achieved had an output voltage of 2V and 10uA. A lot less (two thousand times) than what this works aims.

The mechanism used by Wu to get this clock is shown in 2.11.

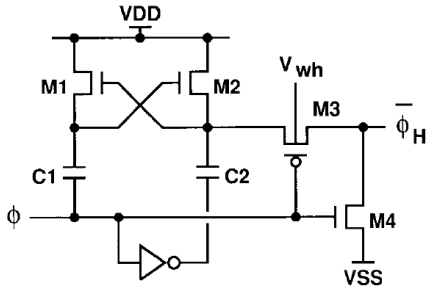

Figure 2.11: Dynamic CTS based Charge Pump, taken from [3].

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It allows the generation of a higher signal synchronous with the clock but its ability to deliver current is still limited to the R_{on} of transistors and the clock applied in these capacitors. This said, Wu's objective seemed to be to increase the practical limit of voltage multiplication and deliverable current was a secondary concern.

2.5 Modern Charge Pumps

Recent history of Charge Pumps include a huge variety of designs, most are still strongly Dickson and Wu influenced [7, 8, 11, 5, 9]. As presented in [4], a Charge Pump that is used, at least partially, in other modern DC-DC converters, which is simple and power efficent is that proposed in [16] and of which the basic pumping cell is shown in figure 2.12.

When Φ is low C_1 is charged, and when Φ is high C_2 is charged. Eventually C_1 and C_2 will be charged to V_{in}, because Vgs of the transistors respectively charging each capacitor will be at V_{in} + V_Φ, so nodes 1 and 2 (the top plate of each capacitor) will be alternately connected to C_{out}, in a way that C_{out} will only be connected to the node that is currently at V_{in} + V_Φ. This is possible because of the S_{w1} and S_{w2} switches, which will also be controlled by Φ and its complement.

A design particullarly interesting for this is work is presented in [5]. It consists in a series-parallel trippler. Two capacitors are charged in parallel with the voltage power source and then, in the subsequent phase, are in parallel with each other and the source to produce a higher voltage. Its topology is presented in figure 2.13.

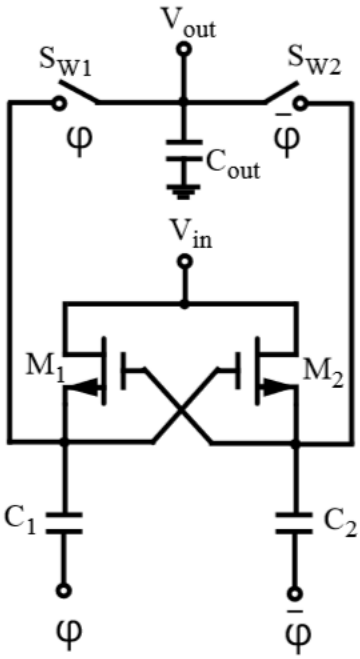

Figure 2.12: Modern Charge Pump, taken from [4].

The basic topology is simple, the challenge resides on the way switches are designed. Pérez-Nicoli proposes a special kind of switch seen in figure 2.14.

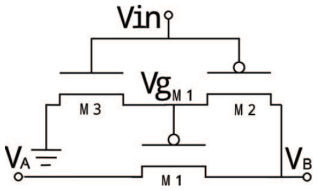

Figure 2.14: Switch proposed, taken from [5].

The transistor that actually transfers charge in the power part of the Charge Pump is M1. This is a PMOS, which is not as good as an NMOS would be, due to reduced mobility of holes when compared to that of electrons. This is a bi-phase converter. So during the phase when $V_{in} = 0$V, transistor M2 charges the gate of M1 to V_B, during this phase V_B is high so V_{gs} is 0V and the transistor is in cutoff. In the next phase $V_{in} = V_{DD}$, M3 discharges M1's gate and so M1 will be conducting and charging the capacitor. A very important point is that the charge used to charge and discharge the gate's capacitor is lost, as it will be referred later. This work will distinguish itself by using a mechanism in which charge is not lost. In Pérez-Nicoli's design the switch that connects to ground is just an NMOS transistor, since turning it on just requires a gate voltage higher than V_{th}.

Design of Charge Pumps is a diverse area of study, because some specific objectives such as energy harvesting focus more on having a high conversion ratio, many converter are micro-power

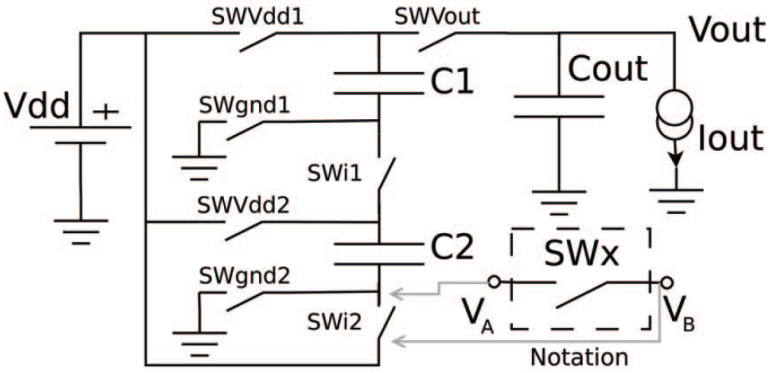

Figure 2.13: Series-Parallel Trippler, taken from [5].

and even nano-power and are not able of delivering significant currents. This work will focus more on output current than existing designs, so a series-parallel converter will be more appropriate. In this way the pulsating clock voltages that are applied in the base of capacitors are obtained from the source through bootstrapped switches, that are more capable to transfer current.

2.5.1 Summary

Under the light of the envisioned application, a Charge Pump circuit can vary a lot. Some are focused in higher conversion ratios and not on output current, some the opposite. Despite this, all topologies can be traced back the Cockcroft-Walton and Dickson Charge Pump. This is why they were presented here.

Cockcroft-Walton proposed a way of achieve a voltage level converter using only capacitors, also limiting the voltage in each individual capacitor. This opened the door for more work in capacitor based converters. Dickson concerns in achieving an on chip solution, originated into his own topology proposal that minimized the impact of stray capacitances. Wu improved upon this devising a dynamic way of turning *on* and *off* the switchs that are intended to transfer charge.

Many more Charge Pump were proposed with some nuances between them, however some of them have limitations on the clock's ability to deliver a charge to the load. This is a concern that will need to be addressed in this work.

Chapter 3

Charge Pump Design

This chapter is the core of this work, and accordingly it is mainly focused on the choice of the appropriate topology. An interesting approach commonly used to solve the problem is also analyzed here, together with a critical assessment on its benefits and limitations. It describes, step-by-step, the details of different parts of the system: main topology, switches, auxiliary circuits, regulation of outputs, etc. Also, details about circuit operation are presented, providing the necessary tools to understand the motivation behind the decisions made.

3.1 Performance Goals

This work aims at designing a charge pump following a concrete set of goals, but keeping in mind important optimization parameters, such as area and energy efficiency. The set of specs to be met by the converter are presented in table 3.1. Other aspects such as, switch frequency, capacitor sizes and type of switches will be decided under the constrains of the goals.

Table 3.1: Performance goals

Input Voltage	0.8V
Input Tolerance	$\pm 10\%$
Output Voltage	1.2V
Output Ripple	$\leq 10\%$

3.2 Operation with variation of PVT

A very important aspect that need to be considered during the design of a chip, and that distinguishes this work from most descriptions of Charge Pumps in literature, is a design oriented towards achieving performance goals are to be fulfilled even under PVT variations. PVT concerns the variation in process, voltage supply and operating temperature, which all influence chip operation. Wafers are fabricated in lots, and variation exists in electrical properties of the semiconductors between lots and also slight variations within a lot. These process variations result

from deviations in the fabrication process, culminating in deviations of impurity concentration densities, diffusion depths and oxide thickness. This happens because environmental conditions may vary during crucial manufacturing steps, such as during depositions and diffusions of the impurities. All of this results in different transistor parameters, namely, different threshold voltages and different geometrical sizes of devices, mainly caused by the limited resolution of the photo-lithographic process. It leads to (W/L) variations in MOS transistors.

The effects these deviations have on device performance, either from environmental or process variations, are normally combined and translated in transistor models that reflect these variations in a slower or faster response. These are commonly referred as process corners and helps the designer to infer if its circuit is, or not, tolerant to fabrication variations along time. In principle, the actual devices are confined within the margins of the corners during production, and most of the times falling around the nominal values. Since CMOS technologies hold two types of transistors, NMOS and PMOS, five combinations define the limits, centred around the nominal: SS SF, TT, FS, FF, where S stands for "Slow", F for "Fast" and T for "Typical", which designates the nominal. The first letter always corresponds to NMOS and the second to PMOS. Actually, process corners is extended to other elements, such as resistors and capacitors, and all combinations normally need to be tested.

Supply voltage variation is taken into account in the performance goals by defining that the input voltage may vary within some margins, usually the slower corresponds to the minimum value and the fast the maximum, besides the typical. In the this work it is limited to -10% and +10% of the nominal voltage of 0.8V.

Chips often are exposed to very different temperatures. Beyond environmental conditions, temperature can be increased in a chip because of power dissipation during switching, short circuits occurring during transitions, caused by brief direct current from supply to ground, and also leakage currents. Electron and hole mobility in Silicon typically diminishes with temperature although the point at which the decrease begins depends on the doping. Also, the threshold voltage depends on temperature.

3.3 Charge Pump Topology

When choosing a topology it has to be taken into account the work already developed in charge pump topologies, mentioned in previous chapters. Most topologies are based on the conventional Dickson Charge Pump or the Series-Parallel converter. The Series-Parallel converter consists in charging a capacitor through a voltage power source and switches. Then that charged capacitor is put in series with the source, thereby producing a higher level voltage, as mentioned before. The Dickson Charge Pump consists in charging capacitors through a diode or switch. A clock voltage is applied to the bottom plate of the capacitors that when set to a high state raises the top plate voltage in relation to the reference. This higher level of voltage is now used to charge another capacitor, or to drive a load. A very important point to ask is where does the high level of the clock comes from?It may just come from a regular clock signal or from the input source

adequately switched. Note that the variation of charge at the top plate of the capacitor corresponds an equal amount of charge change (opposite sign) at the bottom plate. It is the clock that supplies that charge, meaning that the clock has to supply the same current that is delivered to the load or that charges a subsequent stage. The aforementioned current is as large as the load that is being supplied, thus, a simple logic clock cannot supply that kind of power. Somehow that power has to come from the input source, this important realization will be further explained in subsection 3.3.1.

Some topologies do not address the fact that there is a voltage drop across diodes or the switches. This has two obvious disadvantages:

1. Maximum achievable voltage is limited.

2. Resistance between stages. This limits the ability to share charge from successive stages. This limitation comes from the diode, and therefore it cannot be controlled beyond sizing it appropriately.

Where this is better addressed is in Wu's Dynamic Charge Transfer Switches citeWu1998. Many Charge Pumps appear to use this technique. The existence of the pass transistors allows the dynamical turning on and off of switches. Although interesting, this topology has its problems, which are explained in the subsection 3.3.2. Before explaining the limitations of the Dynamic CTS Charge Pump it is fundamental to understand the basic operation of the Charge Pump, explained in the next subsection.

3.3.1 Basic operation of a Charge Pump

A crucial point made before is that, unless supplying very small currents, the clock signal used in many Dickson based Charge Pumps is a kind of a "Power Clock" in a way that the waveform is the same as the logical clock, but its ability to supply current has to be far greater. Because the only place that a large current can be drawn, in the circuit, is from the input power source, this "Power Clock" has to be the input source appropriately switched. This can be done with inverters, in a simple manner like that shown in 3.1.

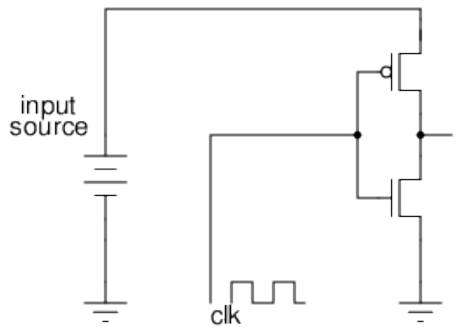

Figure 3.1: Commutating the source with an inverter.

If large currents are to pass through this inverter, then low R_{on} resistance will be required. It may be done by increasing the W/L of the transistors but this will increase the gate capacitance that the clock has to charge and so significant current may be required from the clock itself in order to charge them. Of course this effect can be minimized by using a chain of inverters and with the clock charging only a minimal inverter. Still, as it will be explained further in this subsection, large average currents will have to be drawn from this device, this will require transistors with massive W/L to reduce their R_{on}. In addition to this, the number of inverters, their size, and frequency of operation will have a direct impact of the circuit consumption and it is desired to keep it as low as possible. This said, an alternative to use this inverter chain would be to use switches, just like the ones that may be use to charge the capacitor in the first place. A simple representation of this would can be seen in figure 3.2.

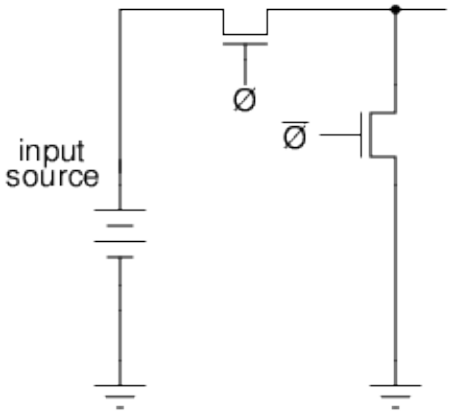

Figure 3.2: Opposite phase signal to switch the source.

Of course, the signal controlling the switches cannot be the logical clock directly, a mechanism would be required to turn *off* and *on* the switches in an appropriate fashion. Wu addresses this by using pre-charged capacitors in addition to pass transistors to turn *off* and *on* the NMOS switches. Independently of the way switches are implemented, some conjectures can be made. Ignoring, momentarily how the switches are actually realized, a simplified representation of this circuit can be seen in figure 3.3.

The circuit operates in two phases. The Discharge phase consists in having C_{out} discharging to the load while C_1 is charging trough a switch. An illustration of this can be seen if figure 3.4. The switch, that is in an *on* state is represented by its *on* resistance R_{on}. The charging of C_1 follows the equation of a simple RC circuit, as expressed in equation 3.1.

$$V_{DD} \cdot u(t) = R_{on} \cdot i(t) + V_{C1}(t) \tag{3.1}$$

For our purposes, C_1, has an initial condition therefore it is important to include this fact in equation 3.1. Also, the voltage at C_1 terminals is a result of accumulation of charge coming from

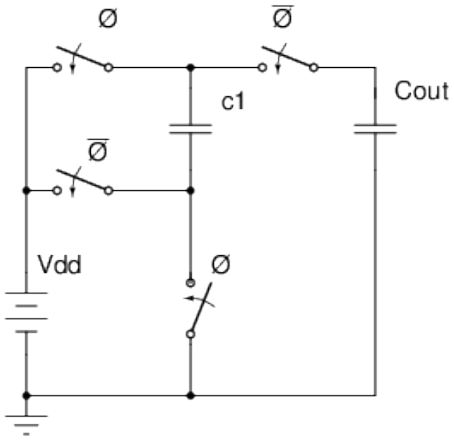

Figure 3.3: Switch based Charge Pump Topology.

the current flowing through it, so:

$$V_{DD} \cdot u(t) = R_{on} \cdot i(t) + V_{C1}(0) + \frac{1}{C1} \int i(t)) \tag{3.2}$$

Applying the Laplace transform to equation 3.2.

$$\frac{V_{DD}}{s} = R_{on} \cdot i(s) + \frac{V_{C_1}(0)}{s} + \frac{i(s)}{C_1 \cdot s} \tag{3.3}$$

and then:

$$\frac{V_{DD} - V_{C_1(0)}}{s} = i(s)(R_{on} + \frac{1}{C_1 s}) \tag{3.4}$$

$$i(s) = \frac{C_1(V_{DD} - V_{C_1}(0))}{RC_1 s + 1} \tag{3.5}$$

$$i(s) = \frac{\frac{V_{DD} - V_{C_1}(0)}{R_{on}}}{s + \frac{1}{RC_1}} \tag{3.6}$$

$$i(t) = \frac{V_{DD} - V_{C_1(0)}}{R_{on}} e^{\frac{-t}{R_{on} \cdot C_1}} \tag{3.7}$$

In equation 3.7 it is given the expression for the current in this part of the circuit and it can be seen that it starts from $\frac{V_{DD} - V_{c1}(0)}{R_{on}}$ and approaches 0 as the capacitor reaches closer to the fully charged state.

As for the voltage:

$$V_{C_1}(t) = \frac{1}{C_1} \int i(t) \tag{3.8}$$

$$V_{C_1}(t) = (V_{DD} - V_{C_1}) \cdot e^{\frac{-t}{R_{on} C_1}} + C \cdot u(t) \tag{3.9}$$

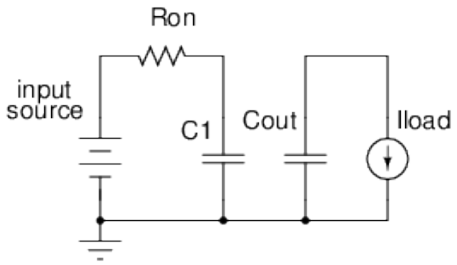

Figure 3.4: Equivalent Circuit during discharge phase.

The constant that appears in result of the integration is resolved by satisfying the initial condition, and therefore we get:

$$V_{C_1}(t) = V_{DD} \cdot u(t) - (V_{DD} - V_{C_1}) \cdot e^{\frac{-t}{R_{on}C_1}} \tag{3.10}$$

From equation 3.7 we know that at $t = 0$ the voltage at the capacitor's terminals is $V_{C_1}(0)$ and given enough time is V_{DD}.

During this phase the output capacitor is discharging.

$$V_{C_o}(t) = V_{C_o}(0) - I_o \cdot t \cdot u(t) \tag{3.11}$$

The current that C_{out} is supplying might not, and most probably is not, a direct current, however as long as the average current for this period does not exceed 20mA, the accepted ripple interval will be fulfilled, if the circuit is correctly designed.

At the beginning of this phase V_{out} should be at its maximum value of: $1.2 + V_{ripple}/2$ and by the end it should not have gone below $1.2 - V_{ripple}/2$. This means that $I_o \cdot T_{dis} \leq C_{out} \cdot V_{ripple}$, being T_{dis} the duration of the discharge phase.

During the charge phase the circuit is a bit more complex, seen in figure 3.5. Now, the previous charged capacitor C_1 is in series with the source and has to charge C_{out} as well as supplying the load during this period.

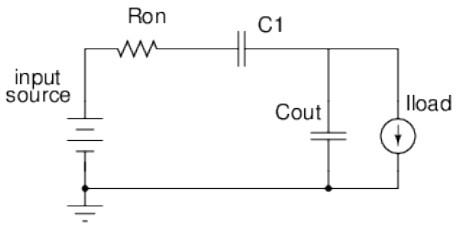

Figure 3.5: Equivalent Circuit during charge phase.

The equation for this period is the following, being C_{out} equal to C_o:

$$V_{DD} \cdot u(t) + V_{C_1}(0) \cdot u(t) - \frac{1}{C_1}\int i(t) = V_{C_o}(0) \cdot u(t) + \frac{1}{C_o}\int i(t) - Io \cdot u(t) \tag{3.12}$$

Applying the Laplace transform.

$$\frac{V_{DD}+V_{C_1}(0)-V_{C_o}(0)}{s}+\frac{Io}{C_o\cdot s^2}=i(s)\cdot\left(\frac{1}{s\cdot C_o}+\frac{1}{s\cdot C_1}+R_{on}\right) \tag{3.13}$$

$$\frac{\frac{s(V_{DD}+V_{C_1}(0)-V_{C_0}(0))}{R_{on}}+\frac{I_o}{R_{on}C_o}}{s\cdot\left(s+\frac{1}{R_{on}C_o}\right)} \tag{3.14}$$

$$i(s)=\frac{\frac{s(V_{DD}+V_{C_1}(0)-V_{C_0}(0))}{R_{on}}+\frac{I_o}{R_{on}C_o}}{s\cdot\left(s+\frac{1}{R_{on}C_o}\right)} \tag{3.15}$$

$$i(s)=\frac{\frac{s(V_{DD}+V_{C_1}(0)-V_{C_0}(0))}{R_{on}}+\frac{I_o}{R_{on}C_o}}{s\cdot\left(s+\frac{1}{R_{on}C_o}\right)}=\frac{A}{s}+\frac{B}{s+\frac{1}{R_{on}C_{eq}}} \tag{3.16}$$

In which:

$$C_{eq}=\frac{C_oC_1}{C_o+C_1} \tag{3.17}$$

and then:

$$A=\frac{I_oC_1}{C_o+C_1},B=\frac{(V_{DD}+V_{C_1}(0)-V_{C_o}(0))}{R}-\frac{I_oC_1}{C_o+C_1} \tag{3.18}$$

Returning to the time domain:

$$i(t)=\frac{I_oC_1}{C_o+C_1}u(t)+\left(\frac{(V_{DD}+V_{C_1}(0)-V_{C_o}(0))}{R_{on}}-\frac{I_oC_1}{C_o+C_1}\right)\cdot e^{\frac{-t}{R_{on}C_{eq}}} \tag{3.19}$$

As in the previous phase, the voltage at its terminals is just the primitive of the current divided by the capacitance.

$$V_{C_o}(t)=-\frac{1}{C_o}\int i(t) \tag{3.20}$$

Resolving the primitive:

$$\frac{-I_o}{C_o+C_1}tu(t)+[R_{on}I_o(\frac{C_1}{C_o+C_1})^2-(V_{DD}+V_{C_1}(0)-V_{C_o}(0))\frac{C_1}{C_1+C_o}]e^{\frac{-t}{R_{on}C_{eq}}}+C\cdot u(t) \tag{3.21}$$

Resolving the constant C:

$$Vo(t) = \frac{-I_o}{C_o + C_1} \cdot t \cdot u(t) + \left[R_{on} I_o \left(\frac{C_1}{C_o + C_1} \right)^2 - (V_{DD} + V_{C_1}(0) - V_{C_o}(0)) \frac{C_1}{C_1 + C_o} \right] e^{\frac{-t}{R_{on} C_{eq}}} + \left[(V_{DD} + V_{C_1}(0)) \frac{C_1}{C_1 + C_o} + V_{C_o} \frac{C_o}{C_o + C_1} - R_{on} I_o \left(\frac{C_1}{C_o + C_1} \right)^2 \right] u(t) \quad (3.22)$$

Because of the action from the current source that is drawing current, given enough time the capacitors will eventually discharge completely, but for correct dimensions, the voltage first increases before starting to fall, defining a point of maximum voltage.

For the values expressed on table 3.2, chosen arbitrarily just to indicate how the voltage would vary in time during the discharge phase, results in waveform presented on figure 3.6

Table 3.2: Design parameters.

Parameter	Value
V_{dd}	0.8V
Io	20mA
R_{on}	1Ω
$V_{c1}(0)$	0.7V
$V_{co}(0)$	1.185V
C_1	100nF
C_o	100nF

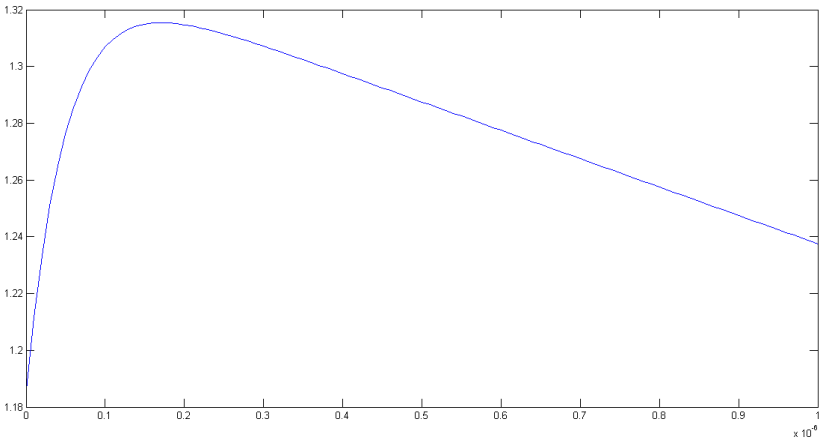

Figure 3.6: Voltage waveform during discharge phase.

Ideally, for the worst possible corner, the discharge phase would be set to end by the clock control, when the maximum voltage is reached. As such, it is desirable to locate the maximum value of the voltage as function of time. That can be resolved by finding the point the derivative

passes through 0.

$$\frac{d}{dt}V_o(t) = 0 \tag{3.23}$$

$$\frac{d}{dt}V_o(t) = -\frac{I_o}{C_o + C_1}u(t) + \left[-\left(\frac{C_o + C_1}{RC_oC_1}\right)\left(\frac{I_o \cdot R_{on} \cdot C_1^2}{(C_o + C_1)^2} - (V_{DD} + V_{C_1}(0) - V_{C_o}(0))\right)\frac{C_1}{C_1C_o}\right] e^{\frac{-t}{R_{on}C_{eq}}} \tag{3.24}$$

with further manipulation:

$$t_{opt} = -\ln\left(\frac{C_o}{\frac{(V_{DD} + V_{C_1}(0) - V_{C_o}(0))(C_o + C_1)}{RI_o} - C_1}\right)\frac{RC_oC_1}{C_o + C_1} \tag{3.25}$$

Substituting C_{out} by C and C_1 by $\alpha \cdot C$, in which α is the relation between the capacitors, results in:

$$t_{opt} = -\ln\left(\frac{1}{\frac{(V_{DD} + V_{C1}(0) - V_{Co}(0))(1 + \alpha)}{R_{on}I_o} - \alpha}\right)\frac{\alpha}{1 + \alpha}R_{on}C \tag{3.26}$$

It is vital to know if t_{opt} is not positive which would mean that the voltage does not rise and therefore the output capacitor instead of charging is further discharged. For t_{opt} to be positive:

$$\frac{C_o}{\frac{(V_{DD} + V_{C_1}(0) - V_{C_o}(0))(C_o + C_1)}{R_{on}I_o} - C_1} < 1 \tag{3.27}$$

so the condition that needs to be satisfied is:

$$R_{on} < \frac{V_{DD} + V_{C1}(0) - V_{Co}(0)}{Io} \tag{3.28}$$

To have a better notion of the values involved, in the worst corner case V_{DD} is 0.72V. $V_{C1}(0)$, which is the voltage at capacitor C_1 at the beginning of this phase (this voltage is generated by charging this capacitor in the previous phase), in the best possible case is very close to 0.72V. For the purpose of this argument lets assume it is 0.72V. Now considering that $V_{Co}(0)$ is 1.2V - $\frac{V_{ripple}}{2}$ which is 1.17V, this leads to:

$$R_{on} < 13.5\Omega \tag{3.29}$$

The condition in equation 3.29 is necessary for the capacitor C_o to charge. However that does not mean that the maximum value will actually be reached. There are other factors to take into consideration, like capacitance, frequency of operation, etc... Thus, another pertinent expression to be found is the value for the maximum voltage. This occurs at $t = t_{opt}$. So, substituting 3.26 in 3.22 results in:

$$Vmax = \frac{R \cdot I_o \cdot \alpha}{(1+\alpha)^2} \cdot \ln\left(\frac{1}{\frac{V_{DD}+V_{C1}(0)+V_{Co}(0)}{R_{on}\cdot I_o}(1+\alpha)-\alpha}\right) + \left[R_{on}\dot{I}_o\frac{\alpha}{1+\alpha} - \frac{V_{DD}+V_{C1}(0)+V_{Co}(0).\alpha}{1+\alpha}\right]\frac{1}{\frac{V_{DD}+V_{c1}(0)-V_{co}(0)}{R_{on}.I_o}(1+\alpha)-\alpha} + (V_{DD}+V_{c1}(0))\frac{\alpha}{1+\alpha} + V_{co}(0))\frac{1}{1+\alpha} - R_{on}.I_o\frac{\alpha}{(1+\alpha)^2} \quad (3.30)$$

A very important realization that comes from 3.30 is the fact that the maximum value of the voltage does not depend on the absolute size of capacitors but rather on the ratio between them.

It is important to notice that for C_1 to charge C_{out} and supply the load, assuming the load current for an entire period has an average value of I_o, the total charge transferred by C_1 has to be $I_o.T$. This is because C_1 is discharged by $I_o.T_{dis}$ in the previous phase, and during this phase the load further absorbs I_oT_{char}, being T_{char} the duration of this phase.

Looking now into how these switches are actually realized, the simplest way is to use a single transistor with appropriate gate levels. When choosing between an NMOS or PMOS transistor, the obvious choice is NMOS because the mobility of holes is less than that of electrons and low resistance will be vital in the process. The applied gate signal has to fulfil some requirements:

- During those phases that the switch should be *off*, applying a low enough gate voltage to have a $V_{gs} < V_{th}$.

- When the switch should be *on*, apply a high enough voltage to eliminate the voltage drop V_{th}, so $V_{gb} > V_{db} + V_{th}$. This condition allows to charge the capacitor to the voltage of the previous stage. If V_{gb} is lower than this, the transistor enters the cut-off region before the capacitor reaches its maximum achievable voltage.

- The higher V_{gb} gets, the higher V_{gs} gets. This leads to a low R_{on} which is very desirable, although V_{gs} should not surpass the max voltage that the transistor withstands to avoid damaging it or accelerate its ageing process.

A representation of this can be seen in figures 3.7 and 3.8. There we can observe the intervals that Vg voltage has to fulfil.

The way these gates are charged and how to respect these intervals will be addressed in section 3.4.

Turning *off* and *on* NMOS switches dynamically is better addressed in Wu's dynamic charge transfer switches charge pump citeWu1998. Although interesting, this topology has its own limitations. This will be tackled in the next section.

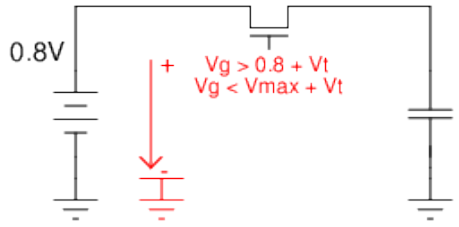

Figure 3.7: Turning on a NMOS switch.

3.3.2 Dynamic CTS Charge Pump: Advantages and limitations

The main advantage of the Dynamic CTS Charge Pump is that it uses pre-charged capacitors to turn *on*, turn *off*, and bootstrap gates. This means, that this circuit can be realized with a certain area-saving factor.

In figure 3.9, we present a two stage dynamic CTS charge pump circuit. Also, for each relevant voltage there are two values, one corresponding to each phase in some circuit elements.

A simple description of the operation of this circuit follows:

Phase $\phi = 1$

1. N_pass is turned *off* because of a V_{gs} of '0V'.
2. P_pass is turned *on* because of a V_{gs} of $2V_{DD} - Vth$, assuming that $2V_{DD} - V_{th} > V_{th}$.
3. Because of the two previous facts the V_{gb} of N_switch is charged to the voltage of the top plate of Cp, $3V_{DD} - Vth$.
4. $3V_{DD} - V_{th} > V_{DD} + V_{th}$, so the capacitor C_1 is charged to V_{DD}.
5. During this phase, C_{out} might be supplying charge to loads, and therefore is discharging.

Phase $\phi = 0$

1. The voltage at the top plate of C_1 rises to $2V_{dd}$.
2. C_1 charges C_p through diode d3.
3. N_pass is turned *on*.
4. P_pass is turned *off*.
5. The gate of N_switch discharges to V_{DD}.
6. The source and gate of N_switch are at the same voltage, so N_switch is turned *off*. This avoids transference of charge in the reverse direction.
7. The top plate of C_1 is now at $2V_{DD}$ so it charges C_{out} through diode d2.

The last voltage drop from C_1 to C_{out} is not avoided. A very important point is that the ability do deliver charge to a load is limited by the ability to transfer charge throughout pumping stages. This means that for C_{out} to deliver a certain amount of charge during a certain phase, in the next phase C_1 has to, not only recharge C_{out}, but also needs to have enough charge left to supply the load during this phase, this has all to be done without its voltage dropping beyond a certain point.

As seen in figure 3.9, the largest V_{gs} of the N_switch is $2V_{DD} - V_{th}$. This might be enough to charge the subsequent capacitor to V_{DD}, but equally important is if it reduces R_{on} enough.

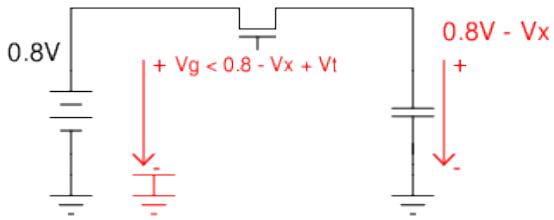

Figure 3.8: Turning off a NMOS switch.

Additionally, a trade-off is involved between having a V_{gs} big enough to reduce R_{on}, but small enough not to damage the transistor.

3.3.3 Choice of Topology

Since an important criteria is to deliver a significant amount of current, the topology proposed by this work is based on figure 3.3. Switches will be NMOS transistor with bi-level converters to charge the transistor's gate. Bi-level converters will be presented in the next section. In figure 3.10 a diagram is shown with the proposed solution.

The question that emerges is how to design these blocks that have to control the gate voltage of the NMOS. These will be Charge Pump based circuit, that will be further explored in the next section.

3.4 Bi-level Converter

From what has been seen before there is a necessity to obtain certain levels of voltage to turn *off* and *on* the NMOS switches in an appropriate way. The way this is done is a crucial part of this work. This chapter will be devoted to analyse the operation of these type of converters, some simulations are made mainly to highlight circuit limitations. Some details might not be mentioned if they are not relevant. Conclusions shown here will be helpful to understand how to design the necessary bi-level converters, however this chapter is not about obtaining the dimensions of a specific design, its about general conclusions and details about these converters and their specificities, which are not described in most DC-DC converter reports found in literature.

First, it is important to understand what is needed from a bi-level converter. The output of this circuit will oscillate between two values: V_{low} and V_{high}. V_{low} must turn *off* the NMOS, V_{high} must turn it on, but must be low enough not to damage the transistor.

In table 3.3 the required voltages for a certain bi-level converter are presented.

Table 3.3: Requirement of a bi-level converter.

V_{low}	$< V_{sb}$ +Vt
V_{high}	$> \tilde{V_{sb}}$ + Vt and $< V_{max}$

To turn the transistor *off*, it must set to be in cut-off region assured by having $V_{gs} < V_{th}$, turning *on* requires $V_{gs} > V_{th}$, but as the next capacitor charges the transistor, it enters in cut-off region so

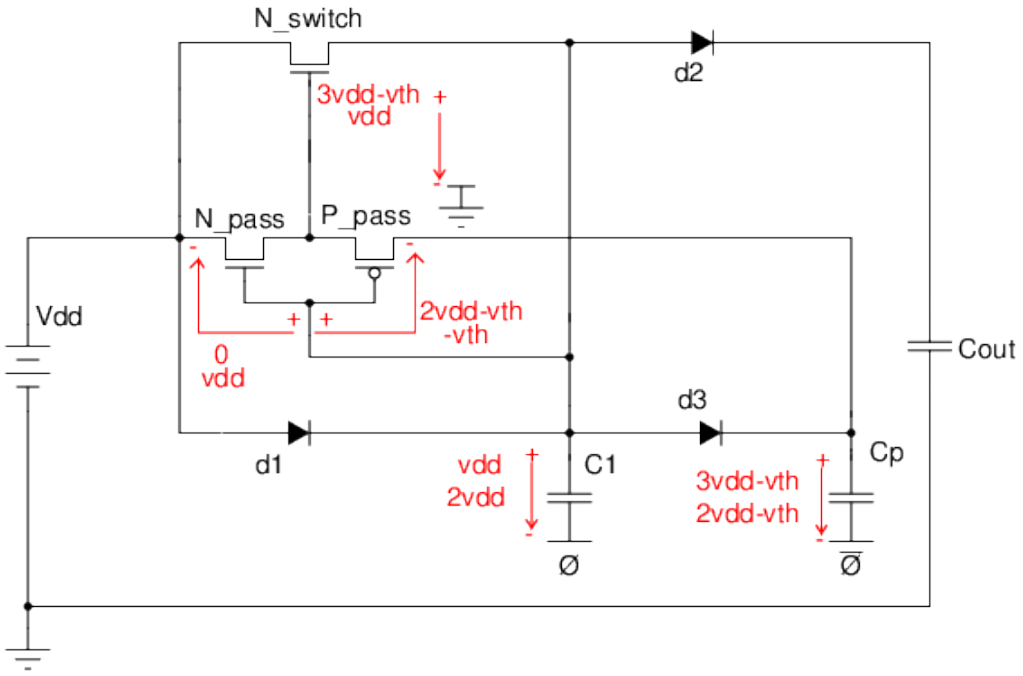

Figure 3.9: Two-stage Dynamic CTS Charge Pump.

the voltage must be V_{th} above whatever voltage we desire to transfer. The voltage that is wished to transfer is denominated $\tilde{V_{sb}}$. Also, V_{gs} must be limited to the maximum voltage that the transistor is able to withstand.

All of this has to be taken into account when designing a bi-level converter because the consequence of having one switch not being turned *off* or *on* adequately is dire to the circuit. The next section will go into details about the way a bi-level converter works, vital information to understand how to design this converter is also presented. Every bi-level will be sensible to PVT corners so some sort of controller will be needed to regulate it. This will be tackled later in this work.

3.4.1 General Operation

A mechanism was devised to accomplish the goal of generating two voltage levels using charge pump converters denominated as "bi-level converters". From a certain input, it generates two different values of voltage that are alternated. Turning *on* and *off* an NMOS switch is done by applying the appropriate gate signals, as seen. Figure 3.11 highlights the mechanism by which this is done in the Dynamic CTS converter.

Two parts of this circuit can be distinguished, one being the power part, that is the part in which charge circulates with the purpose of actually supplying the load, the other is the bootstrapping part that exists to control the gates of the NMOS switches. An important factor is that in Wu's Dynamic CTS these two parts overlap in capacitor C_1. This has two advantages:

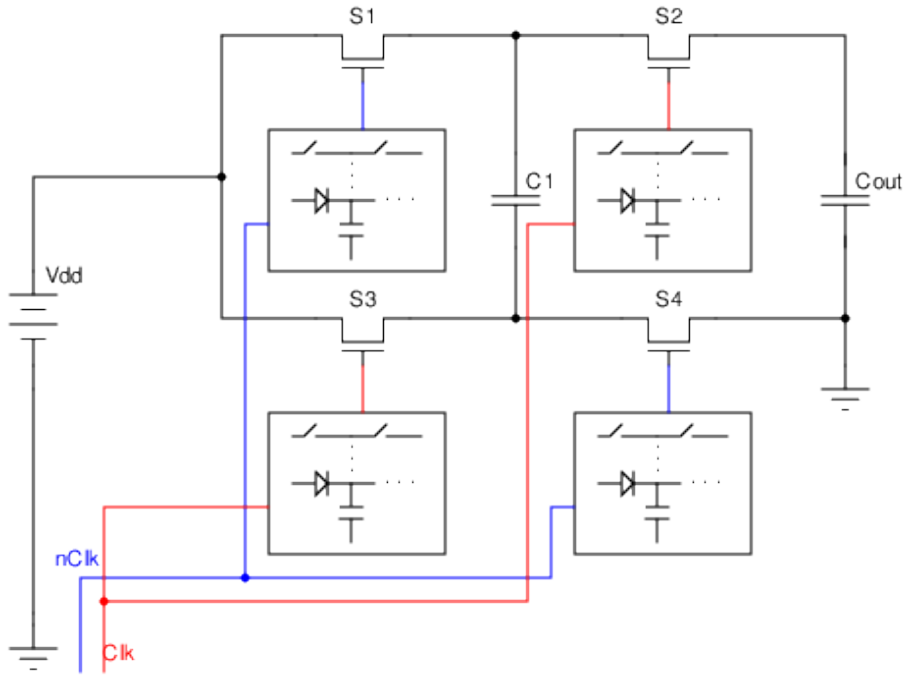

Figure 3.10: Proto-bi-level.

- A capacitor is saved from the bi-level charge pump part, although this capacitor would be significantly smaller as the ones from the power part.
- This capacitor alternates between V_{DD} and $2V_{DD}$ instead of $V_{DD} - V_t$ and $2V_{DD} - V_t$.

However the peak-to-peak voltage of the wave generated by the converter seen in figure 3.11, might not be enough for turning *off* the switch in one period and turning *on* in the other. A solution would be to add a previous stage as seen in figure 3.12.

The addition of pre-stages allows for higher voltages to be attained, the mechanism of achieving the alternate wave is the same but the inclusion of more stages increases the alternating levels. The voltage variation mechanism can be seen in table 3.4.

Table 3.4: Relevant Voltages in N-Stage Singular Bi-level Converter.

Phase	C_n	C_{n+1}	C_{n+2}	Vgs(N_pass)	Vgs(P_pass)	Drain
Φ	nV_{DD}-nVt	(n+2)V_{DD}-(n+1)Vt	(n+2)V_{DD} - (n+2)Vt	$2V_{DD} - Vt$	Vt	nV_{DD} - nVt
$\bar{\Phi}$	(n+1)V_{DD}-nVt	(n+1)V_{DD}-(n+1)Vt	(n+3)V_{DD} - (n+2)Vt	-Vt	$-2V_{DD} + Vt$	(n+3)V_{DD} - (n+2)Vt

One important note is the values under C_n are not the actual voltage between the capacitor's terminals as this voltage does not vary much in steady state, it is the voltage at the top plate of the respective capacitor.

The aspect of the waves in each stage can be seen in figure 3.13. This is a result of a simulation of a partial converter with no pass transistors, just the diodes and capacitors, to better understand what happens when they are added.

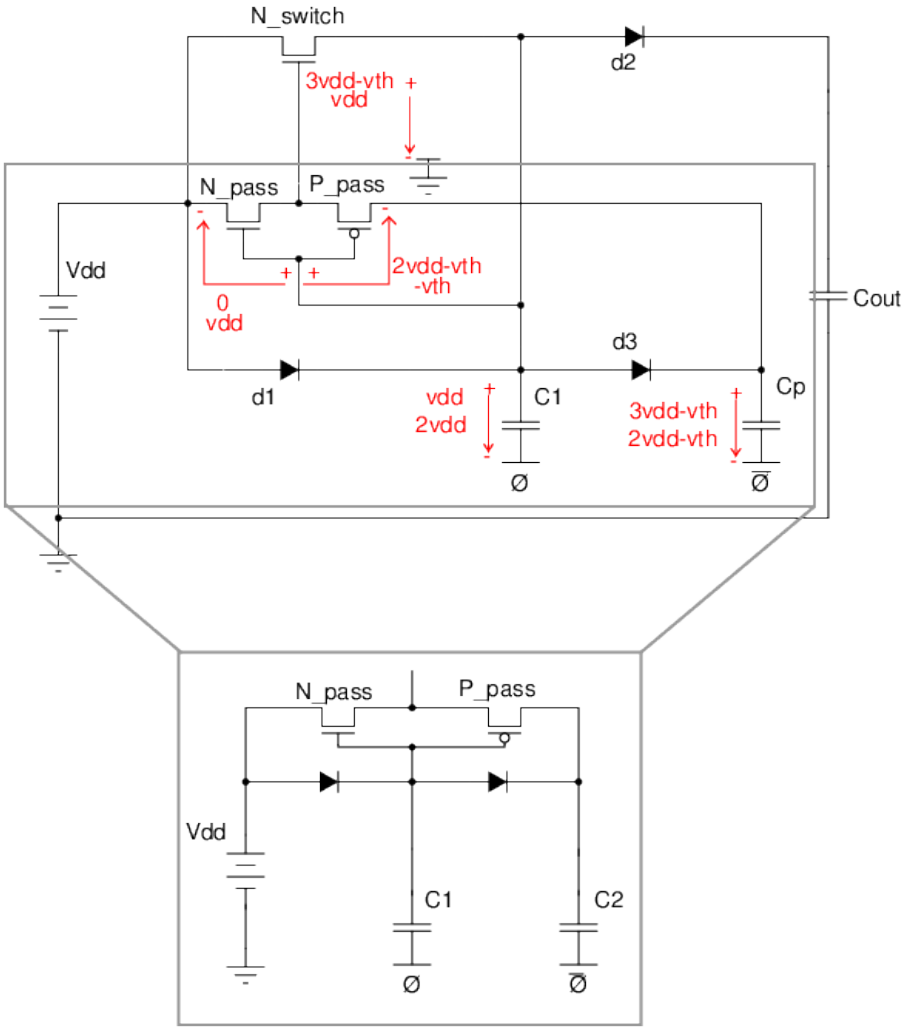

Figure 3.11: Proto-bi-level converter of Dynamic CTS charge pump.

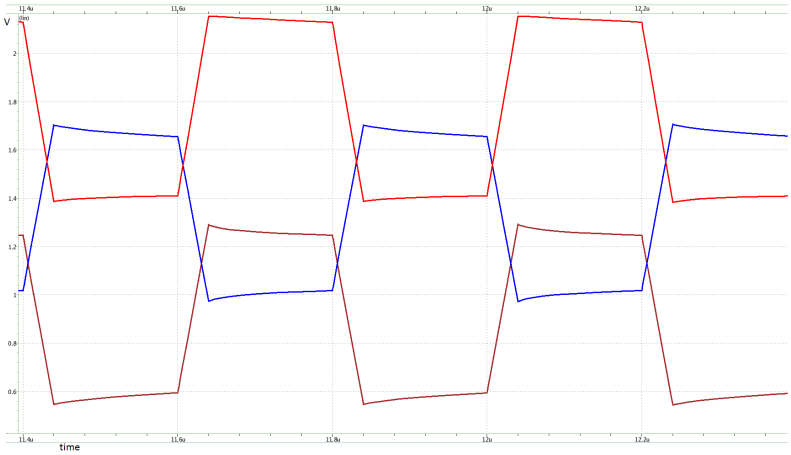

Figure 3.13: Wave aspect for each stage in Bi-level converter (First stage in brown, second stage in blue and third stage in red).

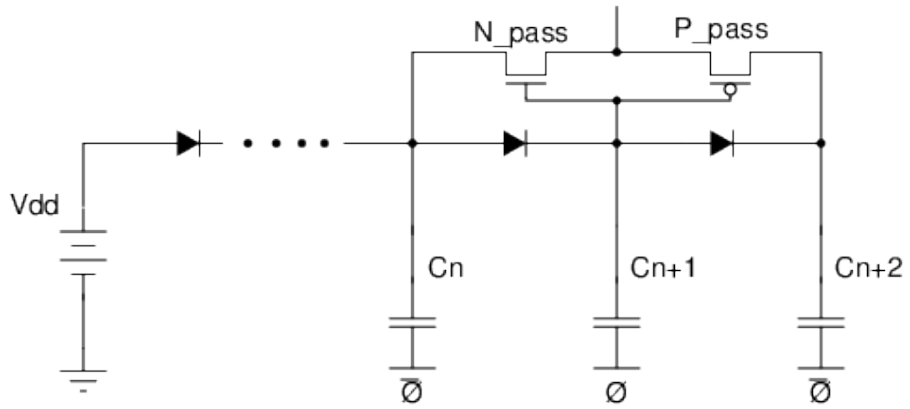

Figure 3.12: N-stages Singular Bi-level Converter.

The analyses of this is quite straight forward. Each stage alternates between a high and low voltage level. When a certain stage is high it charges the next stage voltage, which is V_{th} smaller than that of the previous stage. That stage then switches to the high voltage and charges the next stage. Adding the pass transistors makes it possible for an output capacitor to be charged to the highest voltage of the last stage, and discharged to the lowest voltage of the first stage in the next phase.

Looking in more detail into the pull-up part, as in figure 3.14. It may take some time for the capacitors to finish their charge transfer, but it is desirable that the final voltage of both capacitor is much closer to $4V_{DD} - 3V_t$, this final value is given by 3.31.

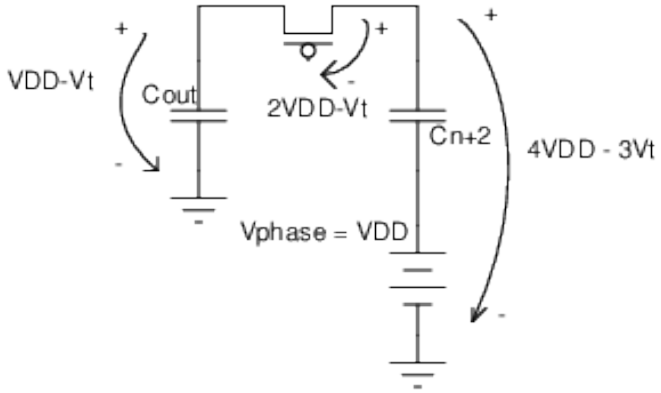

Figure 3.14: Aspect of circuit part responsible for charging the output.

$$V_{finalpullup} = \frac{C(4V_{DD} - 3Vt) + C_{out}(V_{DD} - Vt)}{C + C_{out}} \tag{3.31}$$

In the pull-down the analogous happens:

$$V_{finalpulldown} = \frac{C(V_{DD} - Vt) + C_{out}(4V_{DD} - 3Vt)}{C + C_{out}} \tag{3.32}$$

From this it possible to get the difference between the high level and the low level, an important information when designing a bi-level converter for a switch, having:

$$V_{pp} = \frac{C(4V_{DD} - 3Vt) + C_{out}(V_{DD} - Vt) - C(V_{DD} - Vt)}{C + C_{out}} \tag{3.33}$$

Simplifying the equation:

$$V_{pp} = \frac{C(3V_{DD} - 2Vt) - C_{out}(3V_{DD} - 2Vt)}{C + C_{out}} \tag{3.34}$$

If the C_{out} is defined as a proportion of C, $C_{out} = \alpha$ C.

$$V_{pp} = C(3V_{DD} - 2Vt).\frac{1-\alpha}{1+\alpha} \tag{3.35}$$

C_{out} is whatever load capacitance the pass transistors are charging but it always includes the stray capacitances between the drain and substrate of the two transistors, so increasing W to reduce their pull-up and pull-down resistance also increases their stray capacity that reduces V_{pp}. Of course, if C_{out} is much bigger than the strays, then there will be no impact.

Figure 3.15 shows a single stage bi-level converter with all the stray capacitors that are involved. Cgs, Cgb, Cdb and Csb are concerning the NMOS diodes, Cgs_n_hv, Cgd_n_hv, Cdb_n_hv and Csb_n_hv are concerning the NMOS pass transistor, which is a high voltage transistor and Cgs_p_hv, Cgd_p_hv, Cdb_p_hv and Csb_p_hv are concerning the PMOS pass transistor, which is also a high voltage transistor.

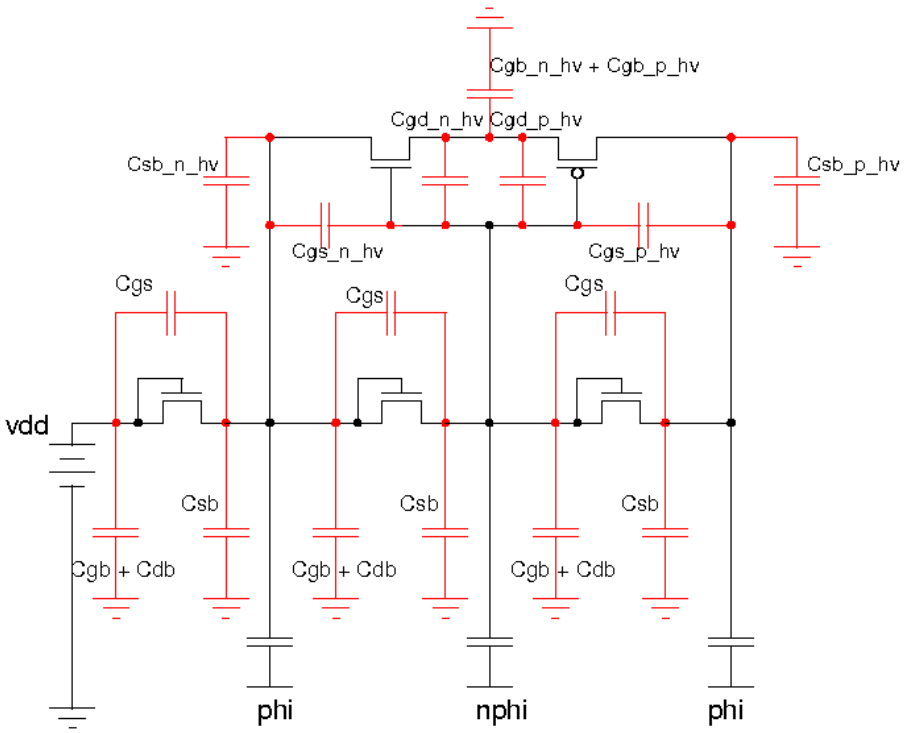

Figure 3.15: Single-Floor Bi-level converter with all the transistors' stray caps represented.

Simplifying 3.15, figure 3.16 emerges.

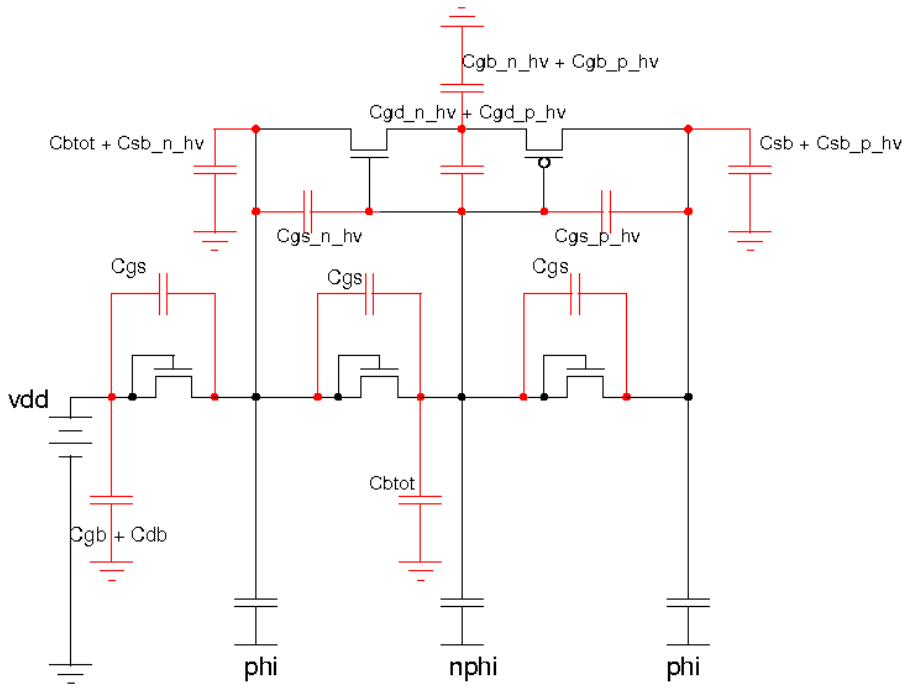

Figure 3.16: Single-Floor Bi-level converter with all the equivalent stray capacitances of the transistors represented.

As an example and to demonstrate the limitations of this, a simulation was ran with the bi-level converter including the pass transistor using minimum size to minimize stray capacitance.

The results of this are in figure 3.17.

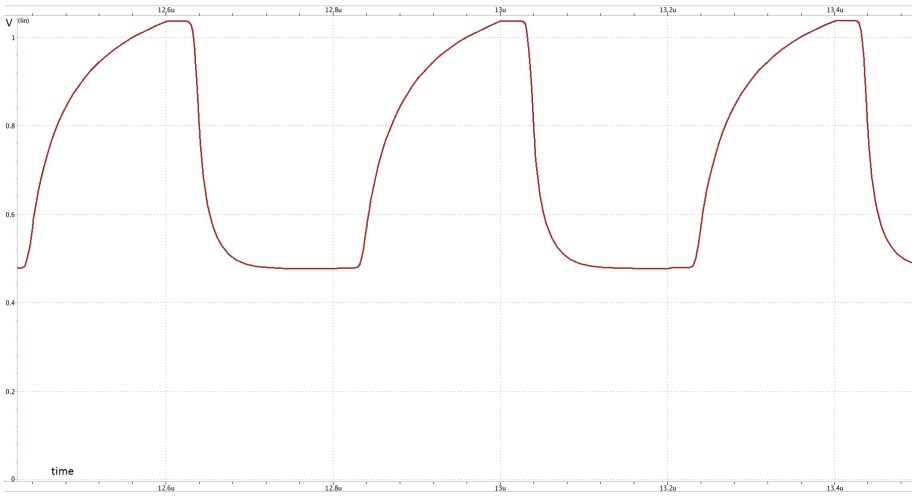

Figure 3.17: Waveform of the output of a Bi-level converter with pull-up problems.

Clearly the pull-up has difficulties whilst the pull-down does not, this is natural because the PMOS has a higher R_{on} for these conditions. Knowing that for the voltage to attain 63.2% of total amplitude, it is going to take a duration of one time constant, which is equal to RC. Here C, is the

series of the two capacitors, which will be dominated by the smaller one, its value is 260fF. So taking this into consideration, we can estimate R from the RC time constant of the circuit. Since during the rise, the voltage varied from 0.483V to 1.04V, that is a variation of 0.557V, 63.2% of that is 0.35V. So, a time constant is the time the voltage takes to reach 0.483 + 0.35, which is 0.835V. It took about 51ns for the signal to reach that value. Therefore the resistance is

$$R_{on} = \frac{51n}{260f} = 196154\Omega \tag{3.36}$$

So the R_{on} of the pull-up is around 196k Ω. This resistance can be reduced by increasing W/L of the transistor, also if the frequency is reduced this rise would not be as noticeable. The period here is 200ns and ideally we want it settled at the end. So, if we assume 20 time constants for the signal to have time to reach its maximum, this means: $20RC = 200ns$. R = 38461 Ω. This is 5 times less than current resistance. Repeating the experiment with a PMOS with 5 times larger WL, the results can be seen in figure 3.18.

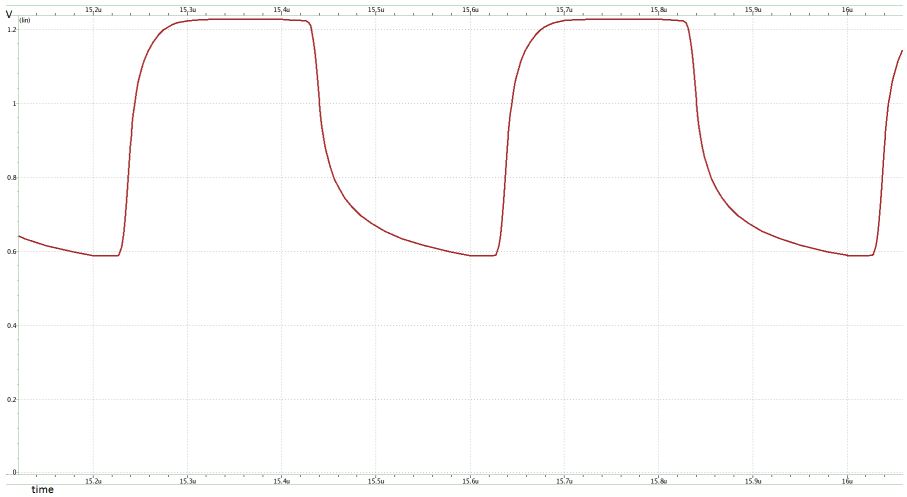

Figure 3.18: Waveform of the output of a Bi-level converter with pull-down problems.

Now the difficulty is in pulling down the node, because the PMOS is in the border of being *off* and with five times less resistance then before makes it harder to pull down the line.

This problem is made worse for bigger loads but a balance can be found, and this problem may not exist if the the frequency of operation is low enough. This shows the limitations of a single stage bi-level converter for this kind of loads.

Additionally, even if the frequency of operation or the load's capacitance is reduced the peak-to-peak value might not be sufficient for a certain switch. A switch may need higher difference between the low and the high level to be adequately turned *off* and *on*. If that is the case, one solution would be to use a bi-level converter with more stages of diode-capacitors and another stage of pass transistors on top, as shown in figure3.19.

There is now another level of pass transistors on top of the chain. It dynamically chooses the higher and lower level of the two smaller bi-level converters. The new voltage levels can be seen

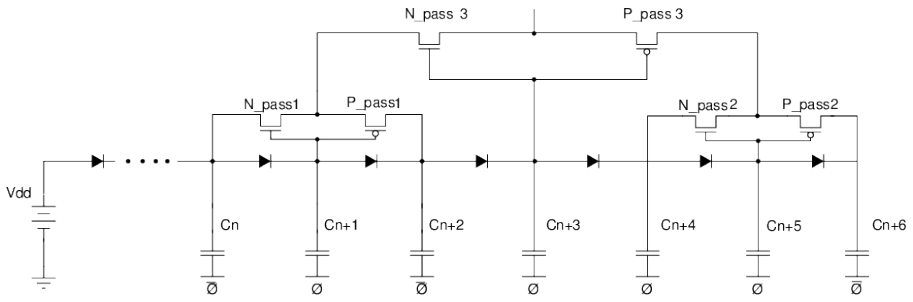

Figure 3.19: Two-stage Dynamic CTS Charge Pump.

in table 3.5.

Table 3.5: Relevant voltages of a two-stage dynamic CTS Charge Pump.

Phase	$Bi-level1$	C_{n+3}	$Bi-level2$	Vgs(N_pass3)	Vgs(P_pass3)	Drain
Φ	nV_{DD}-nVt	(n+4)V_{DD}-(n+3)Vt	(n+4)V_{DD} - (n+4)Vt	$4V_{DD}-3Vt$	Vt	nV_{DD} - nVt
$\bar{\Phi}$	(n+3)V_{DD}-(n+2)Vt	(n+3)V_{DD}-(n+3)Vt	(n+7)V_{DD} - (n+6)Vt	-Vt	$-4V_{DD}+3Vt$	(n+7)V_{DD} - (n+6)Vt

Now the difference between two levels is $7V_{DD}-6Vt$, a bigger fluctuation than in the previous proposal of just $3V_{DD}-2Vt$, in the best case. However, it is important to clarify the following: When the output is charged or discharged by the drain of the two top-level pass transistors, current flowing has to pass two transistors, there is a bigger R_{on} than in previous converters. The top pass transistor is well turned *on* because of having a large V_{gs} (positive for the NMOS, negative for the PMOS), so their R_{on} is lower than in the lower level pass transistors, but the transistors of the lower level have lower V_{gs}. This can be a problem because the R_{on} of the total pull-up and pull-down limits the speed at which the output can be charged and discharged, and therefore limit the frequency of operation of the bi-level converter.

The results for simulations with no load capacitor, although there are still stray capacitances, can be seen in figure 3.20. It is easy to observe the difference in peak-to-peak voltage, but the interesting part is to see its ability to handle a load.

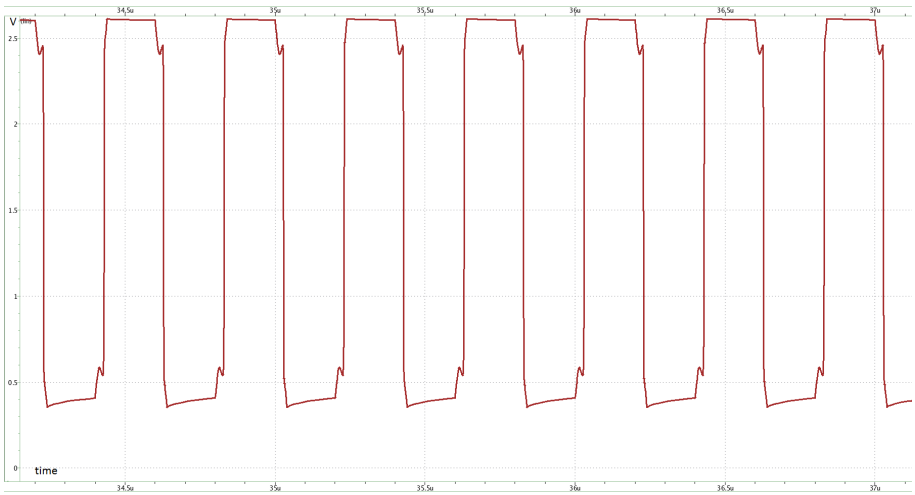

Figure 3.20: Waveform of the output of a two-stage dynamic CTS Charge Pumps.

Results for simulations with the same load as the single stage bi-level converter, of 350fF, are in figure 3.21.

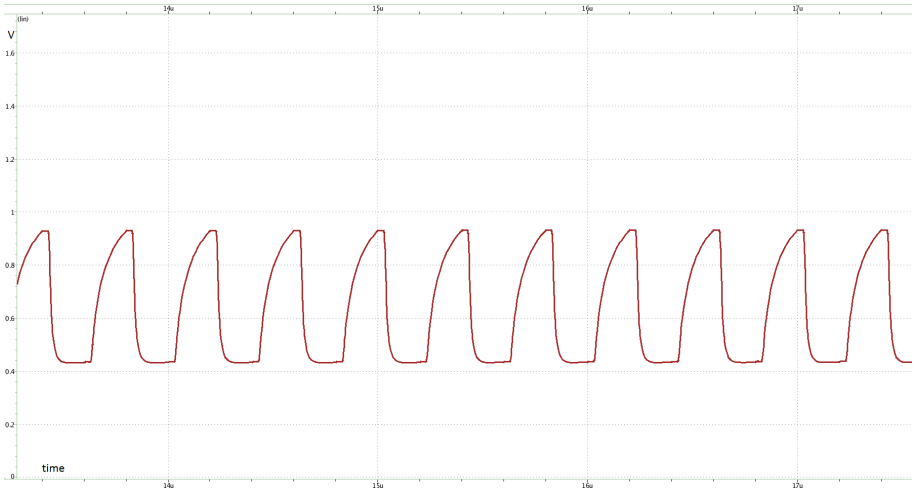

Figure 3.21: Output voltage waveform of Two-stage Dynamic CTS Charge Pump with a significant load.

Although this topology of converter has a higher peak-to-peak voltage, for a significant load, it has a lot more difficulty charging it than the single stage bi-level converter.

Another possibility for a converter of this kind, involves using an intermediate single stage bi-level converter, used as part of a bigger bi-level converter as seen in figure 3.22.

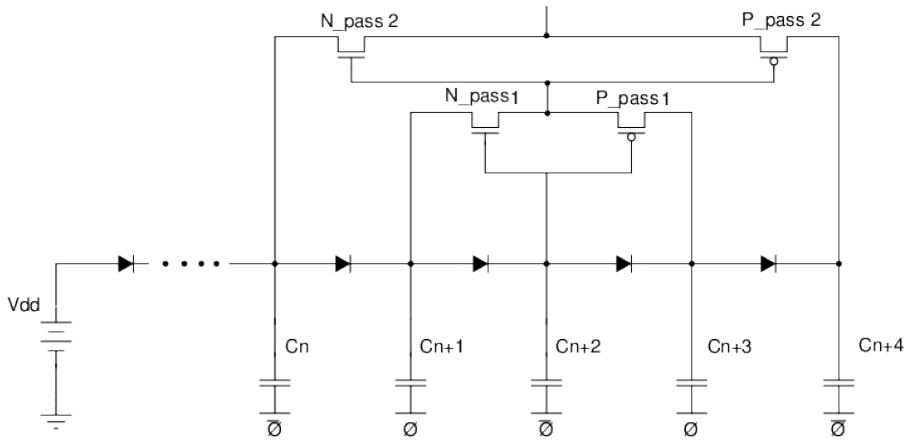

Figure 3.22: Intermediate floor Bi-level converter with pre-added stages.

The dynamic operation of this converter can be seen in table in table 3.6.

Table 3.6: Comparative table of different bi-level converters.

Phase	C_n	Intermediate Bi-level	C_{n+4}	Vgs(N_pass2)	Vgs(P_pass2)	Drain
Φ	nV_{DD}-nVt	(n+4)V_{DD}-(n+3)Vt	(n+4)V_{DD} - (n+4)Vt	$4V_{DD}-3Vt$	Vt	nV_{DD} - nVt
$\bar{\Phi}$	(n+1)V_{DD} - nVt	(n+1)V_{DD}-(n+1)Vt	(n+5)V_{DD} - (n+4)Vt	-Vt	$-4V_{DD}+3Vt$	(n+5)V_{DD} - (n+4)Vt

The difference between the two levels is $5V_{DD}-4$Vt, but the pull-up and pull-down resistances are again of a single transistor. However, these will now have a large Vgs, as desired. A comparative table of the three solutions is presented in 3.7. With the highest amplitude we have the two stage Bi-level but with the highest difficulty in pulling up and down. If the amplitude is sufficient the intermediate stage bi-level is a robust solution because it allows a lower pull-up and pull-down resistance.

Table 3.7: Variation of Vgs Voltages for High Voltage transistors.

Converter	Amplitude	$R_{pull-up}$	$R_{pull-up}$
Single stage Bi-level	3V_{DD}-2Vt	R_{P-pass}(Vgs = 2V_{DD} - Vt)	R_{P-pass}(Vgd = $-2V_{DD}$ + Vt)
Two stage Bi-level	7V_{DD}-6Vt	R_{P-pass}(Vgs = 2V_{DD} - Vt)+R_{P-pass}(Vgs = 4V_{DD} - 3Vt)	R_{P-pass}(Vgd = $-2V_{DD}$ + Vt)+R_{N-pass}(Vgd = $-4V_{DD}$ + 3Vt)
Intermediate stage Bi-level	5V_{DD}-4Vt	R_{P-pass}(Vgs = 4V_{DD} - 3Vt)	R_{P-pass}(Vgs = $-4V_{DD}$ + 3Vt)

A fundamental thing to mention is that to increase the output voltage of a bi-level converter two solutions exist, increasing the ratio between the capacitors of the bi-level and the load capacitance. The other solution is adding pre-stages but this causes both V_{low} and V_{high} to rise. However these should be limited to enable adequate voltages turning *off* in the V_{low}, and to protect the transistor in the V_{high}. Area minimization is a concern, and the area of the circuit will be largely due to the capacitors of the bi-level converters, which will be internal and made of metal coupling capacitances.

3.4.2 Choice of bi-level converter

For the reasons already mentioned in this work, we will use converters of the intermediate type. This allows low R_{on} resistances when pulling up or down the output while still having high enough peak-to-peak voltages. When needed V_{low} and V_{high} voltage will be increased adding pre-stages. The schematic showing the final proposal including all this information will be presented later.

3.5 Parameter Definition and Optimization

Until this point, some fundamental aspects were mentioned for the understanding of this circuit, but the parameters of this Charge Pump have yet to be established. These parameters are: C_1, C_out, T_{charge}, $T_{discharge}$ and the R_{on} of the switches. From T_{charge} and $T_{discharge}$ the frequency of operation is directly derived from:

$$f = \frac{1}{T_{charge} + T_{discharge}} \tag{3.37}$$

This, naturally, allows a certain freedom in parameter definition, so it is important to know what are the limits of these parameters. C_1 and C_{out} will be external capacitors, this means that they will cost the same for reasonable capacitances and occupy approximately the same area. The frequency of operation typical for this applications range from hundreds of kHz o a few tens of MHz. Although, obviously higher frequencies will cause more restrictions, namely: faster comparators and lower RC allowed on paths. The R_{on} of the switches will depend basically on the V_{gs} and W/L of the transistors. The NMOS switches will, during the steady state, be in triode region when conducting. This is because the V_{ds} voltages will be small, and V_{gs} voltages large. Therefore their current will be given by [17]:

$$i_D = k'_n \frac{W}{L}(V_{ov} - \frac{1}{2}V_{ds})V_{ds} \tag{3.38}$$

R_{on}, knowing that $V_{ov} \gg V_{ds}$, can be approximated by:

$$R_{on} = \frac{1}{k'_n \frac{W}{L} V_{ov}} \tag{3.39}$$

So to reduce the resistance, either V_{gs} or W/L are raised. The problem with this is that the switch's gate is charged by the bi-level converter, and if W/L is increased (assuming L is the minimum, this means an increase of W) the gate capacitance also increases and it will be harder for the bi-level converter to charge that capacitance. So independently of the way the resistance is lowered, by increasing V_{ov} or W/L, this will require a more powerful bi-level converter. A more powerful bi-level converter is one with higher number of stages or bigger internal capacitors. Both of these conditions will mean more area, since the capacitors of each bi-level converter will be internal as opposed to the power ones, which will be external.

An optimizations was ran to find the durations of the charge phase T_{charge} and discharge phase, $T_{discharge}$, the frequency of operation and the size of the capacitors. The basic idea is to define parameters that allow the higher possible R_{on} resistance of the switches that still allow the circuit to operate within the defined specifications.

So, as explained back in section 3.3.1, during the phase in which the output is charged, the voltage at the output capacitor rises to a certain point and it starts to decrease due to the action of the load, so our objective is to know the expression for the maximum V_{out} and then assure that this value is 1.2+ $\frac{V_{ripple}}{2}$. The value for maximum V_{out} is obtained by replacing t in the equation for the voltage during phase two 3.22 with the expression for t_{opt}, the instant of the maximum voltage, given by expression 3.26 results in 3.30.

This expression depends on $V_{c1}(0)$ that is the voltage at C_1 in the beginning of discharge phase. The rest of the variables are already known, except for α and of course, R_{on}.

V_{c1} may start at $V_{c1}(0)$ but C_1 discharges during this phase, and the next phase it is recharged again to $V_{c1}(0)$. So voltage at the beginning of the charge phase ($V_{c1}(0)$) is the voltage at the end of the discharge phase $V_{c1}(T_1)$.

During the discharge phase V_{c1} is given by:

$$V_{DD} - (2V_{DD} - Vmax) \cdot e^{\frac{-t}{R_{on}C_1}} \tag{3.40}$$

The duration t, is in this case T_1 and it is given by:

$$T_1 = \frac{V_r C_o}{I_o} \tag{3.41}$$

$$V_c1(T_1) = V_{DD} - (2V_{DD} - Vmax) \cdot e^{\frac{-V_r \cdot C_o}{I_o \cdot R_{on}C_1}} \tag{3.42}$$

$$V_{c1}(T_1) = V_{DD} - (2V_{DD} - Vmax) \cdot e^{\frac{-V_r}{I_o \cdot R_{on}\alpha}} \tag{3.43}$$

Remembering $V_{c1}\ (T_1) = V_{c1}\ (0)$, but it is defined as a function of the same variables as V_{max}. The procedure for this optimization is the following:

- An α vector is defined.
- An initial R_{on} is chosen.
- V_{c1}(T) is defined as function of α.
- t_{opt} is defined as function of α.
- Values of α that originate negative or complex values of t_{opt} are filtered.
- V_{max} is defined as function of α.

- If in all values of of V_{max} vector there is a value that equals or is greater than $1.2 + \frac{V_{max}}{2}$, the α that originates that V_{max} is chosen, if not R_{on} is decremented and the algorithm runs again.

Eventually a value of α and R_{on} will be chosen. Although t_{opt} has not a definite value, it is still a function of C. This means that a degree of liberty exits in choosing these parameters.

Knowing the R_{on} needed and knowing the maximum voltage that can be applied to a gate's switch we can determine the gate capacitance that has to be charged by the bi-level converter. A simulation was ran for some fixed capacitive loads, defined by the necessary R_{on}, in which the parameter varied was the period. The objective is to observe how the maximum achievable voltage of a bi-level converter is affected by frequency of operation.

The result is seen in figure 3.23.

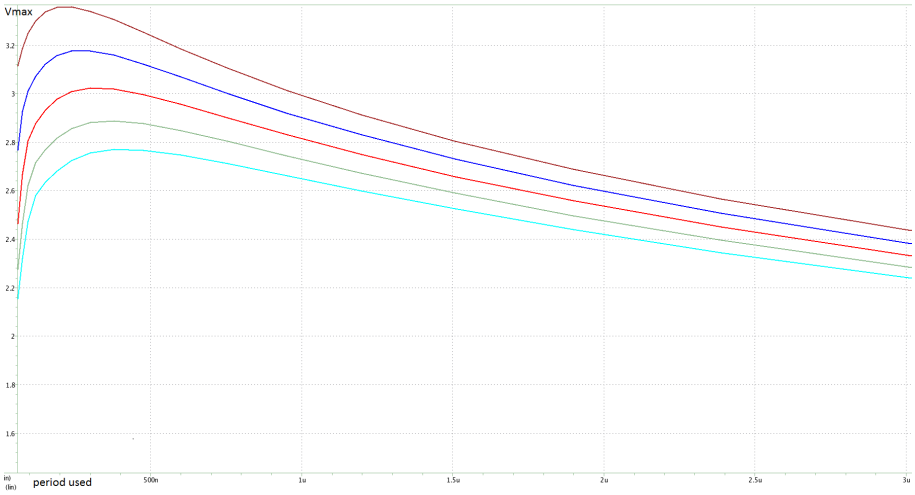

Figure 3.23: Maximum output voltage of a bi-level converter for different internal capacitances in function of period.

Each line represents a different value of the bi-level's internal capacitors.

It is observable that a peak exits for each line and that depends on the value of the internal capacitors. Approximately the maximum occur for periods between 200ns and 400ns. Having that into account, the ratio of the capacitors α and also choosing values for the capacitors that are readily available, we end up with the following parameters 3.8.

Table 3.8: Parameters.

C_1	100nF
C_{out}	150nF
Frequency	2.5MHz

3.6 Closed-Loop Regulation

Closed-loop regulation is unavoidable to reach this work's goals. Since this circuit is a switched-capacitor type, regulation will be done by managing the clock signal. The clock signal will be generated by a block specialized in doing that, but is not the focus of this work, although care was taken to ensure that the clock does not attack significant loads. The clock feed the regulators, and these will manipulate the clock as necessary.

3.6.1 Regulation of Bi-level Converters

Figure 3.24 demonstrates the bi-level converter output voltage regulation process.

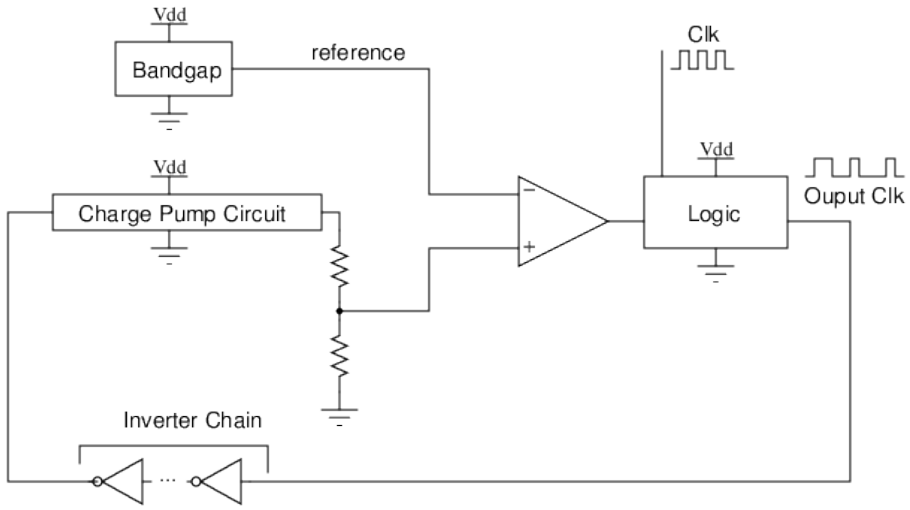

Figure 3.24: Regulation scheme of a Charge Pump.

A bandgap is used to generate a temperature independent voltage level. This is widely used in electronics and well known [18]. In this work the bandgap will not be designed. Because the level of the reference voltage has to be lower than the input voltage and the Charge Pumps outputs will be typically higher than the input voltage, a voltage divider will be required. In the figure it is resistive but it can also be capacitive to reduce consumption. The Charge Pump can be any individual bi-level converter. A comparison is done and by the use of a logic circuit an output clock with whatever processing needed will be outputted. This allows for the clock that feeds the system to charge minimal size logic gates only. An output clock is required for the Charge Pump. The output clock goes through an inverter chain so its fanout is appropriate. Two things should be mentioned about this:

- Having a chain of inverter with constant fanout with a specific value is not fundamental here, despite being so in other logic circuits. This is because the design methodology is used to minimize delay. Delay is not a concern here since all bi-level converters operate with identical delay. Also adding more inverters will only increase consumption. So the key in the dimensioning of this inverters is to have a small chain powerful enough to supply the

current needed by the bi-level converters and also to check the output alignment between all the bi-level converters. However, it is important to mention that a fanout that guaranties alignment between phases is still important.

- Additionally, the charge that the bi-level converters need to operate is obtained when the system is initialized and then the only current needed is to compensate looses. This is a fundamental idea and it is because when a bi-level charges an output it loses charge but when it discharges the output, it regains charge. So there is an energy conversion. Of course leakage current to the ground still have to be compensated but its steady state current needs are not so big.

Remembering, there are two key ideas when dimensioning the bi-level: The output should go low enough to turn *off* a switch, and it can not go high enough to avoid damaging the switch. Since the amplitude is known, regulation can be done by observing only one of the levels. The question becomes which is the more desirable level to observe. The answer is the lower level because the voltage divider will consume less this way since a smaller voltage will result in a smaller current.

It is then established that the control will look into the lower level voltage to decided its action, but what will the output clock actually control is the important part. For the operation of a bi-level converter, pulse skipping is not feasible since a certain bi-level cannot skip clocks if the others are not also doing so. The gate signals would be different for the same phase switch and the Charge Pump would not work. Instead the regulation is done be deciding if the pre-stages can be dynamically turned *off* and *on*.

For the reasons mentioned earlier instead of the control scheme of figure 3.24, the appropriate way to control the bi-level converter is shown in figure 3.25.

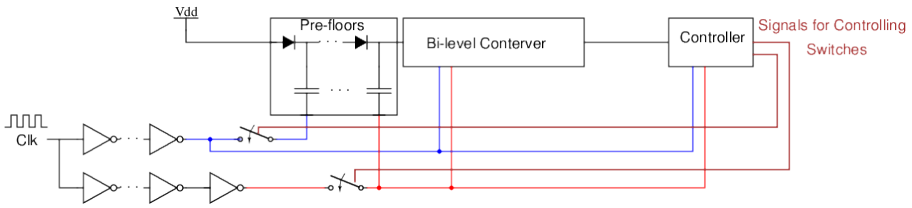

Figure 3.25: Regulation scheme of a Bi-level converter.

The equation that describes V_{low} and V_{high} can be seen in 3.44 and 3.45.

$$V_{low} = p(V_{DD} - Vth) \tag{3.44}$$

$$V_{high} = (p+a)V_{DD} - (p+a-1).Vth \tag{3.45}$$

where p is the number of pre-stages and its effect is in both levels (V_{low} and V_{high}), and a depends on the actual number of stages of the bi-level converter, excluding the pre-stages. As was seen before, there are ways of achieving a bi-level converter with different number of pumping stages, and therefore, different a.

Having this controller to turn *on* and *off* the previous stages to adjust the p factor is a very important realization of the work because even in the occurrence of PVT the output can be adjusted. With this scheme, levels are changed without altering the duration, number, or period of pulses.

3.6.2 Regulation of the Output

The values determined until this point, for the operation of the circuit, are supposed to assure the operation of the system in the worst circumstances, with the maximum load current possible, but when circumstances change, some control will be required. In this work, controllers were realized using Verilog-A modules that could be easily replaced by regular analogue comparators and simple logic. There will be presented two simple control topologies: PWM control and Pulse-Skipping control.

The idea behind the pulse-skipping control is that when the output is above the desired level a charge phase is skipped and the voltage continues to discharge.

The pulse skipping gives the possibility to avoid unnecessary switching that spend energy.

A diagram of the pulse-skipping controller can be seen in figure:

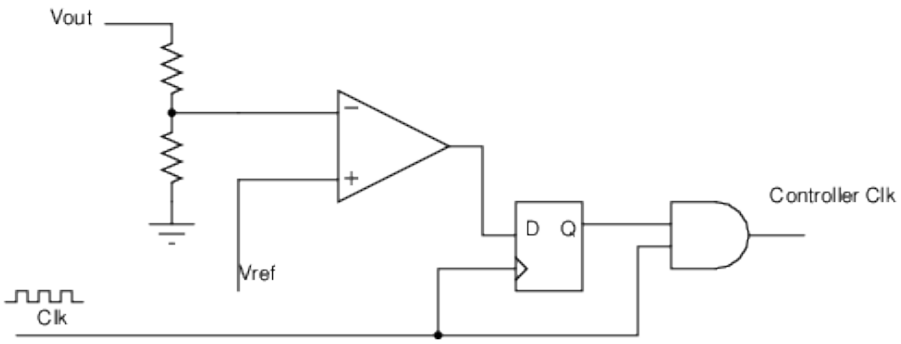

Figure 3.26: Pulse-Skipping Controller Diagram.

The reference can be created from a bandgap, and therefore is limited to the value of the supply. The resistive divider is needed to reduce the voltage of the output, since the output will have a voltage higher than the supply.

It is also important to present how another simple control solution would work. This simple solution is PWM control and can be seen in figure 3.27.

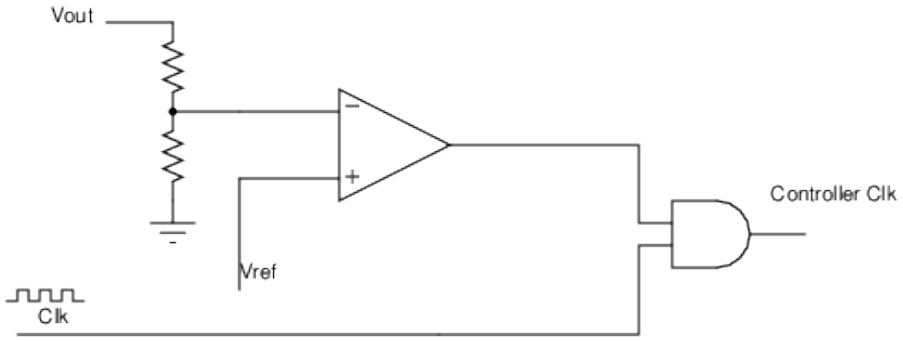

Figure 3.27: Pulse-Width Controller Diagram.

The *and* gate assures that when the clock is low, the controller clock will also be low. When the clock is high the state of the output clock will depend on the comparator's output. If the Charge Pump is in charge phase and, as so, the output voltage is increasing, when that voltage surpasses V_{ref} the output clock goes low and the charge phase is ended. This mechanism prevents the output voltage from going above V_{ref}. If either this solution or Pulse-Skipping are enough to adequately control the output voltage, deserves a deeper look.

The Charge Pump's performance is affected by PVT variations and also by the output current being drawn. As a simplification, we assume PVT variations can result in two different circuits: the high boost and the low boost. The high boost is the most optimist case in terms of easiness to boost voltage. This circuit happens when input the voltage is high, transistor's R_{on} are low, and V_{th} voltage is also low. The low boost is the pessimist case. This situation occurs when the input voltage is low, transistor's R_{on} are high, and V_{th} voltage is also high. As for the output current, we also assume two extreme cases. The maximum current (20mA), and a very small current. So four kinds of situations can occur, shown in table 3.9.

Table 3.9: Circuit Scenarios.

Circuit Scenario	Output Current
High Boost	High Current
High Boost	Low Current
Low Boost	Low Current
Low Boost	High Current

It is obvious that the hardest case for the Charge Pump is the Low Boost - High Current scenario. However, the circuit is designed in such a way that, in that case, with the chosen duty cycle, frequency, and component values, it is not needed any control to comply with ripple and average output. However none of the other scenarios would be compliant without any regulation. That is because these cases are less pessimist and as so boosting would be increased, leading to higher average output voltages.

The High Boost - Low Current scenario could be resolved with just PWM, using a reference of 1.2V. This is because in the discharge phases the output would not lose much charge, since output

current is low. In the charge phases the regulation would prevent voltage from going above 1.2V expected for small increases due to latency.

A representation of what happens in this case is given in 3.28.

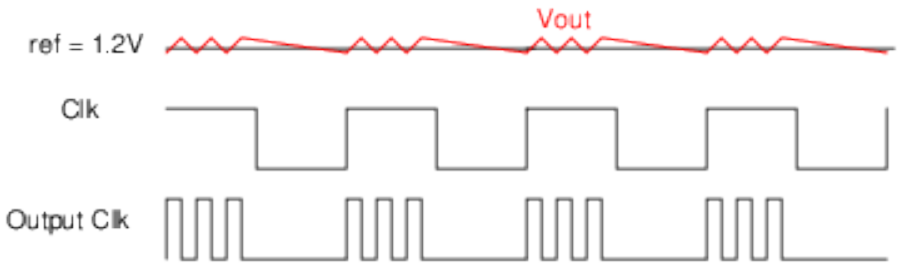

Figure 3.28: High Boost - Low Current case with PWM control.

During charge phase output voltage would oscillate around 1.2V. During the discharge phase the output would fall but not much since it is assumed a low current.

So, no regulation is need for Low Boost - High Current, and PWM regulation would be enough for High Boost - Low Current. The other cases are a bit more complex. First lets analyse the High Boost - High Current. The amount of charge that is lost in the discharge phase has nothing to do with the boost capacity of the circuit, it has only to do with the load current and the output capacitor (already estabilished). So if a PWM regulation was applied, the situation in figure 3.29 would occur.

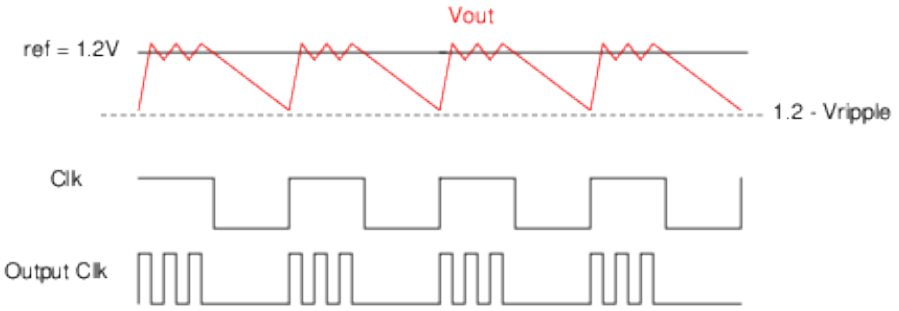

Figure 3.29: High Boost - High Current case with PWM control.

In the charge phase, the output would be kept around 1.2V. However in the discharge phase, the output would fall to 1.2 - V_{ripple}, and it should not go below 1.2 - $\frac{V_{ripple}}{2}$. PWM is clearly not appropriate for this scenario. Neither is Pulse-Skipping, and the reason is the following: If at a certain point, in the circuit's operation, it is decided to skip a pulse, it then takes another T seconds until the circuit can charge again. So the output capacitor discharges $I_o \cdot T$. This value is double of the accepted ripple, since at maximum current it takes approximately half a period for the circuit to vary the ripple and this T is more than that. The truth is that Pulse-Skipping is not appropriate for high load currents, only smaller ones.

The only case left to look at is Low Boost - Low Current. For PWM case, this is not much different than High Boost - Low Current. The only element that would vary would be the width

of the output clock's high level. In the discharge phase few charge is lost. In the charge phase the controller prevents output from going over 1.2V. PWM would be adequate for this case. Pulse-Skipping also would work for this case, and would work like shown in figure 3.30.

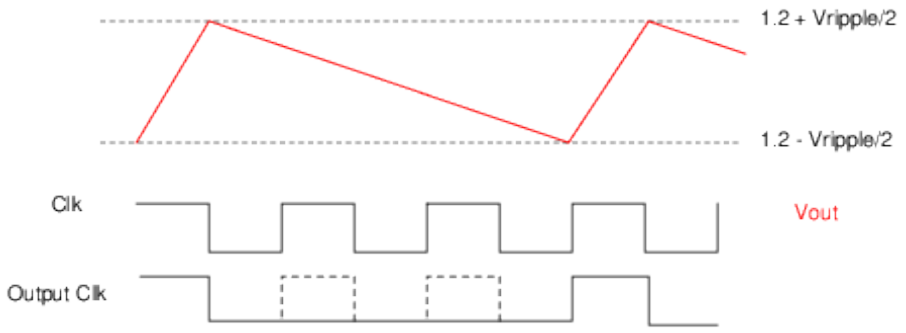

Figure 3.30: Low Boost - Low Current case with Pulse-Skipping Control control.

This situation has the advantage of being efficient, since a lot of pulses may be skipped.

A summary table of what was said about this, until this point, can be seen in 3.10.

Table 3.10: Summary table

Case		No Regulation	PWM (ref = 1.2)	Pulse-Skipping (ref = 1.2 - Vr/2)
High Boost	High Current	Doesn't comply	Doesn't Comply	Doesn't comply
High Boost	Low Current	Doesn't comply	Complies	Doesn't comply
Low Boost	Low Current	Doesn't comply	Complies	Complies
Low Boost	High Current	Complies	Doesn't Comply	Complies

None of these two solutions are compliant for all cases. The solution adopted involves using a combination of the two, and changing the reference voltages. The references to the PWM moves up to $1.2 + \frac{V_{ripple}}{2}$, this by itself prevents the voltage from ever getting above the upper limit.

For the Low Boost - High Current case, this control does not interfere, since for this case, only at the very end of the charge phase, the output voltage reaches the upper bound. In High Boost - High Current case the situation in 3.31 happens.

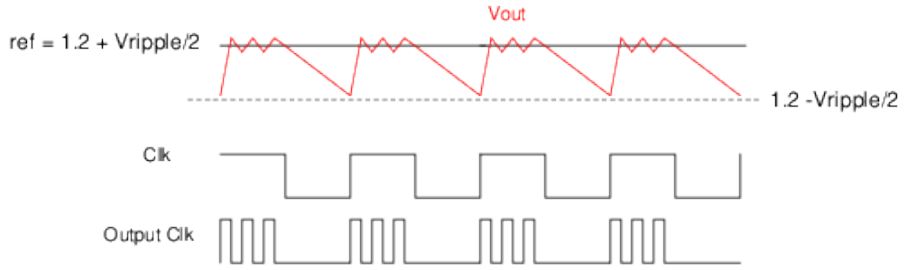

Figure 3.31: High Boost - High Current case with Pulse-Skipping and PWM Control control.

It is assured that the output does not go above the upper bound, and during the discharge phase, the output only falls to 1.2 + $\frac{V_{ripple}}{2}$, by design. So it is also assured that the lower bound is not passed.

However, for just PWM with a reference of 1.2 + $\frac{V_{ripple}}{2}$, both low output current cases will have problems, because as explained earlier, for low currents the output voltage will tend to follow the reference. There, the average output voltage would be around $\frac{V_{ripple}}{2}$, a situation that is undesired.

It is here that the pulse-skipping part acts and it would result in a situation as seen in figure

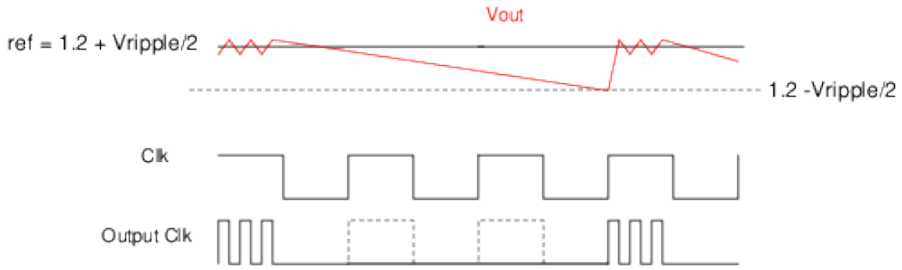

Figure 3.32: Low current cases with Pulse-Skipping and PWM Control control.

Both low current cases will comply. They would just differ only the width of the high levels of the output clock.

In the figure 3.33 it can be seen a representation of a scheme with both controls.

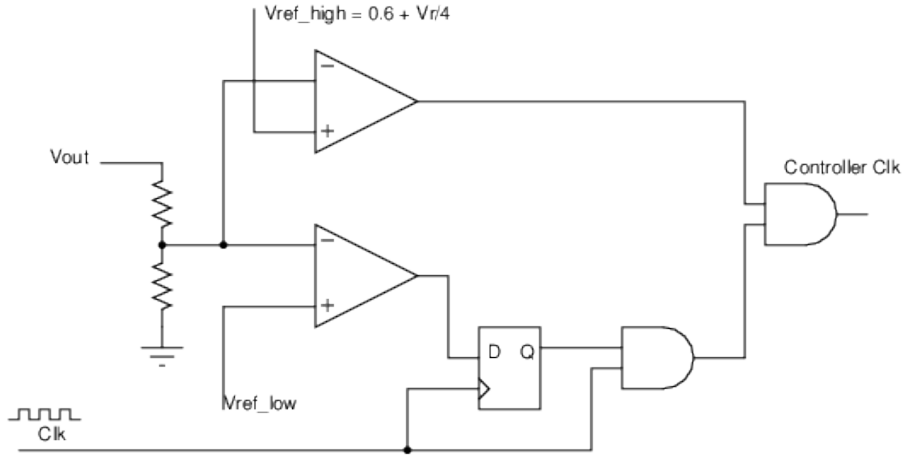

Figure 3.33: Pulse-Skipping and PWM Controller Diagram.

When the output rises above the maximum level allowed: $1.2 + V_{ripple}/2$ the output of the top comparator falls to zero and because of the and gate the output clock also falls to zero. When the output is above $1.2 - V_{ripple}/2$ charge phases are skipped, in this way the average value of the output is controlled.

Current loads that vary quickly and significantly still offer a challenge. This control does not totally guaranties that all possible cases are accomplished. However, this control covers a big range of loads, and offers good results as it will be seen in the simulation section.

3.7 Summary

In short, the Charge Pump used will be Series-Parallel in result of having to provide a relatively high current that other methodologies seen in Chapter 2 would fail to achieve.

Bootstrapping the NMOS is a necessary thing and how to achieve this with a bi-level converter was presented. They are converters that transform a DC input into a square wave. The voltage of the two stages can be increased by adding more stages but to increase the amplitude between the two stages only a different topology can enable this. Three topologies were presented, with varying amplitude and transition times. The choice depends on the context but an intermediate bi-level converter offer the lower pull-up and pull-down resistance while having a higher amplitude.

The key idea when choosing the dimensions of the power part of the circuit is to find the highest possible R_{on} that allows circuit operation. This is so, because in this way switches can be smaller and the bi-level that charges them can also be smaller. Bi-level converters are desired to keep small because their internal capacitor will be a major area contributor. The bi-level converters that will be used in this work have an important distinction from those seen in typical designs. That distinction is that the charge in the gates of the transistors that act like switches is recycled. This is different from designs like [5] in which gates discharge to ground and therefore is more wasteful.

Even after defining final dimensions, regulation is needed. It enables the circuit to deal with different loads, but also different environmental conditions. A combined solution of Pulse-Skipping and PWM is proposed. The Pulse-Skipping part looks to the level of output voltage and decides if a pulse can be skipped or not. The PWM part regulates the duration of the pulse. This control was not simulated in gate level, mainly because it is not the main focus of this work and because it can be implemented with simple comparators and gate-level logic. Instead, a Verilog-A module was used.

F

Chapter 4

Final Circuit Proposal and Results

4.1 Final Circuit Proposal

The final proposed circuit consists of a series-parallel Charge Pump, realized with four NMOS switches and two capacitors. The parameters of the circuit where mentioned back in table 3.8.

Switches are controlled with above supply gate signals generated with bi-level converters. The one used is the intermediate bi-level converter shown in figure 3.22, and was picked because of the high peak-to-peak voltage and low pull-up and pull-down resistance it presents. Bi-level converters have a controller to assure that voltages reach a sufficient level without surpassing safety limits. The scheme of this control was shown back in figure 3.24.

The output voltage is controlled with a pulse-skipping/pulse width modulation control, as presented in figure 3.33. When the output is above the required voltage, charge phases are skipped. If before the end of the charge phase the output has already gone above the required voltage, the phase is ended by the controller.

A digram of the solution is seen in figure 4.1.

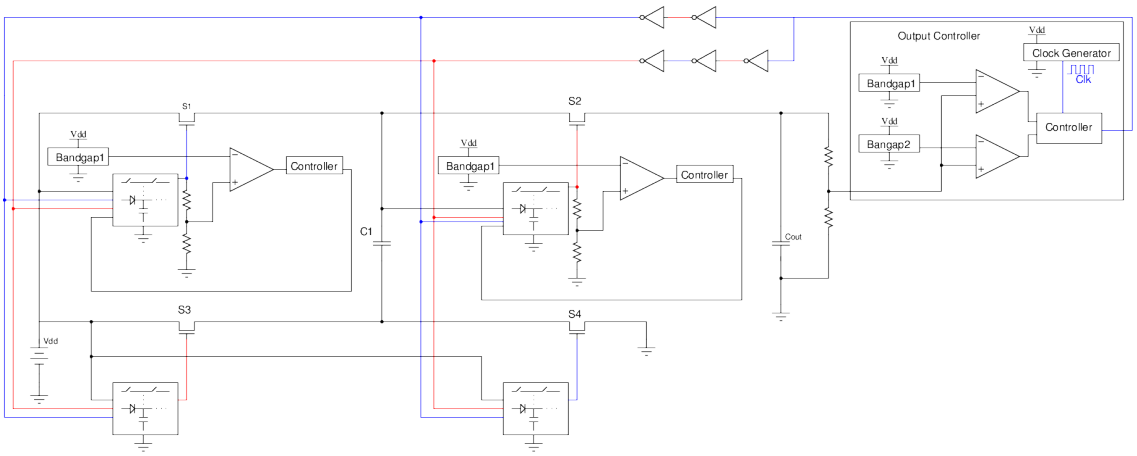

Figure 4.1: Diagram of the proposed circuit.

4.2 Simulations and Results

This chapter will be devoted to simulating the proposed solution.

4.2.1 Typical Ratings

To evaluate the performance of the circuit in typical conditions: process, voltage and temperature.

A simulation was ran with a steady load of 10mA, half the maximum load.

The output wave is in figure 4.2.

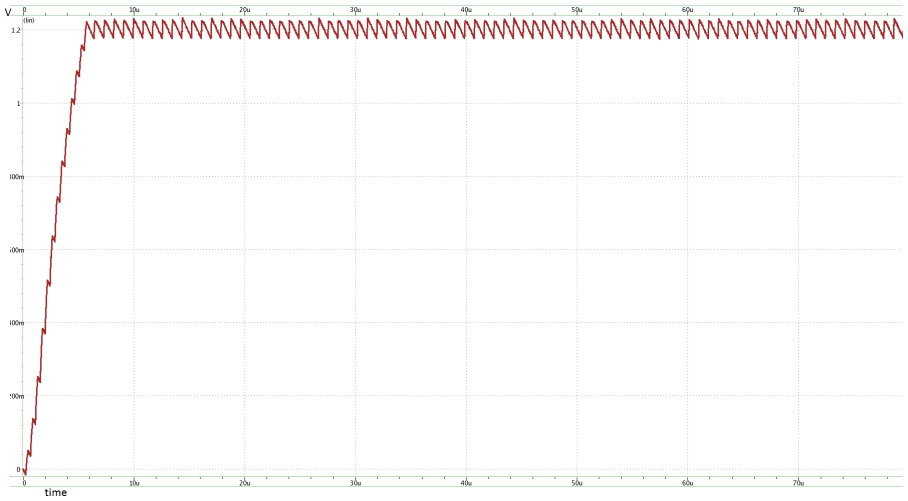

Figure 4.2: Output voltage waveform for the typical case, supplying 10mA.

The metrics that can be obtained from the simulation are in tables 4.1.

Table 4.1: Metrics for circuit performance supplying a current of 10mA.

Avg. Vout	1.2V
Io	10mA
Ripple	4.72%
Io / Iabs	24.9%
Efficiency	37.4%

4.2.2 Line Regulation

A simulation was ran to evaluate the line regulation of the circuit. Line regulation consists in fixing a certain load and then varying the input voltage to evaluate the impact of that on the output voltage.

Line regulation is defined by:

$$LineRegulation = \frac{V_{out}(maxVdd) - V_{out}(minVdd)}{V_{out}(nomVdd)} * 100\% \tag{4.1}$$

First, the typical case with the maximum output current (20mA) is tested and the resulting output voltage waveforms for each input voltage is seen in figure 4.3.

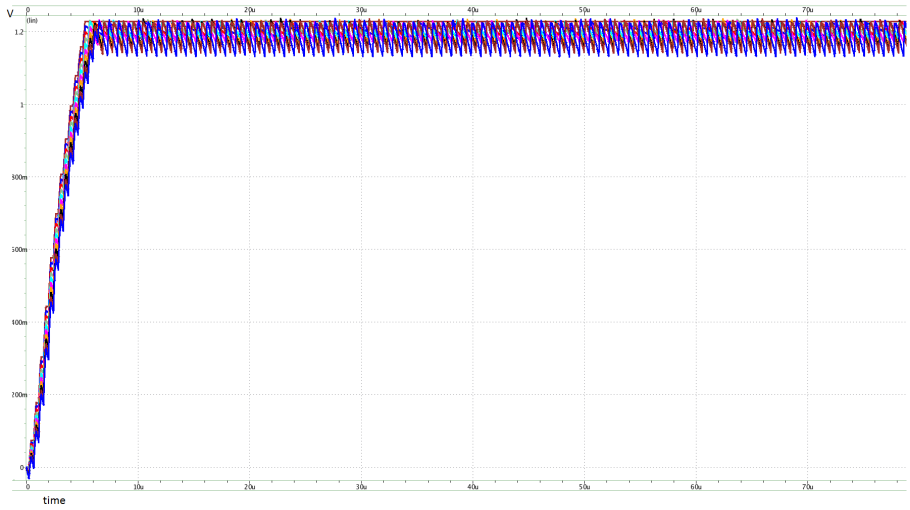

Figure 4.3: Output voltage waveform for various input voltages.

The average output voltage for each input voltage is presented in figure 4.3.

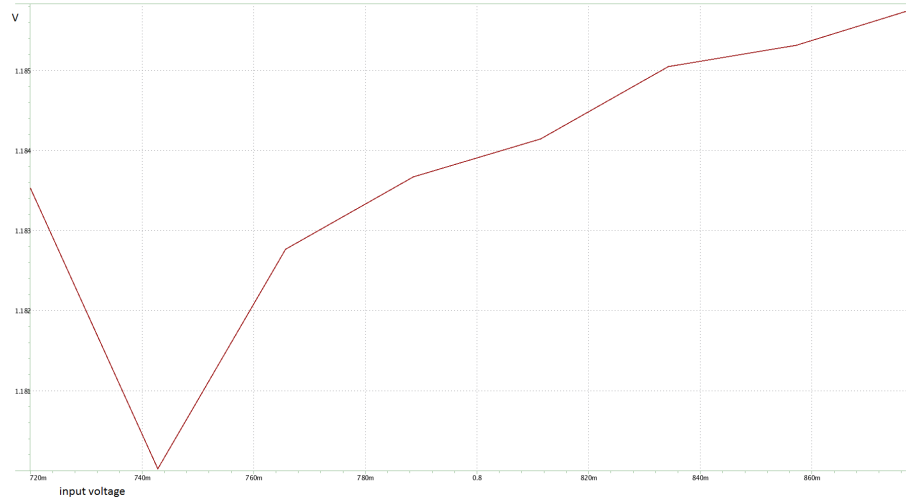

Figure 4.4: Output voltage waveform for various input voltages.

The Line regulation, for the typical case is:

$$LineRegulation = \frac{1.19 - 1.183}{1.2} * 100\% = 0.58\% \tag{4.2}$$

Simulation was repeated for extreme corners, table 4.2 summarizes the corners that were simulated:

Table 4.2: Corner simulated for line regulation.

V_{DD}	from: 0.72V	to: 0.88V	n^o points: 8	
Temperature Values	-40	125		
Transistor	SS	SF	FS	FF
High Voltage Transistor	SS	SF	FS	FF

The output voltages for each corner and input voltage can be seen in figure 4.5.

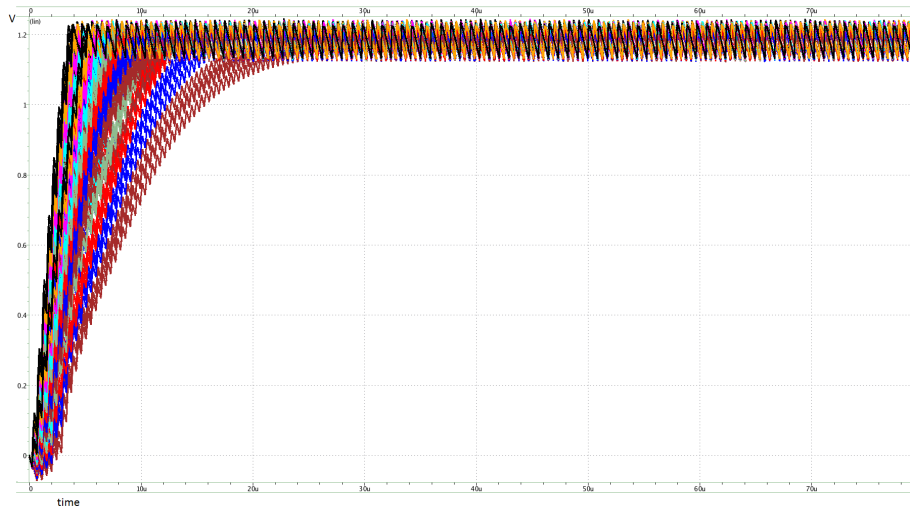

Figure 4.5: Output voltage waveform for various input voltages at various PVT corners.

And for each corner there is a line regulation wave, that demonstrates how the average output voltage varies with the input voltage. This is seen in figure 4.6.

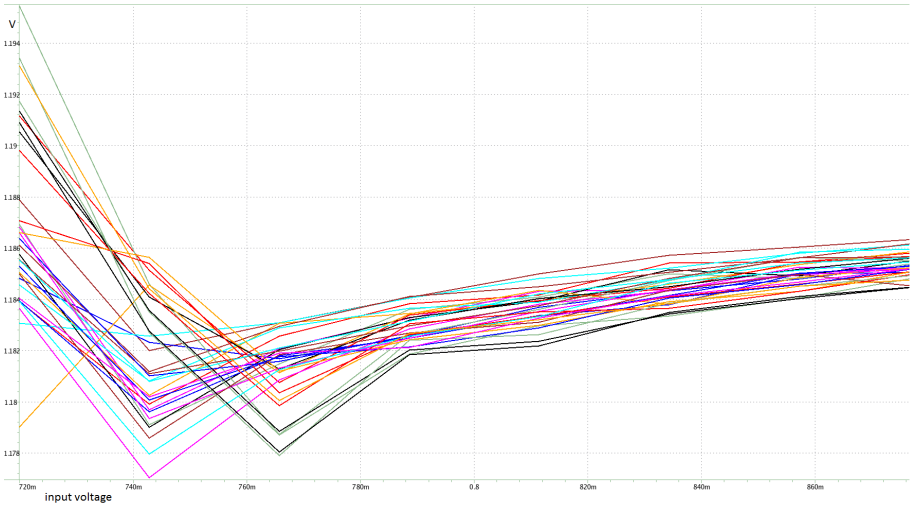

Figure 4.6: Average Output voltage as a function of input voltage for each corner.

The worst line regulation is of 1.42%.

4.2.3 Load Regulation

Load regulation measures the effect on the output voltage due to different values of the output current.

$$LoadRegulation = \frac{V_{minload} - V_{maxload}}{V_{nominalload}} \tag{4.3}$$

As in the line regulation, a simulation was ran to evaluate load regulation in the typical case.

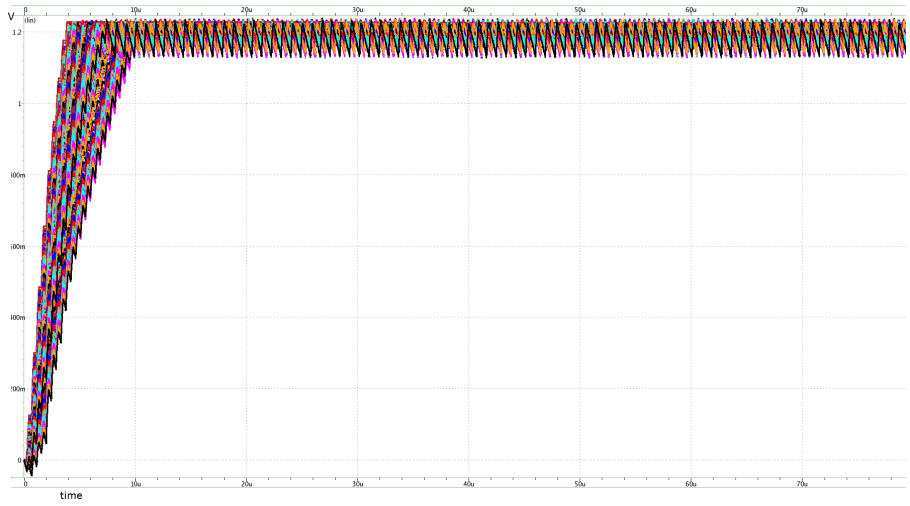

Figure 4.7: Output voltage wave for various output currents.

The average output voltage for each output current is seen in figure 4.3.

Figure 4.8: Output voltage waveform for various input voltages.

$$LoadRegulation = \frac{1.227 - 1.184}{1.2} * 100\% = 3.58\% \tag{4.4}$$

Then, the extreme cases, represented in table 4.3. where simulated:

Table 4.3: Variable sweeped for line regulation simulation.

V_{DD}	from 0.72V	to 0.88V	nº points: 8	
Temperature Values	-40	125		
High Voltage Transistor	SS	SF	FS	FF

The output wave for each corner and for each load is seen in figure 4.9.

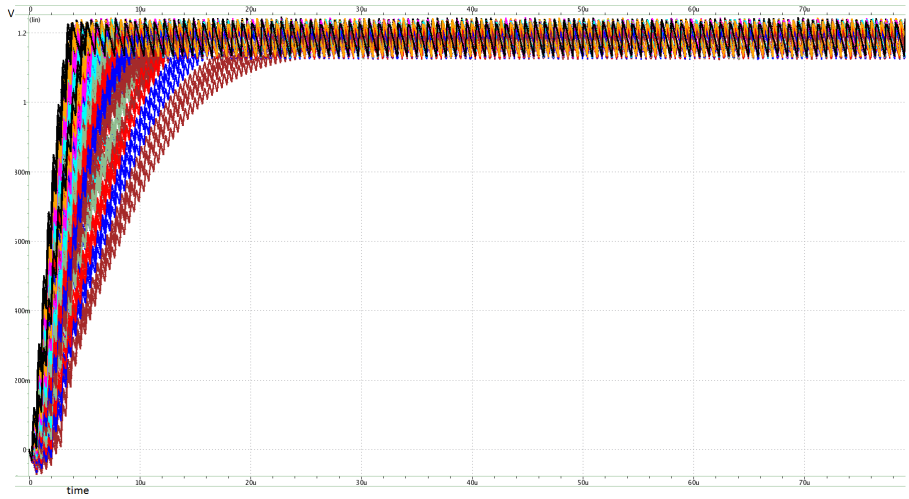

Figure 4.9: Output voltage wave for various output currents at various corners.

And for each corner there is a load regulation wave, that demonstrates how de average output voltage varies with the output current. This is seen in figure 4.10.

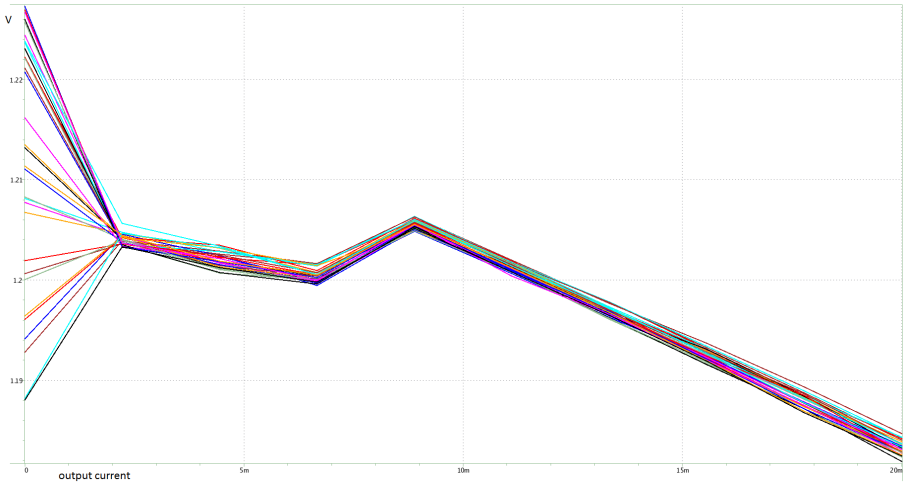

Figure 4.10: Output voltage wave for various output currents at various corners.

The worst load regulation is 3.92%.

4.2.4 Irregular Loads simulation

A simulation was ran using as a load current source signals in a form of a: triangular wave, pulse wave, sine wave and one resistor.

Each current waveform is shown in figure:

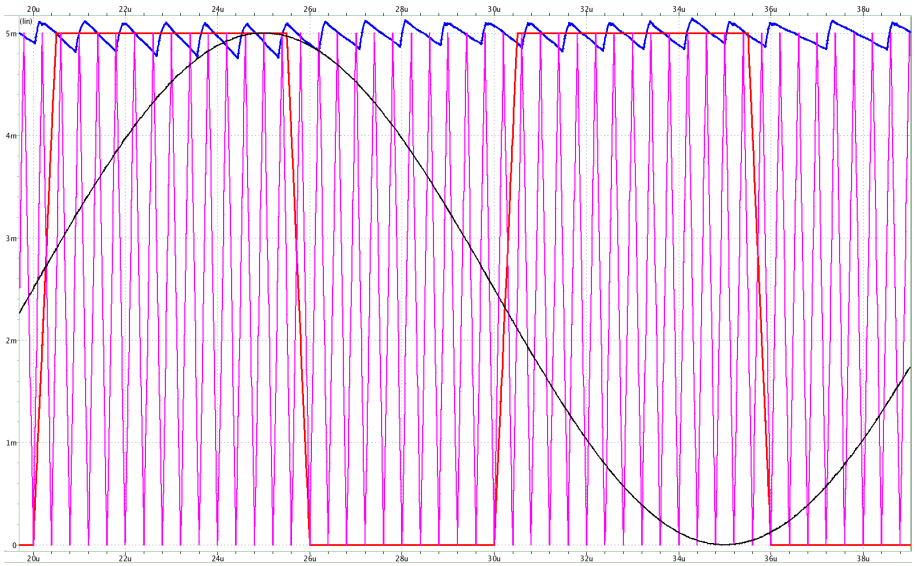

Figure 4.11: Currents applied as loads.

This results in a total waveform with the following shape:

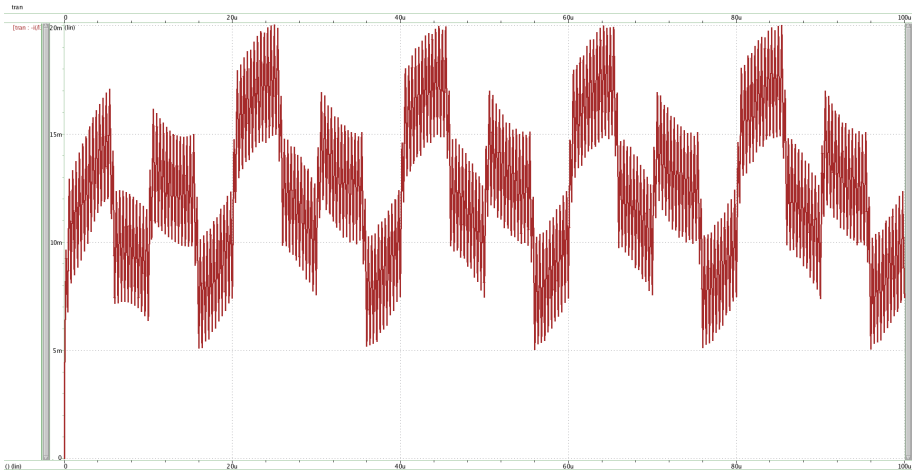

Figure 4.12: Current applied as load.

The simulation was ran in the presence of all corners. As shown in table:

Table 4.4: Test corner of irregular load simulation.

V_{DD}	0.72V	0.8V	0.88V		
Temperature Values	-40	125	25		
Transistor	SS	SF	FS	FF	TT
High Voltage Transistor	SS	SF	FS	FF	TT

The medium value of the output as function of the process and temperature can be seen in Appendix A in figure A.1.

It is noticeable that the output voltage, although varying only between 1.2V and 1.192V, is particularly sensitive to the input voltage. Naturally a lower V_{DD} leads to slightly lower output voltage. To better illustrate this, a figure is presented in figure A.2.

Another important metric is efficiency that is defined as:

$$Efficiency = \frac{Useful power output}{Total power input} \tag{4.5}$$

in which, useful power output is the output voltage multiplied by the current delivered to the load, divided by the time interval. Total power input is the input voltage multiplied by the input current divided by the time interval.

Efficiency is the most affected of the metrics, in figure A.3 it can be seen how Efficiency varies as function of process for each combination of V_{DD} and temperature. Two relevant facts are observable: the effect of V_{DD} is dominant. For each V_{DD} there are three waves corresponding to the three temperatures tested. From this it can be seen that for each value of V_{DD} increasing the temperature affects negatively the efficiency for almost all process corners.

To better illustrate how V_{DD} affects efficiency figure A.4 was produced.

Naturally, since the output voltage is desired to be the same for any V_{DD}, increasing V_{DD} increases the input power if the input current remains the same. So, another important aspect to monitor is how the relation between average input and output currents (I_{in}/I_{out}) is affected. This can be seen in figure A.5. What can be observed from this result is that, actually, I_{in}/I_{out} increases with a higher value of V_{DD}.

Another important measure is output ripple voltage, whose variation as function of PVT corner can be seen in A.6. Ripple can be as high as 8.4%, which is not a large variation and no significant correlation was found between ripple and the occurrence of one single temperature, voltage or process condition.

In table 4.5 a summary of the circuit's performance is presented.

Table 4.5: Summary table.

	Vout		Ripple		Efficiency	
Temperature Values	Value	Corner	Value	Corner	Value	Corner
Max	1.2	25º, 0.88V, hv_fs, mos_fs	8.44%	-40º, 0.88V, hv_sf, mos_tt	76.7%	-40º, 0.72V, hv_sf, mos_tt
Min	1.192	-40º, 0.72V, hv_fs, mos_sf	7.02%	25º, 0.72V, hv_ss, mos_ff	21.7%	125, 0.88V, hv_ff, mos_ff

4.2.5 Maximum Rating

If a typical chip is produced, at 25º and $V_{DD} = 0.8$V, if I_o is swept even beyond the 20mA. The result can be observed in figure 4.13.

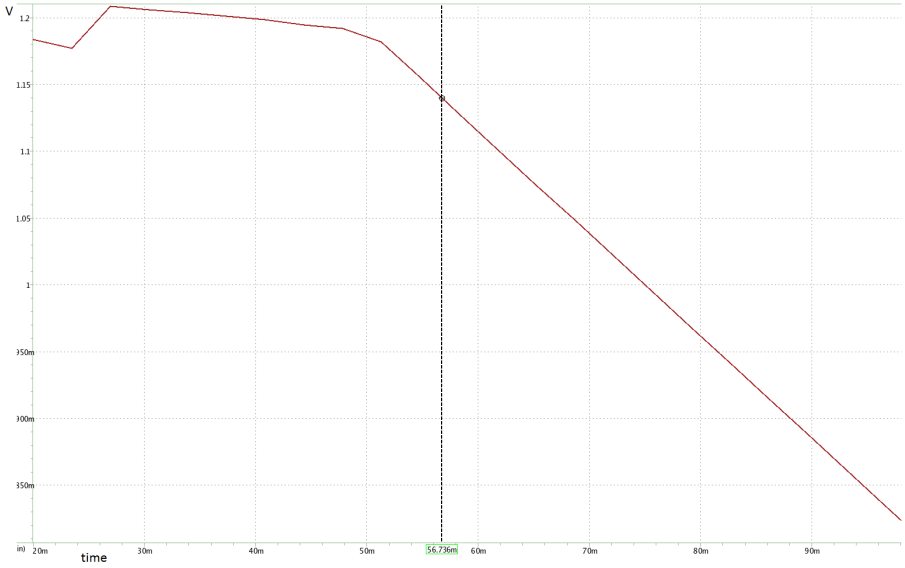

Figure 4.13: Sweep of Io for an input of 0.8V.

Only at $I_o = 56.7$mA, the average V_{out} fall to 95% of the nominal 1.2V, which is 1.14V.

Again, using a typical chip with 25º of temperature if it is supplying a 20mA current, and V_{DD} is varied beyond its limits, the average output voltages can be seen in figure.

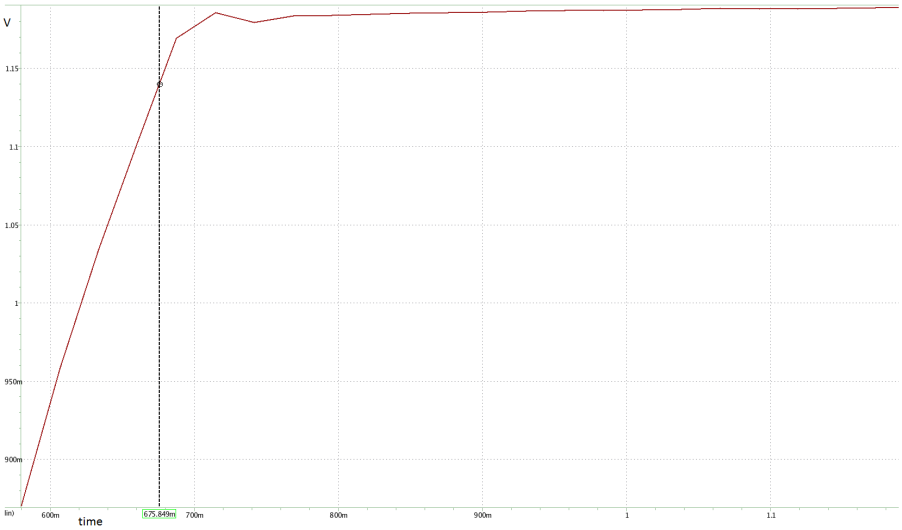

Figure 4.14: Sweep of V_{DD} for a load of 20mA.

For the lowest bound of acceptable V_{out}, 95% of 1.2V, the lowest complying V_{DD} is 676mV, beyond this the circuit output remains stable.

4.2.6 Monte Carlo

When a chip is being fabricated uniformities in manufacturing originate deviations in the device's parameters. Part of those uniformities affect from chip to chip in a wafer and so are referred as inter-die. Those were covered before, every time a process variation was assumed. But another type of uniformities that can occur is intra-die, affecting differently each part of the same chip (die). They are caused by spatial uninformities in the process and are also known as mismatch varations [19]. With more modern processes mismatch variations became even more important. Monte Carlo simulation allows the use of random variation in transistor's dimensions to emulate what can happen in real world fabrication and therefore observe how these variations affect the general functioning of the device.

These variations are particularly harmful for devices that depend on matching. This is not, for the most part, the case of the Charge Pump. If the NMOS switches' dimensions deviate from their optimal values, this can hurt the circuit's performance, but since what matters in charge transfers is the R_{on} resistance, small differences in dimension will only lead to small differences in the amount of charge transferred. The same is the case for the NMOS diodes used in the bi-level converters. The transistors that do the pull-up and pull-down of the switches' gates can be more affected since variations in dimensions of a PMOS will affect the pulling-down done by the NMOS and vice-versa.

It is thought that random variations in dimensions will note impact intensely the device's operation and to verify that claim a Monte Carlo simulation was ran comprising 24 corner cases with 100 instances of Monte Carlo per corner. Average output voltage was drawn and can be seen in figure 4.15.

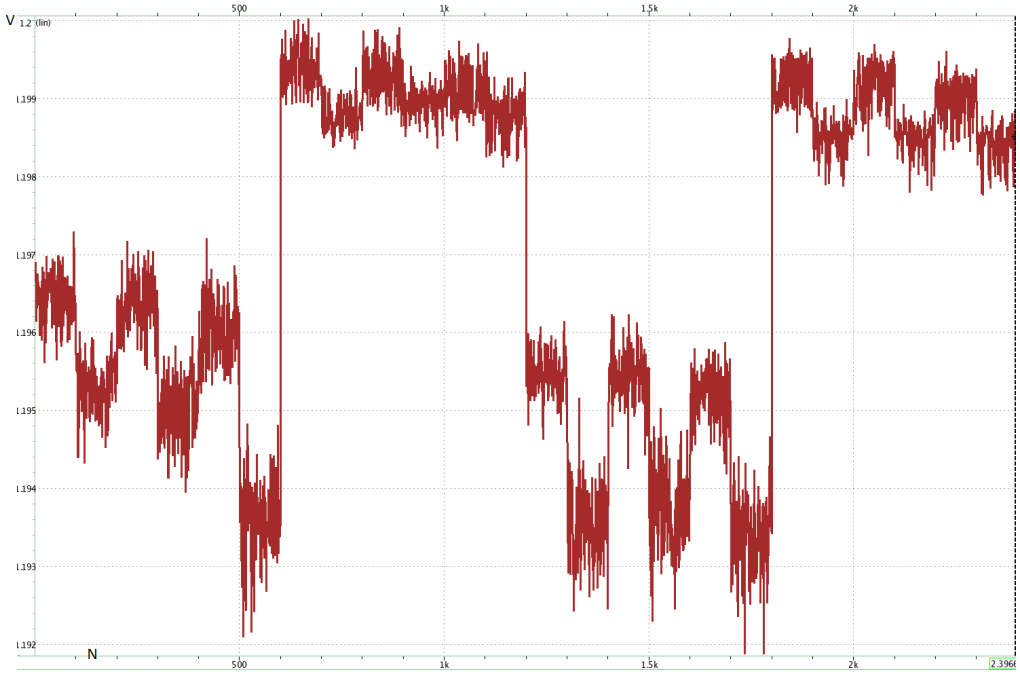

Figure 4.15: Average output voltage of 100 instances of Monte Carlo for 24 PVT corners.

As seen, the worst and best average output voltages are identical to those seen in the PVT corners without Monte Carlo. Corners are not specified because this image serves mainly to illustrate that there is no significant difference from the PVT simulation done before.

Also ripple voltage is presented in figure 4.16.

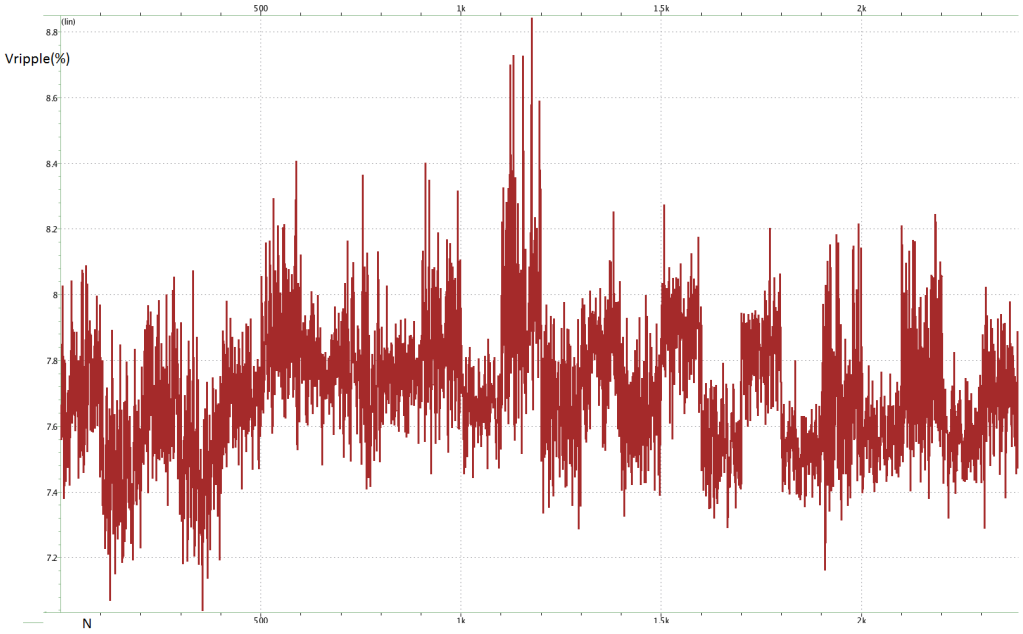

Figure 4.16: Ripple voltage of 100 instances of Monte Carlo for 24 PVT corners.

Again results are not significantly different from non-Monte Carlo simulations.

4.3 Summary

This Chapter presented the final solution proposed and results of simulations. First a typical case was presented, in which temperature was 25º, processes were typical and supply 0.8V, for this case average output voltage, ripple and efficiency were calculated. Then, line regulation was evaluated, both for the typical and then for all the PVT corner cases. Typical line regulation is 0.58% and in the worst case 1.42%. Subsequently load regulation was evaluated, in a similar way to line regulation. Being the typical case 3.58% and the worst case 3.92%. So the proposed circuit behaves well for the intervals of current and input voltage for which it was designed, namely 0.72V-0.88V and 0mA - 20mA. Since the previous simulations were about DC loads, and the circuit might supply loads with very different profiles, a special category of simulations were ran, denominated as irregular loads simulation. In this, the current drawn from the converter is a conjunction of various currents sources, namely sine, square, triangular and a resistor. Performance parameters were evaluated and the goals were met. The worst case of voltage ripple is 8.44%, and an average output voltage of 1.192V. Efficiency was the most affected parameter but in the best case can reach 76.7%. Also, the limits of the converter were tested and it was asserted that for typical conditions, the circuit can supply 56.7mA without the average output voltage falling more than 5% of

the aimed voltage. If the output current is 20mA and all other conditions typical, the circuit can operate with an input voltage of 676mV, without the averaged output voltage falling below 95% of 1.2V. Monte Carlo simulation, that involves introducing random parameter deviations between devices, was also introduced but no significant variation existed from previous performances, as expected.

Chapter 5

Conclusions and Future Work

In this chapter an itemized summary is presented of the work developed. Also, a goal achievement evaluation will be done. Finally a review on what can be done to improve this design further, is presented.

5.1 Work Development Summary

The objective of this work was to design a Charge Pump based on inductorless DC-DC converters, complying with a certain set of goals and robust to PVT and mismatch (Monte Carlo). In order to achieve this, the following was done:

- An introductory chapter was written, acting as a preview of the work. It was made clear what this work is devoted to, what was the motivation behind it and what problems were anticipated. Also a preview on the document's structure was given.

- A basic review on DC-DC converters was made. A more detailed study of existing Charge Pump topologies, was given in the beginning. This included the Cockcroft-Walton Charge Pump, the first known Charge Pump that laid ground for the following topologies. Then the Dickson Charge Pump was presented. The study of this topology was fundamental, mostly to understand more recent designs because many of them are strongly based on it. Wu's Dynamic CTS Charge Pump was then analysed. It inspired the bi-level converters that was vital for this work. Its principles were extrapolated to the other parts of the circuit. Lastly some more recent topologies were given the spotlight. Post-Wu work on this theme is very vast and details of the designs are of importance, mainly, when trying to achieve a certain set of goals. Those might have been high conversion ratio, alternating between step-up and step-down, high efficiency and other. These authors picked up the ideas until a certain point and adapted to their goals, which was what this work has also done. It is the understating of this work that no major breakthrough was done since Wu. Nonetheless modern topologies, more relevant to this work, were looked into and analysed.

- A core study of the Charge Pump operation was made and special attention was given to the topology eventually chosen. These included a detailed study of the two-phase operation, giving the relevant equations and higher level analysis.

- A general system block was given. Then, a complex and vital part, the bi-level converter, was looked upon with a rather detailed view. It was explained that this circuit was important to turn *off* and *on* switches. When designing a circuit that should alternate between two levels of voltage with a certain period, two parameters are very important: The average level of voltage and the difference between the low and the high level (this is the amplitude). The average level can be increased adding levels of pumping at the beginning of the circuit. These pre-levels also give the possibility of being turned *off* and therefore adapt to varying conditions of the circuit. For example, when the supply is high the pre-level are turned *off* to reach a certain level of voltage that avoids damaging the switch. When the supply is low, pre-levels are turned *on* to turn the switch *on* adequately. These is also valid to temperature and process since all of this is reflected on the levels of the bi-level converter. In this resides most of the PVT robustness.

- After the general parts were explained, it was exposed how the parameters of the circuit were decided. This was done mostly in light of area, since bi-level converters are made mostly of capacitors, that have to be integrated, and which are very impactful on area. The bottleneck when reducing the area is the R_{on} of switches. Since raising the bootstrapping of gates to increase the overdrive voltage of the transistor involves either adding more stages, or increasing the size of the capacitors. Using the deduced circuit equations it was possible to find that the bigger R_{on} that still allows circuit operation, and the rest of design parameters were obtained from this. The duration of the period is the sum of the duration of the two phases. The phase of discharge is given by the voltage that the output capacitor is allowed to fall at maximum load. The duration of the charge phases were found to be the value at which the maximum voltage, on the output capacitor, is reached.

- Since the circuit can supply various kinds of loads, with various kinds of magnitudes and also resist the variations of environmental conditions and process deviations that affect the output wave, a closed-loop controller is needed. When the load is low, in relation to the capability of the circuit, the output falls less than normal, so charge phases can be skipped, saving power. But still when conditions are above worst case the regular duration of the charge phase results in an increase above the desired . To correct this a comparator can be added and used to turn *off* the charge phase when the output reaches the desired level. This acts as a Pulse-Width-Modulation controller. A detailed exposure on this was made.

- The final aspect of the circuit is then given. Simulations to verify the compliance and evaluate parameters were ran.

5.2 Goal evaluation

As observed in the previous chapter, the ripple is limited between 7.4% and 8.4%, V_{out} is between 1.91V and 1.99V. And finally efficiency between 26% and 76%. Therefore the goals were achieved.

5.3 Future Work

The work that can be done upon this, is mostly steps in the direction of a final chip design. Before that, simulations on ageing can be drawn to evaluate the circuit behaviour when operating during years. This may identify some problems but it is expected to not be a source of many problems because the regulation that exists, intends on limiting the voltages applied. Not going above the maximum voltage of a specific transistor was a constant concern during this work and going above maximum voltages is the main cause of reduction in transistor's life time. The regulation part should be replaced by gate level logic. This can be done by synthesising the synthesizeable part of the RTL code, or implemented directly with transistor level design, since the algorithm is relatively simple. The comparison can be done by regular comparators since 2.5MHz is not a too high frequency. In the end the physical layout can be done. The circuit uses the bi-level converters that are similar between them, with some dimension adjustment, so the layout can use a modular approach.

Appendices

Appendix A

Appendix A

A.1 Results of Irregular Load Simulations

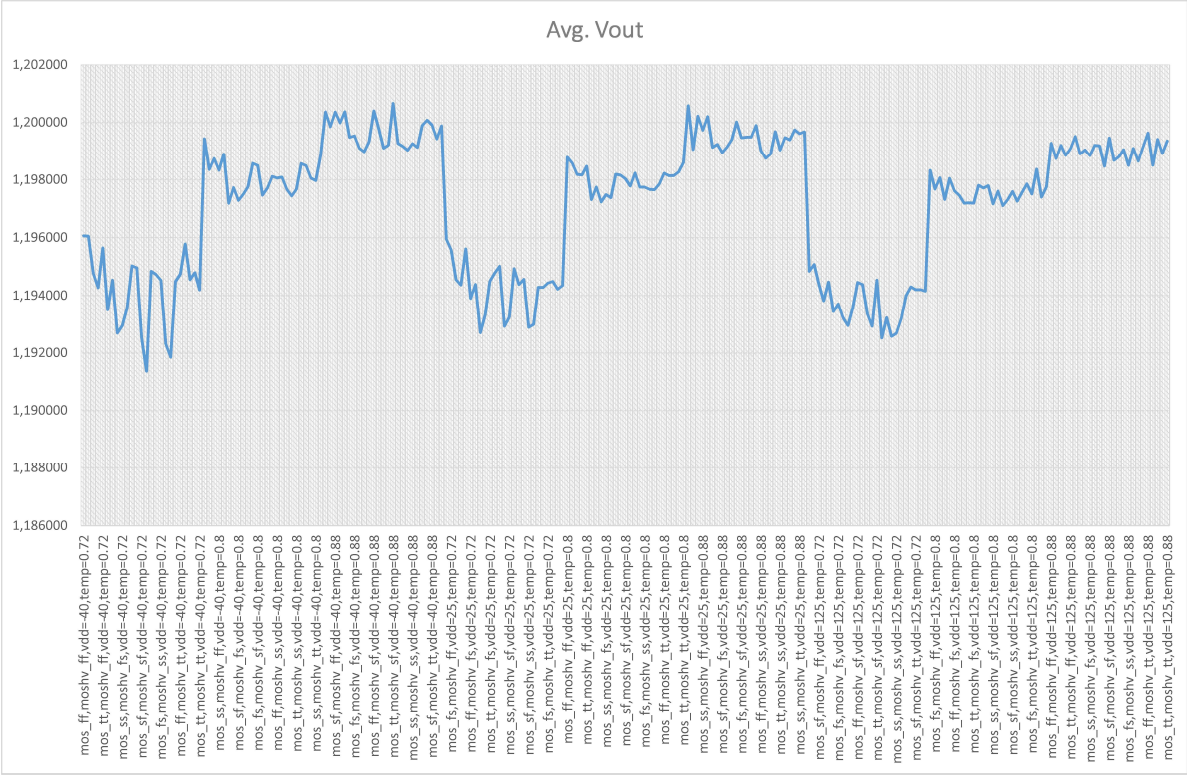

Figure A.1: This figure demonstrates the average V_{out} in function of temperature and process for the proposed converter supplying an irregular load.

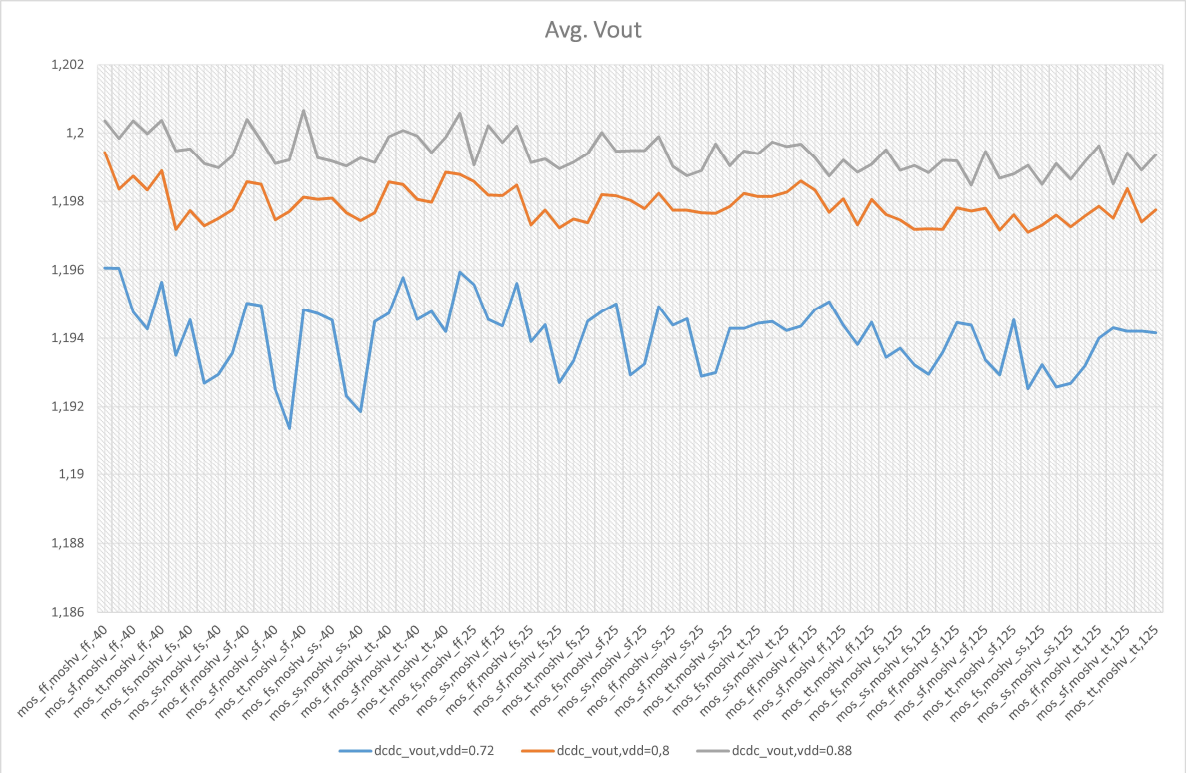

Figure A.2: This figure demonstrates the average V_{out} in function of temperature and process for the proposed converter supplying an irregular load for each value of V_{DD}.

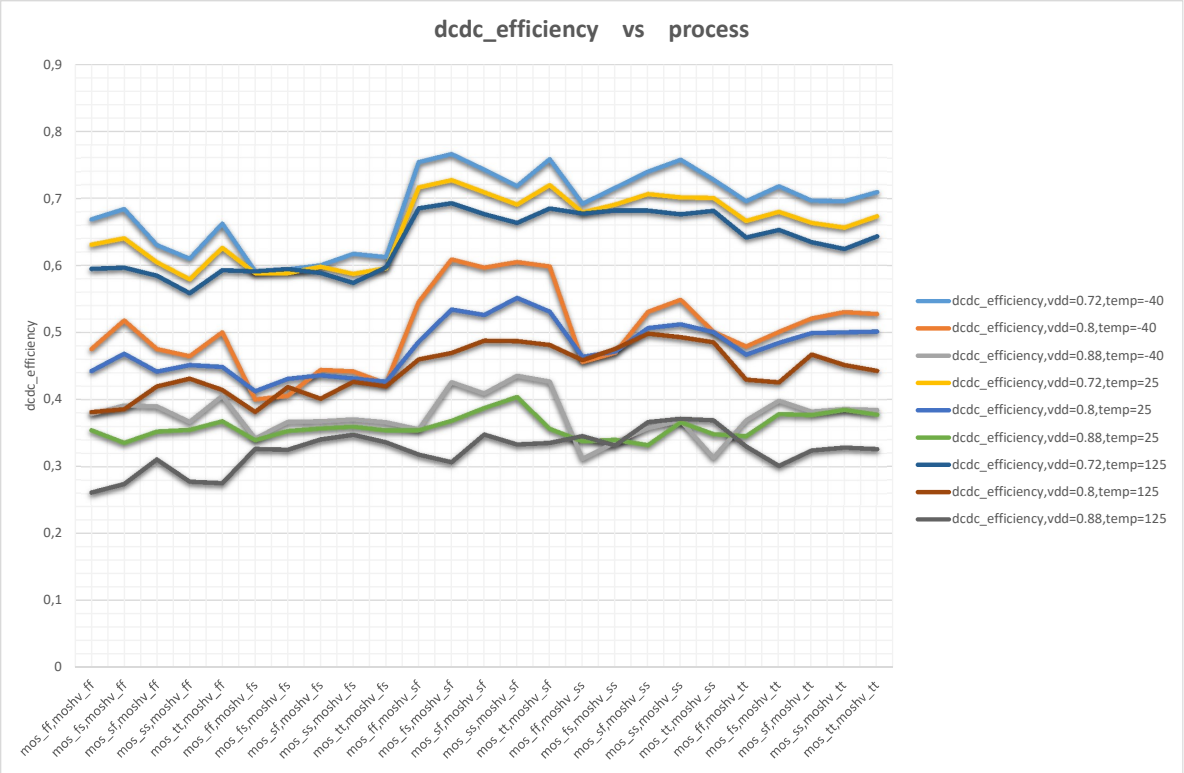

Figure A.3: This figure demonstrate how Efficiency varies in function of the process for each temperature and V_{DD}.

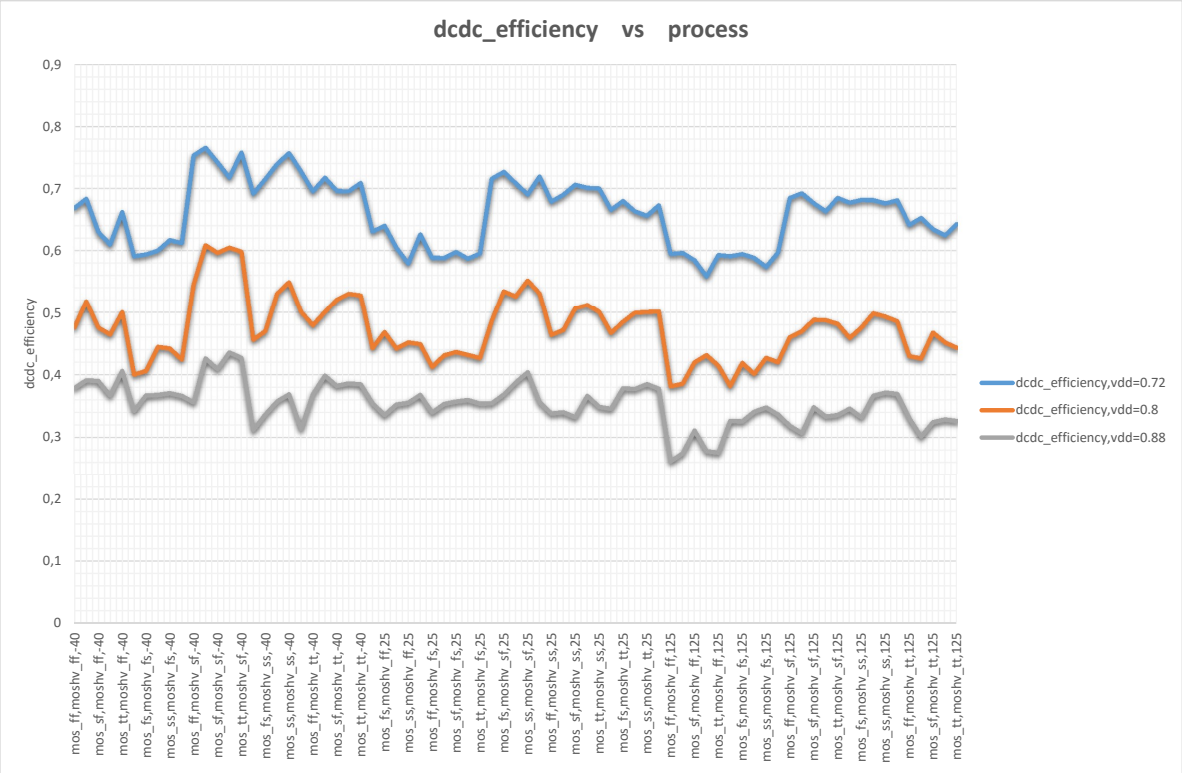

Figure A.4: This figure demonstrate how Efficiency varies in function of the process and temperature for each value of V_{DD}.

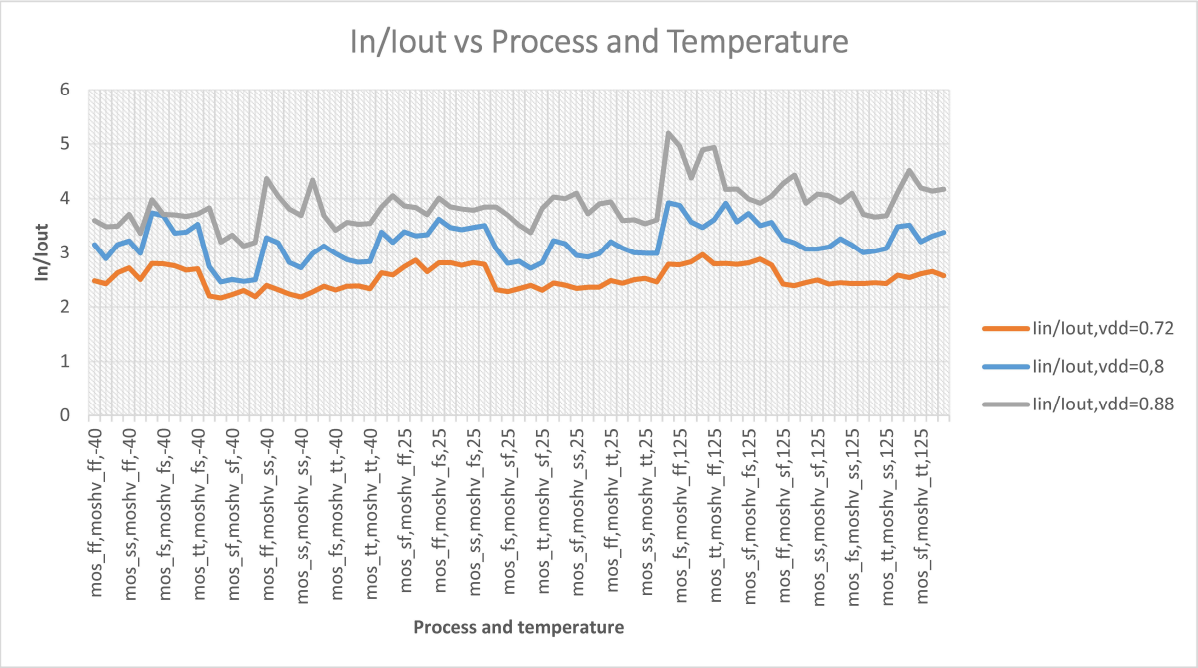

Figure A.5: This figure demonstrates how I_{in}/I_{out} varies in function of the process and temperature for each V_{DD}.

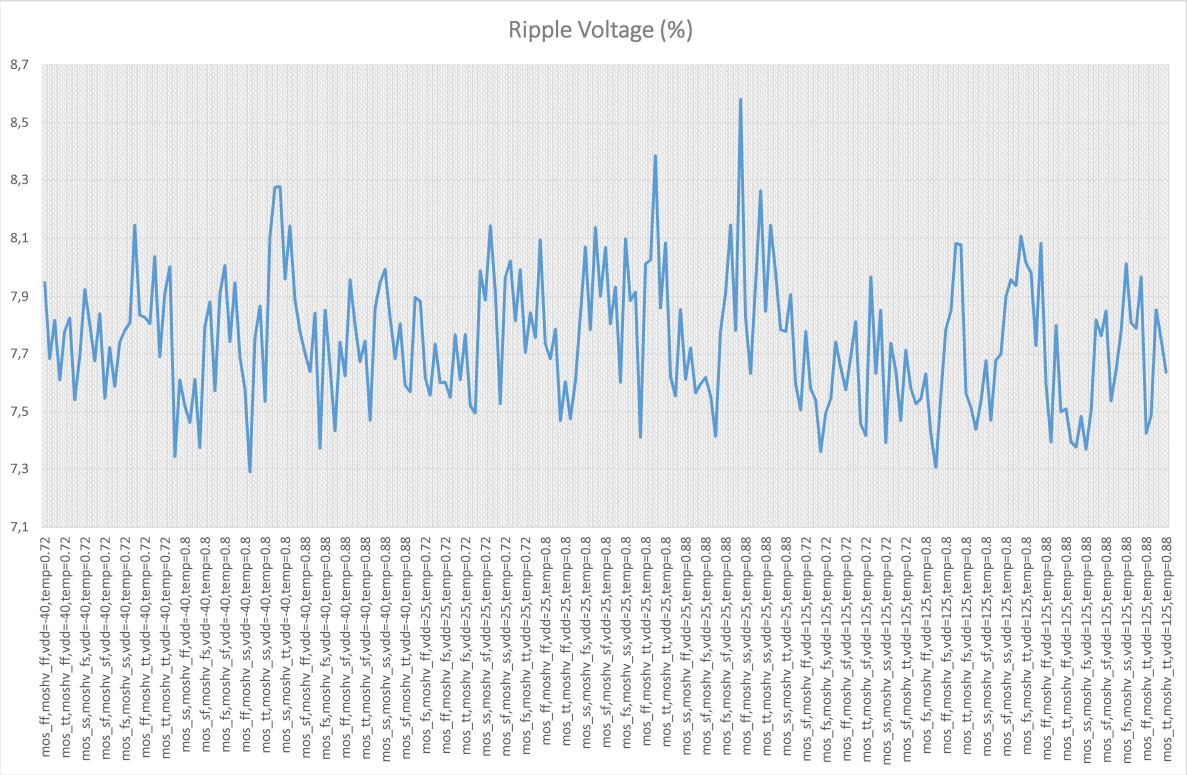

Figure A.6: This figure demonstrates how the output ripple, in percentage, varies in function of the process and temperature and V_{DD}.

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