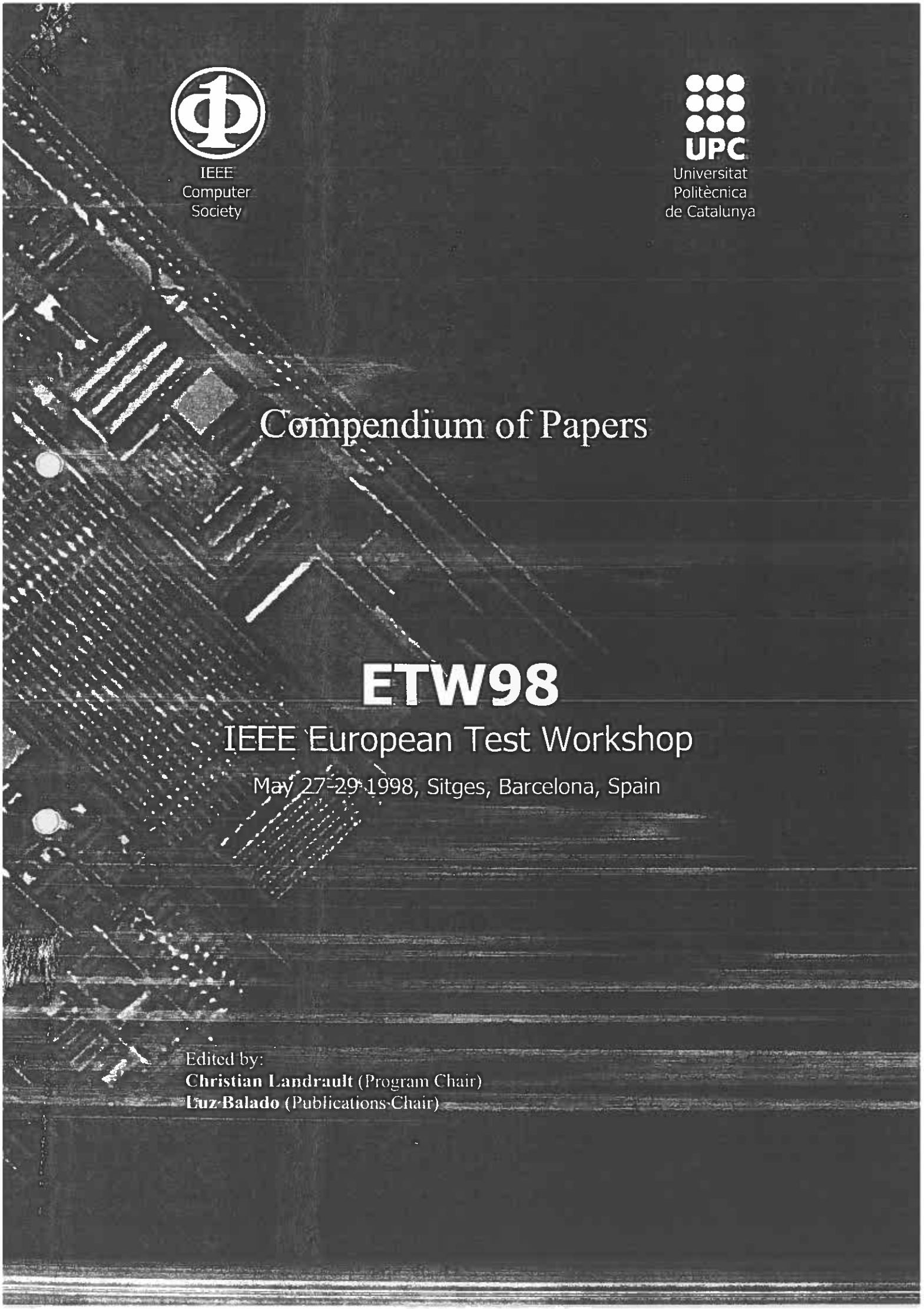
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On Improving BST for Concurrent Functional Verification

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Abstract:

An enhanced IEEE 1149.1 Boundary Scan Test infrastructure allows concurrent error detection, in a discrete way, with no impact on the mission circuit performance. Some drawbacks of the original solution are now improved.

Keywords: Functional Test, BST, DFT.

1. Introduction

An enhancement to the IEEE 1149.1 Boundary Scan (**BS**) Test (**BST**) std [1], aiming concurrent error detection, was introduced at the ETW'97 [2] and allows this infrastructure to provide a discrete functional verification, when supported by a BST controller. The overhead of this approach to the 1149.1 BST std is no more than 15%, with no changes in the Test Access Port (**TAP**), but has 2 main weakness: single pattern search and sequential designs. Now we present 2 improvements concerning these points:

1- the search *for multiple pattern combinations simultaneously,* without changing the BS cells and with a small overhead to the BS infrastructure. This multiple search, together with statistic analysis based on [3, 4], allows to predict much shorter fault latency times, meaning over an order of magnitude improvement, and may be shown compatible with typical requirements concerning test pattern number and latency delays in most Real-Time designs.

2- a step towards a more effective concurrent verification of sequential designs, based on a duplex architecture sharing a common BST infrastructure. Error confinement and the decision to disable the defective CUT, based on fault location, are decided at scan level, with enhanced BS cells.

The paper follows with a brief review of the original proposal (2), and an explanation of the design solutions developed (3, 4).

2. Background

The enhancement introduced at ETW'97 relies on the input and output group of Scan cells bounding the *mission circuit* or *circuit under test (CUT),* and an on-board BS-controller (**BSμC**). Such a kind of controller will be found in many designs to provide system-level BST interface [5]. It is not required for the CUT to work (properly) but the test patterns previously defined to verify the CUT may be stored in its internal 1-4KB ROM; they are the only thing CUT-dependent since the scan process needs no specific program.

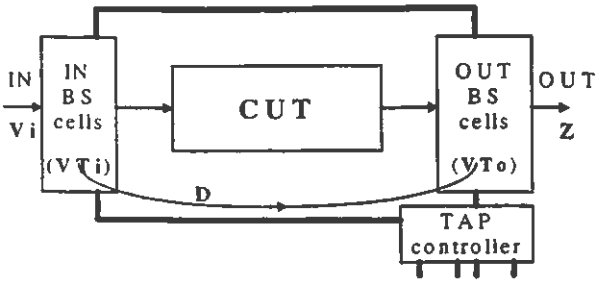

Fig.01- The CUT and IN-OUT BS cells

The BSμC scans the test patterns (VTi+VTo) continuously and the input group activates the **D** signal upon *detection* of an input match (Vi=VTi), triggering the out group to perform several functions: output capture, checking or output injection bypassing the CUT. The main advantages are:

- independence and transparency to the CUT.
- fully 1149.1 compliant; standard or observation-only simplified cells may be used.
- no impact on the CUT performance.
- no need to redesign the base CUT.
- minimal overhead: 10-15% to the std BST.
- two levels of fault detection available: pattern mismatch or a too low number of matches,
- ability to correct some output patterns (those stored in the ROM).

The main limitations of this solution are:

- single input pattern search, impacting fault latency,
- sequential designs, because a wider state space enlarges detection intervals.

3. Multiple Search

Since each input BS cell has a single latch available, the search may be single pattern only. To reduce the latency interval a multi-pattern search is desirable, but additional latches seem an unacceptable overhead, possibly 1149.1 std not compliant, and will impact BS cells *reliability*.

To solve this problem, without changing the std cells, a partition technique of the input BS group was developed to search multiple pattern combinations: 16 is typical but 32 and more combinations may be searched simultaneously. The deterministic test patterns defined to verify the CUT are top *fault coverage* (*fc*) patterns with a high path sensitisation capability; most combinations *covered* by them may also be expected to approach this rule. This way 16, 32 or more combinations of the loaded input test pattern (VTi) are searched simultaneously, half of them being effective to detect faults. We are trying to find possible relations to the other half of the pattern combinations.

This partition method applied to an ***n*** input CUT may convert asymptotically an $\mathbf{O(2^n)}$ search into an **O(n)** scan process and, besides, a small number of test patterns (and their combinations) may allow a high fc. The overhead to the infrastructure already described is about 5%, and then the multiple search hardware overhead will be within 18% to the std BST.

4. Sequential Designs

The general idea defined in [2] is also valid for sequential designs. However, a *N* input with *S* memory elements circuit has $2^{(N+S)}$ combinations to search: the wider state space increases the latency interval and the number of test patterns required also. In order to keep this number acceptable to be stored in ROM, and avoid wrong states to go into deep degradation (if the latency delay is high), a duplex architecture seems to be the best approach if *common mode faults* may not be considered in the fault model.

This 2-CUT architecture shares a single BST chain, with common input *detection* and output *decision* groups. To allow this feature the output BS cells are redesigned to receive both CUT outputs (A, B), and deal with the content of one *std* latch (C), to be considered when the detection (D) signal is active only.

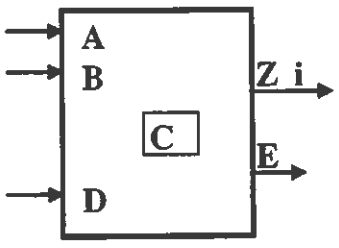

Fig 02. the output decision cell

The enhanced cell has two functions:

- *Comparison* between CUT outputs (A, B); this feature is always working until a mismatch occurs.
- *Voting* among A, B and the cell latch C; this is allowed when an input match (D) occurs only, meaning that C content must match the CUT outputs.

CUT mismatch disables momentarily the outputs (**Zi**), which is translated as a known state, or the previous (correct) output is maintained. The Error signal is also set to disable all the output bits. Meanwhile both CUT continue working until fault location allows to resume operation based on the fault-free CUT. CUT partition may reduce the latency interval, which can be statistically predicted but not guaranteed.

Conclusions

Multiple pattern combination search may allow a high matching rate and fast detection. The enhanced decision BS cells mean an overhead near 50% to the std cell, and are fully 1149.1 compliant with no changes in the TAP controller, allowing the test patterns to be reused with a very small cost.

Intended mainly for VLSI ICs and valuable for most fault models, excluding common mode faults (yet some of them can be detected), this design solution is aimed as an intermediate option for *critical but not life critical* systems, with a cost hoped to be lower than self-checking designs [6,7,8], since a BS-controller (8 mandatory pins) may support several CUT ICs.

Selected Papers

1- *IEEE Standard 1149.1 Test Access Port and Boundary-Scan Architecture*, IEEE Inc, NY, 1991

2- J.M.V. Santos, J.M.M. Ferreira, " POST: Pseudo On-Line BS Failure Detection", *ETW'97 compendium of papers*, Poster Session 3, Cagliary, Italy, May 1997.

3- V.D. Agrawal, "An Information Theoretic Approach to Digital Testing", *IEEE Trans. on Computers*, vol. c-30, pp. 582-587, August 1981.

4- D. Wagner and T. W. Williams, "Enhancing Board Functional Self-Test by Concurrent Sampling", *IEEE ITC 1991*, pp. 633-40.

5- *Texas Instruments IEEE 1149.1 Testability Primer*, 1994, SSYA002B, http://www.ti.com/sc/docs/jtag/jtag2.htm.

6- M. Nicolaidis, "A Unified Built-In-Self-Test Scheme: UBIST", *IEEE FTCS'18 D. of Papers*, pp.157-63, 1988.

7- M. Lubaszewski, B. Courtois, "On the design of Self-Checking Boundary Scannable Boards", *Proc. of ITC*, 1992, IEEE, pp.372-81.

8- E. Bohl, R. Stephan, W. Glauert, "The Architecture of the Fail-Stop Controller AE11", *IEEE IOLTW'97, Crete*, pp. 47-52, 1997.