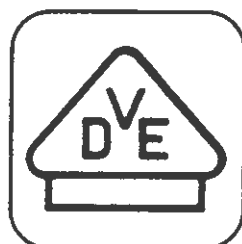


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A new algorithm for diagnosing interconnect faults on Boundary Scan boards

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Introduction

Following a comparative study of test pattern generation (TPG) algorithms for boundary scan boards, an adaptive TPG algorithm is proposed, fulfilling the requirements of different testing scenarios.

Response ambiguity

Response ambiguity (occurrence of aliasing and confounding syndromes [Jarw89]) is related to the number of '0' bits existing in the set of assigned STVs (and-shorts assumed). This is because the number of '0' bits existing in the SRV of a set of shorted nets will be greater or equal than the number of '0' bits in any of their STVs.

A step which may be taken to minimize the number of SRVs requiring further clarification is to assign in first place those STVs with a smaller number of '0' bits. The minimum weight algorithm [Yau89] adopts this heuristic, and a similar approach is also used in the maximum independence algorithm [Yau89]. Having the same number of '0' bits in every STV (such that any faulty SRV will not alias to an assigned STV) [Wagn87] [Chen90] is an alternative approach, but it does not lead to a globally more efficient solution.

A representative cost function for quantifying potential response ambiguity consists of the ratio of the number of possible short faults with a non-unique SRV, to the number of non-unique SRVs. This is shown in fig.1 on the basis of a normalized cost, where the base cost corresponds to the value of the ratio described, for the binary search algorithm [Kaut74]. For each value of N (number of nets), this cost was determined by simulating the $(2^N - (N+1))$ possible short faults.

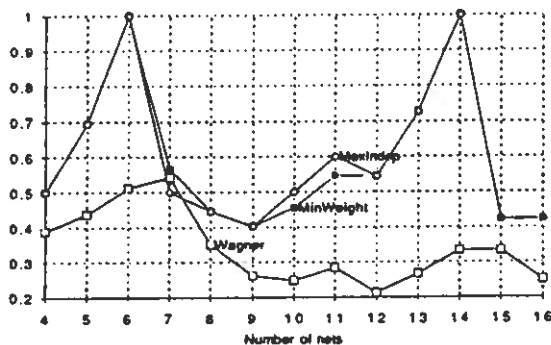


Fig.1: Normalized cost for various TPG algorithms.

The cost function for the walking sequence algorithm [Hass88] is zero, since each possible short fault has a unique SRV. However, this takes place in exchange for a very large number of TPs, leading to long application times. In spite of the low cost figures shown in fig.1, the Wagner algorithm [Wagn87] uses twice the number of TPs required by the other algorithms. If the same number of TPs were allowed for the minimum weight, the maximum independence, and the Wagner algorithms, comparison of their cost figures would show significantly lower values for the first two.

A new TPG algorithm

The various testing scenarios that may be found share a common requirement for a set of TPs with complete fault detection, and fast application time. Additionally, further tests may have to be performed if the board is to be repaired. A natural choice fulfilling all these requirements consists of an adaptive algorithm, using a first set of TPs with minimum application time and complete fault detection capability. A second set of TPs is then available as an option to enhance diagnosis, if required.

Both the Goel and McMahon [Goel82] and the optimal C-test [Jarw89] adaptive algorithms perform a binary search for faults in the first step. An optional second step, based on a walking sequence, enables unambiguous fault location. The difference between these two algorithms resides only on the set of nets over which this walking sequence is to be generated, and illustrates the tradeoff present in the second step: the need to find a balance between the complexity of TPG, and the number of TPs generated. This balance may be achieved by skipping any search among those nets with a common SRV (the identification of aliasing or confounding syndromes will not be performed). A set of three or more nets sharing a common SRV may or may not contain puzzling (aliasing or confounding) syndromes, and will be termed an *Eventually Puzzling Syndrome* (EPS).

An adaptive algorithm using the concept of EPSs, and employing a first set of TPs with minimum size, and complete fault detection capability, may now be specified as follows:

- The first step uses the minimum weight TPG procedure, and assigns to each net an STV with $\text{ceil}[\log_2(N+2)]$ bits.
- The second step generates a walking sequence over the nets sharing a common EPS. Since all EPSs are solved in parallel, the number of TPs generated is given by the maximum number of nets present in any EPS.

The procedure proposed for the second step would normally generate an intermediate number of TPs, when compared to the Goel and McMahon or the optimal C-test algorithms. However, and since a lower ambiguity-cost procedure is used in the first step, the number of TPs generated in the second step may actually be lower (or even not necessary).

References

- [Chen90] Cheng, Lewandowski, Wu, 21st ITC, 1990
Diagnosis for wiring interconnects
[Goel82] Goel, McMahon, 13th ITC, 1982
Electronic chip-in-place test
[Hass88] Hassan, Rajski, Agarwal, 19th ITC, 1988
Testing and diagnosis of interconnects using boundary scan architecture
[Jarw89] Jarwala, Yau, 20th ITC, 1989
A new framework for analyzing test generation and diagnosis algorithms for wiring interconnects
[Kaut74] Kautz, IEEE Trans. Computers, April 1974
Testing for faults in wiring networks
[Wagn87] Wagner, 18th ITC, 1987
Interconnect testing with boundary scan
[Yau89] Yau, Jarwala, 20th ITC, 1989
A unified theory for designing optimal test generation and diagnosis algorithms for board interconnects

A New Algorithm for Diagnosing Interconnect Faults on Boundary Scan Boards

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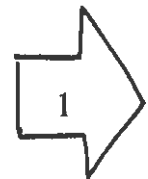
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Abstract

The general characteristics of known TPG algorithms for board level interconnect testing are summarized, and their potential response ambiguity is discussed on the basis of a common cost function. It is shown that an adaptive (two-step) algorithm provides complete diagnostic capability with a minimum number of test patterns, and an algorithm is proposed which allies a minimum ambiguity first step, with a reduced analysis second step.

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General characteristics of board level TPG algorithms - I

Algorithm	Binary search [Kaut74]	Wagner [Wagn87]	Walk. sequence [Hass88]	Min. Weight [Yau89]	Max. Indep. [Yau89]	Self Diagnosis [Chen90]	Global Diagn. [Chen90]
Num. TPs (p)	$\lceil \log_2(N+2) \rceil$	$2^{\lceil \log_2(N+2) \rceil}$	N	p Note 1	$p=f(E,N)$ Note 2	Minimum p for which $N \leq \binom{p}{p/2}$ is verified.	Minimum p for which $N \leq 2 + \sum_{i=1}^p \binom{i}{i/2}$ is verified.
Applic. time Note 3	9 ms	18 ms	500 ms	p ms	24 ms Note 4	12 ms	11 ms
Diagnosis	Poor. Aliasing and confounding may occur.	Poor. Only confounding may occur.	Complete.	Poor. Better for large values of p.	Complete.	Aliasing is eliminated. SRVs will always differ from STVs.	Aliasing is eliminated.
Comments	Minimum number of TPs generated.	Small number of TPs generated.	Too many TPs generated.	Vector assignment to nets aims to minimize aliasing and confounding.	Additional information (PCB layout, process characteristics) required.	All STVs have the same number of zeros, meaning that faulty nets will never have fault free SRVs.	Faulty nets may have fault free SRVs.

Note 1: p is specified by the user.

Note 2: p is given as a function of the maximum short extent (E) and the number of nets (N).

Note 3: Approximate values, assuming a circuit with 500 nets, 1000 BS cells, and a 1 MHz TCK.

Note 4: Assuming a circuit with 1000 BS cells, and a maximum short extent (E) of 20.

$\lceil \log_2(N+2) \rceil$ represents the first integer not smaller than $\log_2(N+2)$



General characteristics of board level TPG algorithms - II

	Binary search	Wagner	Hassan	Min. Weight	Max. Indep.*	Self Diagnosis	Global Diagn.
n1	0001	00001111	011111111111	0111	0111	000111	11111
n2	0010	00011110	101111111111	1011	1011	001011	01111
n3	0011	00101101	110111111111	1101	1101	001101	10111
n4	0100	00111100	111011111111	1110	1110	001110	01011
n5	0101	01001011	111101111111	0011	0011	010011	10011
n6	0110	01011010	111110111111	0101	1001	010101	01101
n7	0111	01101001	111111011111	0110	1100	010110	10101
n8	1000	01111000	111111101111	1001	0101	011001	11001
n9	1001	10000111	111111110111	1010	1010	011010	00110
n10	1010	10010110	111111111011	1100	0001	011100	01010
n11	1011	10100101	111111111101	0001	1000	100011	01100
n12	1100	10110100	111111111110	0010	0110	100101	10010

*

The TPG procedure of the Maximum Independence ~~was used~~ algorithm was used (considering that no additional information was available) to generate the maximum number of $\lceil \log_2(N+1) \rceil$ TIS.

Diagnosis capability

Diagnostic ambiguity may be described on the basis of aliasing and confounding syndromes [Jarw89]:

net	Applied	Responses
n1	0001	0001
n2	0010	0010
n3	0011	0001 <
n4	0100	0100
n5	0101	0100 <
n6	0110	0100 <
n7	0111	0100 <
n8	1000	1000
n9	1001	0001 <
n10	1010	1010
n11	1011	1011
n12	1100	1100

" < " indicate faulty SRVs.

Aliasing: Is net n1 shorted to nets n3 and n9?

Confounding: Are (n4,n7) and (n5,n6) two independent shorts?

A cost function for the potential diagnosis ambiguity of TPG algorithms

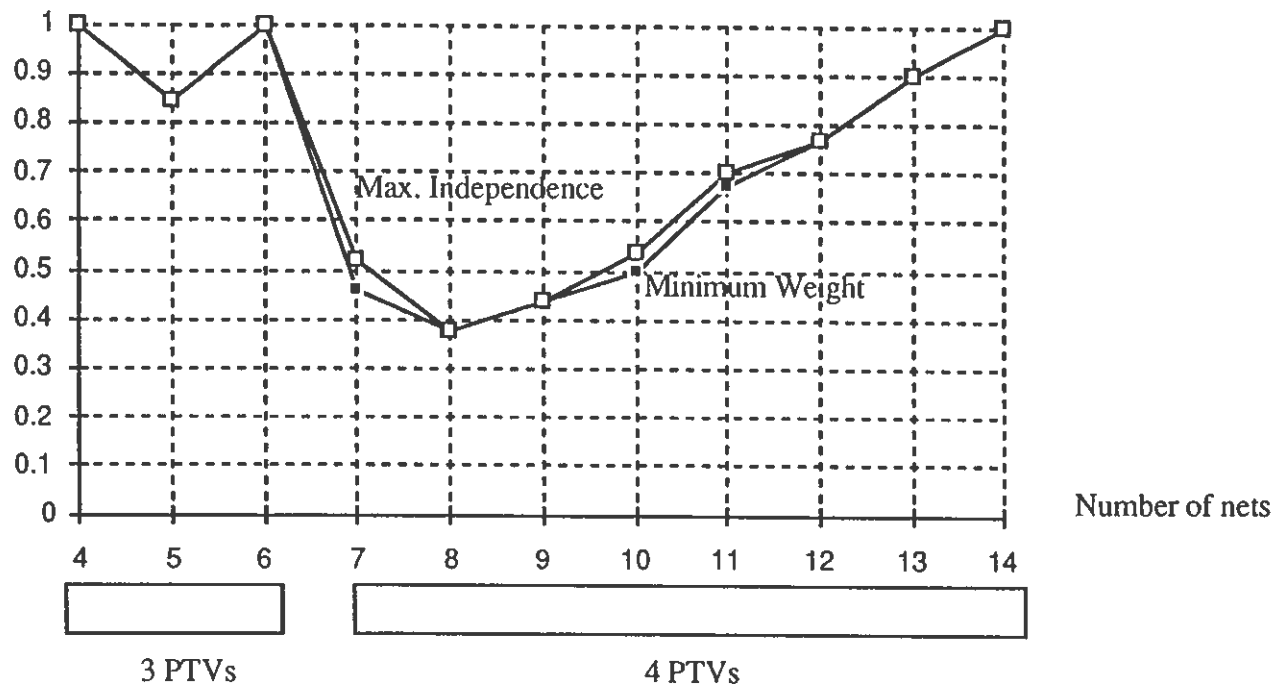
Ambiguity occurs when a set of faulty nets with a common SRV may be partitioned in any number of disjoint subsets, each characterized by the same original SRV. Moreover, the larger the number of such sets with the same SRV, the worse.

A cost function was determined by a simulation program which computes the SRV of each possible short fault. Disjoint short faults with the same SRV are flagged, and the number of occurrences for each case is found. The cost function is defined by the expression:

$$\frac{\text{number of disjoint short faults} \sum_{i=1} \text{disjoint_short_faults}[i].\text{number_of_occurrences}}{\text{number of disjoint short faults}}$$

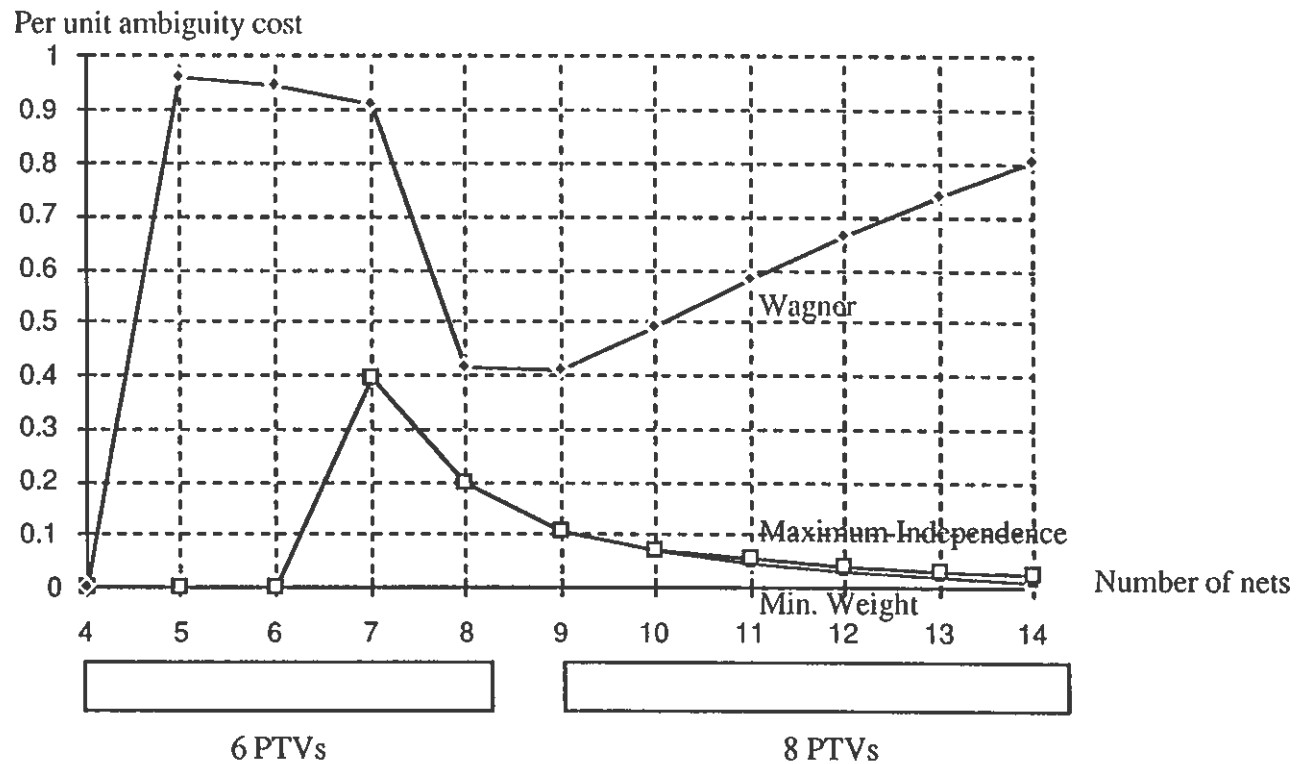
A per unit cost function is computed, by referring these values to those found for the binary search TPG algorithm.

Per unit ambiguity cost



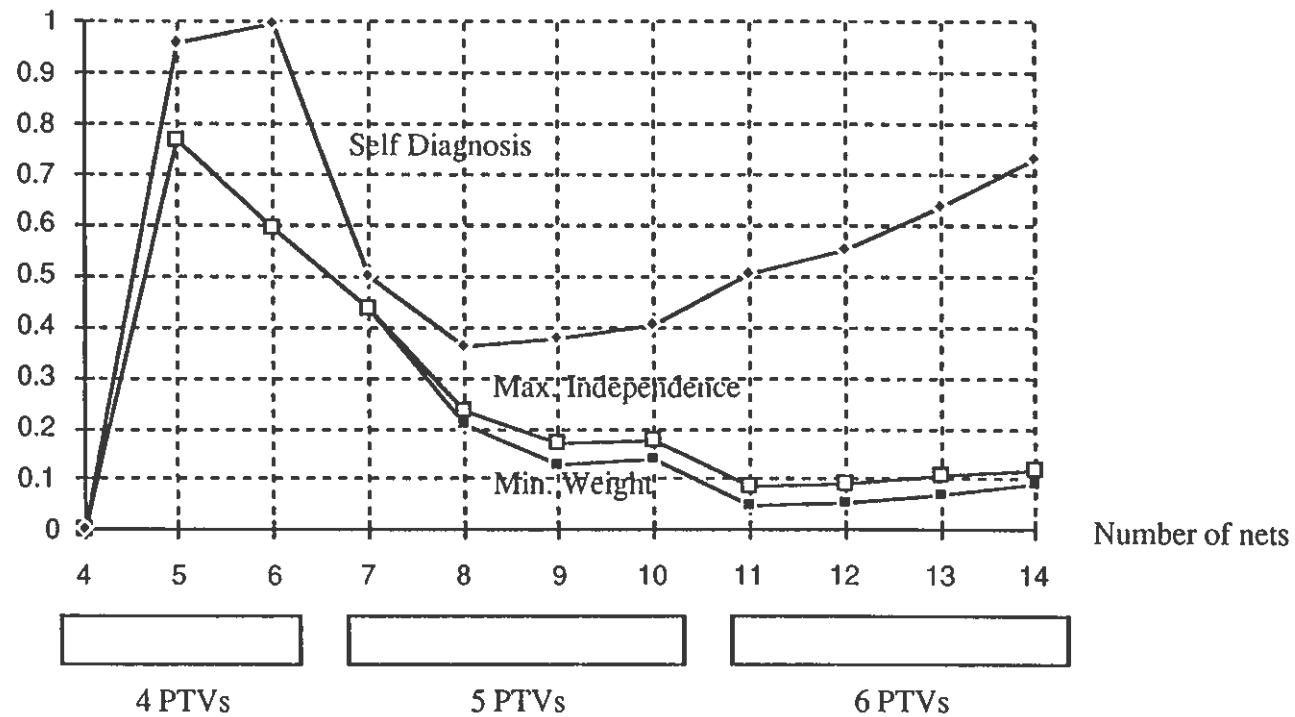
Except when every STV has to be used ($\log(N+2) = \text{ceil}[\log_2(N+2)]$), the Minimum Weight and the Maximum Independence algorithms will exhibit a better diagnostic accuracy.

$$\text{ceil}[\log_2(N+2)] = \lceil \log_2(N+2) \rceil$$



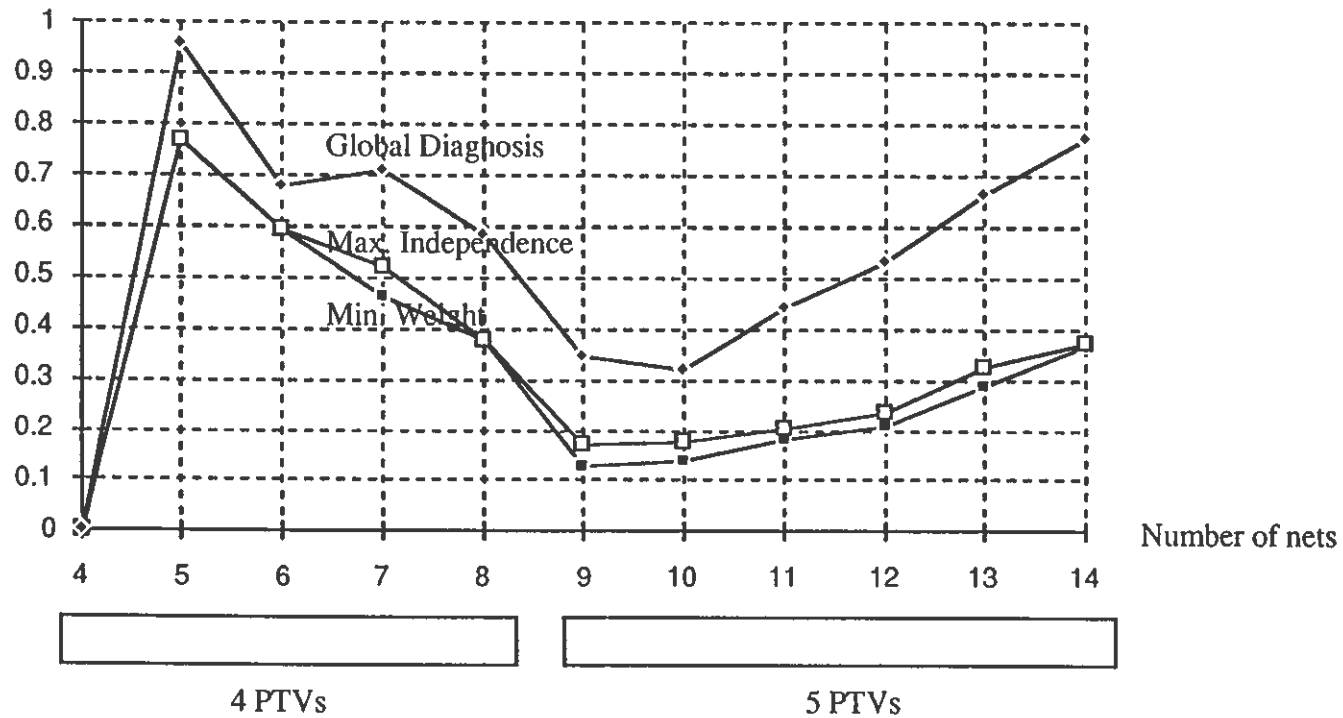
When the number of TPs used is the same as in Wagner, the Minimum Weight and the Maximum Independence algorithms will exhibit a better diagnostic accuracy.

Per unit ambiguity cost



The Self Diagnosis algorithm eliminates the occurrence of aliasing syndromes (SRVs will always differ from STVs), but the overall diagnostic accuracy is worse (confounding syndromes are not avoided).

Per unit ambiguity cost



The Global Diagnosis algorithm eliminates the occurrence of aliasing syndromes, but the overall diagnostic accuracy is worse (confounding syndromes are not avoided).

Adaptive TPG algorithms: second step TPG procedures

When a second set of TPs may be applied, complete diagnostic capability with a reduced number of TPs becomes possible. Analysis of the first step SRVs provides the input to the TPG procedure used in the second step.

The second step TPG procedures of known TPG algorithms [Goel82] [Jarw89] [Chen90] range from very simple analysis of SRVs, non-optimized number of TPs [Goel82], to very complex analysis of SRVs, leading to the minimum number of TPs [Jarw89].

A compromise may be found by performing only a limited analysis on the set of SRVs. When three or more common SRVs are found, aliasing or confounding syndromes may be present. But complexity is kept low by avoiding any further analysis, and simply considering this set as an *Eventually Puzzling Syndrome (EPS)*.

The concept of EPSs as a simplifying alternative

EPSs may or may not contain aliasing or confounding syndromes, but the task of determining the minimum number of TPs required to solve them [Jarw89] is a very complex problem. The straightforward solution of a walking sequence over each EPS will generate a slightly larger number of TPs, but at a much lower price.

EPSs do not share faulty nets, which means that all EPSs may be solved independently, and simultaneously. In other words, a number of TPs equal to the maximum number of nets in any EPS is sufficient for complete diagnosis, and there is no need for one TP per faulty net [Goel82].

Proposal of an adaptive algorithm

An adaptive algorithm with minimum ambiguity first step, and reduced analysis second step, may therefore be specified as follows:

- The Minimum Weight TPG procedure is used in the first step, generating a minimum number ($\text{ceil}[\log_2(N+2)]$) of TPs, with the lowest ambiguity cost.
- A walking sequence over each EPS will be conducted on the second step, providing complete diagnostic capability. Since all EPSs are solved simultaneously, the number of TPs will be given by the maximum number of nets in each EPS.

While the approach used in the second step would normally lead to an intermediate number of TPs (when compared with [Goel82] and [Jarw89]), the use of a minimum ambiguity TPG procedure in the first step may actually lead to a globally better solution.

References

- [Chen90] W. Cheng, J. Lewandowski, E. Wu
Diagnosis for wiring interconnects
Proceedings of the 21st ITC, 1990, pp.565-571
- [Goel82] P. Goel, M. McMahon
Electronic chip-in-place test
Proceedings of the 13th ITC, 1982, pp.83-90
- [Hass88] A. Hassan, J. Rajski, V. Agarwal
Testing and diagnosis of interconnects using boundary scan architecture
Proceedings of the 19th ITC, 1988, pp.126-137
- [Jarw89] N. Jarwala, C. Yau
A new framework for analyzing test generation and diagnosis algorithms for wiring interconnects
Proceedings of the 20th ITC, 1989, pp.63-70
- [Kaut74] W. Kautz
Testing for faults in wiring networks
IEEE Transactions on Computers, Vol.C-23, N°4, April 1974, pp.358-363
August 1989, pp.18-30
- [Wagn87] P. Wagner
Interconnect testing with boundary scan
Proceedings of the 18th ITC, 1987, pp.52-57
- [Yau89] C. Yau, N. Jarwala
A unified theory for designing optimal test generation and diagnosis algorithms for board interconnects
Proceedings of the 20th ITC, 1989, pp.71-77