The **POST** Approach to On-line Failure Detection Based on BST

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**Abstract:**  
An enhanced BST infrastructure, fully IEEE 1149.1 std compatible, enables on-line detection of pre-defined circuit conditions, opening the way to real-time monitoring Fault-Tolerant designs. A restricted Fault-Tolerance capability is also possible, with POST ability to inject a set of corrected output values.  
**Keywords:** On-line Test, BST, Fault-Tolerance, DFT.

1. **Introduction**

The Boundary Scan Test (BST) technology was defined in the IEEE 1149.1 std [1], and is now widely accepted for Off-Line (OFL) tests. ASIC libraries and CAD tools give to design and test engineers a quick path to this powerful infrastructure, and many ICs are available with BST.

In Fault-Tolerant (FT) systems [2,3,4] reliability is the prime concern. These "systems with the ability to survive to faults" [5], (are built to) exhibit a high capability to hide many types of failure modes, and therefore require additional testability solutions. As the BST infrastructure will be present in an increasing number of circuits for structural tests, it may be expected to help improve failure detection during circuit operation. However having an OFL nature, the BST structure is really inefficient in On-Line (ONL) operation, and solutions providing BST-to-system logic synchronisation are required. An additional reason to recommend enhancements in the BST infrastructure, if significant benefits are within sight, is that pin-limited ICs predominate over core limited ICs.

The solution proposed POST (Pseudo On-line Scan-based failure detection) is a partial design diversity approach to FT, involving:

a) an enhancement to the BST infrastructure allowing expected conditions to be detected without disturbing normal system operation;

b) a technique to verify ONL In-Out circuit relations;  

c) Ability to inject some corrected outputs; POST may, alone, extend the FT concept to low cost designs.

The paper follows with a background review (2), POST presentation (3) and failure detection analysis (4). Fault-Tolerance features (5) and final remarks (6) conclude it.

2. **Background**

The two major traditional FT architectures, Static and Dynamic, usually assume single fault models [6,7,8]. Static or Masking FT is widely based upon Triple Modular Redundant with Voting (TMR) architectures or on Error Correcting Codes (ECC), and the errors are masked with the help of the redundant information. Fault detection is unnecessary in these schemes, but to avoid fault latency the circuits must be (periodically) checked.

In Dynamic or Reconfiguration schemes, one of the spare replicated Hardware (HW) Functional Blocks (FB) available, replaces the active FB if it fails. Fault detection is necessary here, continuously or at "reasonable" time intervals, according to the error confinement delay acceptable in the application.

Additional detection problems still arise from the fault type, which may be permanent or temporary, and in this case intermittent or transient. Transient faults are usually the most difficult type to detect.

Most practical FT approaches presently available still have some problems. TMR and Fail-Safe circuits, with no error detection, become weak in VLSI, where production defects are usually multiple and common mode failures in replicated structures have a high probability of simultaneous occurrence. Self-Checking circuits need coding techniques and Checkers, meaning that the base system has to be redesigned. A time interval to allow all the input vectors to be exercised, is also supposed to that faults may be safely detected.

Previous work relating BST applied to failure detection areas, to our knowledge, can be summarised as follows: a proprietary solution to automatic event detection and capturing in a BST environment referred by Whetzel [9], addresses off-chip implementation and different objectives, therefore leading to higher cost in terms of PCB area and to larger design cycles. Its usefulness for ONL failure detection is also handicapped by the triggering and capture methods, mainly directed for debug or stop-and-go modes. A concurrent testing technique in a BST environment was proposed by Salaja [10], but not 1149.1 compliant and depending on the completion of the test (a real handicap); internal test vector storage makes the solution potentially dependent on production and common mode defects.
The FiBS technique proposed by Chau [11] allows BST based fault injection, providing independent @ (stack-able) and s-open pin control, but ONL synchronisation is however not supported, which greatly restricts the usefulness of this approach for practical FT purposes. BUBST for Self-Checking boards, using BST for OFL detection of simple faults and concurrent checker analysis was also introduced recently by Lubaszewski and Courtois [12], simplifying coding requirements but is not 1149.1 compliant.

The most recent designs using BST for ONL failure detection assume modules with (two) replicated circuits, one of them being disconnected and tested OFL, while the other does its job. Problems to disconnect and synchronize both circuits make the solution not compatible with the 1149.1 std [13]; other solution uses replicated ASICS exchanging checked information between them, which requires additional lines, has synchronisation problems and provides no protection against common mode defects [14].

3. POST: A General View
3.1 Definitions and Terminology
Fault-Tolerance always means additional cost because some redundancy is necessary, and an on-board dedicated BST-controller (BSuC) may therefore be considered, such as the one presented in [15]. It is a dedicated ASIC (2000 gates and 28 pins) with 16 TMS lines, allowing independent BST TAP access and faster scan solutions compared to a single BST chain. TCK may be any submultiple of the BSuC CLK, and TCK ≤ CLK ≤ 33MHz. This CLK and the system clock may be equal or different. Providing independence of the main circuit and fast scan operations in ONL conditions, it may additionally perform OFL tests during power-up or when required.

Four basic levels are considered in our methodology, beginning with the circuit, designed according to the specification and optimised. Then:

FB- Functional Blocks are identified by testability or functional criteria, to be BS/POST (almost) completely testable. A FB may be one (or more) integrated circuit (IC), and multiple-FB ICs are possible using internal scan chains. In practice some FB I/Os may be not relevant for a given FT problem, and this is exploited to achieve speed improvements.

CHAIN- the testable circuit, with FBs in series, parallel or interleaved. Clusters in the Chain may be tested off-line and as referred in 6.1.

MODULE- usually it will be a single CHAIN and a BSuC dedicated to the FBs, but for FT purposes it may have two or more, redundant Chains. Physically a Module is considered to be a board (PCB).

SYSTEM- the top level, delivering the service stated by the project specification. Usually built up of Modules, a simple System may be a single Module.

FBs are defined to allow for testability concepts (C&O) in the Chain. Modules, expected to be error self-contained, add the FT concept.

Off-Line tests can take place using a single BST chain. This means long Test Vectors (VT), complex to generate, store, analyse, and reducing test speed. Internal PROM releases BSuC pins for independent TMS lines, to provide parallel TAP access to the necessary FBs for each application, leading to powerful and faster solutions. The other TAP signals TCK, TDI and TDO are tied in parallel.

3.2 FB level operation
Given a working FB, we look for:
- pick-up a VTi from the set stored
- shift VTi into the BST chain of
- wait for a similar VI to appear a
- detect a VTi=VI condition and
- compare VI with a stored, except

POST is an 1149.1 compatible requirements, and optimum
suggestions:

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Fig. 07-Hierarchical design relations

Fig. 02- Independent control of FB TAPs in the Chain
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For each FB we have (Fig.03):

Vi= input Vector, arriving at the FB inputs.
Vo= output Vector, captured at the FB outputs.
VTo= input Test Vector, expected.
VTo= output Test Vector, expected as the result of VTi.

- fault coverage of each VTi+VTi pair, or set of pairs.
A fault is, for our purposes, any kind of defect, permanent or temporary, in the FB. On-line failure detection deals with defect coverage, but being more difficult to quantify, we shall refer fault coverage.

**Fig. 03- FB general view, with**

a) If IN and OUT BS cells are number of required TCK cycles:
   of VTi or VI vectors. b) BS cells placed in location A need not be.

The Capture Bit (CB) is a sim. with no pin connection (valid u for OFL tests simply means one to activate POST, CB resets with BS sample or if loaded v "transparent" to the BST infras.

**Fig. 04- Reading CB through**

The mandatory Sample/Prelatch read CB, load VTi and read Vo.
through IR cycles, is made avai.

**Fig. 05-reading CB through IR bits, and the S/P mode is sup.

Capture. Only the first Vo is caj VTi=VI condition happens betw.

POST relies on a careful ana.

machine time diagrams and c.
compatibility to the std is maint.

a) IN and OUT BSs store.

changed and no delay is introdu.
The control of FB's at the Chip level is achieved through the use of control signals. The control signals are generated by the Chip control circuitry. The Chip control circuitry includes the Chip control logic and the Chip control data. The Chip control logic is responsible for generating the control signals. The Chip control data is responsible for providing the data required by the Chip control logic.

The Chip control logic generates the control signals based on the input data. The input data is provided by the Chip control data. The Chip control data is generated by the Chip control circuitry. The Chip control circuitry includes the Chip control logic and the Chip control data. The Chip control logic is responsible for generating the control signals. The Chip control data is responsible for providing the data required by the Chip control logic.

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Writing and solving the equations relating these four parameters, we can design the chart below, with the number of TCK cycles as a function of F and n. The almost line represents the polling frequency (f_p) in kHz, related to TCK, and represented here for the maximum TCK frequency of the BS5C, 33 MHz.

The analysis above gives the worst case (lower) polling frequency because n is taken for all FBs. Regarding practical designs all the VTI/VT0 bit number will be known, and so the exact solution may be computed.

4. Post and failure detection

POST is ON-Line in a discrete (not continuous) way, which explains the Pseudo ON-Line expression.

Detection and Capture are really ONL, but faults may only be detected by the BS5C after reading V0. Now we claim that:

a) If the output of a FB is updated at intervals ΔTou (time update output, constant or variable), and
b) If a number N of VT, with a f_c = X% is verified between two consecutive output updates, then:
c) X will be the probability of a fault to be detected, generating no erroneous FB output, or:
d) The probability of the output to be error-free is X%.

Proof: The first part of assertion b) is accepted valid in Off-Line Tests, by nature. During useful and normal life of digital systems, faults are accepted to happen slowly and ones at a time, many orders of magnitude slower than ΔTou, meaning that conclusion c) must be accepted if assertion b) is verified.

Many examples of real-time systems may be found in the literature [14], from basic system control, elevator, automotive, train, up to plane and space craft control circuits, for which the acceptable fault latency interval usually lies in the 10-100ms interval. According to the figures in point 3, something between 500 and 10,000 VTI/VT0 pairs may be expected to be verified, for each FB during the acceptable fault latency intervals, providing an efficient failure detection mechanism.

In general purpose circuits, the number of FBs in the BS5C must be defined so that the verification time is shorter than the acceptable error confinement delay, defined according to the application requirements.

5. Fault-tolerance features

We have seen in point 3 and 4 that there is an example of a system using BS5C in a debug purposes, avoiding additional anticipated cost of the processor, allows FB outputs to speed, with the real ICs and prototypes for debug and validation.

6. Strengths, Limitations and Enhancements

Some enhancements to POST are found in the literature [14]. The VTI/VT0 pairs are a subset of the simulation functional test vectors. Automatic VTI/VT0 selection tools are being developed, according to the following general rules:

a) calculate β, the f_c for each V0-Vo pair,
b) order VTI by their efficiency coefficient γ = α_c * f_c,
c) select the VTI for the verification rate desired: the Nth VTI with higher γ,
d) Estimate the global f_c. In some cases a f_c=100% may be obtained with M+N vectors, the depth of the circuit being the dominant factor.

f) If a VTI is not detected, the BS5C should replace it after an interval related to the average delay for an input match, otherwise POST rate will degrade.

POST efficiency will be optimised if VTI checking restarts from the top of the above list after each output update, or at cyclic intervals when justified.

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5. Fault-Tolerance features of POST
We have seen in point 3 the failure detection
mechanism. But there is another possibility: upon
detection of an error (Vo≠VTo) the POST structure may
switch for the VTo injection node. In this mode
VTi+VTo are shifted in, and when the triggering input
condition occurs (VTi=V), VTo will be injected at the
outputs of the FB.
Two immediate applications:
a) System self-synchronised Fault-Injection for FT
debug purposes, avoiding additional HW fault injectors.
Anticipated coded information from the system
processor, allows FB outputs to be changed, at circuit
speed, with the real fCs and without the need to build
prototypes for debug and validation of FT designs.
b) Discrete replacement of a defective FB
Uploading selected VTI/VTo pairs into BS/POST cells,
allows the VTO to be available at the FB outputs when
expected, bypassing the FB internal logic.
The B5uC may enter in a FT survival routine, reading
VI and searching the correct VTO (or the best approach
one) to be injected. The Chain may still provide a
Graceful Degradation mode of operation, one VTI/VTo
pair at a time. Software implementations of this survival
mode are named Imprecise computations [17], and aim
to provide in (safe) time, if not the correct output at
least a valid and safe approach. A defective elevator
circuit logic may still provide a continuous, blind,
shuttle service between entrance level and the last floor
restaurant (the origin of POST idea), or a defective
printer logic will still print slowly and a single font type
only. In both cases a failure warning will be reported,
but repair may be delayed.

6. Strengths, Limitations and Research
Some enhancements to POST are possible, but the VT
search process must always be done at BS/POST cells
level, otherwise the B5uC will be overcharged, and
fault coverage will decrease. As such, solutions based
on reading VI and search VTI/VTo in memory, seem to
have a restricted practical interest. Some of the possible
enhancements:
a) In cases where not all the bits of VTi have to, or can,
be defined, using the standard IN BSes the R2 flip-flop
will be available to store a mask bit, and the input
VTi/VI match may be controlled at bit level.
b) If the B5uC is not required to read Vo, or the cells
can not be grouped, POST may be used with no VI
read. VTi and VTO will be shifted into the IN and OUT
BS groups, with detection capability. With 2 CB cells,
the B5uC may follow the operation.
c) POST may be used as Pseudo-CHECKER. Only
OUT BSes are needed, and the B5uC may continuously
verify the captured Vo. A new instruction is desirable to
bypass other cells, increasing the scan speed.
d) VTI detection may be greatly improved with
qualitative information, or if anticipated coded
information is passed to the B5uC by the main
processor, allowing a VTI to be loaded just before it is
expected to occur.

6.1- Strengths of POST
POST has two ways to detect errors (and defects), the
basic one being output mismatch (VTo≠Vo), which
provides detection of defects internal to the FB. But
each FB input group may be seen as a kind of checker
to the previous part of the Chain, and so the B5uC may
also look for an unreasonably low number of input
matches, which may be a result of defects in the circuit
behind the FB. This may be applied to clusters.
Other strengths of POST are:
a) Independence: POST has no impact on the circuit
performance. The Chain may be designed and tested
without the B5uC, to be added later. The same is valid
if the B5uC fails and a watchdog disables it.
b) Easy of design and test: The Chain may be designed
as a whole, and no coding methods are required. POST
B5c will then be routed through desired (FT relevant)
test points, so the number of vectors to test the FB is not
increased by POST. The increased testability provided
by the FBs allows the number of VT required to test the
Chain/circuit to be lower than with a global solution,
bringing non negligible speed improvements.
c) Upgrading: If operating conditions change or a better
set of VTI is defined, by deeper simulation or
monitoring field operation, the B5uC ROM may be
reprogrammed.
d) Rekey: in order to deal with temporary faults, POST
may be allowed to retry the detection of a some errors.
e) Discrete Fault-Tolerance provided by VTo injection.
f) Field Report: the B5uC may keep a trace of all
detected failure situations, stored in memory, which
can be helpful for field engineers.
g) According to the type of BS cells used, POST means
a 10-15% overhead to the std BST. So POST will
probably mean about 1% overhead to the circuit,
excluding the B5uC, obviously external.

6.2- Limitations of POST:
a) Single VTI search at a time
As the scan cells can store a single bit, the resulting
average fault-latency will be a lower bound of a
multiple VTI search, but this seems not to be
compatible with the 149.1 std. Nevertheless the
number of VTI searched at a given time is equal to
the number of BS in the Chain.
b) POST and Sequential circuits
In its actual stage, POST is interesting mainly for
combinational circuits. Sequential circuits, mainly
their depth, restrict the usefulness of POST to FBS with 2 or
3 Flip-flops. However some characteristics seem to be
promising for sequential designs, such as the possibility
of masking some VTI bits and the B5uC ability to
accept more than one VTI for each VTI. As Pseudo-
Checker, POST may deal with complex sequential
blocks, watching the outputs only.
6.3. Future Research

a) Alternative implementations to reduce the average fault latency, and enhancements for sequential circuits are being considered.
b) Can we envisage the use of the BSμC as a VOTER, in a Module with 2 replicated Chips? Will the Module behave as a TMR-like system, with POST helping disagreement decisions? Is the VTU/VTO memory storage still required?
c) What is the behavior of a TMR Module supervised by POST, if the first failed Chip is kept in a degraded operation mode. Is the Module able to sustain a second Chip failure without degrading performance?
d) How do BS Cells influence the FB/Chip reliability?

The figures known point to a 3-5% increase in the failure rate, but this problem and BS Cells protection against circuit injury needs further analysis.

CONCLUSION

Technology enhancements and cost reduction has allowed Fault-Tolerance features in medium-cost designs, some of them referred as "critical but not life critical" systems. Errors and faults must be detected as soon as possible, but not with the requirements of life-critical designs, usually error masking or fail-stop mechanisms, meaning additional resources to provide the high redundancy required ("Morphy was an optimist"), but reducing circuit reliability also.

POST allows a BST enhanced infrastructure to verify on-line the circuit I/O operation, without disturbing system operation and with a fault-coverage and a restricted FT as corollary. With a good cost/benefit relation, fully 1149.1 compliant and requiring no additional instructions, POST may expand BST applications into FT systems design. Actual test speed is being determined with respect to benchmarks, and results concerning fault latency, area overhead and scan insertion timing will be presented in a future paper.

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High-Level Test 5

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INE

Abstract

Boundary-scan based test 1149.1 and P1149.4) can provide mixed-signal board testing in life cycle. The present paper test specification and test plan comments. It describes a mixed-signal language and the associatiuty. The paper includes examples.

1. Introduction

The growing number of and their increasing complexity the constant need for add more demands by new technologies and manufacturing, packaging an difficulty of testing mixed-signal accordingly and is adversly market.

In this paper we consider related to high-level mixed-s We assume the boards are boundary-scan based test bus 1149.1 standard [1], extended tiles through the use of spec [2.3] and/or by the addition of described in the P1149.9 [4] This approach builds on the standard for digital systems, different phases of a product's life the use of low cost test equipn Several support ICs for (BST) have been described [2,3,5,6] and some are avai They range from relatively improve the observability as digital boards [5] to sophisti [8]. BST-based test support capabilities are described in [2] The testing of mixed-signal