FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO



Development of a System for Solar Energy Harvesting in Indoor Lighting Environments

Pedro Pires

Mestrado Integrado em Engenharia Eletrotécnica e de Computadores

Supervisor: Prof. Cândido Duarte (FEUP)

Co-Supervisor: Daniel Oliveira (SiliconGate)

October 22, 2015

U.PORTO
FEUP FACULDADE DE ENGENHARIA UNIVERSIDADE DO PORTO

MIEEC - MESTRADO INTEGRADO EM ENGENHARIA ELETROTÉCNICA E DE COMPUTADORES | **2014/2015**

A Dissertação intitulada

"Development of a System for Solar Energy Harvesting in Indoor Lighting Environments"

foi aprovada em provas realizadas em 15-10-2015

o júri

Presidente Professor Doutor Diamantino Rui da Silva Freitas
Professor Associado do Departamento de Engenharia Eletrotécnica e de Computadores da Faculdade de Engenharia da Universidade do Porto

Professor Doutor Paulo Mateus Mendes
Professor Associado do Departamento Eletrónica Industrial da Universidade do Minho

Professor Doutor Manuel Cândido Duarte dos Santos
Professor Auxiliar Convidado do Departamento de Engenharia Eletrotécnica e de Computadores da Faculdade de Engenharia da Universidade do Porto

O autor declara que a presente dissertação (ou relatório de projeto) é da sua exclusiva autoria e foi escrita sem qualquer apoio externo não explicitamente autorizado. Os resultados, ideias, parágrafos, ou outros extratos tomados de ou inspirados em trabalhos de outros autores, e demais referências bibliográficas usadas, são corretamente citados.

Autor - Pedro Coutinho Pires

Faculdade de Engenharia da Universidade do Porto

© Pedro Pires, 2015

Abstract

The present dissertation addresses the study of a power harvesting system based on photovoltaic (PV) energy conversion in indoor environments. The proposed system consists of a PV cell connected to a DC/DC switched-capacitor (SC). Most PV systems rely on maximum power point tracking (MPPT) to extract the maximum power from the PV cell. However, such power may not delivered to the load, which means the power may be lost in the DC/DC converter due to sub-optimum operating conditions.

The solution proposed overcomes this issue by targeting the maximum output energy delivered to a load or stored in a capacitor. To this end, the power conditioning stage is a multi ratio parallel-series SC DC/DC converter with a load power maximisation scheme. The algorithm is implemented with an asynchronous state machine (ASM), that dynamically changes the topology of the converter to match the load impedance to the internal impedance of the source. This algorithm exploits the geometric relation of the voltage at the terminals of the PV cell, with its open circuit voltage, through an adaptation of the fractional open circuit voltage MPPT scheme to a multi ratio approach. The ASM is also the phase controller of the converter and is able to prevent the load from discharging to the source by dynamically suspending the switching process, should an energy drop on the source occurs. The complete system has been modelled and tested with real office lightning profiles obtained on different places.

Resumo

Este documento aborda o estudo de um sistema de colheita de energia com base na conversão de energia fotovoltaica em ambientes interiores.

O sistema proposto consiste numa célula fotovoltaica, ligada a um conversor corrente contínua-para-corrente contínua (CC/CC) the capacidades comutadas. A maioria dos sistemas fotovoltaicos recorre a técnicas de seguimento do ponto de máxima potência para extrair a máxima potência da célula fotovoltaica. No entanto, essa potência poderá não ser integralmente entregue à carga, o que significa que parte da mesma é perdida no conversor CC/CC devido a condições de operação subótimas.

A solução proposta ultrapassa este aspeto, operando no sentido de maximizar a potência entregue à carga ou armazenada num condensador. Para este fim, o andar de condicionamento de potência é um conversor CC/CC paralelo-série de capacidades comutadas, reconfigurável em vários rácios de conversão de tensão e controlado por um esquema de maximização da potência entregue à carga. O algoritmo é implementado por uma máquina de estados assíncrona, que dinamicamente altera a topologia do conversor the forma a adaptar a impedância da carga à impdância interna da fonte. Este algoritmo explora a relação geométrica da tensão nos terminais da célula fotovoltaica com a sua tensão de circuito aberto, mediante uma adaptação do esquema do seguimento do ponto de máxima potência da fração da tensão de circuito aberto, a uma abordagem multi rácio. A máquina de estados assíncrona é também o controlador de fase do conversor e é capaz de prevenir descargas de energia da carga para a fonte, que podem ocorrer mediante uma quebra de fornecimento energético da fonte, suspendendo e retomando, de forma dinâmica, o processo de comutação do conversor. O sistema foi modelado e testado em diferentes perfis energéticos, obtidos por medições em locais diferentes.

Acknowledgements

First and foremost, I would like to thank my parents and my sister for their support, caring and patience that helped me along the path I have walked so far. I am fully aware of their sacrifices and it will not go without saying that they made all the difference.

To my supervisor, Professor Cândido Duarte, and co-supervisor, Engineer Daniel Oliveira, for their guidance and expertise, and for taking the time to keep me focussed on task at hand. I am most grateful for the role they performed in this project.

I would also like to express my appreciation to SiliconGate. For their willingness to provide me with a place to work on this project and for proposing the project it self.

I thank Pedro Coke, for his help on the early stages of this project.

A special thanks to Rita Robalo for her caring and her wonderful ability to always find the right word or kind gesture to lift my spirit.

To all my friends I thank their availability, for a talk or a cup of coffee, for a day of work or a night out. Their friendship is most cherished.

To all the professors I had the luck to meet that enjoyed teaching, thank you for moulding me into the student I am.

Finally, I thank Maselga and Kikko, for the copious amounts of coffee that slowly drained me of a small fortune in coins, but provided me with numerous moments of joy.

To all, thank you for taking a part in this journey.

Pedro Coutinho Pires

"In the realm of ideas everything depends on enthusiasm...
In the real world all rests on perseverance."

Johann Wolfgang von Goethe

Contents

Abstract i

Resumo iii

1 Introduction 1
- 1.1 Motivation . . . 1
- 1.2 Goals of this Dissertation . . . 2
- 1.3 Methodology . . . 3
- 1.4 Structure of the Document . . . 3

2 Background and Literature Review 5
- 2.1 Photovoltaic Indoor Energy Conversion . . . 5
  - 2.1.1 Principles of Operation . . . 5
  - 2.1.2 Photovoltaic Cell Technology State of the Art . . . 7
- 2.2 Energy Conditioning . . . 10
  - 2.2.1 Background . . . 10
  - 2.2.2 Energy Conditioning Literature Review . . . 13
- 2.3 Energy Storage . . . 16
  - 2.3.1 Background . . . 16
  - 2.3.2 Energy Storage Technology State of the Art . . . 17
- 2.4 Maximum Power Point Tracking . . . 19
  - 2.4.1 Background . . . 19
  - 2.4.2 Maximum Power Point Tracking Literature Review . . . 20
- 2.5 Conclusions to this Chapter . . . 24

3 Indoor Photovoltaic Energy Conversion 27
- 3.1 Photovoltaic Cell Characterisation . . . 27
- 3.2 PV Cell Sensing Conditions . . . 30
  - 3.2.1 Places of Measurement . . . 30
  - 3.2.2 Weather Conditions . . . 31
  - 3.2.3 PV Cell Under Test . . . 31
- 3.3 Indoor Operation of Photovoltaic Cells . . . 32
  - 3.3.1 Current and Voltage Characterisation . . . 32
  - 3.3.2 Input Capacitance Characterisation . . . 35
  - 3.3.3 Energy Feasibility Considerations . . . 36
- 3.4 Practical Photovoltaic Cell Modelling for Simulation . . . 39
- 3.5 Conclusions to This Chapter . . . 42

4 Power Conditioning **43**
4.1 SC DC/DC Parallel-Series Voltage Doubler Mathematical Model 44
4.2 Converter Performance Analysis 47
4.2.1 The Flying Capacitor 47
4.2.2 The Switch Conductance Resistance 50
4.2.3 The Input and Output Capacitors 51
4.3 Impedance Matching 55
4.3.1 Arbitrary Ratio SC DC/DC Parallel-Series Converter Model 59
4.4 Conclusions to This Chapter 66

5 Photovoltaic Energy Conversion **69**
5.1 Output Power Maximisation 73
5.2 Additional Energy Concerns 80
5.2.1 Load Discharge 80
5.2.2 Dormant Time Periods 81
5.3 Conclusions to This Chapter 87

6 Photovoltaic Energy Harvesting System - Proposed Approach **89**
6.1 Proposed System Overview 90
6.1.1 Control Block - The V_{OC} Sampler 90
6.1.2 Control Block - The Ratio Selector and the Phase Controller 91
6.1.3 Conversion Block - The Reconfigurable SC DC/DC Parallel-Series Converter 93
6.2 Multi Ratio Energy Harvester Performance 93
6.2.1 Load Variation 93
6.2.2 Source Variation 95
6.3 Multi Ratio Energy Harvester Indoor Operation 99
6.4 Constrained Power Maximisation 103
6.5 Reconfiguration for Unitary and Step Down Conversion 105
6.6 Conclusions to This Chapter 108

7 Final Remarks and Future Perspectives **111**
7.1 Summary and Contributions of this Work 111
7.2 Discussion of the Results 112
7.3 Future Work 115

A PV Cell Test Platform PCB Schematic **117**

B PV Cell Characterisation Results **119**

C PV Cell Capacitance Measurements **185**

D Energy Feasibility Results **187**

E PV Cell Behavioural Model **225**

F Voltage Doubler Mathematical Model **227**

G Input Voltage Operation Range and Load Power **229**

H The Open Circuit Voltage Sampler Block **233**

I The Ratio Selector Block **237**

J Asynchronous State Machine Phase Control **241**
J.1 Basic ASM Controller 241
J.2 The Phase Controller Block - Multi ratio ASM 243
J.3 The Optimised Phase Controller Block for Constrained Power Maximisation . . . 247
J.4 The Optimised Phase Controller Block for Constrained Power Maximisation and Unitary or Step Down Reconfigurability 251

List of Figures

2.1 PV cell physical structure and equivalent circuit 5
2.2 Characteristic *I-V* curve of the ideal PV Cell 6
2.3 Characteristic *I-V* and *P-V* curve of the practical PV cell 7
2.4 Light source relative intensity and PV Material spectral response 8
2.5 Office and outdoor illuminance levels 9
2.6 Power density of different light sources at various illuminance levels 9
2.7 SC DC/DC main blocks and electrical model 10
2.8 Charge Pump operation and the topology changes on each half period 11
2.9 Common SC topologies and their evolution according to the clock signal phase. . 15
2.10 Commercially available storage devices 18
2.11 Schematic representation of partial shading conditions 19
2.12 Comparison of the tracking factor of different MPPT methods 21
2.13 The two approaches on how to sense the system state, to perform MPPT 23

3.1 Principle of the PV cell characterisation 28
3.2 Scheme of the PV cell characterisation board 29
3.3 Scheme of the places for the PV cell characterisation tests 30
3.4 PV cell models used for indoor operation characterisation 32
3.5 *I-V* and *P-V* curves, V_{OC} and MPP time variation for the IXYS SLMD121H04L PV cell 33
3.6 Energy conversion during a day for the IXYS SLMD121H04L PV cell 34
3.7 Characterisation of the IXYS SLMD121H04L PV cell 34
3.8 Typical energy accumulation profile during a day 37
3.9 Effect of the startup energy or the energy consumption on the PV energy profile . 38
3.10 Energy feasibility analysis of the IXYS SLMD121H04L model on 2015-05-22 . 38
3.11 Scatter plot of startup energy *versus* maximum consumption 39
3.12 PV cell *I-V* curve fitting algorithm 40
3.13 PV cell behaviour modelling 41

4.1 Parallel-Series Voltage Doubler and Switching phases 44
4.2 Voltage doubler mathematical model outputs 46
4.3 Voltage doubler performance with flying capacitance at different switching frequencies 48
4.4 Voltage doubler performance with frequency for different flying capacitor sizes . 49
4.5 Voltage doubler performance with switch R_{ON} resistance at several switching frequencies 51
4.6 Voltage doubler performance performance analysis with input and load capacitors for several switching frequencies 52

4.7 Influence of the input capacitor on the voltage doubler . . . 53
4.8 Influence of the load capacitor on the voltage doubler . . . 54
4.9 Source-load relation . . . 55
4.10 Voltage doubler performance with R_L at several switching frequencies . . . 57
4.11 Voltage doubler performance with switching frequency, for several values of R_L . . . 58
4.12 Seeman approach to the SC DC/DC voltage doubler . . . 60
4.13 SC DC/DC SSL approach analysis . . . 61
4.14 R_{IN} behaviour with frequency . . . 62
4.15 Performance analysis under a varying load . . . 64
4.16 Input voltage and load power behaviour with the load resistance . . . 65

5.1 PV cell used in simulation . . . 70
5.2 PV energy system performance with load resistance . . . 71
5.3 Load resistance sweep keeping the PV cell at the MPP . . . 72
5.4 Factional opern circuit voltage analysis for the IXYS SLMD121H04L model on the 11th of June . . . 75
5.5 K ratios for KV_{OC} which better approximate the MPP . . . 76
5.6 Load power maximisation scheme principle . . . 76
5.7 Behaviour of the load power and input voltage for a varying load . . . 77
5.8 Fractional V_{OC} operation ranges *versus* output power variation formulation example 78
5.9 Fractional V_{OC} operation ranges *versus* output power variation . . . 78
5.10 Output variation due to a source energy drop . . . 81
5.11 Asynchronous state machine algorithm . . . 82
5.12 ASM phase controller results . . . 83
5.13 ASM phase controller results with a PV cell as energy source . . . 84
5.14 ASM phase controller results with a PV cell as energy source . . . 85

6.1 Proposed system architecture . . . 90
6.2 The V_{OC} Sampler . . . 91
6.3 The Ratio Selector and Phase Controller . . . 91
6.4 Reconfigurable SC DC/DC parallel-series converter . . . 94
6.5 Reconfigurable SC DC/DC parallel-series stage . . . 95
6.6 Multi ratio energy harvester performance with load variation . . . 96
6.7 Multi ratio energy harvester performance with variation of the energy source . . . 97
6.8 Multi ratio energy harvester indoor performance with a constant current drawing load . . . 99
6.9 Indoor PV cell behaviour used in simulation . . . 100
6.10 PV cell *I-V* curves used in simulation . . . 100
6.11 Multi ratio energy harvester indoor performance with a constant current drawing load . . . 101
6.12 Lowest energy *I-V* curves on the 22nd and 23rd of May . . . 102
6.13 Extrapolated energy accumulation . . . 103
6.14 Constrained power maximisation . . . 104
6.15 Energy accumulation with constrained power maximisation . . . 105
6.16 Topology of the converter for a VCR equal or inferior to 1 . . . 106
6.17 Operation of the converter with the unitary and step down reconfigurations available 107
6.18 Energy accumulation with constrained power maximisation and voltage unitary and step down reconfigurability . . . 107

6.19 Operation of the converter with the unitary and step down reconfigurations available, under indoor light conditions 108
6.20 Enhanced system architecture 109

A.1 PV cell test board PCB 118

B.1 Weather conditions during the days of the PV cell characterisation tests 119
B.2 Scheme of the places for the PV cell characterisation tests 120
B.3 PV data for the IXYS SLMD121H04L on 19th of May of 2015 121
B.4 Maximum power point coordinates for the IXYS SLMD121H04L on 19th of May of 2015 122
B.5 PV data for the CYMBET CBC-PV-01N on 19th of May of 2015 123
B.6 Maximum power point coordinates for the CYMBET CBC-PV-01N on 19th of May of 2015 124
B.7 PV data for the Amorton AM-1454 on 19th of May of 2015 125
B.8 Maximum power point coordinates for the Amorton AM-1454 CA on 19th of May of 2015 126
B.9 PV data for the Amorton AM-1417 on 19th of May of 2015 127
B.10 Maximum power point coordinates for the Amorton AM-1417 CA on 19th of May of 2015 128
B.11 PV data for the IXYS SLMD121H04L on 22nd of May of 2015 129
B.12 Maximum power point coordinates for the IXYS SLMD121H04L on 22nd of May of 2015 130
B.13 PV data for the CYMBET CBC-PV-01N on 22nd of May of 2015 131
B.14 Maximum power point coordinates for the CYMBET CBC-PV-01N on 22nd of May of 2015 132
B.15 PV data for the Amorton AM-1454 on 22nd of May of 2015 133
B.16 Maximum power point coordinates for the Amorton AM-1454 CA on 22nd of May of 2015 134
B.17 PV data for the Amorton AM-1417 on 22nd of May of 2015 135
B.18 Maximum power point coordinates for the Amorton AM-1417 CA on 22nd of May of 2015 136
B.19 PV data for the IXYS SLMD121H04L on 23rd of May of 2015 137
B.20 Maximum power point coordinates for the IXYS SLMD121H04L on 23rd of May of 2015 138
B.21 PV data for the CYMBET CBC-PV-01N on 23rd of May of 2015 139
B.22 Maximum power point coordinates for the CYMBET CBC-PV-01N on 23rd of May of 2015 140
B.23 PV data for the Amorton AM-1454 on 23rd of May of 2015 141
B.24 Maximum power point coordinates for the Amorton AM-1454 CA on 23rd of May of 2015 142
B.25 PV data for the Amorton AM-1417 on 23rd of May of 2015 143
B.26 Maximum power point coordinates for the Amorton AM-1417 CA on 23rd of May of 2015 144
B.27 PV data for the IXYS SLMD121H04L on 24th of May of 2015 145
B.28 Maximum power point coordinates for the IXYS SLMD121H04L on 24th of May of 2015 146
B.29 PV data for the CYMBET CBC-PV-01N on 24th of May of 2015 147

B.30 Maximum power point coordinates for the CYMBET CBC-PV-01N on 24th of May of 2015 148
B.31 PV data for the Amorton AM-1454 on 24th of May of 2015 149
B.32 Maximum power point coordinates for the Amorton AM-1454 CA on 24th of May of 2015 150
B.33 PV data for the Amorton AM-1417 on 24th of May of 2015 151
B.34 Maximum power point coordinates for the Amorton AM-1417 CA on 24th of May of 2015 152
B.35 PV data for the IXYS SLMD121H04L on 6th of June of 2015 153
B.36 Maximum power point coordinates for the IXYS SLMD121H04L on 6th of June of 2015 154
B.37 PV data for the CYMBET CBC-PV-01N on 6th of June of 2015 155
B.38 Maximum power point coordinates for the CYMBET CBC-PV-01N on 6th of June of 2015 156
B.39 PV data for the Amorton AM-1454 on 6th of June of 2015 157
B.40 Maximum power point coordinates for the Amorton AM-1454 CA on 6th of June of 2015 158
B.41 PV data for the Amorton AM-1417 on 6th of June of 2015 159
B.42 Maximum power point coordinates for the Amorton AM-1417 CA on 6th of June of 2015 160
B.43 PV data for the IXYS SLMD121H04L on 7th of June of 2015 161
B.44 Maximum power point coordinates for the IXYS SLMD121H04L on 7th of June of 2015 162
B.45 PV data for the CYMBET CBC-PV-01N on 7th of June of 2015 163
B.46 Maximum power point coordinates for the CYMBET CBC-PV-01N on 7th of June of 2015 164
B.47 PV data for the Amorton AM-1454 on 7th of June of 2015 165
B.48 Maximum power point coordinates for the Amorton AM-1454 CA on 7th of June of 2015 166
B.49 PV data for the Amorton AM-1417 on 7th of June of 2015 167
B.50 Maximum power point coordinates for the Amorton AM-1417 CA on 7th of June of 2015 168
B.51 PV data for the IXYS SLMD121H04L on 8th of June of 2015 169
B.52 Maximum power point coordinates for the IXYS SLMD121H04L on 8th of June of 2015 170
B.53 PV data for the CYMBET CBC-PV-01N on 8th of June of 2015 171
B.54 Maximum power point coordinates for the CYMBET CBC-PV-01N on 8th of June of 2015 172
B.55 PV data for the Amorton AM-1454 on 8th of June of 2015 173
B.56 Maximum power point coordinates for the Amorton AM-1454 CA on 8th of June of 2015 174
B.57 PV data for the Amorton AM-1418 on 8th of June of 2015 175
B.58 Maximum power point coordinates for the Amorton AM-1417 CA on 8th of June of 2015 176
B.59 PV data for the IXYS SLMD121H04L on 11th of June of 2015 177
B.60 Maximum power point coordinates for the IXYS SLMD121H04L on 11th of June of 2015 178
B.61 PV data for the CYMBET CBC-PV-01N on 11th of June of 2015 179

B.62 Maximum power point coordinates for the CYMBET CBC-PV-01N on 11th of June of 2015 180
B.63 PV data for the Amorton AM-1454 on 11th of June of 2015 181
B.64 Maximum power point coordinates for the Amorton AM-1454 CA on 11th of June of 2015 182
B.65 PV data for the Amorton AM-14111 on 11th of June of 2015 183
B.66 Maximum power point coordinates for the Amorton AM-1417 CA on 11th of June of 2015 184

C.1 PV cell capacitance measurement circuit 185
C.2 Capacitance analysis for the tested PV cell Models 186

D.1 Feasibility of the IXYS SLMD121H04L on 19th of May of 2015 188
D.2 Feasibility of the CYMBET CBC-PV-01N on 19th of May of 2015 189
D.3 Feasibility of the Amorton AM-1454 on 19th of May of 2015 190
D.4 Feasibility of the Amorton AM-1417 on 19th of May of 2015 191
D.5 Feasibility of the IXYS SLMD121H04L on 22nd of May of 2015 192
D.6 Feasibility of the CYMBET CBC-PV-01N on 22nd of May of 2015 193
D.7 Feasibility of the Amorton AM-1454 on 22nd of May of 2015 194
D.8 Feasibility of the Amorton AM-1417 on 22nd of May of 2015 195
D.9 Feasibility of the IXYS SLMD121H04L on 23rd of May of 2015 196
D.10 Feasibility of the CYMBET CBC-PV-01N on 23rd of May of 2015 197
D.11 Feasibility of the Amorton AM-1454 on 23rd of May of 2015 198
D.12 Feasibility of the Amorton AM-1417 on 23rd of May of 2015 199
D.13 Feasibility of the IXYS SLMD121H04L on 24th of May of 2015 200
D.14 Feasibility of the CYMBET CBC-PV-01N on 24th of May of 2015 201
D.15 Feasibility of the Amorton AM-1454 on 24th of May of 2015 202
D.16 Feasibility of the Amorton AM-1417 on 24th of May of 2015 203
D.17 Feasibility of the IXYS SLMD121H04L on 26th of May of 2015 204
D.18 Feasibility of the CYMBET CBC-PV-01N on 26th of May of 2015 205
D.19 Feasibility of the Amorton AM-1454 on 26th of May of 2015 206
D.20 Feasibility of the Amorton AM-1417 on 26th of May of 2015 207
D.21 Feasibility of the IXYS SLMD121H04L on 6th of June of 2015 208
D.22 Feasibility of the CYMBET CBC-PV-01N on 6th of June of 2015 209
D.23 Feasibility of the Amorton AM-1454 on 6th of June of 2015 210
D.24 Feasibility of the Amorton AM-1417 on 6th of June of 2015 211
D.25 Feasibility of the IXYS SLMD121H04L on 7th of June of 2015 212
D.26 Feasibility of the CYMBET CBC-PV-01N on 7th of June of 2015 213
D.27 Feasibility of the Amorton AM-1454 on 7th of June of 2015 214
D.28 Feasibility of the Amorton AM-1417 on 7th of June of 2015 215
D.29 Feasibility of the IXYS SLMD121H04L on 8th of June of 2015 216
D.30 Feasibility of the CYMBET CBC-PV-01N on 8th of June of 2015 217
D.31 Feasibility of the Amorton AM-1454 on 8th of June of 2015 218
D.32 Feasibility of the Amorton AM-1417 on 8th of June of 2015 219
D.33 Feasibility of the IXYS SLMD121H04L on 11th of June of 2015 220
D.34 Feasibility of the CYMBET CBC-PV-01N on 11th of June of 2015 221
D.35 Feasibility of the Amorton AM-1454 on 11th of June of 2015 222
D.36 Feasibility of the Amorton AM-1417 on 11th of June of 2015 223

G.1 Fractional V_{OC} operation ranges *versus* output power variation for the IXYX SLMD121H04L229
G.2 Fractional V_{OC} operation ranges *versus* output power variation for the CYMBET CBC-PV-01N 230
G.3 Fractional V_{OC} operation ranges *versus* output power variation for the AMORTON AM-1454CA 230
G.4 Fractional V_{OC} operation ranges *versus* output power variation for the AMORTON AM-1417CA 231

List of Tables

1.1 Comparison of power densities of different energy sources 2

2.1 Available PV cell technologies 7
2.2 Conversion efficiency comparison of different available PV cells 9
2.3 Possible ratios for SC Converters with 1-3 flying capacitors 11
2.4 VCR values for common SC converter topologies. 13
2.5 Comparison of battery technologies 18
2.6 Tracking efficiency of different control strategies 23
2.7 Summarising table for Energy Harvesting chips 24
2.8 Summarising table for Energy Harvesting solutions tested 24

3.1 Weather conditions on the characterised days 31
3.2 Main characteristics of the characterised PV cell models 32
3.3 PV cell capacitance measurements 36

4.1 Input Voltage and load resistance at the intersection of the load power curves of adjacent ratio converters 66

6.1 DC/DC configuration states 93

Acronyms and Abbreviations

ASM	Asynchronous State Machine
BFV	Best Fixed Voltage
CMOS	Complementary Metal Oxide Semiconductor
CP	Charge Pump
DC	Direct Current
DSSC	Dye-Sensitised Solar Cells
EH	Energy Harvesting
FB	Feedback
FSL	Fast-Switching Limit
INC	Incremental Conductance Method
INR	Incremental Resistance
LDO	Low Drop-Out
LRCM	Linear Reoriented Coordinates Method
LUT	Look-Up Table
MEC	Mountain Equipment Co-op
MOSCAP	Metal Oxide Capacitor
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
OCC	One-Cycle Control
PSD	Power Spectral Density
P&O	Perturb and Observe
POS	PV Output Senseless
PV	Photovoltaic
RCC	Ripple Correlation Control
SC	Switched Capacitor
SSL	Slow-Switching Limit
VCR	Voltage Conversion Ratio

Chapter 1

Introduction

1.1 Motivation

We are living in an era in which energy concerns take an important role on the geopolitical dynamism amongst the nations of the world. The pressing dependency of energy as well as the associated, environmental issues, led to the search of local and renewable energy sources. There are several alternatives to be exploited, such as solar, piezoelectric, vibration, thermoelectric, etc. However, all these options share a common limitation: low energy density. According to previous studies, solar energy is the one that provides the highest energy density per volume unit for low-power systems [1–3], as depicted in Table 1.1. Harnessing solar energy is also interesting due to its obvious environmental advantages as a clean energy source option.

The Sun is the oldest and most potent energy source known to man. It continuously delivers 1.2×10^5 terawatts of solar radiation to earth, from which humanity uses about 13 TW [4]. It is therefore an energy source potentially able to cover all the energetic needs of humanity. European Union, for instance, plans to raise the amount of energy obtained from renewable sources up to 20% until 2020 [5]. Solar energy harvest, however, still needs some improvement in order to become competitive in the market as the best reported efficiency for solar cell conversion rounds 30% [6], being nevertheless under research and development, as reviewed in Subsection 2.1.2.

The evolution of concepts like the "internet of things" [7], and the growth of sensor networks and embedded distributed systems, demand for electronic devices that are independent from the power grid. The most straightforward application of this technology would be a wireless sensor network [8]. WINS [9] and SmartDust [10] are examples of such projects, aiming to integrate sensing, computing, and wireless communication capabilities into a small devices which could be produced at low-cost and large numbers. The main goal of the development of the low power energy harvesting technology would be to effectively reduce power grid dependency of these nodes, thus making them more deployable and independent. Ultimately, it aims to completely snip the electric coords and allow for a self sustainable unlimited operation.

Human wearables, are another application for Energy harvesting. Starner, in [11], presents a survey on methods to exploit the expenditure of energy during everyday actions, to power devices

like a computer, avoiding the impediment of a battery. Other sources of energy generation such as breath or blood pressure, body heat, and finger and limb motion are also analysed.

Further limiting the subject into PV energy harvesting, developments are made mainly in the area of wireless nodes, namely for sensorial data collecting such as those proposed on [12–14]. Other applications include data routing [15] or home automation [16].

Batteries have been used for these application for many years, but they require regular maintenance at usually hard-to-access places [17]. The capability to obtain the needed energy from the surrounding environment, commonly known as power harvesting or energy scavenging, has therefore become a desirable method of powering electronic nodes.

Even though one might conclude that solar energy is more energy dense than the alternatives, when it comes to low-energy surroundings such as indoor environments, a system based on this kind of power harvesting still faces some design challenges. For instance, it must operate as efficiently as possible in order to allow for a self-sustained functioning. In addition, if the available energy is reasonably low, it must be able to enter a sleep or low-power state in which its energy consumption is residual, so that until sufficient power is harvested and stored or environmental conditions changes, the system can be recharged or powered up [18–23]. However, when it comes to implementing a low power solar based energy harvest system, photovoltaic (PV) cells – the energy transducer – are more compact devices than those that harvest energy from other sources, so they can be easily integrated in smaller devices [24] which is a desirable feature as dimension directly correlates with power expenditure.

Table 1.1: Comparison of power densities of different energy sources [3, 19].

Harvesting Method	**Power Density**
Solar cells (outdoor)	15 mW/cm^3
Solar cells (indoor)	10 μW/cm^3
Piezoelectric	330 μW/cm^3
Vibration	116 μW/cm^3
Thermoelectric	40 μW/cm^3
Human Power	330 μW/cm^3
Airflow (5 m/s)	380 μW/cm^3
Acoustic Noise (100 dB)	960 nW/cm^3

1.2 Goals of this Dissertation

This Masters Thesis aims to propose an energy harvesting system based on PV light energy and suitable for indoor operation.

This works aims to develop an energy harvesting system, subject to PV energy conversion in indoor environments, which is capable of efficiently extracting energy from a PV cell, maximising the power delivered to the load, adapt to a variable source behaviour and support varying load conditions.

Specifically, the goals are:

- Study and characterise the operation of the PV cells in indoor environments;

- Develop a behavioural model of the PV cell for practical analysis;
- Develop a mathematical model of the power converter of the system;
- Acquire insight on the influence of the components of the power converter in order to chose a suitable circuit;
- Develop a generic model of the power converter for analysis of arbitrary voltage conversion ratios;
- Implement an algorithm to maximise the power delivered to the load by the system, subject to indoor environment constraints;
- Devise a power converter suitable for the aforementioned algorithm.

1.3 Methodology

Following the order used in Section 1.2 the methodology is as follows.

To study the operation of the PV cells, a Raspberry Pi [25] micro computer was used to control a platform developed for the characterisation process. The latter, implemented with commercial of the shelf components, allowed up to four PV cells to be characterised. Small dimension PV cells were used for this task. The data gathered from the sensing process was then analysed in Matlab [26]. In parallel, a mathematical equation to model the characteristics of the PV cell was developed. It was latter used to generate a behavioural model to use in simulation. In order for this model to accurately mimic the "real" I-V curves of the PV cell, a quadratic error minimisation algorithm was used to find the best fitting parameters for the equation.

The study of the power conversion stage was approached using a mathematical model which was then validated through comparison with results obtained from simulation in Spectre [27]. This model was used to gain insight on the influence of each of the components of the circuit in its operation. It also allowed the choice of the values of these components for the following work.

The load power maximisation scheme was validated in simulation using, initially ideal energy sources and passive loads, i.e. resistors, and then it was validated in simulation, making use of the data gathered from the PV cell characterisation through the behavioural model developed in the same chapter. The functional blocks of the controller that operates the proposed algorithm were implemented in Verilog-A and validated in simulation.

The power converter driven by the aforementioned algorithm was designed using EDA software and validated in simulation, using data taken from measurements of real indoor circumstances.

1.4 Structure of the Document

This document is organised as follows.

Chapter 2 will overview the theoretical fundaments and state of the art of the relevant technology for this work, namely PV cells, energy harvesting systems and power conditioning schemes.

In Chapter 3 the operation of the PV cells will be characterised when in indoor environments. The power conditioning stage of the energy harvesting system will be studied on Chapter 4, in order to develop, in Chapter 5, a power conditioning algorithm for the proposed solution for an energy harvesting system, based on PV energy conversion. The latter will then be presented in Chapter 6, overviewing each of the functional blocks that compose the system, and validating its operation through simulation.

Finally, on Chapter 7, the final conclusions from this work will be drawn, and future perspectives for this work will be discussed.

Chapter 2

Background and Literature Review

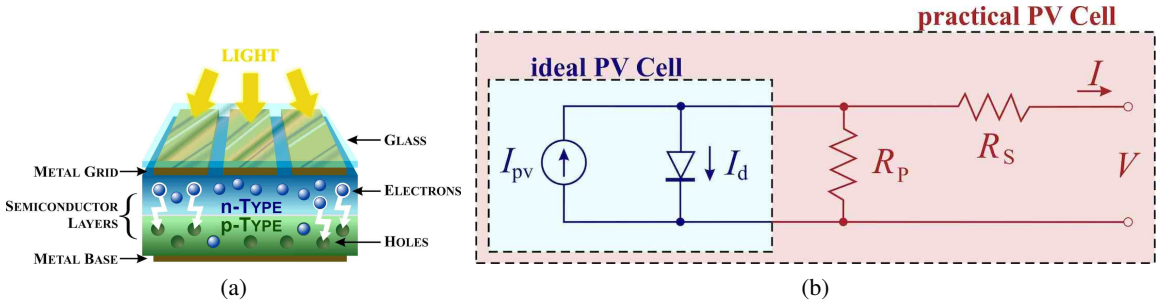
2.1 Photovoltaic Indoor Energy Conversion

2.1.1 Principles of Operation

As stated in [17], a PV cell can be seen as a voltage-limited current source at a wide range of operation (unlike a battery, which is a voltage source). Fundamentally, it is a semiconductor diode whose *p-n* junction is exposed to light [28] – Figure 2.1a. The incidence of light on the cell generates charge carriers that originate an electric current if an external path to the current is provided. This happens when the energy of the incident photons is sufficient to detach the covalent electrons of the semiconductor (depending on the semiconductor material and the wavelength of the incident light). Summarising, this phenomenon may be described as the absorption of solar radiation, the generation and transport of free carriers at the *p-n* junction and the collection of these electric charges at the terminals of the PV device [29].

Figure 2.1b depicts the ideal *vs* practical model of the PV cell. A basic description of the ideal model is

$$I = I_{pv,cell} - \underbrace{I_{0,cell}\left[e^{\frac{qV}{AKT}} - 1\right]}_{\mathrm{I_d}} \tag{2.1}$$



(a) (b)

Figure 2.1: PV cell physical structure and equivalent circuit – (a) Physical Structure; (b) Equivalent circuit of the ideal and practical PV cell.

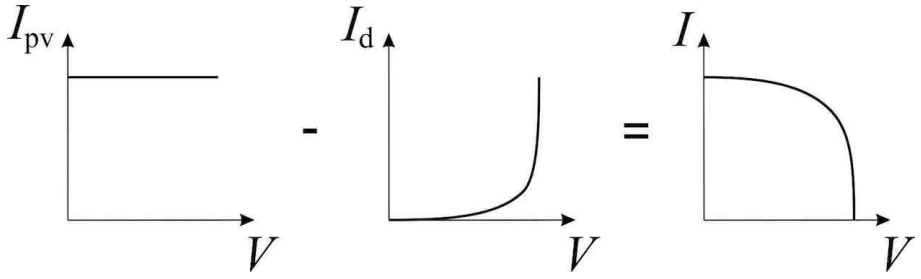


Figure 2.2: Characteristic *I-V* curve of the ideal PV Cell.

where $I_{pv,cell}$ is the current generated by the incident light (proportional to the sun irradiation), I_d is the Shockley diode equation, $I_{o,cell}$ is the reverse saturation or leakage current of the diode, q is the electron charge ($1.60217646 \times 10^{-19}$ C), k is the Boltzmann constant ($1.3806503 \times 10^{-23}$ J/K), T (in Kelvin) is the temperature of the *p-n* junction and A is the diode ideality constant. Figure 2.2 shows the *I-V* curve originated from (2.1).

One should notice that (2.1) does not describe the practical model of a PV array, which is composed of N_s connected cells. To do so, additional parameters must be included in (2.1) [30]:

$$I = I_{pv} - I_0 \left[e^{\frac{\mathrm{V}+R_s I}{V_t A}} - 1 \right] - \frac{\mathrm{V}+R_s I}{R_p} \tag{2.2}$$

where I_{pv} and I_0 are the photovoltaic and saturation current of the array, $V_t = N_s kT/q$ is the thermal voltage of the array of N_s connected in series. Given the case of N_p cells connected in parallel, then the photovoltaic and saturation current would be expressed as $I_{pv} = I_{pv,cell} N_p$ and $I_0 = I_{0,cell} N_p$ [30]. Cells connected in parallel increase the current and when connected in series provide greater output voltage. Finally, in (2.2) we have R_s as the equivalent series resistance of the array and R_p as the equivalent parallel resistance.

From (2.2), one can obtain the *I-V* and *P-V* curves depicted in Figure 2.3, which clearly show three important points of operation: short circuit, MPP and open circuit. It shows also the hybrid behaviour of the PV cell as current or voltage source. Depending on the operation point, the influence of R_s and R_p vary – R_s is stronger on the voltage source region and R_p takes over on the current source region.

Some literature refines this model to provide better accuracy and serve different purposes. For example, by using an extra diode to represent the effect of carriers recombination [31–33] or even a three diode model [34] to further atone for effects not considered in previous models. For simplicity sake, the single diode model is typically used because it offers a good compromise between low complexity and accuracy [35].

The possible performance of a specific PV cell is directly dependent on the material from which it is built. Table 2.1 summarises the currently available PV cell technologies. The used material, along with the light source, influence the PV cell response because light sources manifests differently on the light spectra [1], as depicted in Figure 2.4a. Moreover, the reaction of different materials also differ depending on the light wavelength [37] – illustrated in Figure 2.4b.

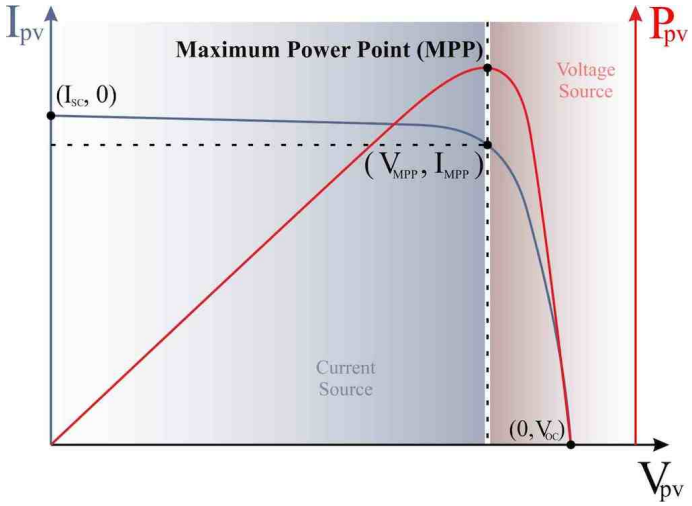


Figure 2.3: Characteristic *I-V* and *P-V* curve of the practical PV cell and the three noteworthy points: short circuit $(0, I_{SC})$, MPP in *I-V* curve (V_{MPP}, I_{MPP}) or MPP in *P-V* curve, and open circuit $(V_{OC}, 0)$.

2.1.2 Photovoltaic Cell Technology State of the Art

It is generally accepted that the modern area of PV power generation had its start in 1954, when Chaplin *et al.* [39] produced a 6 % crystalline silicon solar cell. This technology was rapidly perceived as a convenient way of generating power in remote locations [36], while benefiting from the advantages of a clean energy source. Since then, while the technology evolved many other applications for solar energy were found. These range from spacial industry, as a way to power satellites or exploration modules, to small sized electronics such as wrist watches or calculators. As a result nowadays there is a wide set of PV cell technologies usually classified by generations according to the material used and the level of commercial maturity [4] as summarised bellow:

First-generation PV systems (fully commercial) are built from wafer-based crystalline silicon (c-Si), either in a single crystalline (sc-Si) or multicrystalline form (ms-Si).

Table 2.1: Available PV cell technologies [36].

Material Used	Subform / Type
Silicon	Crystalline
	Multicrystalline
	Amorphous
	Micro-crystalline
III-V Compounds	Gallium Arsenide
	Indium Phosphide
	Gallium Antimonide
Polycrystalline Compounds	Cadmium Telluride
	Copper Gallium Indium Diselenide
	Copper Indium Disulphide
Organic Materials	Dyes
	Polymers
	Fullerenes

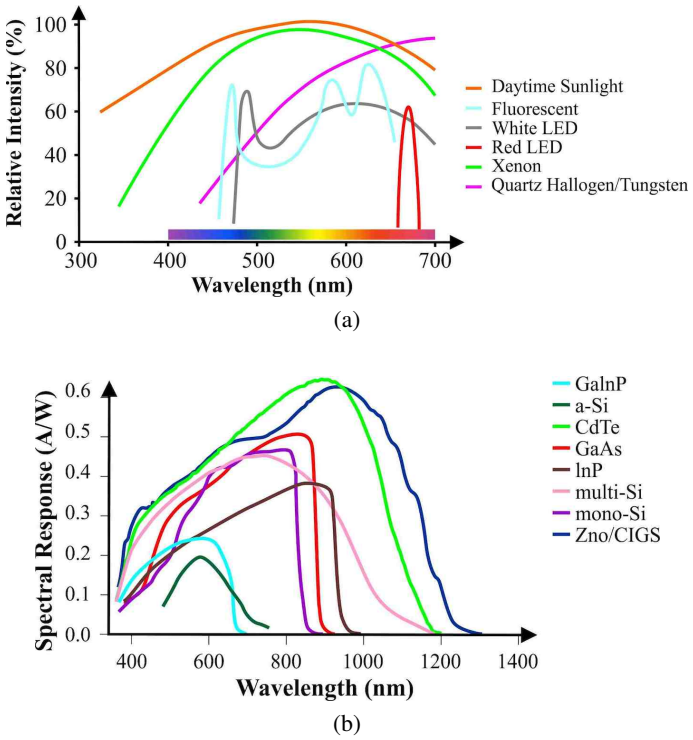


Figure 2.4: (a) Light source relative intensity *vs* spectral content [38]; (b) PV Material spectral response [37]

Second-generation PV systems (in early market deployment) are based on thin-film technologies, divided in three main families: (1) amorphous and micromorph silicon (a-Si / μc-Si); (2) cadmium telluride (CdTe); (3) copper indium selenide (CIS) and copper indium-gallium diselenide (CIGS).

Third-generation PV systems (still in demonstration and additional novel concepts under development) include technologies such as concentrating PV and organic PV cells [40, 41];

Silicon based PV cells dominate the market because of the obvious advantages Si has over other PV materials, namely abundance, and a well established technological base [42], despite its high processing cost [43]. However, third-generation technologies, still in their infancy, may prove an interesting future alternative and the development of nanostructured materials [44] may aid in that process. Novel and emerging concepts such as *quantum dots*, *quantum wells* and *super lattice technologies* [45–47] may achieve very high efficiencies by overcoming the thermodynamic limitations of conventional (crystalline) cells.

When it comes to indoor lighting, the exploitation of PV cells has to cope with the specific characteristics of such environments. Illuminance for instance, usually ranges from 100 to 1000 lux – generally, one to two orders of magnitude lower than the outdoor illuminance [1] as shown in Figure 2.5.

Since the conversion efficiency of the PV cells also decreases for lower illuminance, this results in an even lower converted energy ratio [48]. Moreover, the efficiency achieved by commercial available PV cells is typically 1/3 of the outdoor solar panel conversion efficiency. This is shown

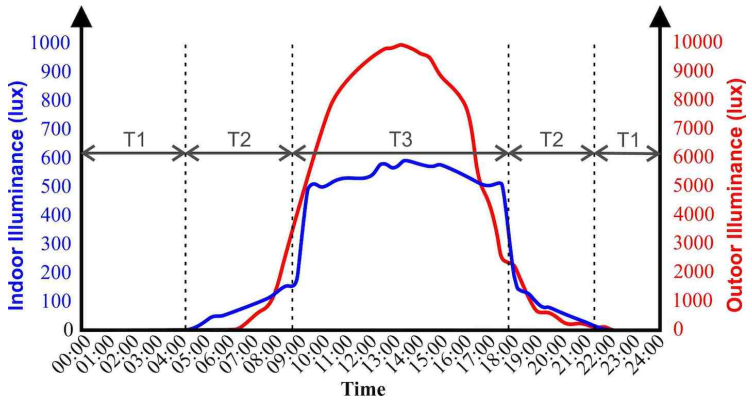


Figure 2.5: Office and outdoor illuminance levels (from [1])

in Table 2.2 for several common solar cell types, such as crystalline Silicon (c-Si), amorphous Silicon (a-Si), and Gallium Arsenide (GaAs).

Table 2.2: Conversion efficiency comparison of different available PV cells [1].

Light origin		**Indoor**	**Outdoor**
Illuminance level (lux)		100 – 1,000	1,000 – 65,000
Solar panel conversion efficiency (%)	c-Si	3 - 8	∼18
	a-Si	2 – 5	8 – 13
	GaAs	2 – 8	7 – 15

Besides this, indoor operation is largely influenced by the existence or absence of artificial light which has a power spectral density (PSD) [1] different from that of the natural (Sun) light, as depicted in Figure 2.4a. According to Wang and O'Donnell [1] and as described in Table 2.2 and illustrated in Figure 2.6, a-Si based cells are more suitable for indoor applications than other technologies.

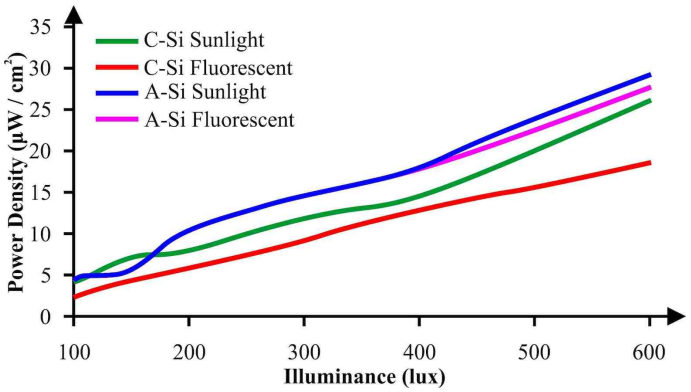


Figure 2.6: Power density of light sources at various illuminance levels [1].

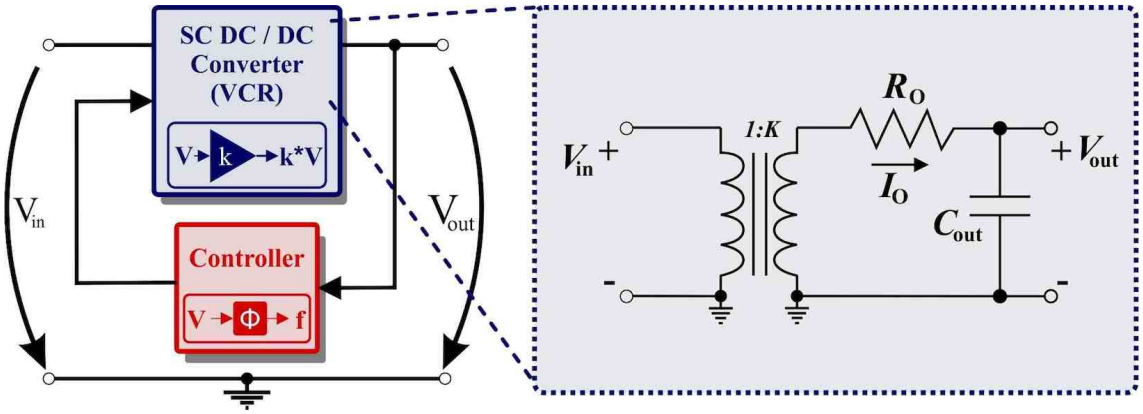


Figure 2.7: SC DC/DC main blocks and electrical model.

2.2 Energy Conditioning

2.2.1 Background

Due to the often unstable conditions at which PV power harvesting systems operate, subject to a time varying unstable supply characteristic, it becomes impractical to directly convey the harvested energy from the energy transducer – the PV cell – to the application unit [49,50], hence the need for a power conversion stage. Its goal is to transfer as much power as possible from the energy transducer to the application unit.

For the power conversion stage, this dissertation will focus on DC/DC Step Up Converters, specifically on inductor-less charge pumps (CP), also known as switched capacitors (SC) Converters. Inductor based CPs were not considered due to the large footprint of an inductor. It means the use of external bulky components [51–53] and it also causes large Electromagnetic Interference (EMI) [54]. SC CPs are therefore an attractive solution, as they consist mainly on on-chip capacitors and transistors, which allow a seamless full integration on silicon [49,55,56].

There are many different topologies of CPs, which will be further analysed in Subsection 2.2.2. However, SC DC/DC converters are functionally divided into two blocks, as depicted in Figure 2.7.

The converter block, which performs the actual voltage conversion, according to its topology, as described above, and the controller block, which acts over a certain variable of the converter, such as the switching frequency, altering the behaviour of the converter block. In broad terms, a DC/DC voltage converter is a circuit that provides an output voltage $V_{out} = K \times V_{in}$, following the general electric model of Figure 2.7.

The K constant is commonly known as voltage conversion ratio (VCR), which if greater than 1 indicates a voltage step up operation. On the other hand, if K is lower than 1 a step down operation is performed. Figure 2.8 show a typical CP operation period (in this case of a Voltage Doubler which has a step up ratio of 2).

In each active phase the SC converter assumes a different configurationn. In Φ_1 the capacitor C_1 is charged by the input source. When changing to Φ_2, the charge in C_1 is partially distributed to C_{out}.

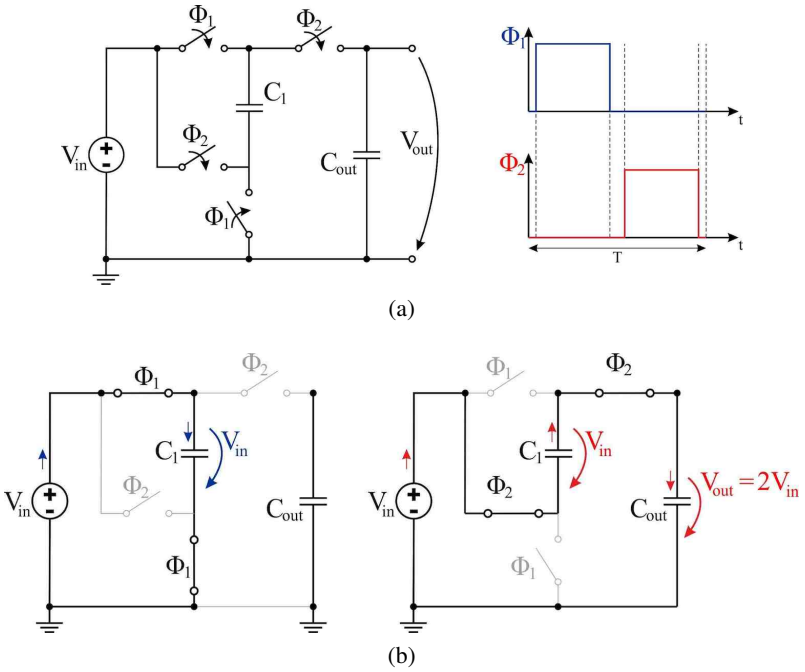


Figure 2.8: (a) Charge Pump (Voltage Doubler) and the two clock signals in phase quadrature; (b) A complete operation period of the CP and the topology changes on each half period.

This operation continues until C_{out} is fully charged and steady-state is achieved. The capacitors that transfer charge between phases – C_1 – are known as *flying capacitors*. According to the signal applied to the switches ($\phi 1$ and $\phi 2$), the equivalent topology changes, as shown in Figure 2.8, causing the disposition of the capacitors to reconfigure (hence the name *flying capacitors*) which in turn causes a charge exchange that allows the energy to gradually flow from input to output.

The ratio K depends on the number of flying capacitors and the topology used. Makowski and Maksimovic [57] enumerated the possible conversion ratios for SC DC/DC converters in terms of the number of flying capacitors, as stated on the "Bounds on Voltage Ratio" Theorem:

$$M = \frac{P[k]}{Q[k]} \tag{2.3}$$

where the positive integers $P[k]$ and $Q[k]$ are the k-elements F_k of the Fibonacci series for $2 \leq k \leq (N+1)$. N is the total number of capacitors, including the output one. For a topology with one to three *flying capacitors*, the attainable ratios are those listed on Table 2.3.

Table 2.3: Possible ratios for SC Converters with 1-3 flying capacitors [57].

Number of Flying Capacitors	Possible Voltage Conversion Ratios
1	$\frac{1}{2}; 1; 2$
2	$\frac{1}{3}; \frac{1}{2}; \frac{2}{3}; 1; \frac{3}{2}; 2; 3$
3	$\frac{1}{5}; \frac{1}{4}; \frac{1}{3}; \frac{2}{5}; \frac{1}{2}; \frac{3}{5}; \frac{2}{3}; \frac{3}{4}; \frac{4}{5}; 1; \frac{5}{4}; \frac{4}{3}; \frac{3}{2}; \frac{5}{3}; 2; \frac{5}{2}; 3; 4; 5$

On the same publication another theorem, "The Number of Switches Required Theorem", bounded the number of switches n_s required to realise a maximum attainable voltage ratio $M_{max}(k)$ with k capacitors as:

$$n_s[M_{max}(k)] = 3k - 2 \tag{2.4}$$

Despite the number of capacitors and switches used, it is the way they are connected that defines which VCR is provided (more on this on Subsection 2.2.2). The output resistance depicted in the electrical model of Figure 2.7, identified in [57] and further studied in [58], presents two different asymptotic behaviours as a function of the switching frequency, the slow-switching limit (SSL) and the fast-switching limit (FSL). The SSL impedance is inversely proportional to the switching frequency. The FSL occurs when the resistances associated with the switches, capacitors and interconnections dominate, and the capacitors act effectively as fixed voltage sources. Other limitations of a CP circuit include *conduction loss* - a fundamental loss mechanism which arises from charging a capacitor through a switch; *Loss due to bottom-plate parasitic capacitors* - lost power due to the charging of bottom-plate parasitic capacitance of the flying capacitors on every cycle; *Gate-drive loss* – the energy expended in switching the gate capacitances of the flying capacitors on every cycle (further detail about this issues on [59, 60]).

A general CP output current can be modelled, according to ([61]), as:

$$I_{OUT} = f_{clk} Q_{avg} = \frac{1}{N-1} f_{clk} C(NV_{IN} - V_{OUT}) \tag{2.5}$$

where N is the ideal voltage step-up ratio, C is the capacitance used in each stage, and f_{clk} is the switching frequency, the variable to be controlled in order to track the MPP. V_{IN} and V_{OUT} are the input and output voltages, respectively. The input current of the CP can be modelled([61]) as:

$$I_{IN} = NI_{OUT} + I_{CP,LOSS} = \frac{N}{N-1} f_{clk} C(NV_{IN} - V_{OUT} + f_{clk}\beta) \tag{2.6}$$

where $I_{CP,LOSS}$ is the internal current loss of the CP, that can be modelled by $f_{clk}\beta$ and β is a constant parameter depending on the specific design [62].

Upon integration of a CPs in a PV system, the input current of the CP is the output current of the PV cell. As well as the input CP impedance which is the output loading of the PV cell. Varying the CP switching frequency is the same as adjusting its input impedance and therefore changing its input current. It now stands out that there is a frequency for each given light irradiance (V_{OC}, [62]) that allows for optimal match between PV cell and CP and thus conveying the maximum power output.

Taking the output current in (2.2) and computing for open circuit operation yields [50, 61]:

$$I_{PH} \approx I_{SAT}\left[e^{\frac{q}{AKT}(V_{OC})} - e^{\frac{q}{AKT}(V_{PH})}\right] \tag{2.7}$$

Considering now (2.7) and (2.6) the switching frequency can be expressed as [61]:

$$f_{clk} = \frac{I_{SAT}\left[e^{\frac{q}{AKT}(V_{OC})} - e^{\frac{q}{AKT}(V_{PH})}\right]}{\frac{NC(NV_{PH}-V_{OUT,CP})}{N-1} + \beta} \tag{2.8}$$

which when V_{PH} equals V_{MPP} results in the corresponding optimal frequency ($f_{clk,optimal}$). Now considering that $V_{MPP} \approx \alpha \times V_{OC}$, where α is an almost constant parameter for a given PV cell, and integrating this result in (2.8) results in a most desired $V - f$ relation for any given irradiance that expresses an optimal frequency at which the entire system will stabilise at $V_{PH} = V_{MPP}$:

$$f_{clk} = \frac{I_{SAT}\left[e^{\frac{q}{\alpha AKT}(V_{OC})} - e^{\frac{q}{AKT}(V_{PH})}\right]}{\frac{NC(NV_{PH}-V_{OUT,CP})}{N-1} + \beta} \tag{2.9}$$

2.2.2 Energy Conditioning Literature Review

The electrical energy provided by the PV cells, in its raw form, cannot be used by the circuitry ahead due to the inherent variability of its output [49, 50]. It must be properly conditioned in order to provide a stabilised voltage (or current) for the loading circuits to use. In low power systems the PV cell output voltage (or current) must therefore undergo a DC conversion process. There are many DC/DC converter types and topologies extensively detailed in literature [63, 64]. However, as stated in Subsection 2.2.1, this dissertation will focus on voltage step up converters and amongst these, SC converters. For these, there are several topologies available. The most common are presented in Figure 2.9 and their VCR listed in Table 2.4.

Table 2.4: VCR values for common SC converter topologies.

Topology	VCR	Observations
Ladder	$(n+3)/2$	n is the number of flying capacitors.
Cockcroft-Walton	$2 \times N$	N is the number of capacitors on the bottom layer.
Dickson CP	$n+1$	n is the number of flying capacitors.
Fibonacci	$F(n+2)$	n is the number of flying capacitors. $F(x)$ refers to the x-th number in the Fibonacci series.
Series-Parallel	$n+1$	n is the number of flying capacitors.
Doubler	2^k	k is the number of stages of the topology.

Historically, the first proposed charge pump circuit was a Dickson charge pump that had a linear topology [55]. Several linear charge pumps optimised for low voltage applications followed but their performance saw substantial decay when used with ultra-low voltage energy transducer [49] such as a PV cell. Cross-coupled SC DC/DC converters such as [65] were then proposed to face this issue. Nevertheless, these failed to operate normally when input voltage was lower than the threshold of transistors. In [49], the authors presented a tree topology with a reduced charge sharing time, leading to an improved charge transfer capability increasing of up to 30% the harvested output power, compared to linear topologies.

When it comes to low-power applications, Maksimovic and Dhar on [59] proposed an attempt to set design objectives and constraints to the area of on-chip power-conversion. In their work they tackle with CP associated issues like conduction and switching losses [59, 60], ultimately advocating the use of identical but opposite-phase SC converters in parallel, thus eliminating the need for separate bootstrap gate drivers – the signals that pull up the operating point of the transistor. Based on this work, Ramadass and Chandrakasan, on [60], propose another approach to minimise SC-associated losses, when considering low-power on-chip solutions. They implement a SC DC/DC converter that harnesses *voltage scaling* [66] to overcome conduction loss, *frequency scaling* [67] to minimise switching losses and a technique called *divide-by-3* to face the bottom-plate capacitance issue. They maintain 70% efficiency over a range of load powers from 5 μW to 1 mW, while delivering load voltages from 300 mV to 1.1 V, in a 0.57 mm^2 area on a 0.18 μm CMOS process. Another important limitation of the SC DC/DC converter is their frequency dependent assymptotic behaviour. Seeman and Sanders, on [68], propose a way to determine and optimise these limits FSL and SSL – refer to Section 2.2. In [69], various power losses inside a power converter were modelled, and an analytical design methodology was presented for optimal transistor sizing. Breussegem also presents a study on die area on [70], concluding that Dickson, Parallel-Series and Fibonacci topologies are equivalent from an area cost point of view. On the other hand, the voltage doubler topology is inferior from this same point of view. A charge pump power converter with variable number of stages was presented in [71], although implemented for a thermoelectric generator system. The authors proposed an algorithm to tune the optimal number of stages, which was theoretically analysed and derived to maximise the charge transfer capability in [72].

A PV cell which is not an ideal source. Therefore there is the need to match the input impedance of the converter with output impedance of the PV cell, in order to extract the maximum power [73]. Pradeep and Vivek, on [74] present a study about the input resistance of the converter, implementing a new control scheme and algorithm that tunes the input resistance of the DC converter to match the PV cell resistance at MPP.

Further studies on DC/DC converter performance can be found in [75] as well as in [76], specifically about two-phase switched capacitor DC-DC converters.

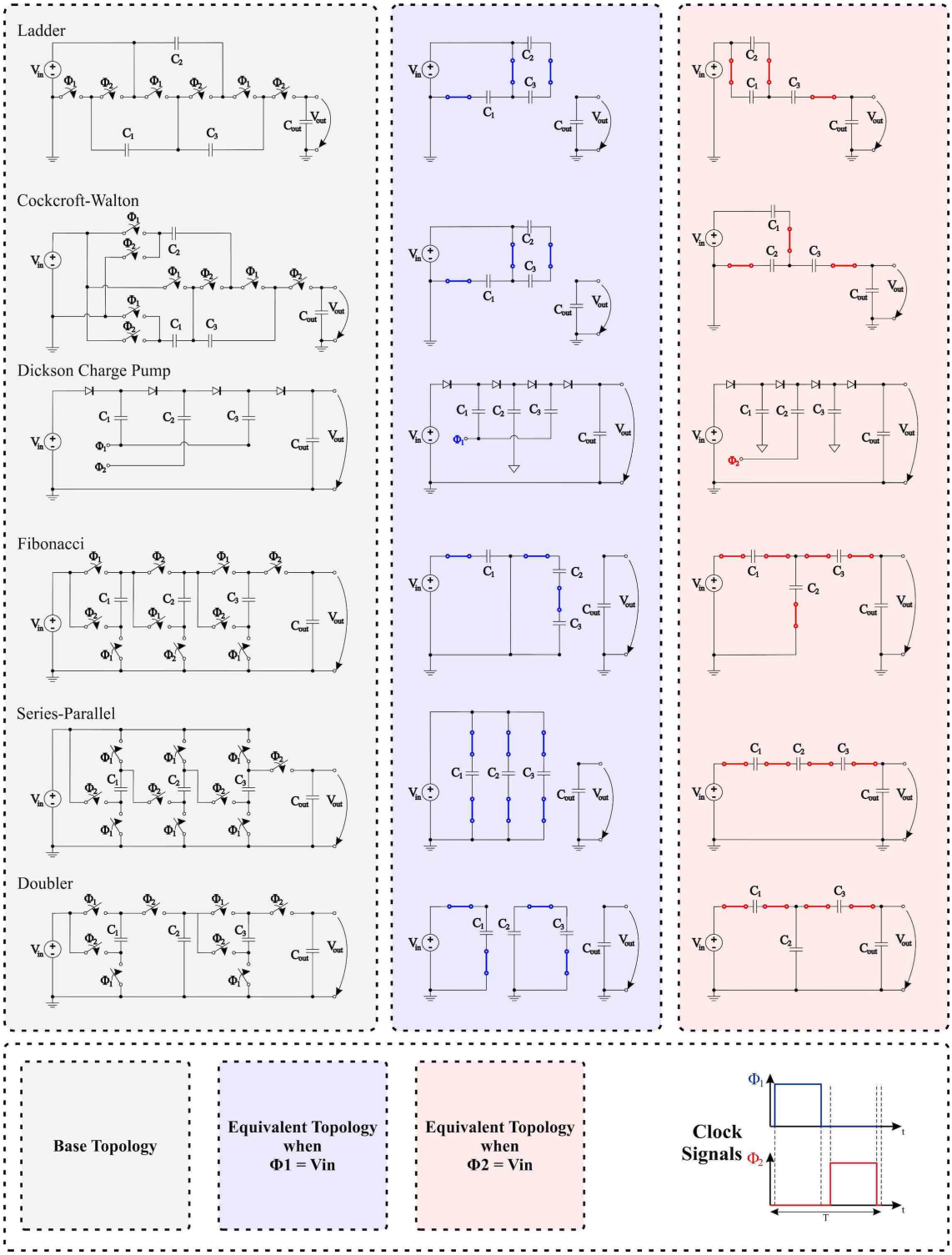


Figure 2.9: Common SC topologies and their evolution according to the clock signal phase.

2.3 Energy Storage

2.3.1 Background

An energy harvesting system requires an energy storage element to better cope with the varying output from the energy conditioning stage [77].

Rechargeable batteries are a widely used storage option. There are several technologies of batteries based on their chemical composition: Sealed Lead-Acid Battery (SLA), Lithium (Li) Air Battery, Li-Ion, Li-Polymer, Nikel-Cadmium (NiCd), Nickel Metal Hydride (NiMH). These battery technologies can be described according to several characteristics [78]: energy density, power density, charge-discharge efficiency (the ratio between stored and delivered energy), self-discharge rate (capacity loss while on idle) and number of deep recharge cycles (a recharge after a complete drain-out). A rechargeable battery is a storage cell with a reversible chemical reaction that depending on the technology, might have certain limitations such as the *memory effect* – loss of energy capacity due to repeated *shallow recharge*, *i. e.* recharge of a partially depleted battery. The battery charging process is yet another aspect to take into account because it may add additional complexity to the overall system. Batteries may allow *trickle charging*, which consists in simply applying voltage to the terminals of the storage device to perform the charging. This method is the most straightforward as it even allows the storage component to be directly connected to the power source [78]. Another option would be *pulse charging*: the use of rapid pulsating current to charge the device. This adds complexity to the system as it requires an additional battery or a dedicated charging circuit [78].

Despite the fact that batteries provide a low cost and wide availability solution for energy storage, they may not be the best alternative for a PV harvesting system [79] because photovoltaic panels are not an ideal source for battery charging. The output is unreliable and heavily dependent on weather conditions. Therefore an optimum charge / discharge cycle cannot be guaranteed. This results in a low battery *state of charge* which in turn leads to sulphation and stratification, both of which shorten battery life [80, 81]. A solution to slow battery ageing would be to use a supercapacitor in parallel with the battery. The supercapacitar would operate as primary energy buffer handling the transient power and minimising the access to the secondary buffer - the battery [14]. Less frequent access to the battery would therefore extend its lifetime. Unfortunately, even with less frequent recharges the battery is still limited to holding charge for a few years before a reduction in energy capacity [14]. Removing the battery altogether and relying solely on the supercapacitor may became a viable option [14].

Supercapacitors are, therefore, an interesting sollution for this application because they provide longer life cycles than ordinary batteries, high power rating, no limitation in deep cycle use and very low negative environmental impact [14, 77, 82]. According to [77], supercapacitors and PV modules are an excellent combination because the energy storage element typically performs deep-cycle discharge every night – discharge most of the stored capacity – and supercapacitors have no limitation in deep cycle use whereas batteries do.

Another important characteristic of supercapacitors is their cycle efficiency, defined as the ratio between the energy input and energy output, which reaches almost 100% [77]. Their terminal voltage can be defined as a linear function their state of charge and it is given by (2.10).

$$V_{cap}(t) = \frac{Q(t)}{C} = \sqrt{\frac{2E_{cap}(t)}{C}} \tag{2.10}$$

where E_{cap} is the energy stored in the supercapacitor and C is the capacitance. E_{cap} varies dynamically as charge or discharge operations are made. The same holds for V_{cap}, whose variation is much higher than the voltage at the terminals of an ordinary battery. Therefore, the charger efficiency of a supercapacitor varies more significantly compared with that of a battery [77].

It is also important to take into account the self-discharge rate of the supercapacitor, which is larger than that of an ordinary battery: it can loose more than as much as 5.9% of its stored energy per day even if no load is connected to it [77, 83]. This voltage decay is given by (2.11).

$$V_{cap}(t+\Delta t) = V_{cap}(t)e^{\frac{-\Delta t}{\tau}} \tag{2.11}$$

where Δt is the elapsed time and τ is the self-discharge time constant. It cannot therefore be used as long-time electrical energy storage, e.g., a few days or more [77]. However short storage times are possible, which copes with a typical PV harvesting system operation profile. Besides this, the charging process of the supercapacitor is a physical phenomena instead of a chemical one (as in batteries). Therefore it is an easily reversible process which results in high efficiency [73]. Further details on the supercapacitor operation principles can be found in [84].

The battery *versus* supercapacitor choice, as is the case with most electronic components, depends on the specifics of the intended application and is all about trade-offs. Charge / discharge cycle limit, discharge depth, physical dimensions / shape, robustness and, of course, cost are therefore parameters to take into account when making such choice.

2.3.2 Energy Storage Technology State of the Art

Following the energy conversion and conditioning process, there is an energy buffering stage that accumulates charge when it is abundant, and supplies it in the remainder. Batteries have been the most widely used option, due to their availability and reasonable cost. In [78], Sudevalayam and Kulkarni compare different battery technologies. These are summarised in Table 2.5.

The authors conclude that both NiMH and Li-based technologies emerge as good storage choices for energy harvesting nodes. Both technologies have pros and cons and the choice depends on the application requirements and constraints. Examples of energy harvesting systems that use batteries as the storage component are implemented in [85–89]. A remark to this comparison is that NiCd batteries are the only type tested that suffers from memory effect. There are also authors who argue in favour of thin-film solid-state rechargeable batteries [90] as an adequate

Table 2.5: Comparison of battery technologies [78]

Battery Type	Nominal Voltage (V)	Capacity (mAh)	Weight Energy Density (Wh/kg)	Power Density (W/kg)	Efficiency (%)	Self Discharge (% / month)	Charging Method	Recharge Cycles
SLA	6	1,300	26	180	70–92	20	Trickle	500-800
NiCd	1.2	1,100	42	150	70–90	10	Trickle	1500
NiMH	1.2	2,500	100	250-1,000	66	20	Trickle	1,000
Li-ion	3.7	740	165	1,800	99.9	<10	Pulse	1,200
Li-polymer	3.7	930	156	3,000	99.8	<10	Pulse	500-1,000

solution for power storage in applications where a high level of integration is required – such as low power energy harvesting systems – because these batteries, built from the deposition of the cathode, electrolyte and anode in thin layers, occupy a very small area. An example of an energy harvesting system that makes use of a thin-film battery is proposed on [91]. Still in the article on [78], supercapacitors are presented as an interesting alternative to batteries. Supercapacitors self discharge at a much higher rate than batteries – as much as 5.9 % per day [83] – and have a very low weight-to-energy density – only 5 Wh/kg as compared to 100 Wh/kg of NiMH batteries. Despite of this, supercapacitors have high charge-discharge efficiency, in the order of 97–98%, and do not suffer from the memory effect. Furthermore, supercapacitors can be trickle charged – refer to Section 2.3 – hence do not need complex charging circuitry [83]. NiMH batteries can also be charged through this method. Theoretically, supercapacitors have infinite recharge cycles [92]. Additionally, they can be used as energy buffers for a jittery energy source [78].

Historically, capacitors have never been used as primary energy buffers due to their limited capacity. Nevertheless, the capacity of a supercapacitor ranges from milli farad to hundreds of farad, which makes them a viable candidate for an energy harvesting system storage component [14]. With the development of the supercapacitor, other storage configurationns appeared. There are for instance hybrid systems – using both a battery and a supercapacitor that complement each other – to achieve higher efficiency and a more stable energy output [84, 92–98]. In order to avoid the encumbrance of having a battery that, no matter the operation regimen, will have a short life – leading to added cost of maintenance or replacement – some authors propose the removal of the battery altogether [99–103]. For visual reference, examples of commercial storage devices are illustrated in Figure 2.10.



Figure 2.10: Commercially available storage devices. Li-Ion: Panasonic-BSG P088-ND; NiMH: Energyzer NH12-700; Thin Film: Cymbet 859-1009-1-ND; Supercap: Tayo Yuden HR4-SERIES.

2.4 Maximum Power Point Tracking

2.4.1 Background

PV systems, in general, suffer from two major problems: the conversion efficiency of the PV device itself, which is low (around 17 %, specially under low light conditions [104]), and the continuously changing weather conditions that influence the power generated by the PV array. In the former case, the performance is essentially constrained by the technology. For the latter the overall efficiency can be improved by implementing an MPPT method, considering the *I-V* curve nonlinearity and temperature/irradiance dependence of the PV cells. For outdoor applications, MPPT methods are almost mandatory and widely used, however, the usefulness of these tracking algorithms diminishes when using PV arrays under partial shading conditions since multiple MPP's exist – see Figure 2.11. In this case, the MPP controller may not be able to recognise the global maximum (i.e. it detects the local MPP instead) and the system efficiency is significantly reduced [105]. On the other hand, for indoor applications, partial shading conditions have no evident effect that can interfere with an MPPT algorithm [106] thus rendering MPPT as essential as for the outdoor case. Indeed there is always a point at which the PV system operates at maximum efficiency, thus extracting maximum power from the PV device – Figure 2.3. MPPT methods may be categorised fundamentally in three groups, as described next.

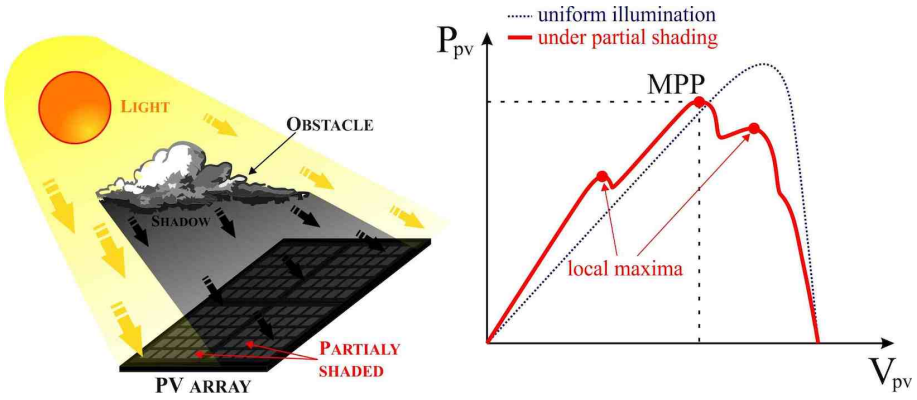


Figure 2.11: Schematic representation of partial shading conditions and the effect on the *I-V* characteristic.

2.4.1.1 Look Up Assignment Table Methods

Techniques in this group are based in the storage of a large dataset of PV data, obtained by experimental measurements. When under operation this dataset is queried in order to assert how to react to the given circumstances [107–110]. However, it is unfeasible to store *all* information and practically impossible that the real operation conditions exactly match those recorded on the table, thus inducing inaccuracies in this technique. This method rather looks for the most approximated data on the previously acquired dataset.

2.4.1.2 Computational Methods

The nonlinear *I*-*V* curve of a PV cell is modelled by a mathematical equation under different varying temperature and insolation levels. Using this model, the corresponding MPP is instantly calculated. Some of these methods also require the costly measurement of solar insolation level [108, 111]. The main drawback of this control system is that it is simply a curve fitting method and, as such, not feasible under all conditions.

The two previous MPPT groups have also the disadvantage of being based on models built for specific cases. This means that, by changing the operation conditions (a different PV cell, for example), renders them less efficient. They are collectively known as "Quasi-MPPT Methods", as they do not actually track the MPP but rather follow a model or approximation [73]. The most widely known method of this group is the fractional open circuit voltage (V_{OC}). It simply assumes that the MPP occurs at a specific fraction of the V_{OC} [112].

2.4.1.3 Perturbation and Observation Methods

These are the most widely used MPPT techniques because of their simplicity [113, 114]. They operate periodically in two phases. First, on the perturbation cycle they affect the PV system. Secondly, on the observation cycle, they assert if the previous perturbation led to an increase or decrease of output power, deciding if on the next cycle the array is perturbed in the same or opposite direction, driving the system towards the MPP. However, these are time consuming methods, leading to power losses and inability to track the MPP on rapidly varying weather conditions – faster computation can tackle this problem [115, 116].

On Subsection 2.4.2, a more in depth evaluation and comparison of different MPPT methods is provided.

2.4.2 Maximum Power Point Tracking Literature Review

Although not strictly mandatory, the use of MPPT techniques is highly recommended because it maximises the energy harvest efficiency by seizing most of the available energy from the environment [73]. In outdoor environments, the employment of these techniques allows an increase of harvested energy in the order of 65 to 90 % [117], which would otherwise be wasted. MPPT refers to a broader expression, applicable for many different energy sources [1–3]. This dissertation will focus on the set of MPPT techniques used in PV energy harvesting. Amongst these, special attention will be payed to those suited for low lighting conditions, as this is the scope of this work. There are some techniques which operate by changing the PV cell position in order to maximise the solar exposure such as the proposed on [118]. These techniques will not be considered because the need to power moving parts, in low energy conditions, may prove a non-sustainable overhead. The low-energy restrictions impose the design of a system that thrives to maintain the interaction between the energy processing system and the harvester at an optimum level [93].

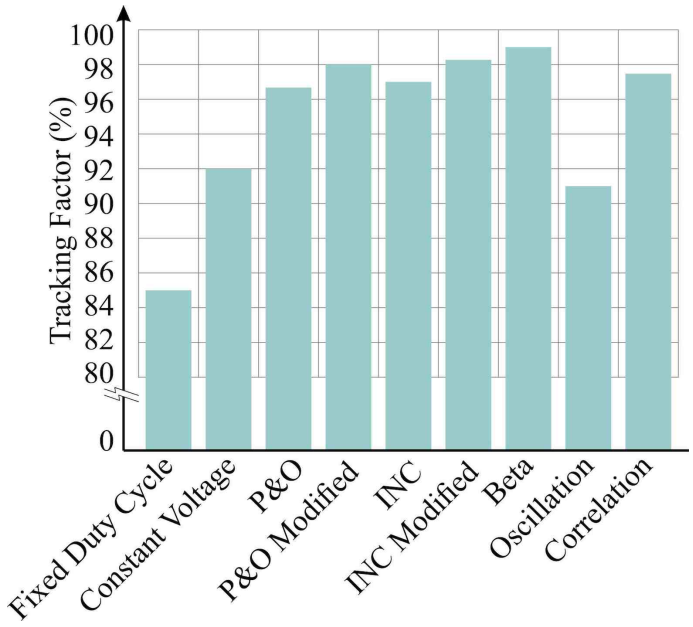


Figure 2.12: Comparison of the tracking factor of different MPPT methods [130].

There are many techniques to track the MPP. A survey on the methods available up to 2012 is made by Ali *et al.* on [104]. Subudhi and Pradhan, on [115] make a comparison between some of these methods considering the number of control variables involved, types of control strategies, circuitry, and cost of applications, in order to provide useful criteria for selecting an MPPT technique for a particular application. They also list some commercially available products. There are also some more focused comparisons between the two simpler methods, perturb and observe (P&O) [119] and incremental conductance (INC) [120] that report better performances for the P&O [121, 122]. An example of an energy harvesting system that uses the P&O method can be found in [119], and using the INC method in [120].

On [123], Ali Reisi presents another comparison between some MPPT methods, by dividing them in three categories: *offline*, *online* and *hybrid* methods. This classification is based on the manner in which the system state is sensed and on how the control is enforced. *Offline Methods* are those referred by other authors as "Quasi MPPT Methods" or "Look Up Assignment Table Methods / Computational Methods" – see Section 2.4. Fractional V_{OC} [112], fractional short circuit current [124] and artificial intelligence methods like artificial neural networks [125] and fuzzy logic [126] are examples of *offline methods*. *online Methods* implement *real time* MPPT and include extremum seeking control method [127], as well as previously mentioned P&O and INC. A *hybrid method* implements both *online* and *offline* strategies in different control loops, as in [128, 129]. Reisi [123] concludes that, under relatively equal implementation conditions the *hybrid* methods have a better performance. Further studies on performance of different MPPT methods, regarding the energy extraction efficiency are made by de Brito *et al.* on [130]. The author states the superiority of the Beta Method (β) [131], as illustrated in Figure 2.12.

These last articles however, focus on PV systems employed to generate high amounts of power,

for house or industry powering purposes. Some of these techniques can however be extended to very low power systems – at the scale of μW or mW [73, 115]. There is the need however, to take careful criterion when choosing a MPPT method, due to the restrictive constraints imposed by an indoor environment energy harvesting system: low generated power, voltage conversion, leakage, efficiency, and power consumption.

On [106], Vignati makes a comparison of different MPPT techniques, listed on [132], to be used on an indoor light energy harvest system. The author prioritises the methods according to a set of parameters withdrawn from previous literature such as tracking speed, implementation complexity, cost and efficiency. Moreover, the author excludes from this evaluation methods that require the use of inverters, such as DC-link capacitor droop control or one-cycle control MPPT, big arrays of PV cells, as array reconfigurationn method and complex computations, for example, $\delta P/\delta V$ or $\delta P/\delta I$, linear current control or methods based on temperature or irradiance sensing. Detailed information about these methods can be found in [104, 115]. Upon evaluation based on these parameters, ripple correlation control (RCC) [133] and fixed voltage methods scored higher while Fractional I_{SC} and INC had the fewest points. Fractional V_{OC} was also well classified and P&O sat on an average score. These results are detailed on [106]. Nevertheless, after experimental tests, the author concluded that at low illuminance levels, the light could be so dim that the power generated by the tested PV panels became too low to run a tracking algorithm ([106]). An usual approach to tackle this issue and to exploit a wider operation range would be to simply *turn off* the MPP tracking. Indeed, several authors implement energy harvest systems that can enter a low power / sleep state, MPP tracker bypass method or topology reconfigurationn to encompass such issue [101, 134–136].

The choice of an MPPT technique, if any, depends on the implementation. There are several parameters to take into account when opting for one or other MPPT method, with its benefits and trade-offs. The method used to sense the system state is one parameter that deserves special attention. It directly relates with the complexity of the system and on more technical aspects like power consumption and dimensions. The type and number of sensors indeed affects the decision of which method to choose [73]. Typically, the physical variables sensed are either voltage, current or both – when there is the need to compute true power as in the $\delta P/\delta V$ or $\delta P/\delta I$ method. Generally, it is preferable to sense voltage, because current sensors are usually expensive and bulky [73]. There are also methods that sense temperature or irradiance, such as I_{MPP} or V_{MPP} computation [115, 121, 122, 132]. There are even methods that need not sense any variable, like the best fixed voltage method [132].

However, besides which variable to sense, it is also important to decide *where* to sense it. Either on the converter input or on the output side. Shmilovitz, on [137], proposes a control approach based on the output parameters i_{out} and v_{out} rather than on the input ones. Figure 2.13 depicts a schematic comparison of the two approaches. The author argues that the power converter used might have an efficiency curve that yields maximum output power at an operation point that does not coincide with maximum input power in which case maximum output power is the choice of preference. Additionally, the output parameter-based controller is simpler and requires

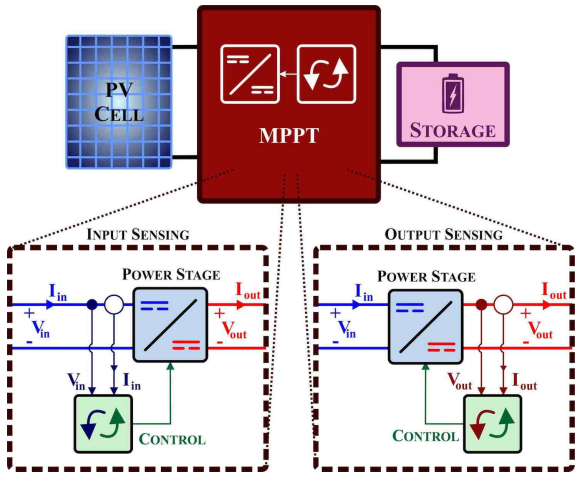


Figure 2.13: The two approaches on how to sense the system state, to perform MPPT.

fewer sensors. Regardless of the particular control algorithm employed, input parameter-based controllers, such as those implemented in [112,138,139], require sensing of i_{in} and v_{in}. In contrary, output parameter-based controllers, as those found on [140–142], requires sensing of only *one* output parameter i_{out} or v_{out}. This is a general feature of output parameter based controllers, which applies to a wide range of load types, including nonlinear ones. The author, backed up by previous work on [143–146] demonstrates that single output parameter control is, in general, possible and advantageous for nearly all practical load types, as shown on Table 2.6.

Table 2.6: Tracking efficiency of different control strategies, adapted from [137].

Control strategy	TE for Resistive Load (%)	TE for Battery Load (%)
Output I and V maximization	97.6	99.3
Input I and V maximization	98.0	99.6
Output I maximization	98.8	99.9
Output V maximization	98.3	99.1
Load characteristics	Resistive, 1 Ω, P_M =170 W	Battery, P_M =170 W

Although still a very young sector in the market, there are some solutions able to perform at very low-power levels. Vignati, on [106], collects a list of all the relevant commercial chips found on the market and in prototyping phase. Their characteristics, based on the datasheets are, for convenience, summarised on Table 2.7.

The author tested BQ25504, MAX17710 and MAS6011, to conclude that MAX17710 is able to squeeze more power at high light levels, rather than a more linear MAS6011, which is the only solution able to work in poorly lit environments, outputting 4 μW at 10 lux. In fact, due to its extremely low power construction, MAS6011 is able to maintain an average efficiency of more than 80% for all the illuminance range [106]. The results of this comparison are summarised in

Table 2.7: Summarising table for EH chips. Prices are for single component and they are extracted from www.digikey.com. Adapted from [106].

Energy Harvester	EH Source Type	Consumption / Starting Voltage	Type / MPPT?	Battery Types	LDO	Cost
Texas Instruments BQ25504	Low V DC (Solar, Thermal)	330 nA / 330 mV	boost / yes	Li-Ion, Li-Va MECs, SC	no	$6.35
Maxim Integrated MAX17710	Low/High V DC/AC (Solar, Thermal,Vibration)	625 nA / 750 mV 1 μW/ 750 mV	linear/ no boost / no	MECs	1.8 V 2.3 V 3.3 V	$8.89
Micro Analog Systems MAS6011	Solar	110 nA / 2.0 V	diode / no	Li-Va	no	$1-1.5
Linear Technology LTC4071	Solar, Piezo	550 nA / —	diode / no	Li-Ion, MECs	no	$4.92
Cymbet Corporation CBC915	Low/High V DC/AC (Solar, Thermal,Vibration)	— / —	CP / yes	proprietary cells	no	$4.91
Anagear Semiconductors ANG1010	Solar Optimized	400 nA / 1.5 V	boost+buck / no	Lithium cells	2 adjustable 0.9-3.0 V	—

Table 2.8.

Table 2.8: Summarising table for Energy Harvesting solutions tested. The "–" symbol means that the power value is less than $1\mu W$. Averaged over 10 samples. Adapted from [106].

Energy Harvester	Converter Type	Solar Module	Load Voltage	Pout at 94 lux	Pout at 980 lux	Average Efficiency
Texas Instruments BQ25504	boost	2×AM-1454	3.0 V	51 μW	629 μW	62.8%
	bost	SP–7375–0.5 V	3.0 V	59 μW	905 μW	47.7%
	bost	2×AM-1454	4.0 V	50 μW	629μW	57.5%
	bost	SP–7375–0.5 V	4.0 V	54 μW	977 μW	45.4%
	bost	SP–7375	4.0 V	29 μW	965 μW	33%
Maxim Integrated MAX17710	linear	AM-1815	4.0 V	57 μW	740 μW	62.9%
	linear	SP–7375	4.0 V	16 μW	1069 μW	44%
	bost	2×AM–1454	4.0 V	n.a.	249 μW	n.a.
Micro Analog Systems MAS6011	linear	AM–1815	3.0 V	63 μW	654μW	88.6%
	linear	SP–7375	3.0 V	75 μW	925 μW	84.9%

2.5 Conclusions to this Chapter

In this chapter, an overview of the operation principles of of each functional module of a typical PV energy harvesting is made.

The photovoltaic process is explained as it configures the energy conversion stage of the system. Given the fact that the energy conversion and energy conditioning stages are two interfacing modules of the system, after introducing the operation of a charge pump, the interaction of these two modules is then analysed and, based on the work on [61], a f-V relation that expresses an optimal frequency at which the entire system will stabilise at $V_{PH} = V_{MPP}$ is extracted. The Maximum Power Point Tracking methodology is also presented as the technique that allows the system

to find and converge to the point of maximum energy extraction. Finally, the principles of energy storage are presented, giving special focus to the supercapacitor as the storage component of the system.

Additionally, a review of the state of the art of PV energy harvesting systems was made, focussing on low power indoor variants of this technology. The progress and current development of each individual module of the system was analysed in the current chapter, hinting for novel concepts and innovative research on these areas.

PV energy harvest, specifically for low power applications, as those that rely on indoor lighting conditions for self powering, is taking an ever growing importance. It conveys the building blocks and concepts to design systems that are able to operate efficiently and self sustainably for an ideally unlimited period of time. By being able to guarantee energetic self sufficiency, these systems become independent from the power grid and thus, widely deployable. The possibilities for such systems vary from data collecting to home automation and their development is of the utmost importance because, on the process of relying to renewable energy sources, they also bring forth environmental advantages.

Chapter 3

Indoor Photovoltaic Energy Conversion

In order to design a system adequate to the indoor operation, it is important to gain insight on the behaviour of the PV cell when subject to the indoor operation constraints (low illuminance). this chapter aims to:

- Development of a platform to bias and measure the PV cell electrical characteristics;
- Characterise the operation of different PV cells, indoors;
- Gain insight on the energy availability of such context;
- Study the feasibility of a system based on indoor PV energy;
- Develop a behavioural model of the PV cell to be used in this work.

On Section 3.1 the PV sensing system used in the experiments, is described, followed by the measurements conditions – i.e. place and weather conditions – on Section 3.2.

The results of the PV cell indoor operation analysis are presented in Section 3.3, specifically the electrical characteristics and behaviour of the PV cells under test – *I*-*V* curve and parasitic capacitance.

On Section 3.4, a PV cell behavioural model for simulation is discussed. It is intended to provide a practical approach to the behaviour of the PV cell to be used in this work.

Finally, Section 3.5, closes this chapter with the summary and discussion of the results.

3.1 Photovoltaic Cell Characterisation

A PV cell behaviour is modelled by an current-voltage (*I*-*V*) curve that defines its behaviour as an energy source. Figure 3.1 illustrates a typical *I*-*V* curve – refer to equation 2.1. It is possible to bias the operation point of the PV cell by changing the resistance at its terminals, hence constraining the output current and therefore forcing it into a specific operation (V, I) coordinate.

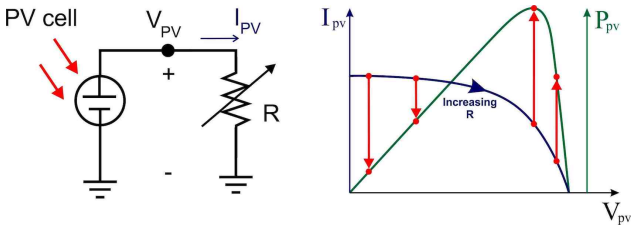


Figure 3.1: Principle of the PV cell characterisation: each value of R at the PV terminals defines an operation point, i.e. a specific (V_{pv},I_{pv}) coordinate with a correspondent voltage-power (V_{pv},P_{pv}) coordinate (also shown in figure).

The system proposed to address the PV characterisation is based on this principle. Several digital potentiometers are used to sweep the resistive value at the PV cell terminals and measuring its voltage, thus tracing its *I*-*V* curve.

The designed system is depicted in Figure 3.2. It comprises a Raspberry Pi board [25] to store the acquired data and digitally control the value for the PV load, digital potentiometers, and digital multiplexers.

The measurement platform is able to vary the resistance between $R \approx 0\,\Omega$ and $R \approx 4\,\mathrm{M}\Omega$ – short circuit and "open circuit", respectively – and effectively analyse the behaviour of the PV cell in the range of interest. The test platform is composed of two chains of impedance load. A high-impedance chain with 16 digital potentiometers in series with the PV, which can reach up to $4\,\mathrm{M}\Omega$, but having a minimum resistance of approximately $5\,\mathrm{k}\Omega$. This limitation is compensated by a low-impedance chain (in parallel with the high-impedance one), composed of a single digital potentiometer, which can vary between approximately no resistance and $5\,\mathrm{k}\Omega$. Along the load sweep, a multiplexer allows the selection of the low or high impedance chain. This platform is designed to operate with four PV cells simultaneously and it is built to be used as a Raspberry Pi shield [1] – as in Figure 3.2.

[1] A system designed to be directly mounted on the I/O port of the Raspberry Pi to extend the capabilities of the micro computer.

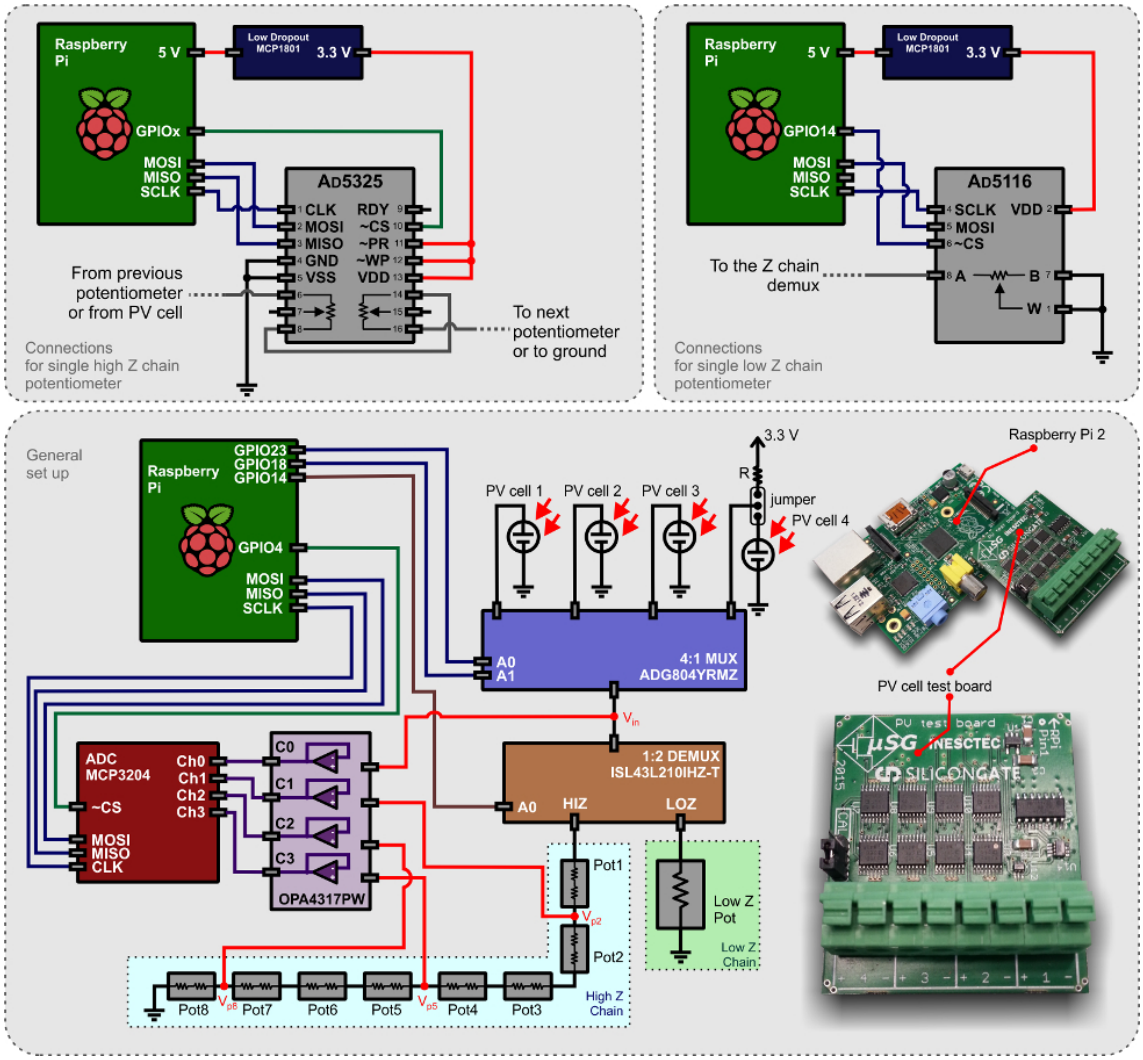


Figure 3.2: Scheme of the test board used to characterise the PV cells under test. Refer to Appendix A for a schematic of the layout.

3.2 PV Cell Sensing Conditions

this section summarises the conditions under which the PV cell characterisation process was conducted. Subsection 3.2.1 illustrates the places where the PV operation sensing took place and Subsection 3.2.2 lists the weather conditions on the days when the PV tests were made.

3.2.1 Places of Measurement

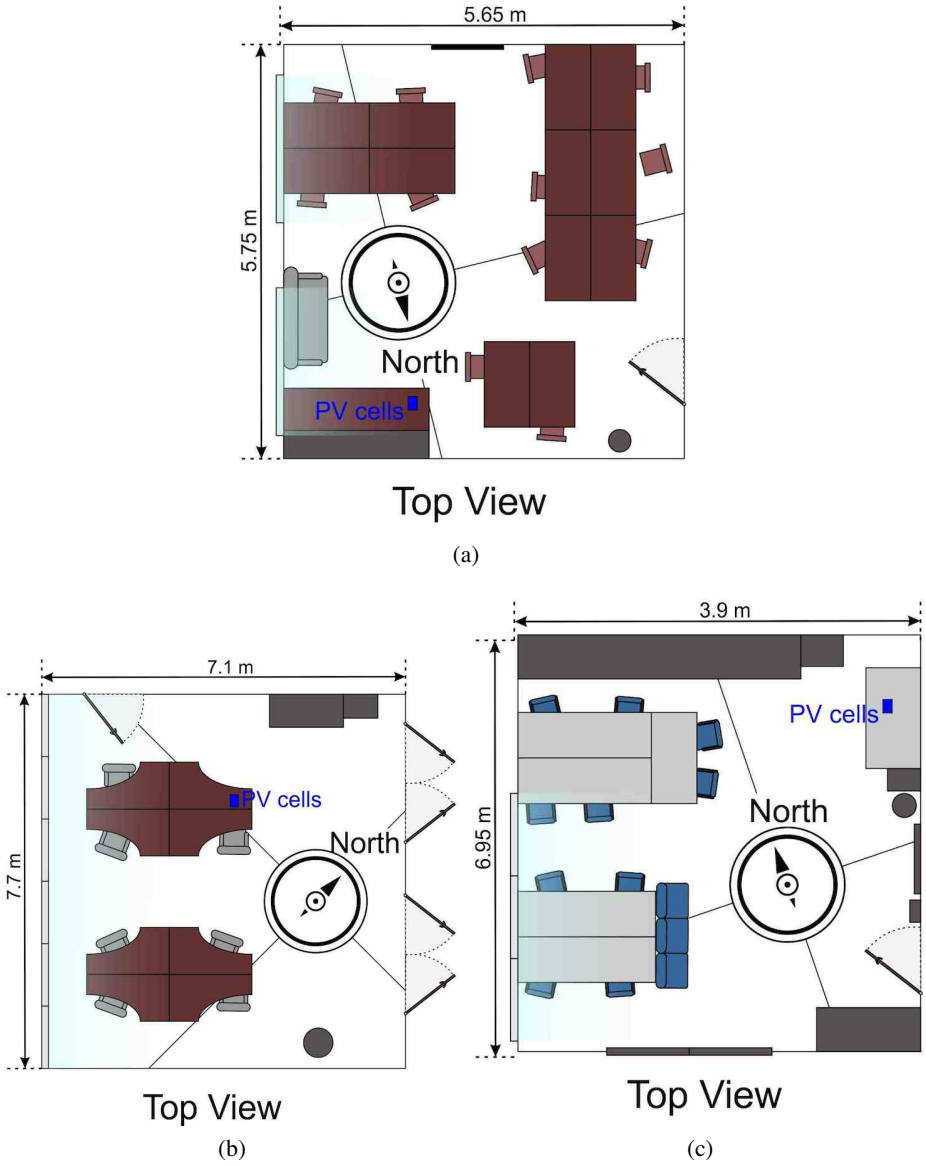


Figure 3.3: Scheme of the places were the PV cell characterisation tests took place – (a) place A; (b) place B; (c) place C.

Figure 3.3 depicts a schematic representation of the rooms at which the PV cell characterisation tests took place, herein denominated as “place A”, “B” and “C”. The characterisation took place in three distinct places, which allowed to test the PV cell operation under different alignments with the solar light trajectory along the day. These rooms varied also in the number and

orientation of the windows, as well as their shape and height, which further varied the testing conditions.

3.2.2 Weather Conditions

Table 3.1 summarises the weather conditions of the days when the PV cells listed in Subsection 3.2.3 were characterised. The place at which these tests were made is also listed (refer to Subsection 3.2.1).

Table 3.1: Weather conditions in Oporto, on the days when the PV cell test platform was operating.

Date (2015)	Place	Minimum Temperature (^{o}C)	Maximum Temperature (^{o}C)	Short Description
19th of May	A	11	20	Sunny, clear sky
22nd of May	B	12	22	Sunny, clear sky
23rd of May	B	11	23	Sunny, some clouds
24th of May	B	14	25	Sunny, clear sky
6th of June	C	12	27	Sunny, some clouds
7th of June	C	15	30	Sunny, clear sky
8th of June	C	20	32	Sunny, clear sky
11th of June	C	13	18	Cloudy, Some rain

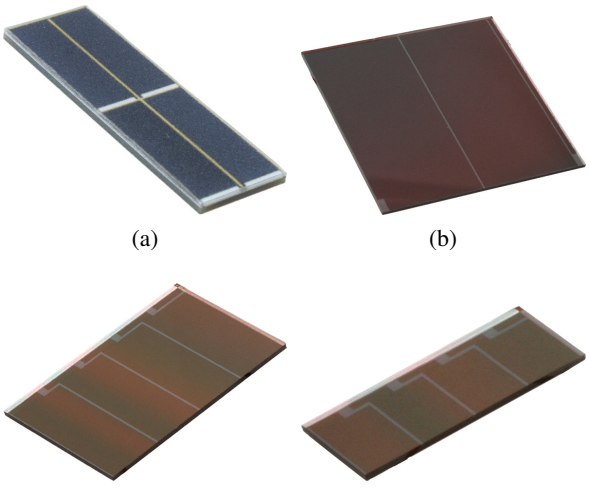
According to Table 3.1, these tests were conducted between May and June which limits the weather to a typical Spring setting. Nevertheless, these days spanned over a fairly wide spectrum of weather conditions, as the meteorologic conditions varied between clean sky sunny days to partially cloudy, as well as cloudy and rainy days. Further detail on the weather conditions of these days can be consulted in Appendix B.

3.2.3 PV Cell Under Test

The models used to characterise the indoor operation of a PV cell are depicted in Figure 3.4.

The main characteristics of the used PV cells are summarised in Table 3.2. These are extracted from the manufacturer datasheets.

Table 3.2 aims to provide the key parameters that describe the PV cell. Not all manufacturers provide the same set of information nor the same amount of detail thus, some characteristics are not present for some models. These specific models were chosen because they vary on dimensions and electric parameters, as well as the type of technology used – monocrystalline silicon and amorphous silicon.



(a) (b) (c) (d)

Figure 3.4: PV cell models used for indoor operation characterisation – (a) IXYS SLMD121H04L [147]; (b) CYMBET CBC-PV-01N [148]; (c) Amorton AM-1454CA [149]; (d) Amorton AM-1417CA [149].

Table 3.2: Main characteristics of the characterised PV cell models. The IXYS SLMD121H04L model characteristics depict the operation under Standard Condition, i.e. 1 sun (= 1000 W/m^2), Air Mass 1.5, 298.15 k. The other three models are characterised under a white fluorescent light at 200 Lux.

Model	**Type**	**Open Circuit Voltage (V)**	**Short Circuit Current (mA)**
IXYS SLMD121H04L	Monocrystalline Silicon	2.52	50.0
CYMBET CBC-PV-01N	Amorphous Silicon	1.2	212×10^{-3}
Amorton AM-1454CA	Amorphous Silicon	1.5	31×10^{-3}
Amorton AM-1417CA	Amorphous Silicon	1.5	12.5×10^{-3}
Model	**Maximum Power Point Voltage (V)**	**Maximum Power Point Current (mA)**	**Dimensions (L x W x H; mm)**
IXYS SLMD121H04L	2.00	44.6	43 x 14 x 2
CYMBET CBC-PV-01N	0.8	201×10^{-3}	58.1 x 56.7 x 1.1
Amorton AM-1454CA	(not provided)	(not provided)	41.6 x 26.3 x 1.1
Amorton AM-1417CA	(not provided)	(not provided)	35 x 13.9 x 1.1

3.3 Indoor Operation of Photovoltaic Cells

3.3.1 Current and Voltage Characterisation

Using the characterisation method illustrated in Figure 3.2 yielded the results shown in Figures 3.5, 3.6 and 3.7. These Figures are an example selected from the acquired data – refer to Appendix B – which depict the operation of the IXYS model on a sunny day and on a cloudy day – 24-05-2015 and 11-05-2015 respectively. The measurements were made ensuring that the PV cells under test were not directly hit by sunlight, depicting a typical indoor environment.

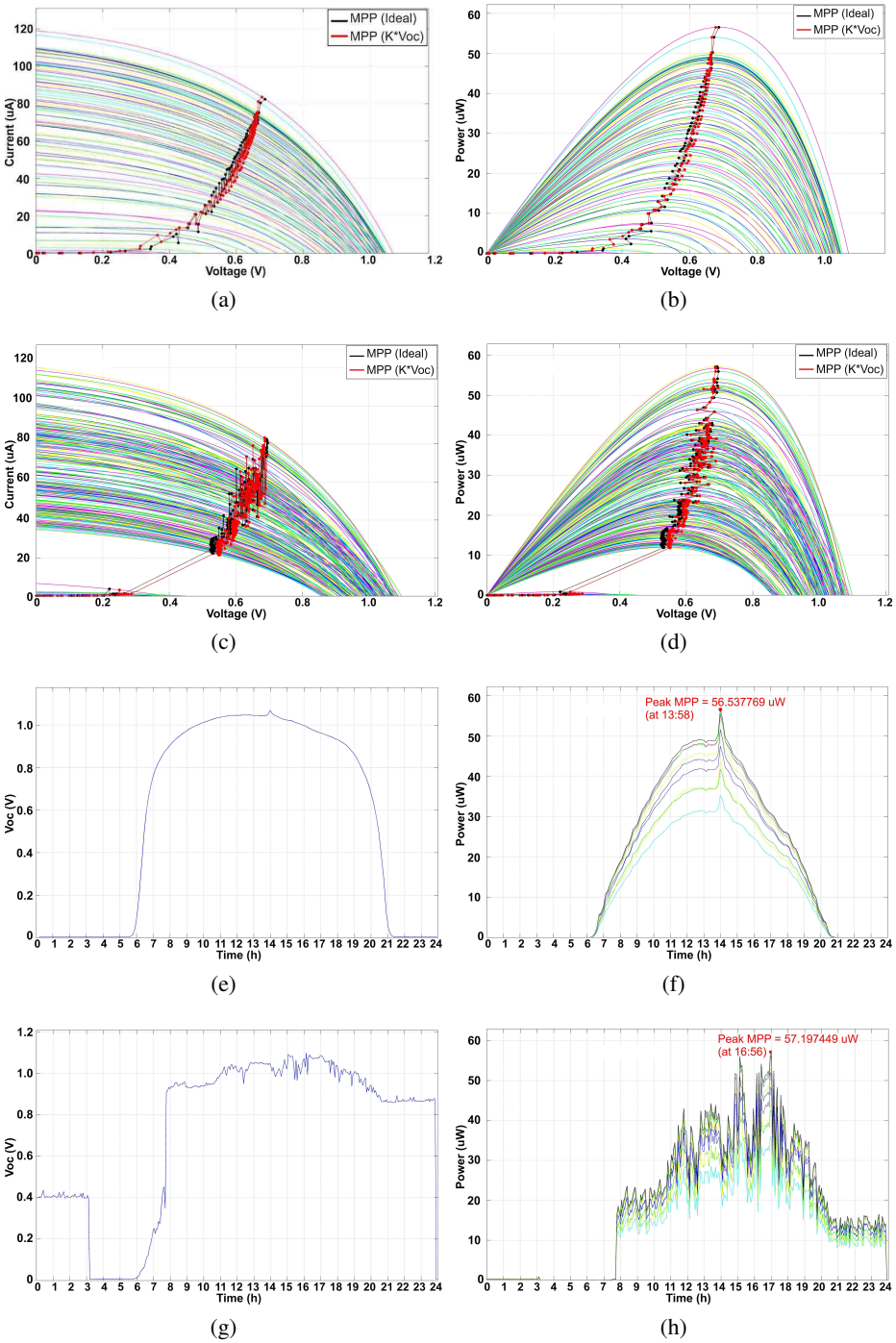
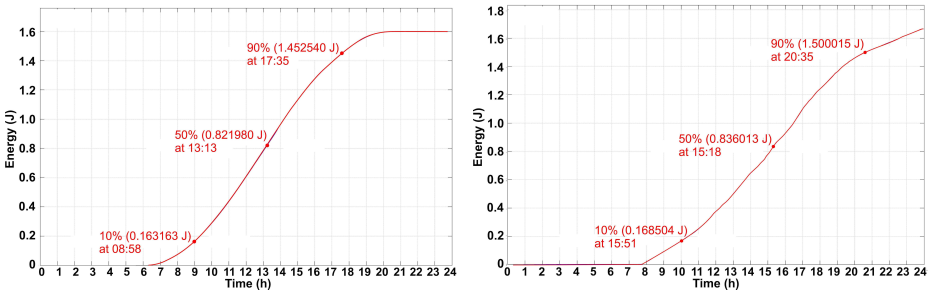


Figure 3.5: V_{OC} and MPP time variation for the IXYS SLMD121H04L PV cell on 24-05-2015 and 11-05-2015 (refer to Section 3.2) – (a) *I-V* and (b) *P-V* illustrate 24-05-2015; (c) *I-V* and (d) *P-V* illustrate 11-05-2015; (e) $V_{OC}(t)$ and (f) MPP(t) illustrate 24-05-2015; (g) $V_{OC}(t)$ and (h) MPP(t) illustrate 11-05-2015.

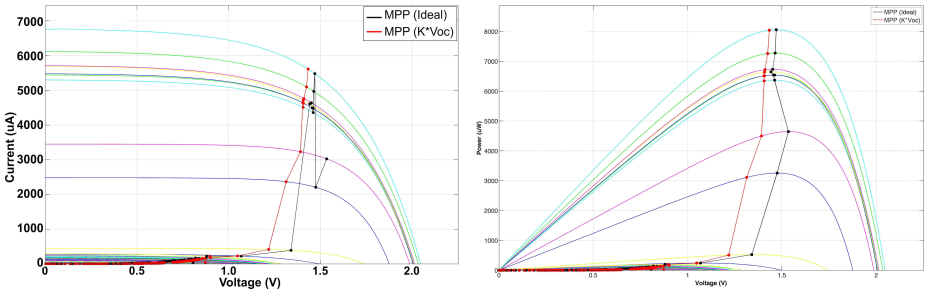
On Figure 3.6 the energy accumulation during a day as well as the instants at which the energy is at 10%, 50% and 90% of its final value, are illustrated.



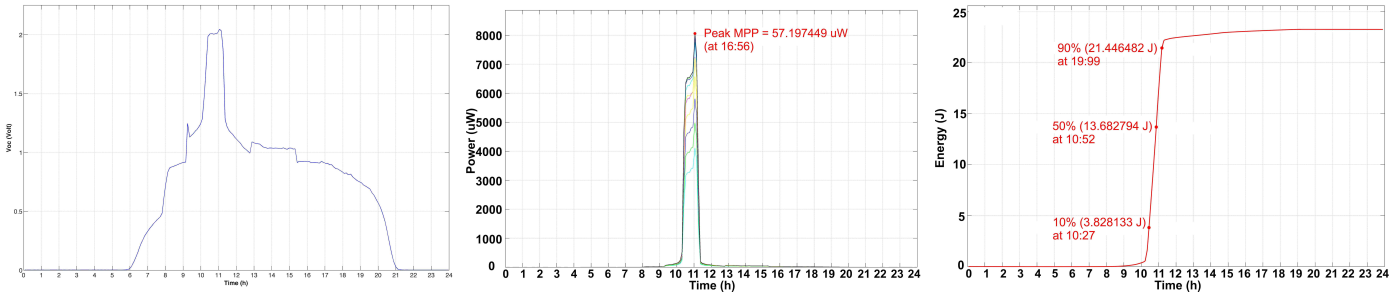
(a) (b)

Figure 3.6: Energy conversion during a day for the IXYS SLMD121H04L PV cell on 24-05-2015 and 11-05-2015 (refer to Section 3.2) – (a) 24-05-2015 and (b) 11-05-2015.

Figures 3.7c, 3.7d and 3.7e depict the operation of the PV cell when subject to direct sunlight, as a reference for comparison – data acquired on 19-05-2015 for the IXYS SLMD121H04L PV cell model. It is noticeable that the PV cell was subject to direct sunlight int a time interval roughly between 10h and 12h.



(a) (b)



(c) (d) (e)

Figure 3.7: Characterisation of the IXYS SLMD121H04L PV cell on 19-05-2015 (refer to Section 3.2) – (a) *I-V*; (b) *P-V*; (c) $V_{OC}(t)$; (d) MPP(t); (e) Energy conversion on 19-05-2015.

The black markers on Figures 3.5a, 3.5b, 3.5c and 3.5d connect the points at which the PV cell output power is maximum, for a given characteristic. The red markers signal the operation point at a fraction of the open circuit voltage – the relevance of this information will be explained in

Chapter 4. On Figures 3.5f and 3.5h, the black line depicts the time variation of the maximum PV output power. The coloured lines depict the PV output power for several operation points given by different fractions of the open circuit voltage. Once more, the relevance of this information will be explained in Chapter 4.

Under indoor environments, there is no direct sunlight hitting the PV cell. The PV cell receives only indirect sunlight, and the most dominant light source is the artificial light, namely from fluorescent lamps. This is why the open circuit voltage remains roughly constant during the working hours of a typical office day. This is also supported by the fact that the V_{OC} time variation is quite similar between a sunny day (24-05-2015) and a cloudy one (11-05-2015). This also results in the similarity between the *I-V* and *P-V* curves which characterise the operation of the PV cell on these days.

Figure 3.5 shows that when the cell operates in an indoor environment, the energy accumulation is spread over the day, as the V_{OC} remains roughly constant thus providing a relatively constant energy flow.

On the other hand, if the PV cell receives direct sunlight, its output increases dramatically, as seen in Figure 3.7. In this case, even though the PV cell is under direct sunlight for a small interval of time, the energy output increases more than tenfold. It is also noticeable the V_{OC} increase during that time, as well as the output current (and voltage). The energy accumulation during the day draws a much more steep characteristic – Figure 3.7e.

Nevertheless, when it comes to indoor environments – i.e. no direct sunlight – the artificial light becomes the dominant energy source and dictates the operation of the PV cell. The operation under these conditions is, as seen in this chapter, approximately constant and the PV output power – in the order of the dozens of *uW* – is kept relatively steady during the operation time which is coincident with the working hours of a typical indoor environment.

3.3.2 Input Capacitance Characterisation

In order to get acquainted with the input capacitance of the PV cells in use, a simple method was used: a square wave was applied to the terminals of each one of the PV cells listed in Subsection 3.2.3, through a series resistance, and the signal at the PV terminals was probed to determine the rise time. The rise time, in turn, would yield the PV cell capacitance. The latter was obtained through (3.1)

$$C_{PV} = \frac{t_R}{0.35 \times 2 \times \pi \times R} \tag{3.1}$$

where t_R is the rise time and R the series resistance used in the test.

Each one of the PV cells was tested using three series resistances of different values – 1 kΩ, 10 kΩ and 22 kΩ and the cell surface was covered in order to ensure that it received no radiation thus interfering with the test. The results of these tests are summarised in Table 3.3 and the analysed waveforms can be seen in Appendix C.

Table 3.3: PV cell capacitance measurements. These were obtained through the method illustrated in Appendix C.

PV Model	R (KΩ)	Rise Time (μs)	Capacitance (nF)	A (cm^2)	nF/cm^2
IXYS SLMD121H04L	1	4.150	1.8871	6.0200	0.3135
	10	22.80	1.0368		0.1722
	22	54.00	1.1162		0.1854
CYMBET CBC-PV-01N	1	189.3	86.080	32.9427	2.6130
	10	1520	69.119		2.0982
	22	4133	85.427		2.5932
Amorton AM-1454CA	1	35.53	16.157	10.9539	1.4750
	10	278.0	12.641		1.1540
	22	524.0	10.831		0.9888
Amorton AM-1417CA	1	11.32	5.1475	4.8719	1.0566
	10	92.80	4.2199		0.8662
	22	182.0	3.7618		0.7721

The analysis made on the capacitance of the PV cells revealed the existence of parasitic capacitance values per area unit that vary between 0.7721 nF / cm^2 and 2.6130 nF / cm^2 for the amorphous silicon cells and from 0.1854 nF to 0.3155 nF for the monocrystalline silicon cell – Table 3.3. These values are in the same proportion as others presented in the literature. In [73] for example, a 16 cm^2 amorphous silicon cell is presented, which has a capacitance of 72.45 nF. This value is comparable with the 86.080 nF displayed by the 32.9427 cm^2 CYMBET CBC-PV-01N model.

3.3.3 Energy Feasibility Considerations

This Subsection aims to provide insight on the energy context on which an hypothetical system, subject to indoor environment conditions and using a PV cell as energy transducer, would operate.

Based on the data acquired through the method detailed on Subsection 3.1, the energy accumulation profile, during a day, behaves as depicted in Figure 3.8. There is an *active* period when the illuminance is kept high enough for the PV cell to convert energy. Usually, in a typical office environment, this *active* time period is coincident with the work hours, and the light source is the artificial light which is on, during that time.

A PV energy based system would mainly have to deal with two issues related to the conveyed energy: the required startup energy of that system, and the operation consumption.

Figure 3.9 illustrates the effect of these two factors on the energy profile. A startup energy requirement would translate in a delayed start on the energy accumulation, as the system would have to first gather enough energy to start and only then would it be able to harvest energy for other purposes. This is illustrated as the blue period of time on Figure 3.9. On the other hand, an energy consumption constraint would mean a less steep energy profile – illustrated as the blue line on Figure 3.9 – as part of the converted energy would be to power the system itself – the latter constraint, in this study, is assumed to be constant, to mimmic the effects of a load drawing a steady flow of energy, or a system operating in steady state.

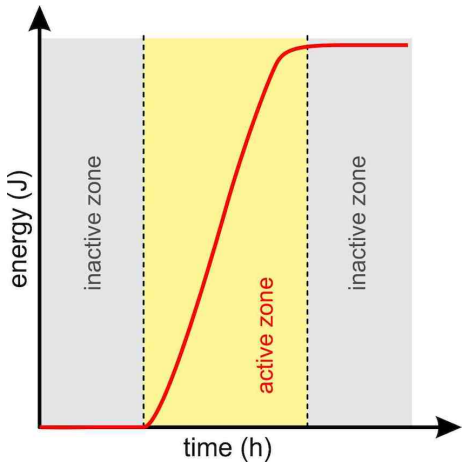


Figure 3.8: Typical energy accumulation profile during a day. The grey areas, labeled as inactive areas, illustrate the time intervals when there is no energy being converted due to low illuminance. The yellow area illustrates the time interval when the illuminance is sufficient for the PV cell to convert energy.

When designing a system to operate under these conditions, these constraints must be taken into account such that: (1) the startup energy must be inferior to the maximum energy converted during the *active* period of the PV cell, otherwise the system would enter the *inactive* time period without gathering enough energy to start and thus, would never work; (2) the energy consumption must be such that, when the system is operating in the *inactive* region, the available energy is never depleted leading to a power down. As a limit, the energy consumption must be, at most, one that causes the stored energy to be depleted precisely when entering the next *active* region.

This extreme situation is depicted in Figure 3.9, as the blue solid line. An higher consumption would lead to a power down – the dashed line interrupted at the X axis – and a lower consumption would allow a surplus of energy on the next day – the dashed line above the solid blue line.

Considering both constraints and aiming for an uninterrupted operation, it stands to reason that the higher the startup energy required, the lower the available energy at the end of the *active* time, thus the lower must be the maximum consumption of the system.

This analysis was made on the energy profiles acquired during the PV cell characterisation process, in order to gain further insight on the indoor energy context. For each energy profile, the energy accumulation curve – refer to Figure 3.10a – was extended, describing a 48 hours energy profile, as two similar consecutive days would yield. Then, an algorithm was used to find the maximum possible consumption, taking into account different startup energy requirements, which allows non stoping operation. The results for the IXYS SLMD121H04L PV cell model on 2015-05-22 are depicted on Figure 3.10b. As the lines change from red to blue – i.e. the startup energy requirement is increased – the maximum energy consumption – i.e. the curve slope – lowers. Plotting the startup energy consumption against the maximum consumption energy yields the *feasibility* curve, illustrated in Figure 3.10c. All the data for the other PV cells, and the other days can be consulted in Appendix D.

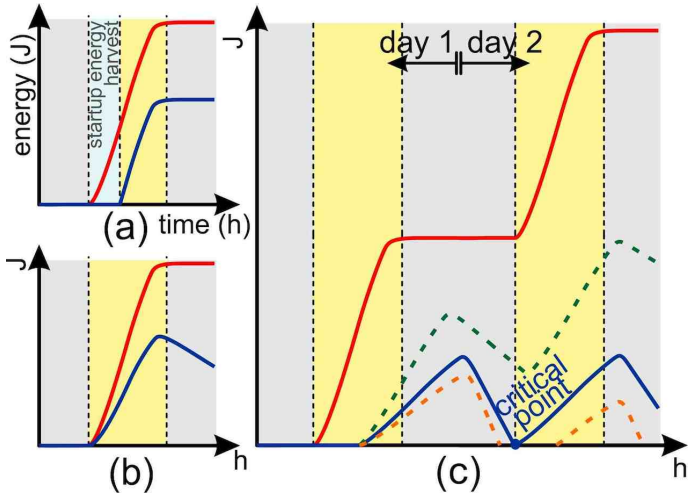
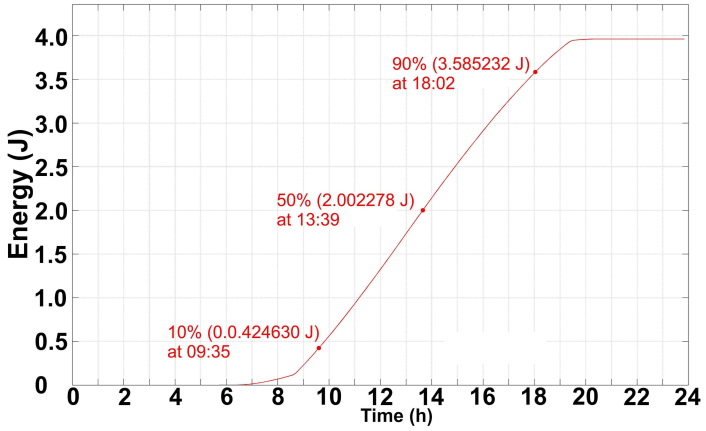
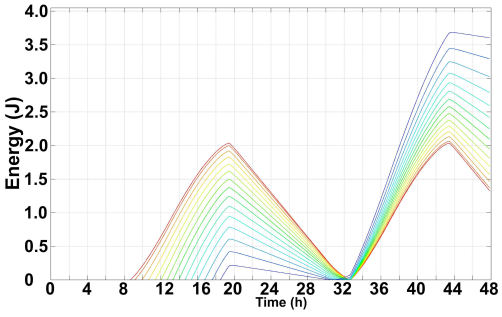


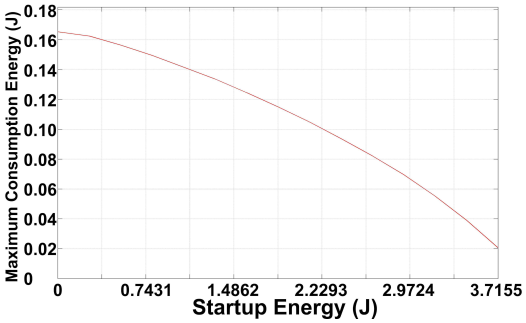
Figure 3.9: Effect of the startup energy or the energy consumption on the PV energy profile – (a) Startup energy constraint; (b) Energy consumption constraint; (c) Both energy constraints.



(a)



(b)



(c)

Figure 3.10: Energy feasibility of the IXYS SLMD121H04L model on 2015-05-22, at SilliconGate – (a) Energy accumulation profile; (b) Energy consumption *versus* startup energy; (c) Energy feasibility.

As previously described, the higher the startup energy, the lower must the maximum energy consumption be. The energy consumption *versus* startup energy points of all the tested PV cells, during all the sensed operation days were gathered in a scatter plot, which can be seen in Figure 3.11, under several levels of zoom.

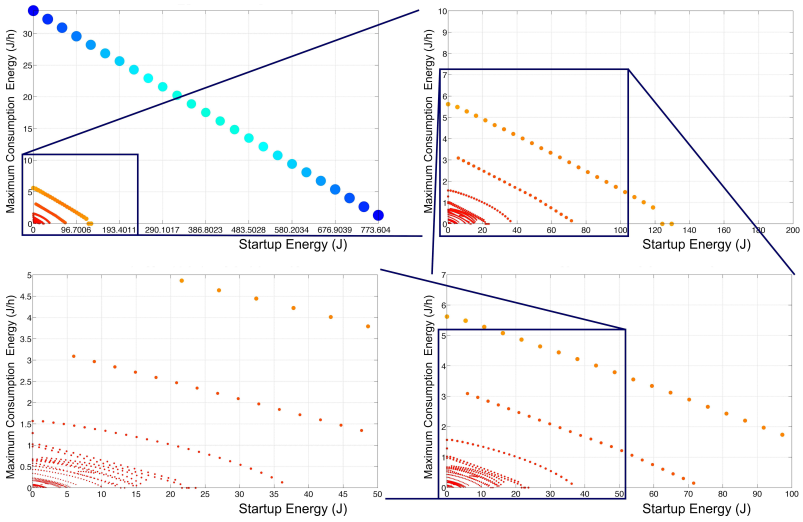


Figure 3.11: Scatter plot of startup energy *versus* maximum consumption.

The farther points from origin illustrate the values for a PV cell under direct sunlight and will thus be interpreted as outliers, regarding indoor lighting environments. Under this assumption, this sensibility analysis illustrates that the vast majority of points lies in a region which describes a startup energy under 100 J and a maximum consumption energy of 5 J/h.

Considering the maximum consumption energy of 5 J/h or, in another terms, $5/3600$ W, a power limit estimation of 1.4 mW is obtained for a system under these conditions. This estimate can be used to infer on the power constraints of an indoor PV based system. As an example, a system which keeps the output at a voltage of 3.3 V, would allow a load current up to approximately 0.42 mA. On the other hand, an hypothetical load drawing, for example, 0.22 mA, kept at the same 3.3 V would allow a surplus of 0.66 mW to be stored.

3.4 Practical Photovoltaic Cell Modelling for Simulation

In order to approach a system in which the PV cell is the energy source, it is useful to make use of models of these devices, in order to allow their analysis in simulation environment. The alternative would be to use physical devices. This, however, limits the range of the study to a specific model and quickly becomes an unpractical approach should one feel the need to vary the conditions of simulation, and the characteristics of the source.

There are several models detailed in literature to model the PV cell behaviour. The most commonly used is the simple current source-diode-parallel resistance-series resistance model – refer to Figure 2.1b. This model is used several times throughout this work, as it models a PV cell

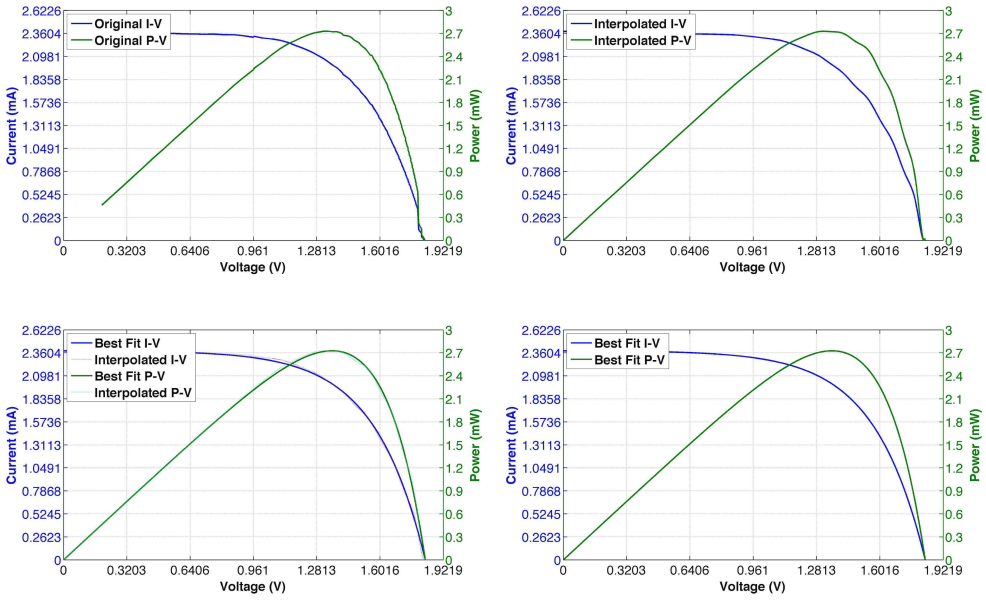


Figure 3.12: PV cell *I-V* curve fitting algorithm.

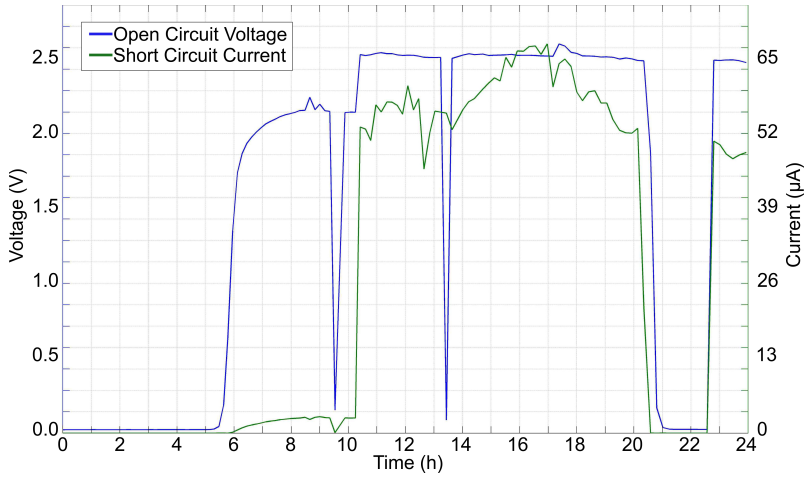
with a simple circuit. Despite its simplicity, it suffers from the advantage of being limited to the electrical characteristics of the components chosen for the circuit and the cumbersome process of parametrising a feasible set of components to accurately describe a specific model.

There are also several behavioural models reported in literature which program the circuit equations of these models – obtained through simple circuit analysis techniques – and use this behavioural descriptions in simulating environments to achieve trustworthy results. This work proposes, however, a characterisation method that, based on the *real I-V* curves of the PV cell, runs a simple curve fitting algorithm that uses (3.2)

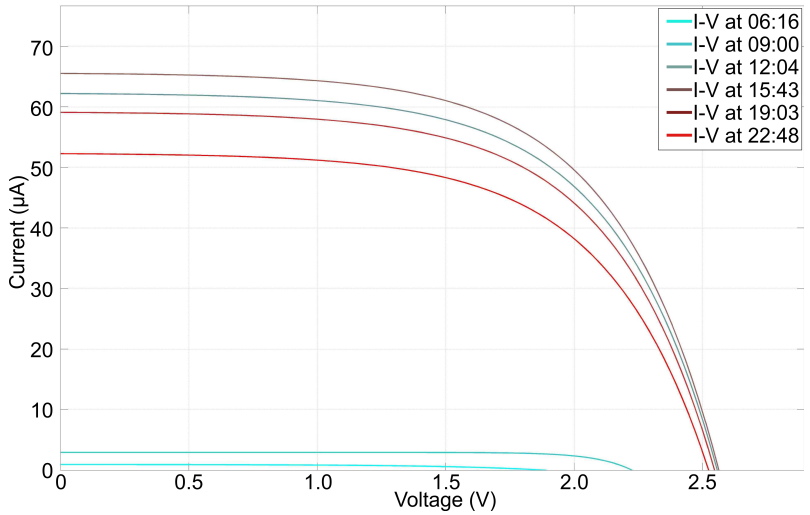
$$I_{PV,model} = \frac{ISC}{1 - e^{\frac{VOC}{A}}} \times (1 - e^{\frac{V_{PV} - V_{VOC}}{A}}) \tag{3.2}$$

to mimmic the *I-V* curve of the PV cell to be modelled.

ISC, VOC and V_{PV} are, respectively, the short circuit current, open circuit voltage and the voltage ate the PV cell terminals. The first two parameters are immediately known through observation of the *real I-V* curve as VOC is the voltage at which the output current is zero and ISC the current for which the output voltage is zero. V_{PV} is the output voltage, which is swept to obtain the points that characterise the curve. A is the parameter that controls the shape of the curve. It is swept between 0 and 1, to find the curve that best describes the PV cell. This algorithm aims to find the value for A which minimises both the mean square error and the model (V_{MPP}, I_{MPP}) coordinate error.



(a)



(b)

Figure 3.13: (a) V_{OC} and I_{SC} variation for the Amorton AM-1417 PV cell model on 2015-05-26. (b) PV cell modelling of the Amorton AM-1417 behaviour on 2015-05-26, through (3.2).

This is a method that results in a practical equation which can be easily used for simulation as it has only an unknown parameter, A, to be found. Figure 3.12 depicts the algorithm outcome.

The algorithm has yet another convenient use which is the ability to easily characterise the time varying operation of a PV cell, as each measurement of the I-V curve, for a given moment in time and under specific meteorological conditions, can be easily expressed in terms of the parameters ISC, VOC and A, as shown in Figure 3.13b. These three parameters, for the example provided, varied as depicted in Figure 3.13a. Appendix E contains a simple verilog-A PV cell model using (3.2).

3.5 Conclusions to This Chapter

In this chapter, four PV cell models were studied under the scope of indoor operation. A test platform was developed to programmatically bias and measure the electrical parameters of a PV cell.

Under indoor environments there is no direct sunlight hitting the PV cell, being artificial light the dominant light source. This leads to a lighting environment roughly stable during the time these lights remain lit, which reflects of the output of the PV cell that becomes also approximately constant during that time. Moreover, being artificial light the dominant light source, the differences between sunny days and cloudy ones is reduced, in terms of energy output of the PV cell.

It is also observable that the output power of the PV cells, in indoor environments, is in the μW order, which is about a thousand times lower than the output reported in the datasheets for outdoor operation.

This chapter also concludes the existence of a parasitic capacitance of the PV cells which vary between approximately $0.1854\,\text{nF}\,/\,cm^2$ and $2.6130\,\text{nF}\,/\,cm^2$ being the capacitance of the monocrystalline silicon cell considerably lower than the reported values for the amorphous silicon models.

An analysis on the energy context of the tested indoor environments was made, which states that indoor lighting environments, when using PV cells similar to those described in Subsection 3.2.3, yield power levels roughly in the order of hundreds of microwatt to a few milliwatt. Subsection 3.3.3 takes 1.4 mW as a rough estimate of the power context of indoor environments. Of course, subject to the use of PV cells such as those tested.

A practical behaviour model of the PV cell was developed in this chapter. It conveys a practical approach to the PV cell behaviour as it mimics the PV cell *I-V* curve using only 3 variables – V_{OC}, I_{SC} and A, a fitting parameter. This practical approach allows the quick modelling of "real" data concerning the PV cell operation, into a form suited form simulation.

Chapter 4

Power Conditioning

This chapter aims to study the power conditioning stage of the energy harvesting system. Specifically the goals for this chapter are:

- Development of a mathematical model for the SC DC/DC parallel-series voltage doubler and subsequent validation through simulation;
- Study the influence of the electrical components of the system in order do choose their values;
- Transition to a generic model of the parallel-series converter for arbitrary conversion ratios, using the approach presented in [68].

To study this mater, a switched capacitor DC/DC converter was chosen as the subject of analysis, due to the advantages discussed on Section 2.2. Specifically, the parallel-series SC DC/DC converter topology was chosen. According to Seeman, on [68], the parallel-series topology – refer to Figure 2.8, which depicts the one-stage parallel-series converter, i.e. a voltage doubler – performs the best in the SSL operation regime – when the frequency is low enough to allow complete charge transfer between the capacitors of the circuit, refer to Subsection 2.2.1. As this system has the energy efficiency as a paramount aspect to take into account, the need to slow the switching frequency to decrease energy consumption may arise. Henceforth, this parallel-series SC DC/DC converter was chosen. Additionally, it provides a topology easy to understand. In half the operation period the flying capacitors are charged in parallel with the energy source. On the other half period the flying capacitors constitute a series path between the input and the output, thus shuttling the charge from the source to the load.

On Section 4.1 the deduction of a mathematical model of the parallel-series voltage doubler will be made and validated through simulation. Afterwards, on Section 4.2, the performance of the SC DC/DC converter will be analysed, using the previously derived converter model. Section 4.3.1 will then make use of a generic parallel-series converter model, to study its operation for arbitrary ratios. The objective is to gain some insight on how the DC/DC converter behaves,

when manipulating its components, varying the switching frequency and integrating with different sources and loads, in order to choose its components and understand how it behaves in distinct contexts. All simulations and validations were performed in Matlab [26] and Spectre [27].

4.1 SC DC/DC Parallel-Series Voltage Doubler Mathematical Model

The operation of an SC DC/DC converter depends on several variables. To gain an overall insight on how this circuit behaves under changing conditions, a mathematical model for the voltage doubler depicted in Figure 4.1 was deducted, using standard nodal analysis of the circuit to derive the time-domain equations for each switching phase.

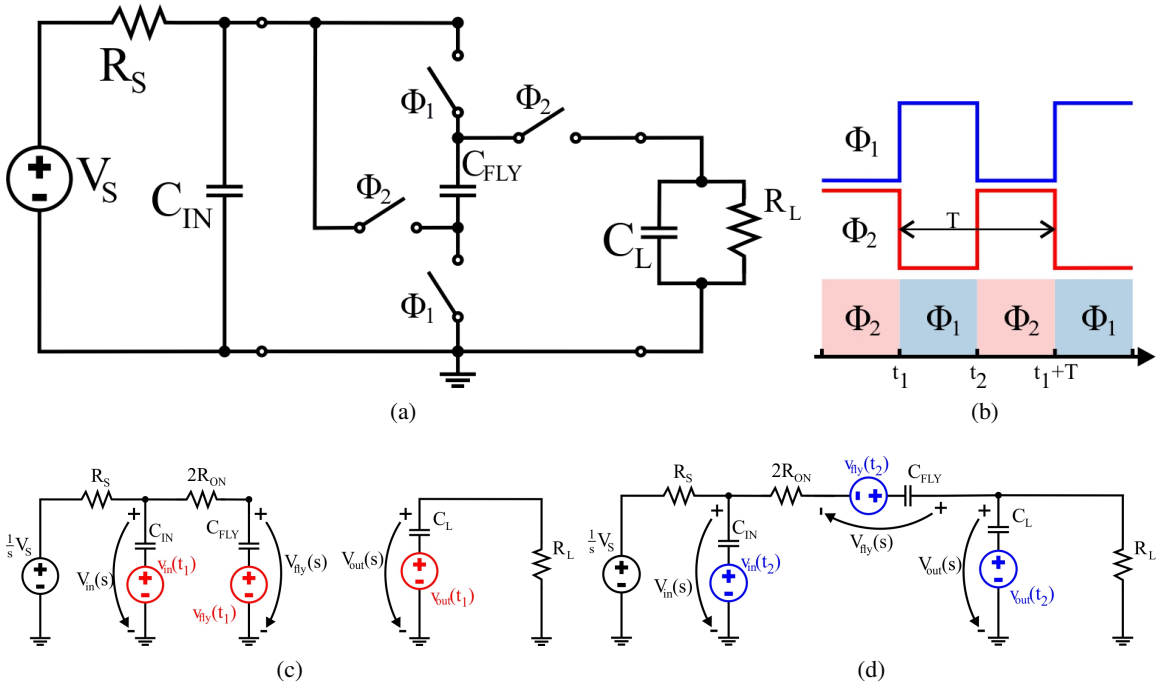


Figure 4.1: (a) Parallel-Series Voltage Doubler circuit; (b) Switching phases and signals; (c) Equivalent circuit for phase 1; (d) equivalent circuit for phase 2.

Signals Φ_1 and Φ_2, illustrated in Figure 4.1b, define the operation phases, when $t \in]t_1, t_2]$ and $t \in]t_2, t_1 + T]$, where T stands for the fundamental period. On Figure 4.1a, the switches are signalled with either Φ_1 or Φ_2, which means that the switch is closed – i.e. in the ON state – during that phase. Figures 4.1c and 4.1d illustrate the equivalent circuits for Φ_1 and Φ_2, where the coloured voltages sources signal the voltage at that node immediately after that phase starts. These will be used to define the boundary conditions when changing switching phase. The $2R_{ON}$ resistors represent the switch resistance when closed. The net has two switches closed on each phase, which were merged in a single resistor for simplicity sake.

Let us use the Laplace transform and its inverse to derive the time-domain equations for Φ_1 and Φ_2, of the three noteworthy signals in the circuit – $v_{in}(t)$, $v_{fly}(t)$ and $v_{out}(t)$. The notation

${V_{node}}^{phase}(s)$ will be used, where *node* identifies the node *in*, fly or *out* where that voltage is felt and *phase* denotes the phase Φ_1 or Φ_2 of the signal.

Using nodal analysis on the circuit in Figure 4.1c, the following relations can be found:

$$\frac{1}{R_S}\left[\frac{V_S}{s} - {V_{in}}^{\Phi_1}(s)\right] - C_{IN}\left[s{V_{in}}^{\Phi_1}(s) - {v_{in}}^{\Phi_1}(t_1)\right] + \frac{{V_{fly}}^{\Phi_1}(s) - {V_{in}}^{\Phi_1}(s)}{2R_{ON}} = 0 \tag{4.1}$$

for the node at the top plate of the C_{IN}. From the current flowing through C_{FLY}, one can write

$$C_{FLY}\left[s{V_{fly}}^{\Phi_1}(s) - {v_{fly}}^{\Phi_1}(t_1)\right] - \frac{{V_{in}}^{\Phi_1}(s) - {V_{fly}}^{\Phi_1}(s)}{2R_{ON}} = 0 \tag{4.2}$$

and finally, analysing the node at the top plate of the C_L yields

$$\frac{{V_{out}}^{\Phi_1}(s)}{R_L} + C_L\left[s{V_{out}}^{\Phi_1}(s) - {v_{out}}^{\Phi_1}(t_1)\right] = 0 \tag{4.3}$$

Similarly, for Φ_2, depicted in Figure 4.1d, one can write:

$$\frac{1}{R_S}\left[\frac{V_S}{s} - {V_{in}}^{\Phi_2}(s)\right] - C_{IN}\left[s{V_{in}}^{\Phi_2}(s) - {v_{in}}^{\Phi_2}(t_2)\right] + \frac{{V_{out}}^{\Phi_2}(s) - {V_{fly}}^{\Phi_2}(s) - {V_{in}}^{\Phi_2}(s)}{2R_{ON}} = 0 \tag{4.4}$$

$$\frac{{V_{out}}^{\Phi_2}(s) - {V_{fly}}^{\Phi_2}(s) - {V_{in}}^{\Phi_2}(s)}{2R_{ON}} - C_{FLY}\left[s{V_{fly}}^{\Phi_2}(s) - {v_{fly}}^{\Phi_2}(t_2)\right] = 0 \tag{4.5}$$

$$\frac{{V_{out}}^{\Phi_2}(s)}{R_L} + C_L\left[s{V_{out}}^{\Phi_2}(s) - {v_{out}}^{\Phi_2}(t_2)\right] + \frac{{V_{out}}^{\Phi_2}(s) - {V_{fly}}^{\Phi_2}(s) - {V_{in}}^{\Phi_2}(s)}{2R_{ON}} = 0 \tag{4.6}$$

Applying the inverse Laplace transform to (4.1 - 4.3) and (4.4 - 4.6) yields, the time-domain equations of $v_{in}(t)$, $v_{fly}(t)$ and $v_{out}(t)$, for phases Φ_1 and Φ_2. Their computation is quite complex and their form is rather lengthy, henceforth they are not presented here. The Matlab script used to get to these equations can be seen in Appendix F. Given the fact that the component values and the sources are constants known at this point, it suffices to state that

$${v_{in}}^{\Phi_1}(t) = f_1\left(t, {v_{in}}^{\Phi_1}(t_1), {v_{fly}}^{\Phi_1}(t_1)\right) \tag{4.7}$$

$${v_{fly}}^{\Phi_1}(t) = f_2\left(t, {v_{in}}^{\Phi_1}(t_1), {v_{fly}}^{\Phi_1}(t_1)\right) \tag{4.8}$$

$${v_{out}}^{\Phi_1}(t) = f_3\left(t, {v_{out}}^{\Phi_1}(t_1)\right) \tag{4.9}$$

and

$$v_{in}{}^{\Phi_2}(t) = g_1\big(t, v_{in}{}^{\Phi_2}(t_2), v_{fly}{}^{\Phi_2}(t_2), v_{out}{}^{\Phi_2}(t_2)\big) \tag{4.10}$$
$$v_{fly}{}^{\Phi_2}(t) = g_2\big(t, v_{in}{}^{\Phi_2}(t_2), v_{fly}{}^{\Phi_2}(t_2), v_{out}{}^{\Phi_2}(t_2)\big) \tag{4.11}$$
$$v_{out}{}^{\Phi_2}(t) = g_3\big(t, v_{in}{}^{\Phi_2}(t_2), v_{fly}{}^{\Phi_2}(t_2), v_{out}{}^{\Phi_2}(t_2)\big) \tag{4.12}$$

Without loss of generality, let us define as reference, in steady state, that $t_1 = 0$ and $t_2 = \frac{T}{2}$. Due to boundary conditions, a steady state periodic solution exists for $t = t_1 = 0$

$$v_{in}{}^{\Phi_1}(t_1) = v_{in}{}^{\Phi_1}(0^+) = v_{in}{}^{\Phi_1}(T^-) \tag{4.13}$$
$$v_{fly}{}^{\Phi_1}(t_1) = v_{fly}{}^{\Phi_1}(0^+) = v_{fly}{}^{\Phi_1}(T^-) \tag{4.14}$$
$$v_{out}{}^{\Phi_1}(t_1) = v_{out}{}^{\Phi_1}(0^+) = v_{out}{}^{\Phi_1}(T^-) \tag{4.15}$$

and, similarly for $t = t_2 = \frac{T}{2}$

$$v_{in}{}^{\Phi_2}(t_2) = v_{in}{}^{\Phi_2}(\frac{1}{2}T^-) = v_{in}{}^{\Phi_2}(\frac{1}{2}T^+) \tag{4.16}$$
$$v_{fly}{}^{\Phi_2}(t_2) = v_{fly}{}^{\Phi_2}(\frac{1}{2}T^-) = v_{fly}{}^{\Phi_2}(\frac{1}{2}T^+) \tag{4.17}$$
$$v_{out}{}^{\Phi_2}(t_2) = v_{out}{}^{\Phi_2}(\frac{1}{2}T^-) = v_{out}{}^{\Phi_2}(\frac{1}{2}T^+) \tag{4.18}$$

thus obtaining a mathematical model of the time domain behaviour of the DC/DC converter.

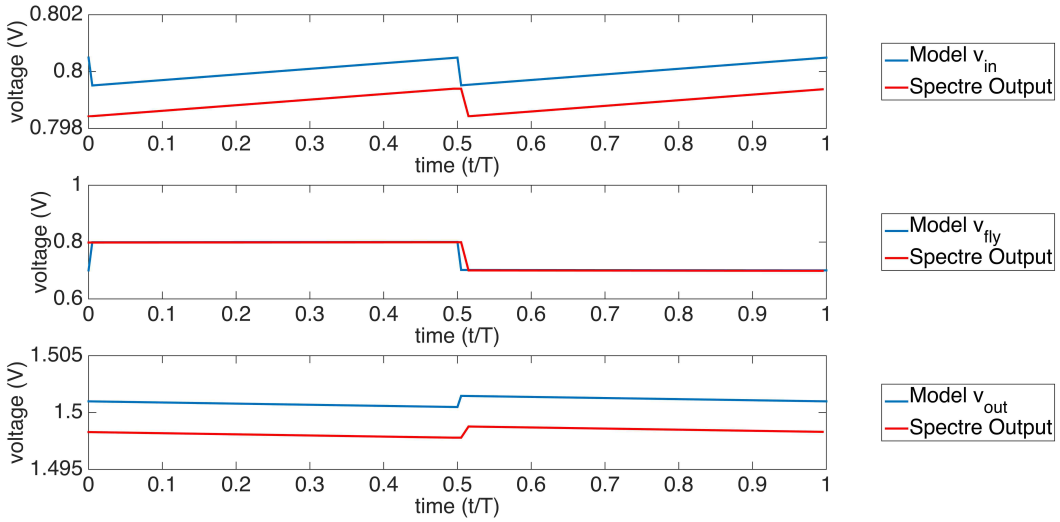


Figure 4.2: Voltage doubler mathematical model outputs and comparison with the results obtained from the simulation of the same circuit in Spectre.

Figure 4.2 depicts the output from this model superimposed to the Spectre output of the same circuit. The parameters for the illustrated comparison are $V_S = 1\,\text{V}$, $R_S = 10\,\text{k}\Omega$, $C_{IN} = 100\,\text{nF}$, $C_{FLY} = 1\,\text{nF}$, $R_{ON} = 1\,\Omega$, $C_L = 100\,\text{nF}$, $R_L = 40\,\text{k}\Omega$ and $f = 1/T = 100\,\text{kHz}$. One can observe that this mathematical approach yields results quite accurate when compared with the results obtained through simulation. The time domain behaviour predicted by the model was then compared to the simulation output of the same circuit in Spectre, in order to validate its usability. This test was done for several different sets of circuit parameter and the maximum error found was of approximately 4 mV of difference between the results of the mathematical model and the simulation output, for $V_S = 1\,\text{V}$. Henceforth, this model will be used to study the performance of the converter.

next section will make use of this model to analyse the operation of the converter.

4.2 Converter Performance Analysis

The operation of the converter depends on the electrical components, the switching frequency and the input-output context in which the converter is deployed. These are the variables that affect its operation. In order to gain insight on their influence and choose feasible values for them, the mathematical model developed in the previous chapter will be used to sweep these variables and analyse their influence.

4.2.1 The Flying Capacitor

The flying capacitor is the component responsible for shuttling the power from the source to the load. It is charged in parallel with the source during one of the switching phases and discharged to the load in the other phase, as it is put in series with the source and the load – refer to Figure 4.1.

The flying capacitor value was swept from 1 pF to 10 nF, for different switching frequencies ranging from 1 kHZ to 500 kHz. The parameters used for this analysis are $V_S = 1\,\text{V}$, $R_S = 10\,\text{k}\Omega$, $C_{IN} = 100\,\text{nF}$, $R_{ON} = 1\,\Omega$, $C_L = 100\,\text{nF}$ and $R_L = 40\,\text{k}\Omega$. The results correspond to average values over one switching period, in steady state operation.

Considering a constant frequency, the overall efficiency of the converter increases with the size of the flying capacitor. The VCR of the conversion block approximates the ideal value, in this case 2, as observable from Figures 4.3d and 4.3e. Similarly, according to Figures 4.3b and 4.3c, the power delivered to the load approximates the value of the power extracted from the source. This means that the losses during the conversion process decrease with the size of the flying capacitor.

Simultaneously, for a constant value of the flying capacitor, an increase of the frequency increases the performance of the conversion as seen in Figure 4.3a.

There is a tradeoff that must be taken into account. In Figure 4.3a, one can see that, for the same frequency, the size of the flying capacitor must be increased in order to achieve better performances. On the other hand, if there are restrictions on area, then the reduction of the flying capacitor value must be compensated with an increase on frequency, to keep the efficiency from falling.

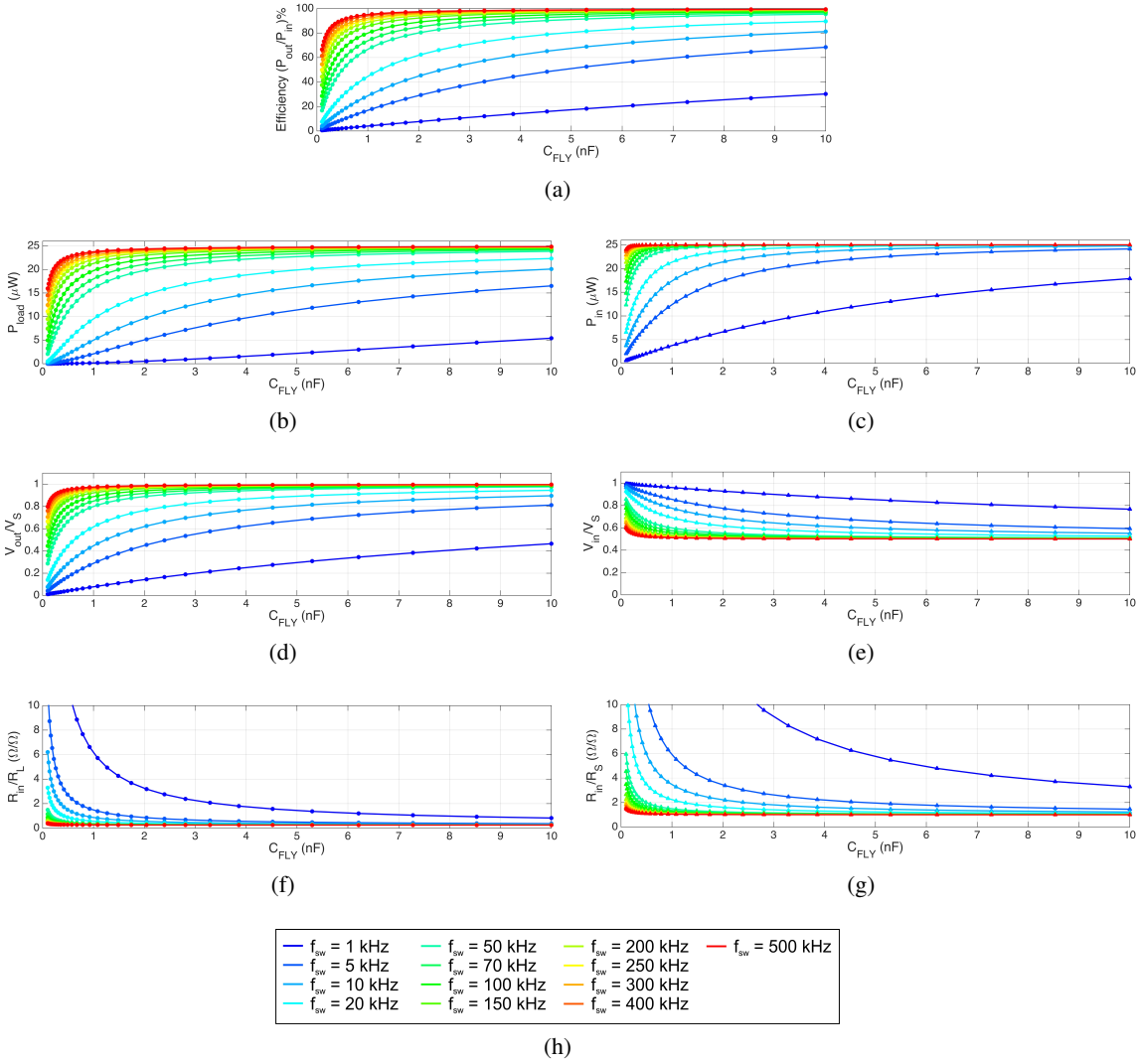


Figure 4.3: Voltage doubler performance with flying capacitance at different switching frequencies. The results obtained to plot these curves were averaged over the switching period when in steady state. (a) Efficiency – $\frac{P_{load}}{P_{in}}$; (b) Load power; (c) Input power; (d) Output voltage, normalised by the source voltage; (e) Input voltage, normalised by the source voltage; (f) Input resistance, normalised by the load resistance; (g) Input resistance, normalised by the source resistance; (g) Analysed frequency range.

The input resistance is a particular aspect to consider. As seen in Figures 4.3f and 4.3g, smaller flying capacitance values require a higher frequency in order to keep the input resistance of the converter bellow unfeasible values. For example, a 1 pF flying capacitor, switched at 50 kHz would yield an input resistance about six times higher than the source resistance, whereas for a 10 nF flying capacitor being switched at the same frequency, the input resistance is already approximately at its lowest value for the analysed range.

The influence of the flying capacitor is always relative to the frequency at which it is being switched. Figure 4.3 portrays the influence of the flying capacitor for distinct values of the switching frequency. An equivalent analysis would be to sweep the switching frequency for distinct values of the flying capacitor. For convenience, Figure 4.4 illustrates that equivalent analysis.

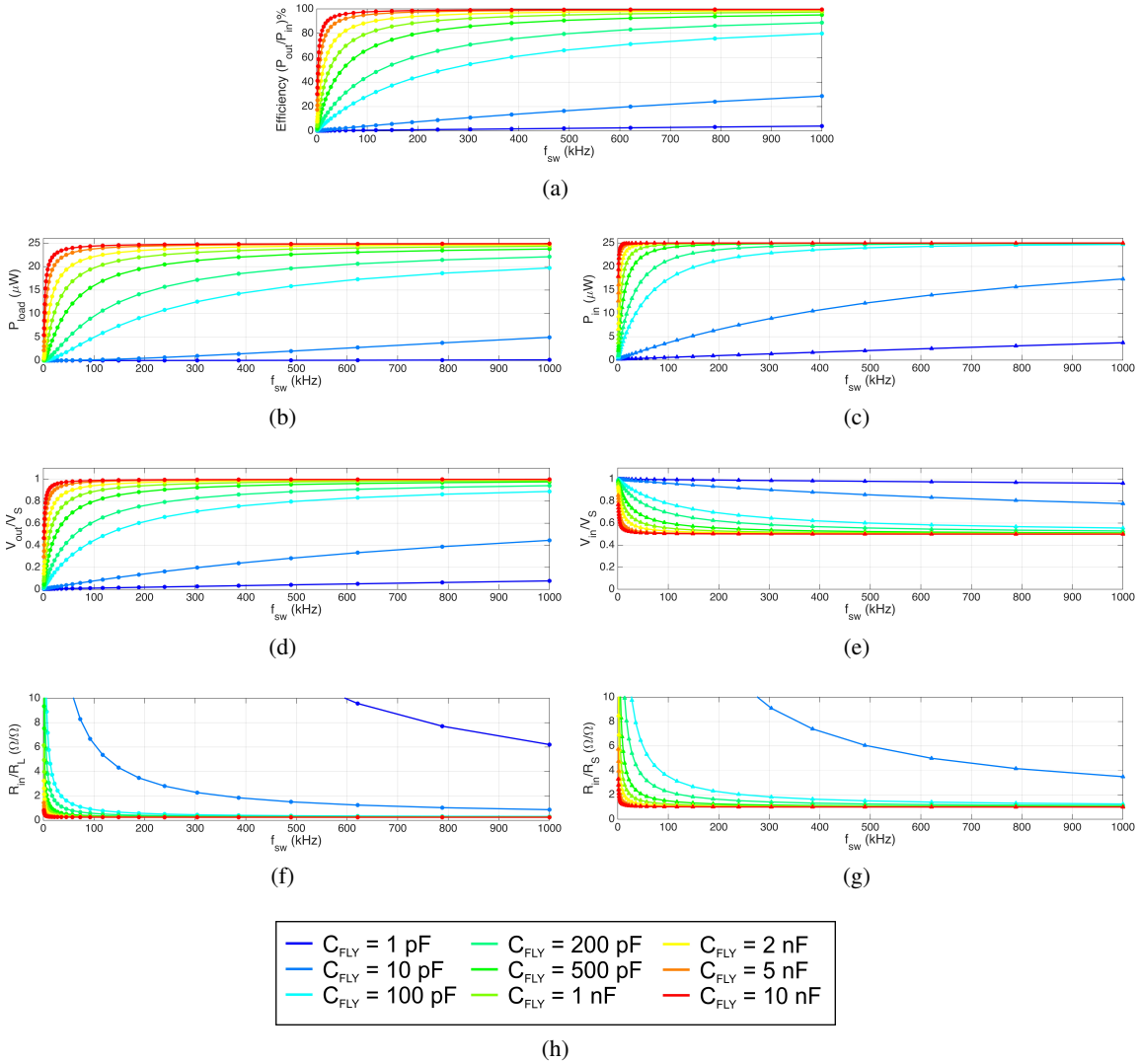


Figure 4.4: Voltage doubler performance with frequency for different flying capacitor sizes. The results obtained to plot these curves were averaged over the switching period when in steady state. (a) Efficiency – $\frac{P_{load}}{P_{in}}$; (b) Load power; (c) Input power; (d) Output voltage, normalised by the source voltage; (e) Input voltage, normalised by the source voltage; (f) Input resistance, normalised by the load resistance; (g) Input resistance, normalised by the source resistance; (g) Analysed flying capacitor values range.

In general terms, a switched capacitor circuit has an input resistance inversely proportional to the switching frequency. For a single switched capacitor, the average current during a period is given by $i_C = Q/T$, where the charge is $Q = C/\Delta V$. If the current of the capacitor is proportional to the voltage across its terminals, computing for $\Delta V/i$ yields $R_{EQ} = T/C = 1/(f \times C)$. Extending this relation to a more complex switched switched capacitor circuit yields the fact that higher frequencies lower the resistance imposed by the circuit to the source, hence lowering resistive losses and finally, increasing the conversion block efficiency. Figures 4.3f and 4.3g depict the evolution of the resistance "seen" by the source – i.e. the input resistance of the DC/DC converter – normalised by the load resistance R_L. It is visible that the increase of the switching frequency leads to a decrease of the input resistance – R_{IN}. In fact, R_{IN} approximates the value of $(1/n^2)R_L$,

a very important result, which will be analysed in Subsection 4.3. For now, let us conclude that R_{IN} decreases with the switching frequency increase. The flying capacitor increase also leads to the decrease of R_{IN}, as there is more charge being shuttled to the output.

Both the increase of the frequency of switching and the flying capacitor cause an increase of the performance of the conversion block. However, it denotes an exponential evolution, i.e. it is quite dramatic for low values of either switching frequency or flying capacitor and tends to "slow" its progression as the frequency or the capacitance achieve higher values. One can observe that, for frequency values over 500 kHz, the slope of the efficiency curve is quit shallow. And for capacitance values above 1 nF, the gain in performance is very small. Considering the fact that in a "real" application, higher frequency means higher energy consumption, the gain of increasing the frequency may not compensate the cost of doing so. Similarly, higher flying capacitor requires more area but, above a certain value, the performance increase is not significative.

4.2.2 The Switch Conductance Resistance

Another parameter that has influence on the converter operation is the R_{ON} resistance. It models the switch conduction resistance of the switches, which leads to conversion losses as there is some energy being dissipated by Joule effect on these devices.

Figure 4.5 portrays a sweep of the resistive value of the closed switches, from 1 Ω to 10 kΩ. This analysis was performed for a range of switching frequencies varying from 1 kHz to 500 kHz. The remaining parameters are are $V_S = 1\,\text{V}$, $R_S = 10\,\text{k}\Omega$, $C_{IN} = 100\,\text{nF}$, $C_{FLY} = 1\,\text{nF}$, $C_L = 100\,\text{nF}$ and $R_L = 40\,\text{k}\Omega$. The results correspond to average values over one switching period, in steady state operation.

The immediate result to consider is the performance decrease, as the R_{ON} resistance increases, which falls bellow 50% for $R_{ON} = 10\,\text{k}\Omega$, as seen in Figure 4.5.

This is an expected and intuitive result. The increase of the switch closed resistance implies higher resistive losses in the conversion circuit, which leads to less power being delivered to the load – Figures 4.5b and 4.5c – and a lower VCR – Figures 4.5d and 4.5d – thus resulting in a performance decrease.

It is also observable in Figures 4.5f and 4.5g that the input resistance of the converter increases as a direct result of increasing the switch resistance of the circuit. The ratio between the input resistance and the source resistance or between the first and the load resistance is dimmed for lower values of switching frequency because, as seen in Subsection4.2.1, for lower values of the latter, the input resistance is high enough for a 10 kΩ increase to be of relevance.

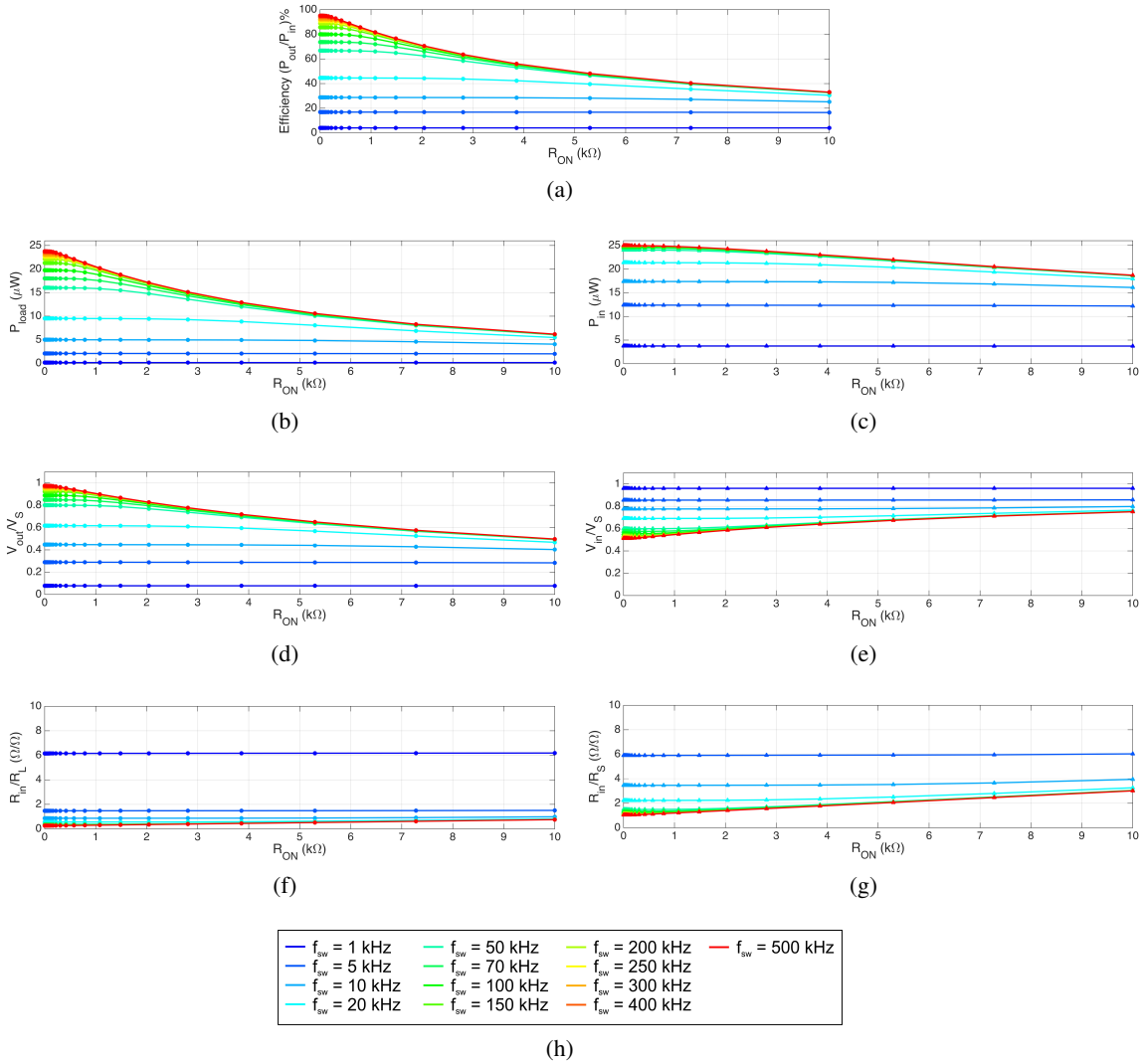


Figure 4.5: Analysis of the parallel-series voltage doubler performance with the variation the switch R_{ON} resistance at several switching frequencies. (a) Efficiency – $\frac{P_{out}}{P_{in}}$; (b) Load power; (c) Input power; (d) Output voltage, normalised over the source voltage; (e) Input voltage, normalised over the source voltage; (f) Input resistance, normalised over the load resistance; (g) Input resistance, normalised over the source resistance; (h) Analysed frequency range.

4.2.3 The Input and Output Capacitors

Using the mathematical model, the value of the size of input and output capacitors was swept from 1 pF to 10 nF. This analysis was performed for a range of switching frequencies varying from 1 kHZ to 500 kHz. The remaining parameters are are $V_S = 1\,\text{V}$, $R_S = 10\,\text{k}\Omega$, $R_{ON} = 1\,\Omega$, $C_{FLY} = 1\,\text{nF}$ and $R_L = 40\,\text{k}\Omega$. For the C_L sweep, C_{IN} was kept at 100 nF and vice versa. The results correspond to average values over one switching period, in steady state operation.

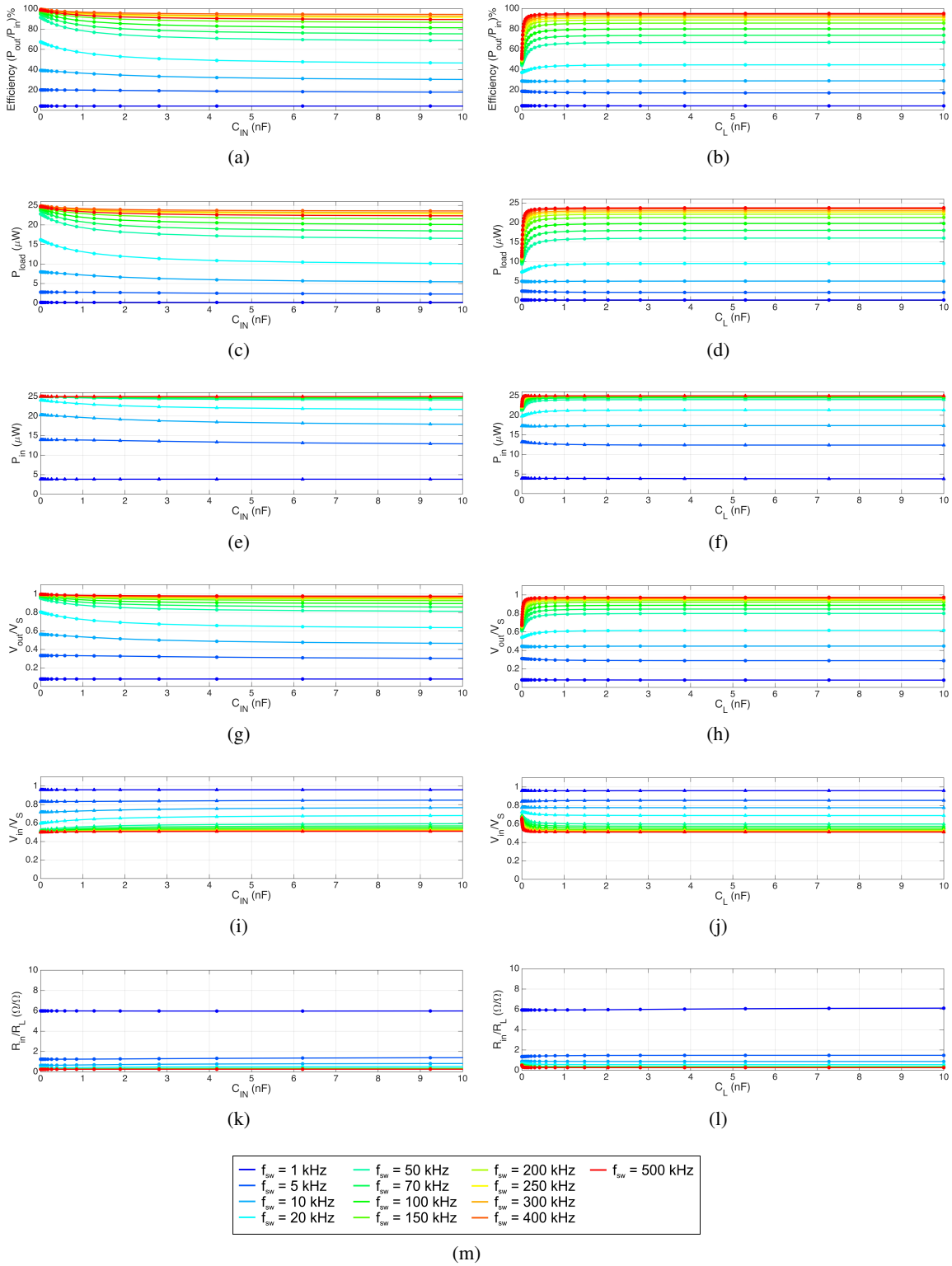


Figure 4.6: Influence of the input and load capacitors for several switching frequencies. (a) Efficiency with C_{IN} and (b) C_L; (c) Load power with C_{IN} and (d) C_L; (e) Input power with C_{IN} and (f) C_L; (g) Output voltage, normalised over the source voltage, with C_{IN} and (h) C_L; (i) Input voltage, normalised over the source voltage, with C_{IN} and (j) C_L; (k) Input resistance, normalised over the load resistance, with C_{IN} and (l) C_L; (m) Analysed frequency range.

As seen from Figure 4.6, both input and load capacitors, present a steady state behaviour roughly constant, despite heir dimensions. There is some variation, of the presented parameters, for the lower end of the studied range. When these have approximate those of the flying capacitor – in this case 1 nF, their variation has a slight influence on the operation of the converter, as depicted in Figure 4.6. Nevertheless, one of the base arguments to choose the parallel-series topology, was its reported superior performance in the SSL regime. However, in order to operate in this regime, the relation between the time constants of the system must be such that allows the charging and discharging of the capacitors to occur completely. This means that $T_{sw} << R_S \times C_{IN}$, $T_{sw} >> R_{ON} \times C_{FLY}$ and $T_{sw} << R_L \times C_L$, i.e. each switching phase is held for a sufficient amount of tim, for the flying capacitor to charge os discharge completely. This in turn implies that the ratios C_{IN}/C_{FLY} and C_L/C_{FLY} must be high enough to allow SSL operation, which keep these capacitors in the operation zone depicted in Figure 4.6, where variations on their size have no influence in the steady state results.

This being said, these components have relevant roles in the operation of the system, which only become visible in a transient analysis.

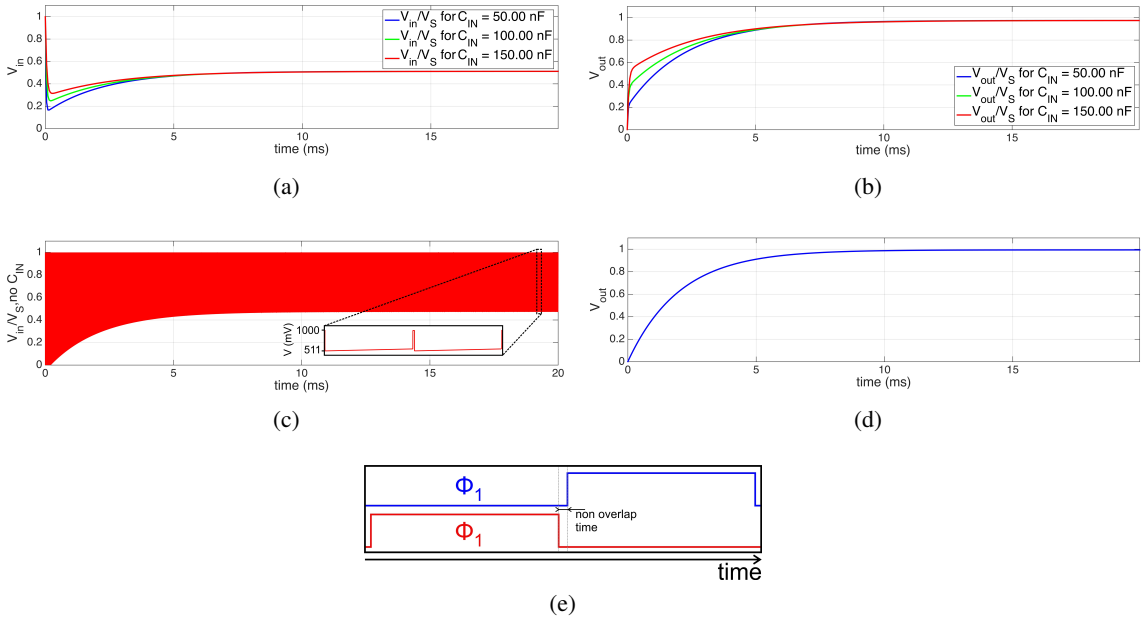


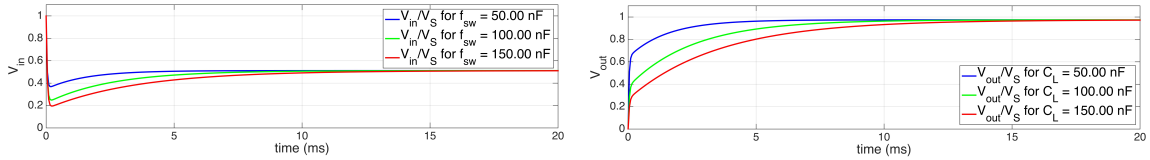
Figure 4.7: Influence of the input capacitor on the voltage doubler. (a) Input voltage (b) Output voltage; (c) Input voltage behaviour with no input capacitor; (d) Output voltage behaviour with no input capacitor; (e) Schematic representation of the non overlap time of the switching signals.

Regarding the first, C_{IN}, Figure 4.7 illustrates the input voltage behaviour for distinct values of input capacitor size – Figure 4.7b – and its behaviour when there is no input capacitor. This analysis was performed in simulation, in order to avoid the necessity to develop another mathematical model, without input capacitance.

One can observe that the presence of the input capacitor allows the voltage to be regulated at the input of converter. In Figure 4.7c, the voltage ripples visibly between approximately 500 mV

and 1 V, the source voltage. This happens because, in order to ensure that the switching signals that drive the switches of the system are never simultaneously high – which would connect both terminal of the capacitors to the ground –, the switching signals have a duty cycle bellow 50 %, in this case the duty cycle was 49.5 %. This means that there is a short interval of time, in which both signals are low – the non overlapping time, Figure 4.7e – in which the source is in open circuit, thus leading the voltage at the input node to rise to V_S. The output voltage is not affected.

Regarding the latter, the load capacitor, although there is no variation in the steady state results by varying its size when $C_L >> C_{FLY}$, changing the size of the load capacitor, affects the time it takes for the output to reach steady state, as the output voltage variation is governed by the $R_L \times C_L$ time constant.



(a) (b)

Figure 4.8: Influence of the load capacitor on the voltage doubler. (a) Input voltage (b) Output voltage.

On Figure 4.8, one may observe that a larger load capacitor leads to a higher $R_L \times C_L$ time constant, i.e. the voltage takes longer to reach steady state.

Nevertheless, the energy in a capacitor is given by $(1/2) \times CV^2$, which means tat larger capacitors also allow more energy to be stored, so there is a trade off that must be carefully wighted, between area, energy storage and the time the capacitor takes to charge.

The electrical components are the degrees of freedom concerning the choice of an adequate conversion block for the system as they dictate how to converter operates in a system.

However, the performance of the converter is also influenced by the system in which it is integrated. The source has specific characteristics – such as its internal resistance – that imposes constraints in the system that must be tackled in order for the operation to be optimal. Similarly, the load affects the performance of the converter.

Ultimately the relation between the resistance of the load and the resistance of the source dictates the power that can be extracted from the latter to the first.

Considering, at this point the importance of the source and the load on the overall performance, one can state that it is desirable for the conversion block to extract as much energy as possible from the source and deliver as much of this amassed energy as possible to the load. This process is highly dependent on the adaptation of the load resistance to the one from the source. Under the scope of this impedance matching process, next section will study the importance of the conversion block on the source-load energy transference.

4.3 Impedance Matching

It remains to study the influence of the load on the system.

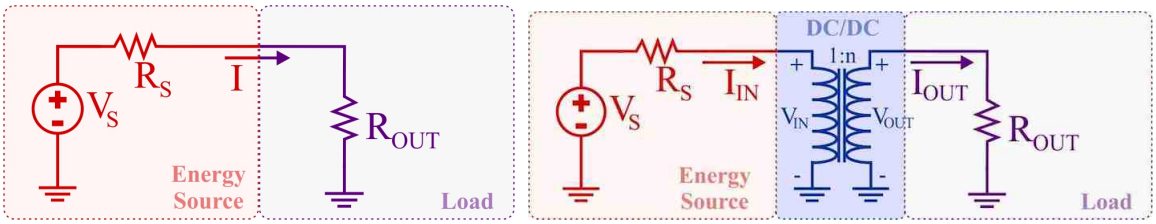


Figure 4.9: Source-load relation. (a) Source directly connected to load; (b) Source-load connection conditioned by a DC/DC converter of ratio n.

When considering a generic source-load relation, such as the one depicted in Figure 4.9a, the current I flowing on that net is given by

$$I = \frac{V_S}{R_S + R_{OUT}} \tag{4.19}$$

and the power delivered to the load resistance is

$$P_{OUT} = I^2 V_S = \frac{{V_S}^2 R_{OUT}}{(R_S + R_{OUT})^2} \tag{4.20}$$

which is maximised when $R_{OUT} = R_S$, as stated by the maximum power transfer theorem. Setting the load resistance equal to the source internal resistance is often called impedance matching.

However, when the energy that flows from the source to the load is conveyed by a DC/DC converter, this relation is different.

A DC/DC converter can be interpreted as a transformer, as portrayed in Figure 4.9b, which ideally relates its input and output according to $V_{OUT} = nV_{IN}$, $I_{OUT} = I_{IN}/n$ and $P_{OUT} = V_{OUT}I_{OUT} = V_{IN}I_{IN} = P_{IN}$. In this case, the power delivered by a generic DC/DC converter with a conversion ratio of n to the load resistor R_{OUT} is given by (4.21).

$$P_{OUT} = \frac{{V_{out}}^2}{R_{OUT}} = \frac{n^2 {V_{IN}}^2}{R_{OUT}} = P_{IN} = V_{IN} I_{IN} \tag{4.21}$$

such that

$$n^2 {V_{IN}}^2 = I_{IN} R_{OUT} \tag{4.22}$$

The input voltage of the DC/DC converter, when fed by a voltage source V_S with a series resistance R_S is

$$V_{IN} = V_S - I_{IN} R_S \tag{4.23}$$

thus, computing (4.22) and (4.23) together yields

$$I_{IN} = \frac{n^2 V_S}{R_{OUT} + n^2 R_S} \tag{4.24}$$

and

$$V_{IN} = \frac{V_S R_{OUT}}{R_{OUT} + n^2 R_S} \tag{4.25}$$

which, equating with 4.21, results in

$$P_{OUT} = \frac{n^2 {V_{out}}^2 R_{OUT}}{(R_{OUT} + n^2 R_S)^2} \tag{4.26}$$

finally, P_{OUT} has a maximum value of

$$P_{OUT,MAX} = \frac{{V_{out}}^2}{4 R_S} \tag{4.27}$$

when

$$R_{OUT} = n^2 R_S \tag{4.28}$$

For the moment, let us assume that $R_L = R_{OUT}$. The use of the R_{OUT} notation to describe the load resistance is not arbitrary and will soon be explained.

Through 4.27 and 4.28, it is to be expected that, when the load resistance – i.e. R_{OUT} – approaches the value of $n^2 R_S$ the power transference is maximised. This happens because when such is verified, R_{IN} – the DC/DC converter input resistance – which, can be obtained by dividing R_{OUT} by n^2 – becomes R_S, i.e. the input impedance of the DC/DC converter becomes *matched* with the voltage source internal resistance.

To verify this hypothesis, the mathematical model was used to sweep the value of R_L from 1 kΩ to 100 kΩ for values of the switching frequency ranging from 1 kHz to 500 kHz, using a voltage doubler configuration with $V_S = 1\,\text{V}$, $R_S = 10\,\text{k}\Omega$, $C_{IN} = 100\,\text{nF}$, $C_{FLY} = 1\,\text{nF}$, $C_L = 100\,\text{nF}$ and $R_{ON} = 1\,\Omega$.

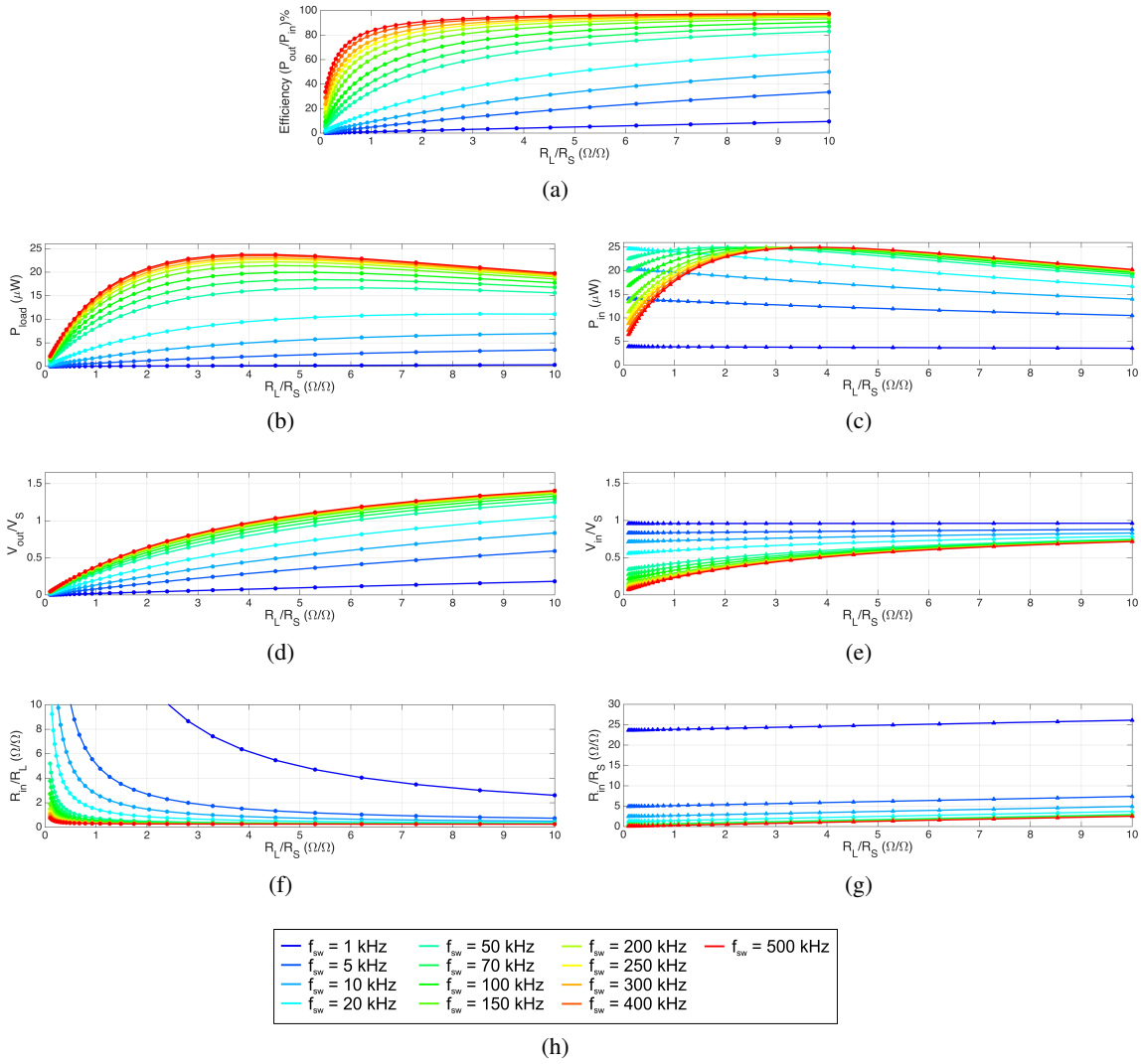


Figure 4.10: Analysis of the parallel-series voltage doubler performance with the variation of R_L at several switching frequencies. (a) Efficiency – $\frac{P_{out}}{P_{in}}$; (b) Load power; (c) Input power; (d) Output voltage, normalised over the source voltage; (e) Input voltage, normalised over the source voltage; (f) Input resistance, normalised over the load resistance; (g) Input resistance, normalised over the source resistance; (h) Analysed frequency range.

Figure 4.10 reveals that, for this case, the load power, in Figure 4.10b, is maximised for $R_L = 4R_S$, which corroborates (4.28). Moreover, the input power – Figure 4.10c – is maximal when the ratio between the input and source resistances is 2, i.e. when the resistance at the converter input equals the internal resistance of the source, once more, as stated by the maximum power point transfer theorem. According to Figure 4.10a the conversion efficiency increases with the load resistance, however, this only means that the ratio, P_{load}/P_{in} approximates 1. The absolute power values do not rise proportionally to the load resistance, as seen in Figures 4.10b and 4.10c.

The overall performance of the system, as seen from the data on Figure 4.10 also increases with the frequency. For further readability, the dual results are presented in Figure 4.11, i.e. a sweep of the frequency, from 1 kHz to 1 MHz, for distinct load resistance values, ranging from 1 kΩ to 100 kΩ.

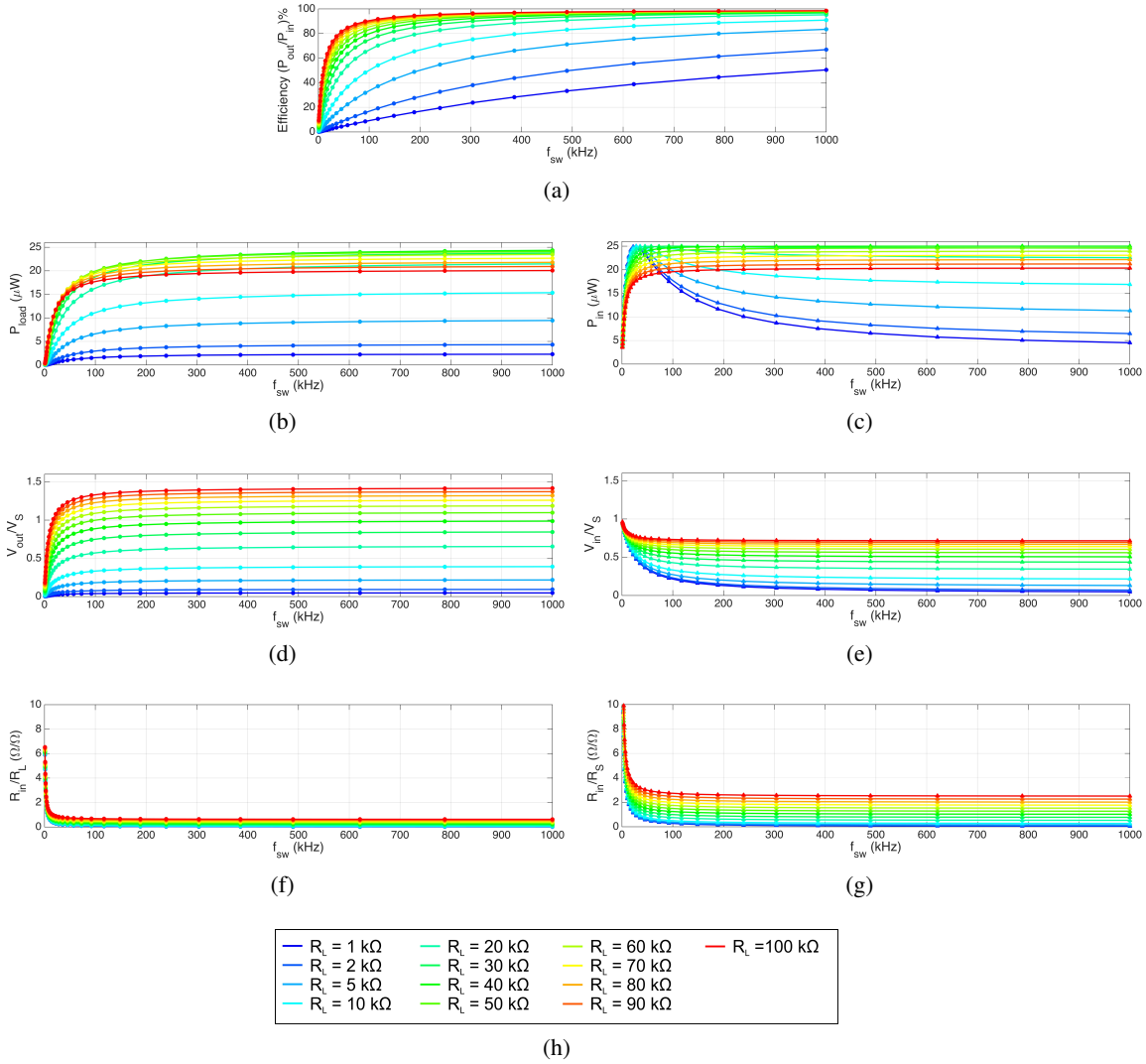


Figure 4.11: Analysis of the parallel-series voltage doubler performance with the variation of the switching frequency, f_{sw}, for several values of R_L. (a) Efficiency – $\frac{P_{out}}{P_{in}}$; (b) Load power; (c) Input power; (d) Output voltage, normalised over the source voltage; (e) Input voltage, normalised over the source voltage; (f) Input resistance, normalised over the load resistance; (g) Input resistance, normalised over the source resistance; (h) Analysed load resistance range.

The range of frequency under analysis was purposely extended to illustrate the fact that, for switching frequencies higher than a certain value, further increase of its value has little effect on the steady state results. Nevertheless, increasing the frequency decreases the input resistance, which approximates the ratio $1/n^2$. For power transference maximisation, two conditions are verified, first, the input resistance, must be $1/n^2$ times the load resistance, which means that the losses on the conversion are minimal, and the input resistance must be equal to the source resistance, for maximum power transference from the source. For the case, with $R_S = 10\,\text{k}\Omega$, for the these two requirements to be fulfilled, R_L must be $40\,\text{k}\Omega$. Inspecting Figure 4.11g, one may observe that the curve that illustrates the frequency sweep for $40\,\text{k}\Omega$, at a frequency higher than 200 kHz, verifies a R_{IN}/R_S ratio of 2 and that the R_{IN}/R_L is at 0.25, i.e. $1/n^2$, with $n = 2$. Cross checking these results in Figure4.10, for $R_L = 40\,\text{k}\Omega$, or, equivalently, $R_L/R_S = 4$, at frequencies higher than the

empirical value 200 kHz, such as 500 kHz, the power extracted from the source and delivered to the load is maximised.

The results illustrated in Figures 4.10 and 4.11 hint about on important aspect of the operation of the converter in regard to changes in the switching frequency and variations in the load. The load affects how much power can be extracted from the source, as the way the source and load resistances ratio greatly affect the power transference. This can be inferred from the fact that the measured parameters, remain roughly constant when the frequency is swept over a certain value but change for different values of R_L.

The frequency, however, dictates how much of the power extracted from the source is conveyed from the source to the load, i.e. affects the performance of the conversion process. Another aspect to take into account is the fact that the performance of the system increases when the load approximates a resistive value n^2 times greater than the internal resistance of the source.This means that, for the same source, different loads require different conversion ratios – n – in order to verify this condition and achieve optimal performances.

The analysis on this up until this point allowed to gain some insight on how the components of the system influence its operation. And how the source and load jointly affect the system overall performance.

For the following analysis on this chapter, the default set of values will thus be $C_{IN} = 100\,\text{nF}$, $C_{FLY} = 1\,\text{nF}$, $R_{ON} = 1\,\Omega$, $C_L = 100\,\text{nF}$ and $f_{sw} = 100\,\text{kHz}$. Moreover, one may assume, regarding the frequency, that a suitable upper limit would be 500 kHz, as increasing it above that value has no significative effect.

These parameters were chosen firstly because, it allows an efficiency of the converter above 90 % and secondly because it allows the system to operate at SSL, which was the initial reason for the choice of the parallel-series topology. As $T_{sw} << R_S \times C_{IN}$, $T_{sw} >> R_{ON} \times C_{FLY}$ and $T_{sw} << R_L \times C_L$ each switching phase is held enough time for the charging and discharging of the capacitors to occur completely.

4.3.1 Arbitrary Ratio SC DC/DC Parallel-Series Converter Model

The mathematical approach used so far to understand the operation of DC/DC converters is an invaluable tool for DC/DC converter analysis that yields accurate and insightful results. It becomes cumbersome rather quickly, however, as one increases the complexity of this circuits. Standard circuit analysis, based on matrix calculations, tends to yield computationally costly formulations that render this analysis unpractical. Furthermore, for each ratio of each topology, the set of equations that defines its circuit must be solved, which makes the task of comparing these different models rather complex. It is desirable to have a pragmatic and simple approach when considering a generic SC DC/DC converter with an arbitrary conversion ratio n. Michael Seeman provided such a tool in [68].

The author approaches the SC DC/DC converter through the metric that determines its performance: the output impedance. The SC DC/DC converter is thus modelled as a physical resistance with a power dissipation equal to the power lost in the circuit due to capacitor charging and switch

resistance. This resistance has an asymptotic behaviour constrained by two limits, the aforementioned SSL and Fast Switching Limits. When an SC DC/DC converter is operating in the first, the switching frequency is slow enough to allow the charge on each capacitor to equilibrate fully during each phase. In the SSL, the currents are modelled as impulsive and the series resistances of the switches, capacitors and interconnects are neglected as they have no effect on the output impedance because they are not large enough to prevent the capacitors from equilibrating fully. Whereas when an SC DC/DC converter is operating in the latter, its losses are related is related to conduction loss in resistive elements of the circuit.

Confronting this modelling technique with the results obtained so far, it becomes clear that both the doubler and tripler are operating in the SSL regime. Figure 4.2 corroborates this assumption as one can observe that the steady state behaviour of the voltage signals portray the charge equilibrium on each phase, for the capacitors in the circuit. There is no noticeable exponential behaviour of the voltage in the capacitors which mean they achieve their final value, on each phase, within a time interval $t_{charge,discharge} \ll \frac{T}{2}_{\Phi_1,\Phi_2}$.

This greatly simplifies the SC DC/DC circuit analysis as its output behaviour is reduced to a simple resistor.

According to Seeman, the parallel-series converter output impedance, operating in the SSL regime can thus be modelled by (4.29)

$$R_{SSL} = \frac{(n-1)^2}{f_{sw} C_{tot}} \tag{4.29}$$

with n as the conversion ratio, f_{sw} as the switching frequency and C_{tot} as the sum of all flying capacitors, reducing its output to the circuit depicted in Figure 4.12.

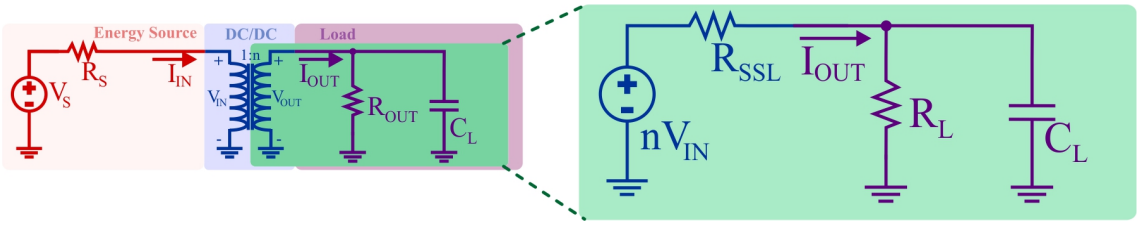


Figure 4.12: Seeman approach to the SC DC/DC voltage doubler.

Observing the circuit on Figure 4.12, one might conclude that when the load capacitor is fully charged, it can be ignored as it behaves as an open circuit and the source, which models the ideal output, outputs a current given by

$$I_{OUT,SSL} = \frac{nV_{IN}}{R_{SSL} + R_L} \tag{4.30}$$

and the output voltage is given by the voltage divisor of the two resistors as

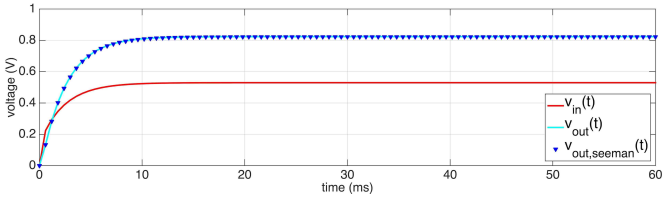
$$V_{OUT,SSL} = nV_{IN}\frac{R_L}{R_{SSL}+R_L} \tag{4.31}$$

which, in turn, leads to a power delivered to the load of

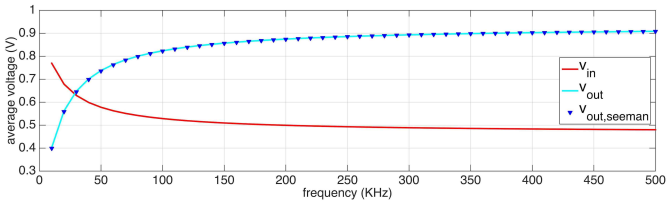
$$P_{L,SSL} = (nV_{IN})^2\frac{R_L}{(R_{SSL}+R_L)^2} \tag{4.32}$$

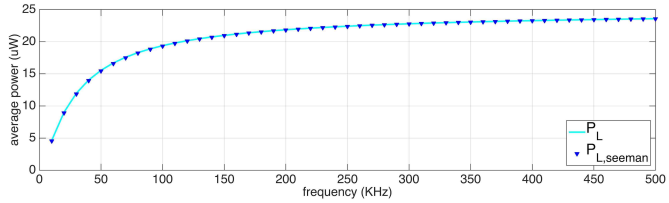
In (4.32) the relation between the SSL resistance and the load power is expressed. As expected, with the increase of R_{SSL}, i.e. decreasing f_{sw} or the value of the flying capacitors, R_{SSL} is increased thus leading to more power being dissipated by this resistor, i.e. grater losses in the converter, and less power being delivered to the load.

Taking as an illustrative example the voltage doubler with $V_S = 1\,\text{V}$, $R_S = 10\,\text{k}\Omega$, $C_{FLY} = 1\,\text{nF}$, $C_{OUT} = 100\,\text{nF}$, $R_L = 35\,\text{k}\Omega$ and $f_{sw} = 100\,\text{kHz}$, the SSL resistance would thus become $R_{SSL} = 9.0909\,\text{k}\Omega$.



(a)





(b)

Figure 4.13: SC DC/DC SSL approach analysis. (a) Transient analysis (b) Frequency sweep.

Figure 4.13 superimposes the results of using this model to those obtained through a Spectre simulation of the standard SC DC/DC parallel-series voltage doubler circuit. Figure 4.13a illustrates clearly that the model approximates quite accurately the transient behaviour of the conventional circuit, with a maximum error of approximately 0.6 %. Moreover, the frequency behaviour

is also well modelled by this approach, as depicted in Figure 4.13b. Due to the simplicity and practicality of this approach to SC DC/DC converters, this model will henceforth be used to model its output behaviour.

When this model is related with the Maximum Power Transfer Theorem, an important conclusion arises. (4.28) states that the power extracted from the source is maximised when $R_{OUT} = n^2 R_S$. Taking into account Figure 4.12, let us rewrite the previous equation as $R_{SSL} + R_L = n^2 R_S$, where $R_{OUT} = R_{SSL} + R_L$. Solving in respect to R_{SSL} yields

$$R_{SSL} = n^2 R_S - R_L \tag{4.33}$$

In (4.33) is stated that, as long as $R_L < n^2 R_S$ there is an achievable value for R_{SSL} that holds the ratio R_{IN}/R_{OUT} equal to $1/n^2$ thus maximising the energy extracted from the source. In other words, for a specific ratio n, assuming the value of the capacitors as predefined, there is a frequency which allows the maximum value of P_{IN} to be attained. If $R_L \geq n^2 R_S$, then the only way to regain the optimal operation point for the source power is to increase the ratio until $R_L < n^2 R_S$ and then manipulate the frequency such that $R_{IN}/R_{OUT} = 1/n^2$. This hints about the necessity to use the conversion ratio as a control variable to retain optimal energy extraction.

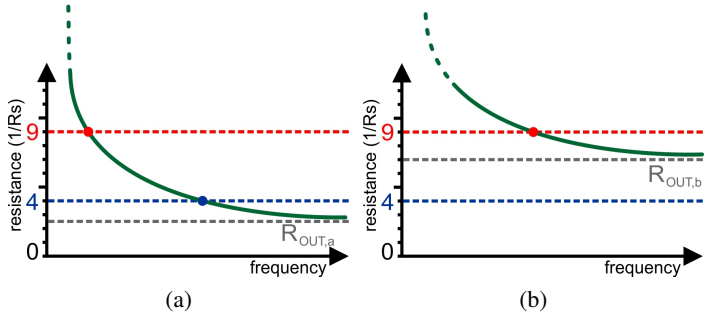


Figure 4.14: R_{IN} behaviour with frequency. Analysis for different load conditions. (a) $R_{OUT} < 4R_S$ (b) $4R_S < R_{OUT} < 9R_S$.

Figure 4.14 illustrates the relation between the frequency behaviour of the input resistance of the converter with the impedance matching process between the source and the converter. The green solid line depicts the input impedance of the converter, multiplied by n^2, which converges asymptotically to R_{OUT} (or, equivalently, R_{IN} converges to R_{OUT}/n^2) as the frequency increases – refer to Figures 4.10 and 4.11. Considering situation 4.14a, where $R_{OUT} < 4R_S$, let us assume that the curve that describes $R_{IN}(f_{sw})$ characterises a voltage doubler. In this case, according to (4.26) and (4.28), the load resistance that maximises the input power is $4R_S$, signalled as the blue dashed line. In this case, there is a frequency at which the doubler can operate that allows the input power to be maximised. It happens when the green line intercepts the blue dashed line, i.e. $n^2 R_{IN} = R_{OUT} = 4R_S$. In situation 4.14b, however, when $4R_S < R_L < 9R_S$, increasing the frequency would approximate the input resistance to R_{OUT}/n^2 which, in this case is a resistive value higher the optimal one for the voltage doubler. The green line would never intercept the blue

dashed line thus, the optimal conditions can not be met by the voltage doubler. Nevertheless, if we consider the voltage tripler – $n = 3$ –, which has an optimal load resistance of $9R_S$, one can observe that there is a frequency at which it can operate that achieves R_{OUT}/n^2, i.e. the green line intercepts the red dashed line.

This illustrates the fact that, different load conditions imply different ratios in order for the optimal conditions to be achieved. Figure 4.14a illustrates yet another important aspect. It is noticeable that, under these conditions, both the double and the tripler can operate at a frequency that achieves R_{OUT}/n^2. However, for the latter, the frequency of operation is lower than the one for the first. Considering (4.29), it becomes clear that matching the tripler input impedance with the source internal impedance becomes costly. Decreasing the frequency increases the output impedance of the converter, i.e. the power dissipated in the conversion process is higher. If the optimal load resistance is out of reach for a given ratio, i.e. $R_L \geq n^2 R_S$, then increasing the ratio may prove a profitable solution to retain the optimal conditions within the operational range. To assert this hypothesis, the parallel-series was subject to a load resistance sweep for its doubler, tripler and quadrupler configurations. The SSL model was used for the simulations and validated against its conventional counterpart circuits.

Figure 4.15 portrays the results of the simulation of the three parallel-series topologies under varying load conditions. The circuit parameters in use are $V_S = 1\,\mathrm{V}$, $R_S = 10\,\mathrm{k\Omega}$, $C_{IN} = 100\,\mathrm{nF}$, $C_{FLY} = 1\,\mathrm{nF}$, $R_{ON} = 1\,\Omega$, $C_L = 100\,\mathrm{nF}$ and $f_{sw} = 100\,\mathrm{kHz}$. Firstly, as further proof of the validity of the R_{SSL} approach, is is clear that the results obtained though the SSL resistance model – the markers – closely approximate those obtained through the simulation of the conventional circuit. The maximum error reported was of 3.7348 %, rendering this approach quite useful and accurate.

Figures 4.15b and 4.15c depict the fact that different topologies operate more efficiently for different load conditions as the energy extracted from the source and delivered to the load has its peak for distinct values of R_L. Figure 4.15d illustrates that, as the load resistance increases so does the efficiency. One must keep in mind, however, that this efficiency is measured as output power over input power. It only expresses that the ratio between these two quantities approximates 1 as the load increases. Nevertheless, in Figures 4.15b and 4.15c, it is clear that the absolute power delivered to the load is lower even though the efficiency is getting closer to 100 %.". This can be explained through the SSL model. As the load decreases, the value of R_L approximates R_{SSL} which means that a greater fraction of the available input power is dissipated in R_{SSL}, i.e. lost in the converter. Even if the efficiency of the converter increases with the load, there is less power being shuttled from the source.

In this analysis the load resistance was normalised by the source resistance in order to emphasise the fact that the best performance occurs when R_L approximates $n^2 R_S$. For different topologies, this means different load resistances to yield maximum power. This immediately states the very important condition that, given varying load conditions, a multi ratio approach allows the output of a greater amount of energy as different topologies have better performances for different load conditions.

Following a multi ratio operation, there is one peculiarity on the performance of the different

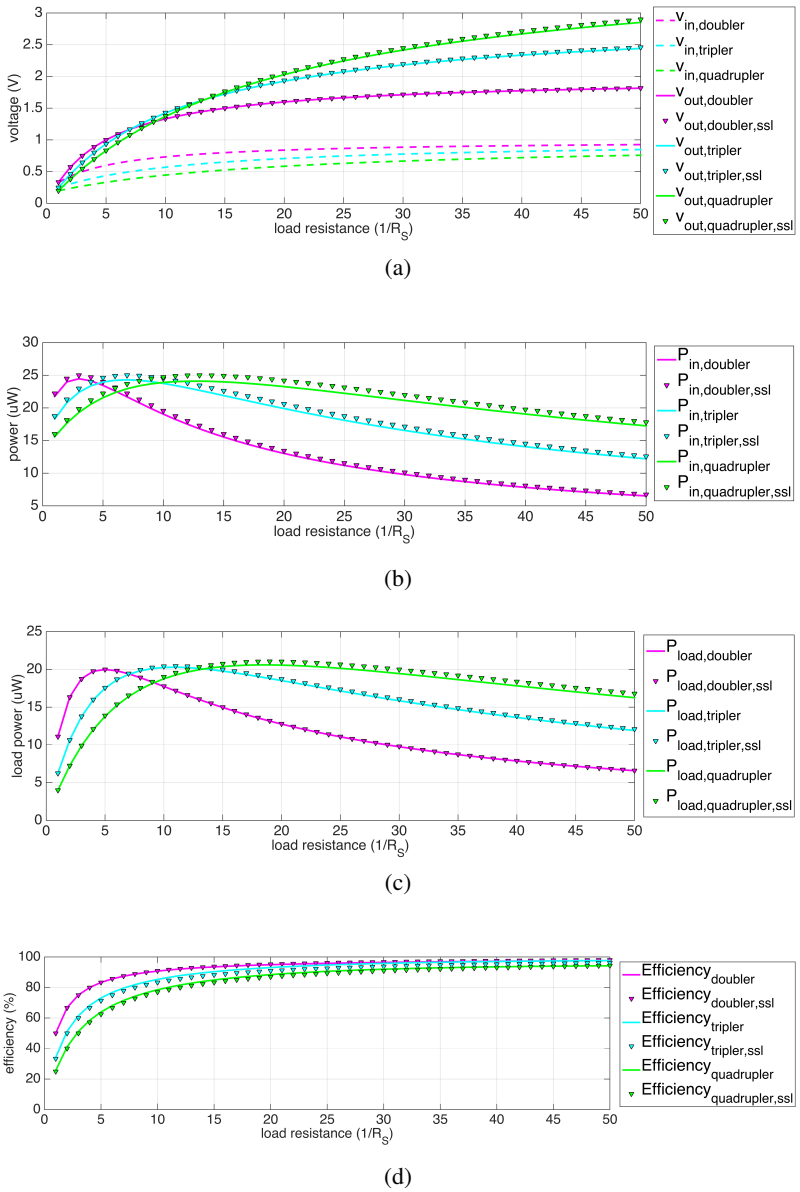


Figure 4.15: Performance analysis of the SC DC/DC parallel-series voltage doubler tripler and quadrupler topologies under a varying load. (a) Input and output voltages; (b) Input power; (c) Power delivered to the load; (d) Conversion efficiency (P_{load}/P_{in}).

topologies that stands out in these curves. From Figure 4.15, one can see that different topologies manifest peak performances at distinct load conditions. Making use once more of the SSL model approach, for a specific ratio, the output power is given by (4.32). As the output power displays a parabolic behaviour with R_L– refer to Figure 4.15c –, it is desirable to change topology when the load conditions are such that the output power curve of the topology of ratio $n+1$ (or $n-1$, when $n > 2$) achieves higher values than the topology of ratio n. From the SSL approach, the output resistance can be defined as $R_{OUT} = R_{SSL} + R_L$ – the sum of the system load, modelled by R_L, and the converter output resistance, R_{SSL}, refer to Figure 4.12.

Considering varying load conditions at a given frequency, i.e. R_l changes but R_{SSL} is constant,

there is an exact value of the load resistance R_l at which the topology must change, to keep the output power maximised. Let us call that value $R_{L,switch}$ – the load value at which the topology must be *switched*. Graphically, $R_{L,switch}$ is the point at which the output power curves of two adjacent ratio topologies intersect. In theory, that point might be found making use of (4.32), setting $P_{OUT,n_\alpha} = P_{OUT,n_\beta} =$ – being n_α and n_β two arbitrary adjacent ratios – and solving in respect to R_L, thus obtaining[1]

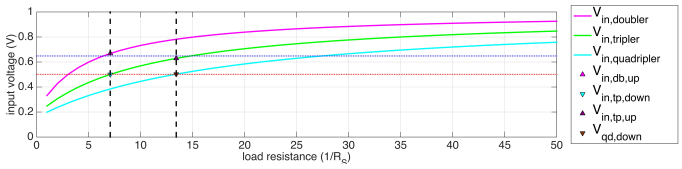
$$R_{L,switch} = \frac{-2(\chi_\beta - \chi_\alpha) \pm \sqrt{[2(\chi_\beta - \chi_\alpha)]^2 - 4(\psi_\beta - \psi_\alpha)(\chi_\beta R_{SSL,\alpha} - \chi_\alpha R_{SSL,\beta})}}{2(\psi_\beta - \psi_\alpha)} \tag{4.34}$$

with

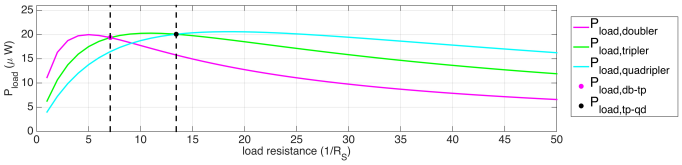
$$\psi_\alpha = (n_\alpha V_{in,\alpha})^2; \quad \psi_\beta = (n_\beta V_{in,\beta})^2 \tag{4.35}$$

and

$$\chi_\alpha = \psi_\alpha R_{SSL,\beta}; \quad \chi_\beta = \psi_\beta R_{SSL,\alpha} \tag{4.36}$$



(a)



(b)

Figure 4.16: Input voltage and load power behaviour with the load resistance. (a) Input resistance; (b) Load power.

From a closer look at the input voltages and power delivered to the load – Figure 4.16 –, for the three topologies analysed previously analysed, one can extract the input voltage values at the intersection of the power curves. On Figure 4.16, the "db", "tp", "qd" subscripts denote the doubler, tripler and quadrupler topologies, respectively, whereas the the "up" and "down" subscripts identify, in Figure 4.16a, for a given ratio, the lowest or highest input voltage value, respectively, for the range illustrated in the same figure by the red and blue horizontal dashed lines.

[1]The variables ψ and χ are just for readability purposes, due to the lengthiness of (4.34).

Table 4.1: Input Voltage and load resistance at the intersection of the load power curves of adjacent ratio converters.

P_{load} **Intersection**	**Doubler** V_{in}	**Tripler** V_{in}	**Quadrupler** V_{in}	R_L **(Eq. 4.34)**	R_L **(Simulation)**
db-tp	667.7 mV	500.3 mV	–	70.695 kΩ	70.7850 kΩ
tp-qd	–	628.7 mV	502.6 mV	131.52 kΩ	134.2339 kΩ

From Table 4.1, when the doubler and tripler curves intersect, these are $V_{in,db,up} = 667.7\,\text{mV}$ and $V_{in,tp,down} = 500.3\,\text{mV}$, whereas for the intersection of the tripler and quadrupler power curves, $V_{in,tp,up} = 628.7\,\text{mV}$ and $V_{in,qd,down} = 502.6\,\text{mV}$. Using (4.34), one obtains at the doubler and tripler load power curves intersection, $R_{L,switch,2-3} = 70.695\,\text{k}\Omega$ and for the tripler and quadrupler load power curves intersection, $R_{L,switch,3-4} = 131.52\,\text{k}\Omega$. The values obtained through simulation for these intersections were $R_{L,switch,2-3} = 70.7850\,\text{k}\Omega$ and $R_{L,switch,3-4} = 134.2339\,\text{k}\Omega$, which are quite approximate to those obtained through (4.34).

From Figure 4.16a, one may observe that the input voltage increases with the load resistance. And that the voltage values at which the load power curves intersect are quite approximate, defining a range, for a specific topology, identified by the subscripts "up" and "down", in Figure 4.16a. One may observe that $V_{in,db,up} \approx V_{in,tp,up}$ and $V_{in,tp,down} \approx V_{in,qd,down}$. There is a maximum error of 39 mV between $V_{in,db,up}$ and $V_{in,tp,up}$, for a source voltage of 1 V (3.9 %) and an error of 2.3 mV (0.23 %) between $V_{in,tp,down}$ and $V_{in,qd,down}$. Assuming that this range as constant, allows (4.34) to predict the load resistance value, as every other parameter is known. More importantly, this behaviour might be used in order to devise a mechanism to maximise the power delivered to load and will be exploited in Section 5.1.

4.4 Conclusions to This Chapter

This chapter aimed to provide insight on the power conversion stage of an energy harvesting system, approaching both the converter circuit and its control mechanism. It studied the performance of the SC DC/DC parallel-series converter. Being the efficiency of the system a paramount aspect to consider, the parallel-series SC DC/DC converter was chosen as the subject of study, due to its reported superiority in low frequency operation, when compared to other topologies.

Firstly, a mathematical approach to the converter was adopted, in order to gain factual knowledge of the conversion operation. This model was validated through Spectre simulation and used to verify the effects of the variables that define the converter, namely its components. The voltage doubler was analysed using through this approach. This analysis allowed to conclude that:

- The increase of the frequency or the flying capacitor increase the conversion efficiency. However,
  - increasing the size of the flying capacitors requires more area;
  - increasing the switching frequency may require a higher power supply;

- The decrease of the area of the flying capacitor may be compensated by the increase of the switching frequency, and vice-versa, in order to maintain efficiency;
- Higher closed switch resistance – R_{ON} – leads to a decrease of efficiency in the energy conversion, as more energy is being dissipated by Joule effect on the converter;
- The size of both the input and load capacitors affects the steady state results of the converter, when these have sizes about the same order of magnitude as the flying capacitor, however, to operate in the SSL, these must be much larger than the latter, in order to $T_{sw} << R_S \times C_{IN}$, $T_{sw} >> R_{ON} \times C_{FLY}$ and $T_{sw} << R_L \times C_L$, i.e. each switching phase is held for a sufficient amount of time, for the flying capacitor to charge os discharge completely;
- Nevertheless, these capacitors have influence on the transient behaviour of the converter:
  - C_{IN} prevents the input source from rising to V_S during the non overlap periods;
  - C_L dictates the time it takes for the load to charge and discharge;
- The highest amount of power that can be harvested from the source to the load when $R_{OUT} = n^2 R_S$, with n as the conversion ratio and R_S as the internal resistance of the source.

Afterwards a generic model based on the output impedance of the converter was adopted, based on the work in [68]. It allowed a simplified and practical analysis of the converter operation and could also be easily used to study the operation of higher ratio converters, for which the previous mathematical analysis would prove computationally costly and less practical. Using this approach, the total load resistance can be decomposed by the resistive value of the load device plus the output resistance of the converter, such that $R_{OUT} = R_{SSL} + R_L$, with R_{SSL} as the latter.

The power delivered to the load displays a parabolic evolution with the resistive value of that load. The load power peaks when $R_{OUT} = n^2 R_S$, which means that different ratios provide better results for distinct load resistance ranges. These ranges, in turn intersect at specific resistive load values which define the optimal load value at which the conversion ratio should be changed, in order to maintain the power delivered to the load maximised. These points correlate with the behaviour of the input voltage that increases monotonically with the load resistance. The behaviour of the input voltage may then be used to determine when the conversion ratio must change, keeping in mind the goal to maximise the power delivered to the load.

After gaining some insight on how the energy conditioning block operates, next chapter will study the energy conversion process when the source is a PV cell.

Chapter 5

Photovoltaic Energy Conversion

In this chapter, the SC DC/DC converter will be studied when integrated on a PV energy harvesting system. It aims to:

- Analyse the DC/DC converter operation when the energy source is a PV cell;
- Devise a scheme to maximise the power delivered to the load.

The energy source is a PV cell behavioural model with electric characteristics similar to those of the characterised PV cells in Chapter 3. These characteristics are simulated using the practical model developed in Section 3.4 of the same Chapter. Section 5.1 will reflect on some energy considerations of such a system, namely the feasibility of the implementation of an energy conditioning scheme to efficiently provide energy to an arbitrary load. Some additional concerns to take into account will be approached on Section 5.2 and finally, Section 5.3 will conclude this chapter with a summary of the withdrawn conclusions.

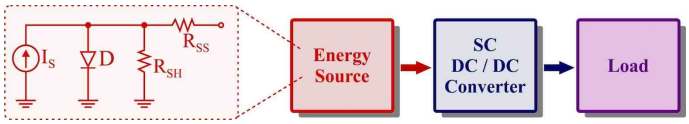
A PV cell is an energy source that can be conditioned into an operation point that yields the maximum power it can provide for a specific set of weather and light conditions. This operation point, the aforementioned MPP, is given by a current-voltage coordinate in its *I*-*V* characteristic for which the *P*-*V* curve achieves the peak value. For each coordinate on the *I*-*V* curve, the PV cell manifests an internal resistance given by the division of the voltage by the current values of that coordinate. For the MPP, we can define a value for that resistance given by

$$R_{MPP} = \frac{V_{MPP}}{I_{MPP}} \tag{5.1}$$

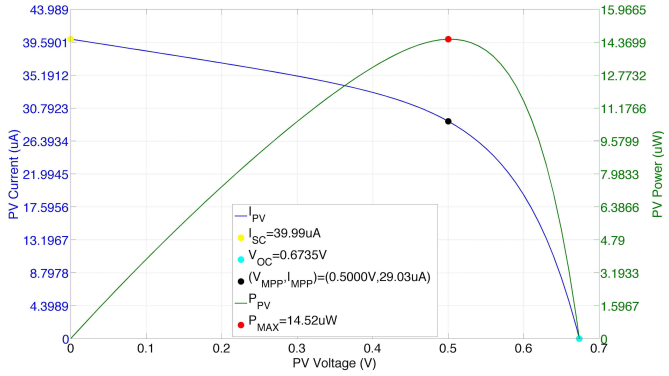
Taking into account results 4.26, 4.27 and 4.28, one might state that the PV cell operates at MPP when

$$R_{OUT} = n^2 R_{MPP} \tag{5.2}$$

To verify this assumption, a load resistance sweep was simulated, from $2 \times R_{MPP}$ to $6 \times R_{MPP}$, using a voltage doubler operating at $f_{sw} = 500\,\text{kHz}$ – a sufficiently high switching frequency for the losses of the converter to be neglected. The PV cell consisted on a current source - diode - shunt resistance - series resistance model, such as the one depicted in Figure 5.1a.



(a)



(b)

Figure 5.1: PV cell used in simulation. (a) current source-diode-shunt resistance-series resistance model. The electric parameters used are $I_S = 40\,\mu$ A for the photon current, the diode is a SPICE model with a saturatio current of 5 nA and an ideality factor of 3, $R_{SH} = 64\,\text{k}\Omega$ and $R_{SS} = 10\,\Omega$; (b) I-V characteristic of the simulated PV cell.

The electric parameters of the PV cell were set in order for the I-V profile to closely approximate the data obtained in Chapter 3. The obtained characteristic for these parameters is depicted in Figure 5.1b. The blue line is the I-V curve, signalled with the noteworthy coordinates that characterise the PV cell: the open circuit voltage, V_{OC}, the short-circuit current, I_{SC}, and the MPP, (V_{MPP}, I_{MPP}). The green line traces the P-V curve of the PV cell.

From Figure 5.1b, R_{MPP} can now be obtained as V_{MPP}/I_{MPP}, thus yielding $R_{MPP} = 17.224\,\text{k}\Omega$. The remainder of the electrical parameters of the simulation are $C_{IN} = 100\,\text{nF}$, $C_{FLY} = 1\,\text{nF}$, $R_{ON} = 1\,\Omega$ and $C_L = 100\,\text{nF}$.

The results of Figure 5.2 illustrate the effect of varying the load. In Subfigure 5.2a are clearly depicted the distinct load resistance values for which different ratio topologies withdraw from the PV cell the maximum amount of energy. Figure 5.2b shows that these optimal load resistance values are given by $n^2 R_{MPP}$ as the portrayed input power curves peak approximately when the load resistance is $4R_{MPP}$, $9R_{MPP}$ and $16R_{MPP}$ for the voltage doubler, tripler and quadrupler respectively. In other words, when $R_{IN} = R_{OUT}/n^2 = R_{MPP} = 17.22\,\text{k}\Omega$.

Setting switching frequency of the DC/DC converter to a value high enough such that the losses in the conversion block are not significative, the ideal load for a given converter ratio is thus $n^2 R_{MPP}$. It is, however, quite unlikely that the load manifests itself as n^2 times greater than the characteristic resistance of the PV cell for which the maximum power is extracted. Revisiting the

scheme on Figure 4.14 and computing together the SSL model simplification and the Maximum Power Transfer Theorem, one might say that, if $R_{OUT} = R_{SSL} + R_L$ then the maximum power the PV may provide will be extracted if $R_{OUT} = n^2 R_{MPP}$, for a given converter with a ratio of n. Taking into account that the value of R_{SSL} is a function of frequency then, if the condition

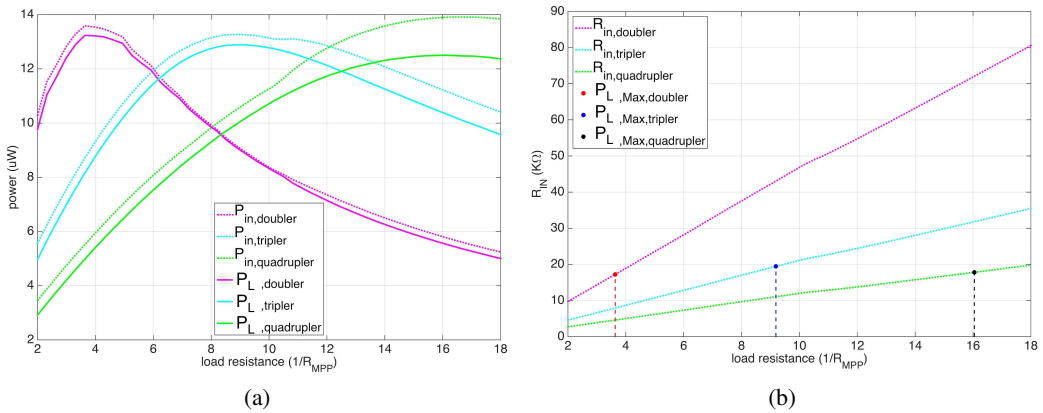
$$R_L < n^2 R_{MPP} \tag{5.3}$$

is verified, then there is a frequency for which the sum $R_{SSL} + R_L$ yields a load resistance value that biases the PV cell into converting maximum power. Replacing result 4.29 into the equality $R_{OUT} = n^2 R_{MPP}$ and solving in respect to the frequency, one obtains the frequency which sets the PV cell into its MPP, f_{MPP} as

$$f_{MPP} = \frac{(n-1)^2}{(n^2 R_{MPP} - R_L) C_{tot}} \tag{5.4}$$

If condition 5.3 is not met though, the conversion ratio n must be increased in order to maintain the MPP in the operation range, otherwise it is not achievable. However, one must keep in mind that the SSL resistance is ideally as low as possible. In other words, it is desirable to decrease the losses in the conversion block to a minimum. Indeed manipulating the SSL resistance though the frequency allows a degree of control to keep the PV cell operating at MPP but it can be costly in terms of conversion efficiency.

To assert the implications of manipulating the frequency in order to keep the PV cell at MPP, a simulation was runt, subjecting the doubler, tripler and quadrupler topologies to an output resistance variation but keeping the PV cell operating the the MPP. To do so, the frequency was dynamically changing according to (5.4), thus altering the value of R_{SSL} to hold the condition $R_{SSL} + R_L = n^2 R_{MPP}$. The electric parameters for the simulation were $C_{IN} = 100\,\text{nF}$, $C_{FLY} = 1\,\text{nF}$,



(a) (b)

Figure 5.2: PV energy system performance with load resistance for doubler, tripler and quadrupler topologies of the SC DC/DC parallel-series converter. (a) Input and output power; (b) Input resistance.

$R_{ON} = 1\,\Omega$ and $C_L = 100\,\text{nF}$.

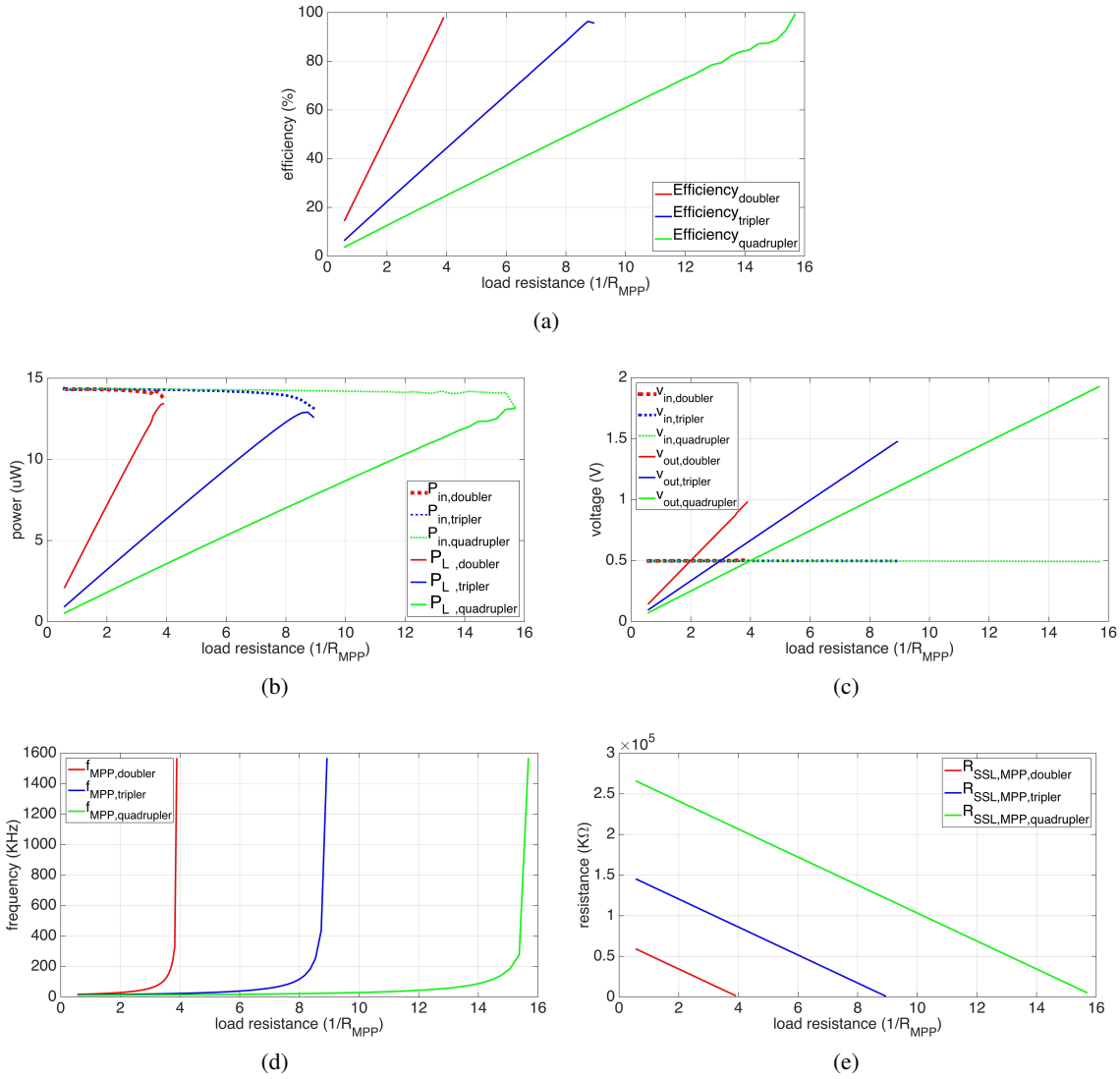


Figure 5.3: Load resistance sweep whilst keeping the PV cell at the MPP, when using the parallel-series voltage doubler, tripler or quadrupler. (a) Efficiency; (b) Input and output power; (c) Input and output voltage; (d) Maximum power point frequency; (e) SSL resistance.

Figures 5.3b and 5.3c portray an roughly constant input behaviour, which means that the frequency dynamically changing according to (5.4) indeed keeps the PV cell at the MPP. Nevertheless it is clear that doing so is quite hurtful to the efficiency of the conversion, as illustrated in Figure 5.3a.

The efficiency peaks when R_{OUT} approximates $n^2 R_{MPP}$. When it gets away from that optimal value, i.e. when R_L gets smaller, the only way to keep the PV cell at the MPP is to compensate the R_L decrease with an increase of R_{SSL}, i.e. lowering the frequency, in order to maintain $R_{SSL} + R_L = n^2 R_{MPP}$ – Figures 5.3d and 5.3e. Decreasing the frequency has exerts a drawback on the efficiency as seen in Figure 5.3a because a greater amount of power is being lost in the converter. On the other hand, holding the equality $R_{SSL} + R_L = n^2 R_{MPP}$ when operating with R_L close to $n^2 R_{MPP}$ may

require unfeasible switching frequencies as they tend to infinity when near n^2R_{OUT} – Figure 5.3d. Be that as it may, on Section 4.2, it became clear that frequencies over a given value ($\approx 500\,\text{kHz}$) yield near optimal converter performance thus it is an acceptable upper bound for the switching frequency.

Even though it is clear that manipulating the frequency allows the converter to keep the PV cell at MPP, it may hinder the overall performance of the system. Despite the fact that the PV cell is providing its maximum power, a significative portion of it is lost in the DC/DC conversion process. As the goal of the system is to maximise the power that is effectively output, keeping the cell at MPP through the means of frequency modulation may be too costly as the conversion becomes lossier for output resistance values farther from the optimal n^2R_{MPP} product. It remains to analyse the effect of manipulating the conversion ratio, i.e. the topology of the converter, in the conversion process, keeping in mind the goal to maximise the output power of the DC/DC converter.

From Figure 4.15, one can see that different topologies manifest peak performances at distinct load conditions. Assuming a constant frequency, sufficiently high for the losses of the converter to be neglected, and making use once more of the SSL model approach, for a specific ratio, the load power is given by (4.32). As the it displays a parabolic behaviour with R_L– refer to Figure 4.15 –, it is desirable to change topology when the load conditions are such that the load power curve of the topology of ratio $n+1$ (or $n-1$, when $n>2$) achieves higher values than the topology of ratio n. There is an exact value of the load resistance at which the topology must change, to keep the load power maximised. As previously, let us call that value $R_{L,switch}$. Graphically, it is the point at which the load power curves of two adjacent ratio topologies intersect. In theory, that point might be found making use of (4.32), setting $P_{L,n1} = P_{L,n2} =$ and solving in respect to R_L, thus obtaining, for two arbitrary adjacent ratios n_α and n_β

Next section will study the possibility to use the behaviour of the electrical parameters to maximise the power output from the converter, taking into account the analysis on Section 4.3.1.

5.1 Output Power Maximisation

In this section, the interaction of the PV cell with the converter will be studied in order to pinpoint the indicators that should be used to design a tracking scheme that keeps the system operating efficiently. As seen on previous Section, the manipulation of the frequency may indeed keep the PV cell operating at MPP. Be that as it may, doing so may become costly has the losses on the converter increase as the frequency decreases. It is thus desirable to keep the converter switching at a rate that maximises its efficiency without requiring unfeasibly high frequencies. The conversion ratio, i.e. the topology, provides a means to match the source impedance with the load.

For different topologies, considering a varying load, the output power peaks at distinct values of that load resistance. Ideally, a system capable of adapting the topology, would manifest, for a

given load, the most adequate configuration, in order to keep the power output at maximal values. It is, however, necessary to recognise when (and how) should the topology change.

Taking into account that the scope of this study is the indoor environment context and assuming the PV cell is an interchangeable part of the system, a simplistic and energy wise efficient method is desirable. This must be applicable for different PV cells and still yield optimal results.

One of the most widely reported method to operate at (approximately) the MPP of the PV cell is the *fractional open circuit voltage*. It relies on the geometric relation between the voltage at MPP – V_{MPP} – and the open circuit voltage – V_{OC}. This peculiarity of the characteristic curve of the PV cell constrains the ratio K, for which $V_{MPP} = K \times V_{OC}$ within a small range around ≈ 0.7.

Making use of the data gathered through the PV cell characterisation process, it was possible to verify, for each PV cell model on each day, the best K factor to use. The criterion was to find the fraction of V_{OC} which better approximates the energy profile when using the Fractional V_{OC} to the one obtained when operating always at MPP.

Using as an illustrative example the data collected for the IXYS SLMD121H04L model on the 11th of June, according to Figure 5.4d, the V_{OC} fraction that yielded better results was 0.63. This tracking efficiency is calculated taking into account the amount of energy gathered for a specific fraction of V_{OC}, over the energy amassed with the operation on the MPP. Figures 5.4a and 5.4b depict the operation point when using $K = 0.63$ – the red line –, superimposed to the operation at MPP – the black line. One can observe that using the Fractional V_{OC} results in an operation profile quite similar to the one at MPP. Figure 5.4c shows additionally that using this approach allows the conversion of an amount of energy – the blue line – rather close to the one when operating at the MPP – the red line. The remaining results for the other measured days and PV models can be seen in Appendix B. Nevertheless, the Fractional V_{OC} approach consistently yields interesting results. Using this approach allows the MPPT scheme to be nothing more than a comparison of the input voltage with a Fraction of the open circuit voltage of the PV, easily achievable in hardware.

However, this method can only be applicable to a wide range of different cases if the K fraction is indeed within a reasonably small range, allowing one to compromise with a constant value for K and still expect good results. To verify it this is indeed a safe assumption, the data gathered during the PV cell characterisation was analysed, in order to find, for each PV cell on each day, the value of K that provided the best results. Figure 5.5 maps all the obtained fractions of V_{OC} that resulted in better performance for each case.

One can observe that the best fractions of V_{OC} gather within an range roughly defined as $K \in [0.6, 0.8]$. This geometric relation may prove an interesting feature to be exploited in a PV energy harvesting system. Conventional Fractional V_{OC} makes use of this characteristic by compromising the conversion stage to a specific K factor and then, by sampling the V_{OC} voltage and computing KV_{OC} – a simple voltage divisor is able to scale down the V_{OC} –, it coerces the input voltage to that value, hopefully yielding good results. The typical scheme to maintain the input voltage at the V_{MPP}, is to change the frequency in order to set an input resistance that allows the input voltage to remain equal to V_{MPP}.

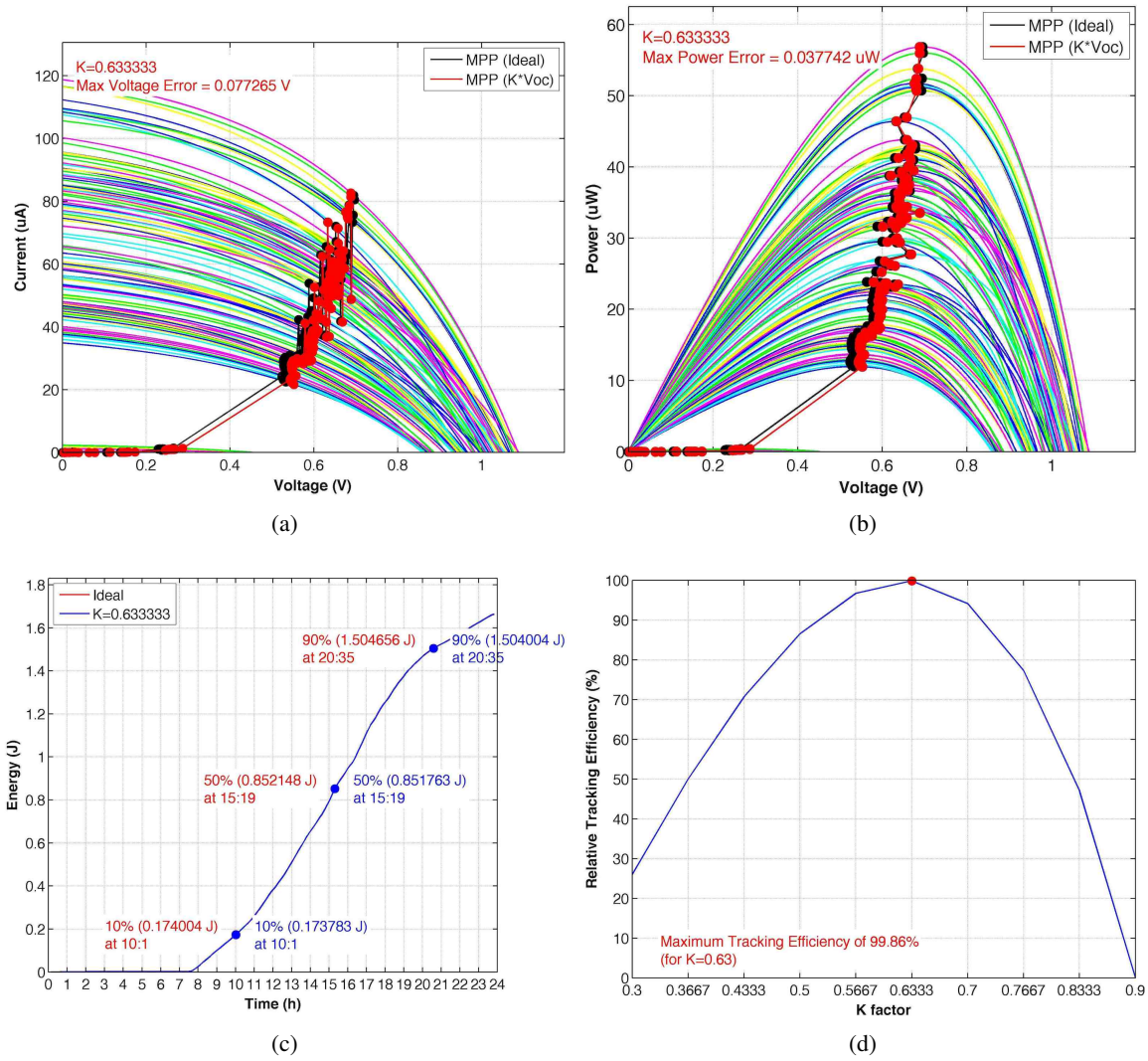


Figure 5.4: Comparison of the results when using the fractional V_{OC} *versus* operating at MPP for the IXYS SLMD121H04L model on the 11th of June. (a) *I-V* characteristic; (b) *P-V* characteristic; (c) Energy accumulation; (d) Tracking efficiency for different fractions of V_{OC}.

As seen on Figure 5.3, however, changing the frequency may lead to conversion losses, ultimately reducing the power conveyed to the load, despite the PV cell being at its MPP. If the goal is to maximise the output power, the impedance matching of the load to the source should be made by means of ratio – i.e. topology – manipulation. If we consider Figure 5.2a, it comes into attention the fact that, when considering the ratio n as the mechanism to adapt the source to the load (aiming for output power maximisation), for each ratio there is a range of operation, in terms of load resistance. In other words, it should only change the conversion ratio when the output power curves intercept. In the mean time, the ratio stays the same. Along that range of operation, the input voltage varies, monotonically, increasing with the load. This was verified for a circuit using an ideal voltage source with a constant source resistance, in Figure 4.16 and this behaviour still holds when a PV cell is the energy source. Figure 5.6 illustrates a mechanism to maximise the

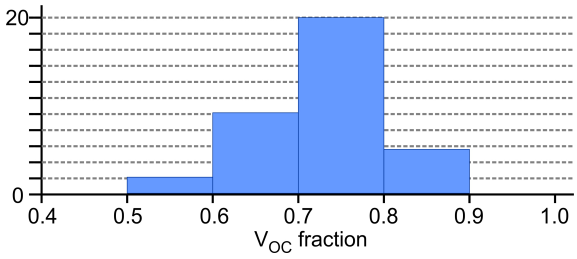


Figure 5.5: K ratios for KV_{OC} which better approximate the MPP.

output power for varying load conditions, considering the behaviour of the voltage.

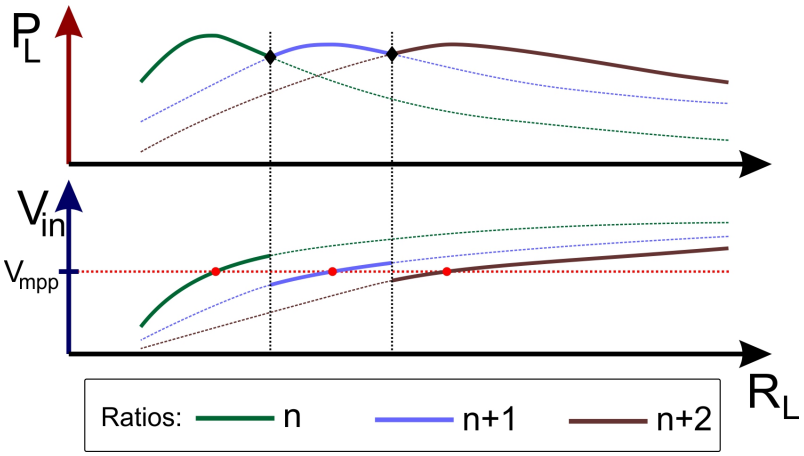


Figure 5.6: Load power maximisation scheme principle.

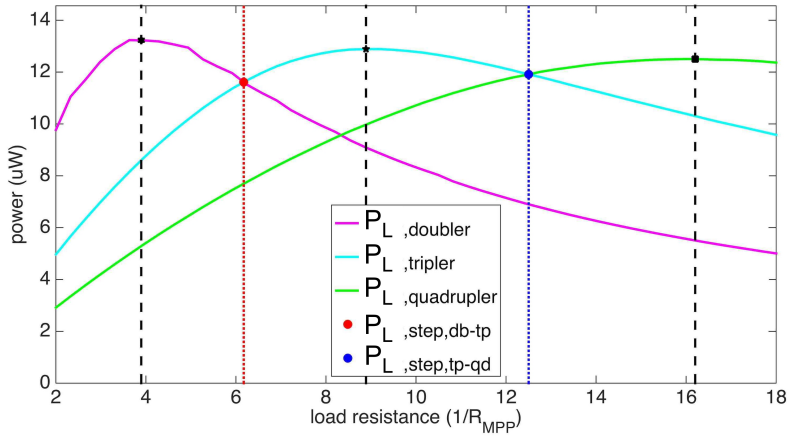
The illustrated scheme depicts the behaviour of the voltage and load power with the load resistance, for three arbitrary adjacent conversion ratios n, $n+1$ and $n+2$. One can see that when the input voltage is the V_{MPP}, the load power achieves its peak, decreasing, afterwards. An ideal load power maximisation scheme would change the conversion ratio in the instant that the load power curves intercept, thus keeping the operation in the range illustrated by the solid lines. This range, in terms of input voltage, includes V_{MPP} but spans above and bellow that value.

A noteworthy fact is that this range remains roughly constant for each ratio. In other words, let us assume than V_{in} varies within $[V_{MPP}-\sigma, V_{MPP}+\gamma[$, then, for a given ratio, when the input voltage increases to $V_{MPP}+\gamma$, if the ratio is increased, then V_{in} drops to $V_{MPP}-\sigma$. Conversely, if the input voltage lowers to $V_{MPP}-\sigma$, then decreasing the ratio rises its value to $V_{MPP}+\gamma$, thus keeping the PV cell biased in that operation range which in turn keeps the load power variation in the area depicted with the solid lines, on Figure 5.6.

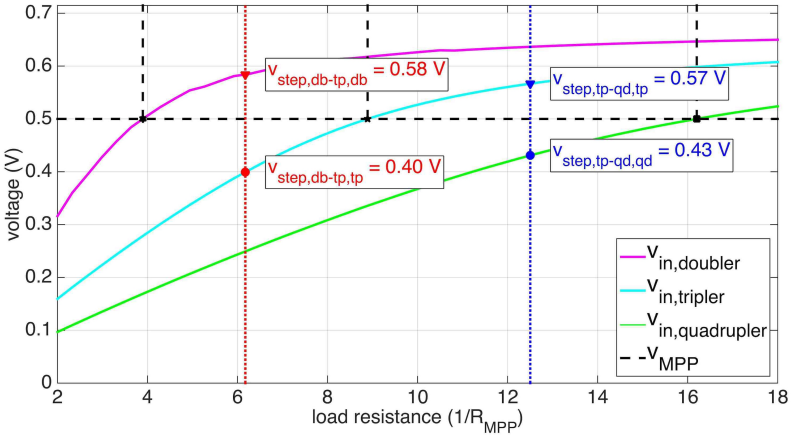
For this matter, R_L at $V_{MPP,n-1}+\gamma$ equals R_L at $V_{MPP,n}-\sigma$, R_L at $V_{MPP,n}+\gamma$ equals R_L at $V_{MPP,n+1}-\sigma$ and $V_{MPP,n}\pm\gamma,\sigma$ are the voltages values that signal when the ratio must be increased or decreased, respectively.

Figure 5.7 overlays the data from the simulation illustrated in Figure 5.2 with the previous considerations. Recalling the simulation parameters: $C_{IN}=100\,\text{nF}$, $C_{FLY}=1\,\text{nF}$, $R_{ON}=1\,\Omega$,

$C_L = 100\,\text{nF}$ and $f_{sw} = 500\,\text{kHz}$.



(a)



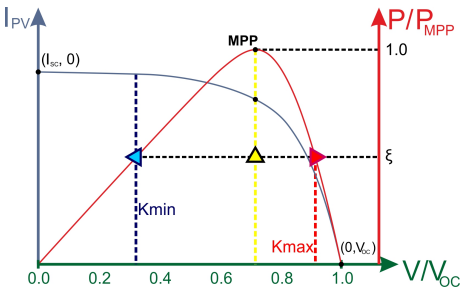
(b)

Figure 5.7: Behaviour of the load power and input voltage for a varying load. (a) Load power; (b) Input voltage.

In Figure5.7a, the points $P_{out,step,db-tp}$ and $P_{out,step,tp-qd}$ signal the intersections of the output power curves for the doubler/tripler and tripler/quadrupler, respectively. These points signal when the ratio should change, in order to keep the output power maximised. Tracing those points into Figure 5.7b, it is clear that both transitions – doubler to tripler and tripler to quadrupler –, occur at a given load value that yields values for V_{in} quite approximate in both counts. Using the previous notation, one can see that, for the doubler $V_{MPP,2} + \sigma = 0.58\,\text{V}$, for the tripler $V_{MPP,3} \mp \sigma, \gamma = [0.40\,\text{V}, 0.57\,\text{V}[$ and for the quadrupler $V_{MPP,2} - \sigma = 0.43\,\text{V}$. This shows that the range $[V_{MPP} - \sigma, V_{MPP} + \gamma[$ remains approximately constant.

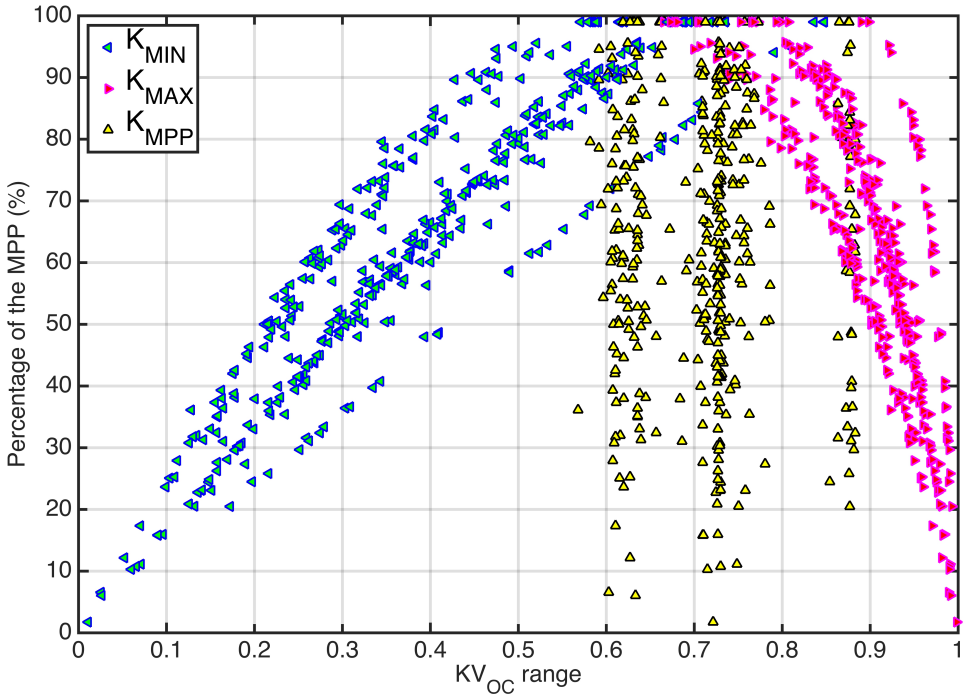
Making use of the same geometric principle on which the Fractional V_{OC} method is based, one can define an admissible range for the input voltage of the converter, based on a proportionality with the open circuit voltage that allows the output power to remain approximate to its maximum. For this case, considering the PV cell illustrated in Figure5.1, with $V_{OC} = 673.5\,\text{mV}$, the range $[V_{MPP} - \sigma, V_{MPP} + \gamma[$, defined in terms of V_{OC} would thus be $[K_{MIN}V_{OC}, K_{MAX}V_{OC}[\approx [0.6V_{OC}, 0.9V_{OC}[$.

Making use of an admissible range for the input voltage may provide an interesting compromise between simplicity and accuracy. In order to get a more in depth perception of the feasibility of this mechanism, an analysis over the data gathered in the PV cell characterisation was made, in order to assert about an acceptable range $[K_{MIN}V_{OC}, K_{MAX}V_{OC}[$ to use in order the make use of the advantages of a multi ratio approach.



(a)

Figure 5.8: Fractional V_{OC} operation ranges *versus* output power variation formulation example.



(a)

Figure 5.9: Fractional V_{OC} operation ranges *versus* output power variation analysis results.

This formulation is better explained in Figure 5.7. The yellow triangle locates the MPP in terms of V_{OC}. The two remaining triangles limit the range within the PV cell voltage may be – $V_{in} \in [K_{min}V_{OC}, K_{max}V_{OC}[$ –, in order to allow the output power to vary between MPP and ξ. The principle to be exploited is the following: from Figures 4.16 and 5.7 one can verify that, with the load variation, the power conveyed to that load presents a parabolic behaviour. It peaks when

$R_L = n^2 R_S$ (or $R_L = n^2 R_{MPP}$ when the source is a PV cell). One should bare in mind that the converter if operating at a frequency high enough for the SSL resistance to be neglected, when compared to the load resistance. This assumption will be used henceforth.

The ideal instant at which the topology should change is when these power curves of two adjacent ratios intercept, thus keeping the output power maximised for a given load. If one assumes that the load power curves intercept when their value falls to a percentage of its maximum – ξ –, which is roughly constant, regardless of the topologies and, that the input voltage varies within a range which is also reasonably constant – $[V_{MPP} - \sigma, V_{MPP} + \gamma[= [K_{MIN}V_{OC}, K_{MAX}V_{OC}[$ – then one can use the input voltage to determine when the topology should change. Defining this output power value as a percentage ξ of the maximum power and assuming the converter is operating at a frequency high enough for its losses to be non relevant, then one can state that the load power closely resembles the power extracted from the PV cell. Taking this into account and making use of the data gathered for the PV cell characterisation process, each *P-V* curve of the gathered data pool was subject to the following procedure: firstly, the MPP was found, in order to have the reference of the peak of that PV curve – this point is then expressed in terms of the fraction of the V_{OC} at which it occurs and depicted by the yellow triangles in Figure 5.9a; Secondly, the *P-V* curve was iterated in order to find, on its rising and falling edges, the points at which the power lowered to a given percentage of the MPP ξ, thus yielding the blue and red triangles on the Figure. On Figure 5.9a, each pair of blue and red triangles expresses the input voltage range $[K_{MIN}V_{OC}, K_{MAX}V_{OC}[$, for which the power extracted from the PV cell may vary between the MPP and ξ. The yellow triangles signal the voltage value, normalised by the V_{OC} at which the MPP occurs.

Considering Figure 5.7a, one may observe that the output power at which the conversion ratio should be stepped up or down is approximately 90 % of the peak output power. In Figure 5.9a, a 90 % power drop results in an acceptable operation range of $[K_{MIN}V_{OC}, K_{MAX}V_{OC}[\approx [0.55V_{OC}, 0.85V_{OC}[$, as this interval gathers most of the operation range limits for the considered power drop. In other words, the input voltage would be allowed to vary within $0.55V_{OC}$ and $0.85V_{OC}$. If it rises to $0.85V_{OC}$, then the ratio should be increased. Conversely, if it falls to $0.55V_{OC}$, then the ratio should be decreased, in order to keep the output power above 90 % of the peak output power.

Using this geometric relation of the characteristic of the PV cell wilds interesting results and, more importantly, an output power maximisation scheme quite simple and straightforward. In theory a voltage division mechanism would be able to provide the V_{OC} faction, which in turn would be used in a voltage comparison mechanism with an hysteresis to provide the operation range of the input voltage, normalised by the V_{OC}.

This geometric relation has, however, some dependence on the PV cell in use. On Appendix G, the previous analysis was made, however, filtering the results by PV cell model. It becomes clear that, due to the different *I-V* characteristics of different PV cells, this analysis yields different $[K_{MIN}V_{OC}, K_{MAX}V_{OC}[$ ranges of operation to maximise the power conveyed to the load.

There are, however, other concerns when designing such an energy harvesting system, besides

the power conditioning mechanism. next section will delve on some additional concerns to take into account when devising an efficient energy harvesting system.

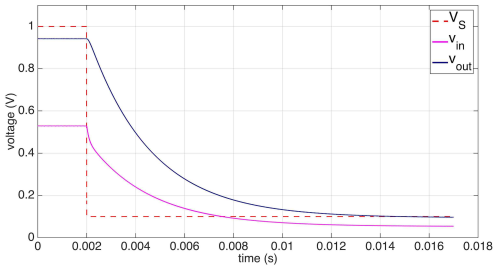
5.2 Additional Energy Concerns

5.2.1 Load Discharge

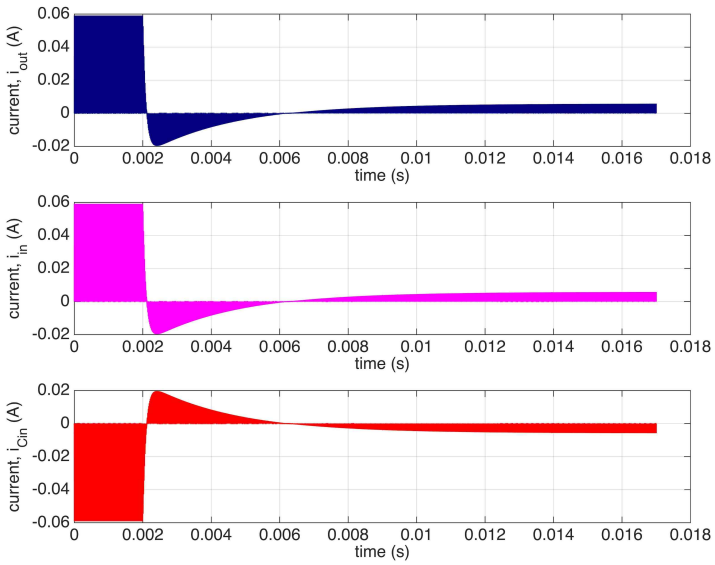
As an energy harvesting system, the main goal is to maximise the output power, thus allowing higher consumption loads to make use of the system or, alternatively, a higher amount of energy to be stored. One very important aspect is to minimise the losses throughout the system and deliver as efficiently as possible the harvested power to the load. For an energy harvesting system that makes use of the PV energy conversion as the power source and an SC DC/DC converter as the power conditioning stage, there is a very important aspect to take into account that comes from the inherent time variability of the energy source. Due to several reasons, but mainly due to the light irradiance variation during the day, there are instants at which the energy converted by the PV cell suffers a drop. For example, if a bystander passes near the PV cell and casts a shadow that lowers the available power on the system. Considering a lossless converter with conversion ratio n, outputting a voltage equal to nV_{in}. Upon that event, the input voltage would become $V_{in}{}^{-} < V_{in}$, resulting in an output of $nV_{in}{}^{-} < nV_{in}$. It is very important to understand if, given this occurrence, the load would discharge part of the amassed power to the input, thus inverting the energy flow from source-load to load-source. An SC DC/DC converter is a bidirectional circuit. If an SC DC/DC converter with a ratio n has its output an input terminals switched, it becomes an SC DC/DC converter with a conversion ratio of $1/n$. This means that there is the possibility for the energy to invert its flow, which would result in a counterproductive outcome. To understand if this is indeed the case, a piecewise linear voltage source was used to simulate the energy supply variation with time.

The source was kept at 1 V sufficient time for the transient phase of the output voltage to end. After the output achieved steady state, the voltage source lowered the voltage to 100 mV within 1 ps. The power converter used in the simulation was a voltage doubler and the remaining simulation parameters are $R_S = 10\,\text{k}\Omega$, $C_{IN} = 100\,\text{nF}$, $C_{FLY} = 1\,\text{nF}$, $R_{ON} = 1\,\Omega$, $C_L = 100\,\text{nF}$ and $f_{sw} = 100\,\text{kHz}$. Figure 5.10b illustrates the evolution of the current at the converter output and input terminals and at the input capacitor cathode. It is clear that, at the voltage drop instant, the output current inverts its direction, flowing *into* the converter. This inversion is verified also on the converter input terminal and on the input capacitor. It becomes clear that a power drop on the source causes the load to discharge part of its energy to the source. Making use of the SSL output model approximation – Figure 4.12 – it becomes clear that, if the input voltage V_{in} lowers such that, for a converter of ratio n, $nV_{in} < V_{out}$, then, the current *must* flow from the output to the input, in order to achieve equilibrium.

This hints about the necessity to include in a system where the energy source is time variant, a mechanism that inhibits the energy flow to invert its direction. Has the main goal is to maximise



(a)



(b)

Figure 5.10: Output variation due to a source energy drop. (a) Voltage; (b) Current.

the output energy, it must only flow from to the output and never otherwise.

5.2.2 Dormant Time Periods

Related to the previous issue is the fact that the system must be able to enter a low consumption state when the energy source is not able to provide an acceptable amount of energy. A typical period of low supply would be the night time, for a light based energy harvest system. As such, keeping the system switching would not only require power to produce the switching signals but would also cause additional losses due to the effect discussed in Subsection 5.2.1. Ideally, one would want the system to recognise it is not being properly supplied and suspend or delay the switching. On [73], the author devises an elegant solution to overcome the problem of the excessive consumption that a switching system may suffer when the energy supply drops. In his work, he proposes an approach to the Fractional V_{OC} MPPT method on which a phase controller, which generates the switching signals, adapts dynamically and automatically the switching frequency. However, this is achieved by an asynchronous state machine (ASM) that runs through its states

sequentially, which in turn produce the signals that drive the switches. The power conditioning stage consists on a voltage doubler whith a charge reusing scheme that replaces the conventional flying capacitor with two complementary metal oxide silicon capacitors (MOSCAP). Finally, the aforementioned ASM operates as follows. State 1 produces a phase signal that allows one of the MOSCAPS to be charged. If the MOSCAP voltage is higher than 95 % of the input voltage V_{in} *and* $V_{in} > V_{MPP}$, with $V_{MPP} = KV_{OC}$, then it advances to state 2. In state two the first MOSCAP is discharged and this state is kept with a delay circuit until it automatically advances to state 3. On state 3, when the second MOSCAP is, in turn, at a voltage higher than 95 % of V_{in}, then the ASM advances to state 4 and discharges the second MOSCAP during a minimum time guaranteed by another delay circuit. The ASM then returns to state 1, completing a run through all its states. This is an elegant solution that replaces a typical oscillator and a possibly complicated computational method to adapt the frequency, with a relatively simple method based on delays and comparators that modulates the frequency to keep $V_{in} \approx V_{MPP}$. However, according to the results illustrated in Figure 5.3, using the frequency to alter the input resistance of the converter, despite effectively allowing the input voltage to be biased to V_{MPP}, it may result in losses in the conversion stage. Moreover, this works advocates the adaptation of the load to the source impedance by ratio manipulation, keeping in mind the output power maximisation, which is not, as previously analysed, necessarily the same as PV cell power maximisation. Nevertheless, this ASM approach may be slightly altered to suit the characteristics of a multi ratio system, thus benefitting from its advantages. An adequate algorithm would be the one depicted in Figure 5.11.

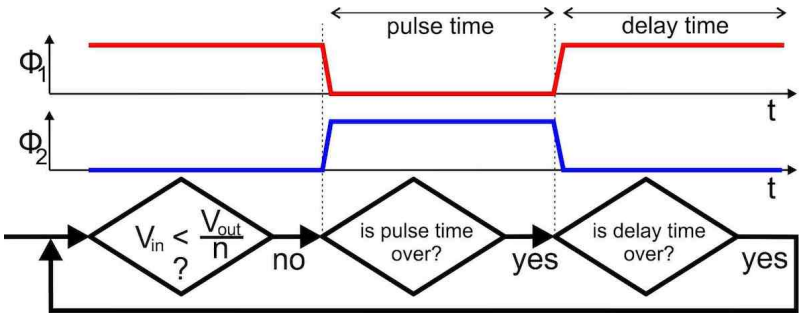
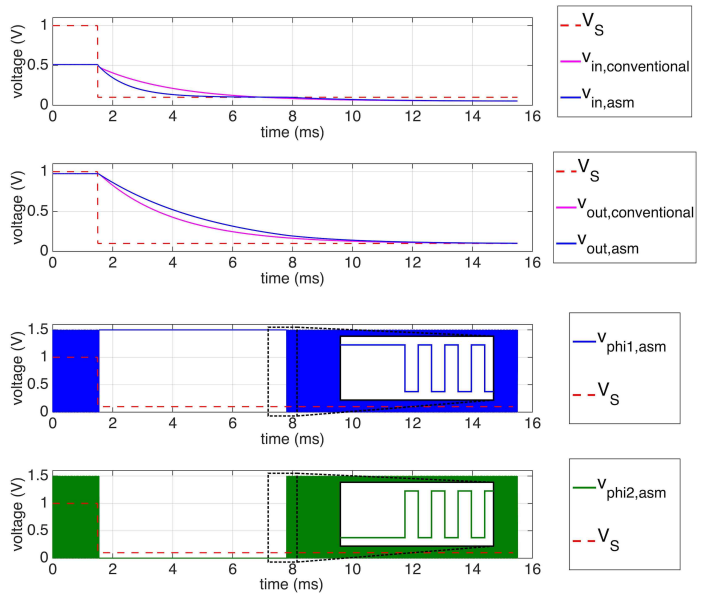


Figure 5.11: Asynchronous state machine algorithm.

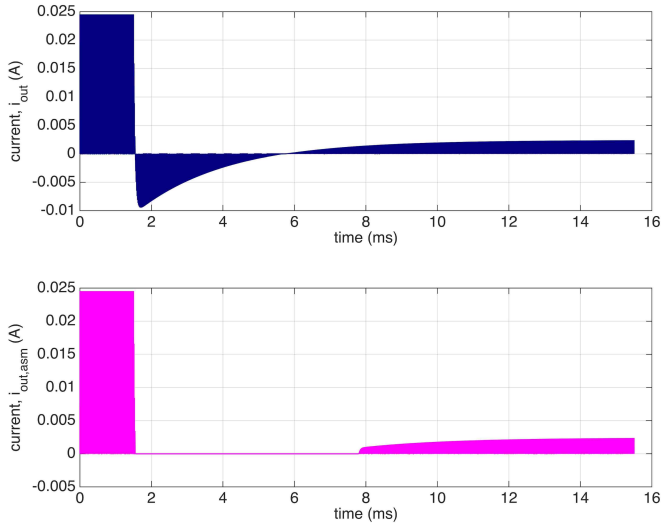
Considering, as an example, a voltage doubler converter as the power conversion stage, the ASM starts with Φ_1 high and Φ_2 low, i.e. the flying capacitor is in parallel with the source, thus being charged. If $V_{in} > V_{out}/2$ then Φ_1 goes low and Φ_2 high – the flying capacitor discharges to the load –, for a predefined pulse width duratio. After the duratio of the pulse the signals return to their original states and remain like so for a predefined delay time. After this, the algorithm restarts. The sum of the predefined pulse width and delay time defines a minimum period – or a maximum frequency – at which the switching may occur. Because only an ideal converter can achieve $V_{out} = nV_{in}$ then it is expected that the system keeps oscillating as long as the source keeps supplying power. However, if the source suffers a power drop, then the condition $V_{in} > V_{out}/2$ no longer holds and the controller keeps the switching signals in their original state – Φ_1 high and Φ_2

low, thus isolating the load from the rest of the system and inhibiting it to discharge to the input.

To verify the feasibility of such approach, an ASM phase controller was described in VerilogA, according to the algorithm in Figure 5.11, and simulated in Spectre. The behavioural model can be consulted in Appendix J.1. The converter under the ASM control was a voltage doubler and the remaining parameters were $R_S = 10\,\text{k}\Omega$, $C_{IN} = 100\,\text{nF}$, $C_{FLY} = 1\,\text{nF}$, $R_{ON} = 1\,\Omega$ and $C_L = 100\,\text{nF}$. The simulation was the same as in Subsection 5.2.1. A piecewise linear voltage source allows the load to reach steady state and the power it supplies is reduced. The conventional oscillator driven system is compared with one controlled by the ASM here described.



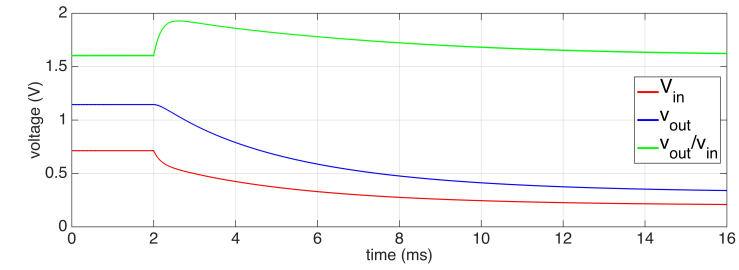
(a)



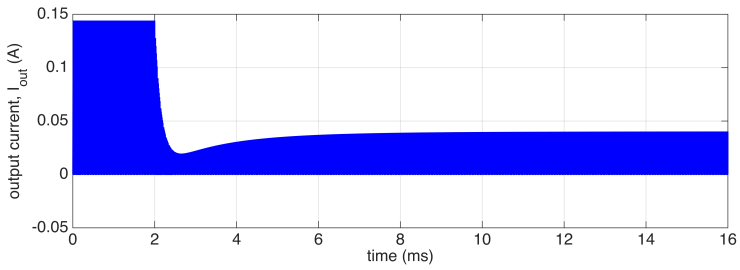
(b)

Figure 5.12: ASM phase controller results when the system is subject to a source energy drop. (a) Voltage; (b) Current.

Figure 5.12 illustrates the results of the simulation. It is clear that, when the source lowers its energy supply, V_{in} falls bellow $V_{out}/2$ thus causing the ASM to suspend the oscillation. When this happens, the power cannot flow from the load to the source, as seen when using a conventional oscillator driven system. It is observable that the load of the system running with the ASM phase controller, discharges at a slower rate than its conventional counterpart. When the supply is low, or non existent – as during the night –, it becomes desirable to lower the power consumption of the system. Keeping the switching process freely running requires power and may even induce a counterproductive effect, as seen in Subsection 5.2.1. This approach, however, provides a possible approach both elegant and effective, that operates based on delay circuits and comparators but nonetheless configuring an adaptive automatic phase controller. Nevertheless, when considering a PV cell energy harvesting system there is a particularity that must be prevented. If the system stops switching to prevent the load from discharging to the source, the PV cell will be at open circuit leading V_{in} to V_{OC}. The condition $V_{in} > V_{out}/2$ is then verified once more and the system restarts the switching. A possible solution would be to disconnect the PV cell from the system. However, from Appendix B one can observe that, despite the PV cell may lower its output power, these changes do not occur quickly enough for this safety mechanism to be triggered There is a gradual decrease in the PV cell output and the converter is able to keep conveying power to the load. Indeed, varying the PV cell characteristic curve, through simulation, in a way that mimics the behaviour of a real model, it was not possible to verify the charge reversal illustrated in Figure 5.10.



(a)

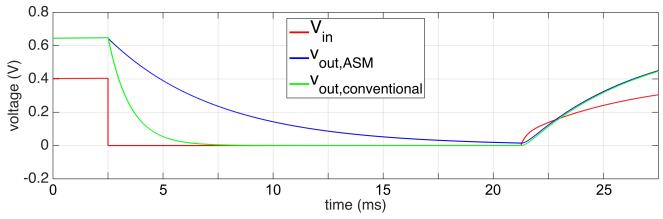


(b)

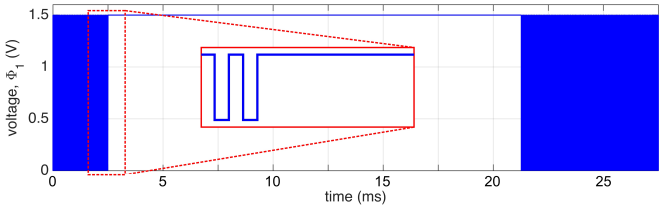
Figure 5.13: ASM phase controller results when the system is subject to a source energy drop with a PV cell as energy source. (a) Voltage; (b) Current.

As depicted on Figure 5.13, even though the PV cell suffers an energy output drop, there is no energy flow reversal and the relation $V_{in} > V_{out}/2$ is held, henceforth the switching does not need to to stop as there is no energy being discharged to the source. On Figure 5.13a, the

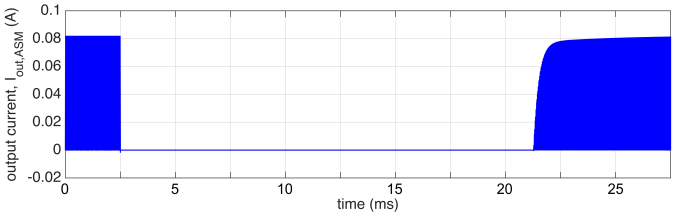
V_{out}/V_{in} ratio is portrayed, revealing that the condition $V_{in} > V_{out}/2$ remains true so, the phase controller never interrupts the switching. For this analysis, the behavioural PV cell model in Appendix E was used as energy source. Initially it was parametrised to generate an I-V curve with $I_{SC} = 100\,\mu$A, $V_{OC} = 1$ V and $A = 0.373$ – refer to Section 3.4 for the meaning of these parameters on the behavioural model – and, at 2 ms of the illustrated range in Figure 5.13, these parameters dropped to $I_{SC} = 20\,\mu$A, $V_{OC} = 0.5$ V and $A = 0.2575$. The remaining simulation parameters are $C_{IN} = 100$ nF, $C_{FLY} = 1$ nF, $R_{ON} = 1\,\Omega$, $R_L = 40\,$kΩ, $C_L = 100$ nF and $f_{sw} = 100$ kHz.



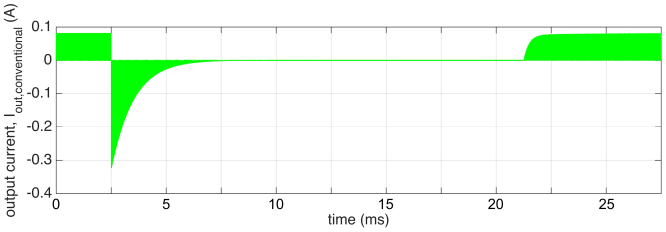
(a)



(b)



(c)



(d)

Figure 5.14: ASM phase controller results when the system is subject to a dramatic source energy drop with a PV cell as energy source. (a) Voltage; (b) Φ_1; (c) Output current whith ASM controller; (d) Output current with conventional non stop switching.

However, if the energy supply drop is severe, for example if the PV cell is covered, thus reducing its output drastically, or, considering an indoor environment, when the artificial lights

are turned off, this mechanism provides the advantage of preventing the load from discharging to the source, thus increasing the time a load would withstand solely on the energy stored in the output capacitor. Figure 5.14 illustrates the results of a simulation of the same system used previously in Figure 5.13, in which the PV cell suffers a dramatic energy supply drop for a short period of time. This is to mimmic the effect of the PV cell being temporarily covered, subjecting the load to an energy supply starvation. At 5 ms the supply drops thus triggering the ASM safety mechanism. From Figure 5.14b one can see that the switching stops. As a result, the output voltage of the system with the ASM mechanism lowers at a slower rate than the one with a conventional non stopping switching. Indeed, from Figure 5.14d, one can see that the latter suffers from an inversion of the current, whereas the first does not. At 12.5 ms the source returns to its initial state and the ASM controlled system resumes the switching process. One can see in Figure 5.14a, the conventional system output voltage fell to zero. This would possibly lead to a system shutdown of the load device, in a real situation. Using the ASM mechanism, however, results in a slower decrease of the voltage, which never reaches zero volt.

This dynamic mechanism to control the phase of the converter, besides serving as a preventive measure for the load discharge, provides also an automatic control mechanism the suspends the switching when there is lack of energy, such as during the night, when there is no energy available to provide to the load, thus rendering the switching unnecessary, harmful, even.

This work exploits the geometric characteristics of the PV cell *I-V* curve, regarding the V_{OC}, then the open circuit must be somehow sensed to use in these computations. There mainly two ways of measuring the open circuit voltage. One of them consists on disconnecting the PV cell from the circuit during a short duration, and measuring the voltage at the PV cell terminals, the V_{OC}. Another one is to use a pilot cell, with material characteristics equal to the one used as power source. This pilot cell, however, serves the sole purpose of providing the V_{OC}, not contributing as a power source. The first method has the disadvantage of temporarily disconnecting the source from the system, which yields, inherently, energy loss as, during that time, the energy is not being conveyed to the output. However, from the data obtained during the PV cell characterisation, one may observe that, although there is a time variance of the PV cell characteristics, this variation occurs within minutes or perhaps even within seconds – refer to Appendix B. This variation, when compared to the time constants of the system – in the order of milliseconds –, is reasonably slow. This in turn allows the V_{OC} sampling to occur at a frequency equally slow. The energy loss during the disconnection time is further reduced due to this ASM approach that detects a drop on the source energy supply and suspends the switching process. A conventional V_{OC} sensing mechanism, operating together with the ASM phase control algorithm, avoids the necessity of an additional PV cell to measure the V_{OC}, thus sparing system area and hardware overhead and increasing its deployability.

5.3 Conclusions to This Chapter

There are several ways to maximise the energy extracted from the PV cell. The most widely reported in literature is the frequency modulation of the signals that drive the switches. However, this method may lead to undesirable losses in the conversion stage.

The PV cell can effectively be biased into the MPP, by manipulating the input resistance through the frequency. If the output resistance, i.e. R_{OUT} is inferior to n^2R_{MPP}, one may reduce the frequency and increase the SSL output resistance to approximate $R_{OUT} = R_{SSL} + R_L$ from n^2R_{MPP}. In this situation the PV cell is biased into outputting the maximum power it can. However, decreasing the frequency to increase the input resistance is actually increasing the amount of energy dissipated in the converter, "artifially" increasing its input resistance. This means that, even though the PV cell it at the MPP, a lower amount of energy is delivered to the load because it is being lost in the conversion stage. Being at the MPP does not necessarily mean that the energy delivered to the load is as high as it can be.

On the other hand, if the output resistance is superior to n^2R_{MPP}, then one can increase the frequency to reduce the SSL output resistance and approximate R_{OUT} from n^2R_{MPP}, as the value of R_{SSL} is inversely proportional to the switching frequency. However, if the converter is already operating at a frequency that minimises the conversion losses, such as 500 kHz, for a converter with $C_{IN} = 100\,\text{nF}$, $C_{FLY} = 1\,\text{nF}$, $R_{ON} = 1\,\Omega$ and $C_L = 100\,\text{nF}$, further increasing the frequency has no relevant effect.

An alternative method is to alter the topology of the converter circuit, i.e. its conversion ratio, in order to match the load impedance with the impedance of the PV cell. This mechanism aims to maximise the output power, which is, as stated, not necessarily the same as maximising the PV cell output. This method must configure the converter to the topology that yields the best overall performance for at a given instant.

This chapter discussed an algorithm to control this multi ratio approach was also discussed on this chapter. It exploited the geometric properties of the *I-V* curve of the PV cells and the monotonic behaviour of the input voltage, as indicators to when the topology must change in order to keep the power output within optimal range. There is a range in which the input voltage may vary that allows maximum power to be delivered to the load. Whenever the input voltage reaches the lowest or highest value of that range, the conversion ratio must decrease or increase, respectively, in order the maintain the load power maximised. This approach benefits from the characteristics of the PV cell as this range of input voltage can be defined by comparison with the open circuit voltage of the PV cell.

However, this mechanism was developed taking into consideration the data gathered during the PV cell characterisation, concerning the characteristics of different PV cells. The results of this mechanism may be further enhanced if it is configured for a specific PV cell. Although the analysed modules were somewhat similar in terms of energy levels and *I-V* there are differences amongst these devices. Namely because they are built from different technologies, which lead to distinct behaviours. As such, designing a mechanism dedicate to a single PV cell model may yield

better results.

This chapter also approached some additional concerns when devising an energy harvesting system. A DC/DC converter is a bidirectional device. This means that there is the possibility for the energy to flow from the load to the charge. This is an undesirable effect that may occur if the PV cell suffers an energy supply drop, for example if a shadow is cast over its surface. To overcome this issue, an ASM control scheme was employed. It allows a dynamical and automatic frequency control that suspends the switching process when there is a supply energy drop.

Additionally it spares the system from additional power consumption by avoiding unnecessary switching – for example at night, when there is no energy supply, therefore, no need to keep the flying capacitors switching.

The power conversion stage was studied in this chapter. It was approached under the scope of an indoor light energy harvesting system, thus the energy efficiency was held as a key aspect to take into account. This analysis was made, aiming for a simple approach and keeping in mind the main goal to maximise the energy delivered to the load. Moreover, doing so without disregarding the constrains imposed by a system that must thrive in an environment with low energy availability, subject to time variation of both the source and the load.

Chapter 6

Photovoltaic Energy Harvesting System - Proposed Approach

This chapter presents a solution proposal for an energy harvesting system based on photovoltaic energy.

The system aims to maximise the power conveyed to the output, while being subject to indoor lighting environment conditions. The impedance matching process between the source and the load is made by means of a multi ratio approach. The conversion stage is controlled by an algorithm that selects the most adequate topology, i.e. ratio, for a given instant, in order to approximate R_L/n^2 from R_{MPP}, being the latter the internal resistance of the PV cell when operating at the MPP, i.e. V_{MPP}/I_{MPP}. The converter converter is a switched capacitor DC/DC converter, with a parallel-series topology, adapted to allow reconfigurability of the number of stages of conversion, thus manipulating the conversion ratio. The phase of the converter, i.e. the state of the switches, is controlled by an asynchronous state machine, based on the work proposed on [73], that implements an algorithm to prevent the load from discharging to the source, when the energy supply is drastically lowered. Additionally, it provides an automatic mechanism to suspend the phase switching when it is not necessary, i.e. when the source is not supplying energy, such as during the night.

On Section 6.1 the system blocks will be presented and their operation will be explained. Section 6.2 will present the results of the system operation validation. Afterwards the system operation will be studied when conformed to indoor environment conditions on Section 6.3. Afterwards, on Section 6.4, and optimisation of the proposed algorithm will be presented, which aims to limit the output voltage to a reference – the rated voltage of the storage device – in order to avoid structural damage to the latter. Section 6.5 follows, with a system enhancement to allow unitary and step down voltage conversion. Finally, Section 6.6 will conclude this chapter.

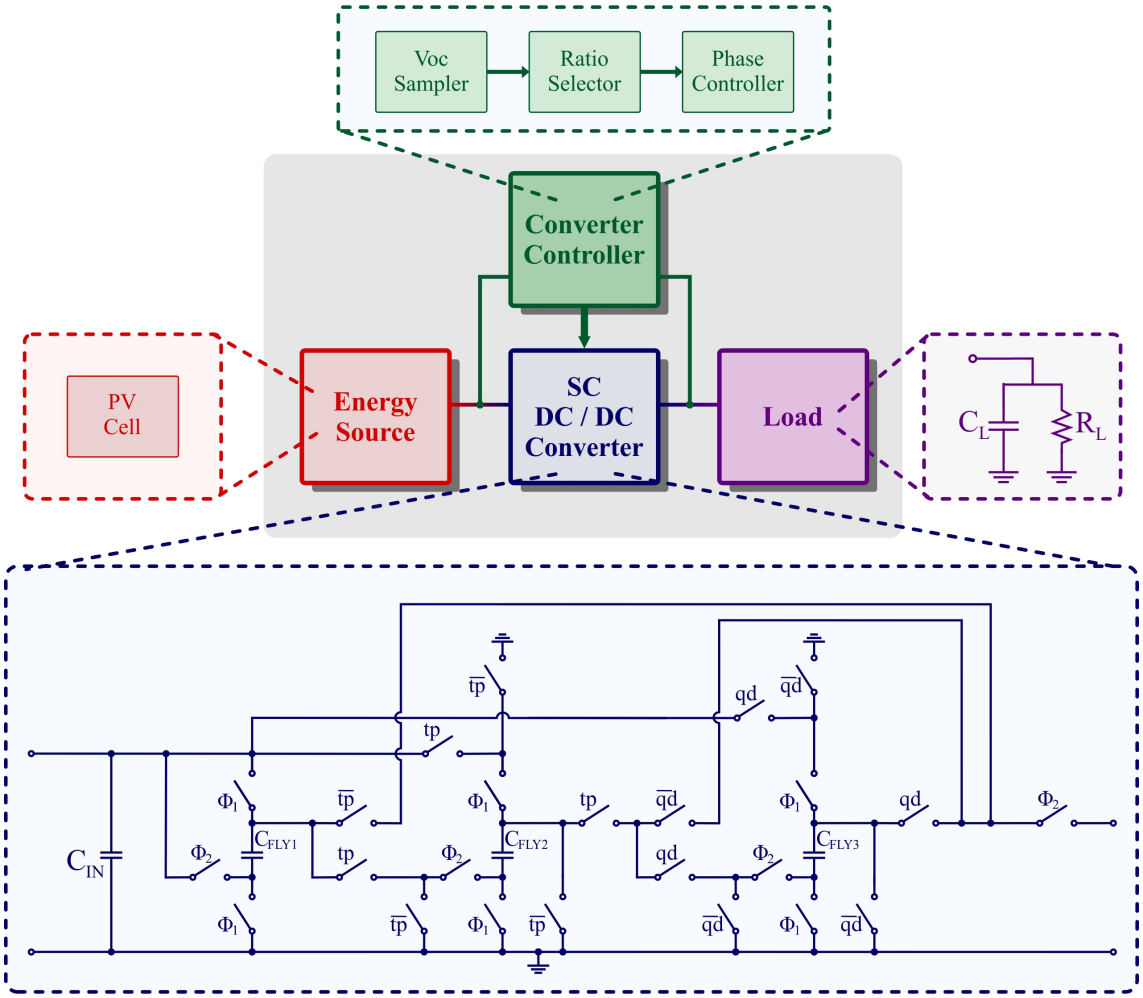


Figure 6.1: Proposed system architecture.

6.1 Proposed System Overview

Figure 6.1 depicts an architectural representation of the proposed energy harvesting system. The power conditioning stage consists a reconfigurable SC DC/DC parallel-series converter. As a proof of concept, its reconfigurability allows the conversion ratio to be $n \in \{2,3,4\}$, i.e. voltage doubler, tripler and quadrupler. Its control system, implemented in Verilog-A, is comprised of three functional blocks, the V_{OC} sampling block, the ratio selector and the phase controller. Together, these implement an algorithm of impedance matching that aims to maximise the power conveyed to the output. this section will provide an explanation of each one of the latter and how they operate as a system.

6.1.1 Control Block - The V_{OC} Sampler

The V_{OC} sampling block – refer to Appendix H – performs a periodic sampling of the open circuit voltage, which it then outputs as a constant value between samples. Essentially it is a

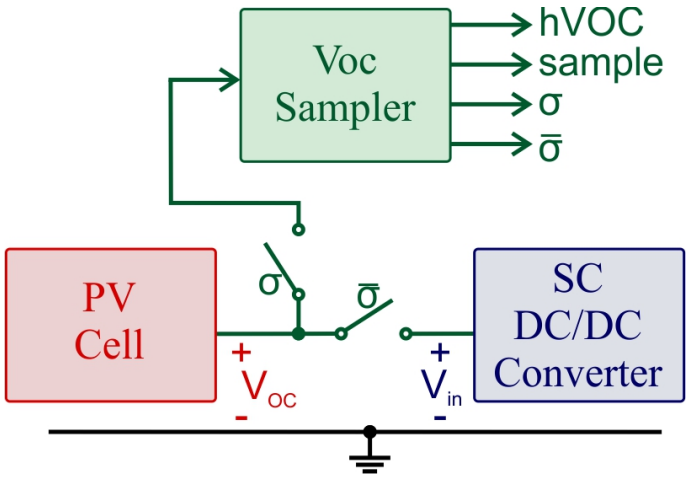


Figure 6.2: The V_{OC} Sampler block.

sample and hold circuit. To do so it makes use of two switches which temporarily disconnect the PV cell from the remaining system, allowing the V_{OC} sensing to be made – refer to Figure 6.2. These switches are controlled by the signal σ and its negated form $\overline{\sigma}$, to ensure mutual exclusivity, i.e. when one is closed, the other is open. These signals are generated by the V_{OC} sampling block. It also outputs the *hVOC* signal – the held V_{OC} sample – and the *sample* signal, which is used in simulation as a flag to signal when the samples are made.

6.1.2 Control Block - The Ratio Selector and the Phase Controller

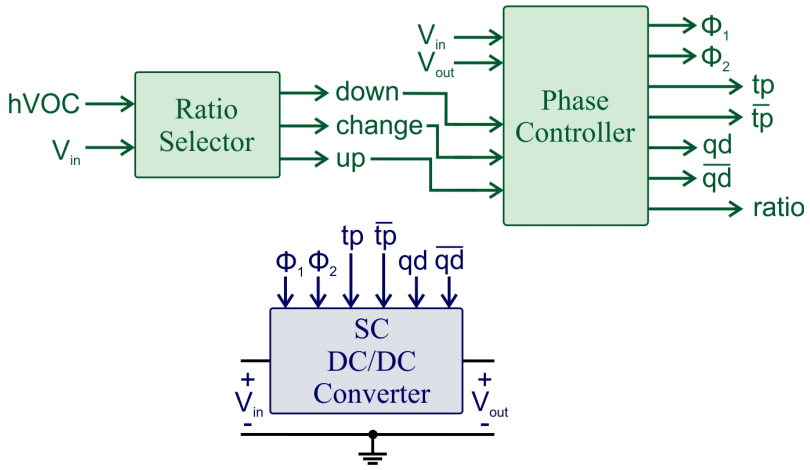


Figure 6.3: The Ratio Selector and Phase Controller blocks.

The Ratio Selector and Phase Controller blocks, depicted on Figure 6.3, comprise the portion of the control system that implement the output maximisation algorithm. They are explained together as their operation is strictly correlated.

The Ratio Selector block – refer to Appendix I – has two inputs. The input voltage of the converter, V_{in}, and the $hVOC$ signal from the V_{OC} Sampler. It then implements an adaptation of the Fractional V_{OC} MPPT scheme. Starting by default at the ratio $n = 2$ it then compares the input voltage with two thresholds, $K_{MIN}V_{OC}$ and $K_{MAX}V_{OC}$. If $V_{in} > K_{MAX}V_{OC}$ the ratio increases by 1. If, on the other hand, $V_{in} < K_{MIN}V_{OC}$, the ratio decreases by 1. This allows the maximisation of the output power – as analysed in Section 5.1 – as the behaviour of the input voltage will dynamically lead the ratio to the value which best adapts the load impedance with the source internal impedance. This block then outputs three three signals, up, $down$ and $change$. The first two consist on a pulse that goes high for a parametrised period of time, whenever the ratio is increased or decreased, respectively. The latter is a pulse that goes high when there is as ratio change. After a ration change is issued, the block becomes inactive for a parametrisable amount of time, to avoid oscillation when the voltage is kept at a voltage near the threshold that triggers the topology change.

The Phase Controller block – refer to Appendix J.2 – controls the switches of the DC/DC converter, thus performing two tasks. First, it generates the signals Φ_1 and Φ_2, which control the switching phase. In regard to this task, it implements an adaptation of the ASM on [73], as explained in Subsection 5.2.2 and detailed on Appendix J.1. It is fed by the input and output voltages of the converter, V_{in} and V_{out}, respectively, and, if $V_{in} > V_{out}/n$, the signal Φ_1, initially in a high state, goes low, for a short pulse, while Φ_2 goes high. The flying capacitor(s) is(are) then put in series, with the source and the load, conveying the charge to the output. When Φ_1 and Φ_2 return to the original state, the flying capacitor(s) is(are) once more in parallel with the source. There is an inactivity period of these switching signals, to ensure a minimum period of switching, i.e. a maximum frequency, after which, a new comparison of V_{in} with nV_{out}. As in a normal operation, V_{in} would only be (at most) equal to V_{out}/n the the efficiency was 100 %, the system will keep switching and shuttling the charge to the output. However, if there is a power shortage on the source, this condition will no longer hold and the Phase Controller will suspend the switching process, isolating the output from the system, which provides a safety mechanism to prevent the load from discharging to the source. This process makes use of the signals up, $down$ and $change$, as the comparison requires the knowledge of the ratio to be made. The $change$ signal acts as a enabling system for the Phase Controller block, to trigger the change of the ratio within the latter.

The other task performed be the Phase Controller block is also related with the control of the switches. This block also controls the configuration of the DC/DC converter. Depending on the ratio n, this block outputs the signals tp, qd and their negated forms $\overline{tp}$ and $\overline{qd}$, which open or close specific switches of the converter, effectively changing its topology into the doubler, tripler or quadrupler configurations, according to Table 6.1 – on Subsection 6.1.3 the reconfiguration process will be further detailed.

The illegal state $tp, qd = 0, 1$ is ensured not to occur as it is not necessary.

This block has one remaining output signal, $ratio$, which is only used in simulation environment to get a visual recognition of the current conversion ratio.

Table 6.1: DC/DC configuration states according to the signals tp and qd.

Topology	tp	qd
doubler	0	0
tripler	1	0
quadrupler	1	1

6.1.3 Conversion Block - The Reconfigurable SC DC/DC Parallel-Series Converter

The energy conditioning stage is a reconfigurable SC DC/DC parallel-series converter. As a proof of concept in this work, three ratios were implemented. Ultimately, the number of ratios depends on the load and source impedance relation, which ideally should be $R_L = n^2 R_{MPP}$, with R_{MPP} as the characteristic resistance of the PV cell at MPP.

The reconfigurability of the converter is provided by the switches drove by the signals tp, qd and their negated counterparts. According to the state of these switches, the parallel-series has one, two or three functional stages, operating as voltage doubler, tripler or quadrupler, respectively – refer to Figure 6.4. One should notice that these switches are controlled independently of those that ensure the switching process, Φ_1 and Φ_2. Both the switching signals and the signals that alter the topology are provided by the Phase Controller block.

Regarding the reconfigurability mechanism, Figure 6.5 portrays how the parallel-series stages may be functionally enabled or disabled, thus changing the number of operational flying capacitors.

When the stage is disabled, i.e. when the switches denoted by $\overline{fly}$ are closed, the stage adopts the topology illustrated on Figure 6.5c. In this state, the flying capacitor is short circuited to the ground in either both Φ_1 and Φ_2 phases, by the switches depicted in blue. Additionally this stage is bypassed by the connection illustrated in red.

On the other hand, if the stage is enabled – Figure 6.5b, its is subject to the switching process, being charged in parallel during Φ_1 and discharged in series during Φ_2.

6.2 Multi Ratio Energy Harvester Performance

In this section, the operation of the system will be presented. The performance of the system will be analysed, when subject to variations of the load and the source. First, on Subsection 6.2.1, this analysis will be made considering only variations of the load. Afterwards, on Subsection 6.2.2, the system will be subject to source variations. this section aims to evaluate the performance of the system when operating in variable conditions, as it is expected from a photovoltaic energy harvesting system.

6.2.1 Load Variation

The system was simulated in Spectre, using as source, the PV cell behavioural model described in Section 3.4 and Appendix E, with the characteristic illustrated on Figure 5.1. The remaining

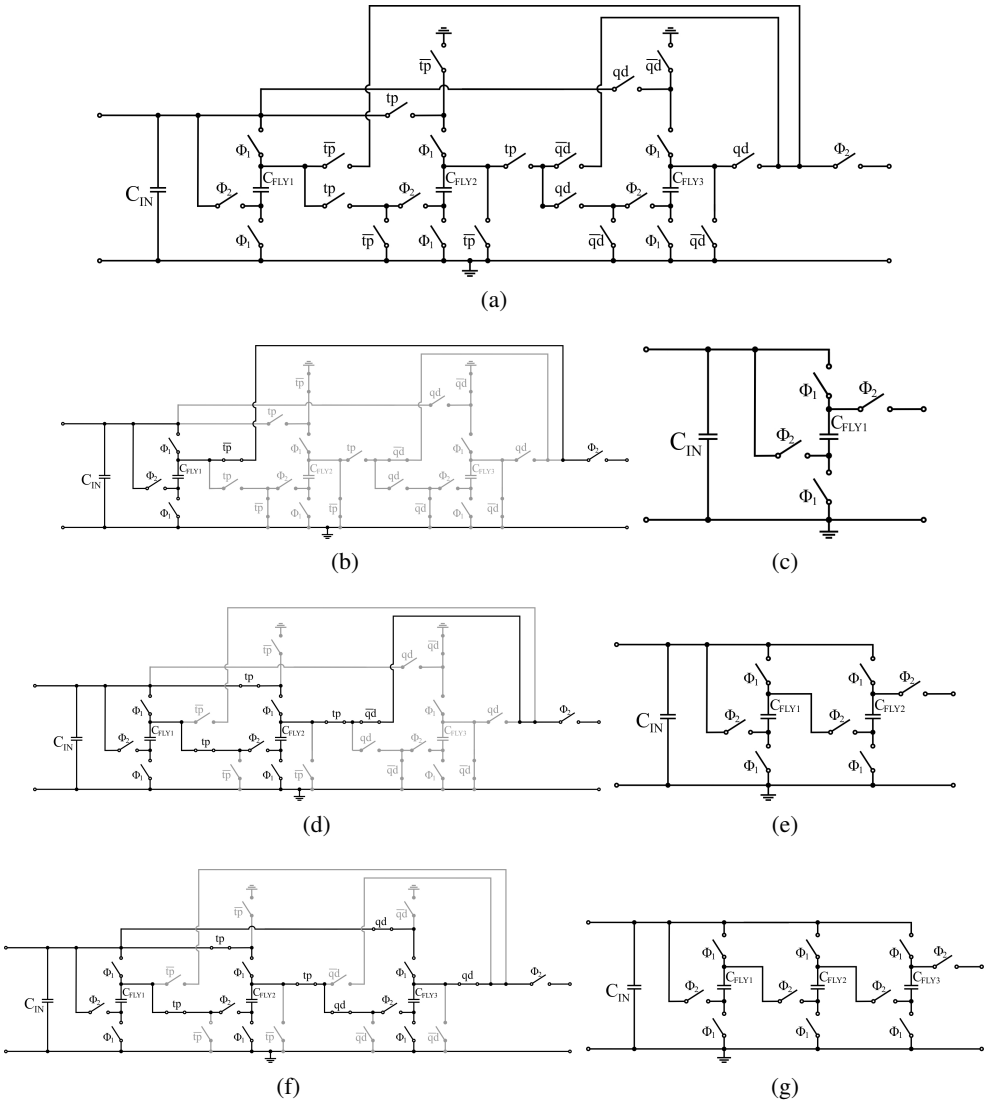


Figure 6.4: Reconfigurable SC DC/DC parallel-series converter. (a) Multi ratio parallel-series; (b) Doubler configuration; (c) Doubler simplified equivalent circuit; (d) Tripler configuration; (e) Tripler simplified equivalent circuit; (f) Quadrupler configuration; (g) Quadrupler simplified equivalent circuit.

circuit parameters are $C_{IN} = 100\,\text{nF}$, $C_{FLY} = 1\,\text{nF}$ and $C_{OUT} = 100\,\text{nF}$. The switching pulses Φ_1 and Φ_2 have a width of $1\,\mu\text{s}$ and a duty cycle of 49.5 %, thus ensuring a switching frequency of 500 kHz, with a non-overlap time of 1 % of the switching period. The algorithm implemented by the control block aims to change the ratio of the converter in order to keep the input voltage V_in within the interval $[K_{MIN}V_{OC}, K_{MAX}V_{OC}[= [0.63V_{OC}, 0.85V_{OC}[$. This interval was chosen, after inspection of the PV cell characteristic in Figure 5.1, because it allows the input voltage to vary within a range that keeps the power conveyed to the load equal or higher than 90 % of its maximum value. The V_{OC} Sampler senses the V_{OC} at a rate of 1 kHz. The insensibility time of the Ratio Selector, after a topology change is set at 0.5 ms.

The results depicted in Figure 6.6 depict the performance of the multi ratio energy harvesting system when subject to the load variations portrayed in Figure 6.6f. This simulation simultane-

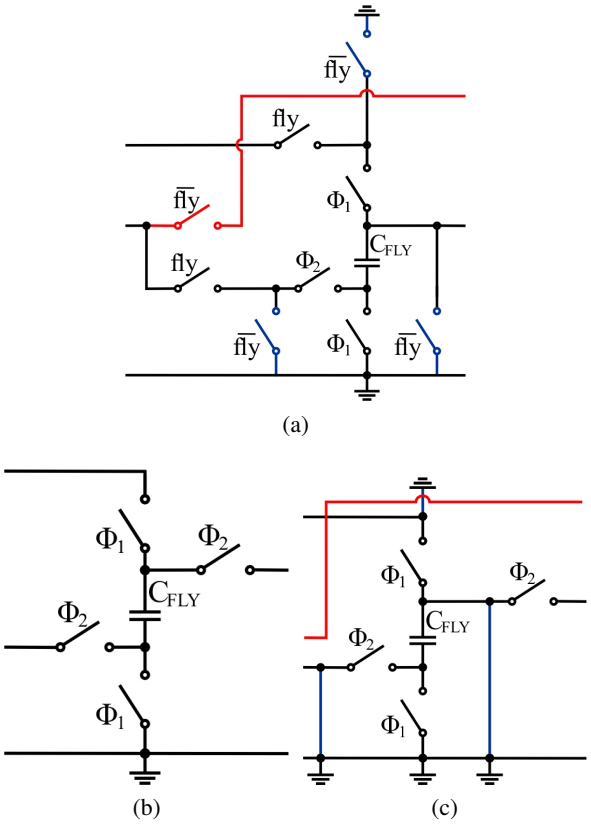


Figure 6.5: Reconfigurable SC DC/DC parallel-series stage. (a) Reconfigurable stage scheme; (b) Enabled stage; (c) Disabled stage.

ously subjected parallel-series voltage doubler, tripler, and quadrupler converters to the same stimulus. These were also connected to PV cell models equal to the one used as source for the multi ratio system. The conventional parallel-series converters were switched at $f_{sw} = 500\,\text{kHz}$. The subscripts, db, tp and qd identify the voltage doubler, tripler and quadrupler converters, whereas the signals with no such subscript denote multi ratio system. This notation will henceforth be used.

From figure 6.6a, one may observe that the input voltage of the multi ratio system – the solid red line – is kept within $0.63V_{OC}$ and $0.85V_{OC}$. This is ensured by topology changes that alter the conversion ratio, as depicted in Figure 6.6e. As a result, the input voltage is either multiplied by 2, 3 or 4, according to the instantaneous ratio of the converter, as seen in Figure 6.6b. The key aspect to retain is that the multi ratio system changes its topology in order to maximise the power delivered to the load – Figure 6.6c. It adopts the topology that best adapts the load resistance to the source internal resistance. One should keep in mind that this happens when $R_L/n^2 = R_{MPP}$. This results in the higher value of amassed energy for the system with a variable ratio, when compared to the single ratio systems, as illustrated in Figure 6.6d.

6.2.2 Source Variation

When the system is subject to a variation of the source parameters, as it is expected for a photovoltaic energy harvesting system, the ideal relation $R_L/n^2 = R_{MPP}$ is still applicable. However,

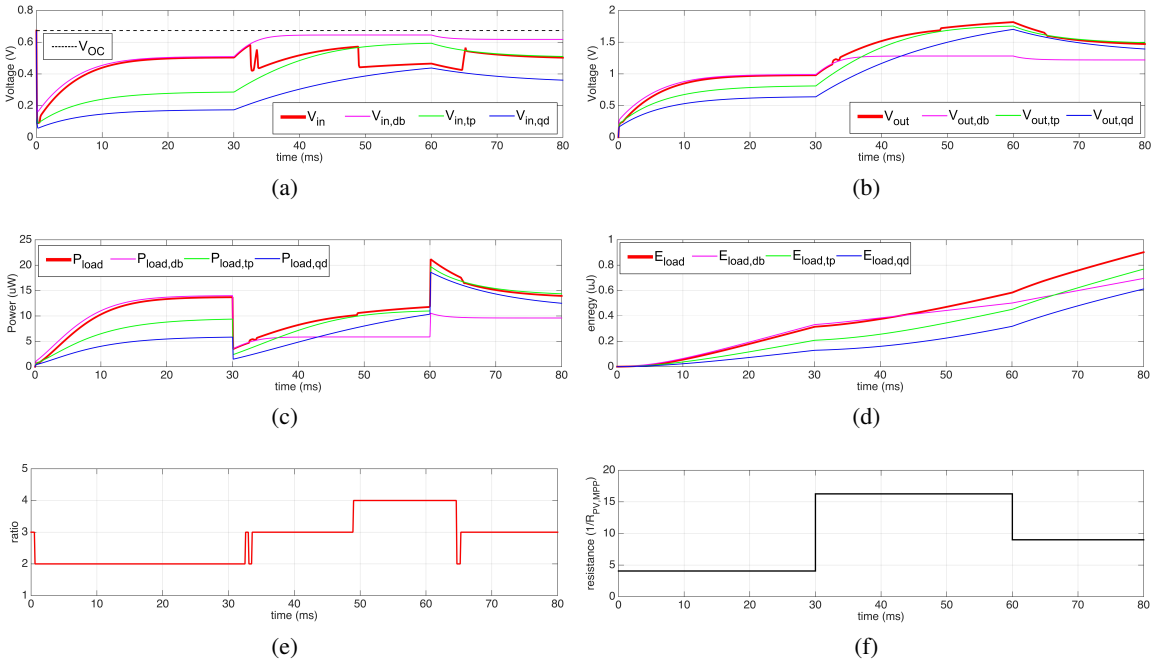


Figure 6.6: Multi ratio energy harvester performance with load variation. (a) Input voltage; (b) Output voltage; (c) Load power; (d) Accumulated load energy; (e) Conversion ratio; (f) Load resistance, normalised by the MPP PV cell resistance.

in this case, it is the value of R_{MPP} that varies, as a direct result of the change of the (V_{MPP}, I_{MPP}) coordinates of the PV cell. The system underwent a simulation in which the source parameters were varied such that the source assumed three different characteristics – Figure 6.7g. These manifested, respectively, during the intervals $[0\,\text{ms}, 30\,\text{ms}[$, $[30\,\text{ms}, 60\,\text{ms}[$ and $[60\,\text{ms}, 80\,\text{ms}[$ and were generated making use of the behavioural model on Appendix E. In order to illustrate the multi ratio operation, these PV cells were chosen as they have distinct R_{MPP} – Figure 6.7f –, which would make more evident the performance differences between each ratio topology. The chosen fractional V_{OC} range was $[0.63V_{OC}, 0.85V_{OC}[$ and the remaining circuit parameters are $C_{IN} = 100\,\text{nF}$, $C_{FLY} = 1\,\text{nF}$, $C_{OUT} = 100\,\text{nF}$ and the switching pulses Φ_1 and Φ_2 have a width of $1\,\mu\text{s}$ and a duty cycle of $49.5\,\%$. The load was set at $R_L = 145\,\text{k}\Omega$, a value that, taking into account the ideal relation $R_L/n^2 = R_{MPP}$ and the fact that the source characteristic resistance at the MPP was varied in simulation, would lead to different ratios performing best at different times, thus enriching the results of this analysis.

Once more, the multi ratio system was compared with single ratio converters, with equal source, load and electrical parameters and being switched at $f_{sw} = 500\,\text{kHz}$.

One may observe from Figure 6.7c that, for each PV cell characteristic there is a conversion ratio that provides the best results – i.e. higher power delivered to the load. Considering only the single ratio converters, it is clear from Figure 6.7c that, for the first PV characteristic, until roughly 7 ms, the voltage doubler delivers the highest amount of power to the load, being surpassed by the voltage tripler that kept the best performance until 30 ms. The voltage doubler performed the best

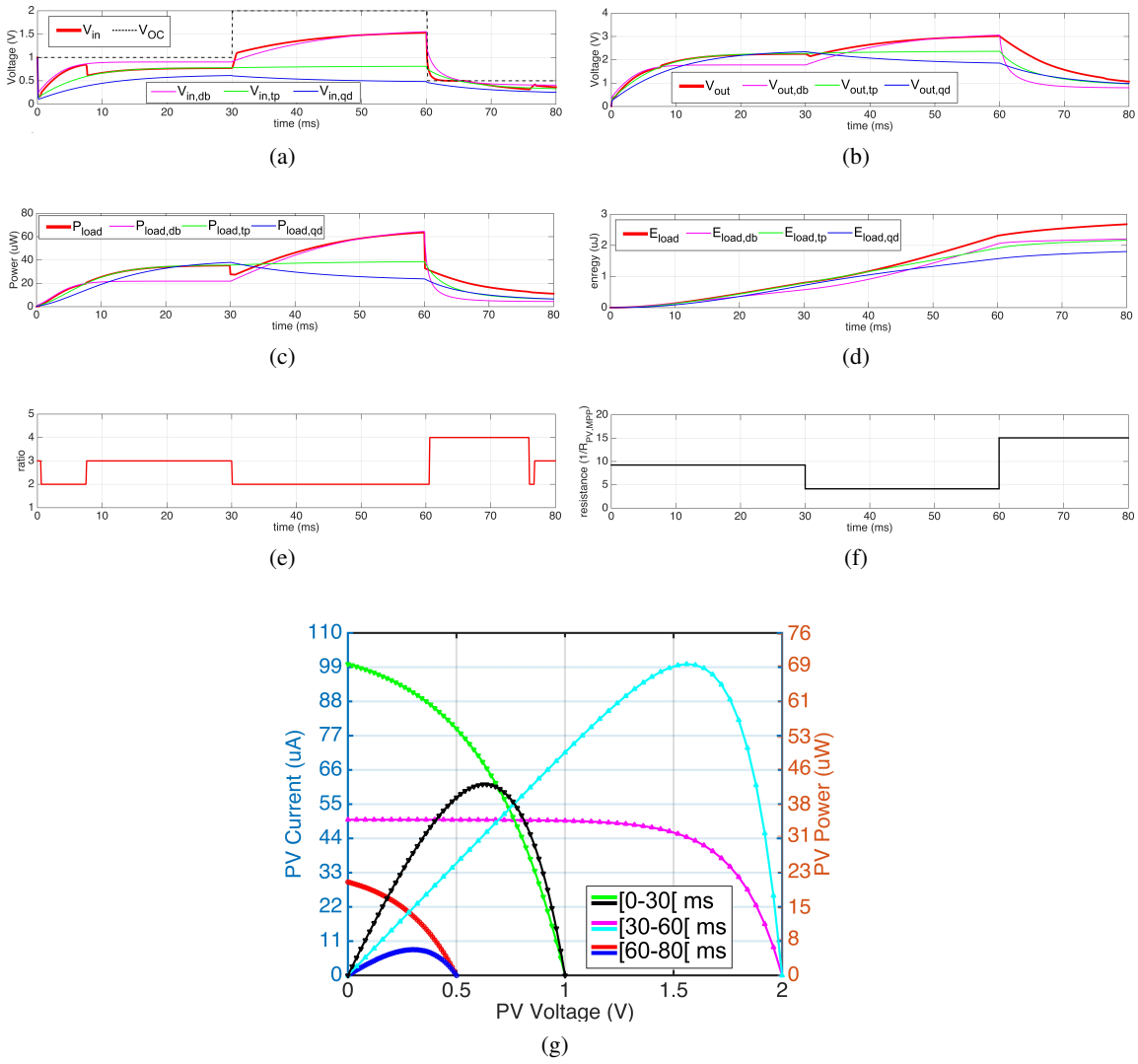


Figure 6.7: Multi ratio energy harvester performance with variation of the energy source. (a) Input voltage; (b) Output voltage; (c) Load power; (d) Accumulated load energy; (e) Conversion ratio; (f) Load resistance, normalised by the MPP PV cell resistance at the MPP; (g) Energy source characteristics, for the simulation.

for the second characteristic and, from 60 ms to 80 ms – the third PV characteristic –, the voltage quadrupler conveyed the higher amount of power.

On Figure 6.7e, the ratio of the reconfigurable converter is depicted. It changes along with the source parameters variation, adopting the ratio that performs best at a given instant. One may observe that it begins as a voltage doubler, at around 7 ms it changes to a voltage tripler, returning to the doubler configuration at 30 ms. Finally it adopts the quadrupler configuration at 60 ms and lowers the ratio to 3 at roughly 76 ms. On Figures 6.7a and 6.7b, the input and output voltage are depicted and it is visible that they follow the ratio changes. As a result of morphing the topology in order to best adapt the load resistance to the the source internal resistance and adopt the best topology at a given moment, the multi ratio approach is able to gather the higher amount of energy, as seen in Figure 6.7d.

The load has been modelled so far as a simple resistor. Being a passive component it does not impose a current on the output of the converter. Another approach would be a load that draws a constant current from the system. If the system is not able to provide that current then it is not able to support such a load. Moreover, different ratio step up converters are able to provide different amounts of current. As a converter steps up the voltage, it steps down the current by the same ratio. So it stands to reason that, lower ratio converters are able to withstand more demanding loads, current wise. In other perspective, when the energy is low, the smaller ratio converters perform better than their higher ratio counterparts.

To verify this hypothesis, the system was compared against single ratio converters. The electric parameters are the same as in the previous simulation. However, the load was modelled as a voltage controlled resistor, that provides a resistance of $1/I_L$ times the output voltage, effectively mimicking a constant current drawing load. For this study the load current was set at $I_L = 5\,\mu$A. Moreover the source PV cell was parametrised in order to imitate the energy profile of a typical indoor environment. The operation characteristics of the IXYS SLMD121H04L on the 23rd of May, 2015, were chosen. Figure 6.8g depicts the behaviour of the PV cell V_{OC}, which rises from zero when the light is turned on, remains roughly constant during the working hours of the day, and falls to zero once more at the end of the day. The red marker are the PV cell characteristics sampled from that day, resulting in the curves on Figure 6.8h. Once more these were generated making use of the behavioural model on Appendix E.

When the energy supply is low, on the first instances of simulation, one may observe on Figures 6.8a and 6.8b that only the voltage doubler is able to keep the output (and input) voltage above 0. This means that only the voltage doubler would be able to withstand such a load. When the simulation advances, the ratio that best performs under these conditions becomes the voltage quadrupler. In fact, amongst the single ratio converters, it is the voltage quadrupler that gathers the highest amount of energy, as depicted in Figure 6.8d. Taking into consideration the multi ratio approach, one may observe that it changes the ratio of conversion, adopting the topology that performs best at a given instance. It begins as a voltage doubler and eventually becomes a voltage quadrupler. As a result, it amasses the highest amount of energy – Figure 6.8d and, on a real situation, would be able to hold the operation when the supply current is low, by adopting a lower ratio topology, and later change into a more profitable ratio, when the supply increases. Figure 6.8f depicts the load resistance, which, being dependent of the output voltage – $R_L = V_{out}/I_L$ –, presents a variable behaviour.

Due to the reconfigurability of the multi ratio approach, it is able to withstand a wider range of source and load variations, by adopting the topology which best reacts to a given context. Drawing from the advantages of distinct topologies, it is capable of harvesting the highest amount of energy, when compared to its single ratio counter parts. On the next section, its performance under indoor lighting conditions, which are the scope of this work, will be analysed.

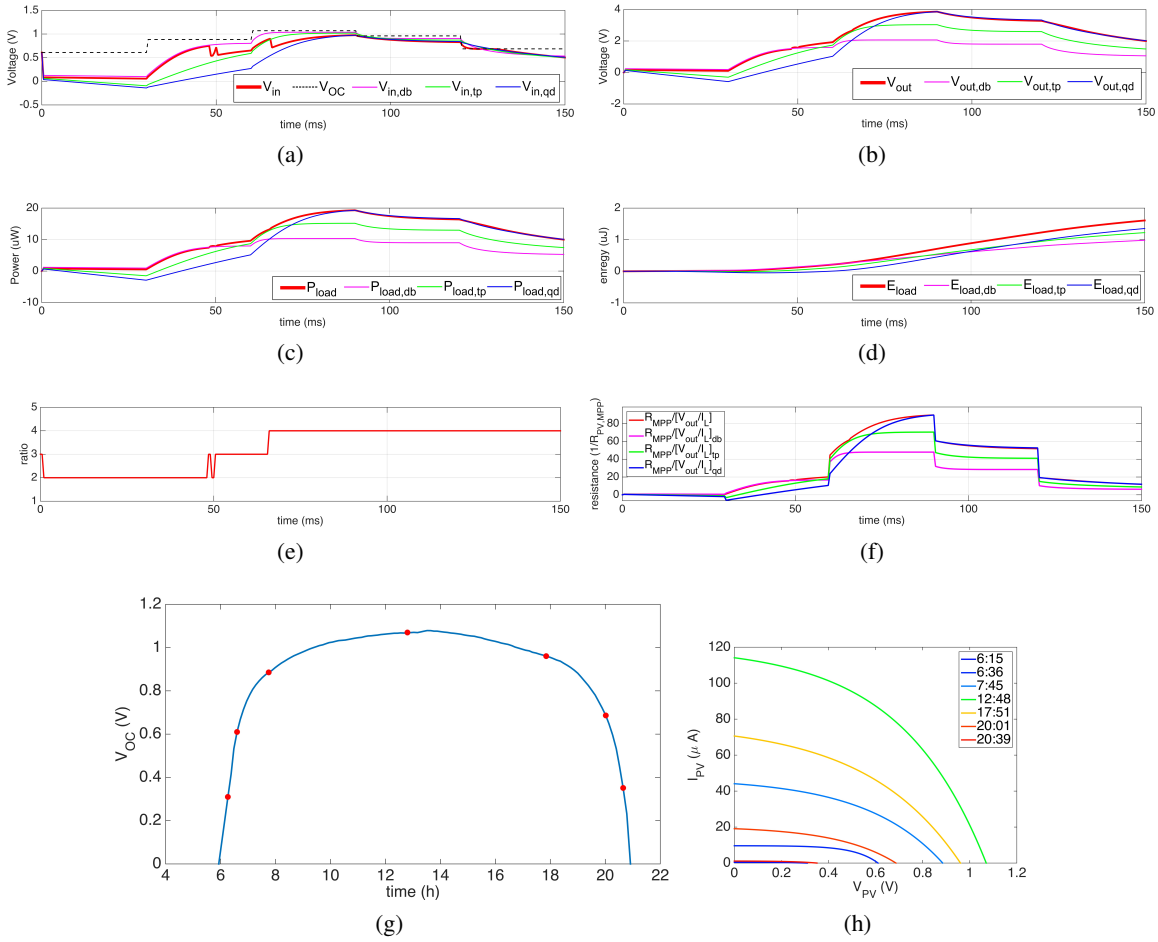


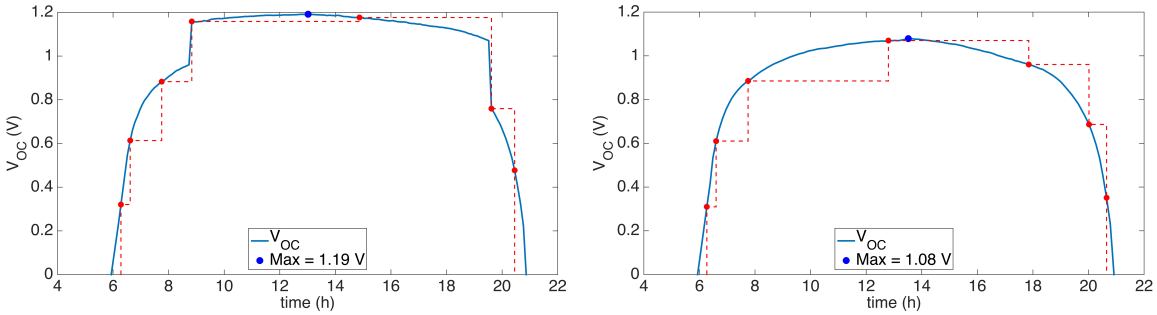
Figure 6.8: Multi ratio energy harvester indoor performance with a constant current drawing load. (a) Input voltage; (b) Output voltage; (c) Load power; (d) Accumulated load energy; (e) Conversion ratio; (f) Load resistance V_{out}/I_L, normalised by the MPP PV cell resistance at MPP; (g) $V_{OC}(t)$ for the IXYS SLMD121H04L on the 23rd of May, 2015; (h) Sampled *I-V* characteristics.

6.3 Multi Ratio Energy Harvester Indoor Operation

The system operation was analysed, simulating the weather conditions of a sunny day with clear sky and a cloudy day, 22nd of May and 23rd of May, respectively. Using the same approach as in Subsection 6.2.2, the PV behaviour during the day was sampled, providing a rough estimate of its evolution during the day, as depicted in Figure 6.9.

On Figure 6.9, the dashed red line illustrates the V_{OC} behaviour with time, when considering the sampled profile for this analysis. This approach was used to study the behaviour of the multi ratio approach because it would be quite unpractical and very computationally costly to perform a transient analysis on 24 hours worth of data. The idea is to analyse the behaviour of the system at specific time instances and extrapolate for the remainder of the day. The red markers on Figures 6.9a and 6.9b signal the sampled instances of the PV cell behaviour, which in turn yielded the *I-V* curves on Figure 6.10.

The behaviour model on Appendix E was used to create a piece wise linear variation of the PV

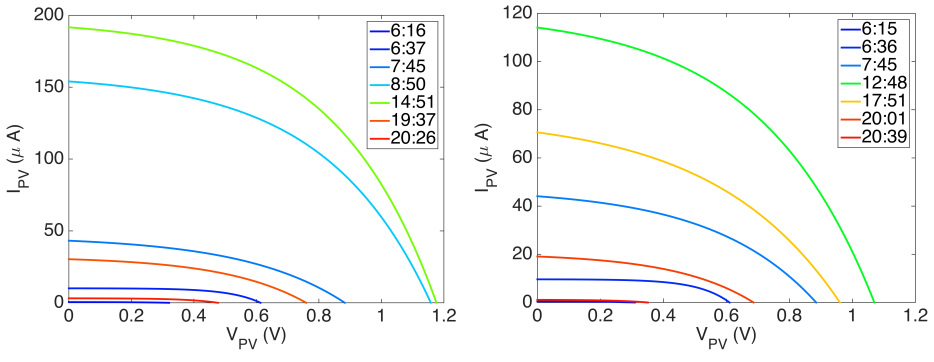


(a) (b)

Figure 6.9: Indoor PV cell behaviour used in simulation. The sampled profile corresponds to the IXYS SLMD121H04L. (a) $V_{OC}(t)$ on 22nd of May, 2015; (b) $V_{OC}(t)$ on 23rd of May.

cell characteristics, thus generating the different PV cell operation points. The load was modelled with a voltage controlled resistor, with a resistance of $1/I_L$ times the output voltage, being I_L a simulation variable. The chosen fractional V_{OC} range was $[0.63V_{OC}, 0.85V_{OC}[$ and the remaining circuit parameters are $C_{IN} = 100\,\text{nF}$, $C_{FLY} = 1\,\text{nF}$, $C_{OUT} = 100\,\text{nF}$. The switching pulses Φ_1 and Φ_2 have a width of 1 μs and a duty cycle of 49.5 %.

Taking into account that the load is effectively drawing 1 μA, one may observe from the results on Figure 6.11 that, for the PV cell characteristics that provide the lowest amounts of energy – the first and the last samples of each day – the PV cell supply is not enough thus the input and output voltage are 0, for the first sample of each day and are visibly decaying for the last ones –Figures 6.11a and 6.11f. Additionally, the ratio remains at 2, according to Figures 6.11e and 6.11j. As the load is drawn a current of 1 μA, it means that the PV cell must be able to provide at least $I_{PV} = nI_L$. Indeed, if one observes these curves carefully – Figure 6.12 – it becomes clear that neither case is able to provide $nI_L = n \times 1\,\mu\text{A}$, even with $n = 2$. However, from the remaining *I-V* curves one Figure 6.9, there is enough energy to allow the system to operate. There is even a surplus of energy, which leads the voltage to rise and eventual so does the ratio.



(a) (b)

Figure 6.10: PV cell *I-V* curves used in simulation. The sampled profile corresponds to the IXYS SLMD121H04L. (a) Sampled *I-V* on 22nd of May, 2015; (b) Sampled *I-V* on 23rd of May, 2015.

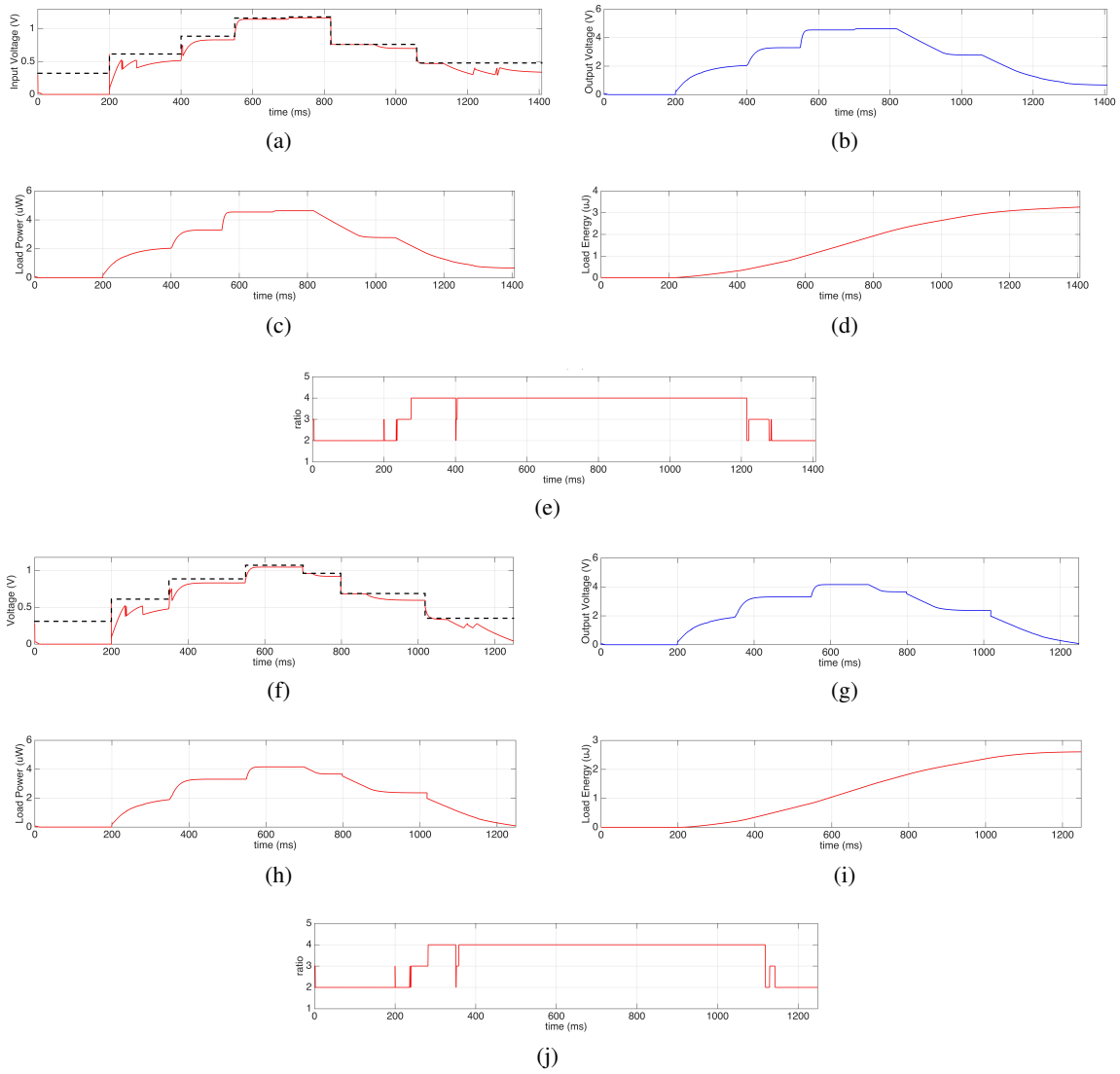


Figure 6.11: Multi ratio energy harvester indoor performance with a constant current drawing load using as source the enrgy profile of the IXYS SLMD121H04L model on the 22nd – (a) to (e) – and 23rd – (f) to (j) – of May, 2015. (a) Input voltage and V_{OC} (black dashed line); (b) Output voltage; (c) Load power; (d) Accumulated load energy; (e) Conversion ratio; (f) Input voltage and V_{OC} (black dashed line); (g) Output voltage; (h) Load power; (i) Accumulated load energy; (j) Conversion ratio.

The system eventually reaches ratio $n = 4$ – Figures 6.11e and 6.11j. In these conditions, the input current stabilises at nI_L, biasing the PV cell to the voltage that corresponds to that current, on its characteristic curve. The output voltage, in turn, is kept at 4 times the input voltage. The accumulated energy during the simulation is depicted on Figures 6.11d and 6.11i however, if one extrapolates the results of the simulation to the time interval of the sampled operation points, thus defining the PV cell behaviour illustrated by the red dashed lines on Figures 6.9a and 6.9b, the accumulated energy would follow the curves on Figure 6.13.

There are several conclusions to be drawn from these results. Firstly, there is no significative different in the gathered amount of energy for a sunny day and a cloudy one, when considering

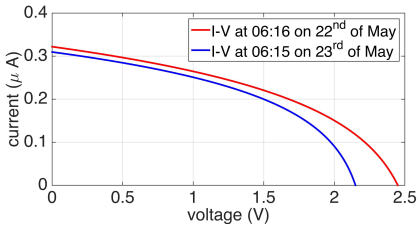


Figure 6.12: Lowest energy *I-V* curves on the 22nd and 23rd of May.

indoor lighting environments. This is due to the fact that the artificial and indirect lighting is dominant in this context. Secondly, if one considers the load as a constant current drawing device, the amount of energy that can be gathered is directly dependent on the current that the load device draws from the system, because it biases the current of the PV cell into nI_L, thus forcing the PV cell into a specific operation point.

The single ratio converters were also subject to the same analysis and time extrapolation. Their accumulated energy is also depicted in Figure 6.13 for the time considered. One may observe that the multi ratio approach yields the best results of the four alternatives. However, the amount of energy amassed by quadrupler is quite comparable to that which the proposed system gathered. This is explained with the fact that during the most of the time, the multi ratio system is operating as a quadrupler. Its advantage emerges during periods of low energy supply in which it adopts a more profitable topology.

Taking into account that the storage device is a capacitor, the stored energy is given by $(1/2) \times CV^2$. This means that it is desirable to keep the voltage as high as possible. This happens if the current drawn by the load is arbitrarily small, which in turn leads to a small amount of current being drawn from the PV cell, thus biasing it into a voltage close to it V_{OC}, the highest amount of voltage it can provide. On the limit, for a load drawing no current, the PV cell would rise to V_{OC} and the energy on the storage capacitor would then be $(1/2) \times C(nV_{OC})^2$. So it stands to reason that the highest amount of instantaneous energy on a day at the storage capacitor is given by the PV cell V_{OC} on its characteristic curve with the highest V_{OC}:

$$E_{C,MAX} = \frac{1}{2} \times C(nV_{OC,MAX})^2 \tag{6.1}$$

In the considered considered cases, with the highest V_{OC} values of 1.19 V and 1.08 V for the 22nd and 23rd of May, 2015, respectively, and the storage capacitor at 100 nF, the highest instantaneous energy would be, respectively 1.1329 μJ and 0.933 12 μJ. One must bare in mind, however, that for the output to rise to nV_{OC}, the current of the PV cell drops to zero, which means no current can be drawn by the load. (6.1) provides, however, a theoretical upper bound for the energy stored in the capacitor.

Hypothetically, a load being supplied only by $E_{C,MAX}$, would have to draw less than 13.112 pW and 10.800 pW, respectively for the 22nd and 23rd of May, to hold 24h without the need to make

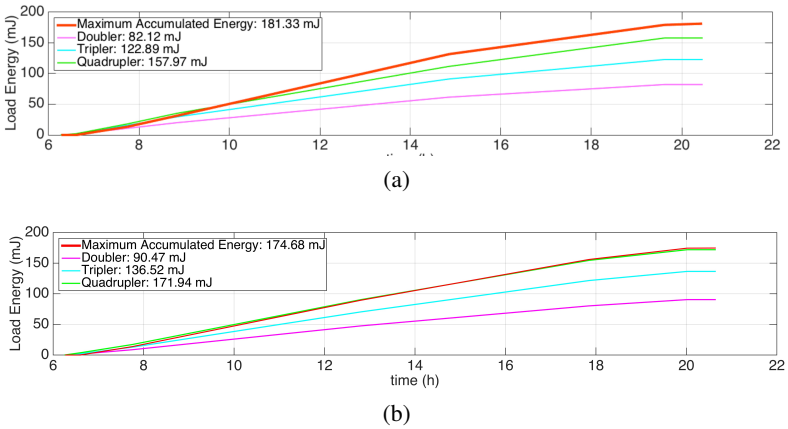


Figure 6.13: Extrapolated energy accumulation for the energy profile defined by the sampled PV cell behaviour. Comparison of energy accumulated by the proposed approach (red line) withe the single ratio topologies. (a) Energy accumulation on the 22nd of May, 2015; (b) Energy accumulation on the 23rd of May, 2015.

use of the energy harvester. If there is the need to support higher power consumption or longer operation time, the necessity to use a capacitor much larger than 100 nF may arise. Moreover, as the capacitor charge is depleted, the voltage at its terminals lowers, which further constrains the load. The use of a supercapacitor, would rise these values several orders of magnitude as there are commercially available products that typically range from a few milli Farad to several hundreds of milli Farad – Section 2.3.

There is, however, an important aspect to consider. Although this work as approached the storage capacitor as an ideal capacitor, which may be charged to an arbitrary voltage, a physical device would have a rated voltage it would withstand before suffering damage. This voltage depends on the technology used but the fact is that, even though there a supply that allows the voltage to achieve an arbitrarily high voltage, one must bare in mind that doing so may result in structural damage of the storage component. Ideally, one should cap the voltage at the rated voltage for the storage capacitor. Next section presents an optimisation of the power maximisation algorithm that takes into account this restriction.

6.4 Constrained Power Maximisation

An optimisation of the previously presented algorithm was developed to meet the restriction of the rated voltage of a storage device, i.e. the maximum voltage it can withstand without damage.

It consists on a small alteration of the multi ratio ASM controller to limit the voltage at a given reference. It functions as the previously used ASM, however, if the output voltage rises above a reference voltage, it suspends the switching. This causes the output voltage to fall bellow the reference. When the output voltage is lower than the rated voltage of the storage device, the switching is resumed. Ultimately, this limits the output voltage to that reference, as it is not allowed to rise above that value – refer to Appendix J.3

Despite this work recurrently advocating the disadvantages of manipulating the frequency due to the losses in the conversion that my ensue, this particular case justifies this procedure. The surplus of power, which is being dissipated in the conversion process due to the down scaling of the frequency, would only result in damage to the storage component. Moreover, reducing the frequency may lead to less power requirement by the system.

The optimised phase controller is thus fed with an addition signal, the voltage reference. It falls out of the scope of this work how this reference is achieved. For this proof of concept let us assume that it is provided to the phase controller.

To verify the operation of this optimisation, the multi ratio system was configured with $C_{IN} = 100\,\text{nF}$, $C_{FLY} = 1\,\text{nF}$, R_{ON}. The input voltage is kept within $[0.63V_{OC}, 0.85V_{OC}[$ the maximum frequency of the system is 500 kHz. The energy source is a PV cell, modelled with the behavioural module on Appendix E, with the characteristic depicted in Figure 6.14a. Finally, the load was modelled as a resistor R_L. The value of R_L varied in simulation – refer to Figure 6.14b – in order to vary the output voltage, to demonstrate the operation of the optimised algorithm.

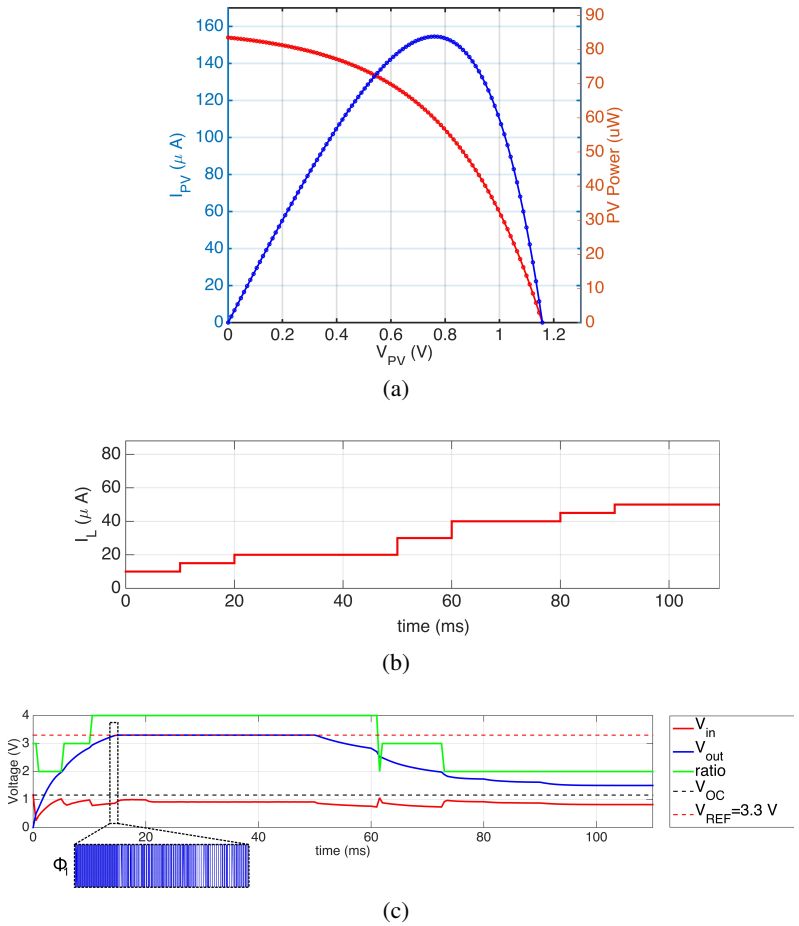


Figure 6.14: Constrained power maximisation. (a) PV cell characteristic used as energy source; (b) Varying load current; (d) Variation of the input and output voltages and the conversion ratio.

One may observe from Figure 6.14c that the output voltage is constrained not to rise above the

reference voltage. In this specific case, the voltage limit was set at 3.3 V merely as an illustrative example. The switching signal Φ_1 is also illustrated, to demonstrate the variation of the switching regime. One may observe that the pulses of Φ_1 occur less frequently in time, when the output voltage rises to the reference voltage of 3.3 V.

If one analyses the energy accumulation with the same PV energy profile as in Section 6.3, however, taking into account this optimisation it stands to reason that it will be lower, because the output voltage is not allowed to rise as much as it could. Figure 6.15, illustrates that, for both days considered in the previous analysis, with this safety measure, the accumulated energy is indeed lower.

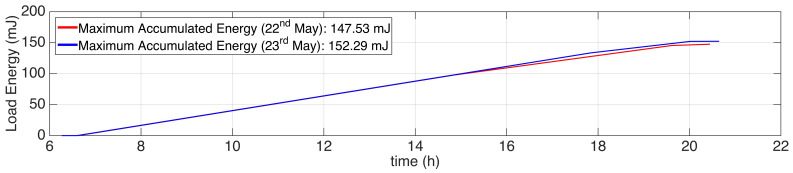


Figure 6.15: Energy accumulation with constrained power maximisation, on the 22nd and 23rd of May.

Nevertheless, this is a necessary measure to safeguard the structural integrity of the storage device. One should notice, however, that the input voltage is limited by the choice of the PV cells for this work. Neither model used for analysis has a V_{OC} greater than the 3.3 V used for reference, otherwise a limiting mechanism would need to be used to constrain the input voltage as well.

6.5 Reconfiguration for Unitary and Step Down Conversion

Only step up voltage conversion has been considered until this point. However, the load power scheme advocated so far is based on the relation $R_L = n^2 R_{MPP}$, which means that, if $R_L \leq R_{MPP}$, the only way to keep the load resistance adapted to the internal resistance of the source, is to make use of conversion topologies that allow voltage conversion ratios equal or inferior to 1.

To achieve a unitary conversion ratio, one must only alter the way some switches in the circuit are controlled.

Figure 6.16 depicts the alteration of the circuit in order to allow reconfiguration into unitary and step down VCR.

For the first case, when the switches driven by the signal *sh* are closed, the switches sw_1 and sw_2 are opened, and sw_3 becomes driven by the signal Φ_1. The topology becomes structurally equivalent to the circuit in Figure 6.16b, and the converter operates as a sample and hold circuit. When Φ_1 is high, the load capacitor is charged to V_{in} and, during Φ_2, it holds the charge.

To achieve step down conversion, i.e. VCR<1, one need only to invert the terminals of the converter. If the terminals of a converter with a VCR of α are inverted, it becomes a converter with a VCR of $1/\alpha$. Therefore, if the presented converter has a set of conversion ratios of $\times 2$, $\times 3$ and $\times 4$, by inverting its terminals, the previous set becomes $\times(1/2)$, $\times(1/3)$ and $\times(1/4)$.

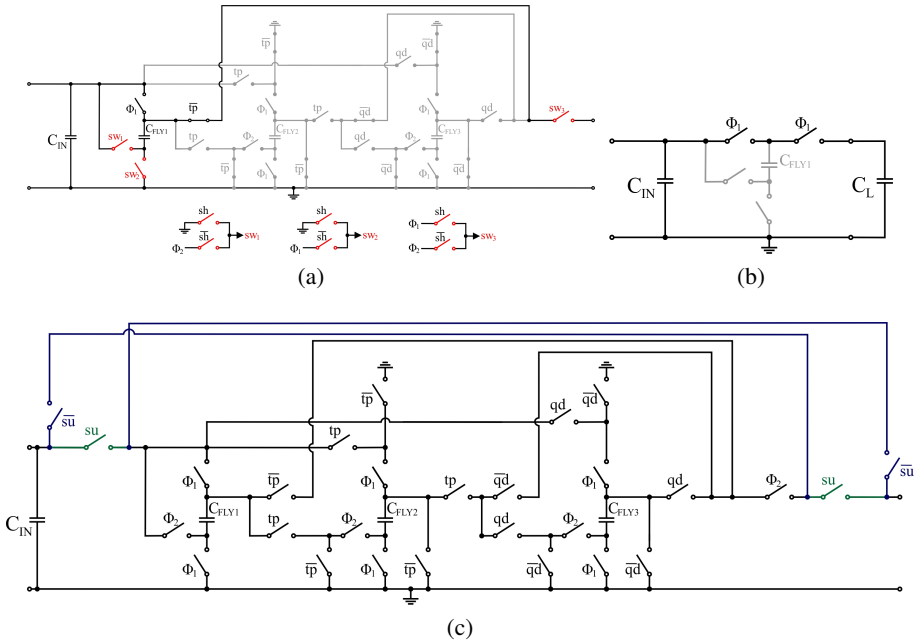


Figure 6.16: Topology of the converter for a VCR equal or inferior to 1. (a) Illustration of the rewired switches and correspondent signals; (b) Equivalent circuit when the topology is set for VCR=1; (c) Structure to allow step down conversion ratios.

Figure 6.16c depicts the adaptation of the circuit that accomplishes the reconfiguration into a step down converter.

The added structures – depicted in blue and green – allow the rewiring of the input and output of the converter and inversion of these terminals. If the signal *su* is high, the converter operates with the step up and unitary set of ratios. If the previous signal is low (and its negated form high), the input and output of the converter are exchanged, and the latter operates as a step down converter, reusing the flying capacitors to achieve this.

Figure 6.17 depicts a demonstration of the adaptations described in this section. The parameters used are: $C_{IN} = 100\,\text{nF}$, $C_{FLY} = 1\,\text{nF}$ and R_{ON}. The input voltage is kept within $[0.63V_{OC}$ $0.85V_{OC}[$ and the maximum frequency of the system is 500 kHz. The energy source is a PV cell, modelled with the behavioural module on Appendix E, with the characteristic depicted in Figure 6.17a. Finally, the load was modelled as a resistor R_L and varied according to Figure 6.17c. The phase controller verilog-A implementation may be found in Appendix J.4.

One may observe that, when the load resistance is lower that the source internal resistance – Figure 6.17c – the converter reconfigures int a step down topology. When $R_L = R_{MPP}$, the converter becomes a unitary VCR converter, whereas for the remaining time of simulation, with $R_L > R_{MPP}$, it becomes a step up converter. The algorithm still strives to keep the load adapted to the source, by reconfiguring the topology. However, by including the step down and unitary conversion ratios, it is now able to perform that impedance matching process in a wider range. It is now able to better withstand loads with low resistance or, equivalently, loads that demand higher current amounts from the system.

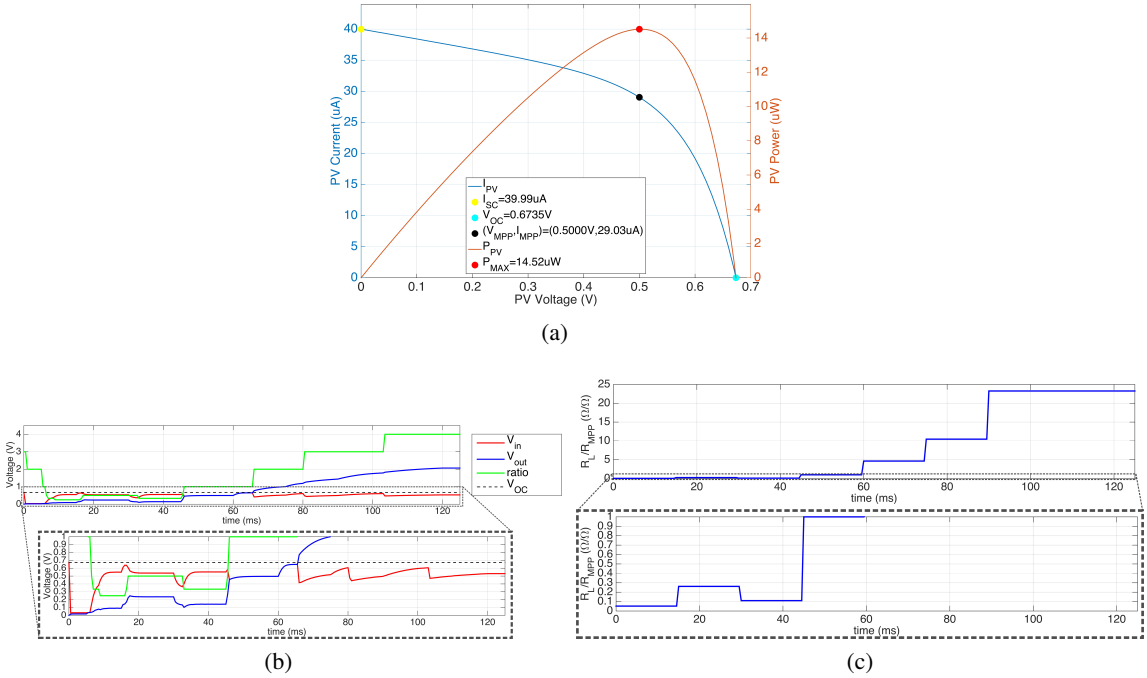


Figure 6.17: Operation of the converter with the unitary and step down reconfigurations available. (a) Characteristic of the PV cell used as source; (b) Voltage behaviour and ratio changes; (c) Varying load resistance used for stimulus.

If one subjects the system to the PV characteristics depicted in Figures 6.9 and 6.10 and extrapolates the energy accumulation as previously performed in Sections 6.3 and 6.4, the result depicted in Figure 6.18 are obtained.

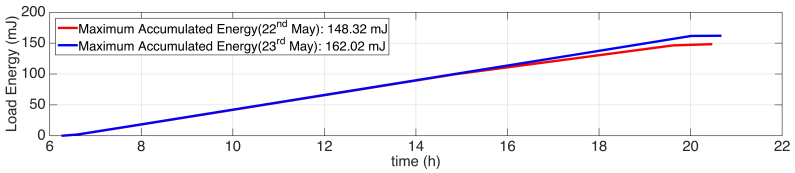
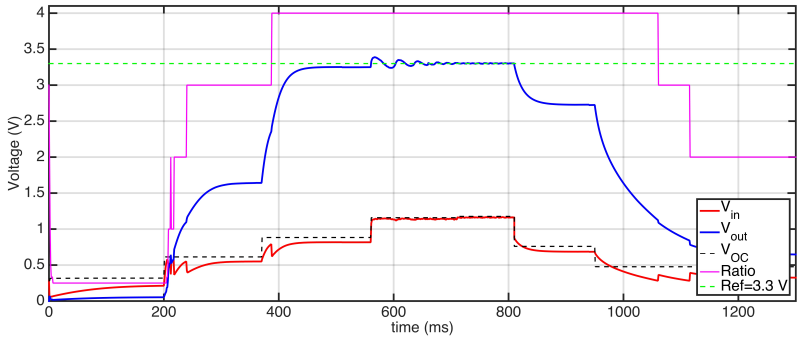
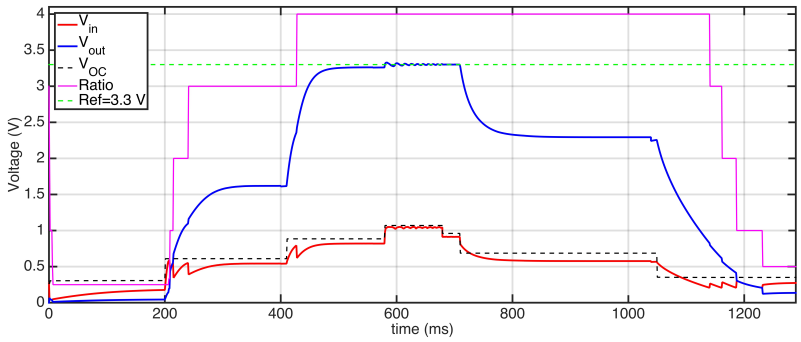


Figure 6.18: Energy accumulation with constrained power maximisation and voltage unitary and step down reconfigurability, on the 22nd and 23rd of May.

One may observe that, although the accumulated energy is lower than the one illustrated in Figure 6.13, due to the load power constraint developed in the previous section, it is still able to harvest more energy than the system without voltage unitary and step down reconfigurability. Indeed, by adopting a topology with a voltage conversion equal or inferior to 1, the system is able to adapt the load resistance to the source internal resistance, within a wider range. If one observes Figure 6.11, it is clear that, when the source provides the lowest levels of energy, at the beginning of the day for example, the system with solely voltage step up topologies reconfigurability is not able to harvest energy. However, when capable of adopting unitary and voltage step down topologies, the system can cope with a wider range of source and load characteristics and, in this case, it is able to harvest energy when the previous system could not, as illustrated in Figure 6.17.



(a)



(b)

Figure 6.19: Operation of the converter with the unitary and step down reconfigurations available, under indoor light conditions. (a) Operation when subject to the PV characteristics on the 22nd of May and on the (b) 23rd of May.

A scheme of the architecture of the system with the enhancements presented in Sections 6.4 and 6.5 can be seen on Figure 6.20.

6.6 Conclusions to This Chapter

In this chapter, a multi ratio approach to an energy harvester based on indoor PV energy was presented. The functional blocks of the controller, implemented in Verilog-A were presented an explained, followed by the topology and operation of the reconfigurable SC DC/DC parallel-series converter.

The algorithm implemented by the controller aims to maximise the power delivered to the load, by exploiting the geometrical characteristics of the *I-V* curves of the PV cell and their correlation with the power extracted from the PV cell. Specifically, monitoring the input voltage and changing the topology of the converter in order to keep it within a range $[K_{MIN}V_{OC}, K_{MAX}V_{OC}[$ allows the power delivered to the load to be maximal.

Moreover, using a reconfigurable converter allows the adaptability a single ratio converter would not be able to provide. When there is low energy available, a lower ratio provides more feasible results: when compared to a higher ratio converter. Considering a load that draws an arbitrary current i^*, than a converter of ratio n would have to draw from the PV cell $n \times i^*$. To deliver the same amount of energy to the load, the first draws less current from the PV cell than

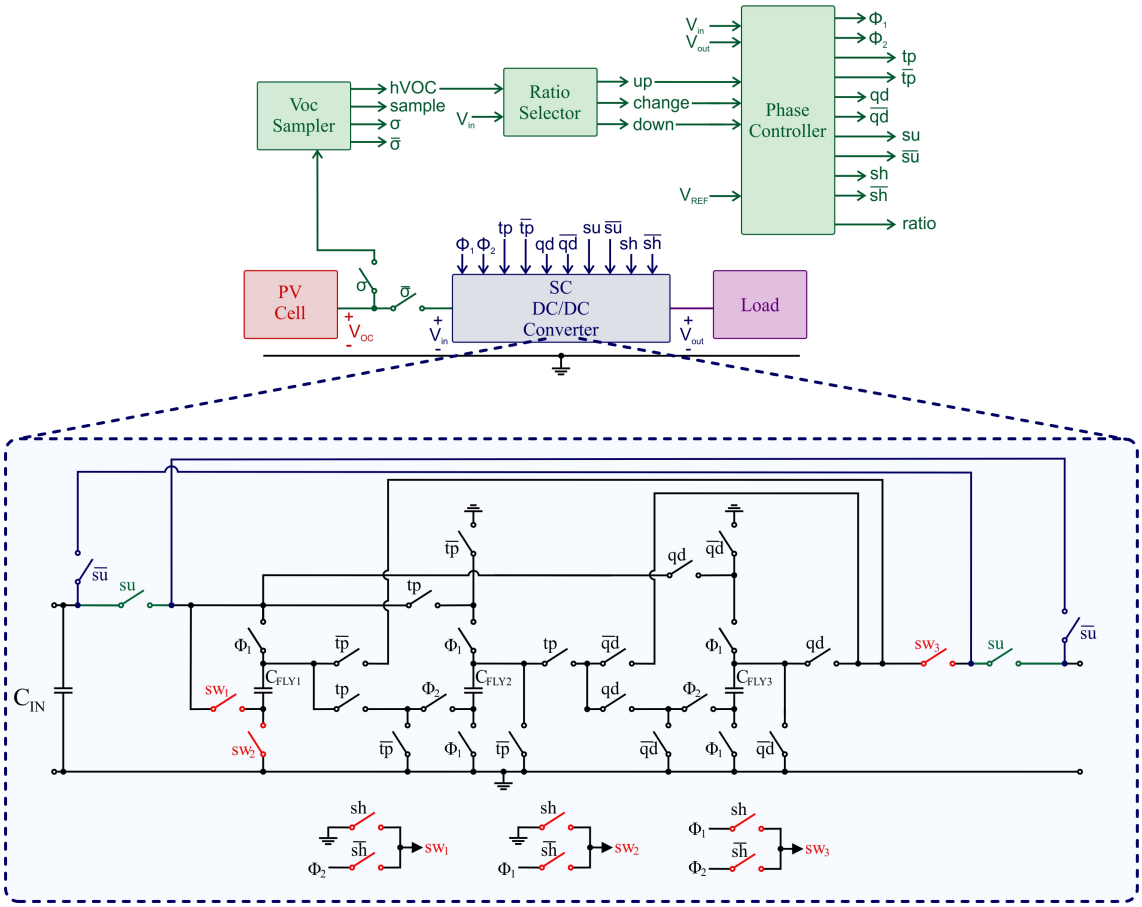


Figure 6.20: Enhanced system architecture.

the latter. However, when there is a surplus of energy available, the reconfiguration of the topology of the converter into a higher ratio allows the system to supply the load at a higher voltage, thus increasing the energy in the storage capacitor.

Another perspective is that a reconfigurable system is able to adapt the load resistance to the PV internal resistance along a wider range, as the optimal relation between these is given by $R_L = n^2 R_{MPP}$.

As a result, under varying conditions a reconfigurable solution is able to gather the highest amount of energy, when compared to its single ratio counterparts, as it adopts the topology that delivers the highest amount of power to the load, at a given time.

Another conclusion that arises from this chapter is a reinforcement of an idea defended on Chapter 3, which is the fact that indoor environments dim the differences between sunny and cloudy days in terms of light energy availability. This happens because the dominant energy source is the artificial lighting, which presents a dramatic difference from what is to be expected in outdoor environments.

Finally, the amount of energy extracted by the system is directly dependent on the demands imposed by the load. However, given the fact that the energy in the storage capacitor is directly

proportional to the voltage drop at its terminals – according to $(1/2) \times CV^2$ – it is possible to define a theoretical upper bound for the energy stored in the load capacitor. The upper limit is given by the highest voltage a PV cell can provide during that day, when the reconfigurable system is operating at its highest ratio, as stated in (6.1).

Considering this upper bound, calculated for two different days, in the data gathered in Chapter 3, yielded that, for a load to hold more than 24h under the conditions, on 22nd and 23rd of May, 2015 (which were two distinct days in terms of weather conditions), without using the energy harvester, it would have to draw less than 13.112 pW and 10.800 pW of power, respectively. This hints about the necessity to use a capacitor much larger than 100 nF.

A supercapacitor, ranging from a few milli Farad to several hundreds of milli Farad, would possibly solve this problem.

This chapter discussed also an optimisation of the phase control algorithm that dynamically suspends and resumes the switching, in order to limit the output voltage to a reference value. This optimisation derives from the fact that physical storage devices have rated voltages they can withstand without damage. In these circumstances, the voltage at their terminals should not be allowed to rise above that value.

In order to consider a more realistic approach, the load power maximisation scheme was altered, to take into account a hypothetical voltage limit a storage device could withstand without structural damage. For this study a 3.3 V limit to the output voltage was considered. Under these circumstance, the accumulated energy lowered, when compared to the one harvested without voltage constraints.

A final improvement of the system was developed in Section 6.5 that allowed the system to adopt topologies for unitary and step down voltage conversion. For the first, the converter operates as a sample and hold, being the load capacitor the device that holds the charge. For the latter, the step down conversion, the input and output terminals are inverted, thus reusing the voltage doubler, tripler and quadrupler configurations to obtain $\times(1/2)$, $\times(1/3)$ and $\times(1/4)$ voltage conversion ratios, respectively. This enhancement allows the system to cope with a wider range of source and load characteristics and still match the load to the source. By adopting these topologies, the system is able to harvest energy when the previous system could not – when the PV cell provides low amounts of energy as at the beginning of the day.

Chapter 7

Final Remarks and Future Perspectives

7.1 Summary and Contributions of this Work

This work performed a proof of concept of an energy harvesting system based on PV energy conversion. The latter is driven by a load power maximisation algorithm that adapts the premises of the fractional open circuit voltage maximum power point tracking scheme to a multiple voltage conversion ratio approach. Its goals are to operate efficiently under indoor lighting environments and maximise the power delivered to the load.

The main contributions of this thesis are:

- Development of a platform to bias and measure the PV cell electrical characteristics;
- Characterisation of the operation of different PV cells, indoors;
- Gathering of experimental data about the energy availability of such context;
- Study of the feasibility of a system based on indoor PV energy;
- Development of a behavioural model of the PV cell;
- Development of a mathematical model for the SC DC/DC parallel-series voltage doubler;
- Characterisation of the influence of the electrical components of the system in the overall performance;
- Study and comparison of different ratio converters, using the approach presented in [68];
- Analysis of the DC/DC converter operation when the energy source is a PV cell;
- Development of an algorithm to maximise the power delivered to the load and prevent the load from discharging to the source;
- Development of a reconfigurable parallel-series SC DC/DC converter suitable to be driven by the previously developed algorithm;

- Optimisation of the developed algorithm to constrain the output voltage by the rated voltage of the storage device;

- Enhancement of the system to allow reconfigurability into unitary and step down voltage conversion topologies.

7.2 Discussion of the Results

In Chapter 3, four PV cell models were studied under the scope of indoor operation using a test platform developed that allowed to measure their *I-V* characteristic. From this analysis, one could conclude that, in terms of light energy availability, indoor environments are characterised by a dominance of the artificial light. This dims the difference of harvestable energy between sunny days and cloudy ones. It also provides a roughly stable lighting environment, during the time these lights remain lit, which reflects of the output of the PV cell that becomes also approximately constant during that time.

Under these circumstances, the output power of the PV cells, in indoor environments, is in the μW order, which is about a thousand times lower than the output reported in the datasheets for outdoor operation. Following the electrical characterisation of the models used in the tests the parasitic capacitance of the PV cells was measured, yielding values ranging from approximately 0.1854 nF / cm^2 to 2.6130 nF / cm^2 being the capacitance of the monocrystalline silicon cell considerably lower than the reported values for the amorphous silicon models. These models, under indoor lighting conditions yield power levels roughly in the order of hundreds of microwatt to a few milliwatt. Following a sensibility analysis, 1.4 mW was obtained as a rough estimate of the power context of indoor environments. Of course, subject to the use of PV cells such as those tested.

On the same chapter a practical behaviour model of the PV cell was developed. It describes the PV cell *I-V* curve using only 3 variables – V_{OC}, I_{SC} and A, a fitting parameter and provides a practical behavioural model that may be used to mimmic the the behaviour of specific PV cell models in a simulation environment.

Chapter 4 studied the energy conditioning stage of an energy harvesting system. The parallel-series SC DC/DC converter was used in this analysis due to its performance in the SSL regime of operation, which is reported in literature to be superior to other topologies. A mathematical model for the latter was developed using nodal analysis. It was then used to gain insight on the influence of the electrical components, the switching frequency and the source-load context in its performance. From this analysis, some sensibility was acquired to size components and choose a switching frequency, in order to keep the converter operating efficiently.

Afterwards a generic model based on the output impedance of the converter was adopted, based on the work in [68]. It allowed a simplified and practical analysis of the converter operation and could also be easily used to study the operation of higher ratio converters, for which the previous mathematical analysis would prove computationally costly and less practical. Using this

approach, the total load resistance can be decomposed by the resistive value of the load device plus the output resistance of the converter, such that $R_L = R_{SSL} + R_{OUT}$, with R_{SSL} as the latter.

The power delivered to the load displays a parabolic evolution with the resistive value of that load. The load power peaks when $R_L = n^2 R_S$, which means that different ratios provide better results for distinct load resistance ranges. These ranges, in turn intersect at specific resistive load values which define the optimal load value at which the conversion ratio should be changed, in order to maintain the power delivered to the load maximised. These points correlate with the behaviour of the input voltage that increases monotonically with the load resistance. The behaviour of the input voltage may then be used to determine when the conversion ratio must change, keeping in mind the goal to maximise the power delivered to the load. There are several ways to maximise the energy extracted from the PV cell. The most widely reported in literature is the frequency modulation of the signals that drive the switches. However, this method may lead to undesirable losses in the conversion stage. This mechanism acts by manipulating the switching frequency such that when the load resistance, i.e. $R_L = R_{SSL} + R_{OUT}$ is inferior to $n^2 R_{MPP}$, one may reduce the frequency and increase the input resistance to approximate its value from $n^2 R_{MPP}$. In this situation the PV cell is biased into outputting the maximum power it can. However, decreasing the frequency to increase the input resistance is actually increasing the amount of energy dissipated in the converter, "artifially" increasing its input resistance. This means that, even though the PV cell it at the MPP, a lower amount of energy is delivered to the load because it is being lost in the conversion stage. Being at the MPP does not necessarily mean that the energy delivered to the load is as high as it can be.

Conversely, when the load resistance is superior to $n^2 R_{MPP}$, then the frequency may be increased to reduce the input resistance thus approximating R_L from R_{MPP}, as the value of R_{SSL} is inversely proportional to the switching frequency. However, if the converter is already operating at a frequency that minimises the conversion losses, such as 500 kHz, for a converter with $C_{IN} = 100\,\text{nF}$, $C_{FLY} = 1\,\text{nF}$, $R_{ON} = 1\,\Omega$ and $C_L = 100\,\text{nF}$, further increasing the frequency has no relevant effect.

Chapter5 analyses an alternative method which consists on altering the topology of the converter circuit, i.e. its conversion ratio, in order to match the load impedance with the impedance of the PV cell. This mechanism aims to maximise the output power, which is, as stated, not necessarily the same as maximising the PV cell output. This method must configure the converter to the topology that yields the best overall performance for at a given instant.

On the same chapter, an algorithm to control this multi ratio approach was also discussed. It exploits the geometric properties of the *I-V* curve of the PV cells and the monotonic behaviour of the input voltage, as indicators to when the topology must change in order to keep the power output within optimal range. There is a range in which the input voltage may vary that allows maximum power to be delivered to the load. Whenever the input voltage reaches the lowest or highest value of that range, the conversion ratio must decrease or increase, respectively, in order the maintain the load power maximised. This approach benefits from the characteristics of the PV cell as this range of input voltage can be defined by comparison with the open circuit voltage of

the PV cell.

However, this mechanism was developed taking into consideration the data gathered during the PV cell characterisation, concerning the characteristics of different PV cells. The results of this mechanism may be further enhanced if it is configured for a specific PV cell. Although the analysed modules were somewhat similar in terms of energy levels and *I-V* there are differences amongst these devices. Namely because they are built from different technologies, which lead to distinct behaviours. As such, designing a mechanism dedicate to a single PV cell model may yield better results.

Still on Chapter 5 some additional concerns when devising an energy harvesting system were approached.

A DC/DC converter is a bidirectional device. This means that there is the possibility for the energy to flow from the load to the charge. This is an undesirable effect that may occur if the PV cell suffers an energy supply drop, for example if a shadow is cast over its surface. To overcome this issue, an ASM control scheme was employed. It allows a dynamical and automatic frequency control that suspends the switching process when there is a supply energy drop.

Additionally it spares the system from additional power consumption by avoiding unnecessary switching – for example at night, when there is no energy supply, therefore, no need to keep the flying capacitors switching.

Finally, on Chapter 6, a proof of concept of the proposed approach was made. It consists on a reconfigurable parallel-series SC DC/DC converter that implements a set of three conversion ratios – $\times 2$, $\times 3$ and $\times 4$. It was validated in simulation, making use of the behavioural model of the PV cell, developed in Chapter 3, to mimic the "real" PV cell characteristic, gathered in the same chapter.

Through the tests performed on this chapter one may conclude that, under varying conditions a reconfigurable solution is able to gather the highest amount of energy, when compared to its single ratio counterparts, as it adopts the topology that delivers the highest amount of power to the load, at a given time. Another perspective is that a reconfigurable system is able to adapt the load resistance to the PV internal resistance along a wider range, as the optimal relation between these is given by $R_L = n^2 R_{MPP}$.

As a result, under varying conditions a reconfigurable solution is able to gather the highest amount of energy, when compared to its single ratio counterparts, as it adopts the topology that delivers the highest amount of power to the load, at a given time.

On the same chapter, a theoretical upper limit for the energy stored in the capacitor was additionally derived. Given by the highest voltage a PV cell can provide during that day, when the reconfigurable system is operating at its highest ratio, this upper limit can be defined as $E_{C,MAX} = \frac{1}{2} \times C(nV_{OC,MAX})^2$. Considering this upper bound, calculated for two different days, in the data gathered in Chapter 3, yielded that, for a load to hold more than 24h under the conditions, on 22nd and 23rd of May, 2015 (which were two distinct days in terms of weather conditions), without using the energy harvester, it would have to draw less than 13.112 pW and 10.800 pW

of power, respectively, for a 100 nF. A supercapacitor, ranging from a few milli Farad to several hundreds of milli Farad, would possibly solve this problem.

This chapter discussed also an optimisation of the phase control algorithm that dynamically suspends and resumes the switching, in order to limit the output voltage to a reference value. This optimisation derives from the fact that physical storage devices have rated voltages they can withstand without damage. In these circumstances, the voltage at their terminals should not be allowed to rise above that value.

In order to consider a more realistic approach, the load power maximisation scheme was altered, to take into account a hypothetical voltage limit a storage device could withstand without structural damage. For this study a 3.3 V limit to the output voltage was considered. Under these circumstance, the accumulated energy lowered, when compared to the one harvested without voltage constraints.

A final improvement of the system was developed in Section 6.5, which allowed the system to adopt topologies for unitary and step down voltage conversion. For the first, the converter operates as a sample and hold, being the load capacitor the device that holds the charge. For the latter, the step down conversion, the input and output terminals are inverted, thus reusing the voltage doubler, tripler and quadrupler configurations to obtain $\times(1/2)$, $\times(1/3)$ and $\times(1/4)$ voltage conversion ratios, respectively. This enhancement allows the system to cope with a wider range of source and load characteristics and still match the load to the source. By adopting these topologies, the system is able to harvest energy when the previous system could not – when the PV cell provides low amounts of energy as at the beginning of the day.

7.3 Future Work

The proposed solution in this thesis is a proof of concept. It regards indoor energy harvesting in indoor environments, making use of a reconfigurable energy converter driven by an algorithm that consists on an adaptation of the fractional open circuit voltage scheme to a multi ratio approach. However it makes use of functional control blocks implemented though behavioural descriptions. As such, the immediate step to follow would be to design these block with "physical" components, to analyse their true analog behaviour. Following this, use of transistors instead of ideal switches, subsequent layout design and parasitic characteristics extraction and analysis would yield a more accurate insight on the power consumption, losses and overall transient behaviour of the system.

This work exploits the parallel-series topology, based on the fact that it has the best performance when operating in SSL, according to [68]. Adding more stages to the parallel-series converter increases the ratio by one. For $n-1$ flying capacitor stages, the conversion ratio is n.

The ideal relation between the load and source resistances depends on the conversion ratio. Moreover, the load power maximisation algorithm used in this work implies that each ratio operates along a range before changing to another topology. An interesting approach would by the study of fractional ratios. Having fractional ratios would result in a greater number of configurations, which in turn would reduce the operation range of each one of these topologies. Presumably,

the deviation of the load power from its maximum value would thus be reduced as well. The analysis of other topologies would open this possibility.

The possibility to combine several instances of the energy harvester, to increase the power output is also a possibility to be taken into account. Moreover, and relating to the previous paragraph, a wider set of ratios can be achieved by using several equivalent converters.

Finally, it remains to test this system in a real situation, i.e. with a physical prototype.

As a system that exploits an energy source independent from the conventional electrical energy grid, it opens the possibility for the design of portable devices or easily deployable devices that can operate virtually indefinitely. The applicability of this technology to wireless sensor nodes is thus a logical step to follow. It gains special relevance nowadays with the increasing use of small portable devices, wearables and sensor grids. The possibility to make use of a "clean" energy source such as the light is also an appealing outcome to the use of energy harvesters.

Appendix A

PV Cell Test Platform PCB Schematic



Figure A.1: PV cell test board PCB schematic.

Appendix B

PV Cell Characterisation Results

The PV cell characterisation took place during several days, in several locations. The weather conditions during these days is illustrated in Figure B.1. Figure B.2 depicts a schematic representation of the rooms at which the PV cell characterisation tests took place. The results of these tests are depicted in Figures B.3 to B.65.

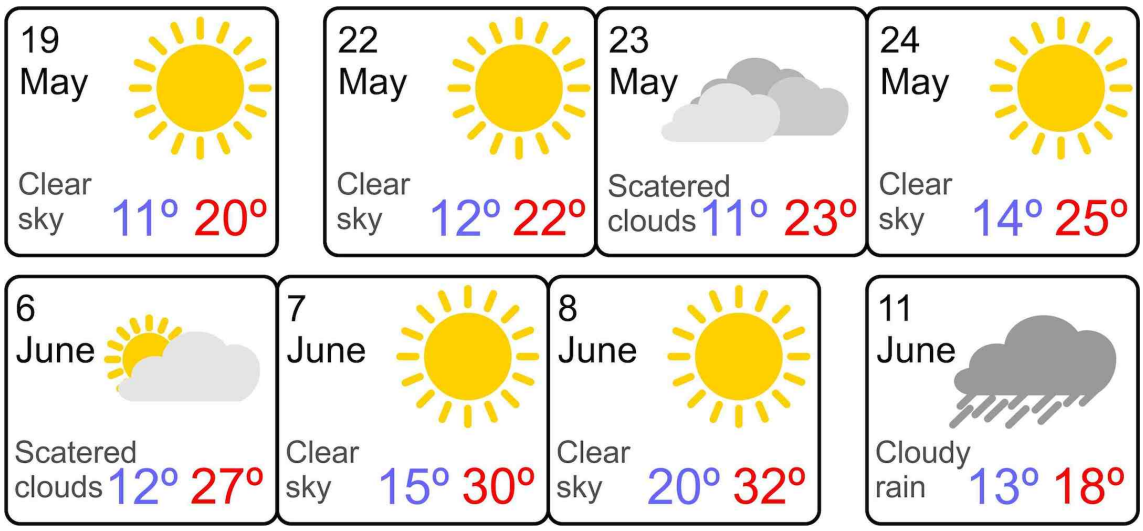
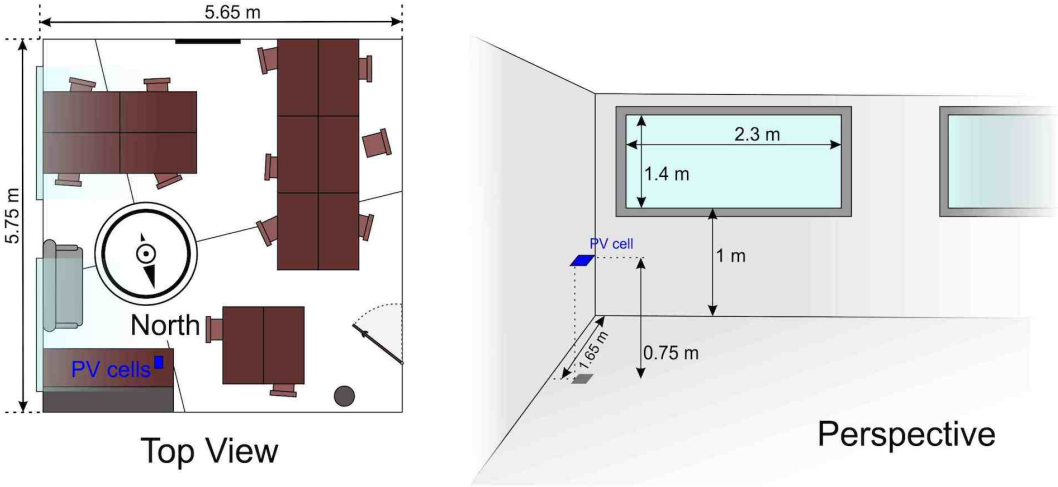
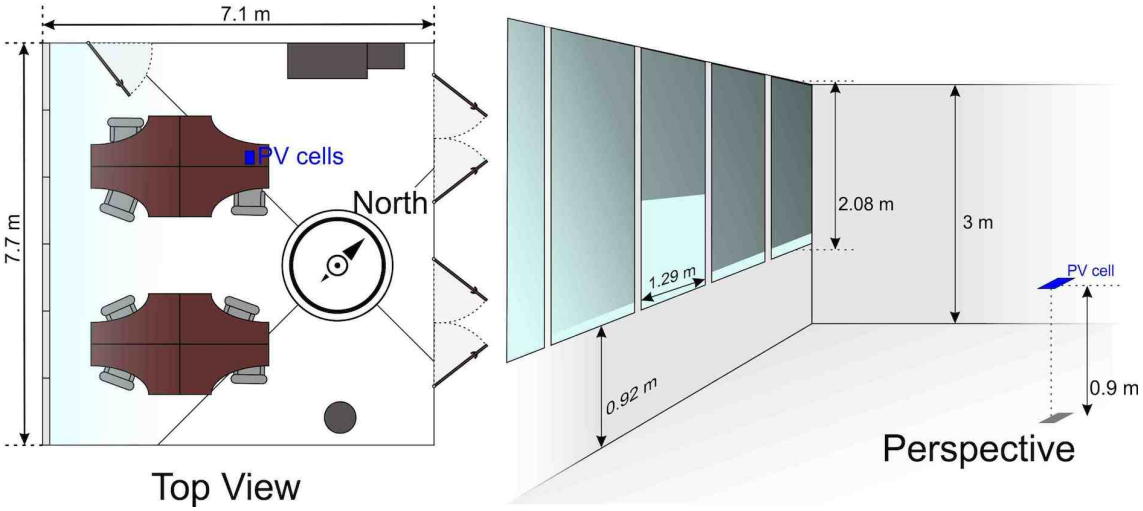


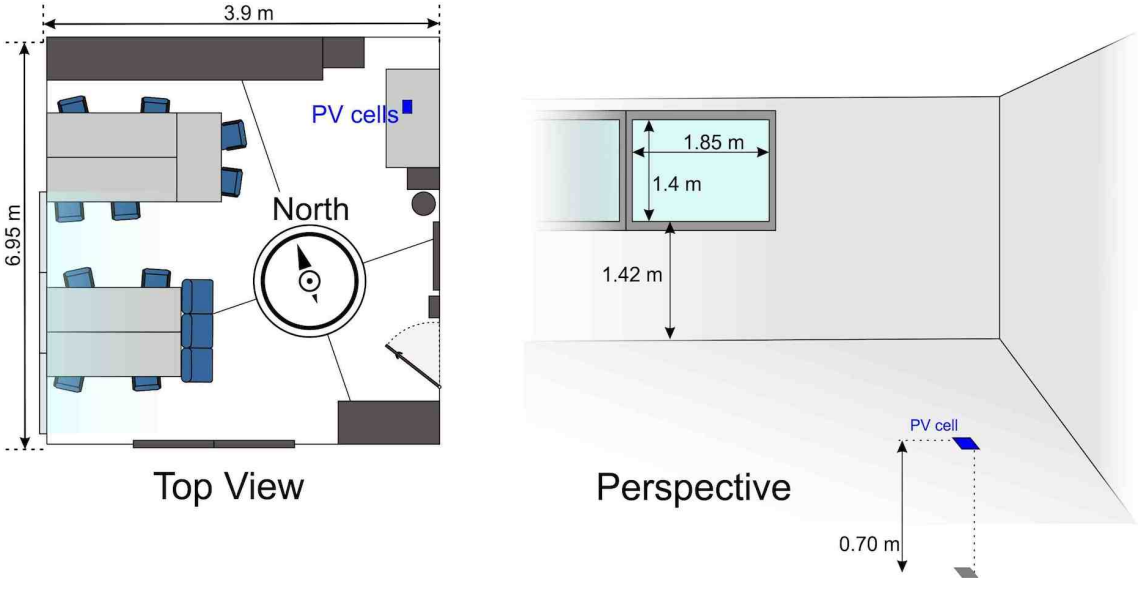
Figure B.1: Weather conditions during the days of the PV cell characterisation tests – extracted from accuweather.com. 19th location A; $22^{th} - 24^{th}$ location B; $6^{th} - 8^{th}$, 11th location C – refer to Figure 3.3c.



(a)



(b)



(c)

Figure B.2: Scheme of the places were the PV cell characterisation tests took place – (a) place A; (b) place B; (c) place C.

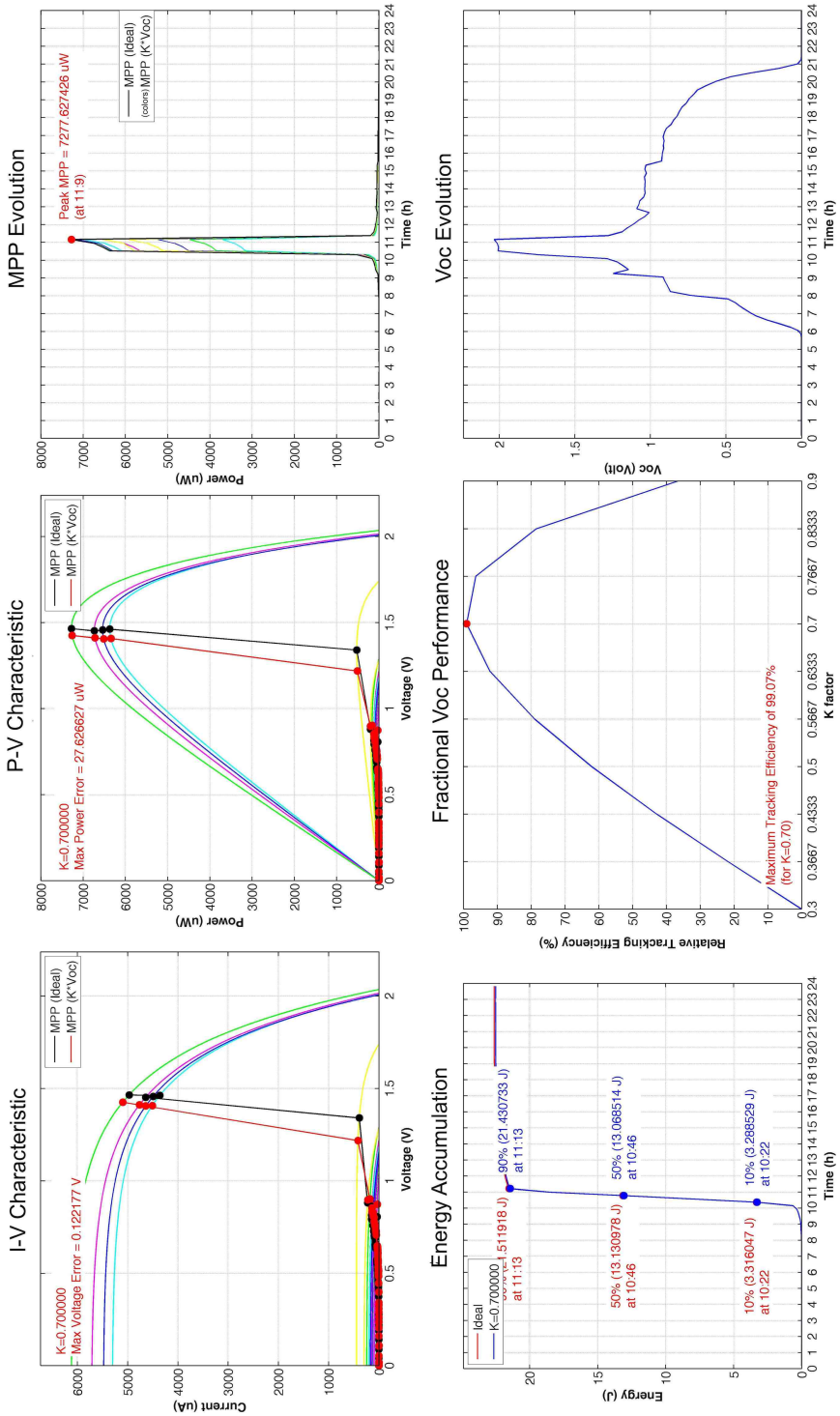
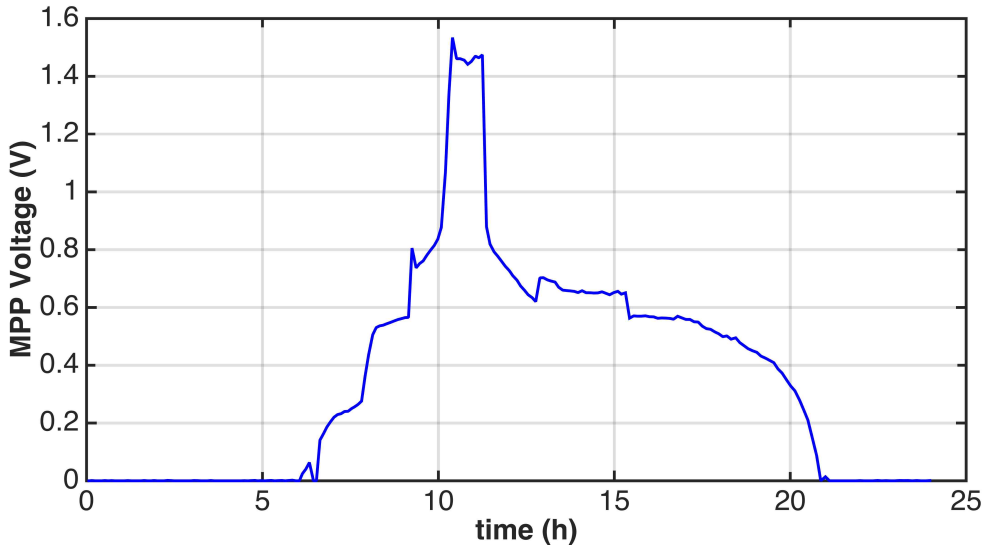
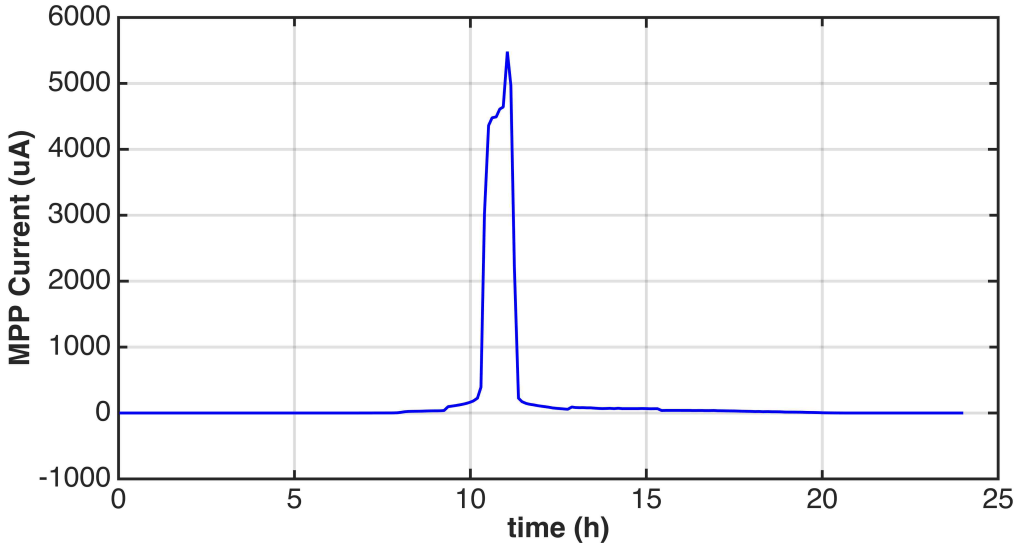


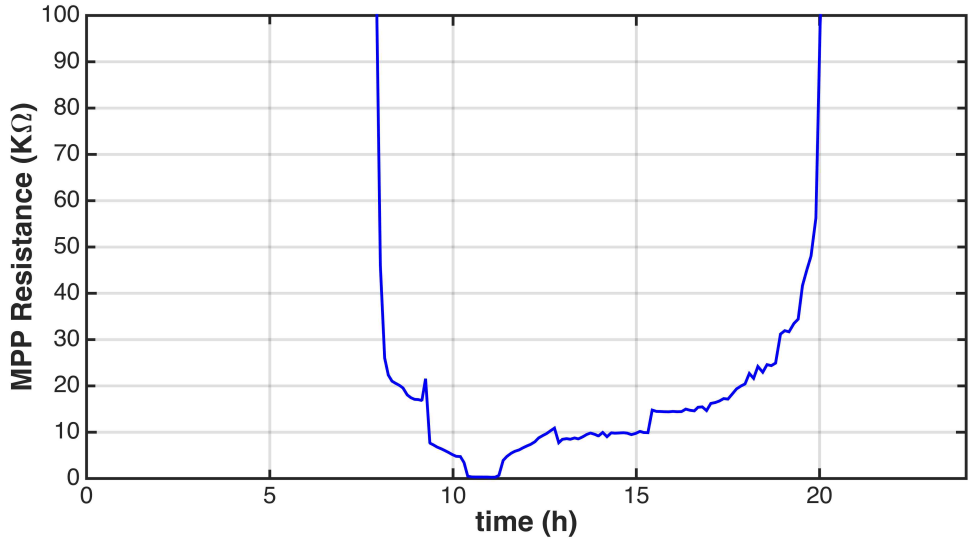
Figure B.3: PV data for the IXYS SLMD121H04L on 19th of May of 2015. Test made on location A.



(a)



(b)



(c)

Figure B.4: Maximum power point coordinates for the IXYS SLMD121H04L on 19th of May of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

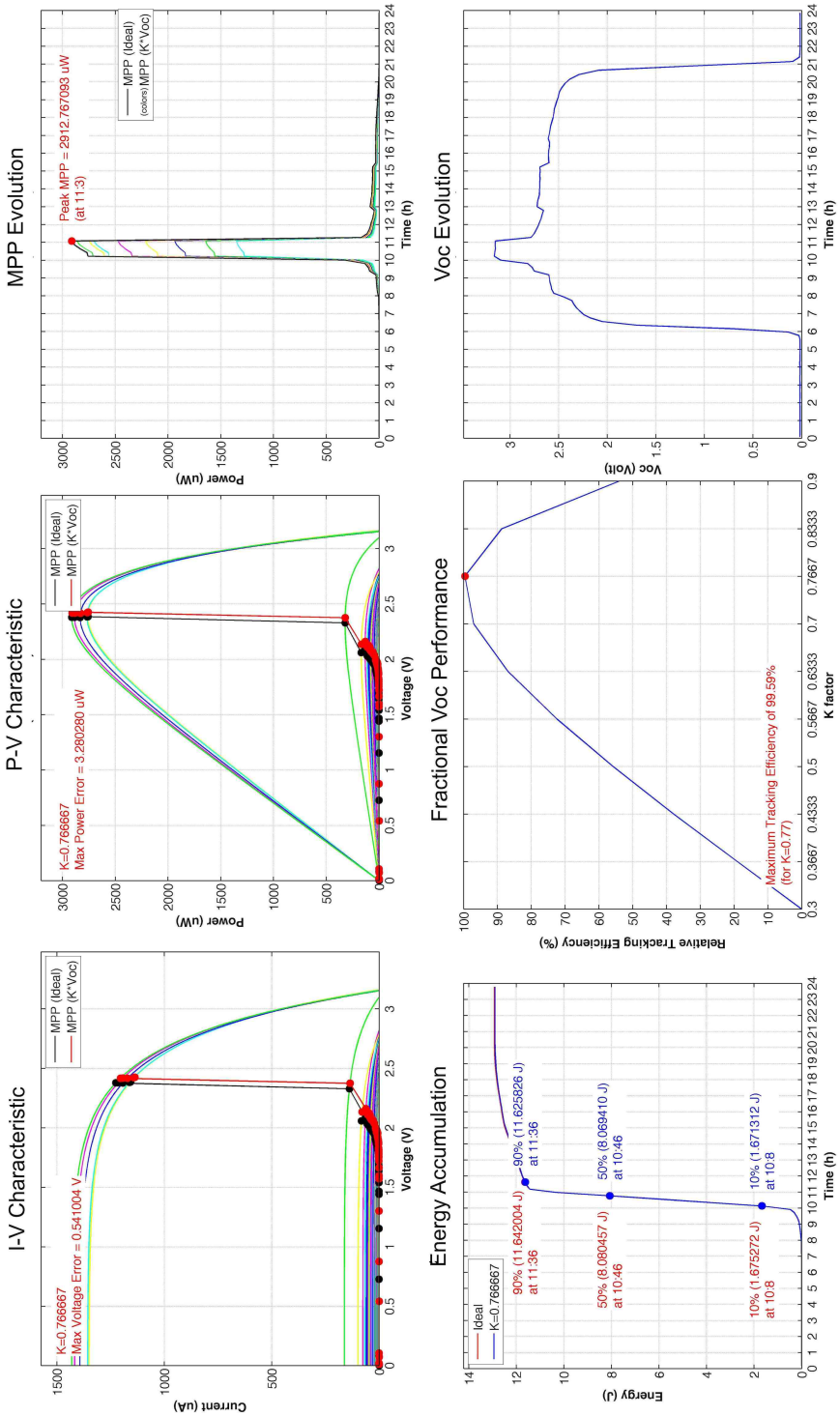
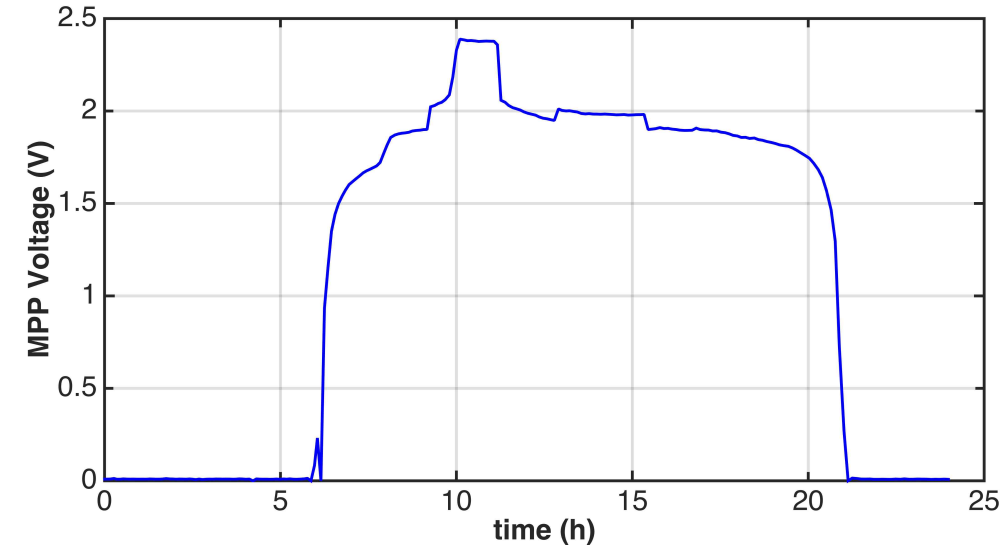
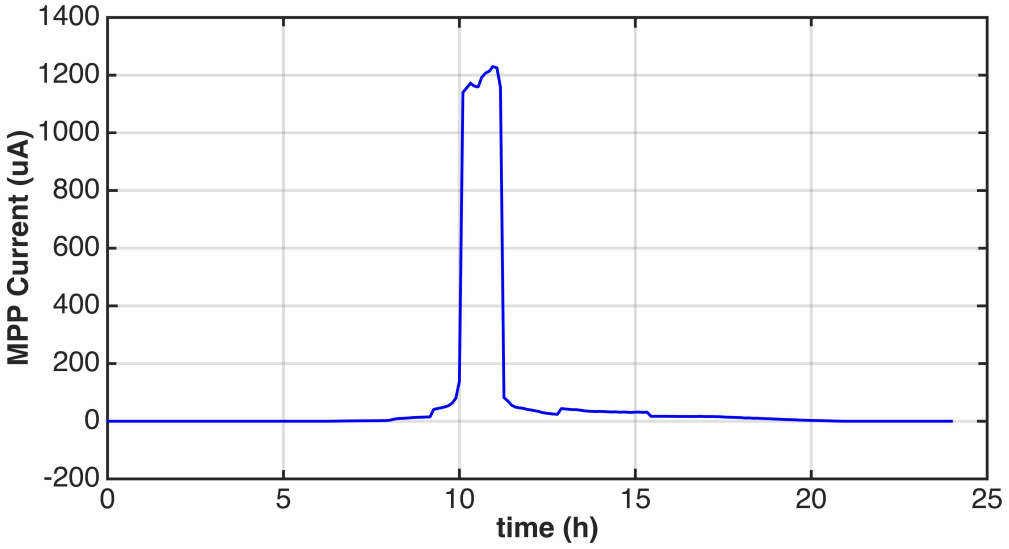


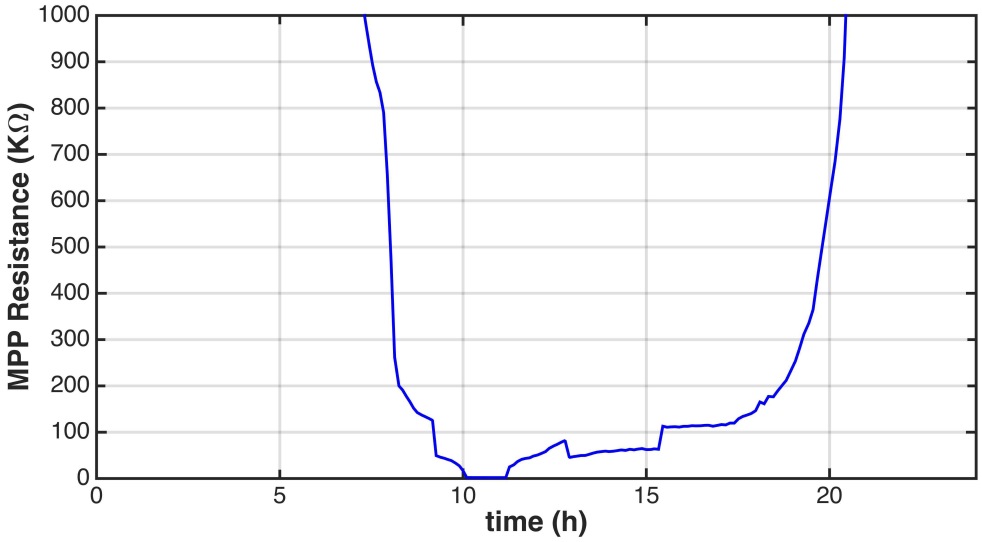
Figure B.5: PV data for the CYMBET CBC-PV-01N on 19th of May of 2015. Test made on location A.



(a)



(b)



(c)

Figure B.6: Maximum power point coordinates for the CYMBET CBC-PV-01N on 19th of May of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

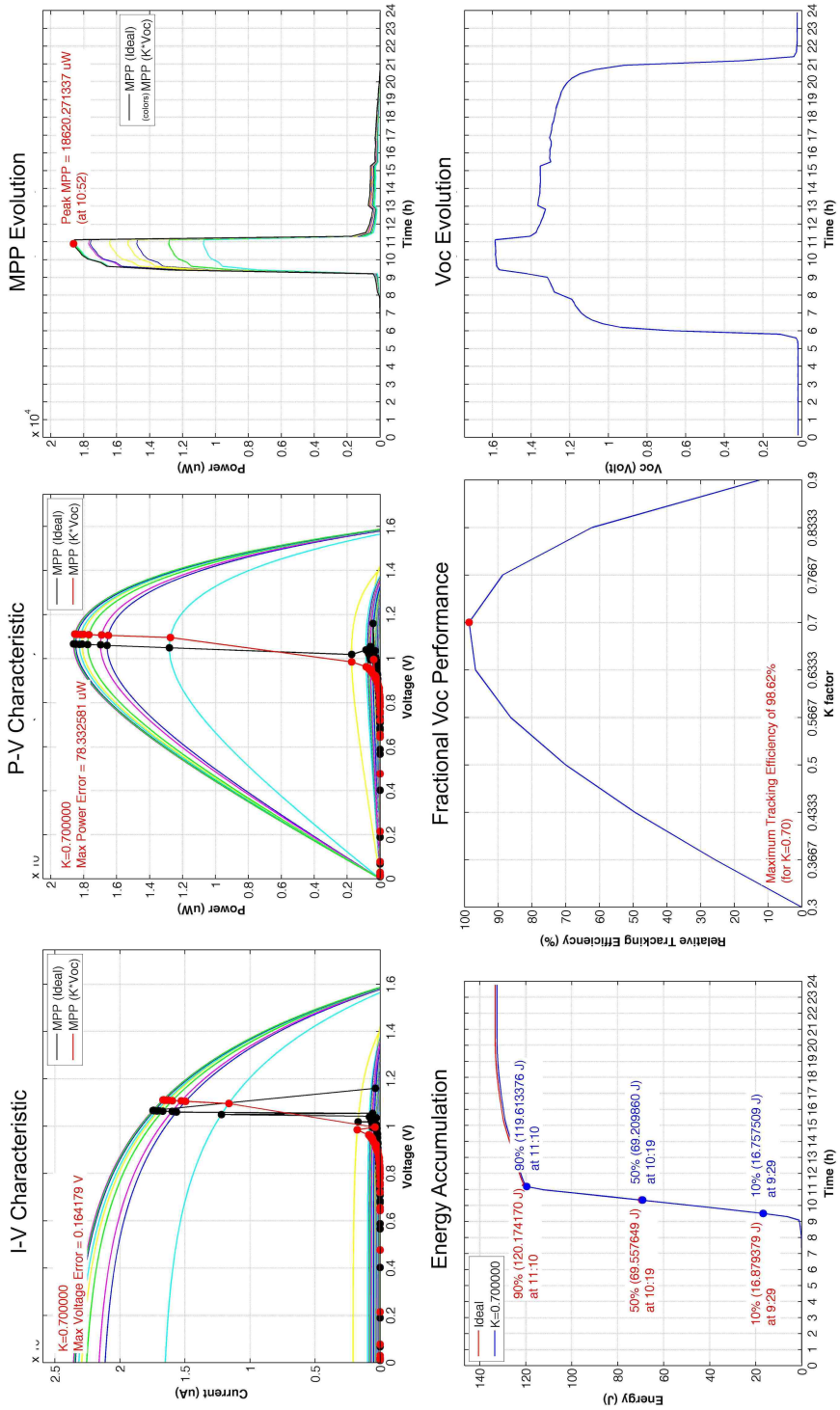
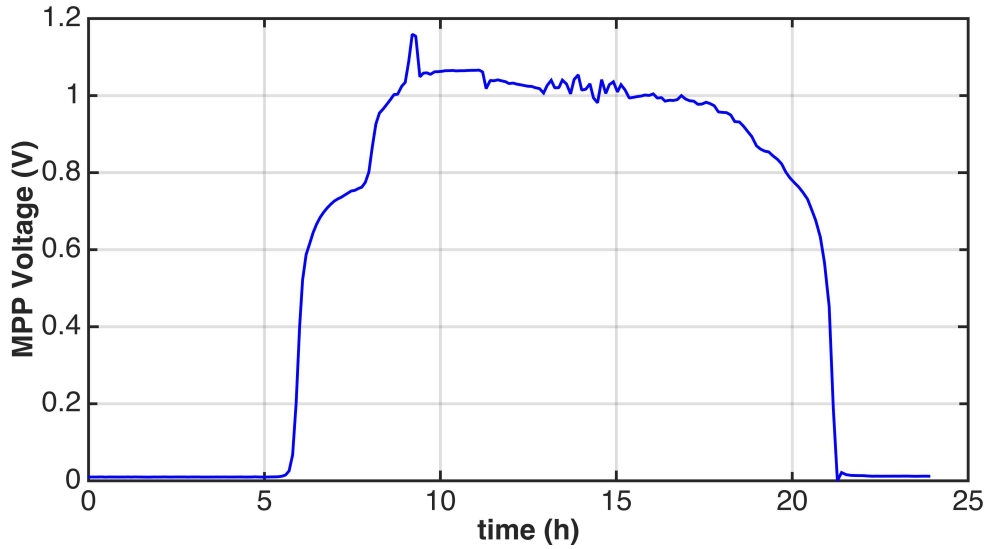
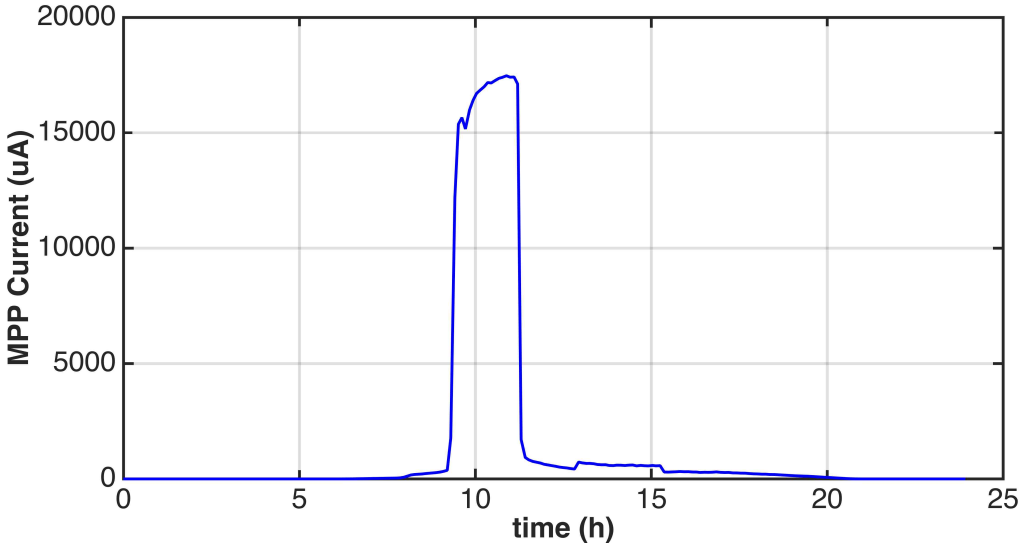


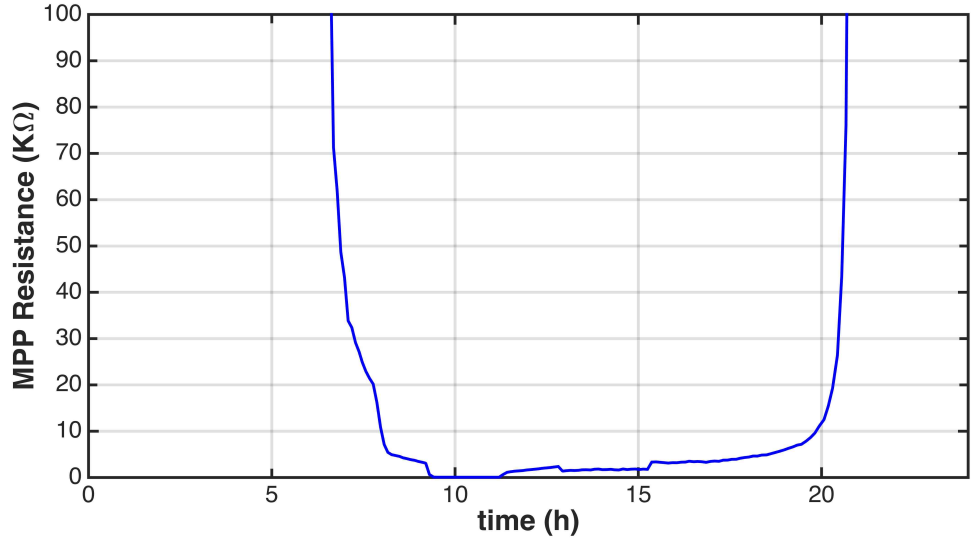
Figure B.7: PV data for the Amorton AM-1454 on 19th of May of 2015. Test made on location A.



(a)



(b)



(c)

Figure B.8: Maximum power point coordinates for the Amorton AM-1454 CA on 19th of May of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

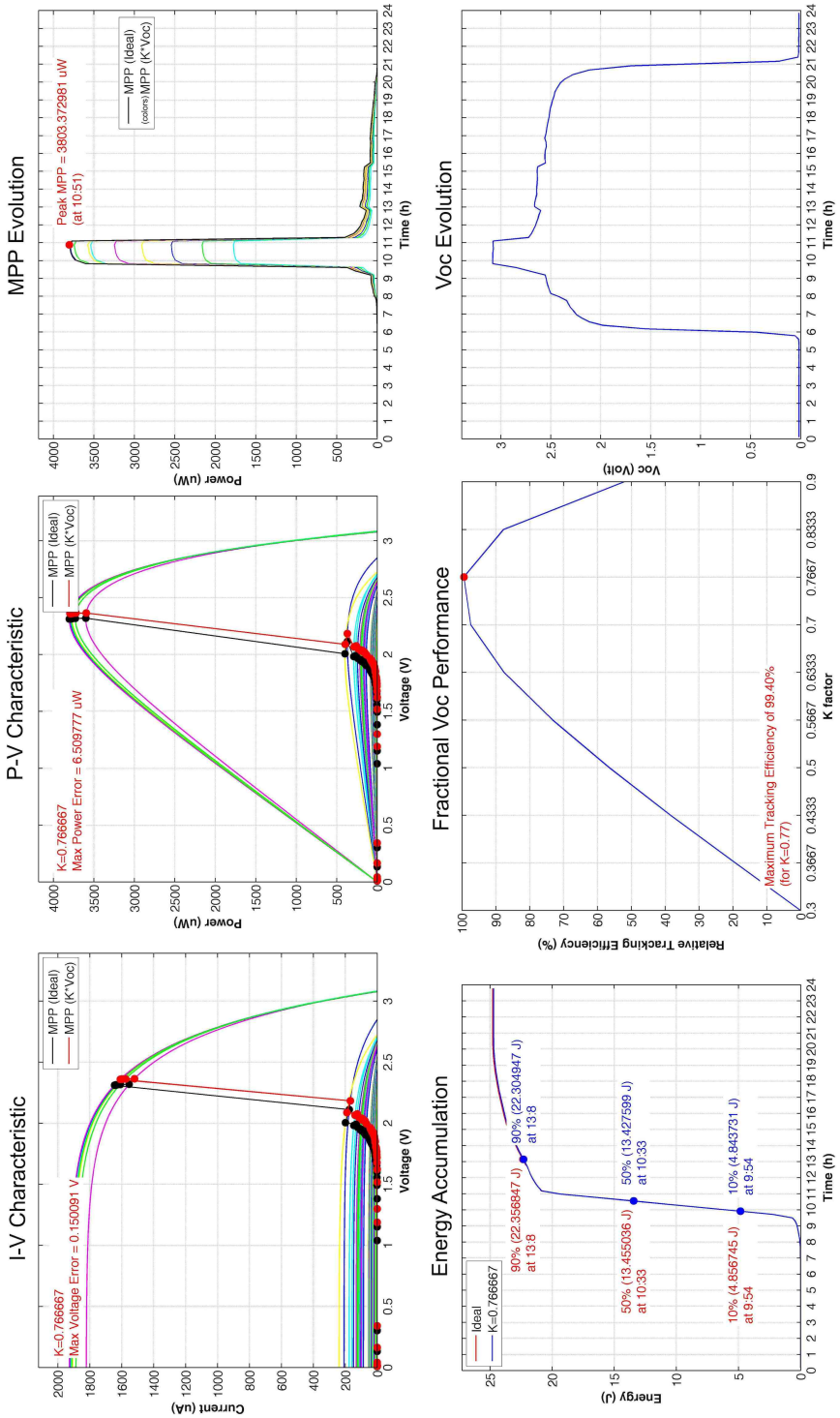
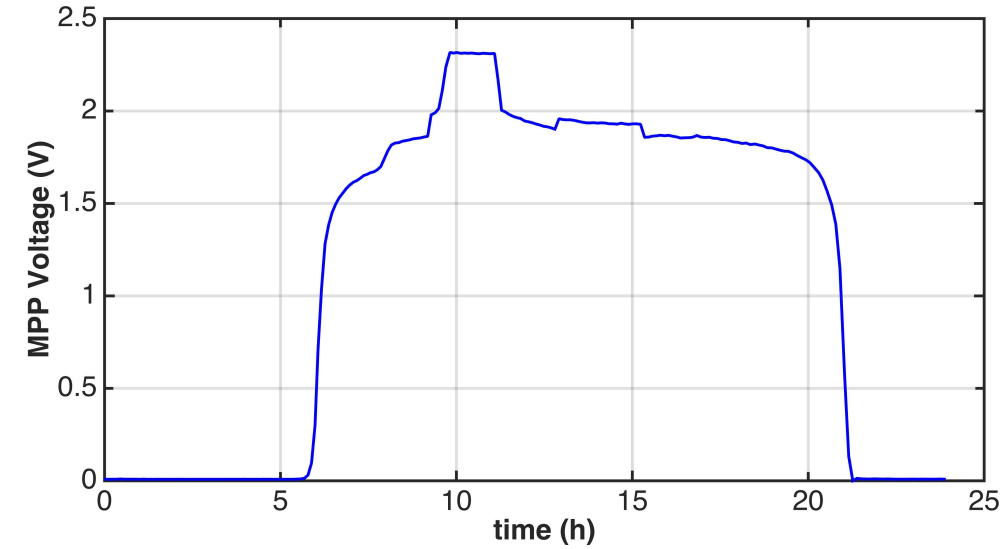
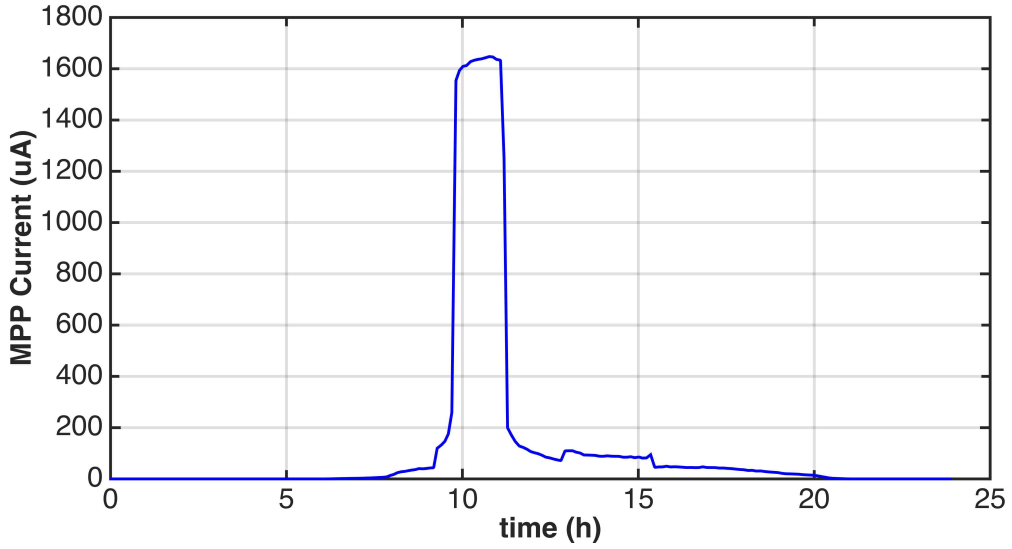


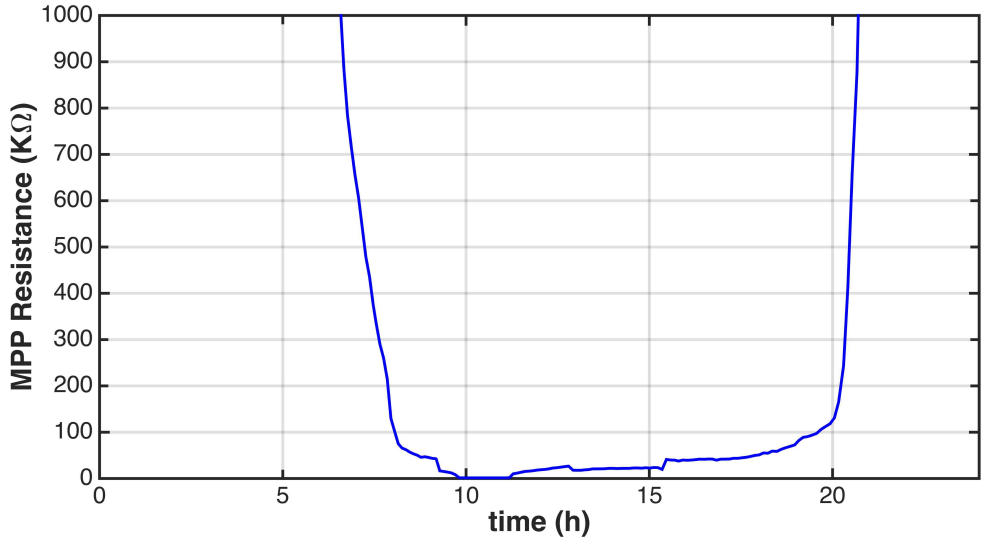
Figure B.9: PV data for the Amorton AM-1417 on 19th of May of 2015. Test made on location A.



(a)



(b)



(c)

Figure B.10: Maximum power point coordinates for the Amorton AM-1417 CA on 19th of May of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

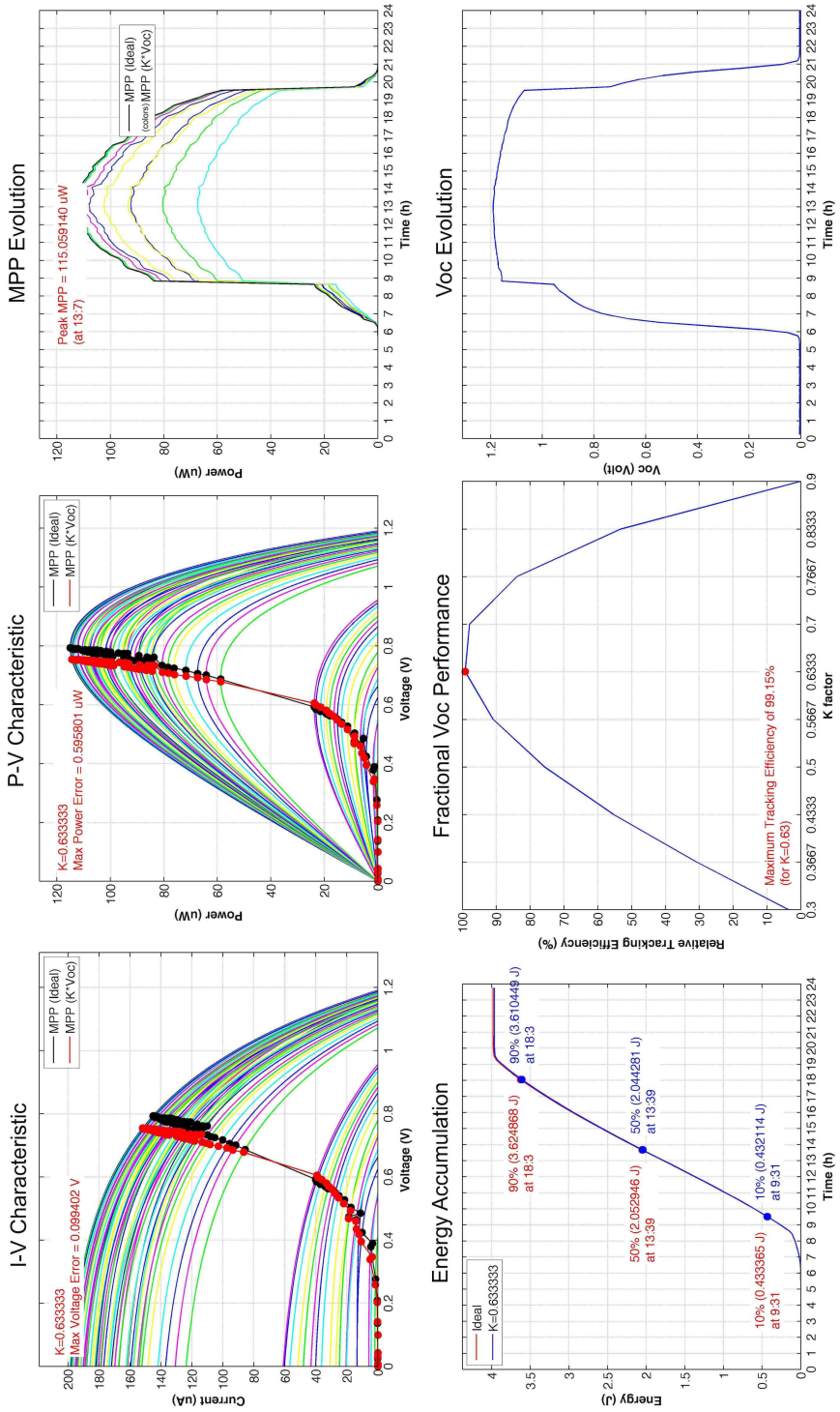
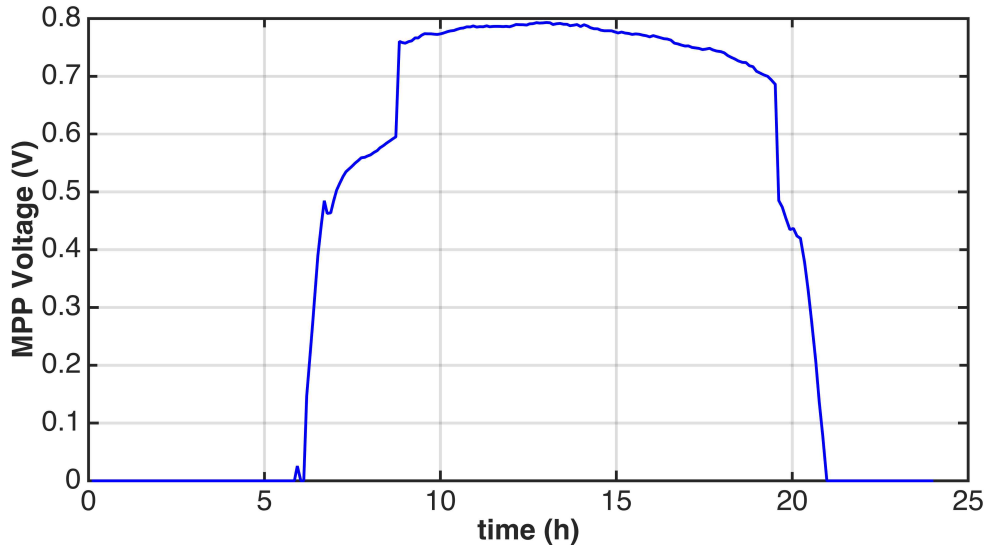
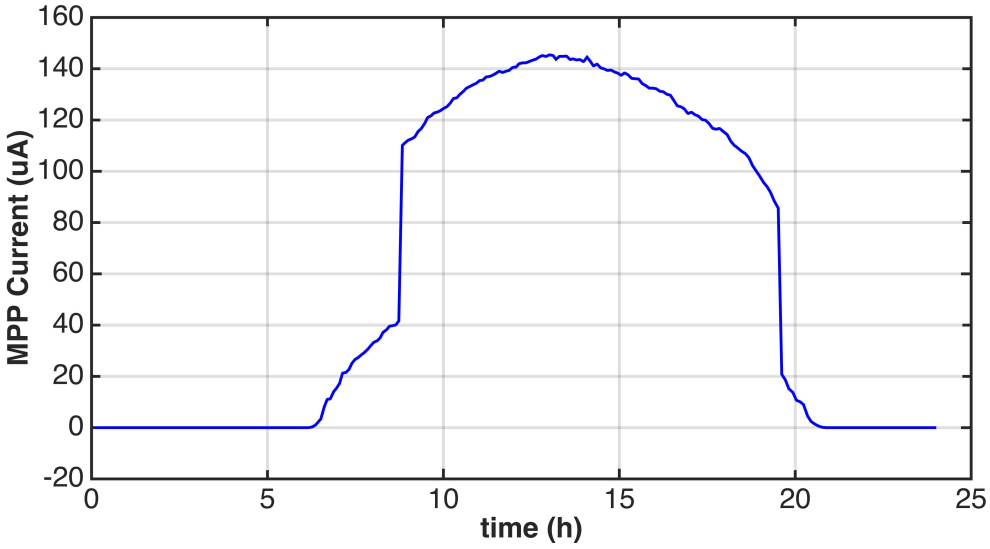


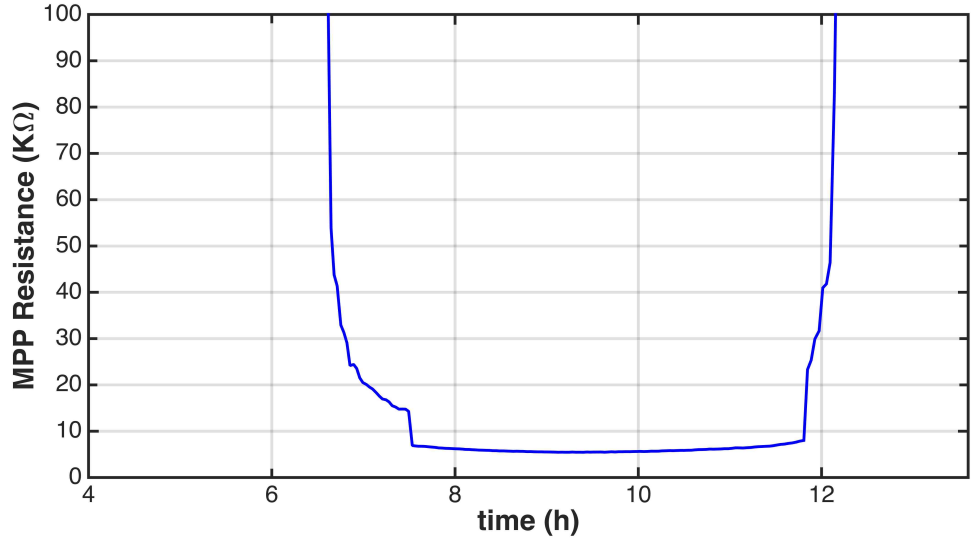
Figure B.11: PV data for the IXYS SLMD121H04L on 22nd of May of 2015. Test made on location B.



(a)



(b)



(c)

Figure B.12: Maximum power point coordinates for the IXYS SLMD121H04L on 22nd of May of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

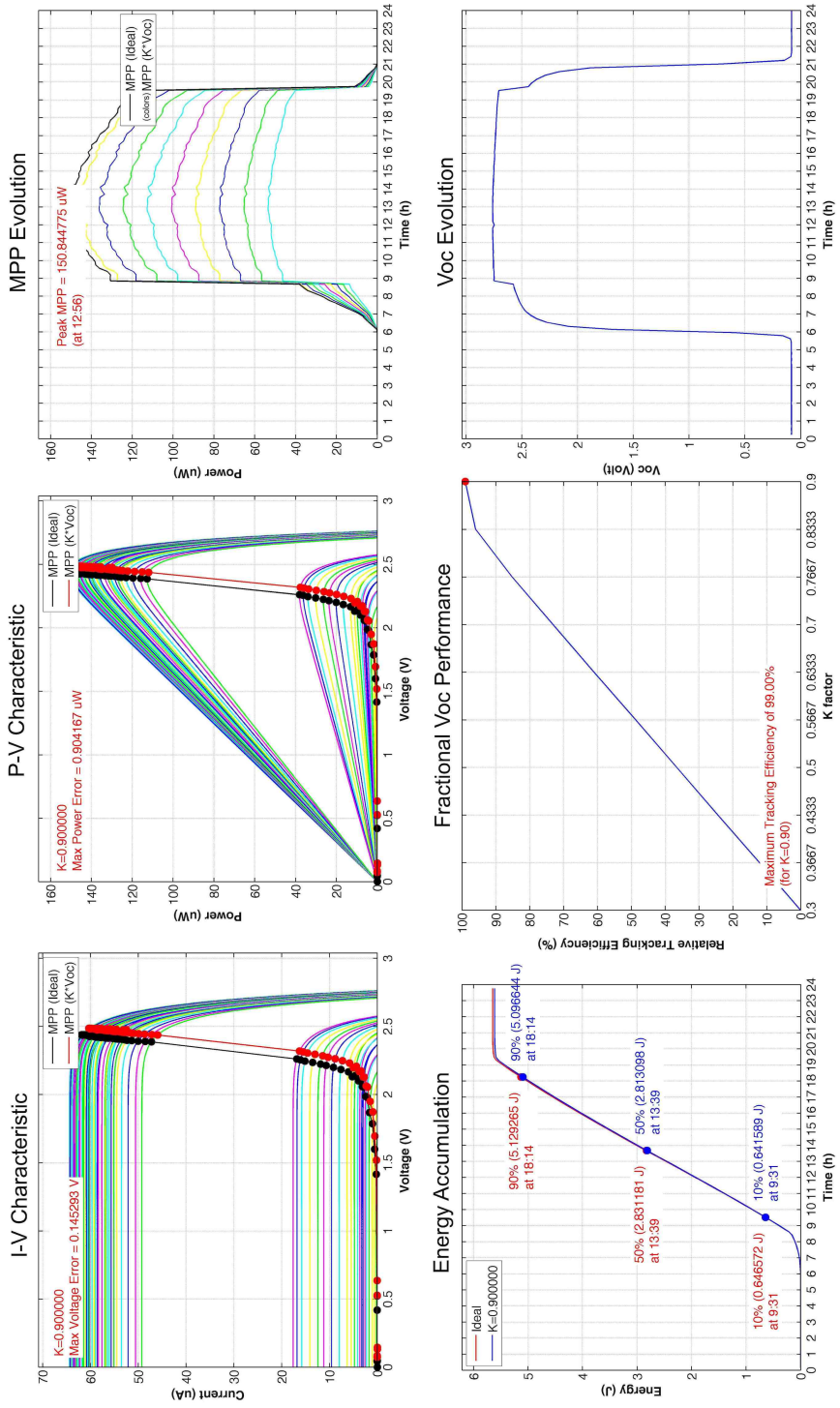
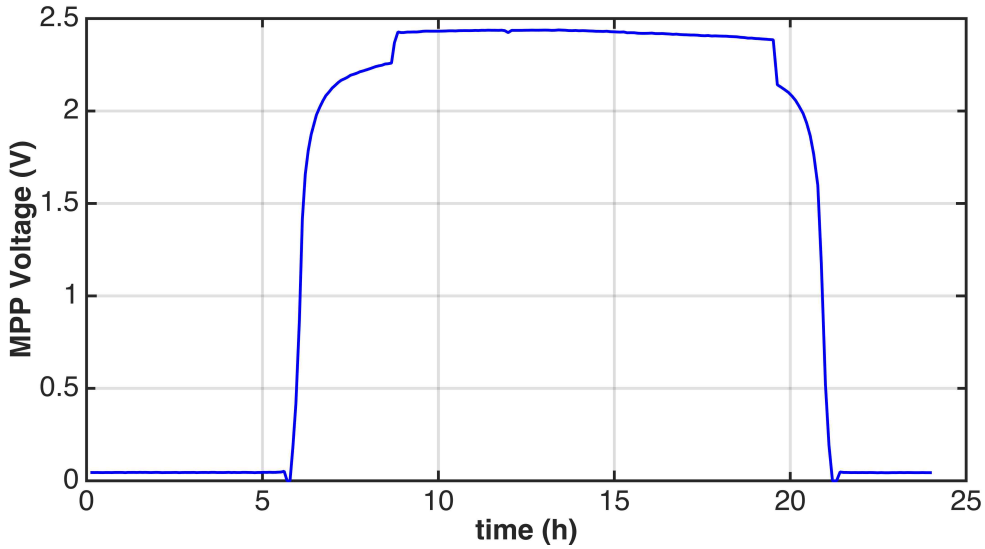
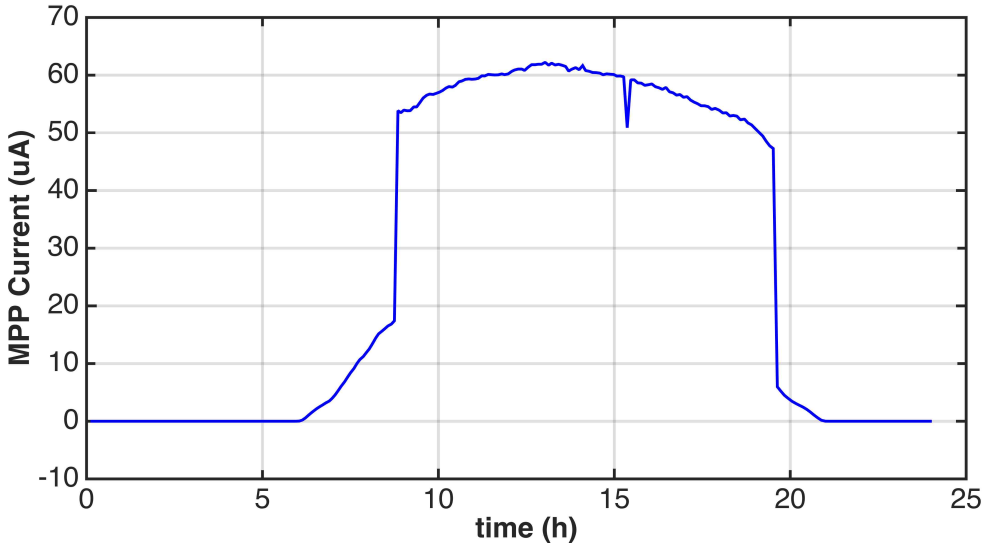


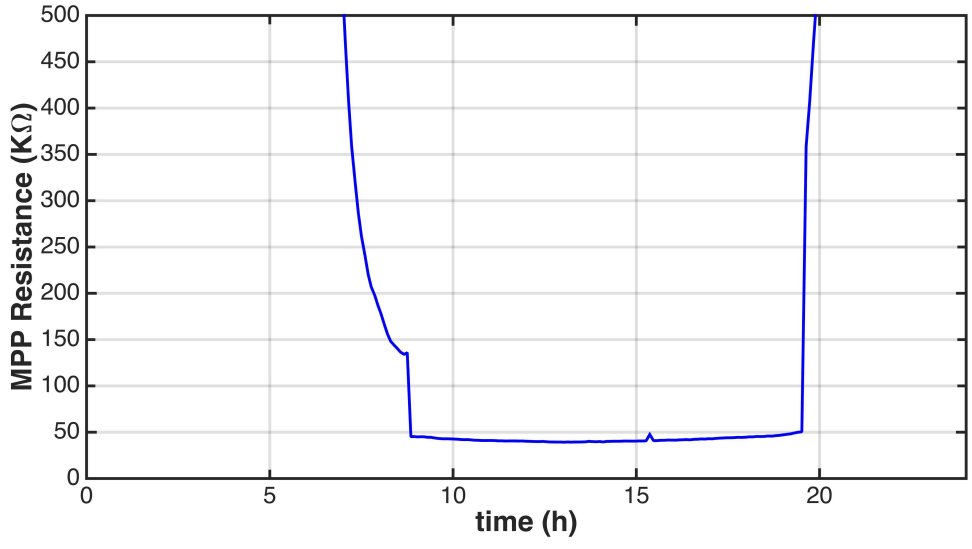
Figure B.13: PV data for the CYMBET CBC-PV-01N on 22nd of May of 2015. Test made on location B.



(a)



(b)



(c)

Figure B.14: Maximum power point coordinates for the CYMBET CBC-PV-01N on 22nd of May of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

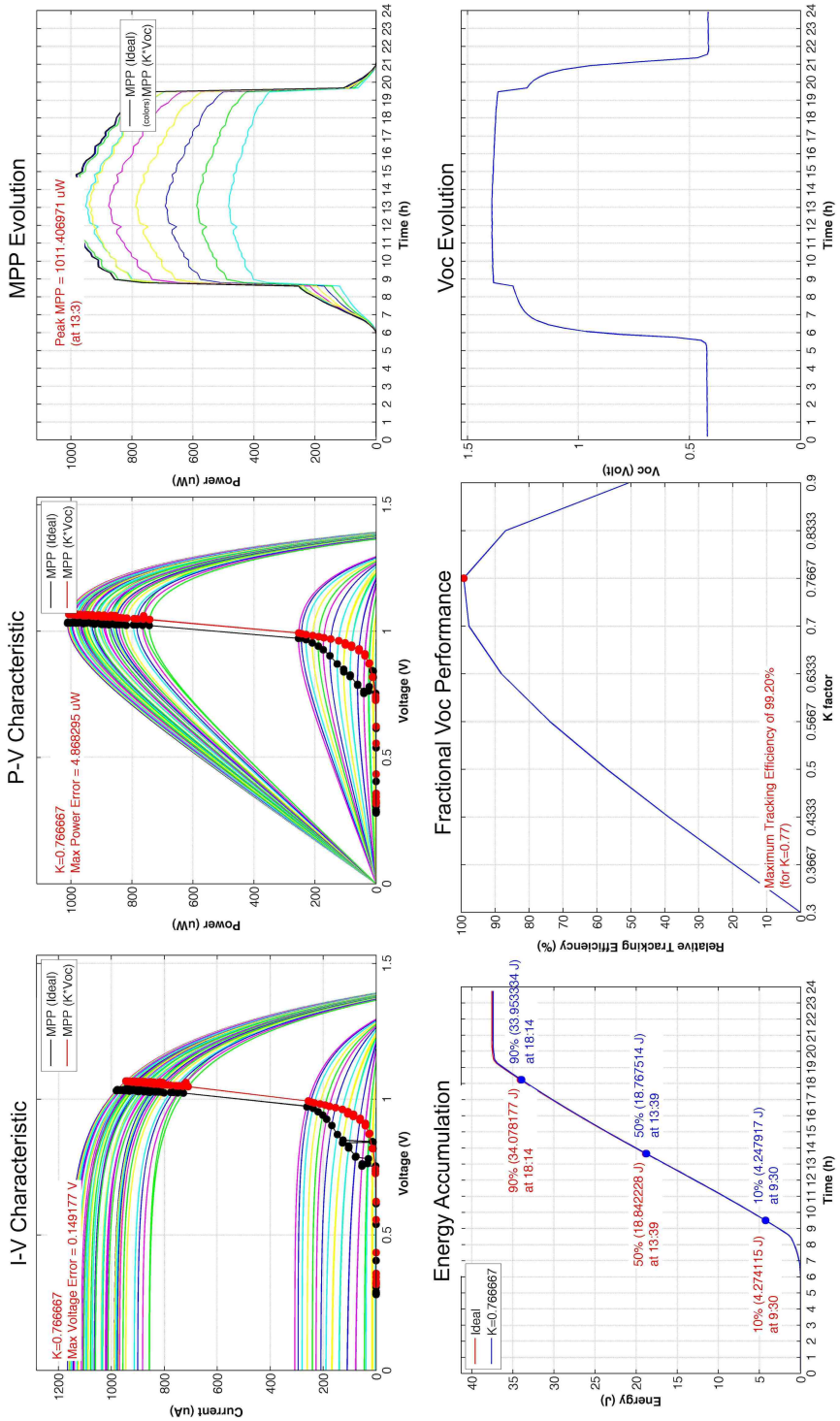
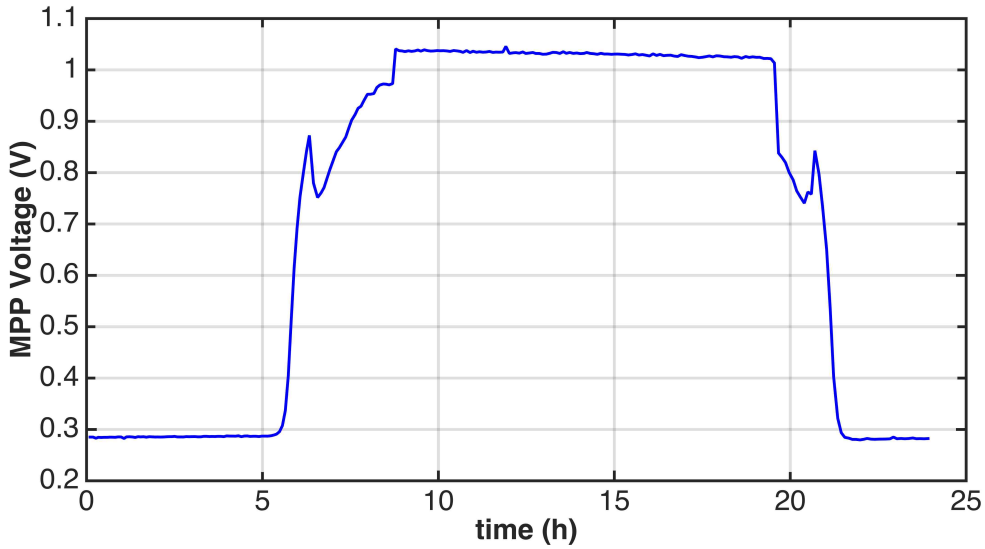
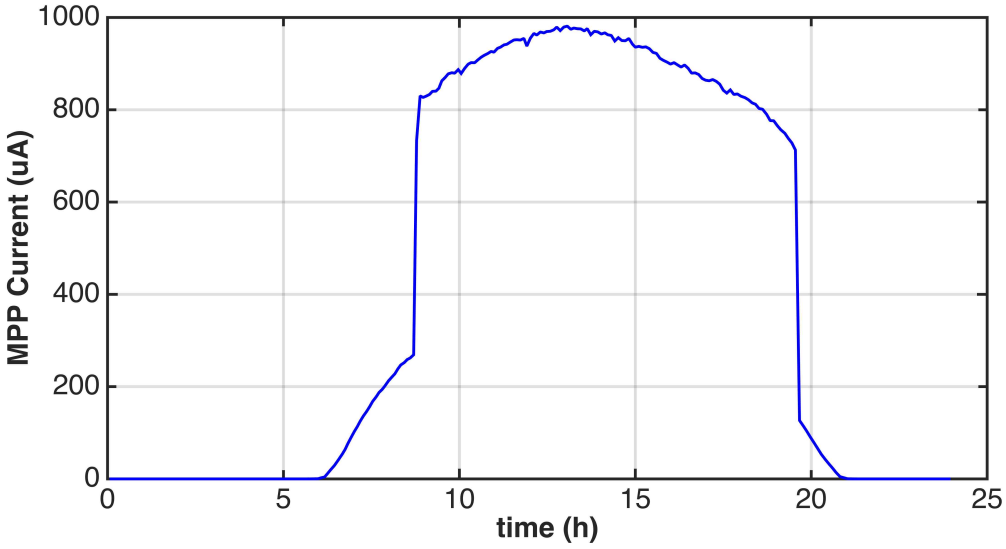


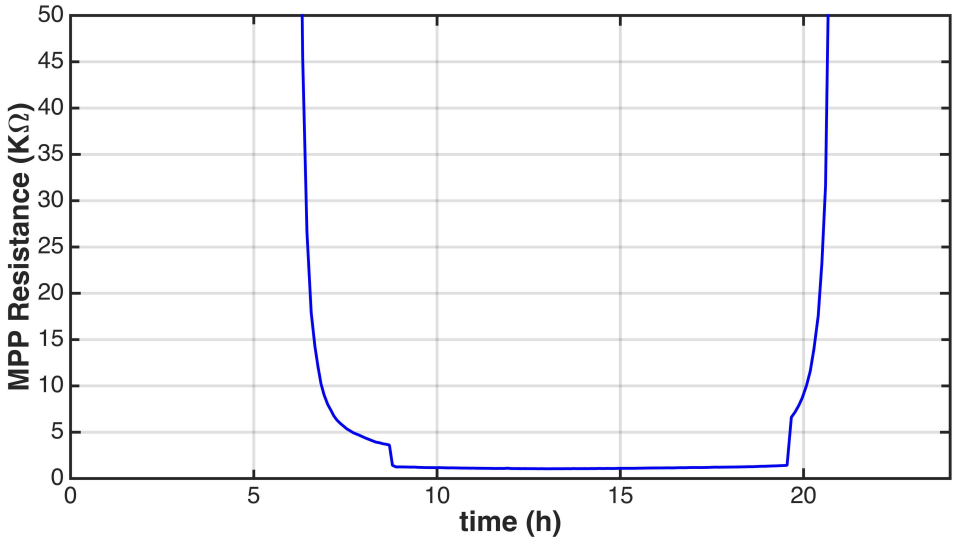
Figure B.15: PV data for the Amorton AM-1454 on 22nd of May of 2015. Test made on location B.



(a)



(b)



(c)

Figure B.16: Maximum power point coordinates for the Amorton AM-1454 CA on 22nd of May of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

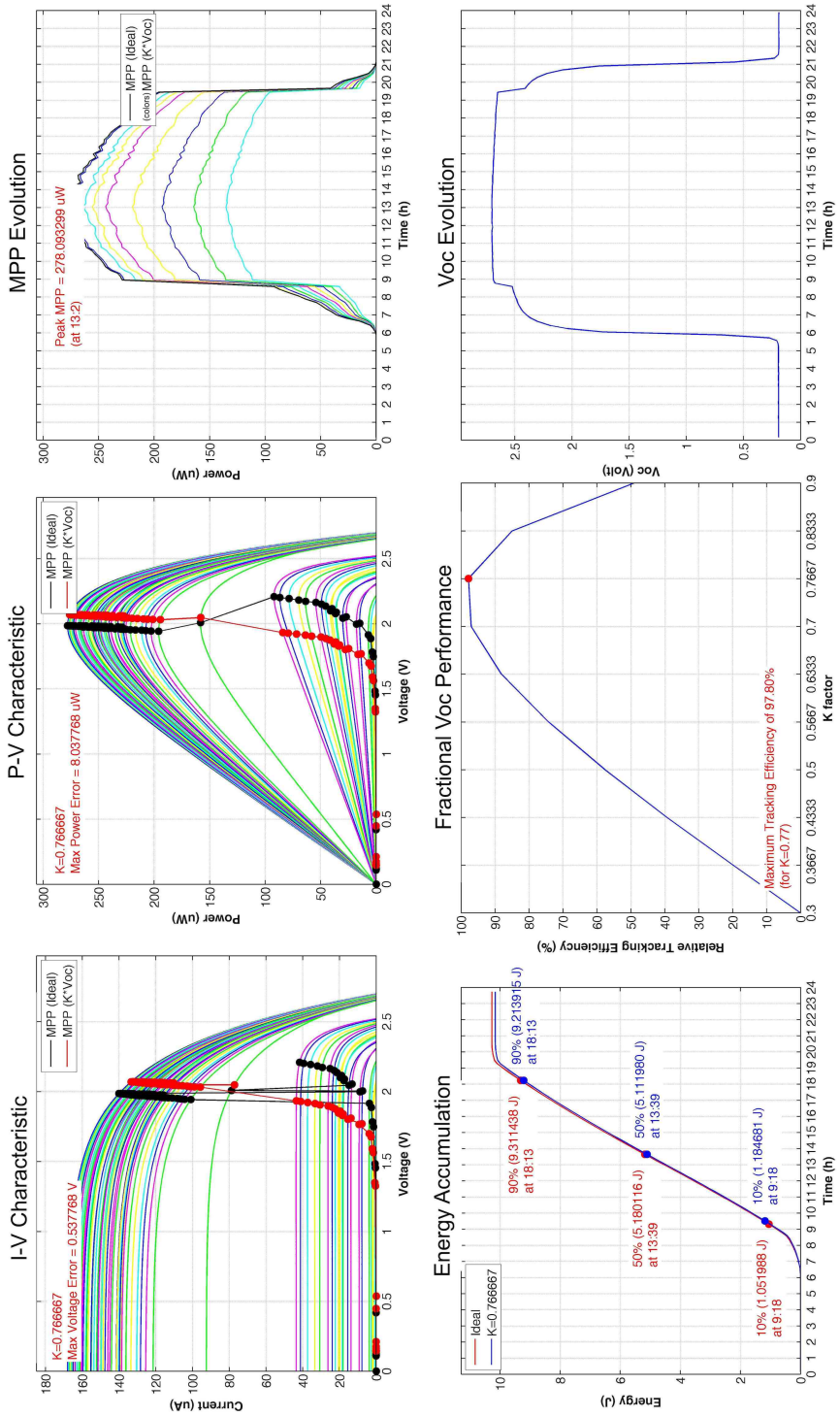
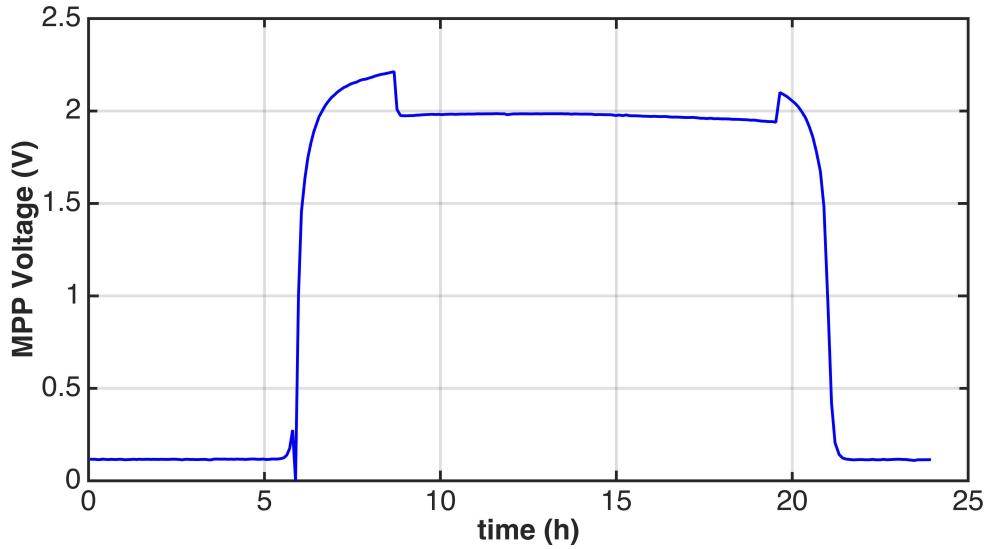
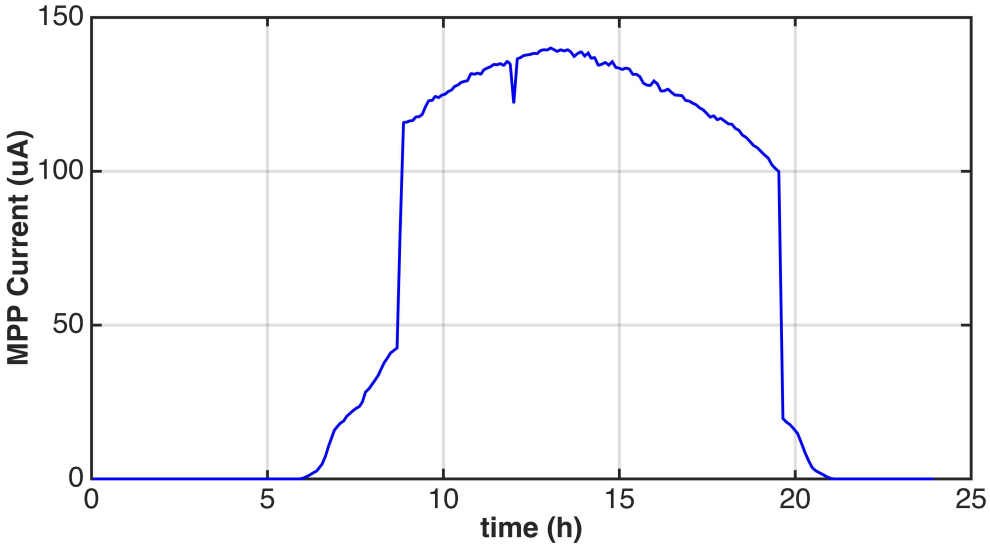


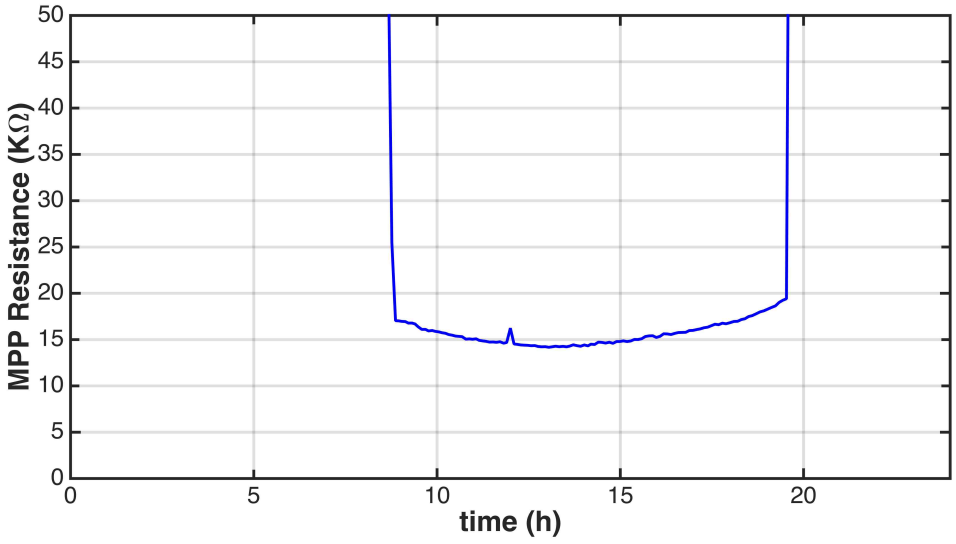
Figure B.17: PV data for the Amorton AM-1417 on 22nd of May of 2015. Test made on location B.



(a)



(b)



(c)

Figure B.18: Maximum power point coordinates for the Amorton AM-1417 CA on 22nd of May of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

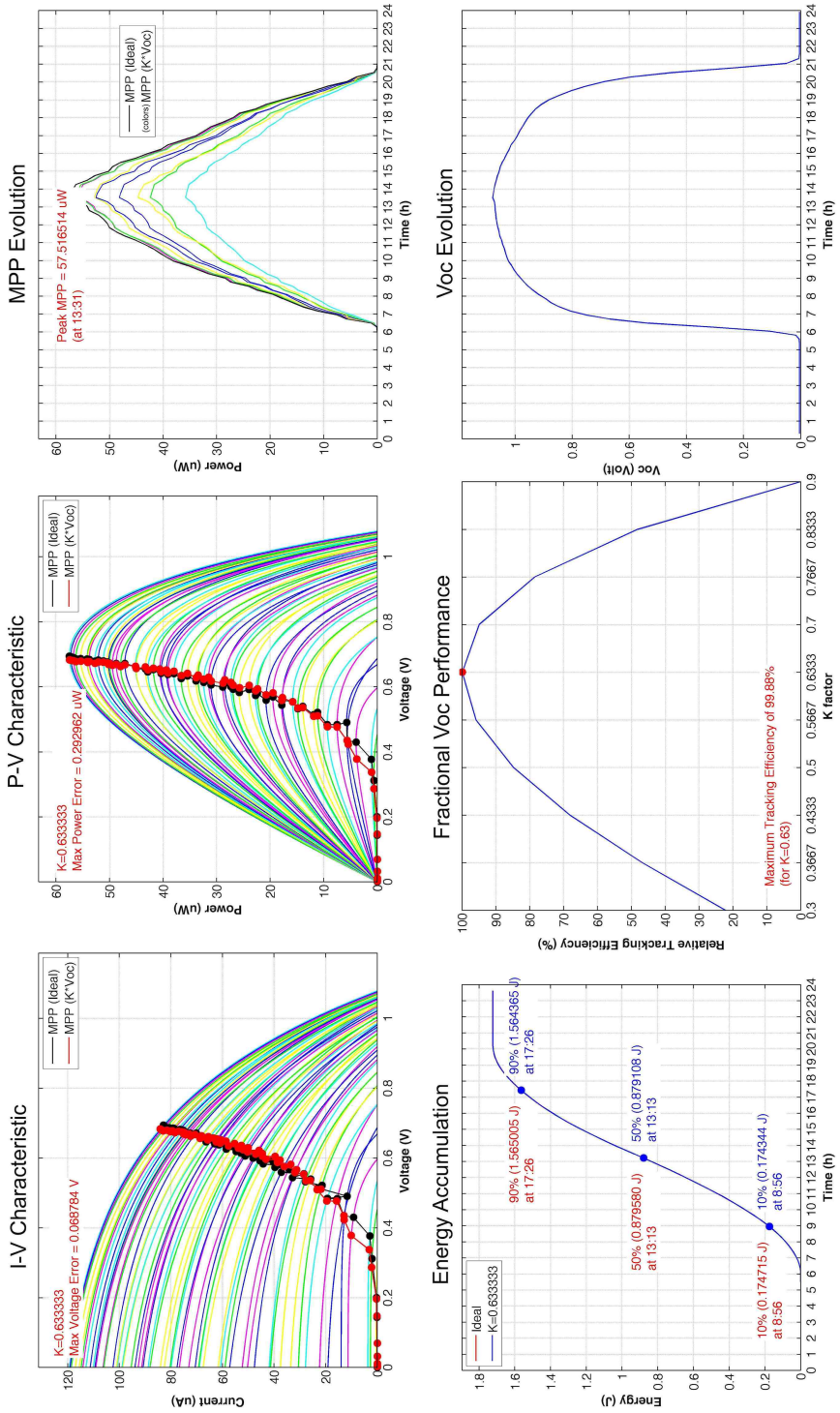
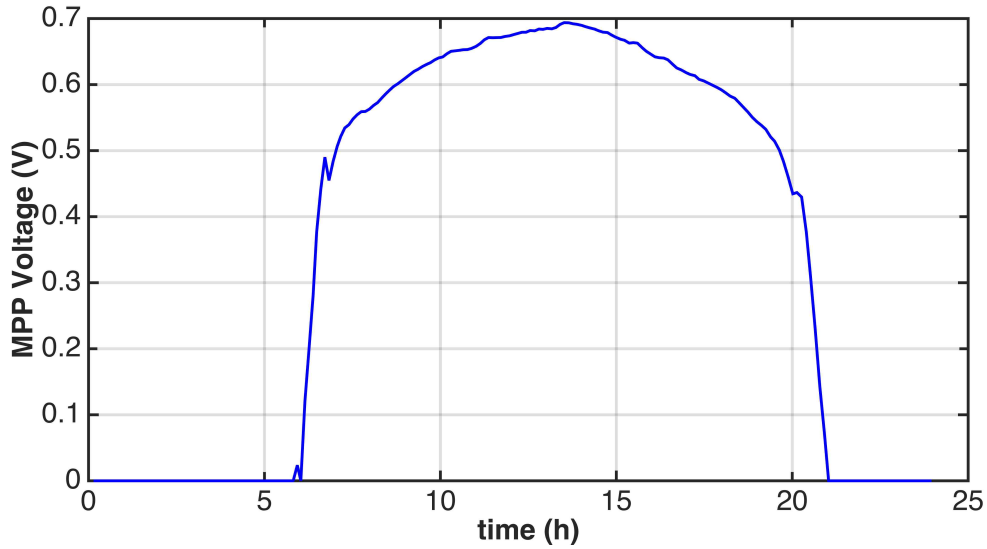
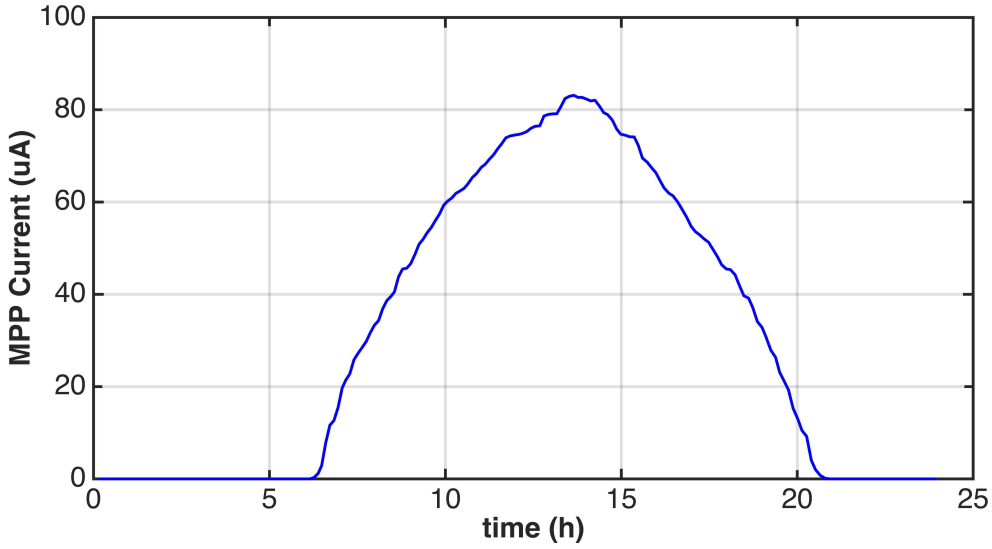


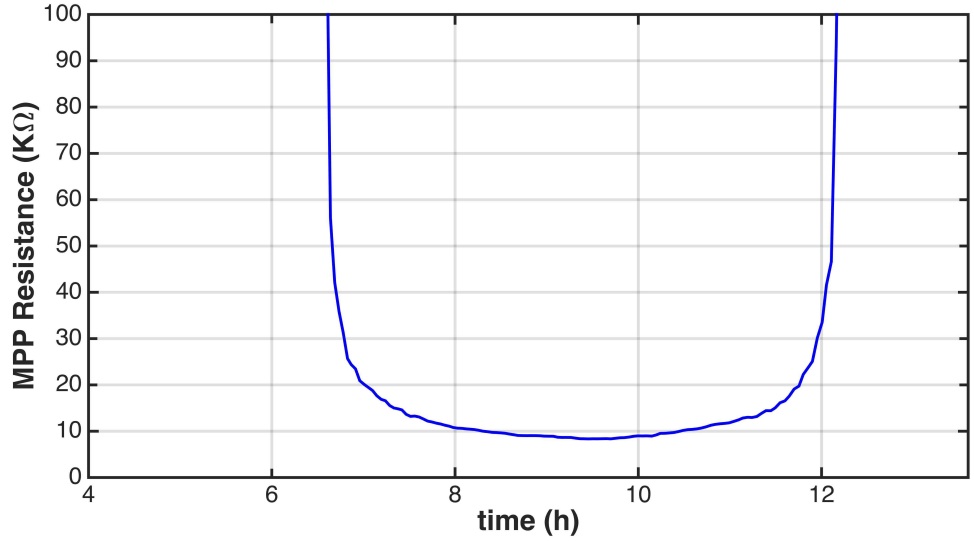
Figure B.19: PV data for the IXYS SLMD121H04L on 23rd of May of 2015. Test made on location B.



(a)



(b)



(c)

Figure B.20: Maximum power point coordinates for the IXYS SLMD121H04L on 23rd of May of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

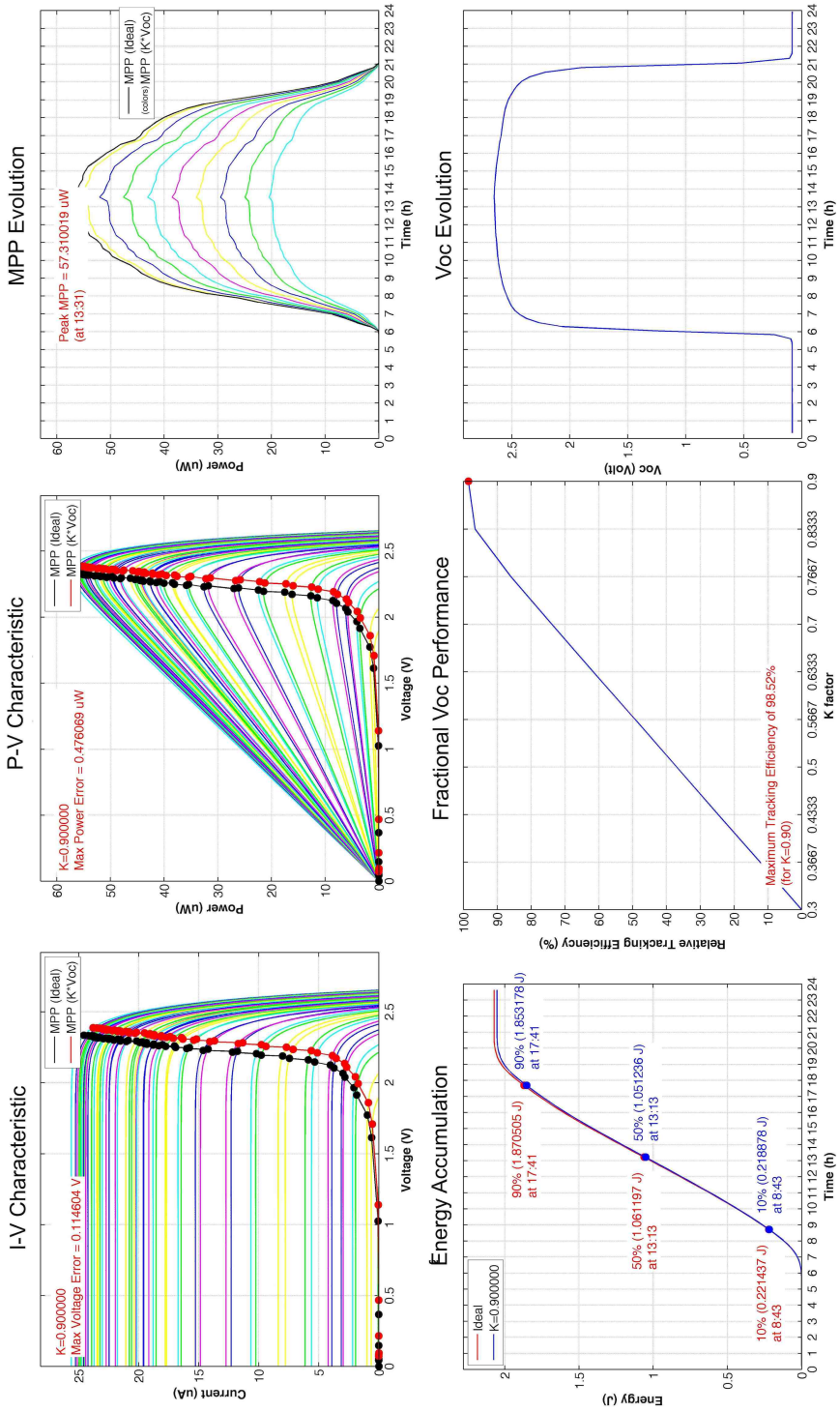
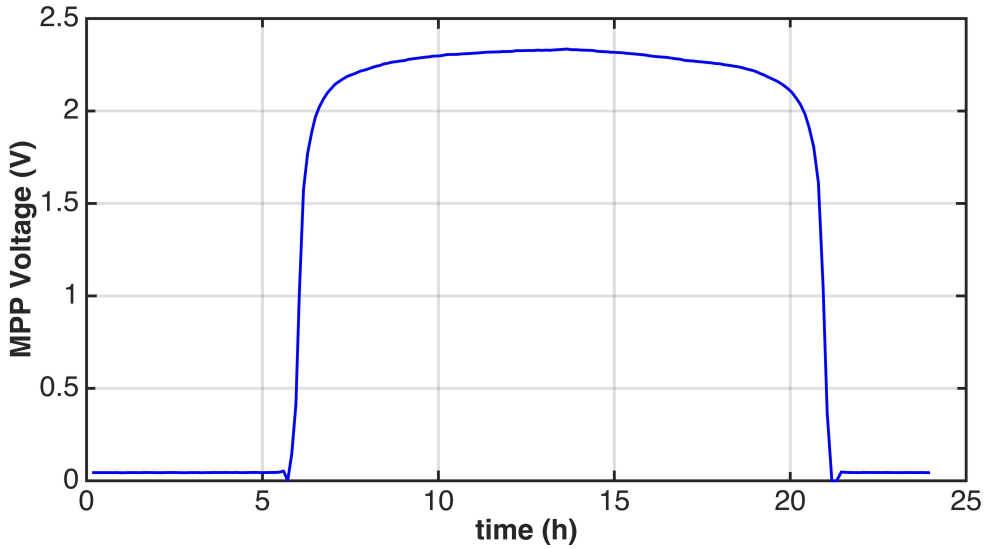
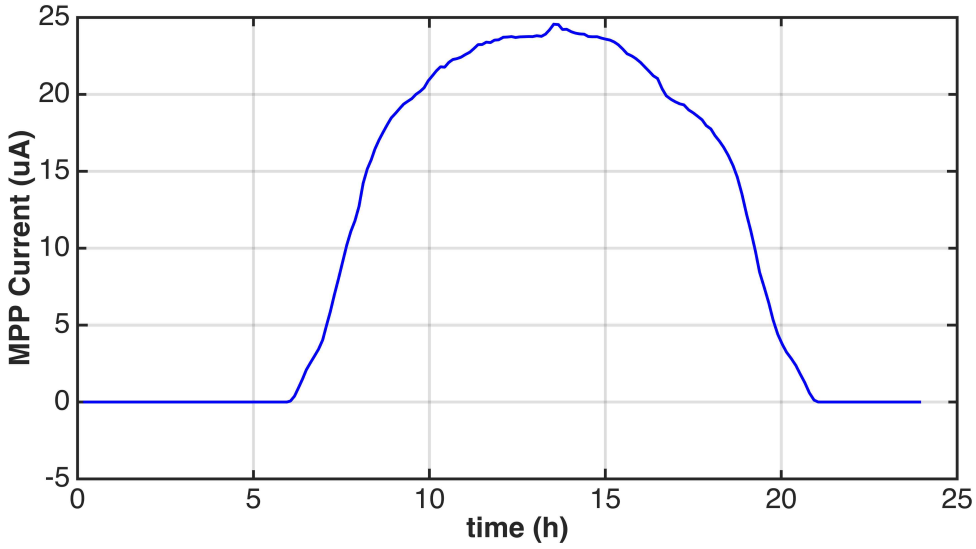


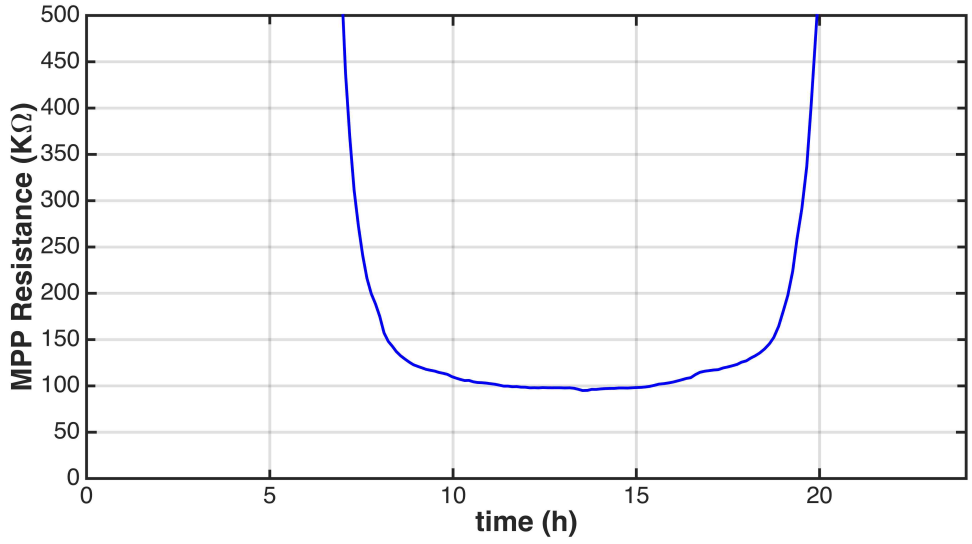
Figure B.21: PV data for the CYMBET CBC-PV-01N on 23rd of May of 2015. Test made on location B.



(a)



(b)



(c)

Figure B.22: Maximum power point coordinates for the CYMBET CBC-PV-01N on 23rd of May of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

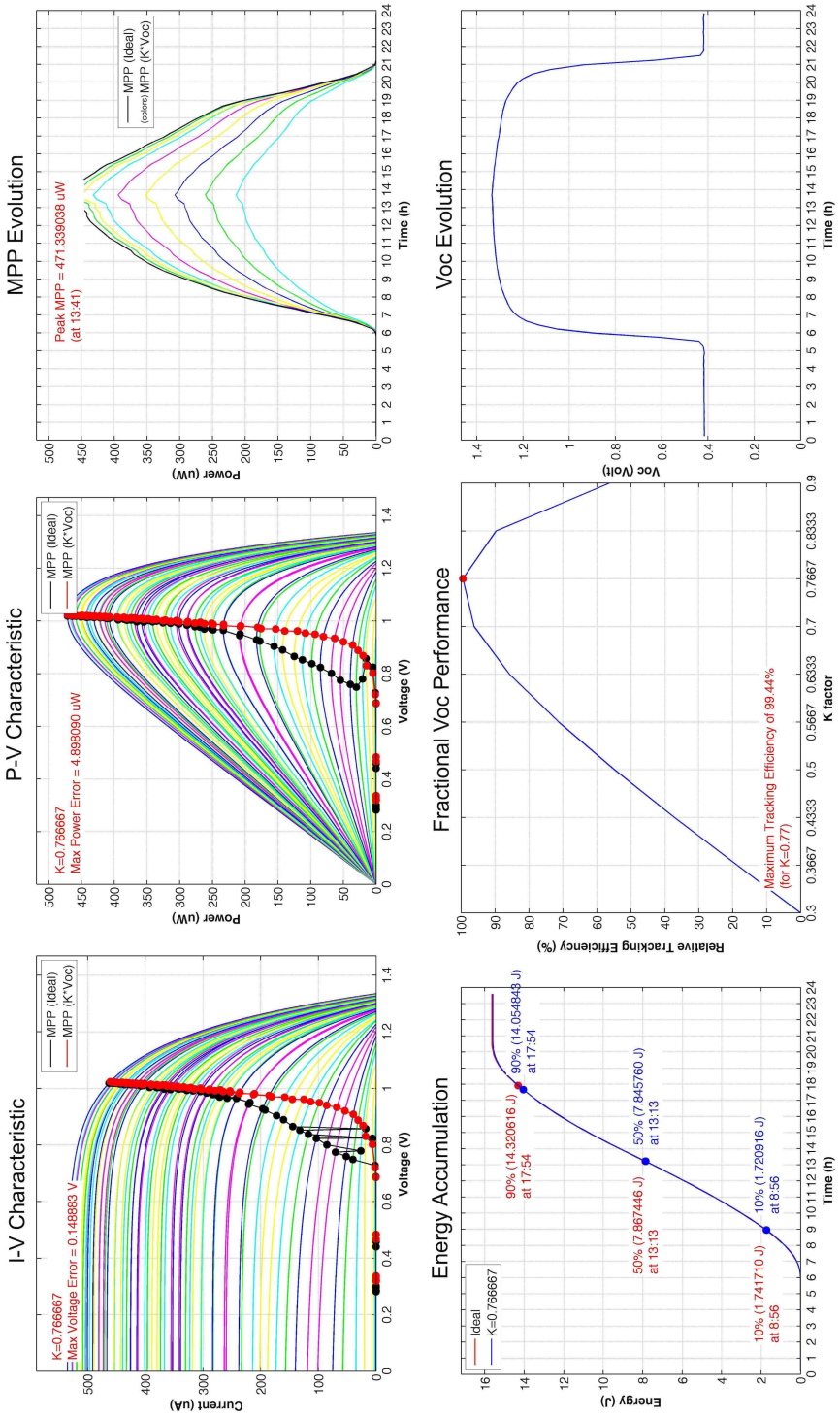
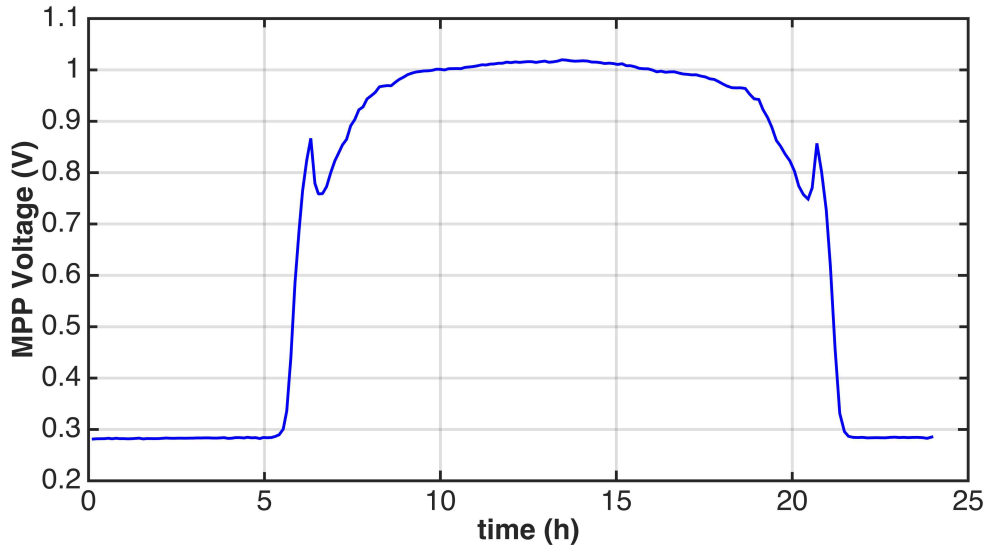
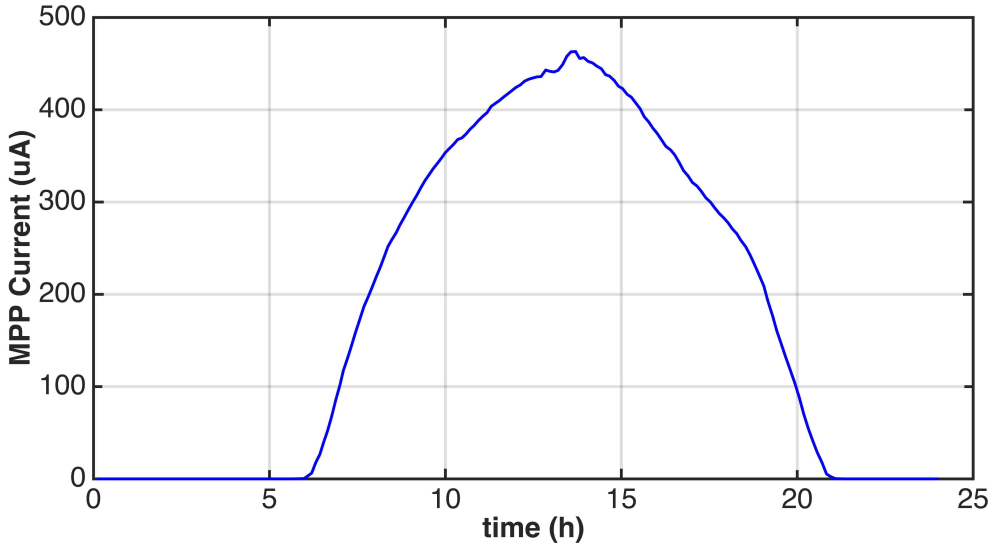


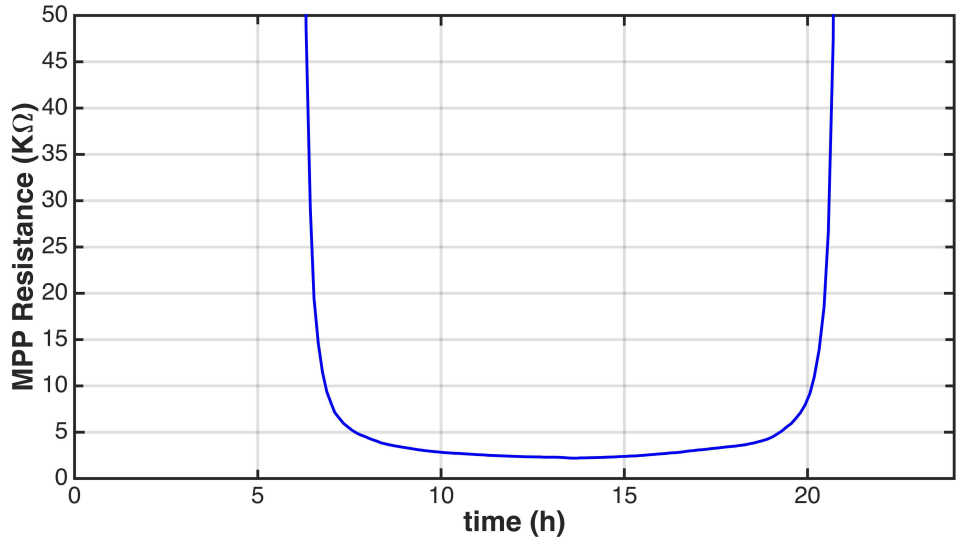
Figure B.23: PV data for the Amorton AM-1454 on 23rd of May of 2015. Test made on location B.



(a)



(b)



(c)

Figure B.24: Maximum power point coordinates for the Amorton AM-1454 CA on 23rd of May of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

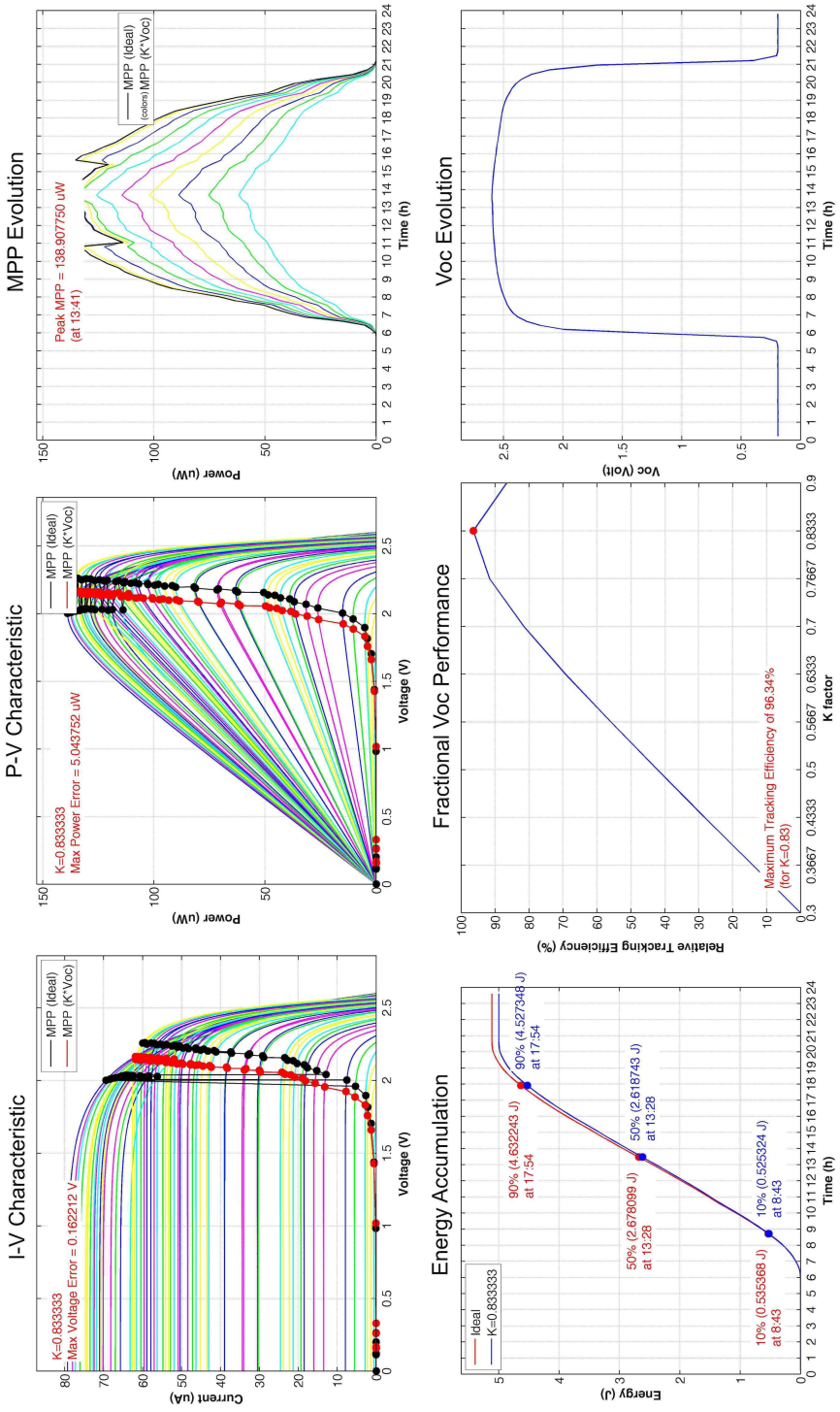
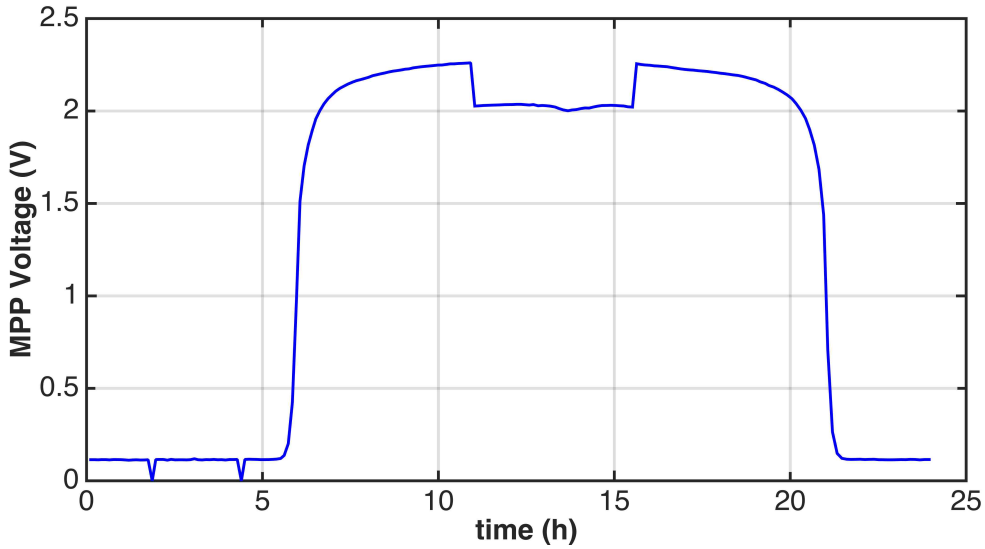
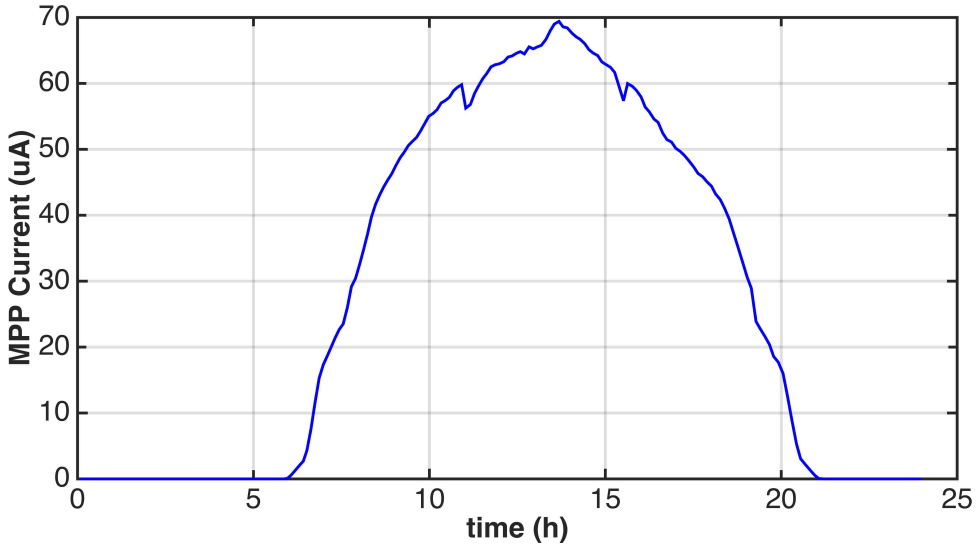


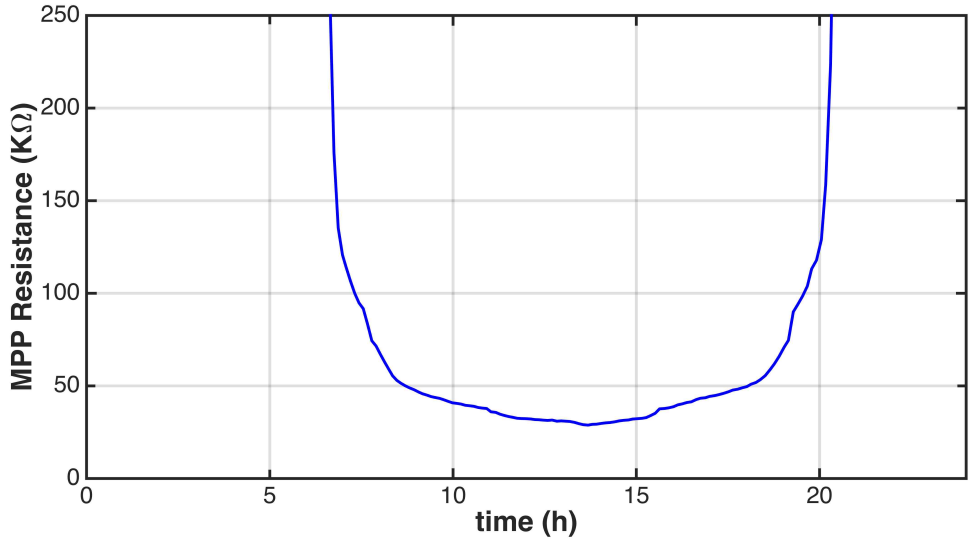
Figure B.25: PV data for the Amorton AM-1417 on 23rd of May of 2015. Test made on location B.



(a)



(b)



(c)

Figure B.26: Maximum power point coordinates for the Amorton AM-1417 CA on 23rd of May of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

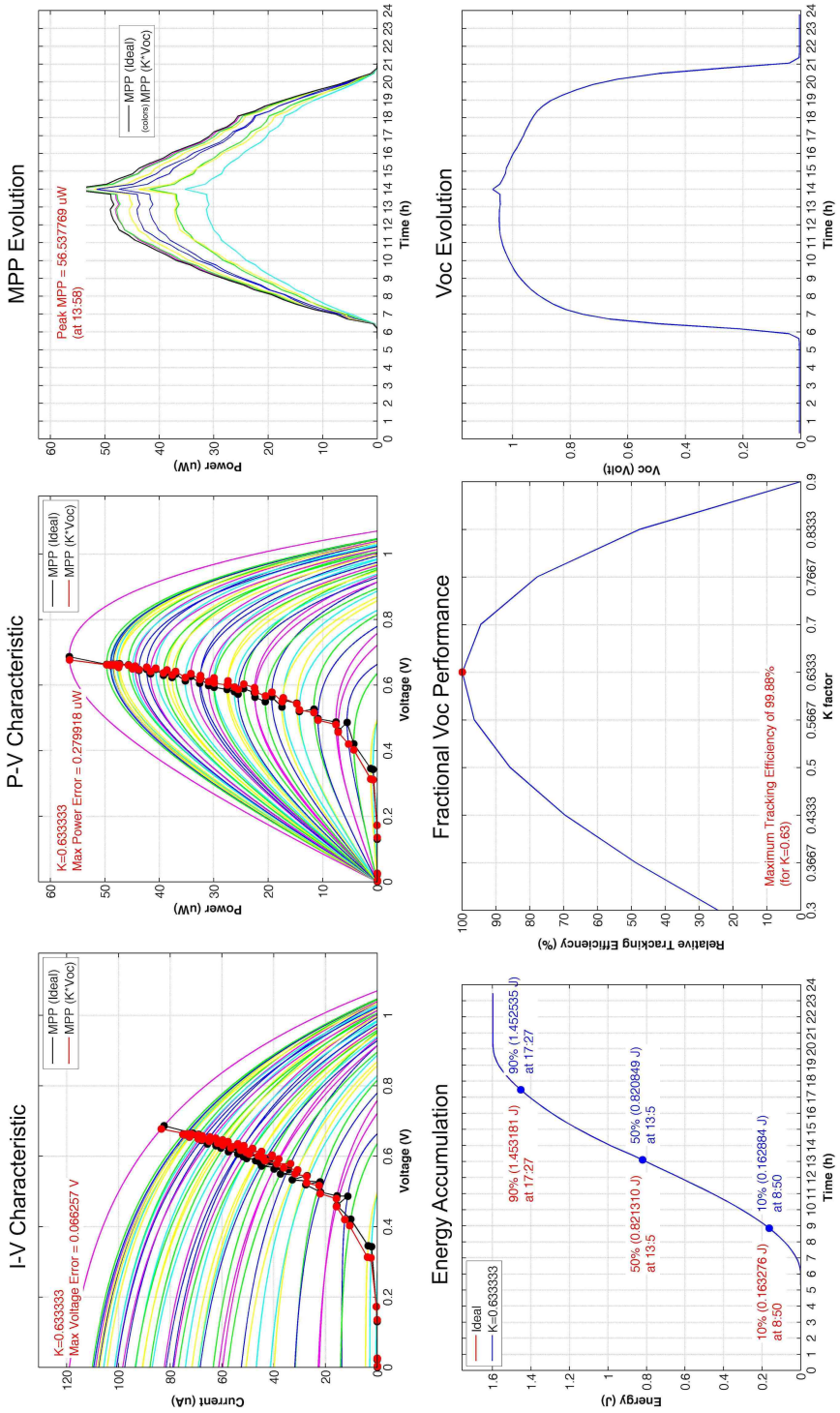
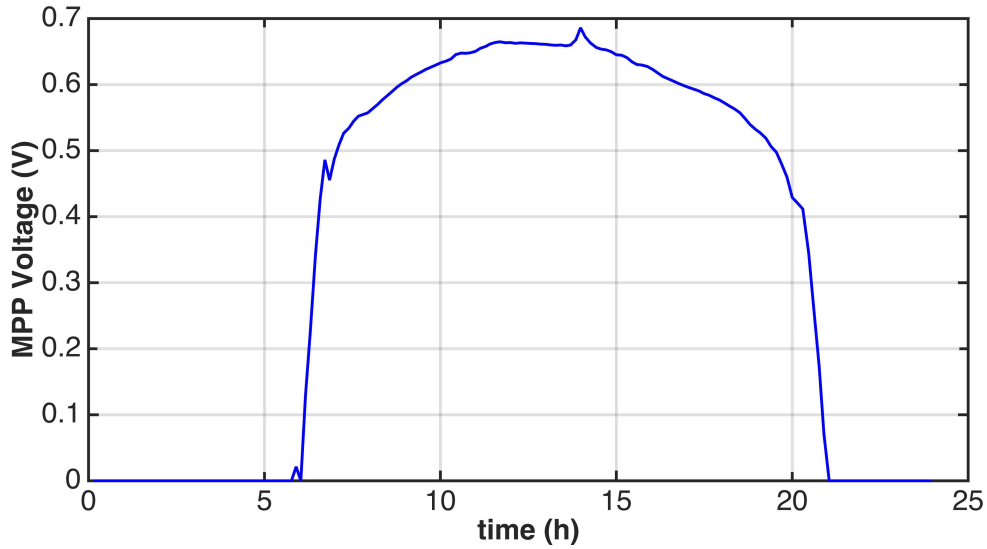
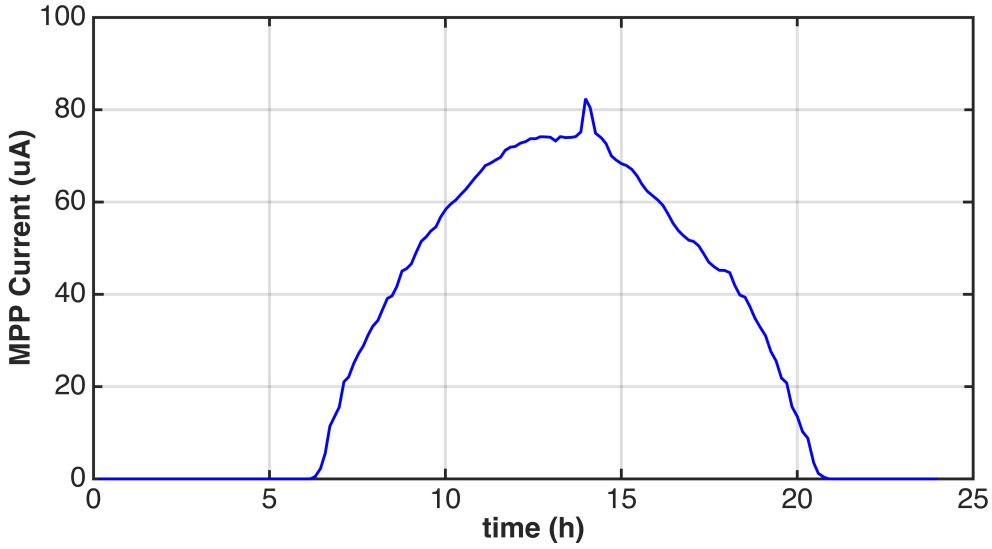


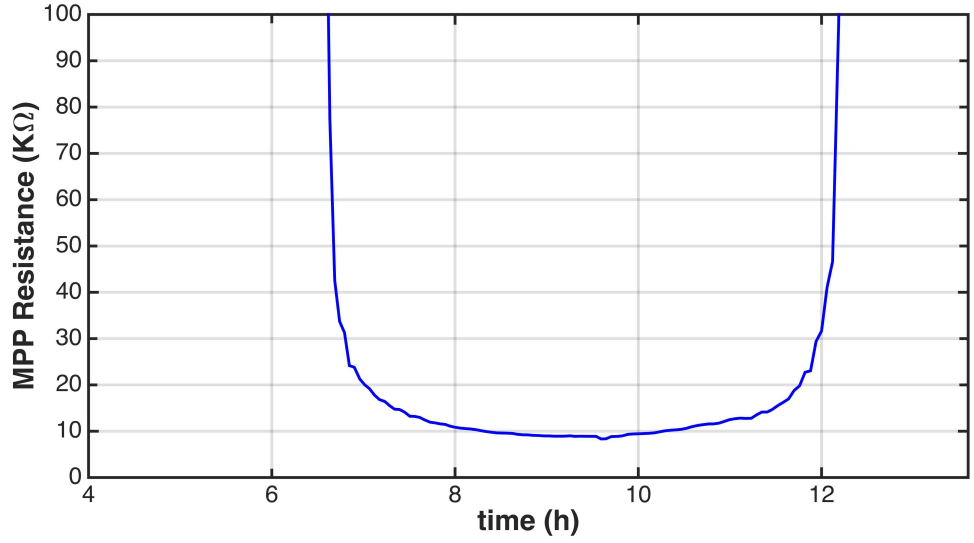
Figure B.27: PV data for the IXYS SLMD121H04L on 24th of May of 2015. Test made on location B.



(a)



(b)



(c)

Figure B.28: Maximum power point coordinates for the IXYS SLMD121H04L on 24th of May of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

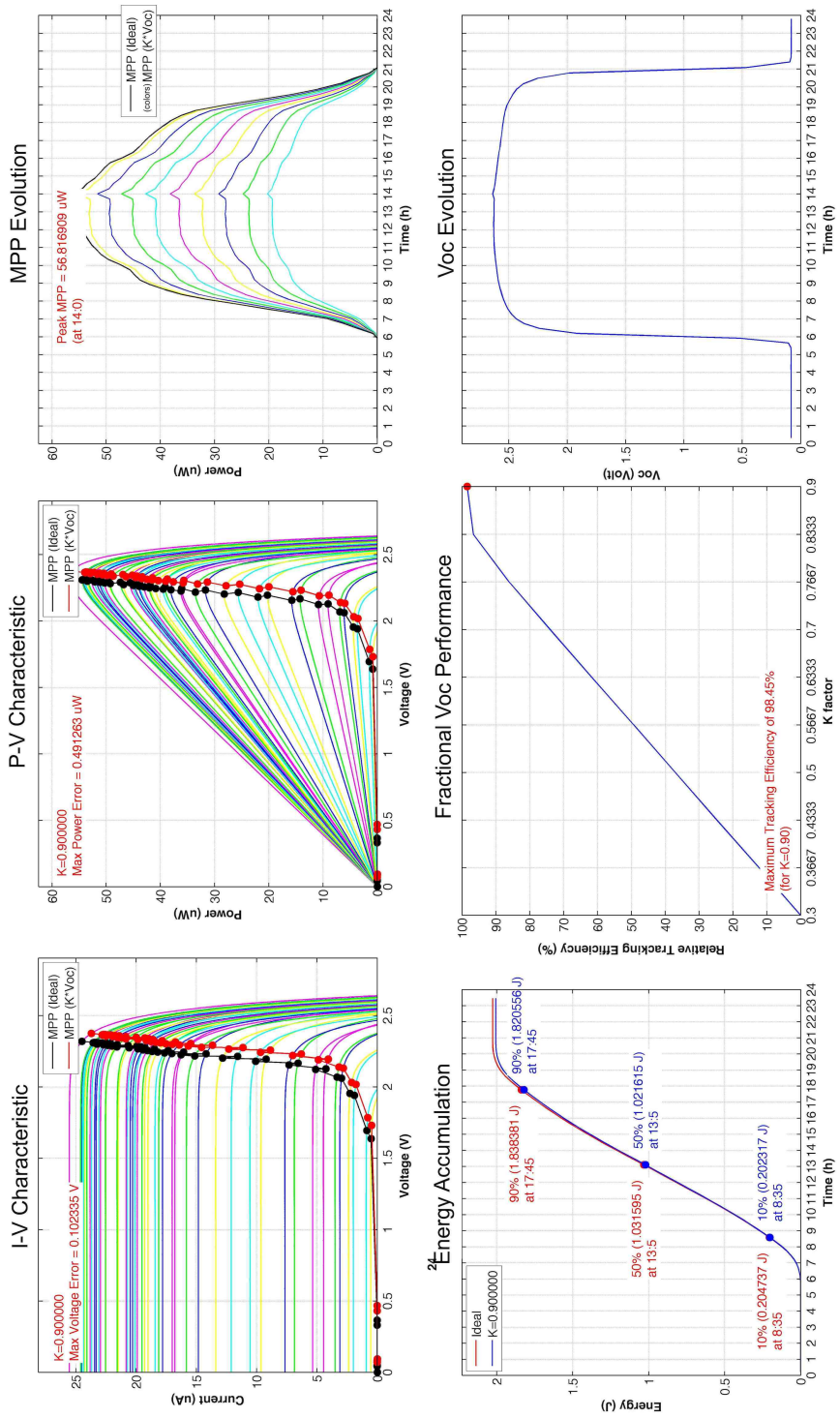
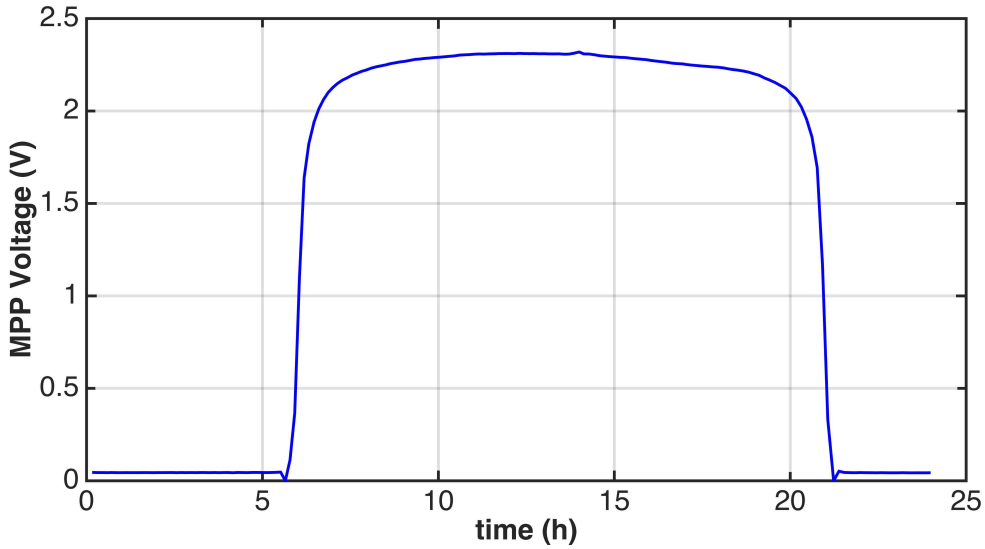
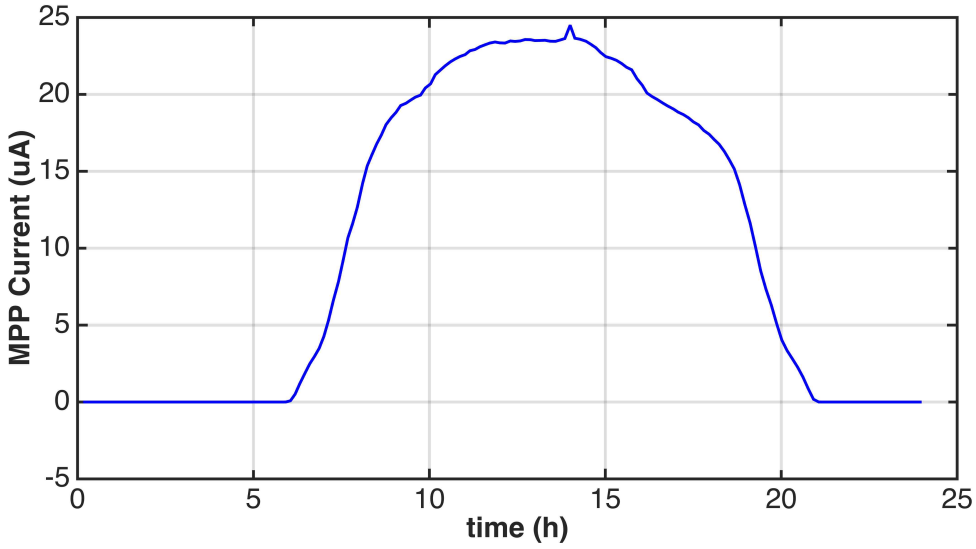


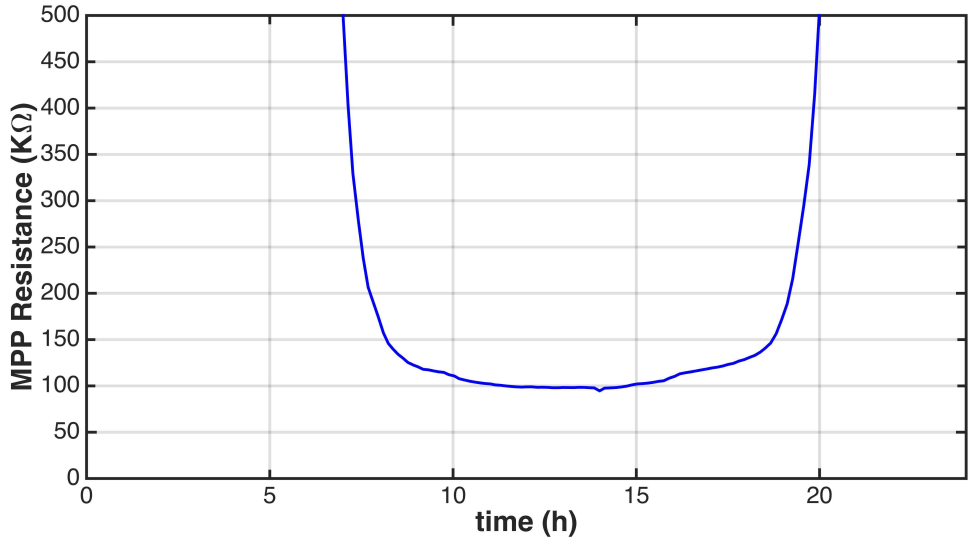
Figure B.29: PV data for the CYMBET CBC-PV-01N on 24th of May of 2015. Test made on location B.



(a)



(b)



(c)

Figure B.30: Maximum power point coordinates for the CYMBET CBC-PV-01N on 24th of May of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

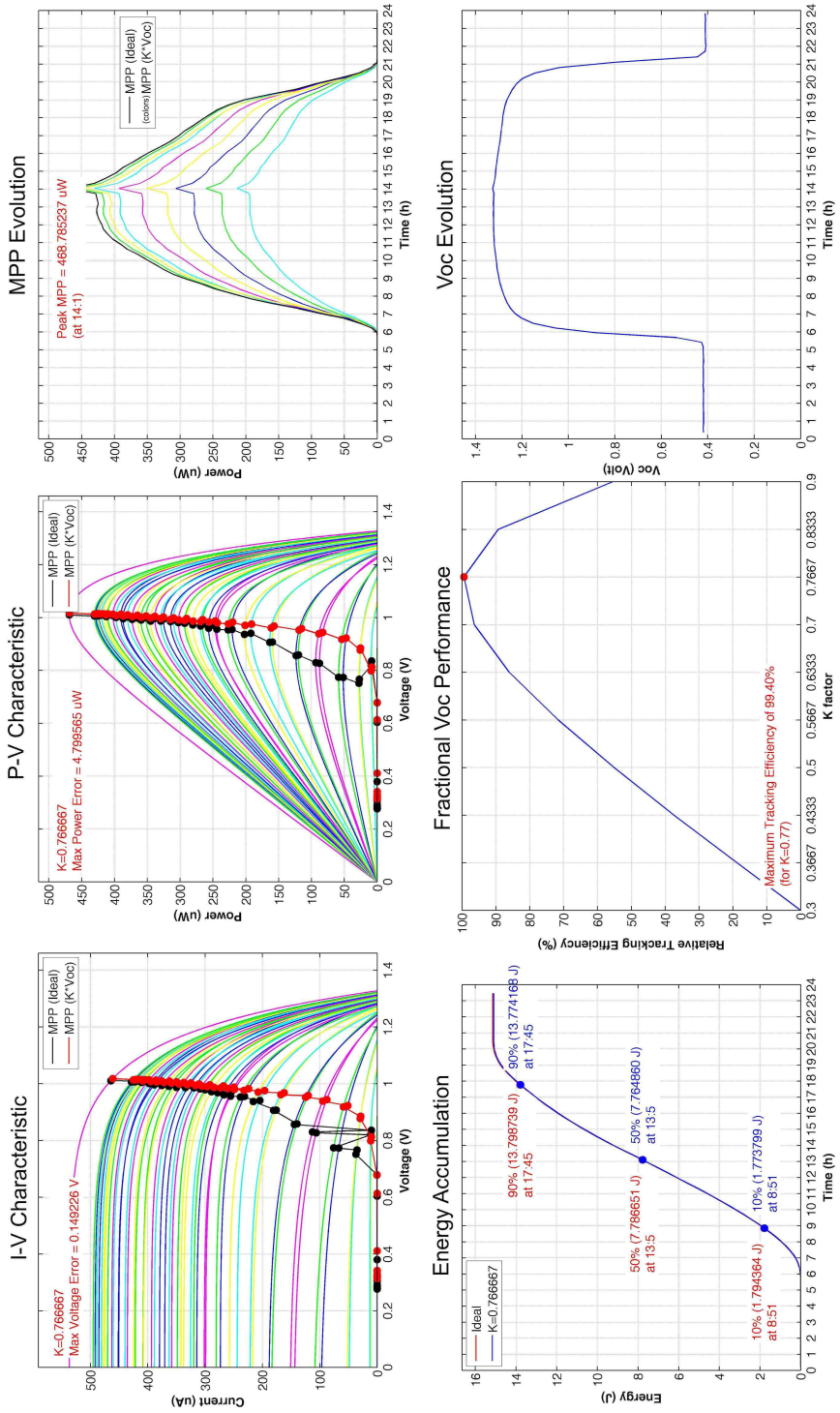
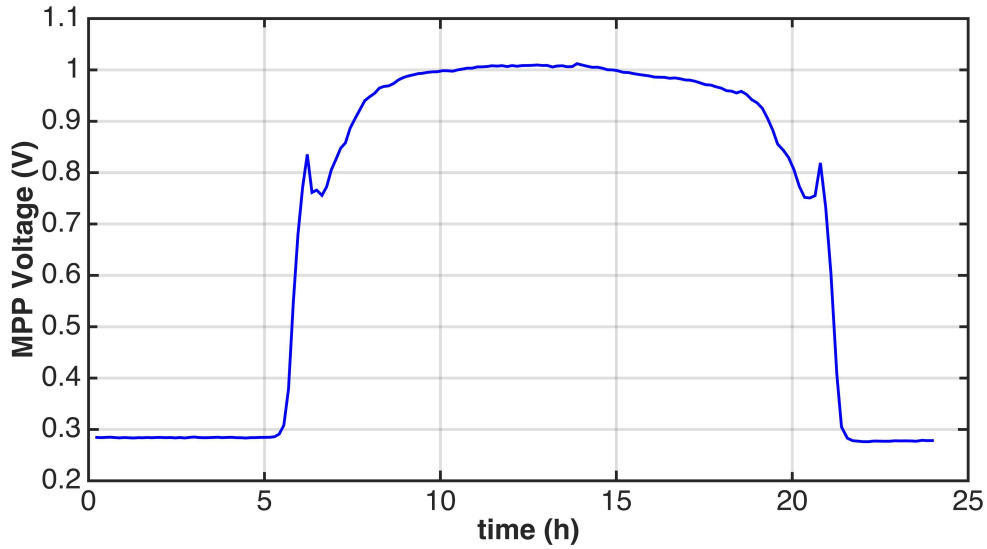
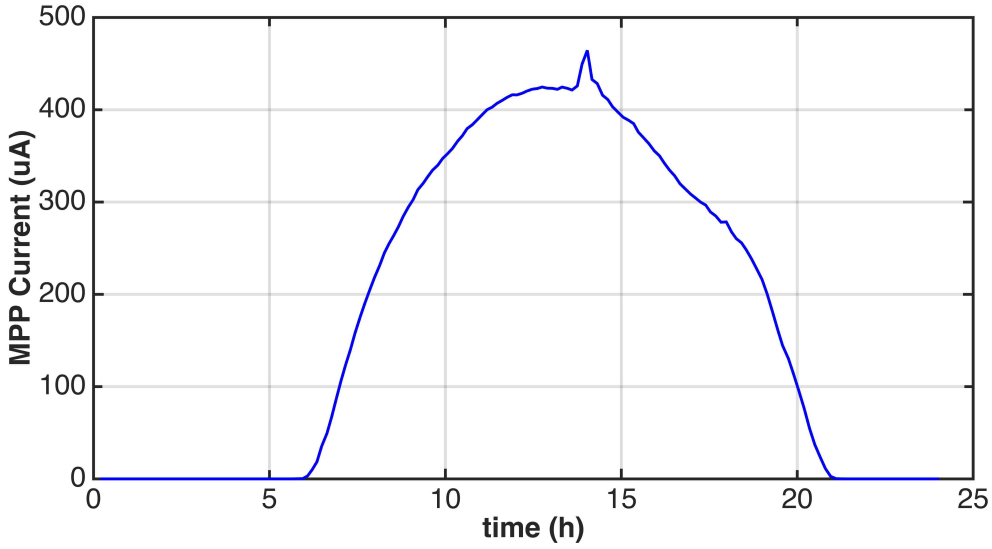


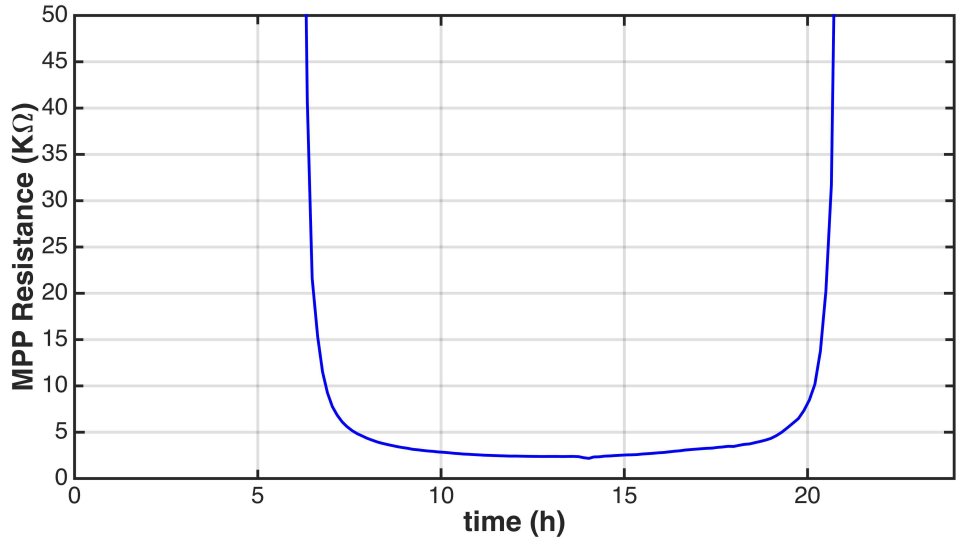
Figure B.31: PV data for the Amorton AM-1454 on 24th of May of 2015. Test made on location B.



(a)



(b)



(c)

Figure B.32: Maximum power point coordinates for the Amorton AM-1454 CA on 24th of May of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

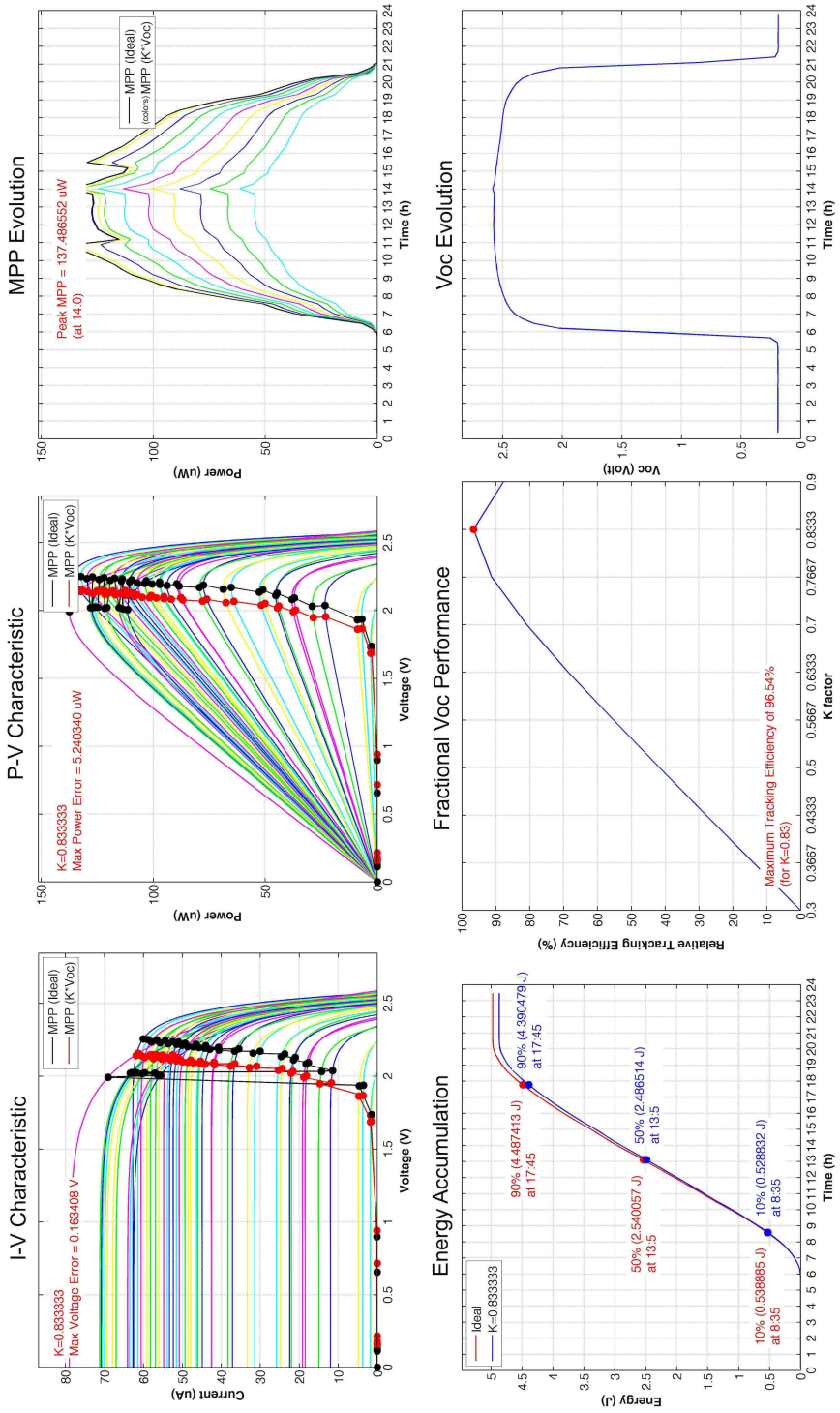
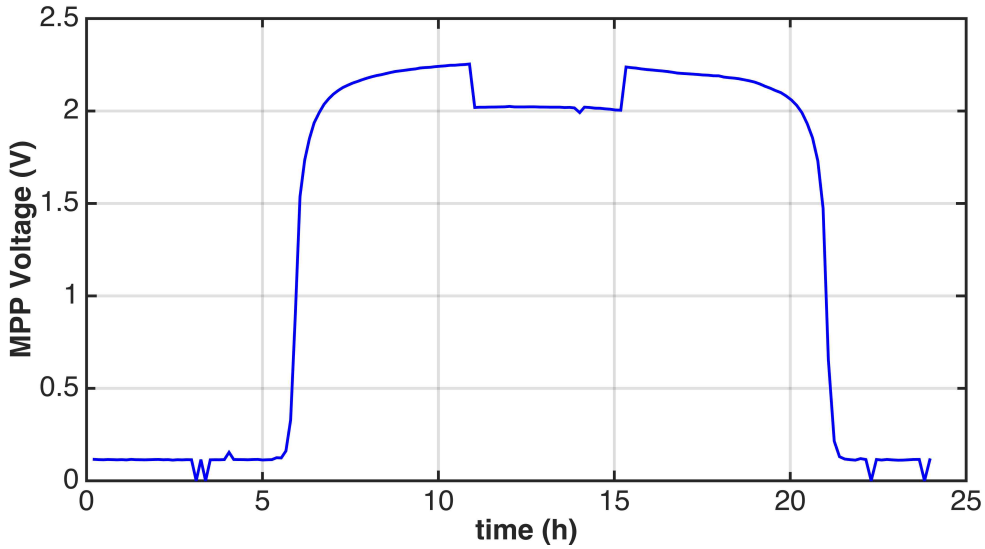
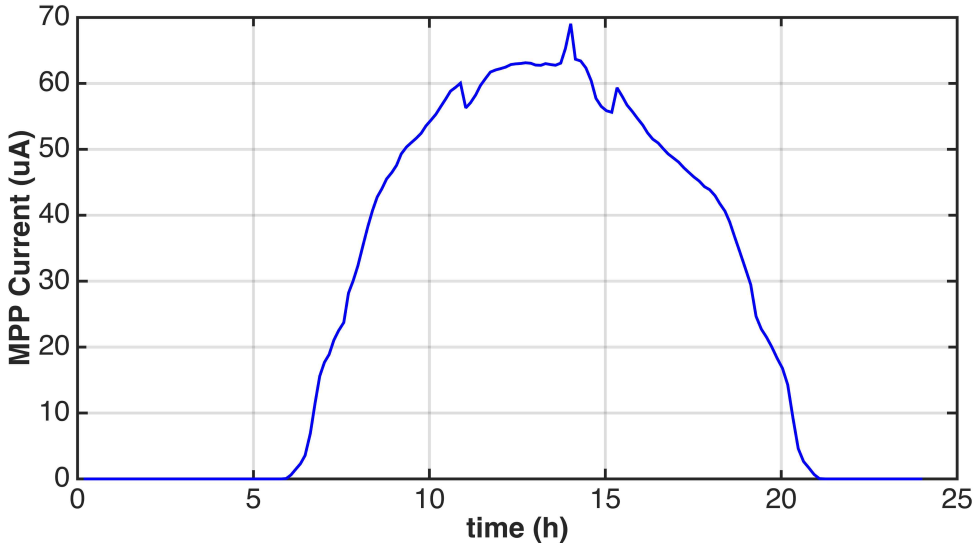


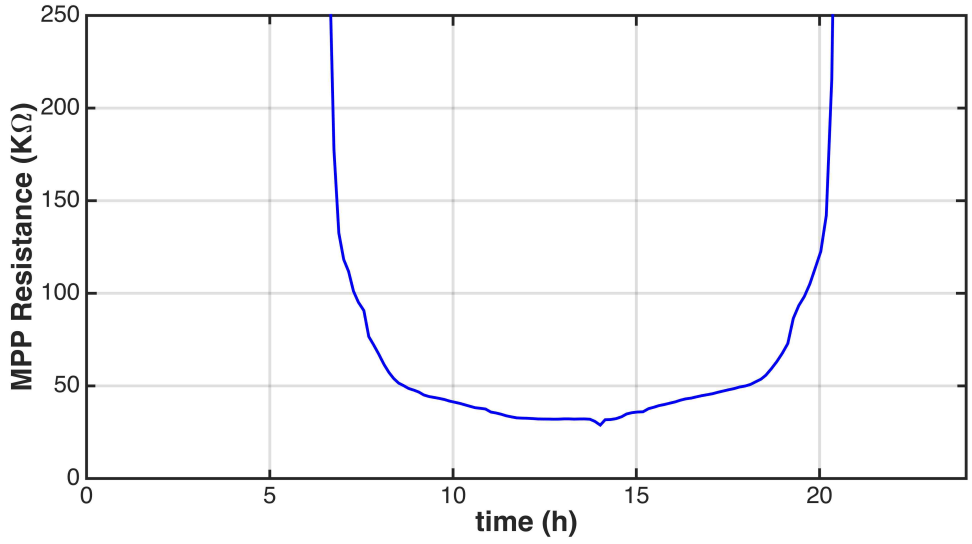
Figure B.33: PV data for the Amorton AM-1417 on 24th of May of 2015. Test made on location B.



(a)



(b)



(c)

Figure B.34: Maximum power point coordinates for the Amorton AM-1417 CA on 24th of May of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

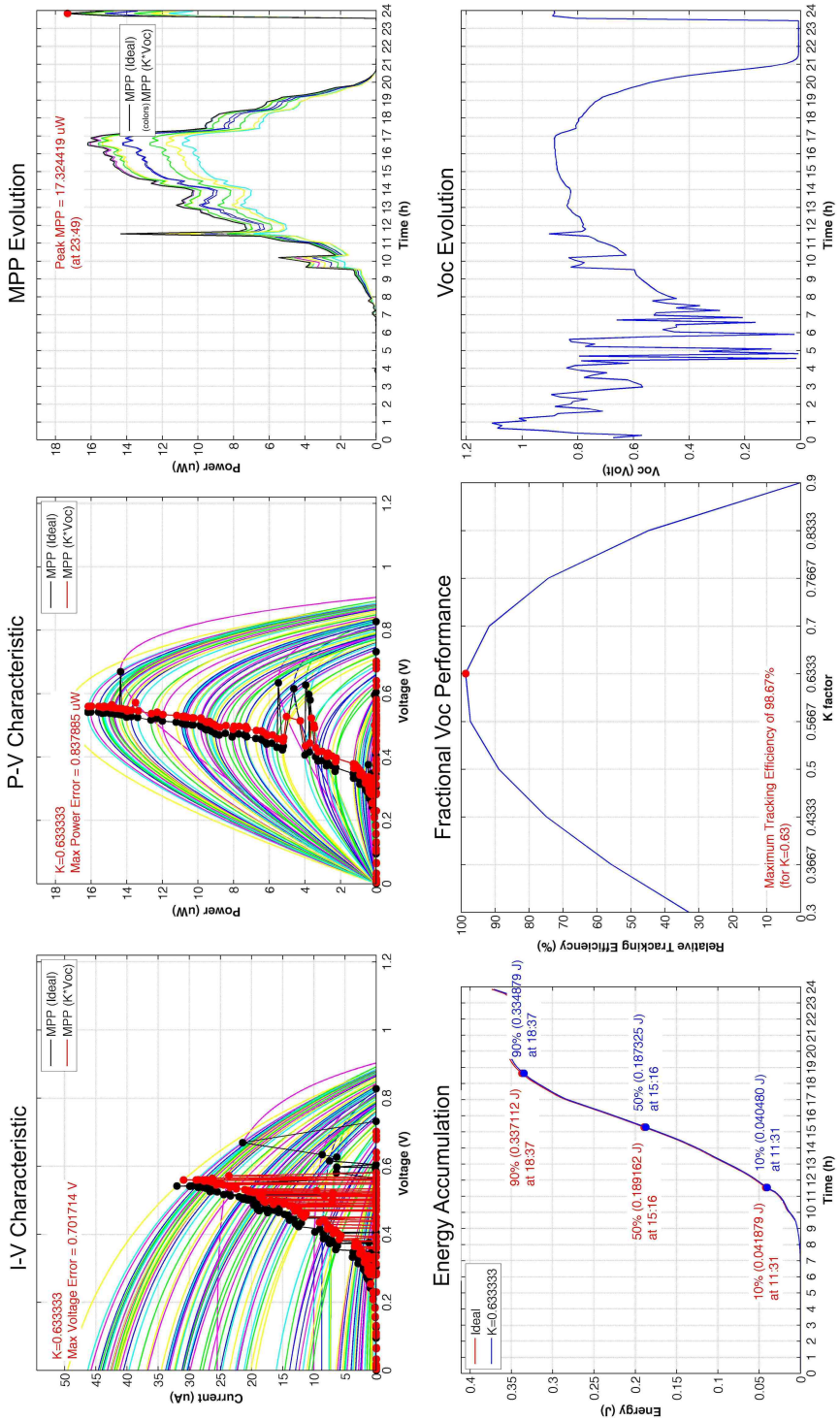
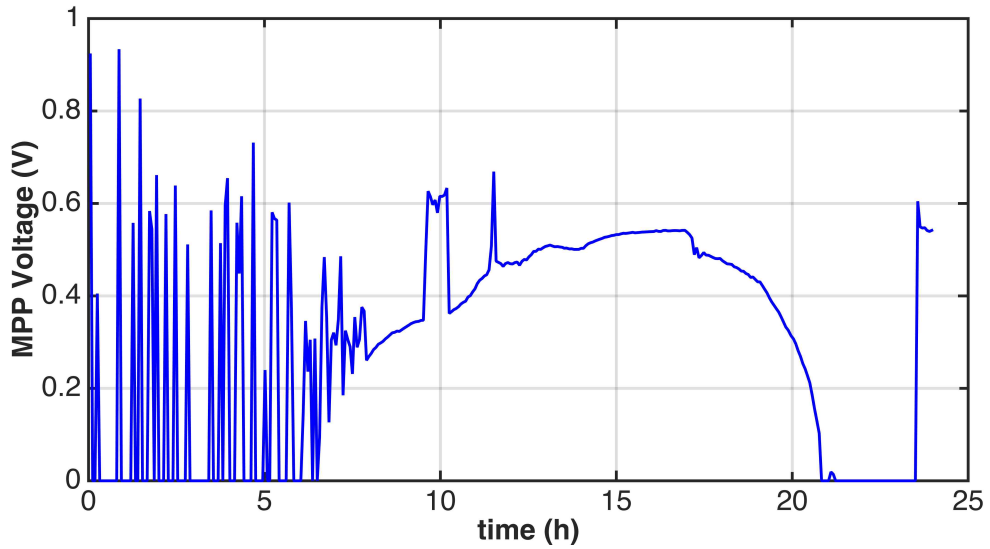
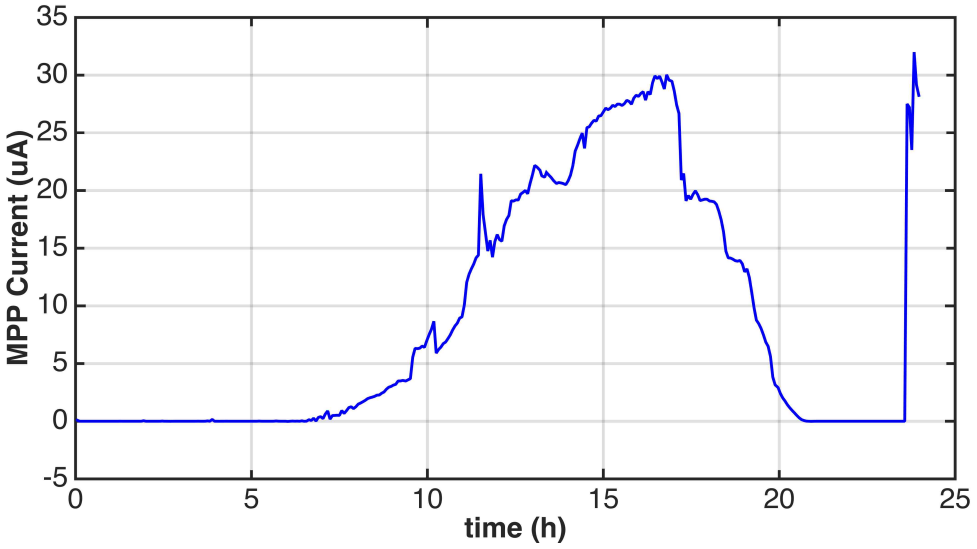


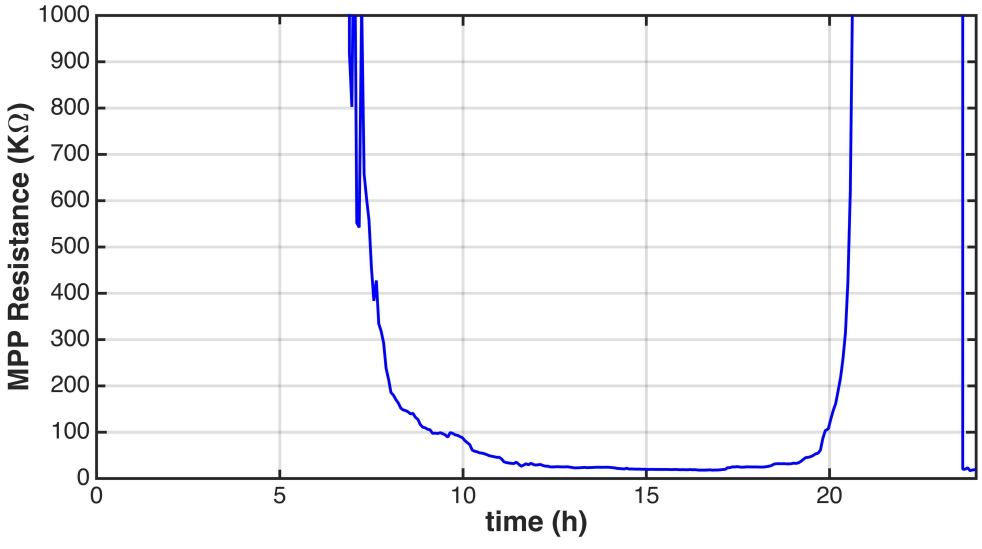
Figure B.35: PV data for the IXYS SLMD121H04L on 6th of June of 2015. Test made on location C.



(a)



(b)



(c)

Figure B.36: Maximum power point coordinates for the IXYS SLMD121H04L on 6th of June of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

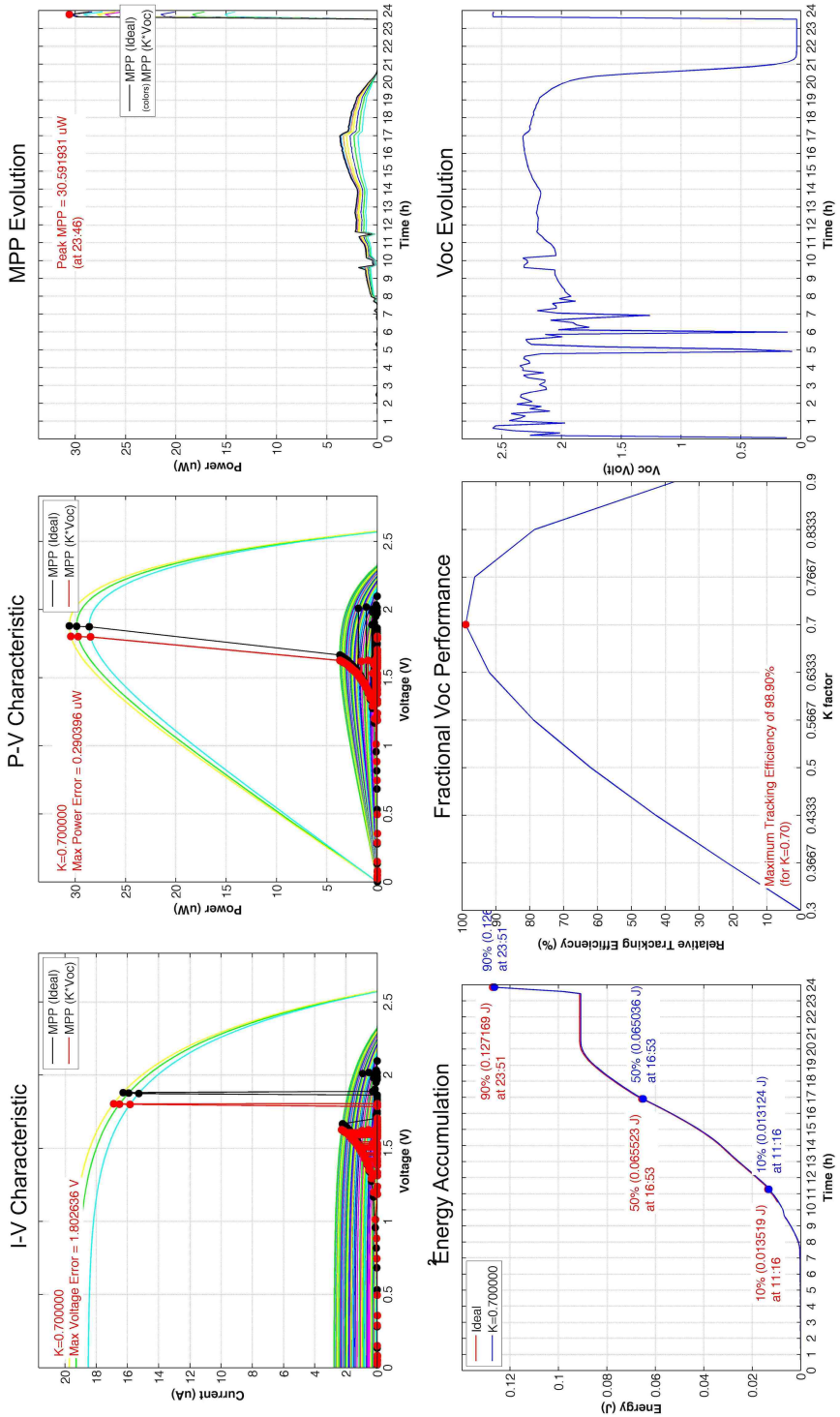
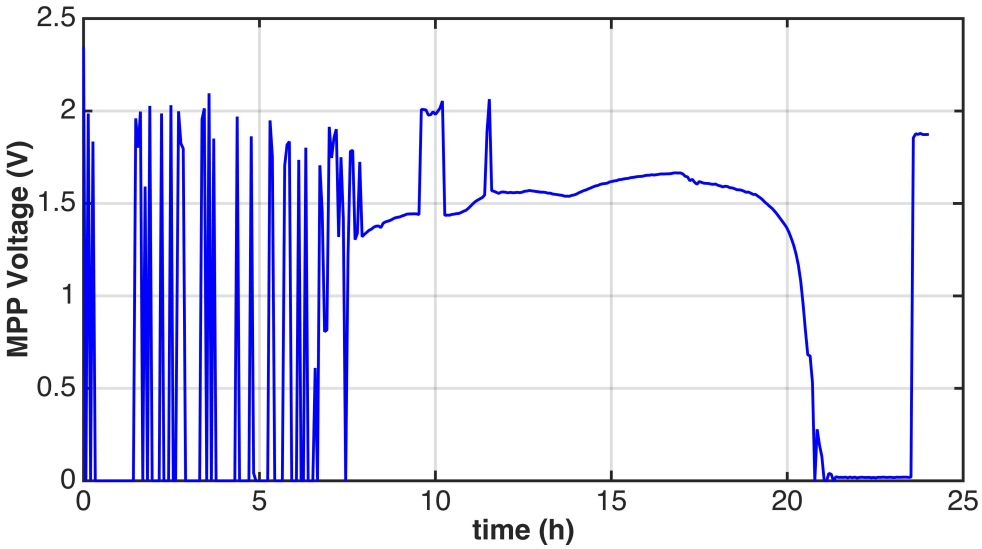
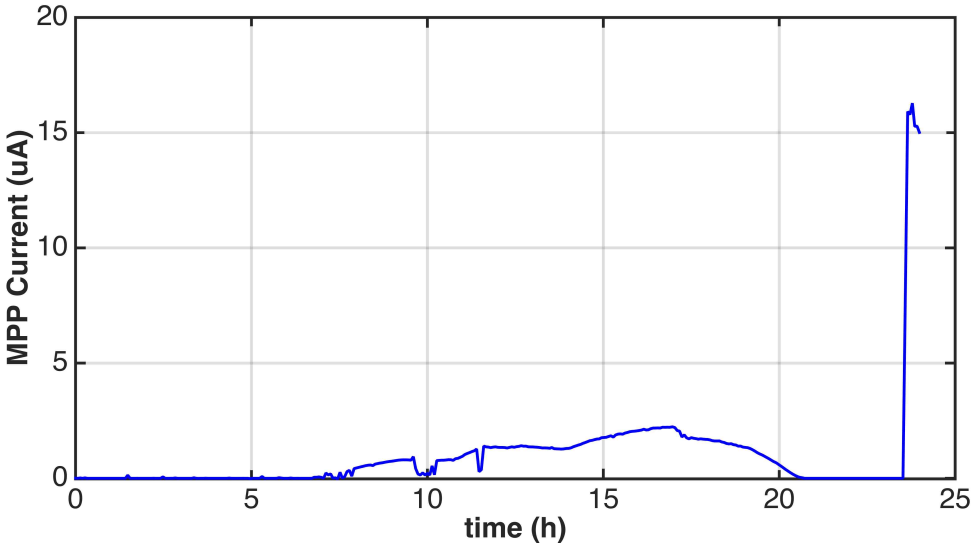


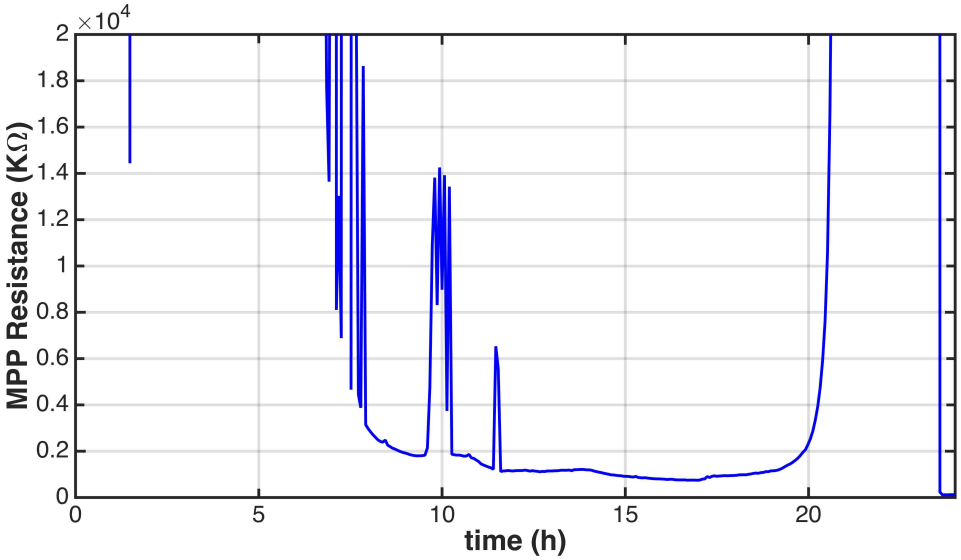
Figure B.37: PV data for the CYMBET CBC-PV-01N on 6th of June of 2015. Test made on location C.



(a)



(b)



(c)

Figure B.38: Maximum power point coordinates for the CYMBET CBC-PV-01N on 6th of June of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

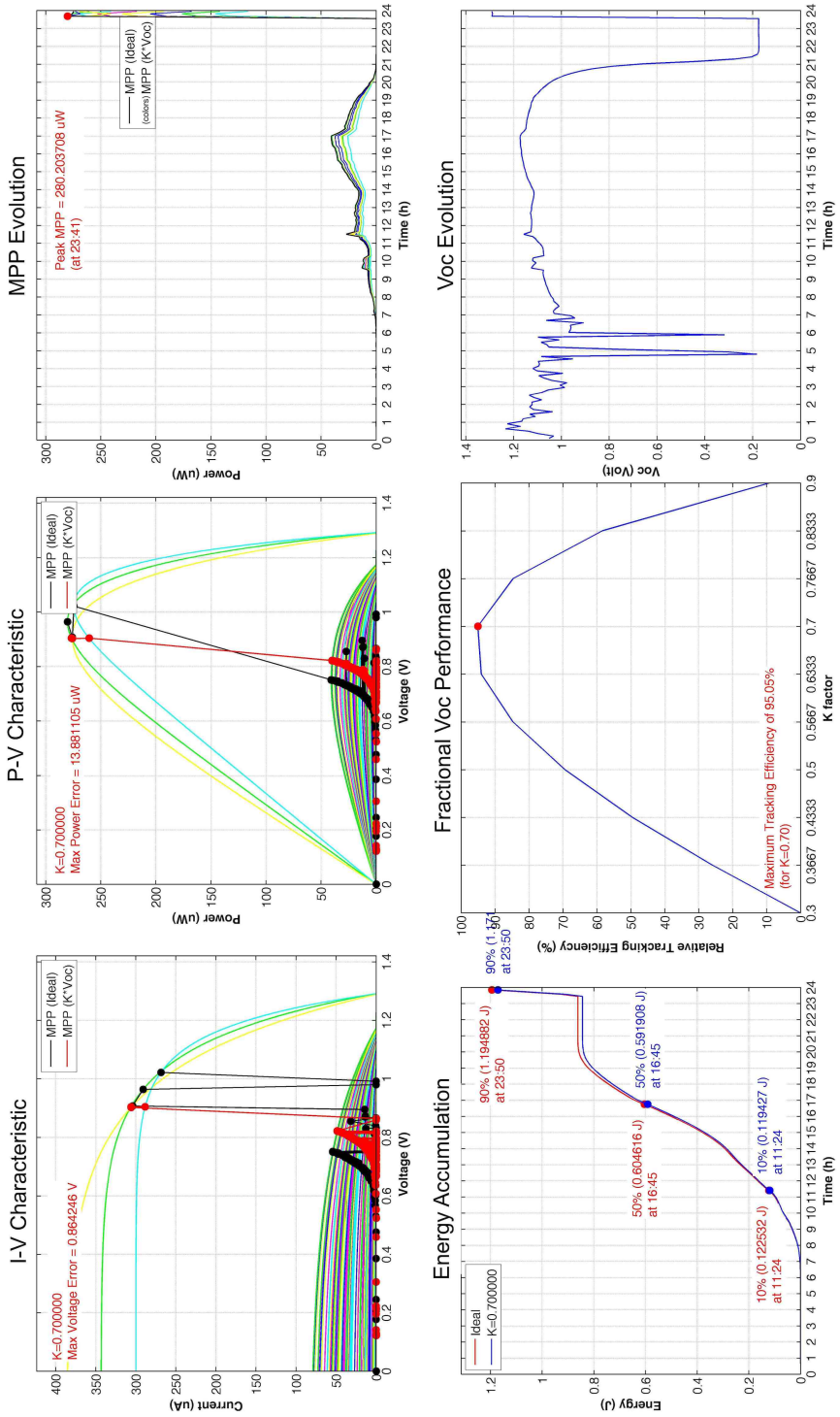
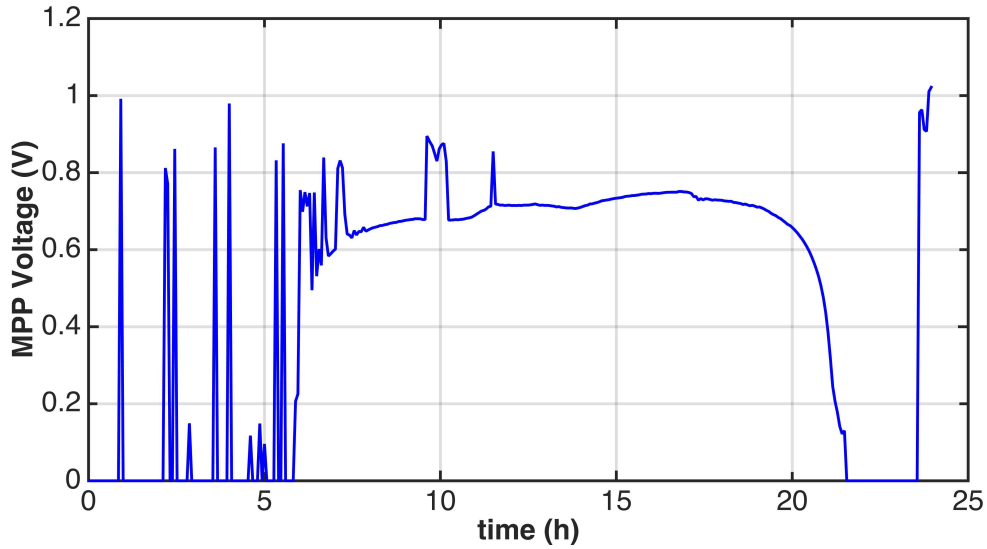
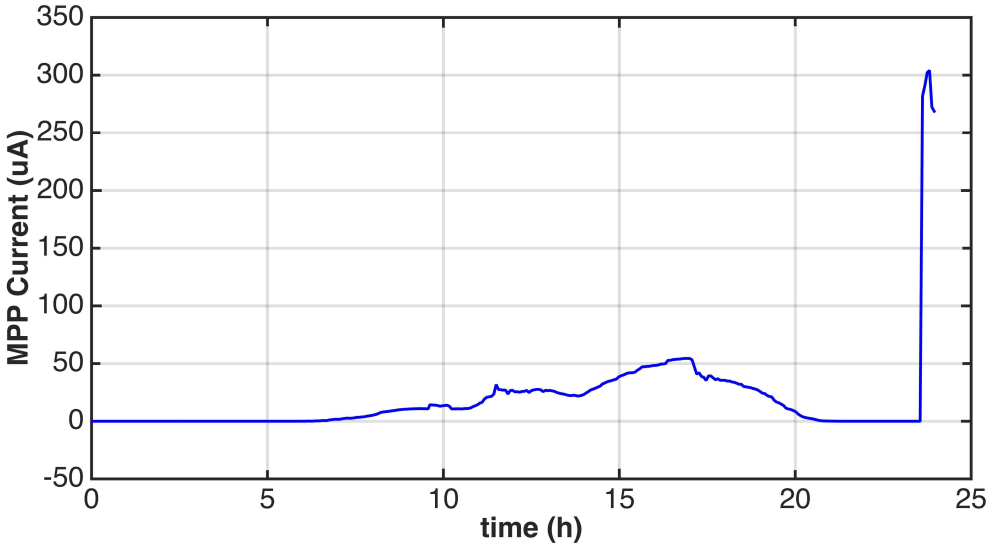


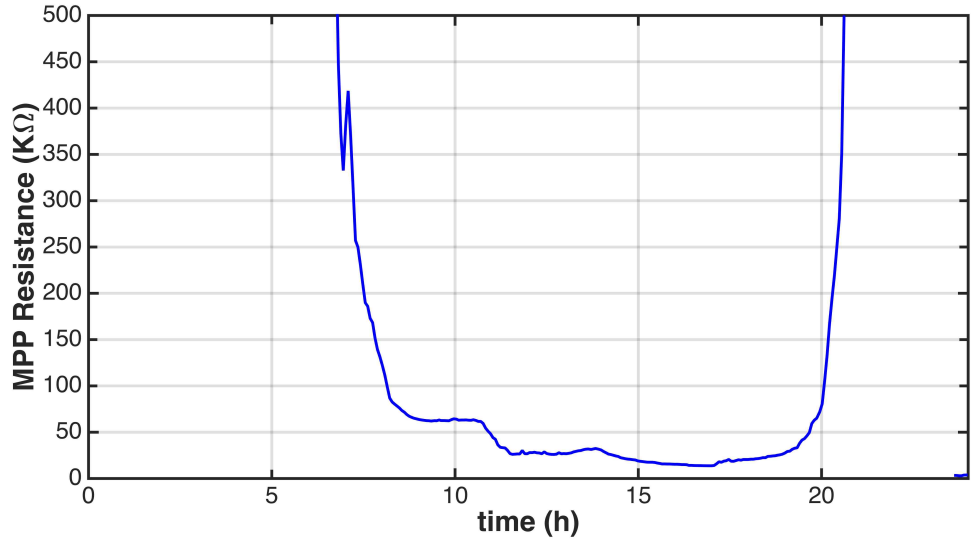
Figure B.39: PV data for the Amorton AM-1454 on 6th of June of 2015. Test made on location C.



(a)



(b)



(c)

Figure B.40: Maximum power point coordinates for the Amorton AM-1454 CA on 6th of June of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

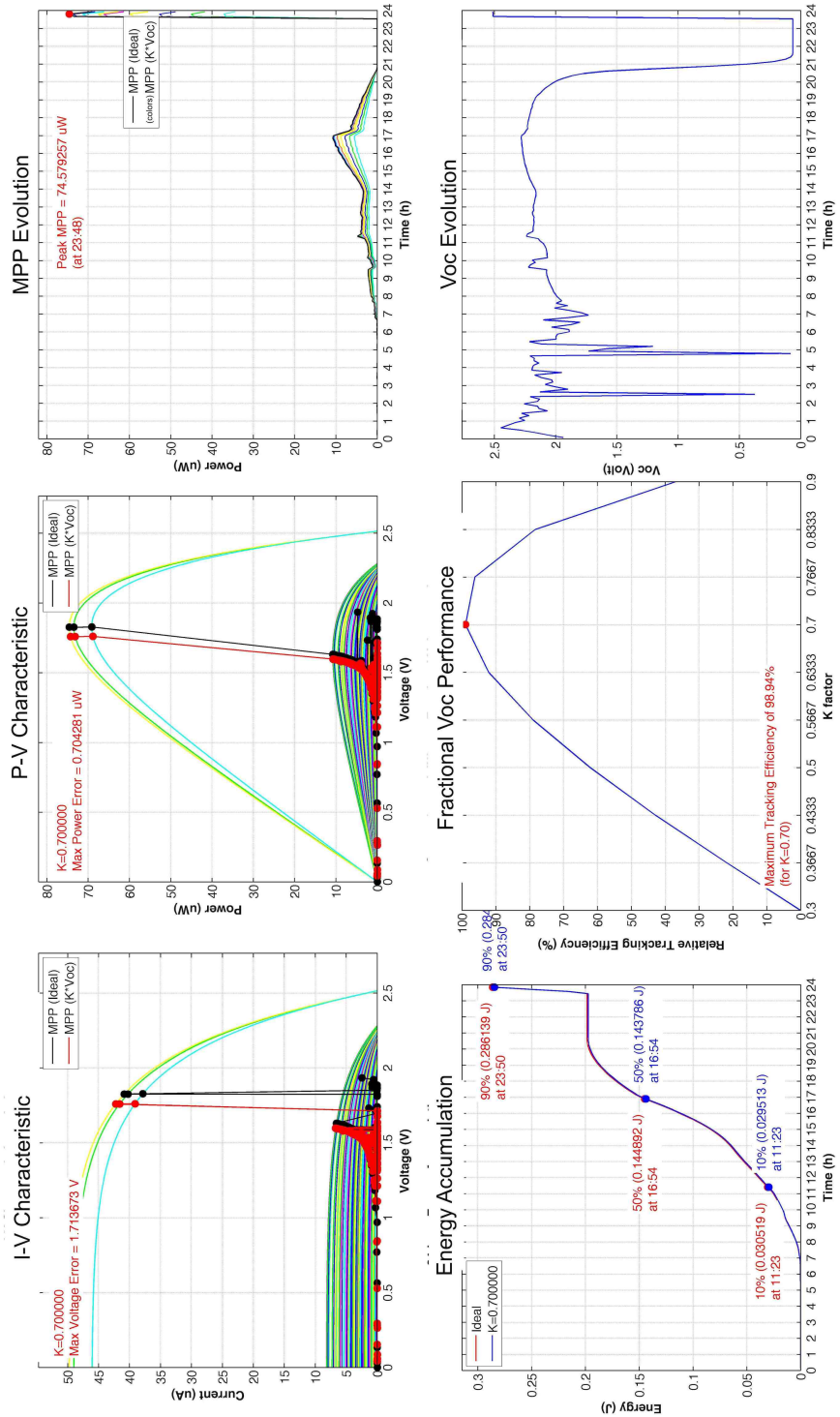
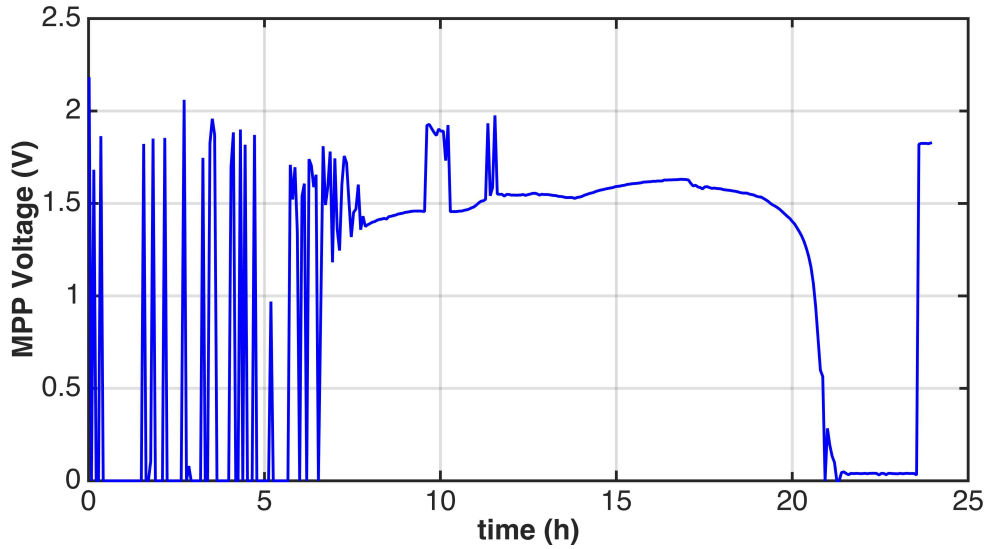
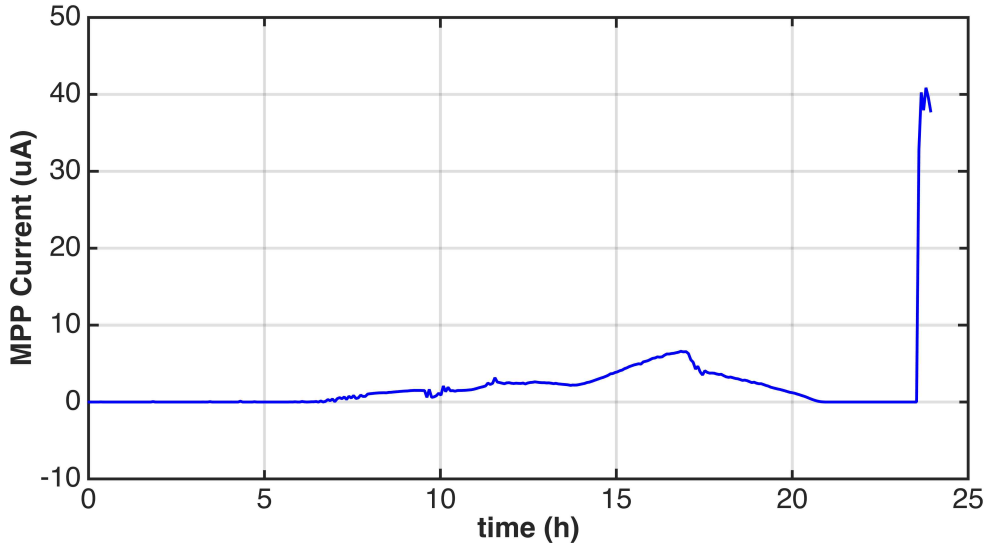


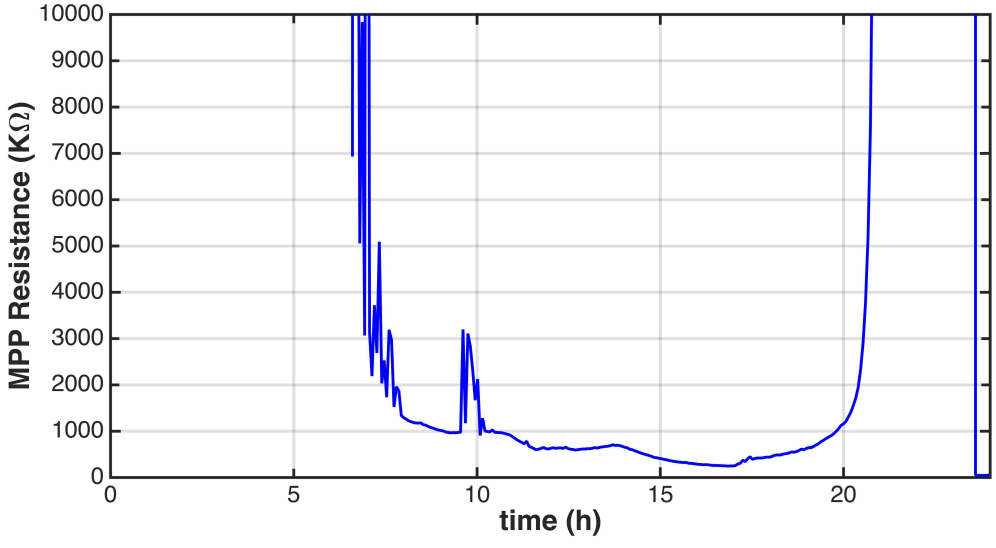
Figure B.41: PV data for the Amorton AM-1417 on 6th of June of 2015. Test made on location C.



(a)



(b)



(c)

Figure B.42: Maximum power point coordinates for the Amorton AM-1417 CA on 6th of June of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

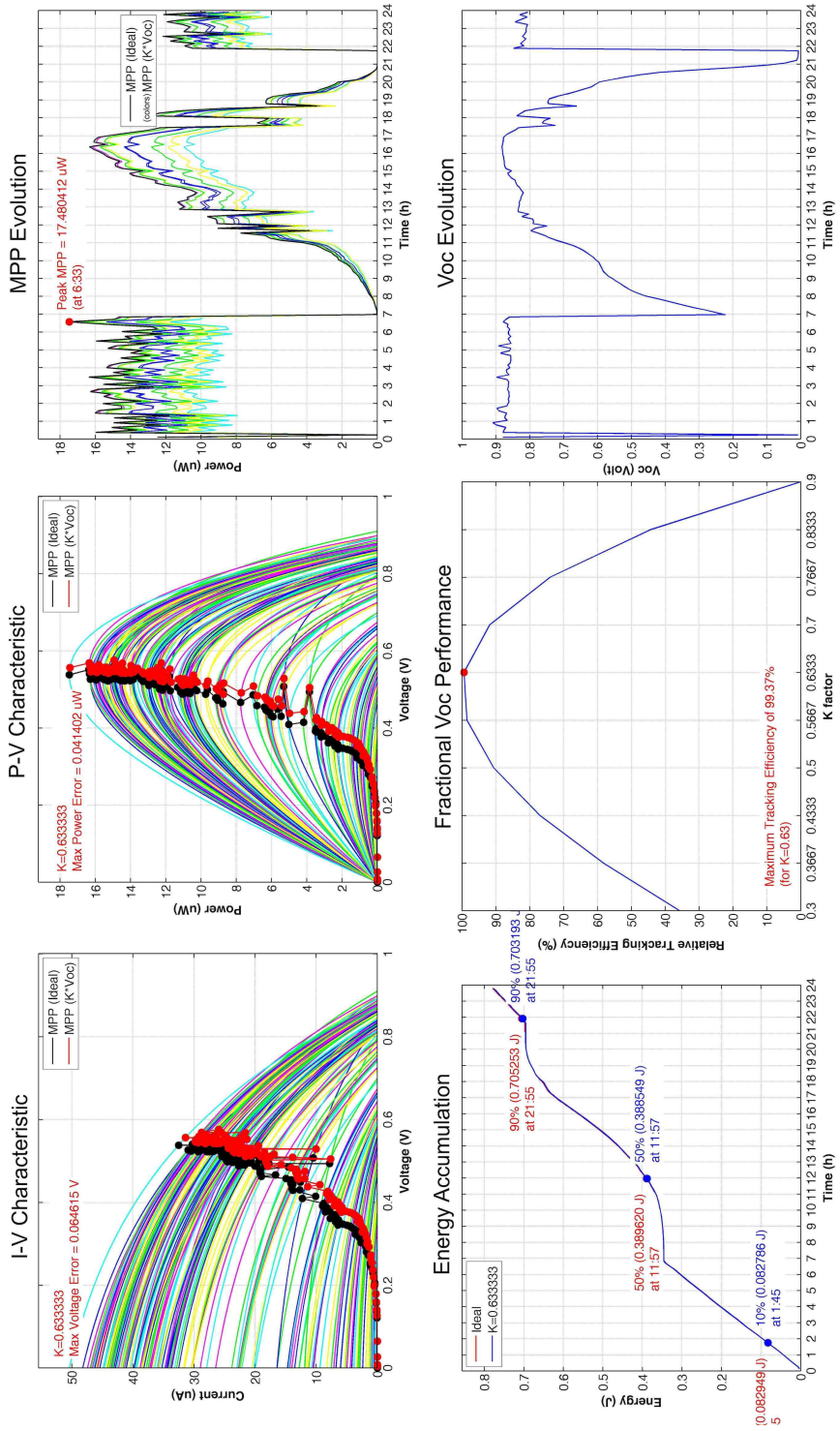
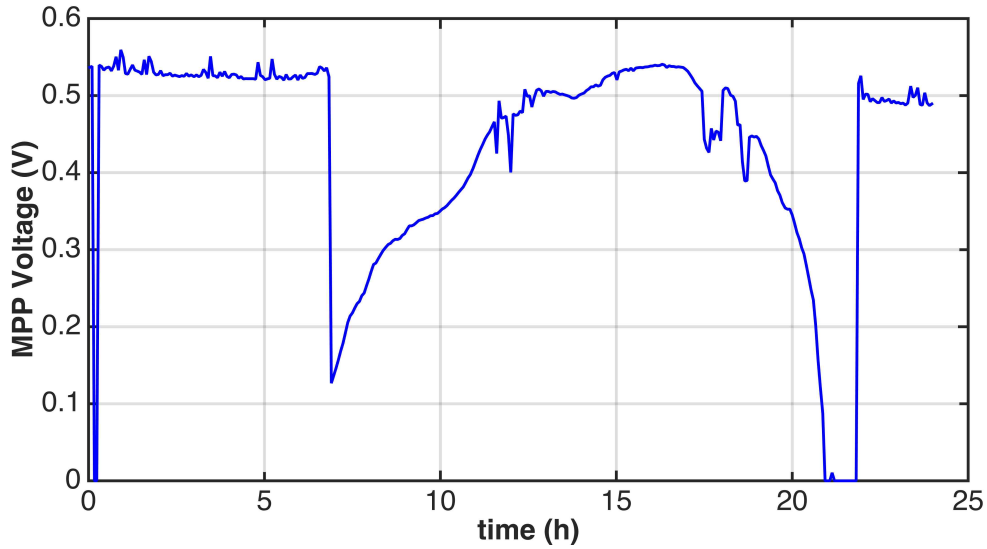
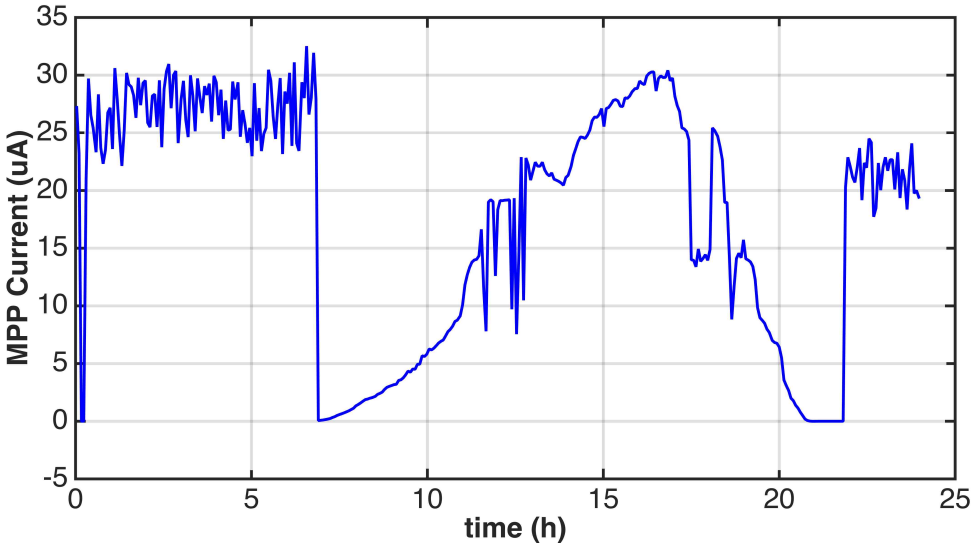


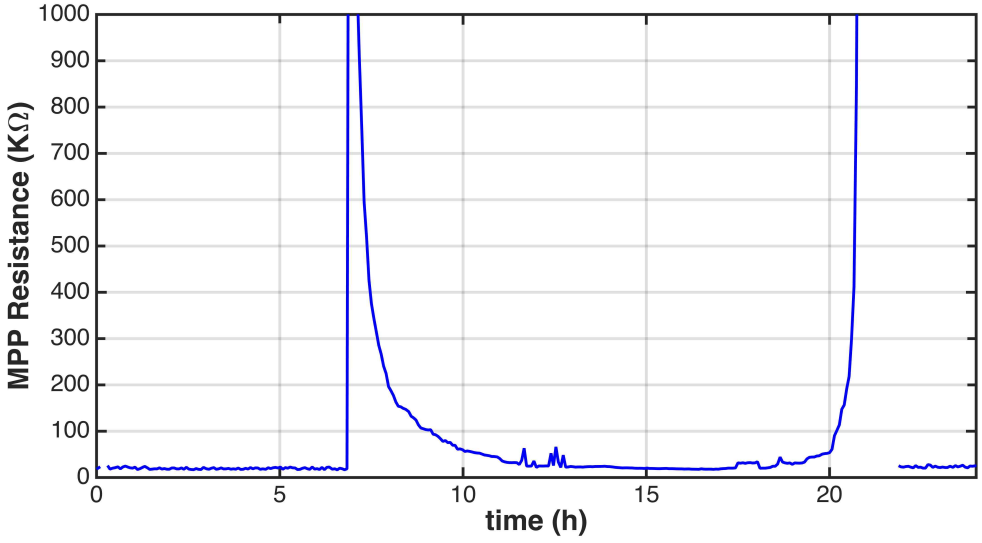
Figure B.43: PV data for the IXYS SLMD121H04L on 7th of June of 2015. Test made on location C.



(a)



(b)



(c)

Figure B.44: Maximum power point coordinates for the IXYS SLMD121H04L on 7th of June of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

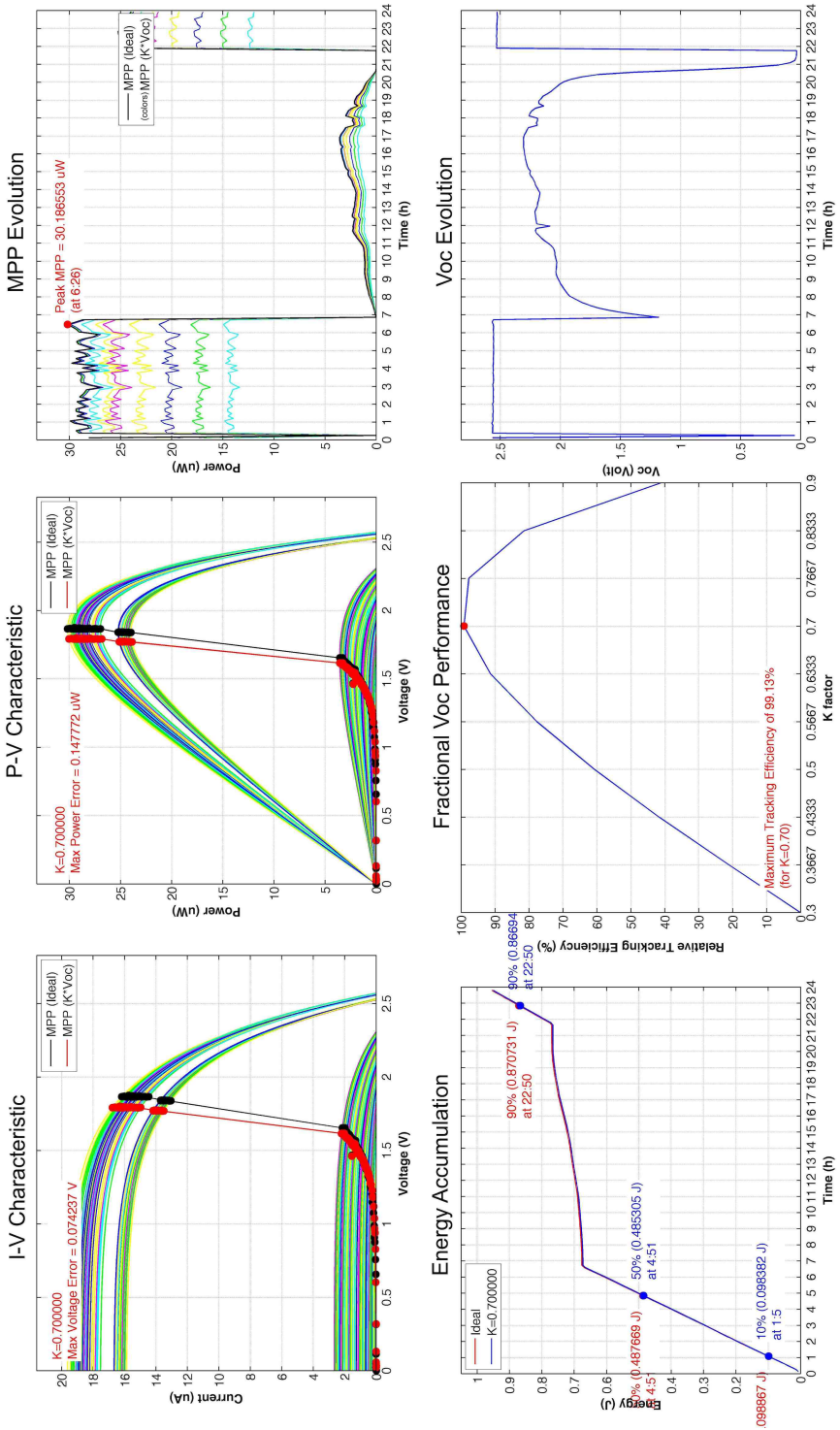
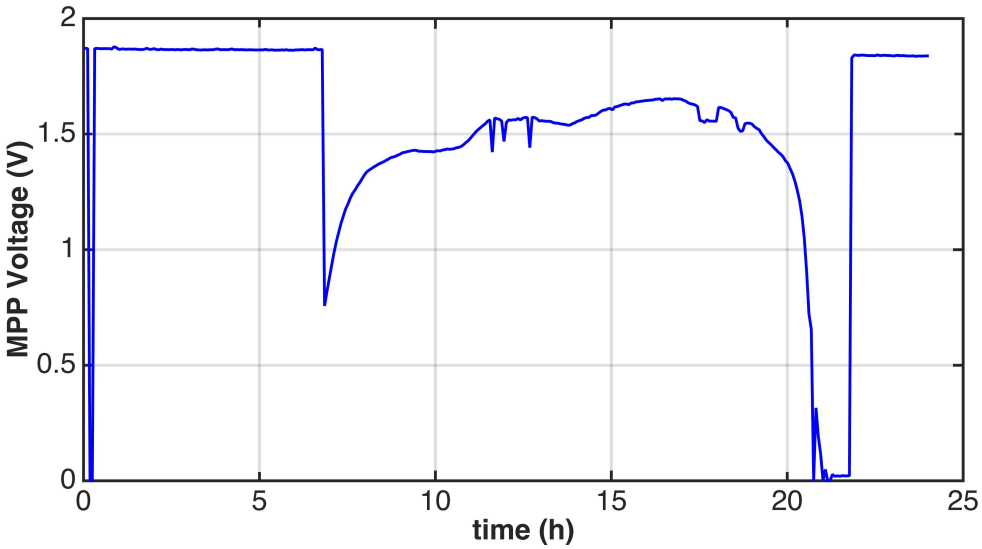
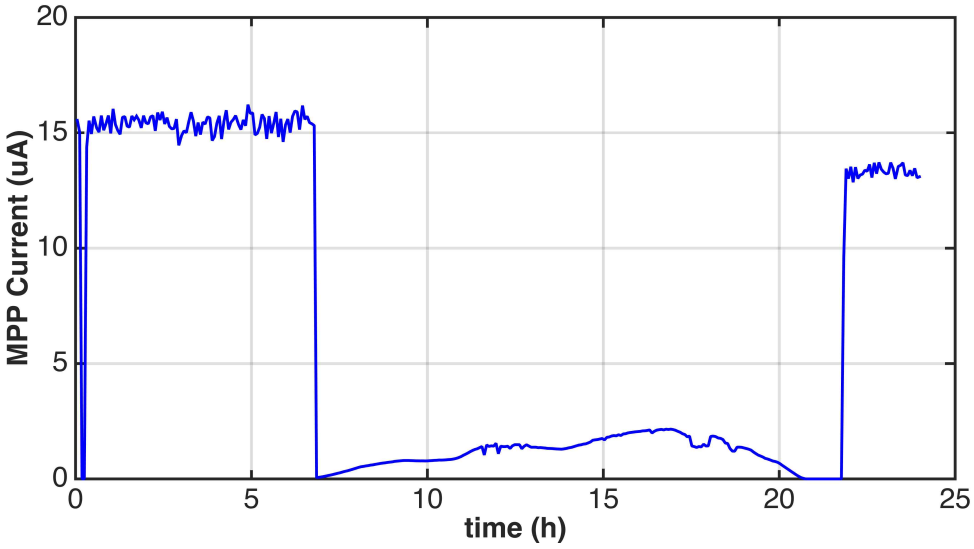


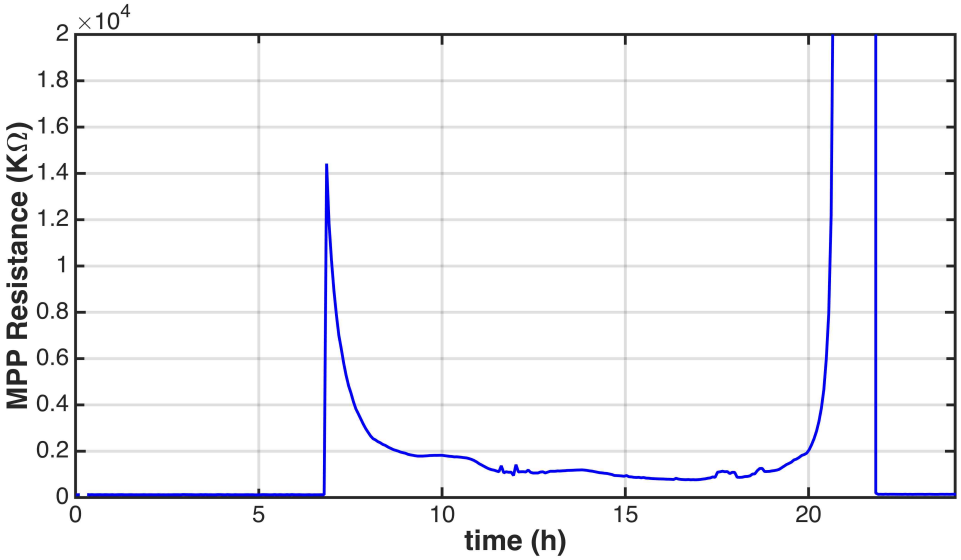
Figure B.45: PV data for the CYMBET CBC-PV-01N on 7th of June of 2015. Test made on location C.



(a)



(b)



(c)

Figure B.46: Maximum power point coordinates for the CYMBET CBC-PV-01N on 7th of June of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

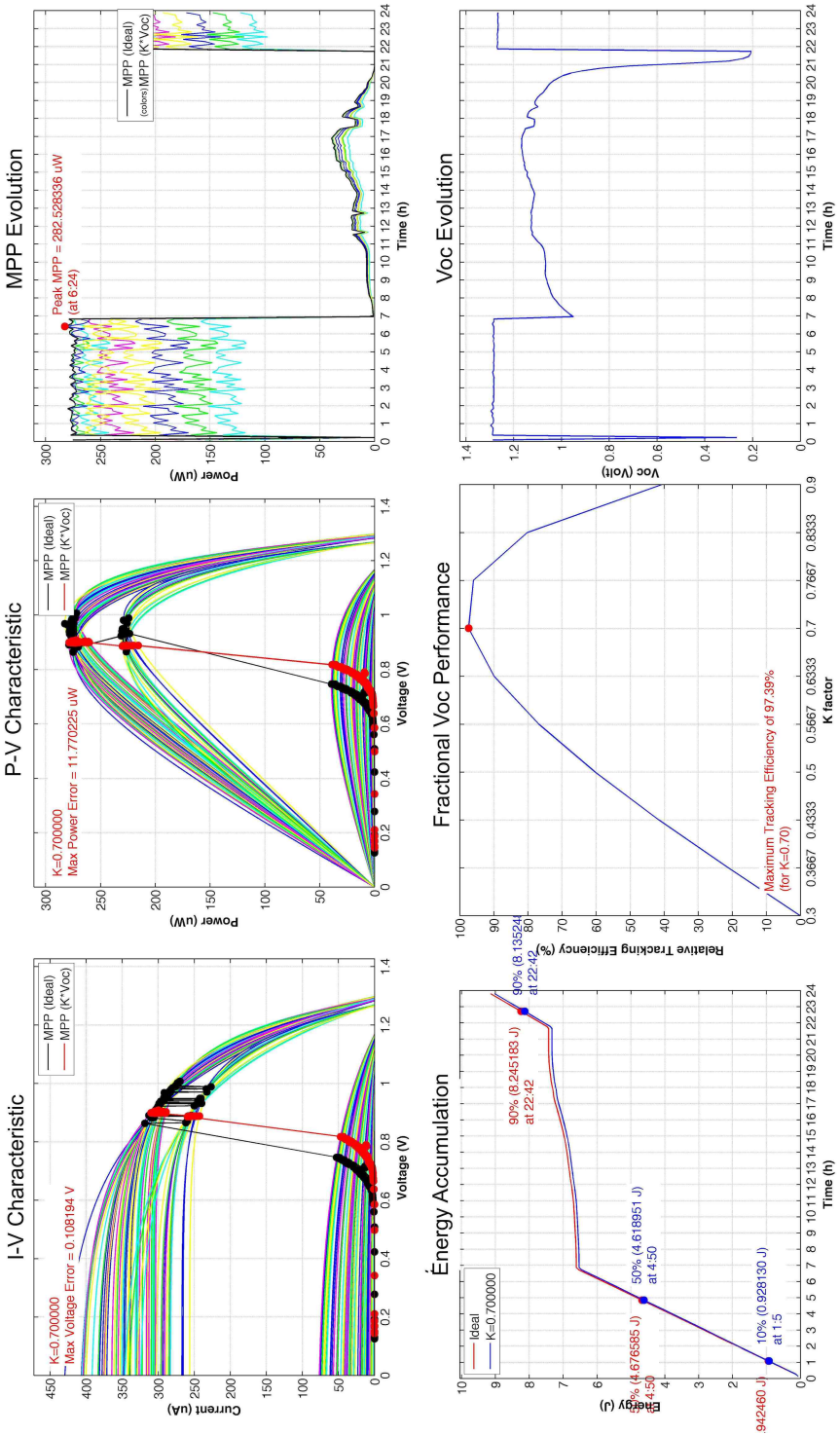
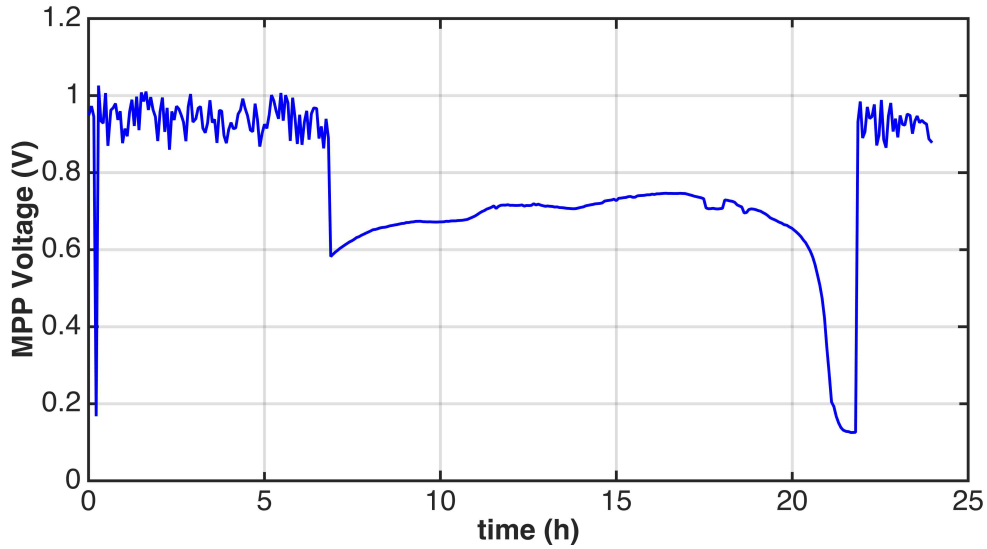
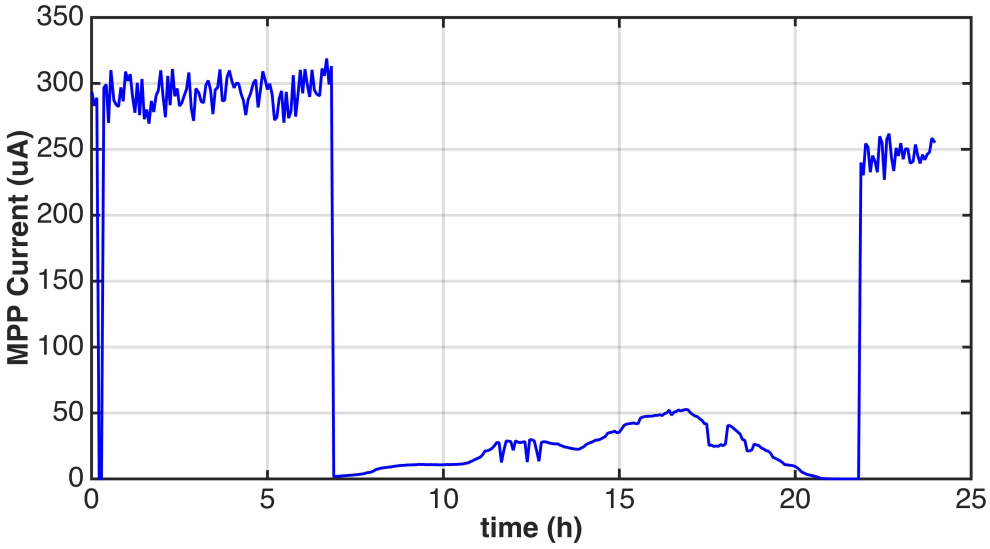


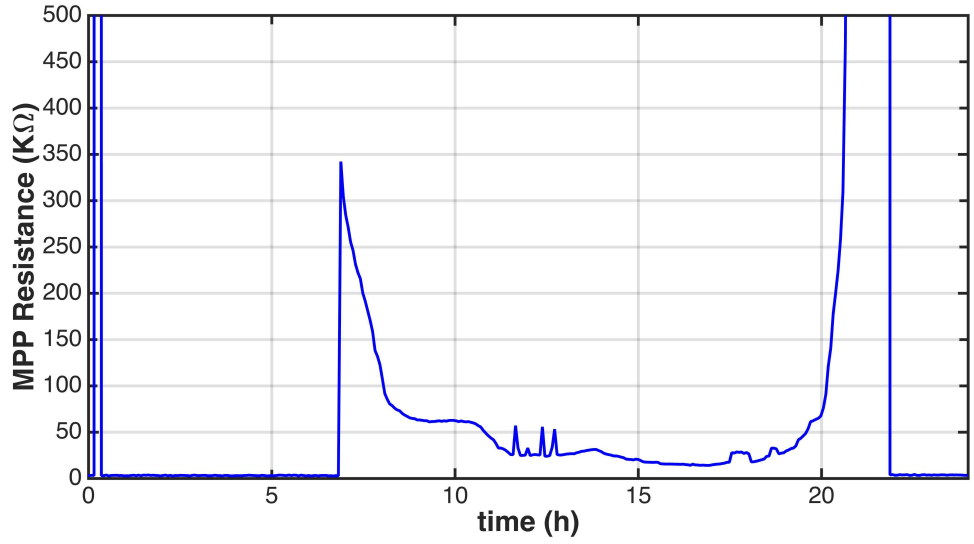
Figure B.47: PV data for the Amorton AM-1454 on 7th of June of 2015. Test made on location C.



(a)



(b)



(c)

Figure B.48: Maximum power point coordinates for the Amorton AM-1454 CA on 7th of June of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

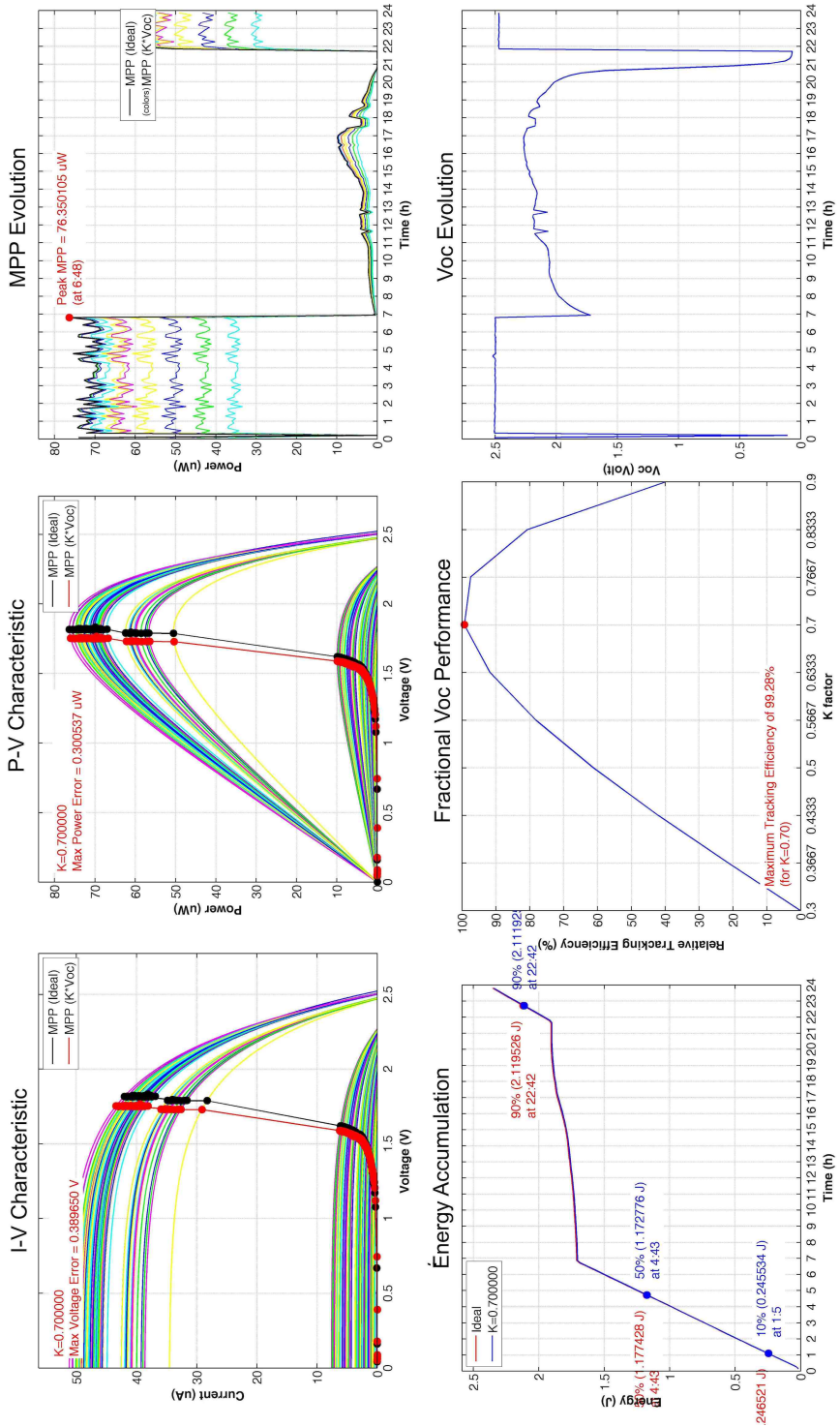
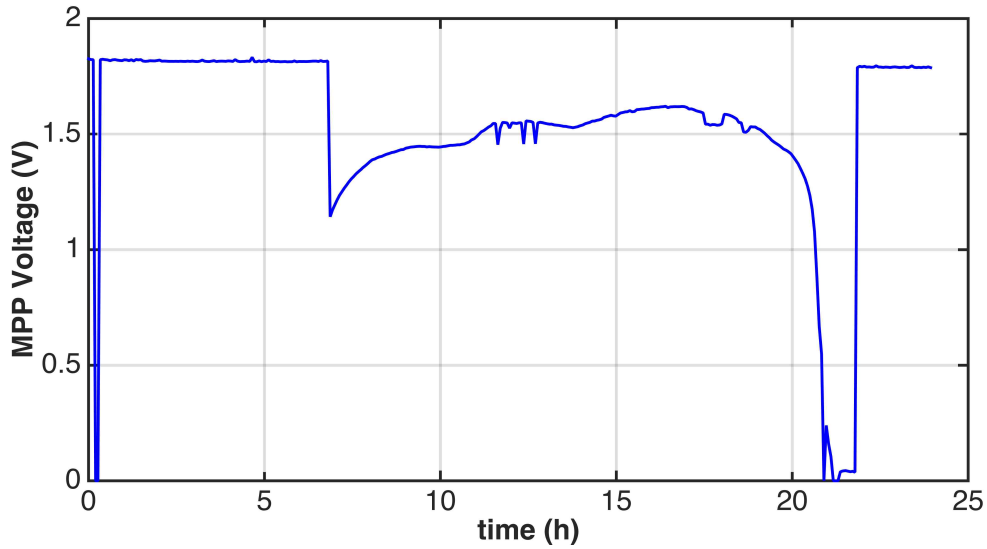
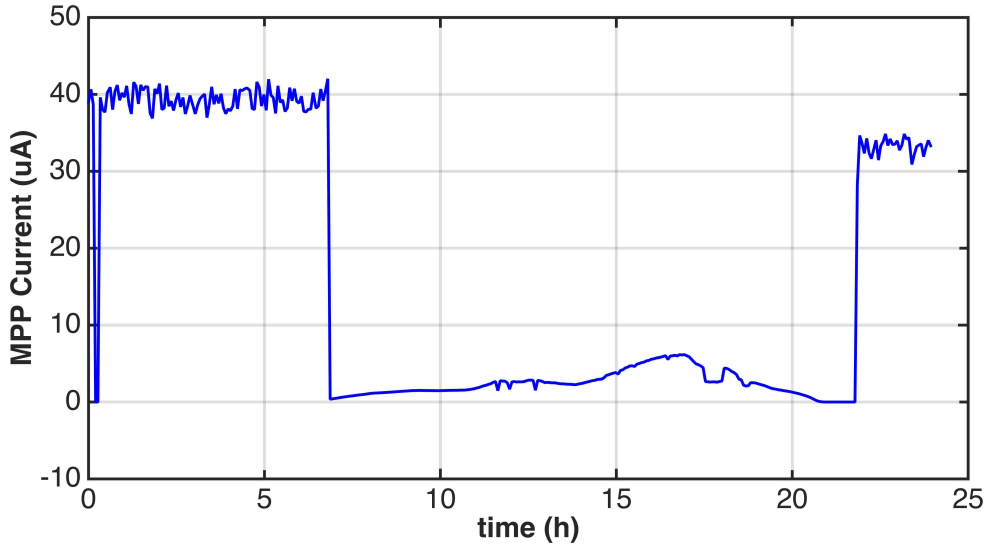


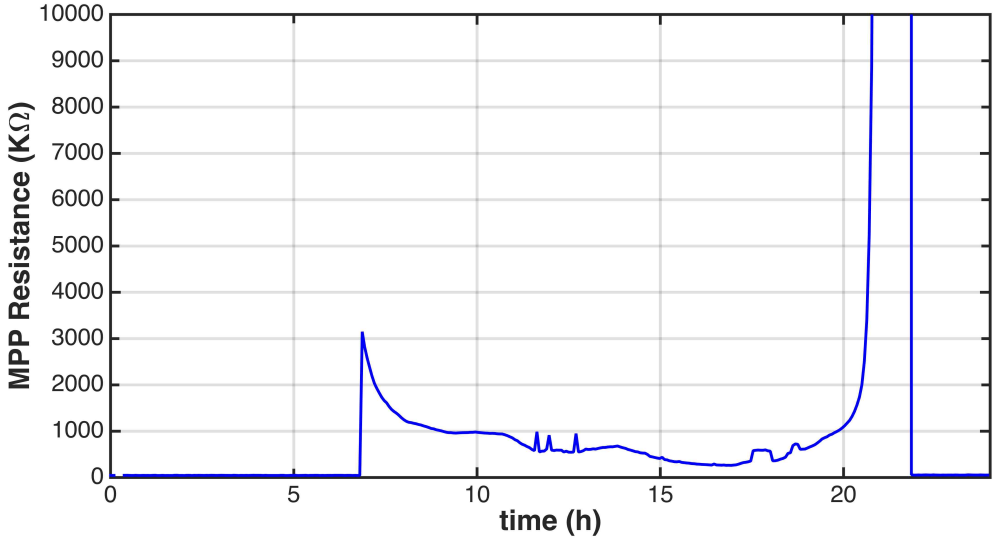
Figure B.49: PV data for the Amorton AM-1417 on 7th of June of 2015. Test made on location C.



(a)



(b)



(c)

Figure B.50: Maximum power point coordinates for the Amorton AM-1417 CA on 7th of June of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

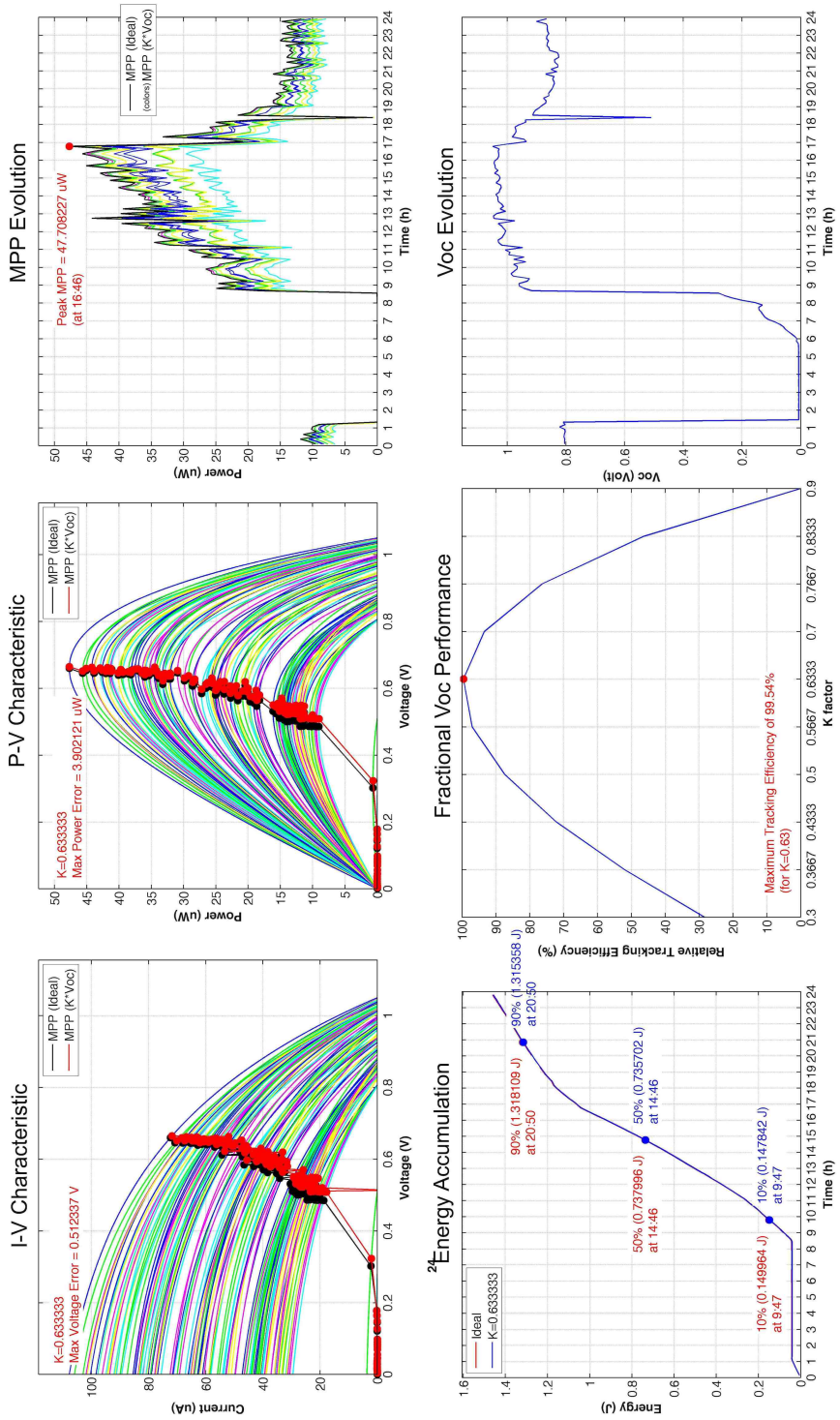
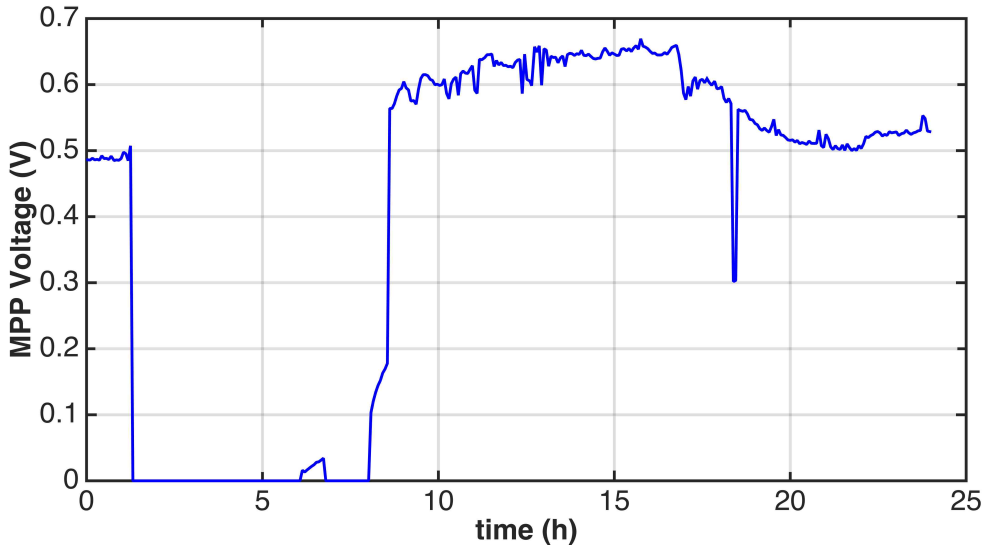
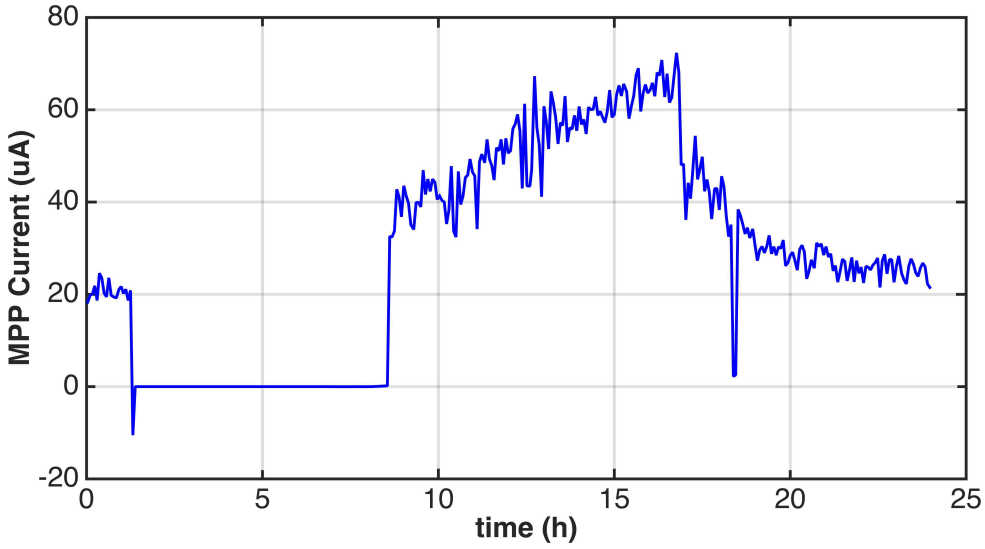


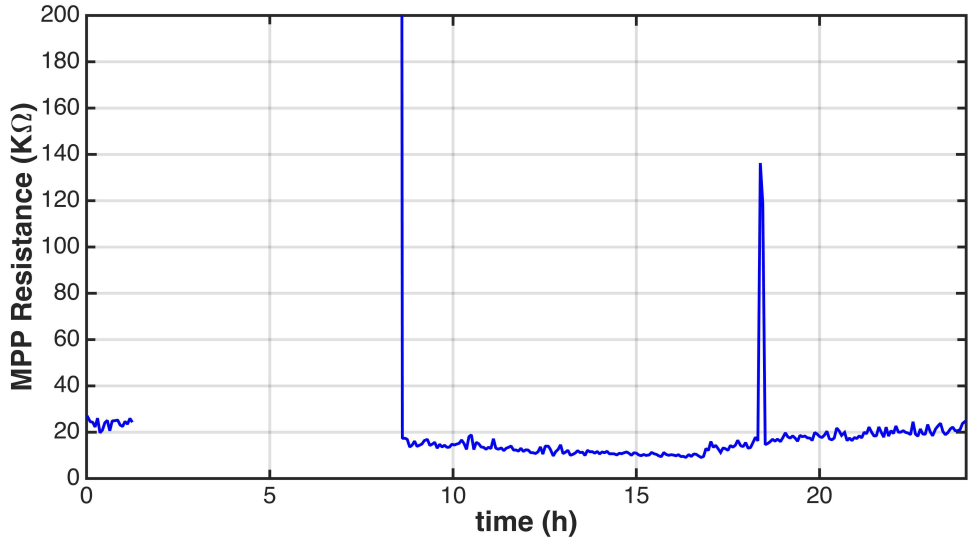
Figure B.51: PV data for the IXYS SLMD121H04L on 8th of June of 2015. Test made on location C.



(a)



(b)



(c)

Figure B.52: Maximum power point coordinates for the IXYS SLMD121H04L on 8th of June of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

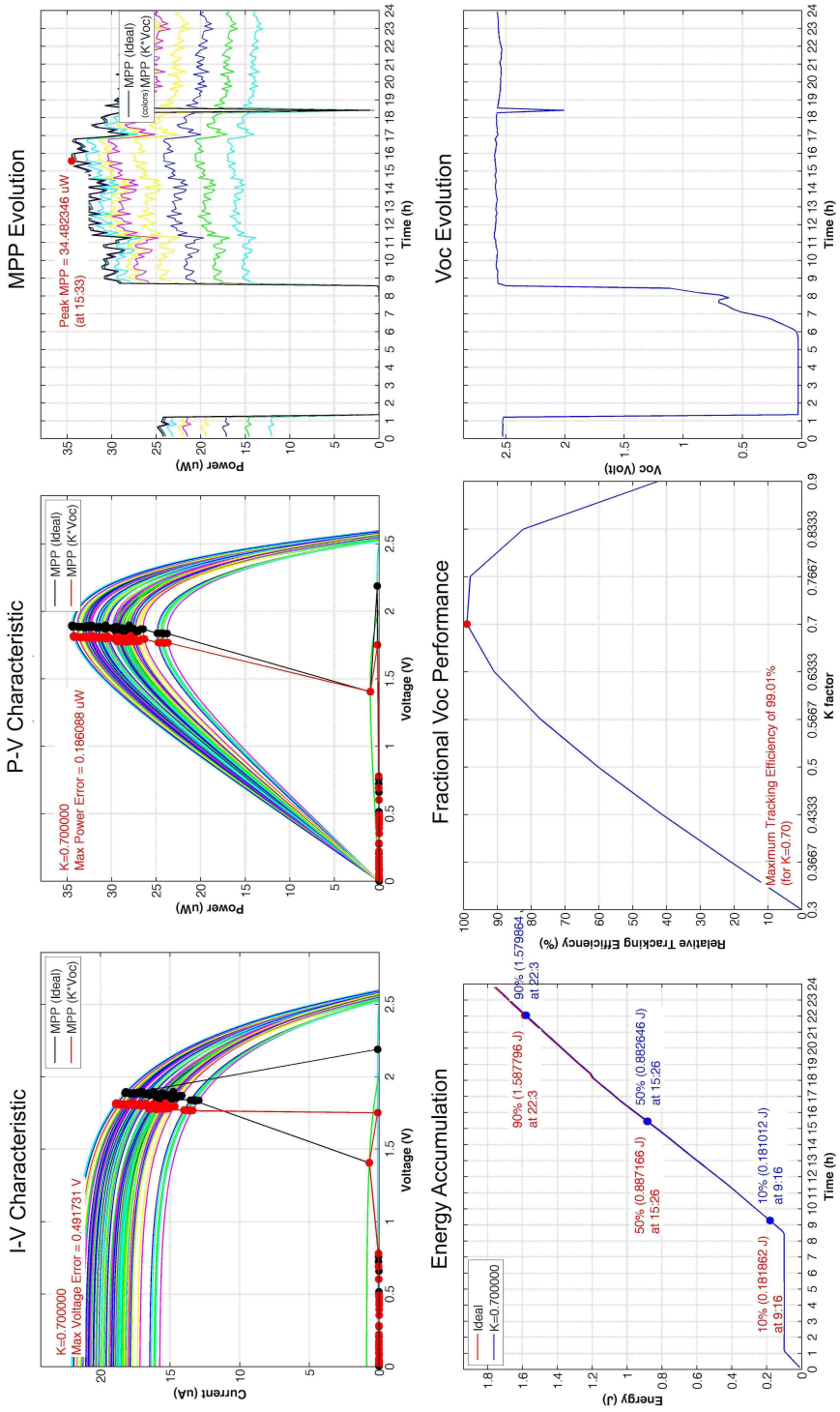
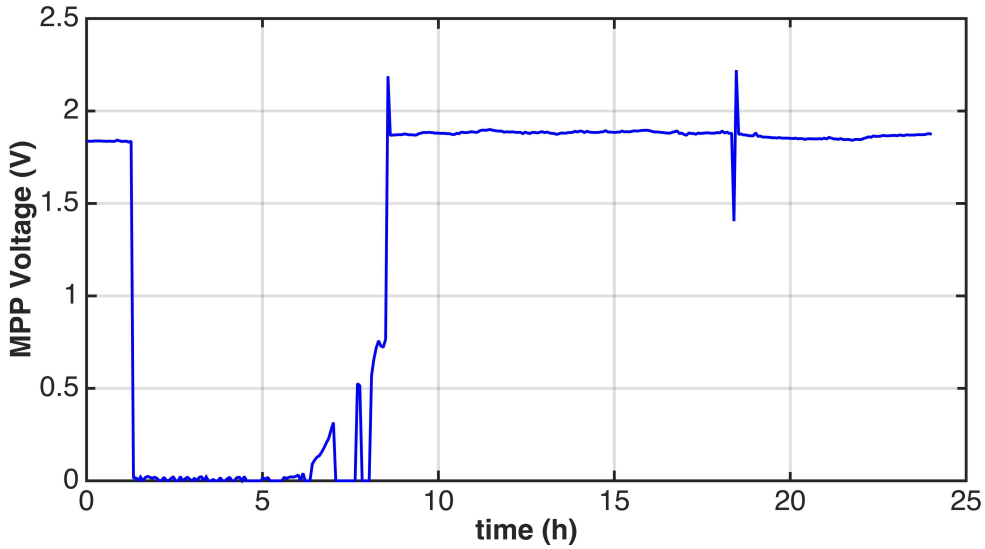
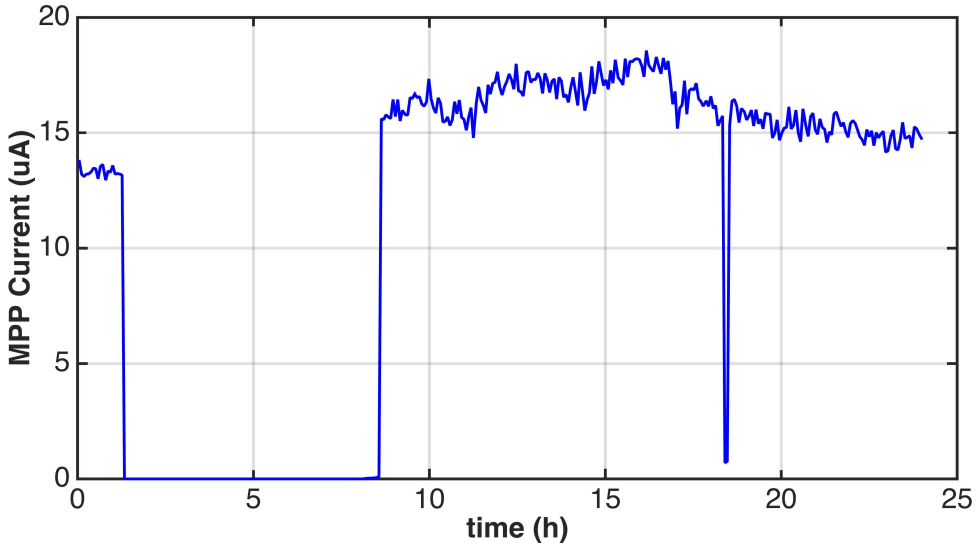


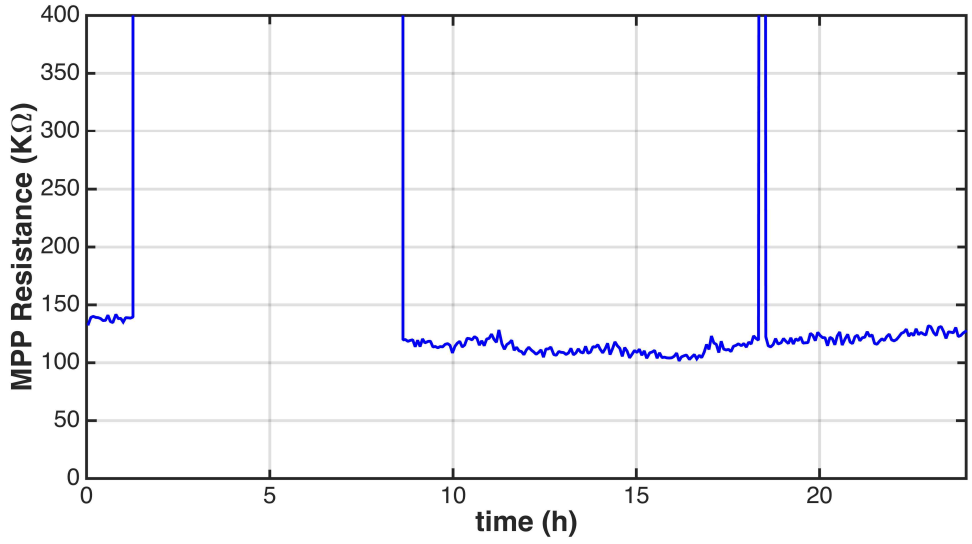
Figure B.53: PV data for the CYMBET CBC-PV-01N on 8th of June of 2015. Test made on location C.



(a)



(b)



(c)

Figure B.54: Maximum power point coordinates for the CYMBET CBC-PV-01N on 8th of June of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

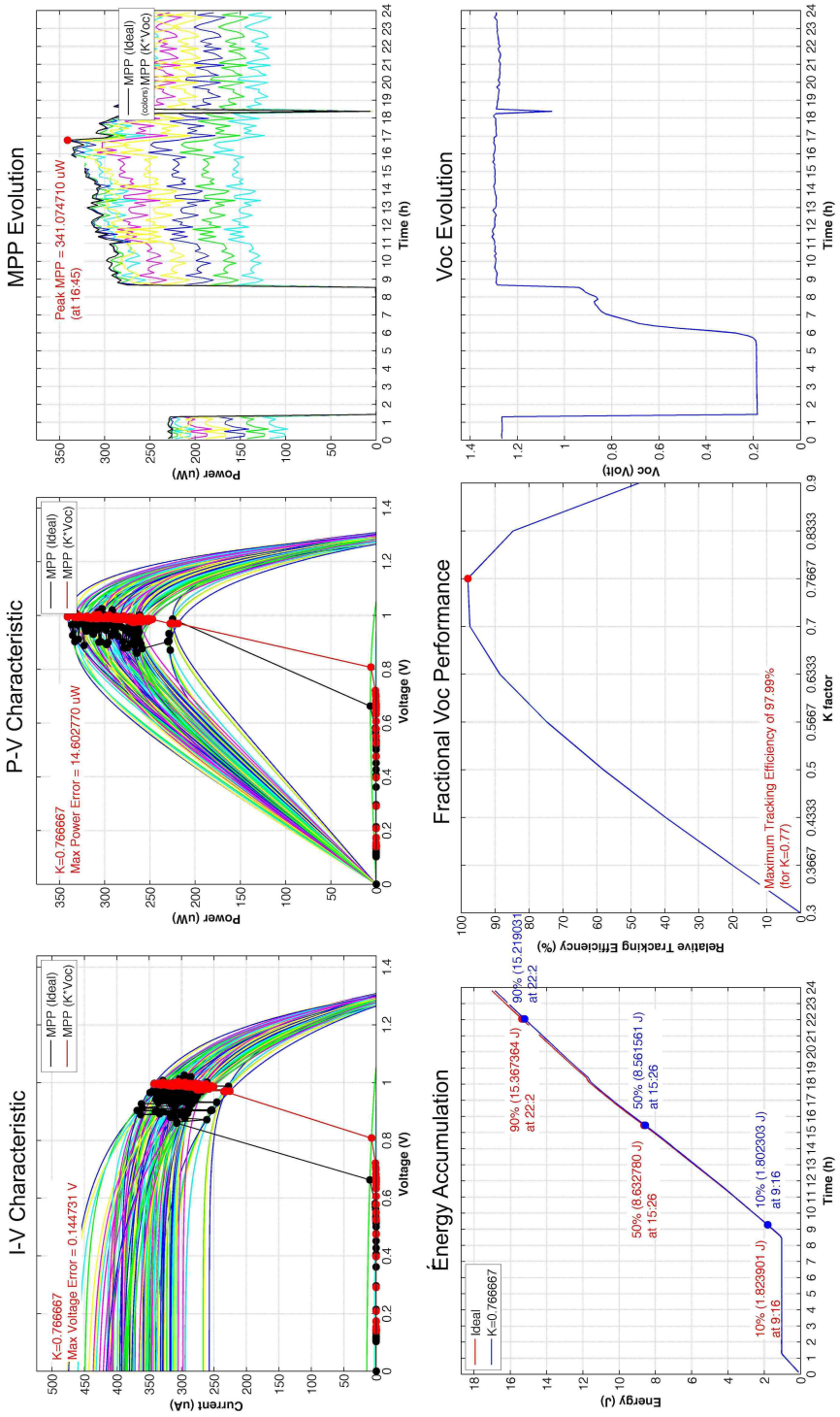
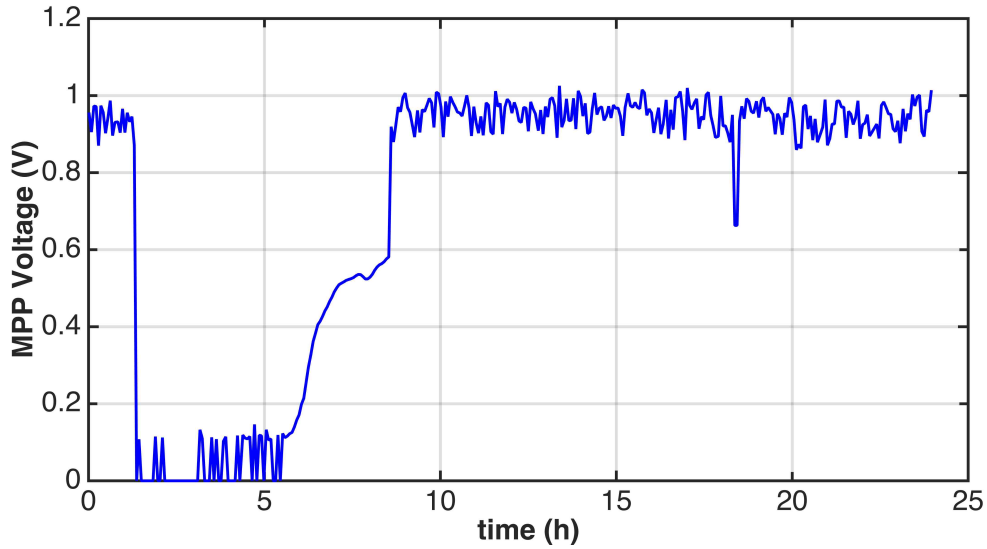
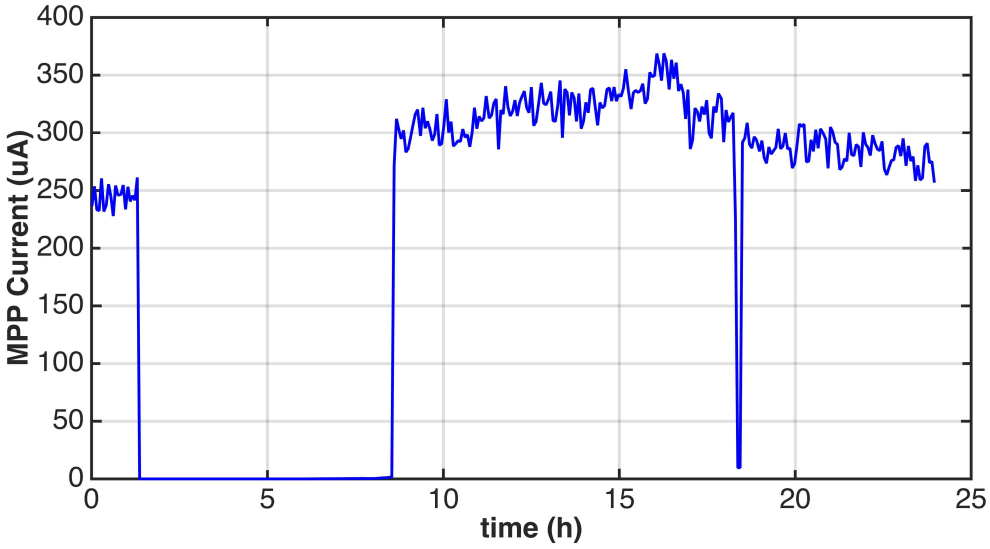


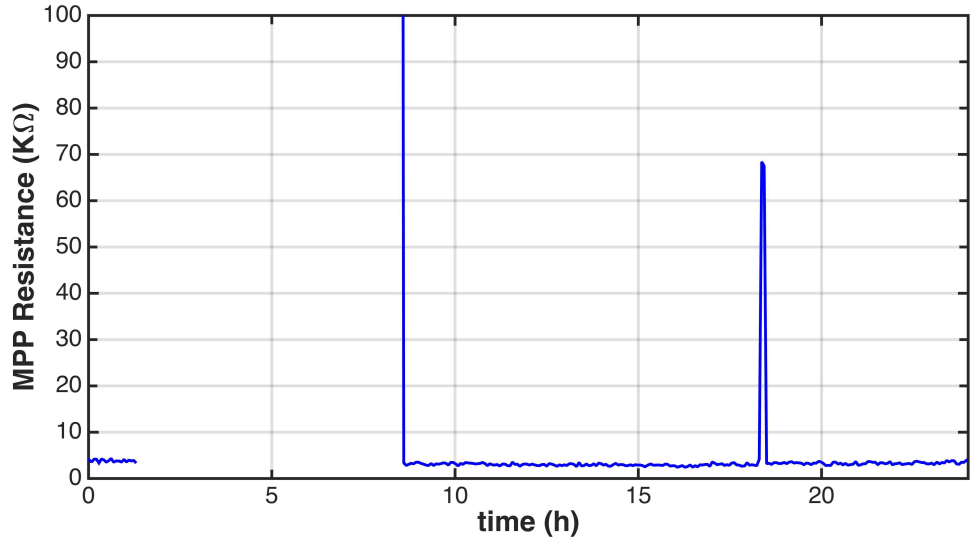
Figure B.55: PV data for the Amorton AM-1454 on 8th of June of 2015. Test made on location C.



(a)



(b)



(c)

Figure B.56: Maximum power point coordinates for the Amorton AM-1454 CA on 8th of June of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

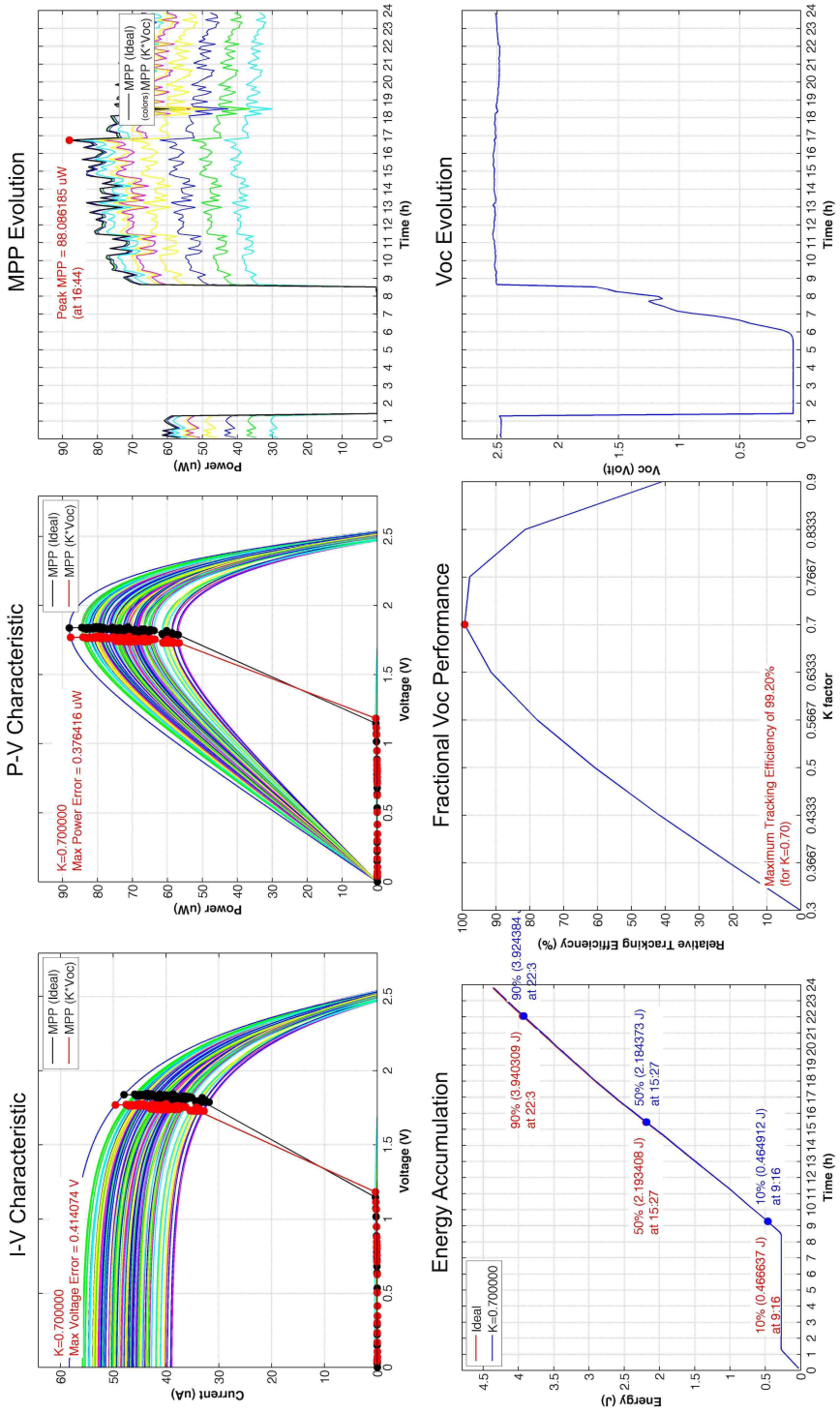
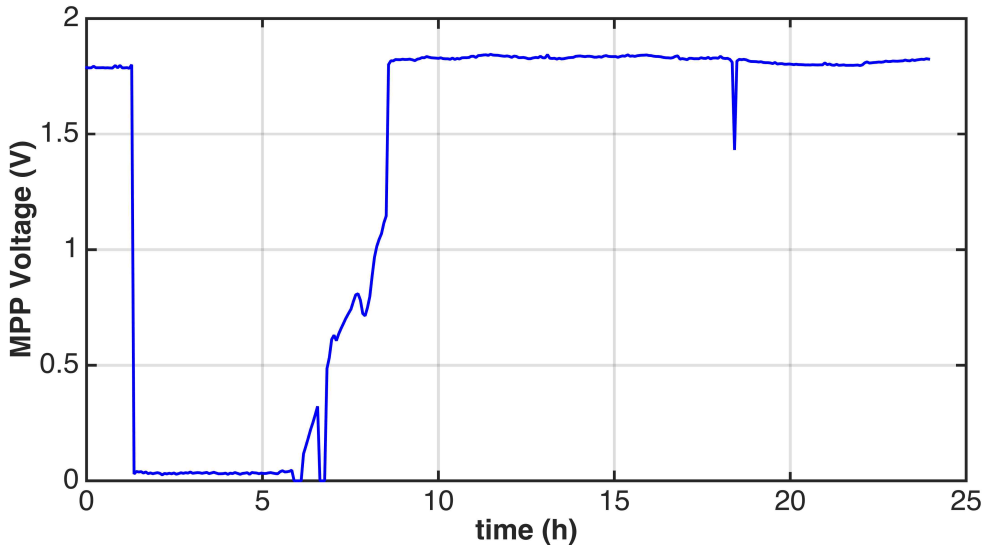
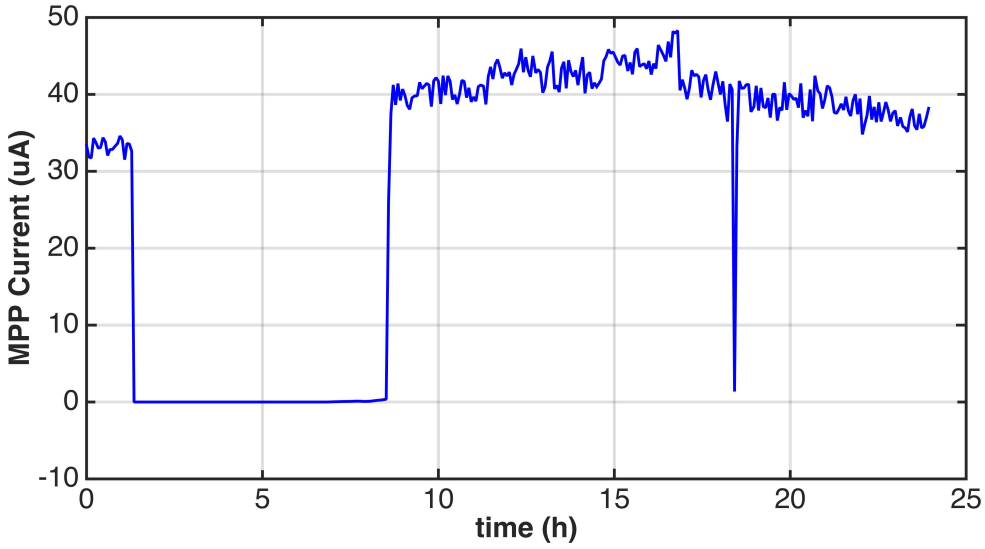


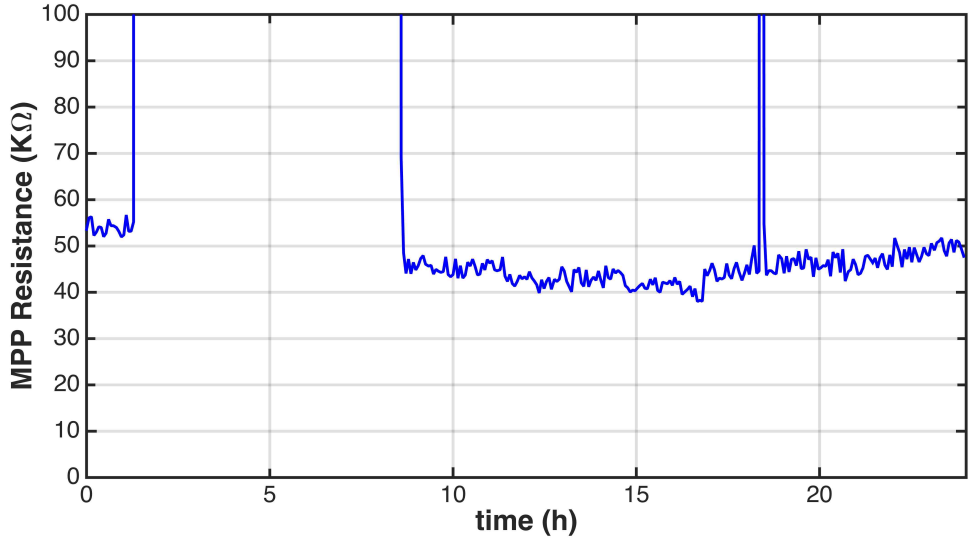
Figure B.57: PV data for the Amorton AM-1418 on 8th of May of 2015. Test made on location C.



(a)



(b)



(c)

Figure B.58: Maximum power point coordinates for the Amorton AM-1417 CA on 8th of June of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

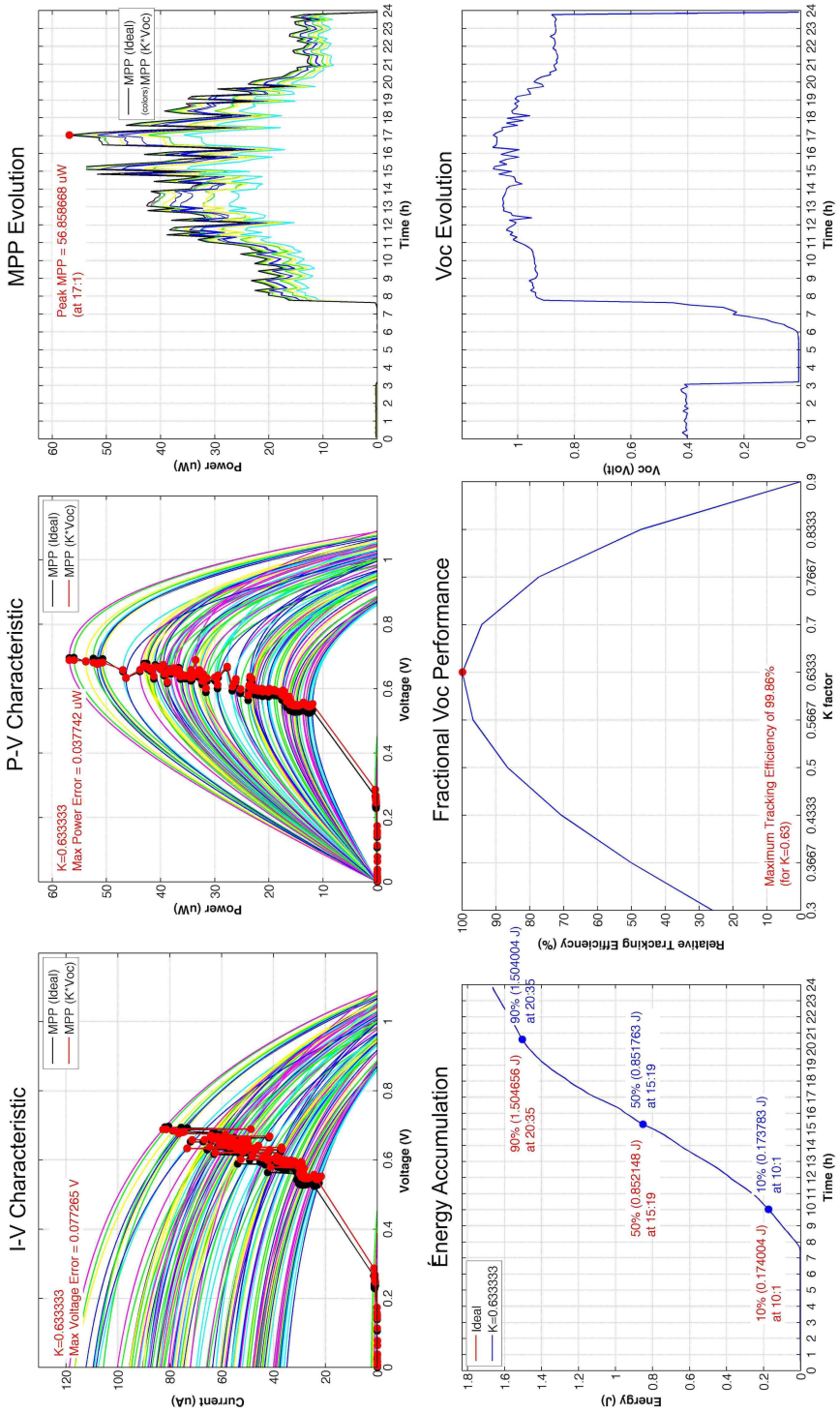
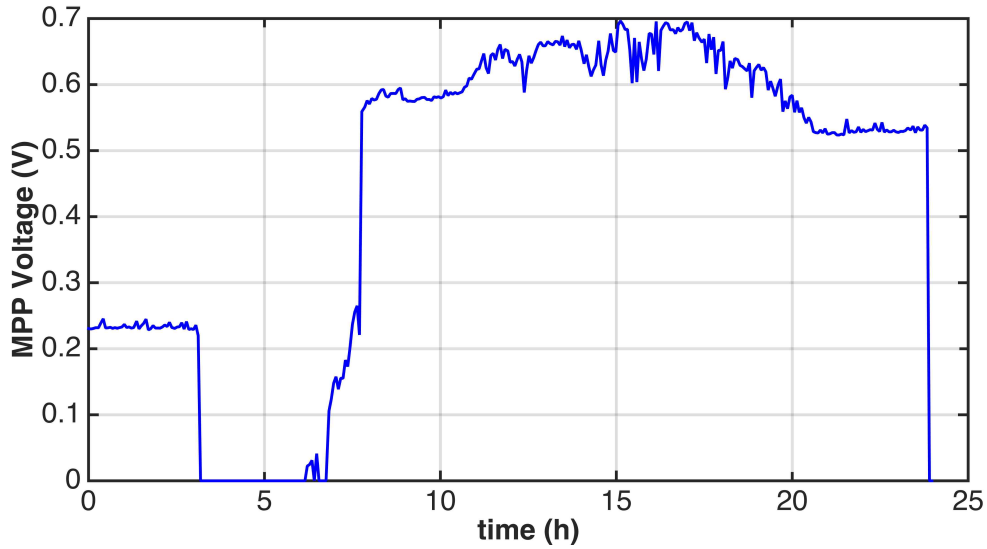
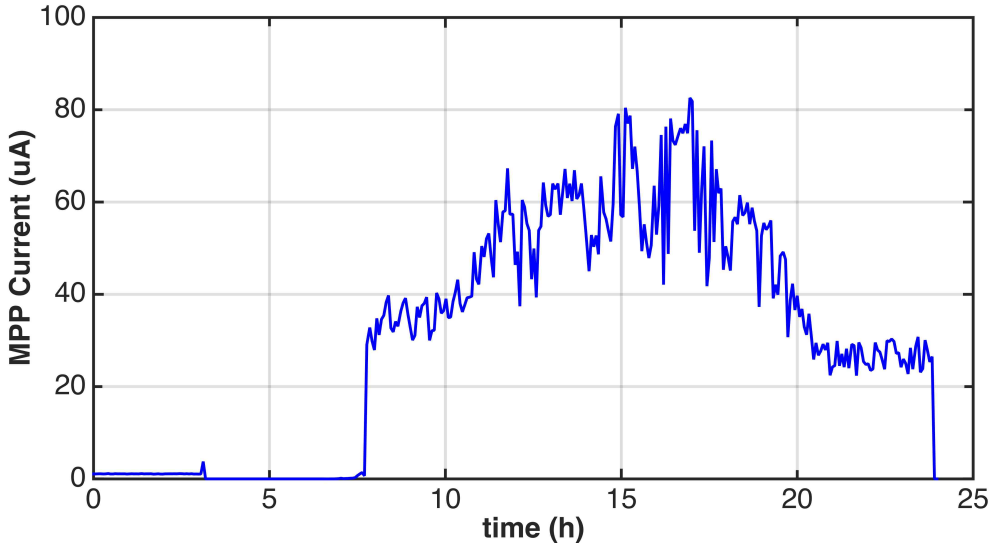


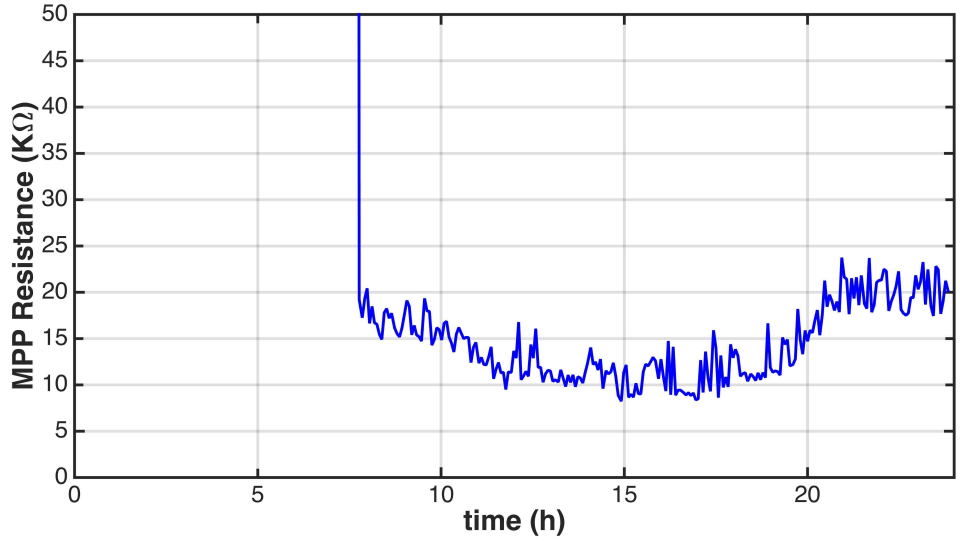
Figure B.59: PV data for the IXYS SLMD121H04L on 11th of June of 2015. Test made on location C.



(a)



(b)



(c)

Figure B.60: Maximum power point coordinates for the IXYS SLMD121H04L on 11th of June of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

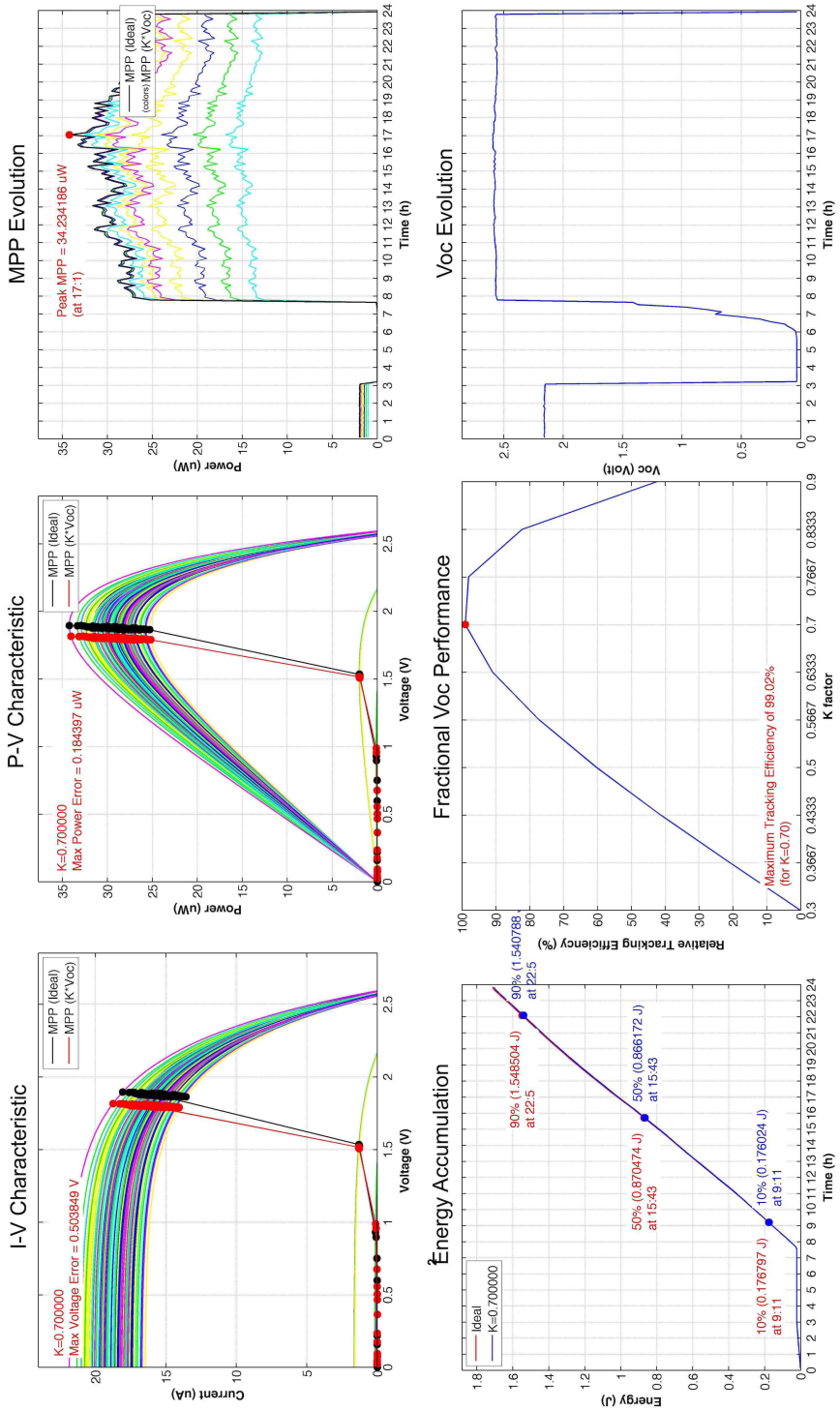
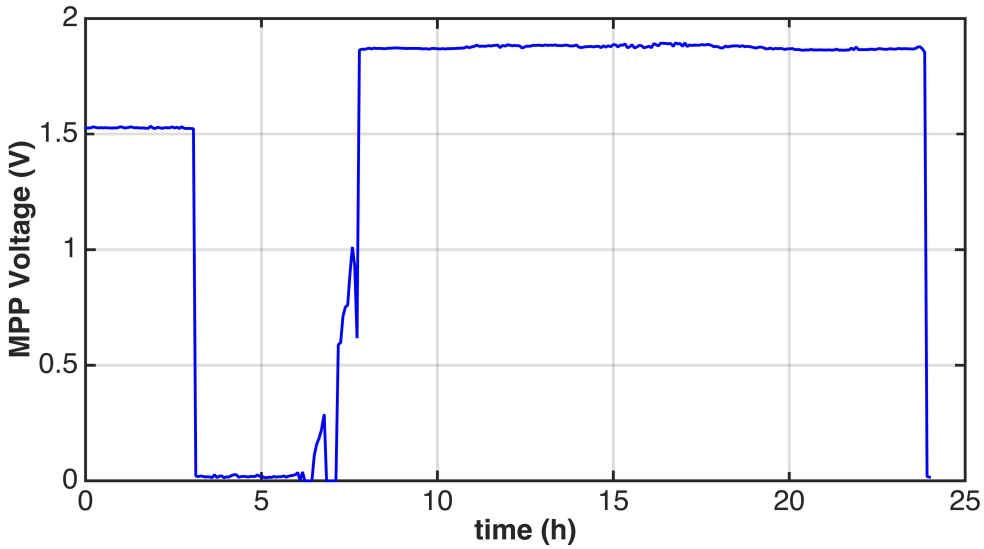
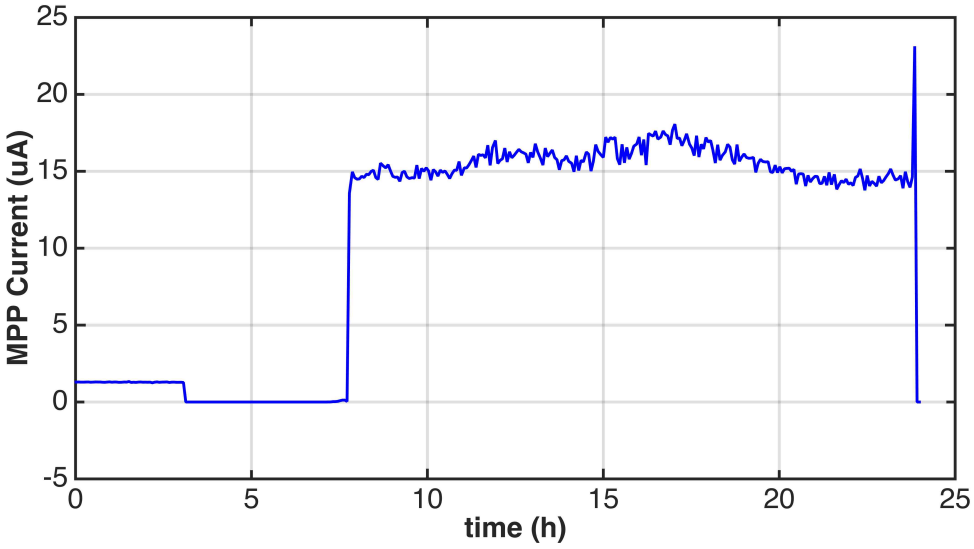


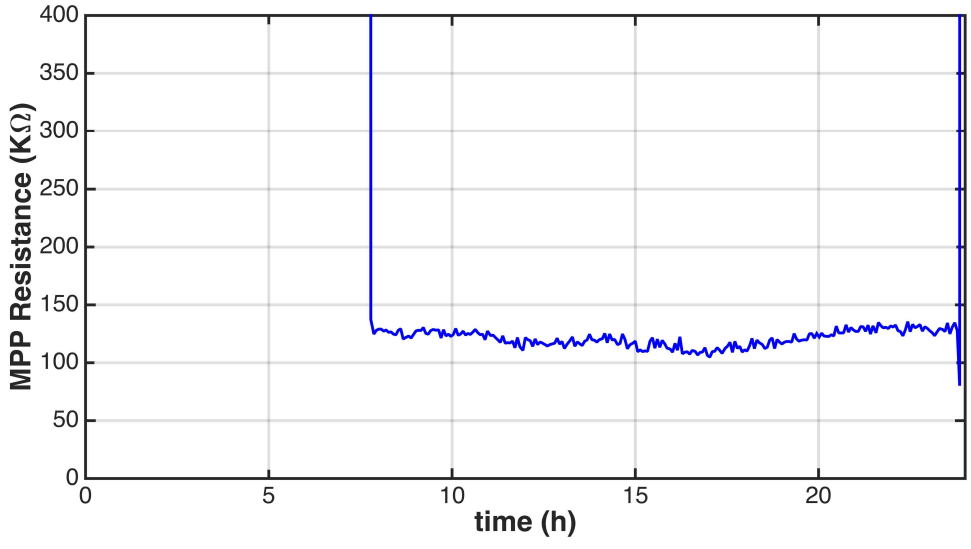
Figure B.61: PV data for the CYMBET CBC-PV-01N on 11th of June of 2015. Test made on location C.



(a)



(b)



(c)

Figure B.62: Maximum power point coordinates for the CYMBET CBC-PV-01N on 11th of June of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

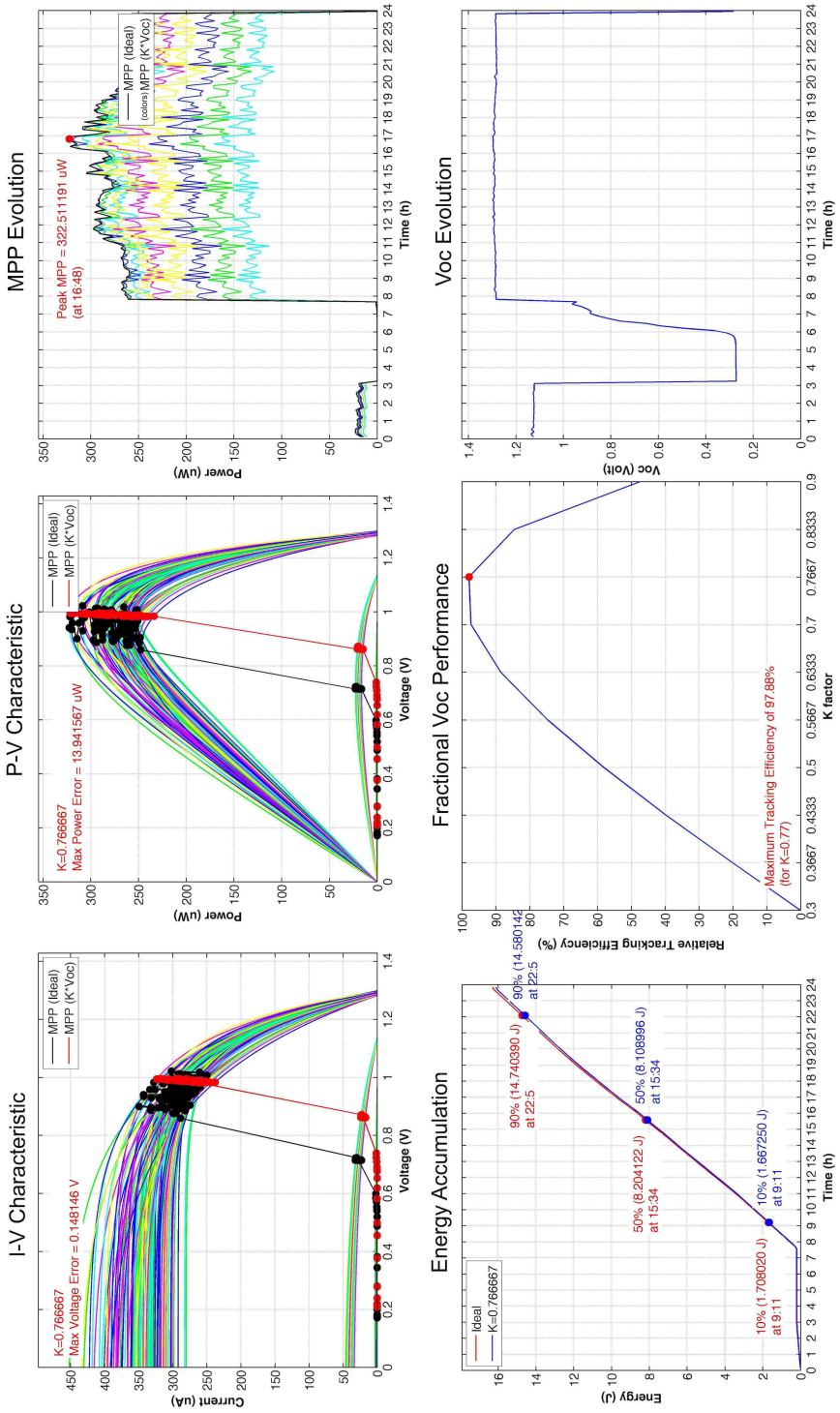
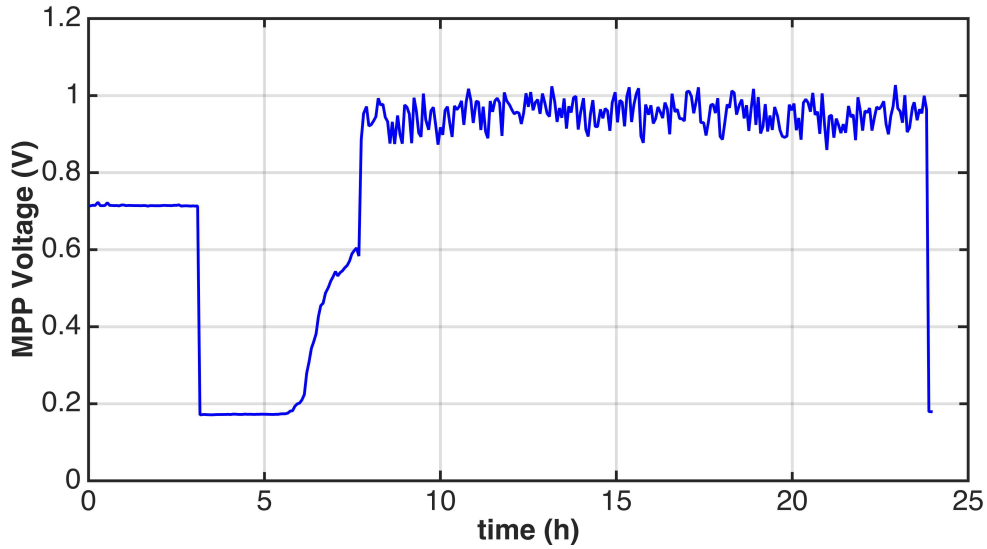
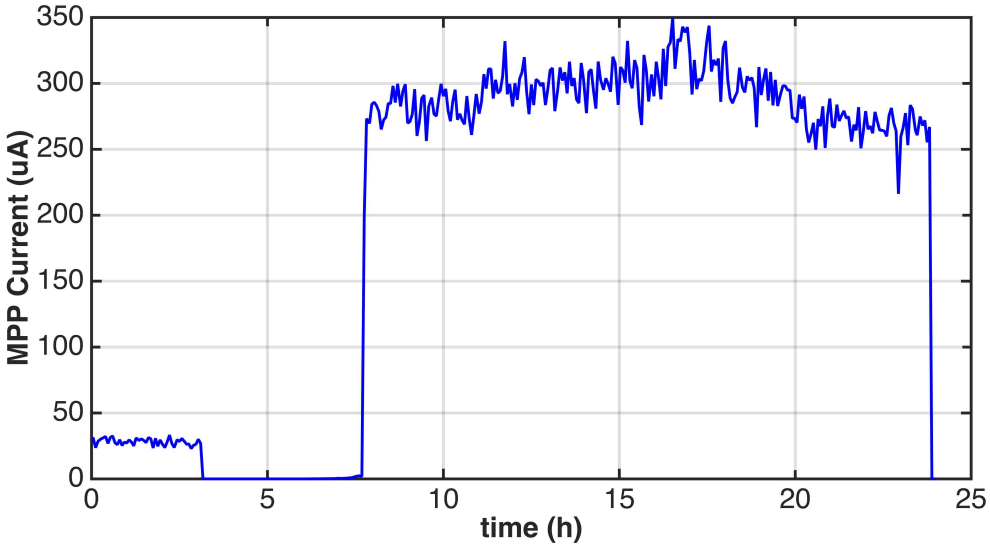


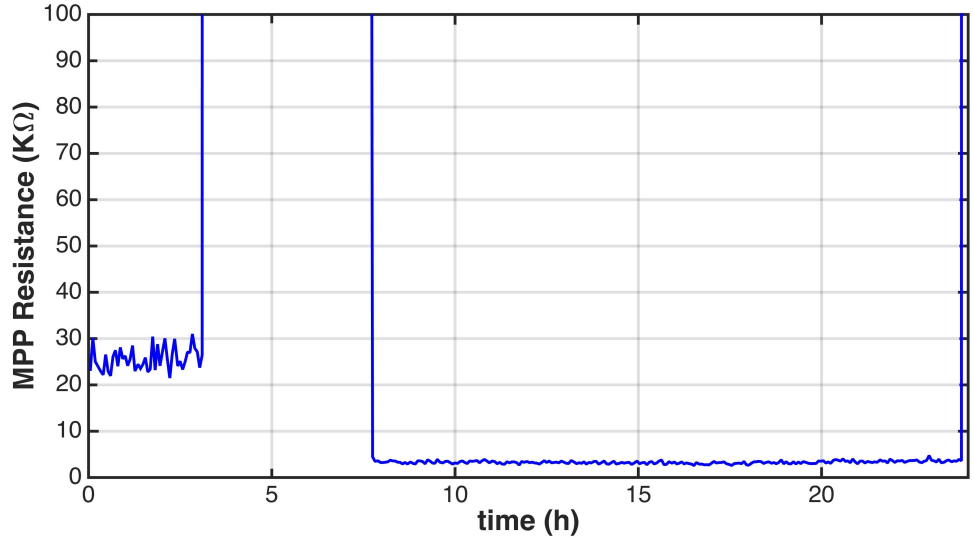
Figure B.63: PV data for the Amorton AM-1454 on 11th of June of 2015. Test made on location C.



(a)



(b)



(c)

Figure B.64: Maximum power point coordinates for the Amorton AM-1454 CA on 11th of June of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

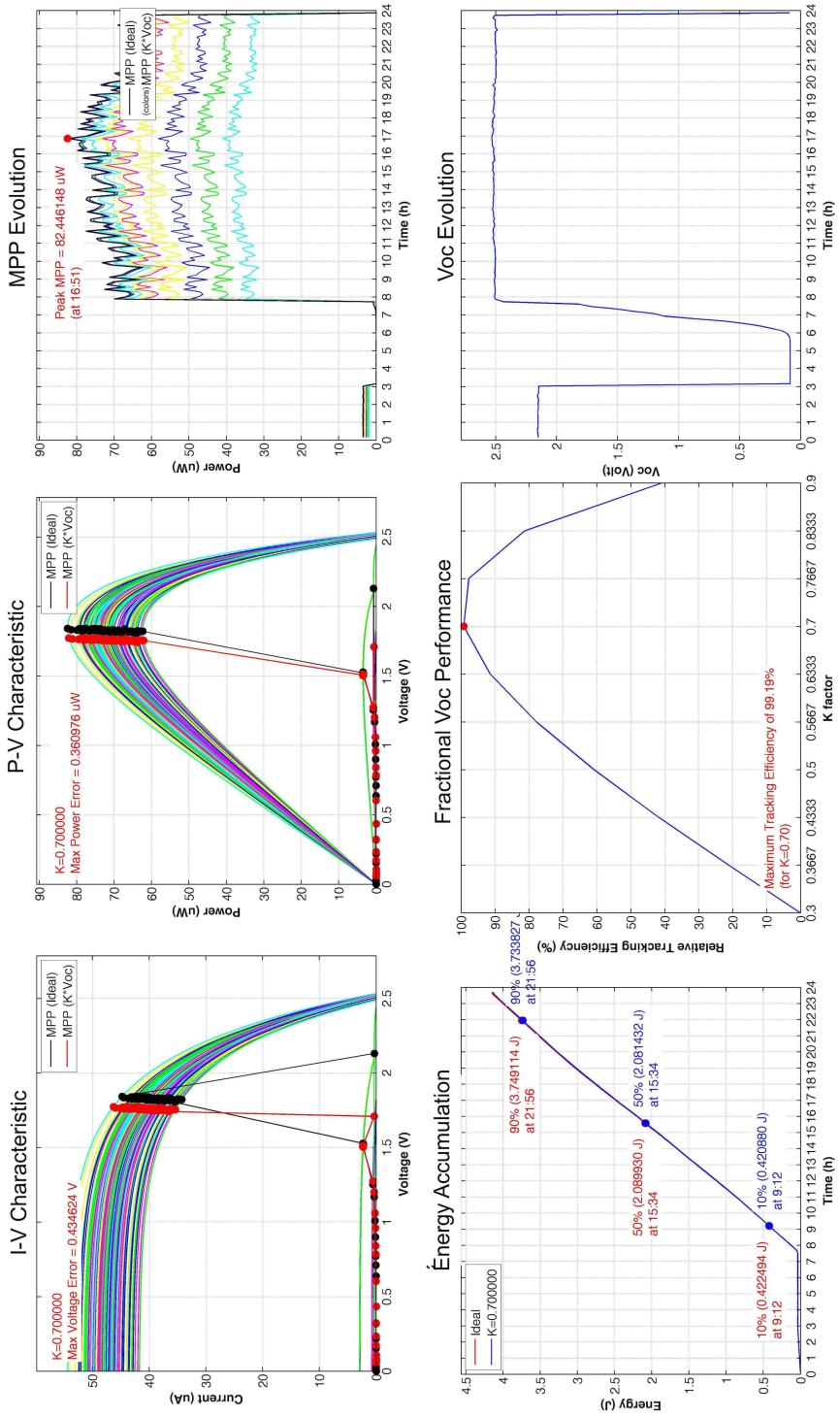
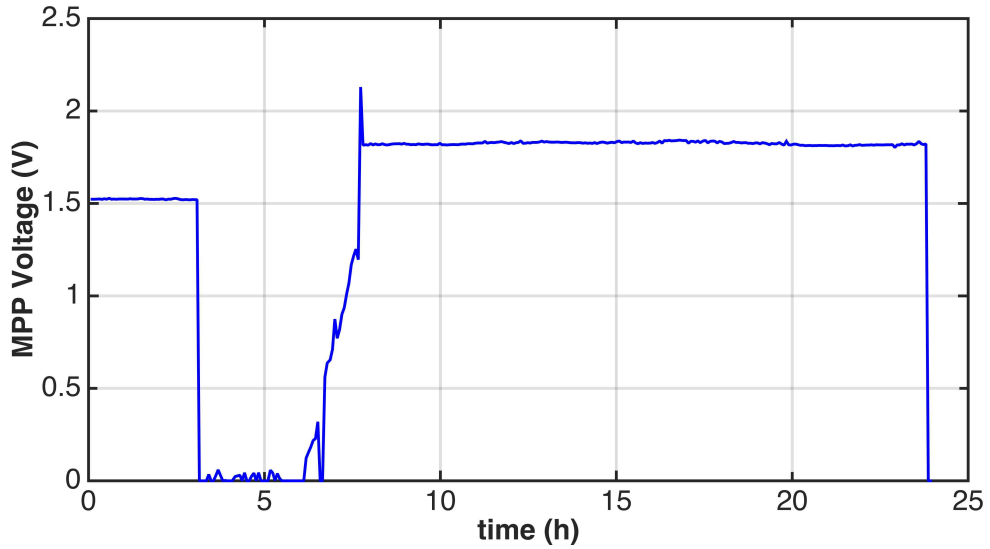
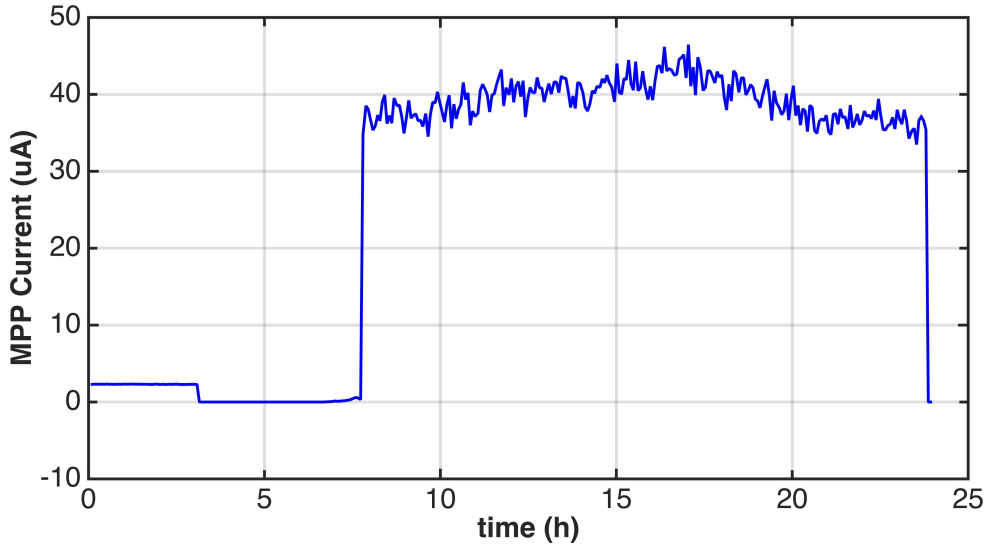


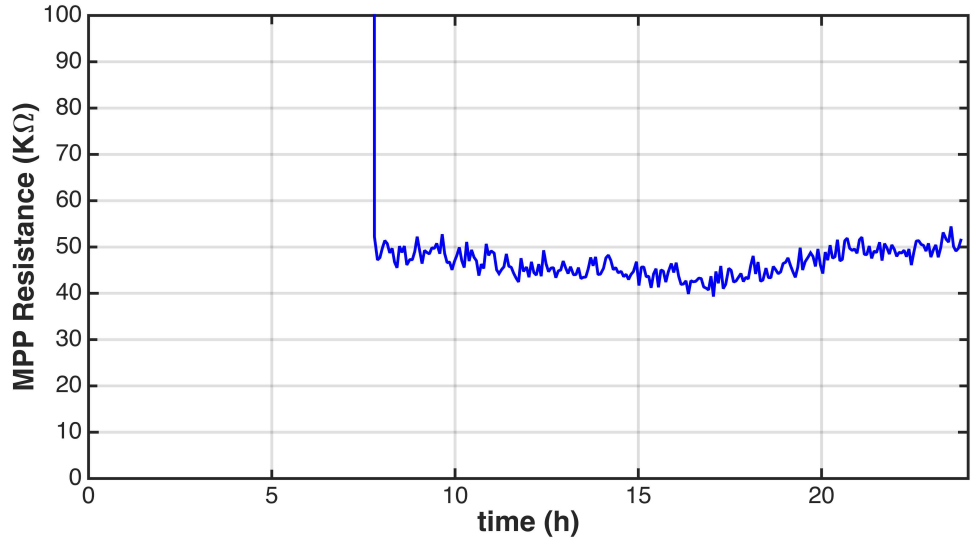
Figure B.65: PV data for the Amorton AM-14111 on 11th of June of 2015. Test made on location C.



(a)



(b)



(c)

Figure B.66: Maximum power point coordinates for the Amorton AM-1417 CA on 11th of June of 2015. (a) V_{MPP}; (b) I_{MPP}; (c) $R_{MPP} = V_{MPP}/I_{MPP}$

Appendix C

PV Cell Capacitance Measurements

The capacitance of the PV cells was measured using the test circuit depicted in Figure C.1.

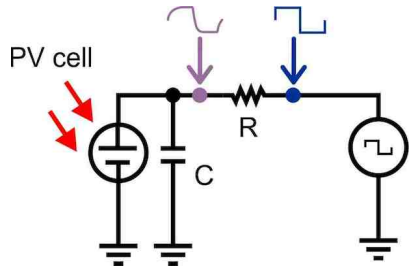


Figure C.1: PV cell capacitance measurement circuit.

As illustrated in Figure C.1, the PV cell under test had a square wave applied at its terminals, through a series resistance. Due to the capacitance of the PV cell, the signal at the terminals of the device is delayed and, by measuring the rise time – t_R – of this signal, the value of the capacitance can be obtained, as a function of t_R and R, the series resistance of the circuit.

The PV cell must be covered in order to ensure it does not work as a power supply. The analysis to obtain the value of the capacitance is thus approximated by the analysis of a simple $R \times C$ circuit. The cut frequency, f_C, is given by $(2 \times \pi \times R \times C)^{-1}$, where $R \times C$ can be expressed as the time constant of the circuit, τ.

Considering t_R as the time the wave takes to evolve from 10% to 90% of its final value, t_R can be approximated by approximately $2.2 \times \tau$ or $0.35/f_C$. Taking the latter and rearranging the previous Equation yields the value of the PV cell capacitance, as a function of both t_R an R, in Equation C.1.

$$C_{PV} = \frac{t_R}{0.35 \times 2 \times \pi \times R} \tag{C.1}$$

The waveforms of the signals probed to analyse the capacitance of the PV cells can be seen in Figure C.2.

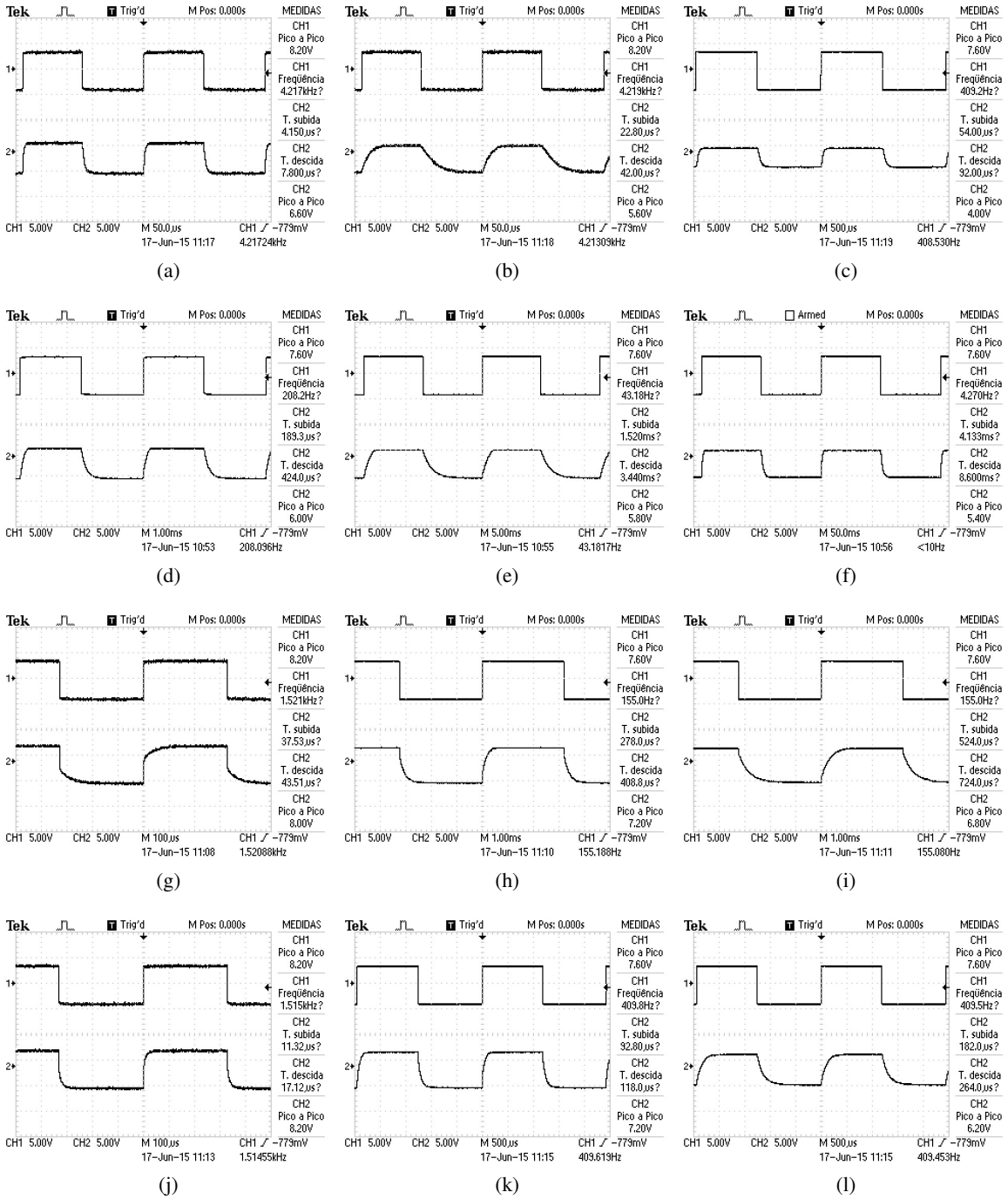
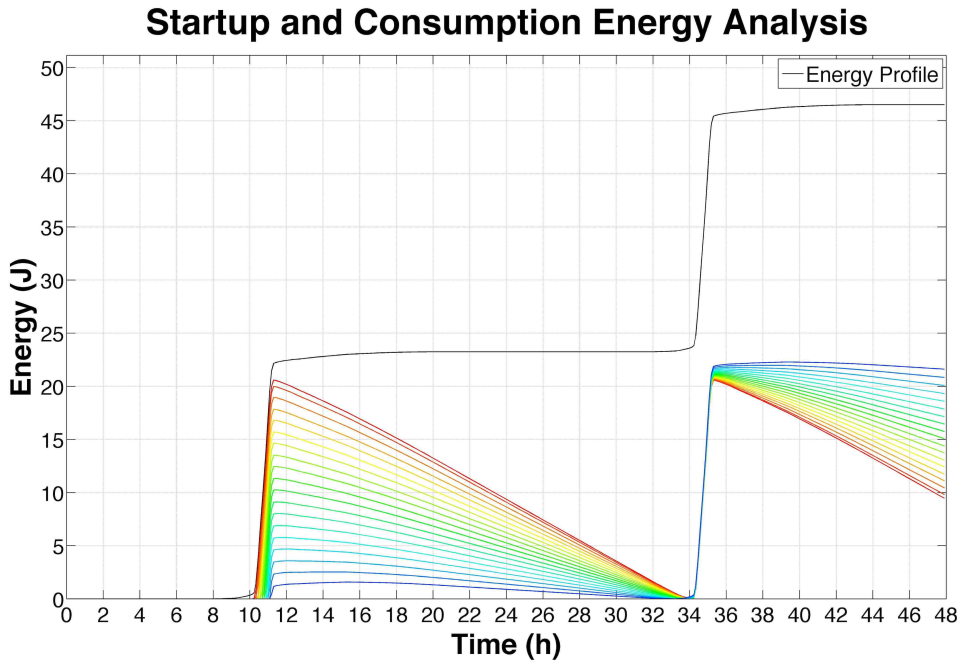


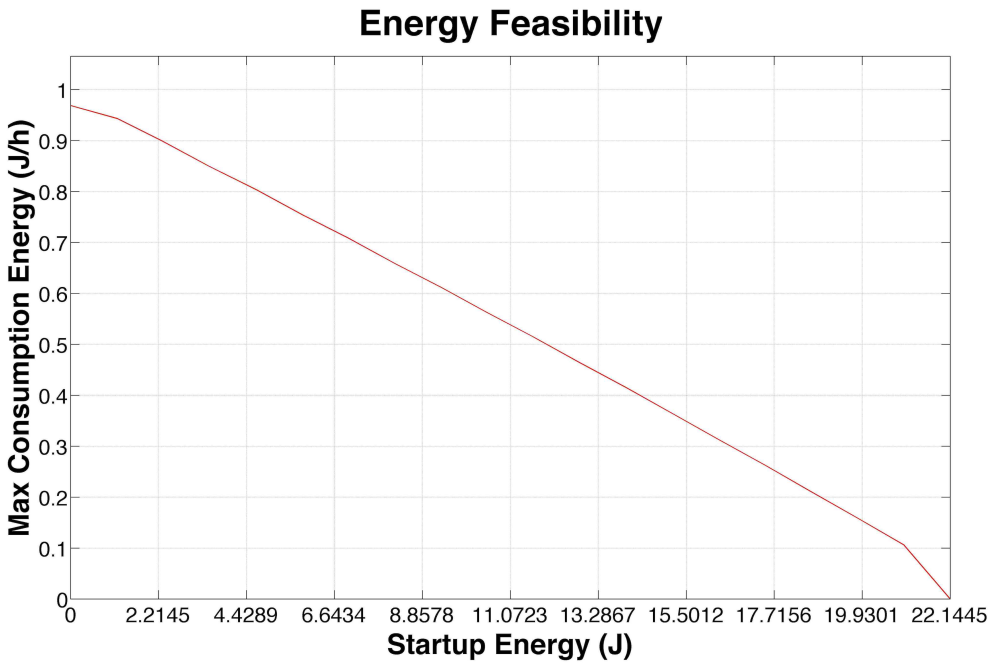
Figure C.2: Capacitance analysis for the tested PV cell Models. IXYS SLMD121H04L PV cell – (a) $R = 1K\Omega$, (b) $R = 10K\Omega$ and (c) $R = 22K\Omega$; CYMBET CBC-PV-01N PV cell – (d) $R = 1K\Omega$, (e) $R = 10K\Omega$ and (f) $R = 22K\Omega$; Amorton AM-1454CA PV cell – (g) $R = 1K\Omega$, (h) $R = 10K\Omega$ and (i) $R = 22K\Omega$; Amorton AM-1417CA PV cell – (j) $R = 1K\Omega$, (k) $R = 10K\Omega$ and (l) $R = 22K\Omega$.

Appendix D

Energy Feasibility Results

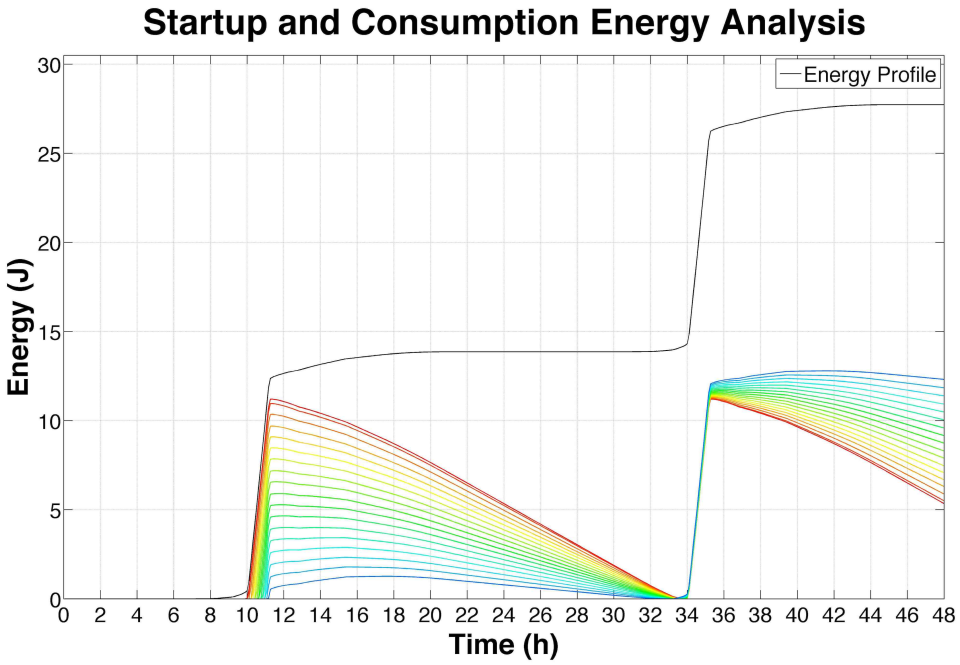


(a)

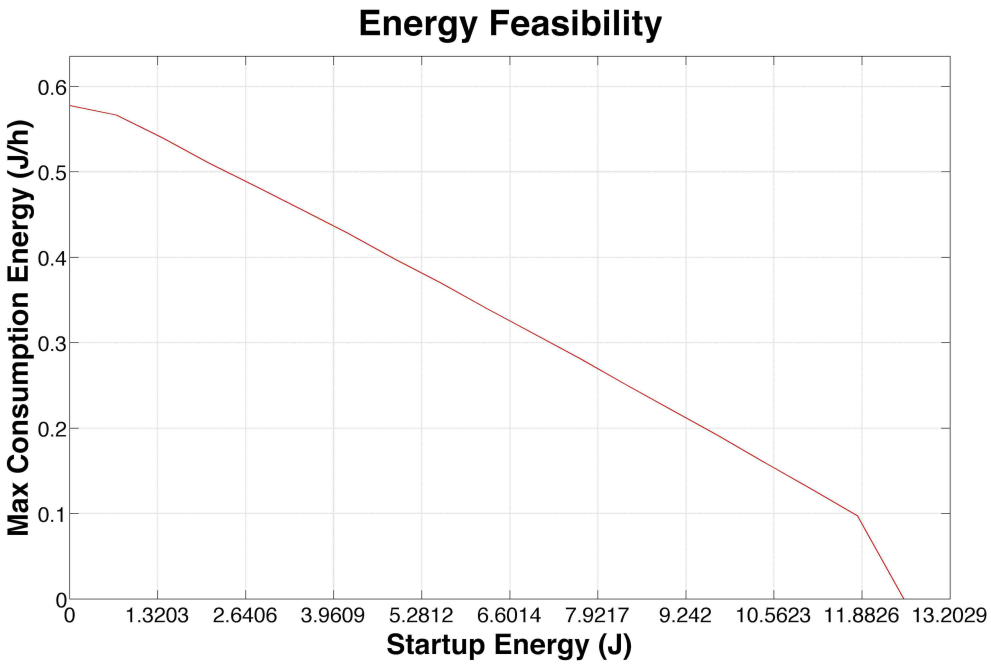


(b)

Figure D.1: Feasibility of the IXYS SLMD121H04L on 19th of May of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

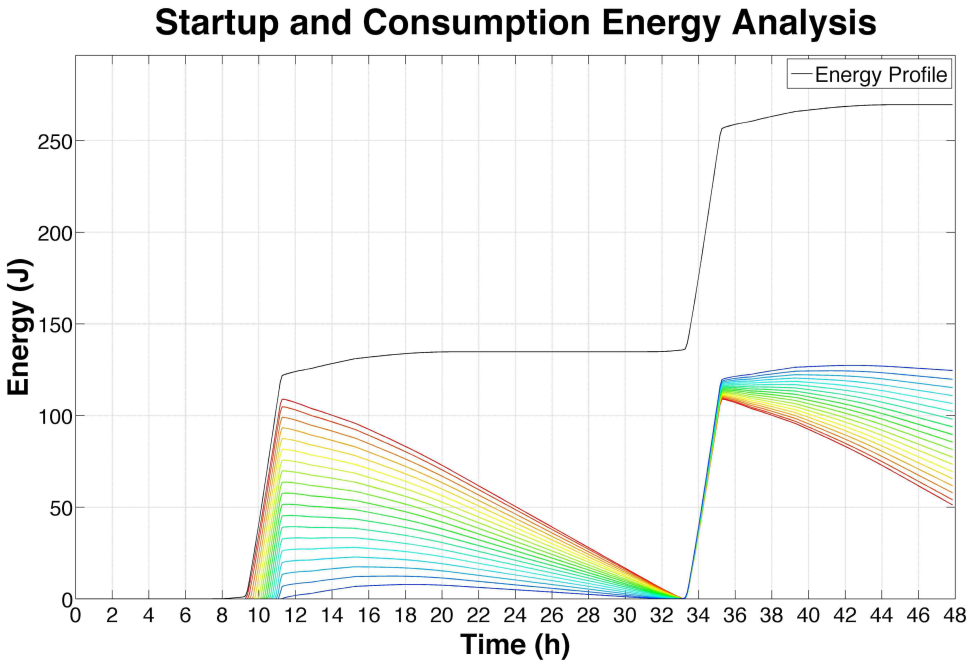


(a)

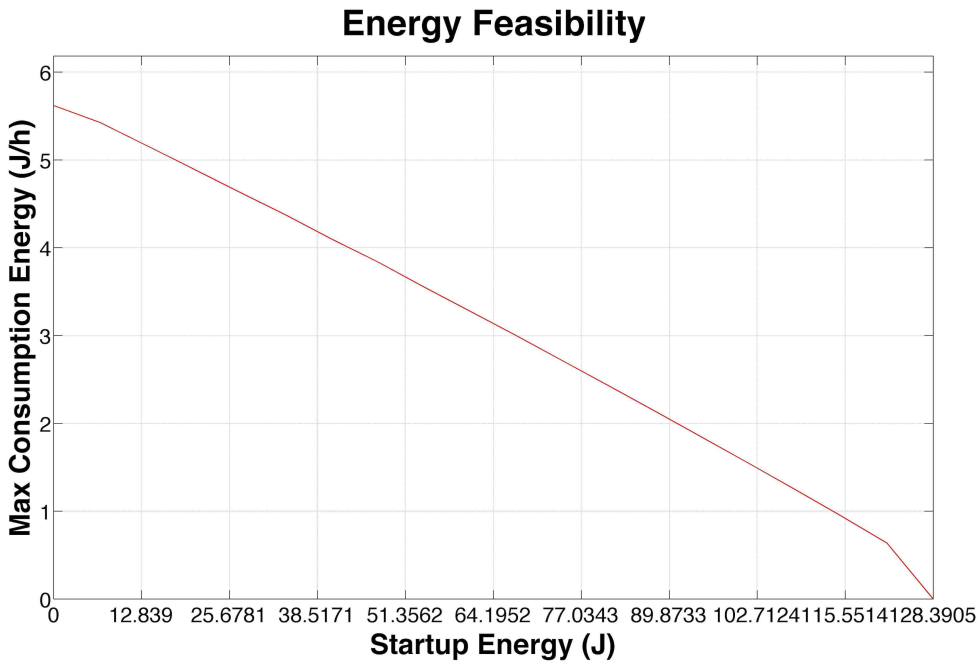


(b)

Figure D.2: Feasibility of the CYMBET CBC-PV-01N on 19th of May of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

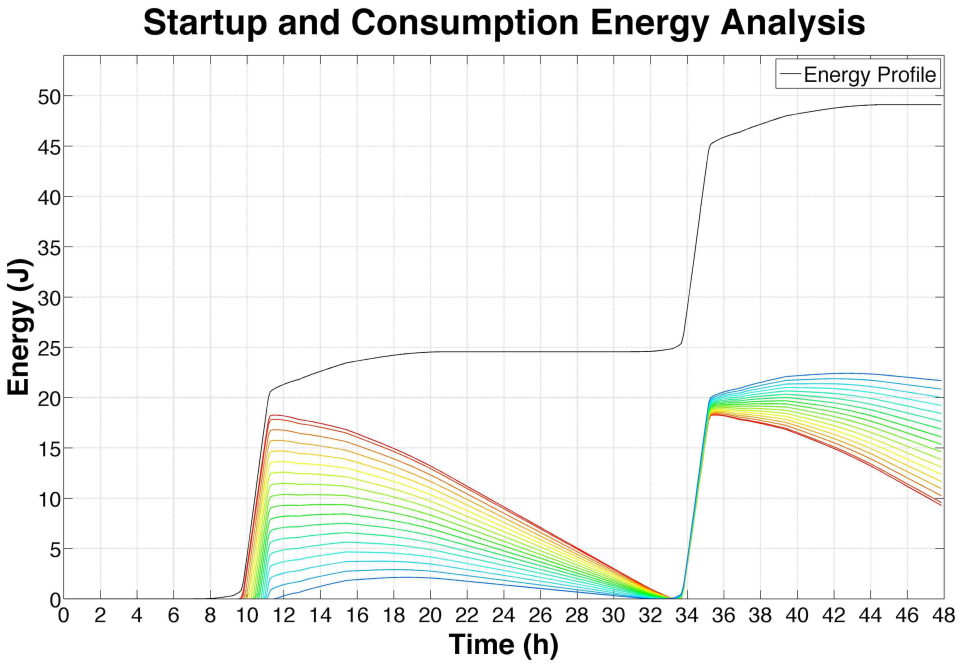


(a)

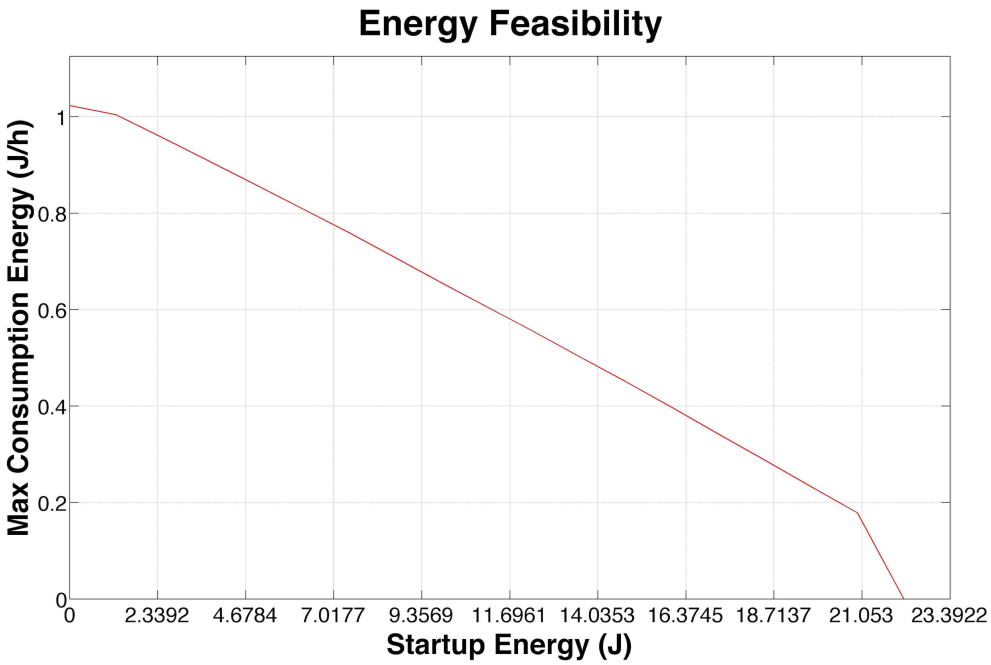


(b)

Figure D.3: Feasibility of the Amorton AM-1454 on 19th of May of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

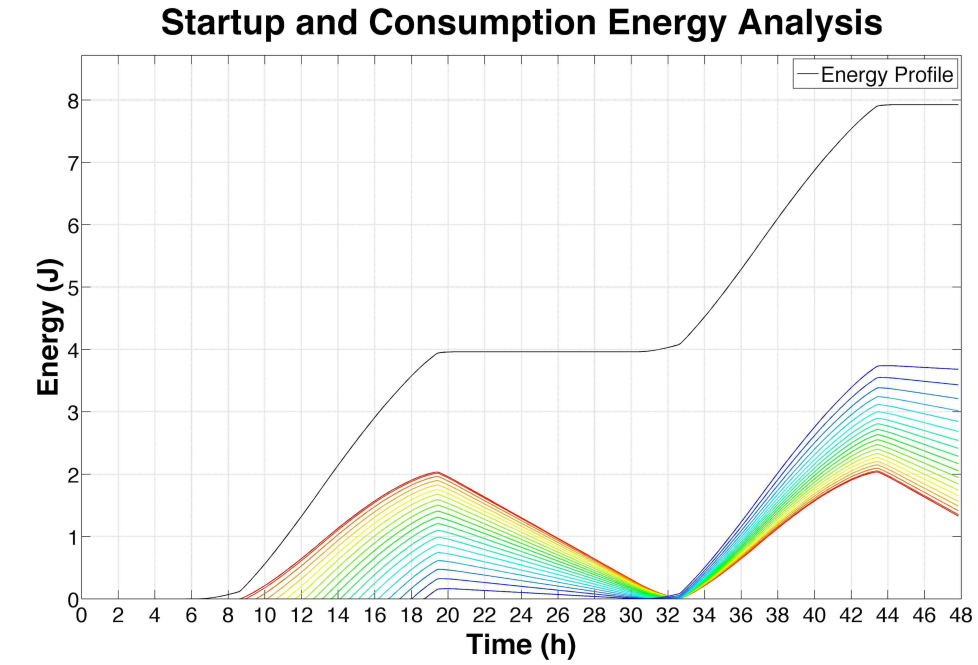


(a)

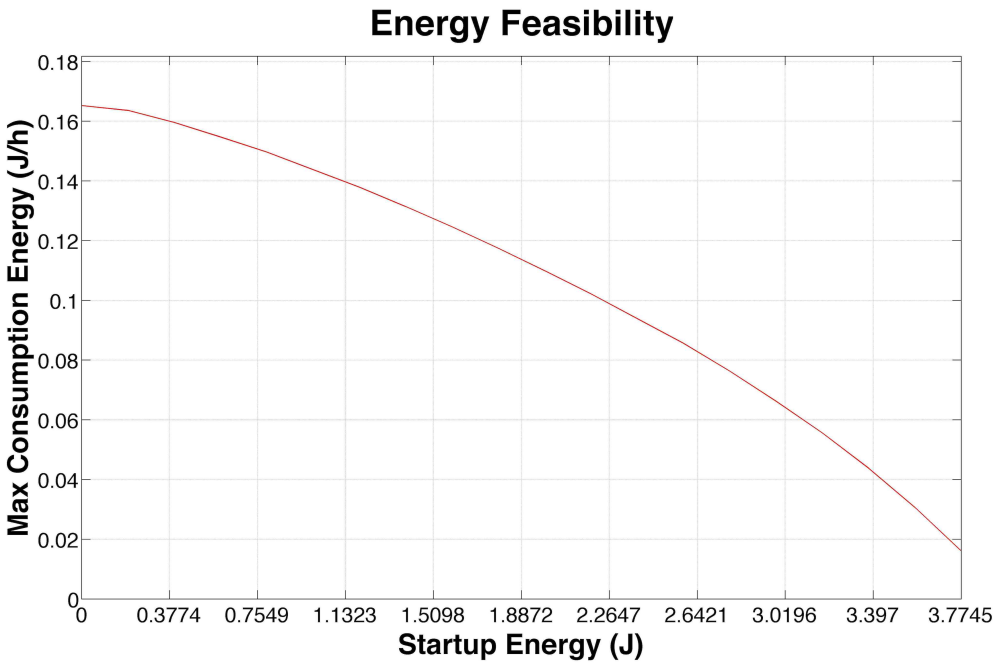


(b)

Figure D.4: Feasibility of the Amorton AM-1417 on 19th of May of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

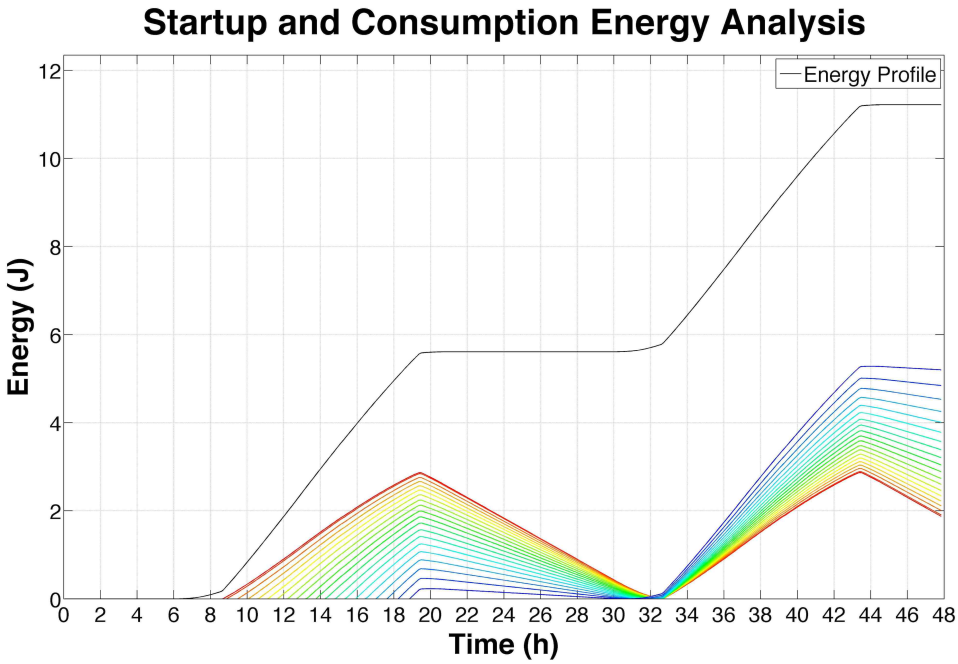


(a)

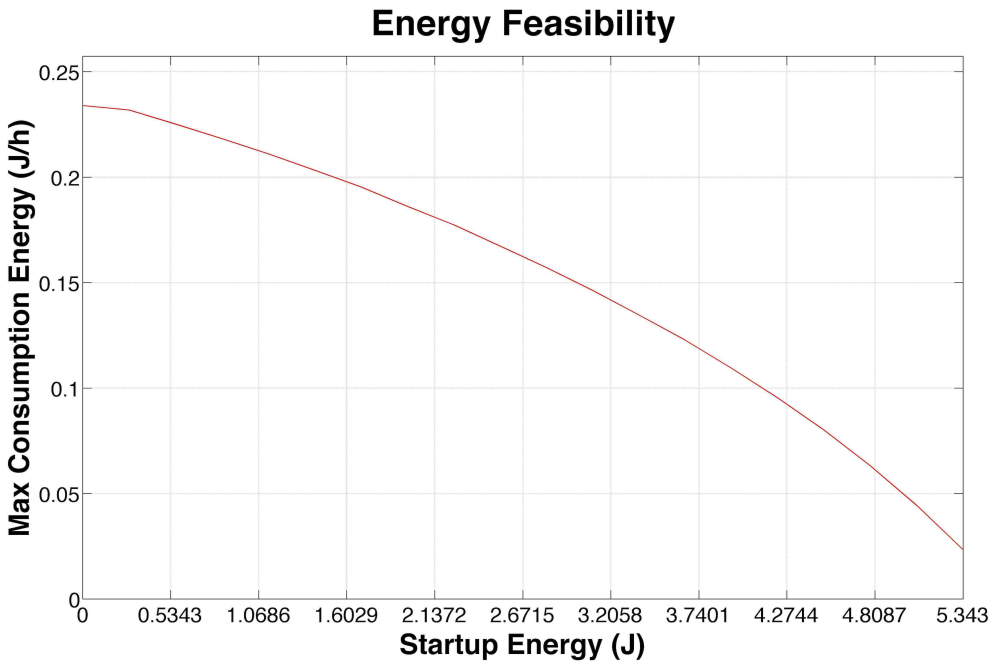


(b)

Figure D.5: Feasibility of the IXYS SLMD121H04L on 22nd of May of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

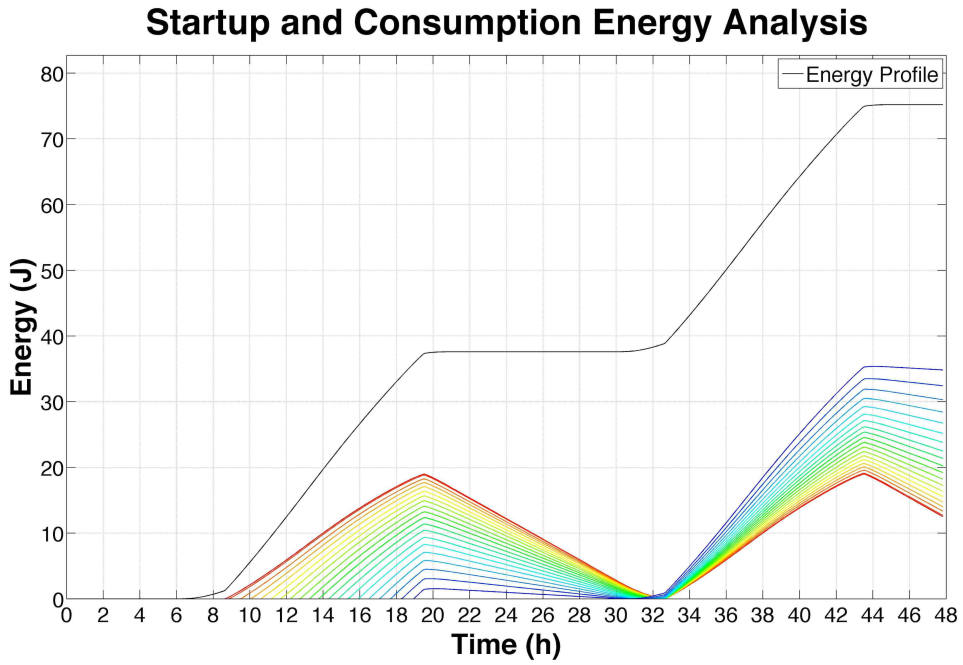


(a)

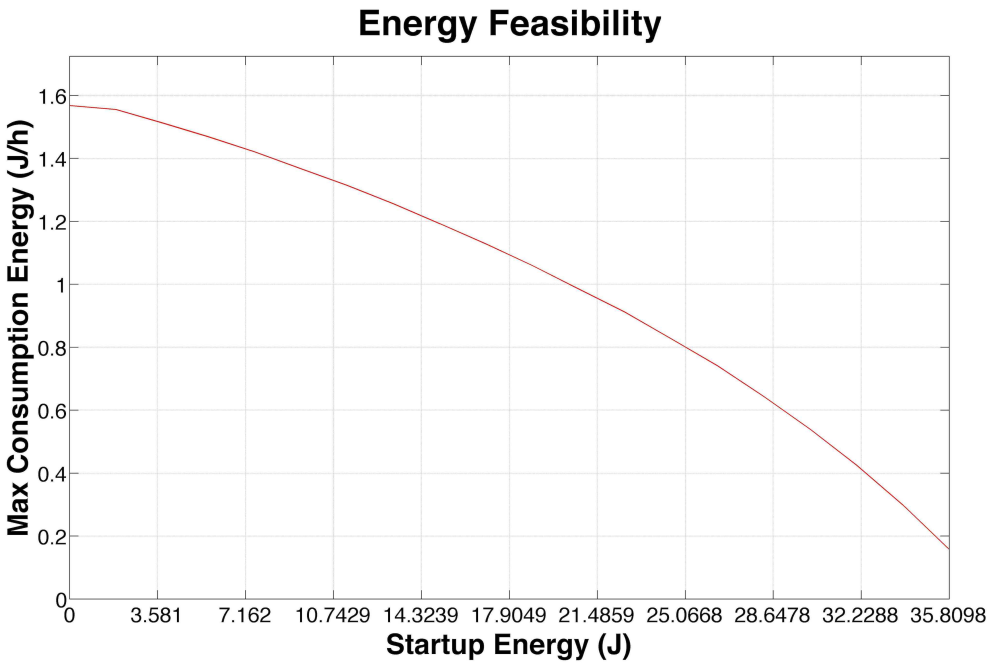


(b)

Figure D.6: Feasibility of the CYMBET CBC-PV-01N on 22nd of May of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

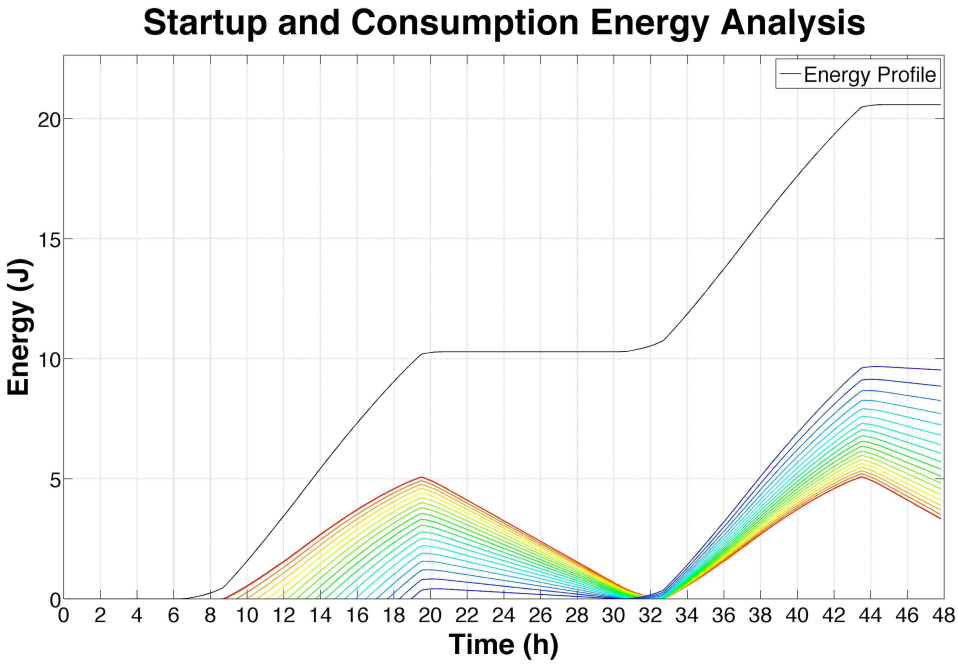


(a)

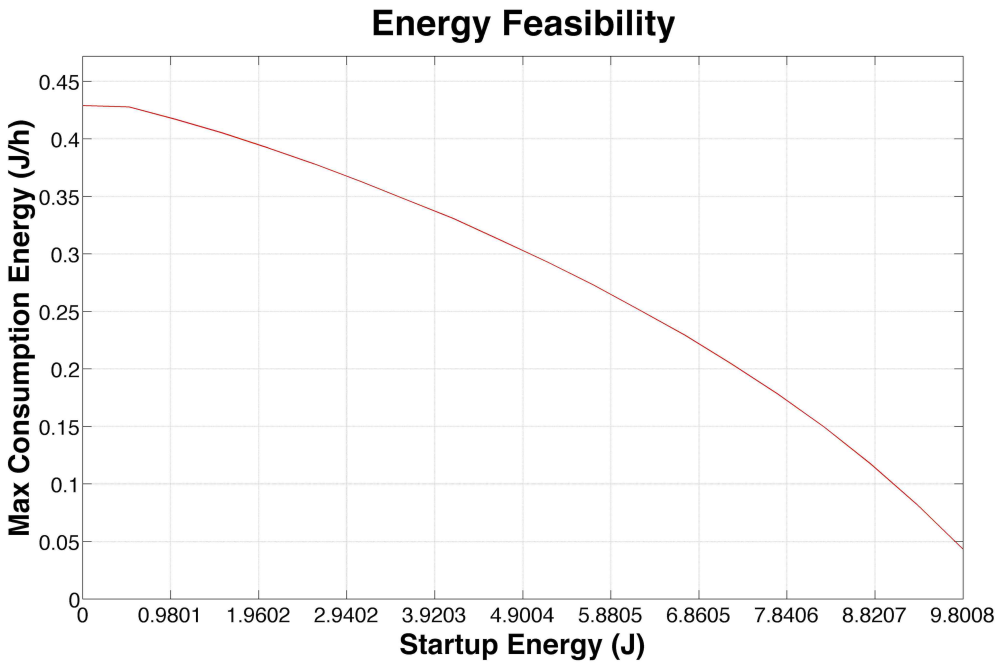


(b)

Figure D.7: Feasibility of the Amorton AM-1454 on 22nd of May of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

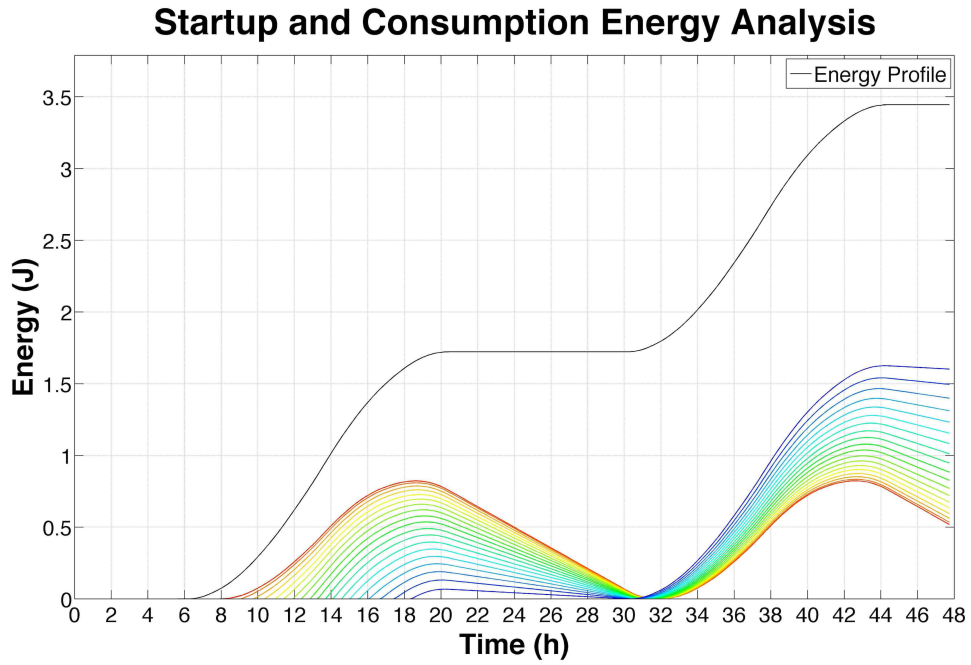


(a)

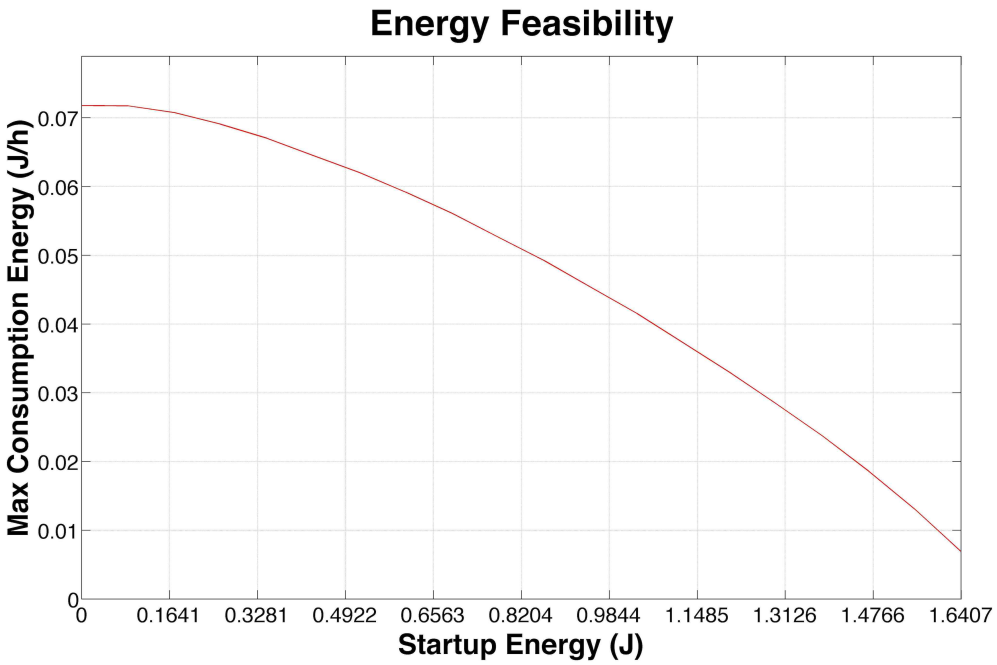


(b)

Figure D.8: Feasibility of the Amorton AM-1417 on 22nd of May of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

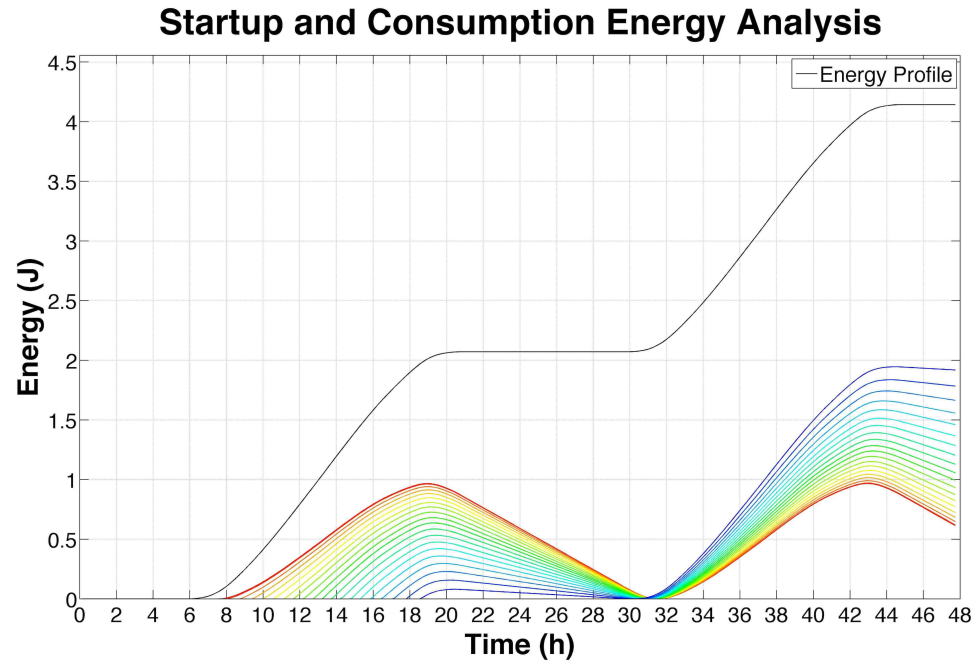


(a)

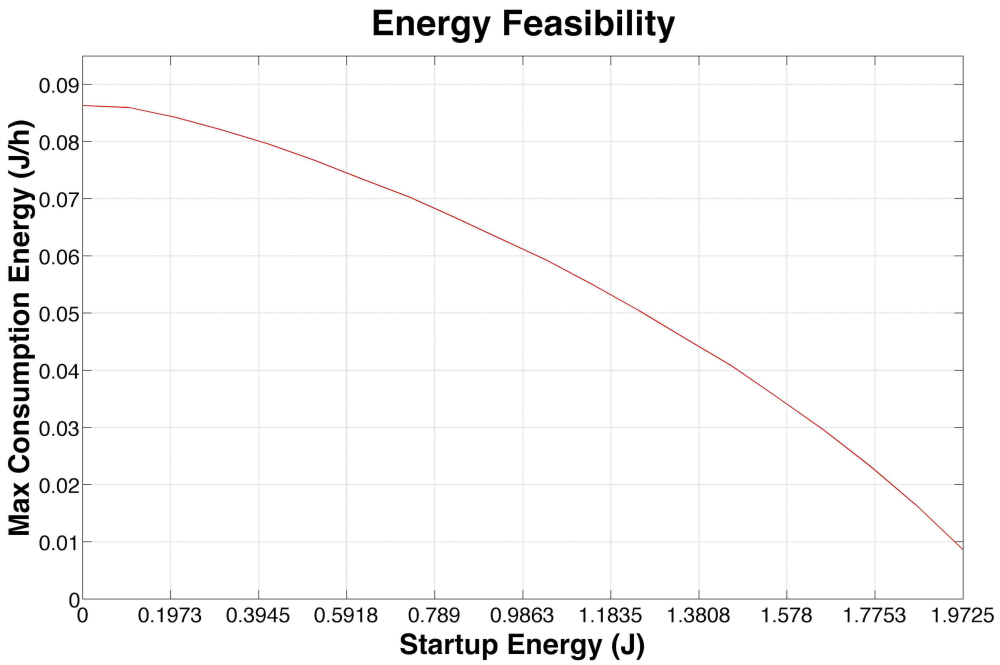


(b)

Figure D.9: Feasibility of the IXYS SLMD121H04L on 23rd of May of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

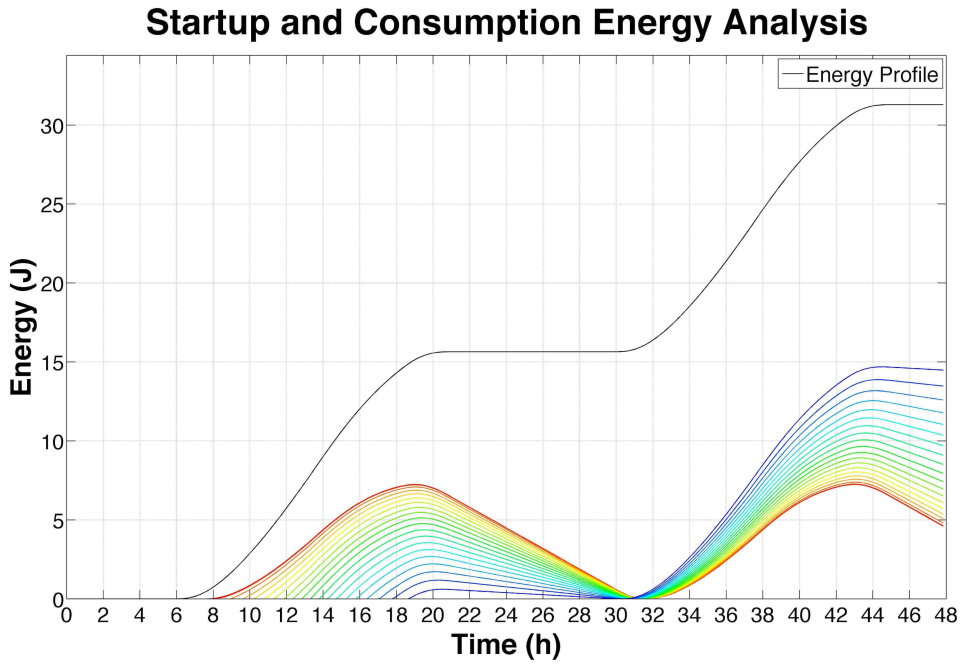


(a)

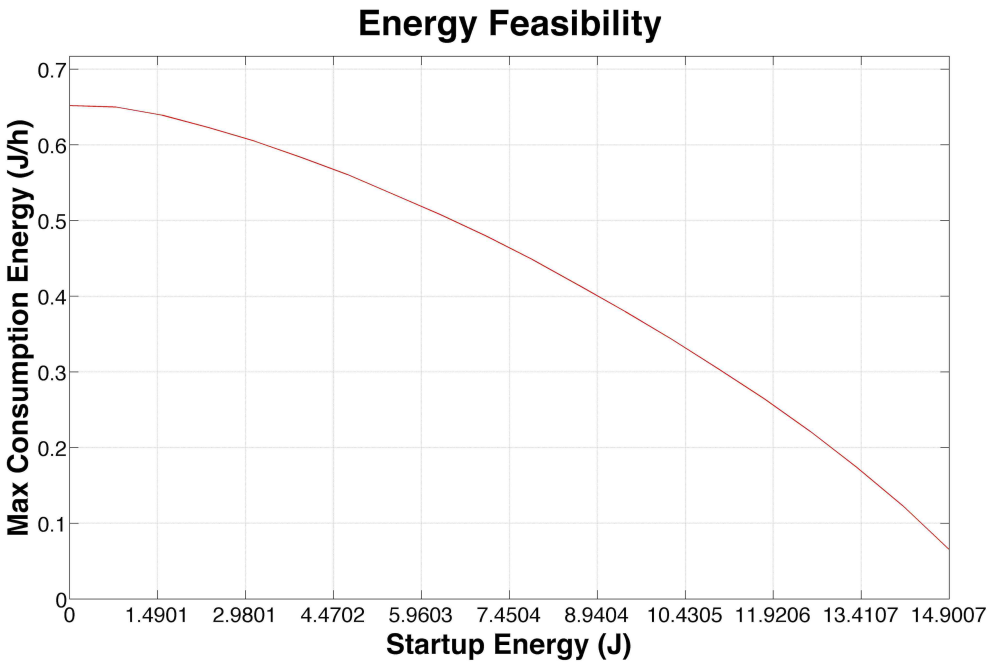


(b)

Figure D.10: Feasibility of the CYMBET CBC-PV-01N on 23rd of May of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

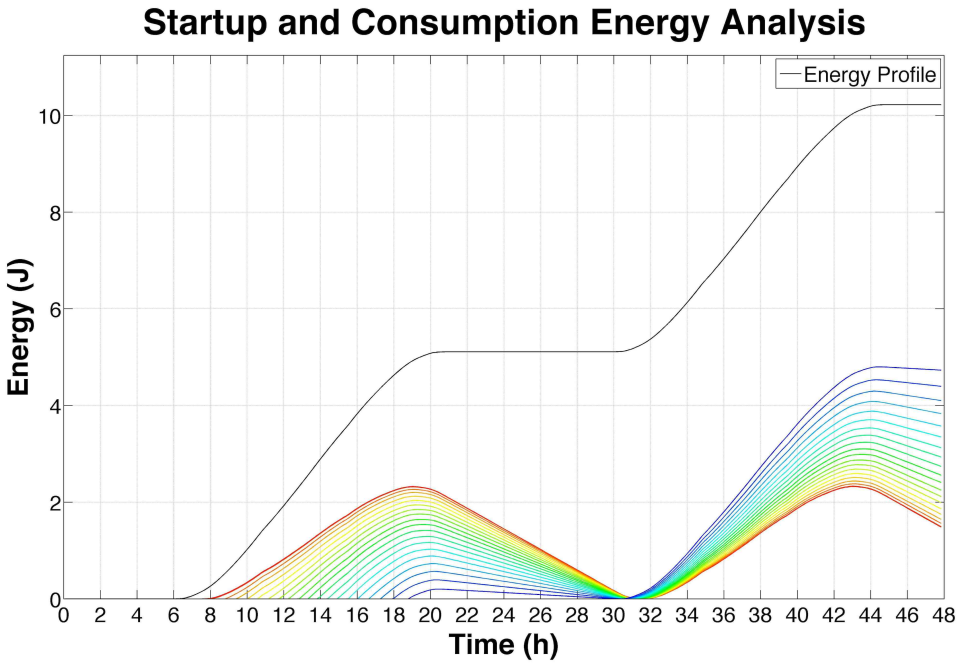


(a)

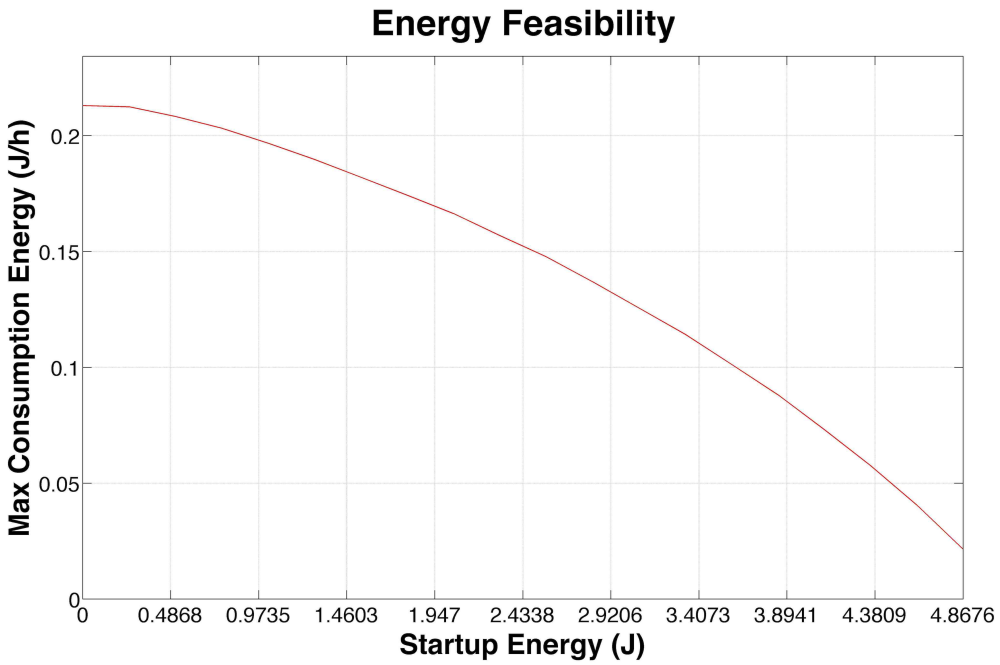


(b)

Figure D.11: Feasibility of the Amorton AM-1454 on 23rd of May of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

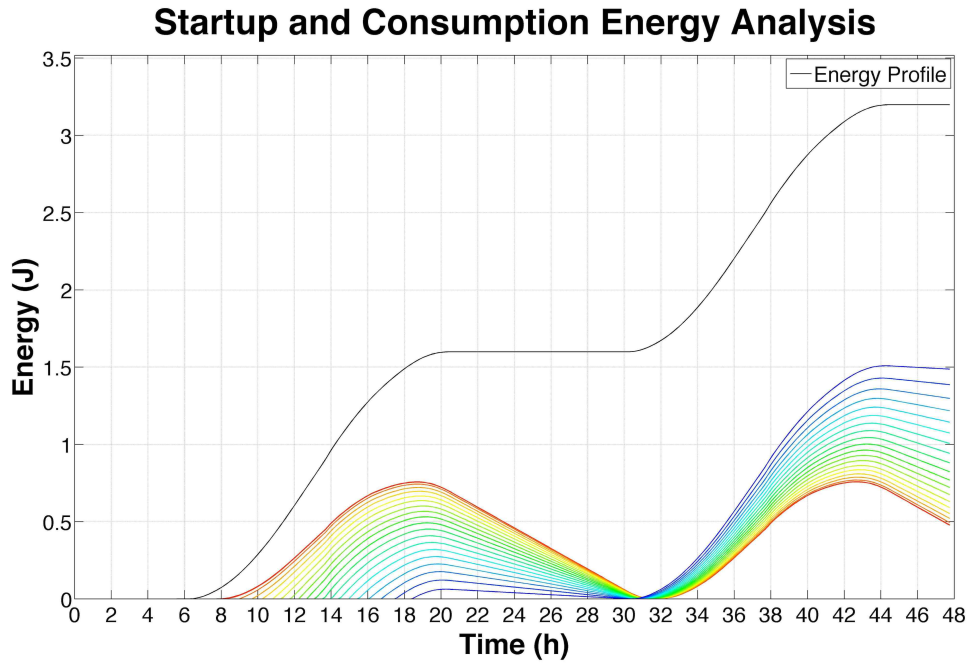


(a)

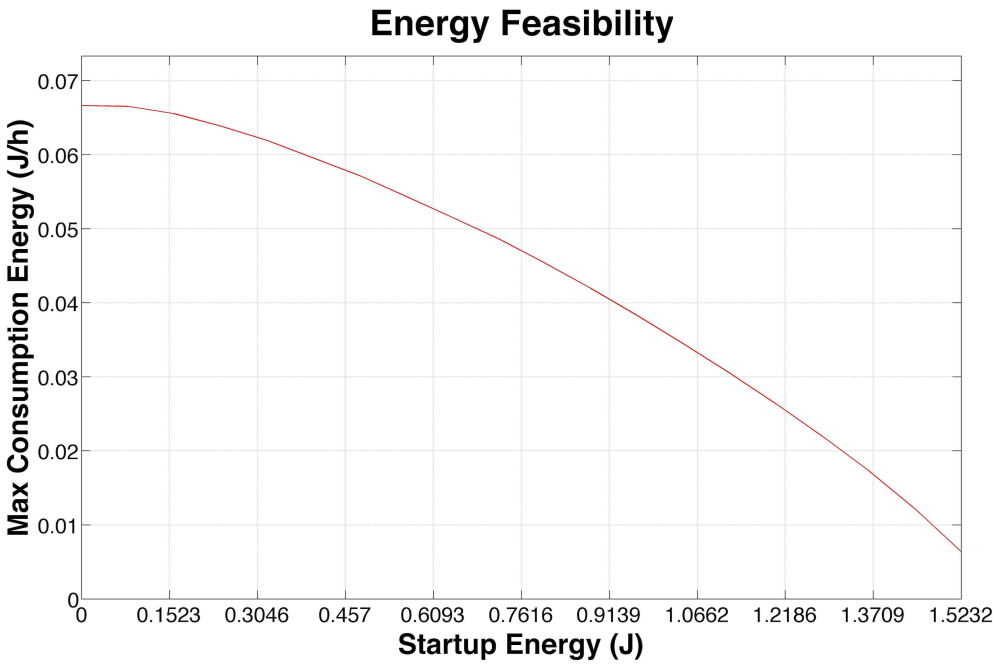


(b)

Figure D.12: Feasibility of the Amorton AM-1417 on 23rd of May of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

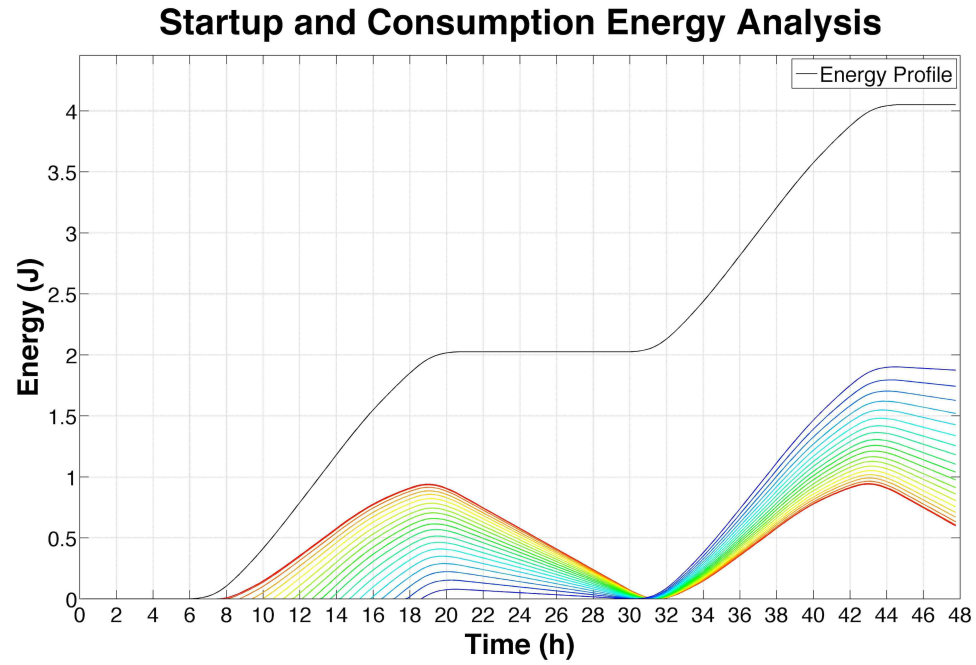


(a)

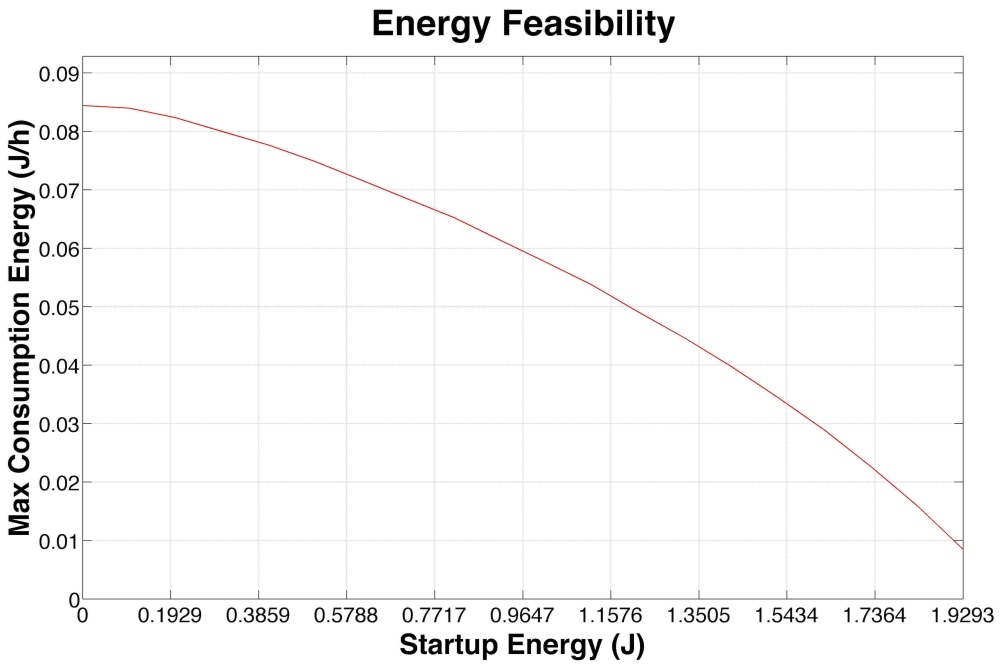


(b)

Figure D.13: Feasibility of the IXYS SLMD121H04L on 24th of May of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

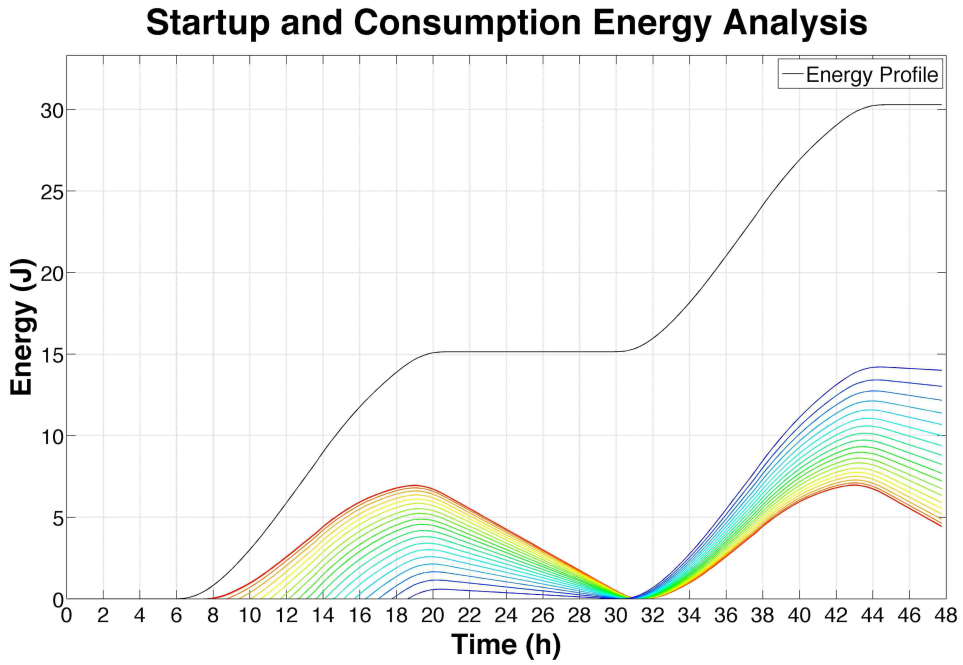


(a)

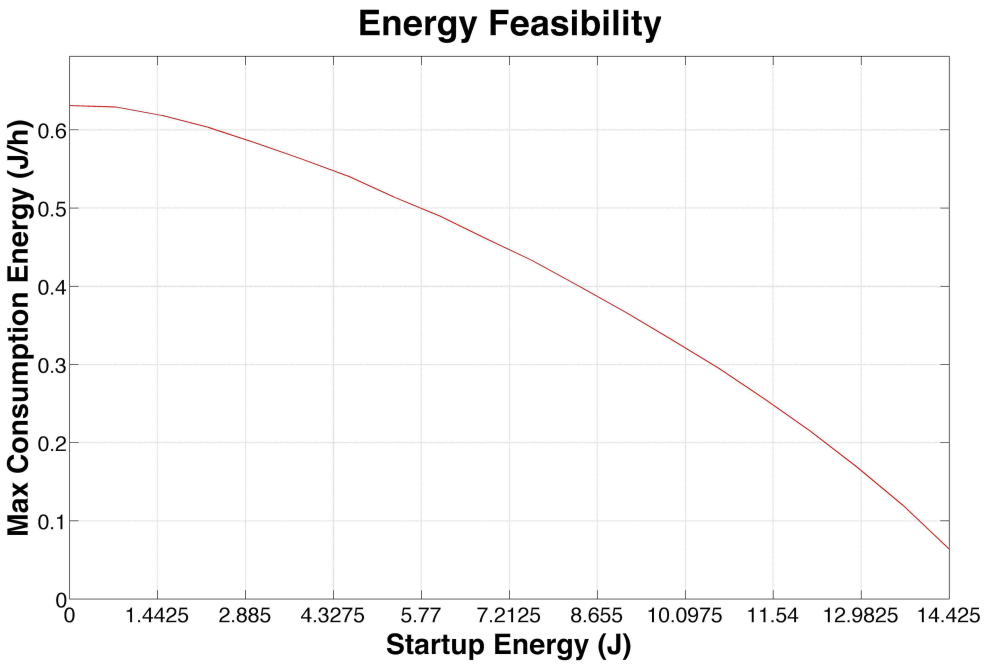


(b)

Figure D.14: Feasibility of the CYMBET CBC-PV-01N on 24th of May of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

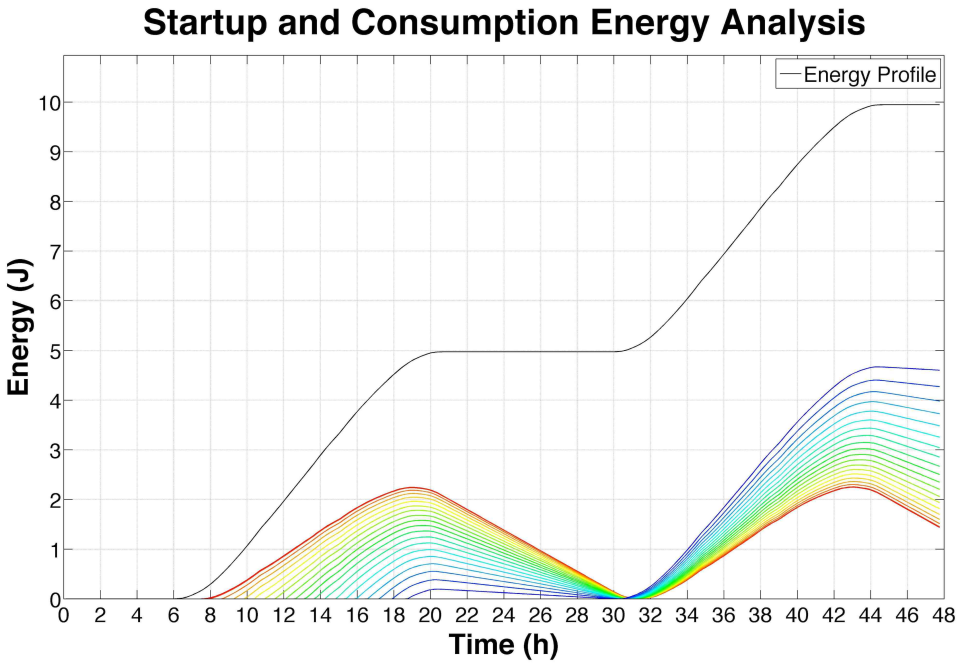


(a)

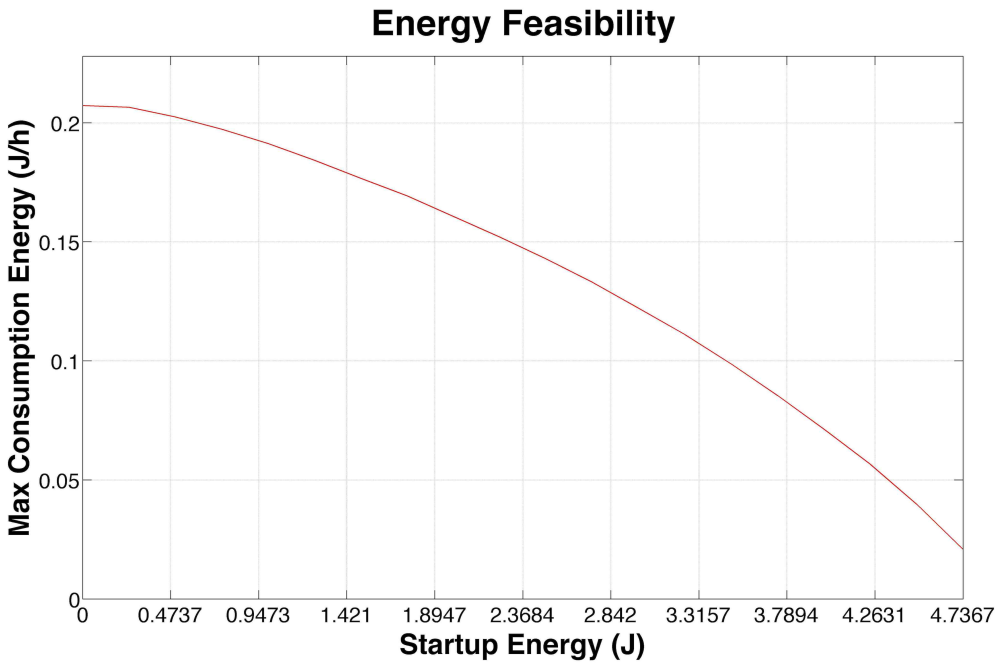


(b)

Figure D.15: Feasibility of the Amorton AM-1454 on 24th of May of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

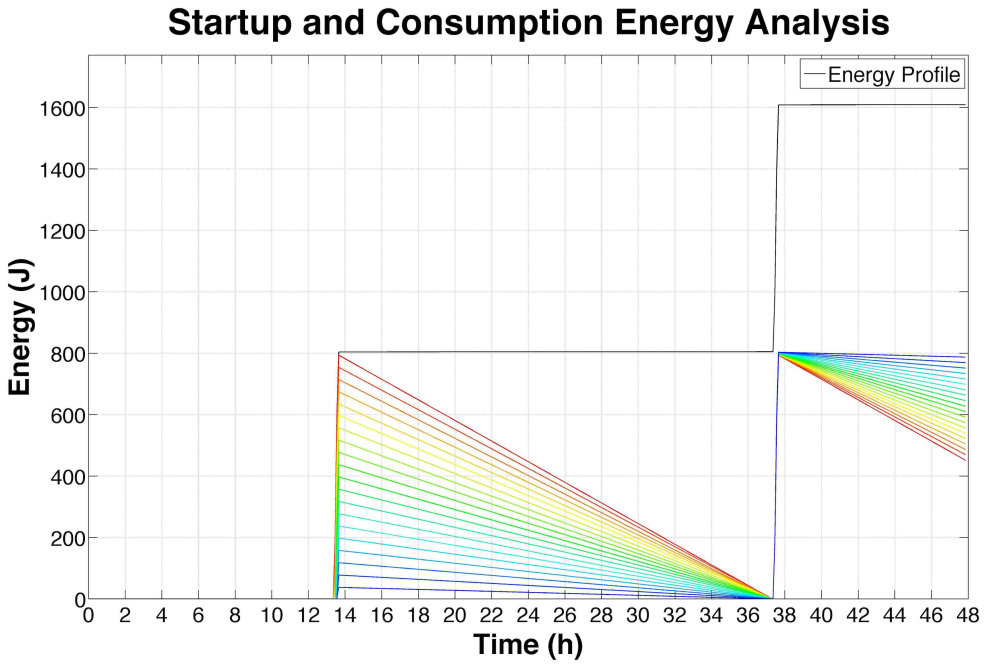


(a)

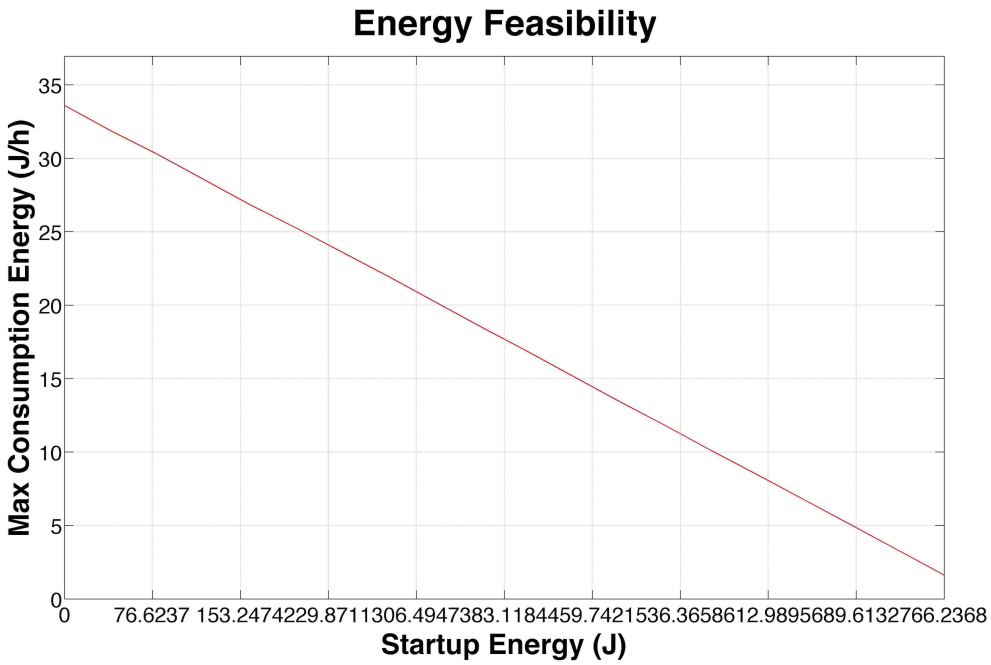


(b)

Figure D.16: Feasibility of the Amorton AM-1417 on 24th of May of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

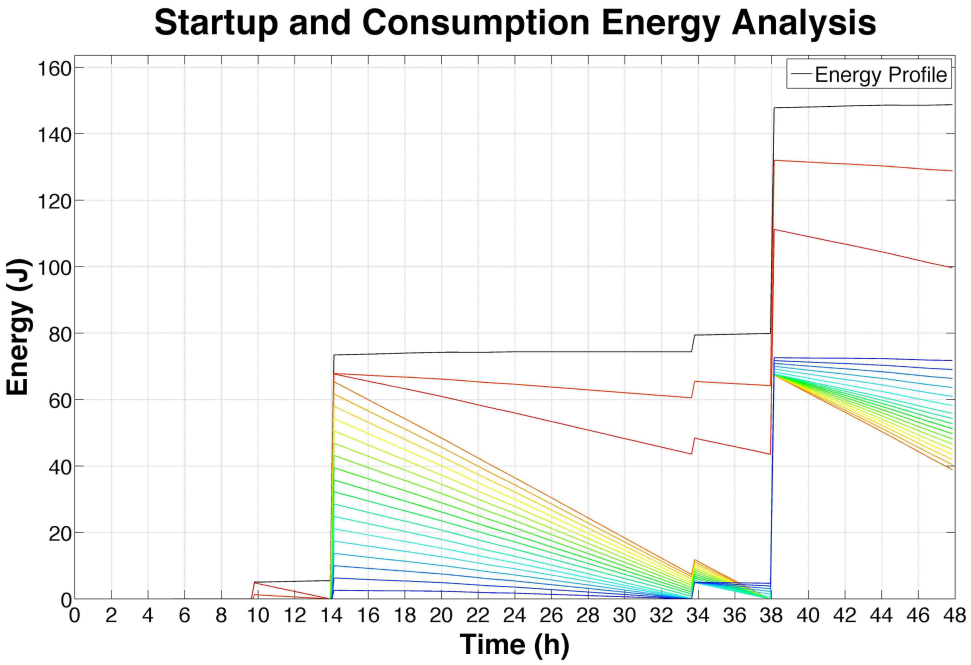


(a)

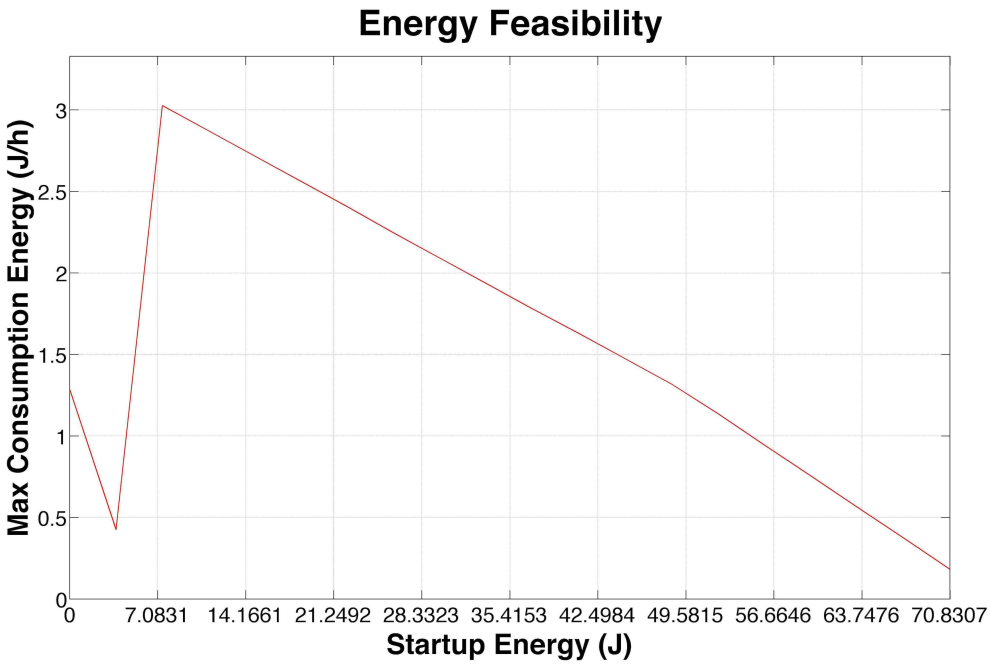


(b)

Figure D.17: Feasibility of the IXYS SLMD121H04L on 26th of May of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

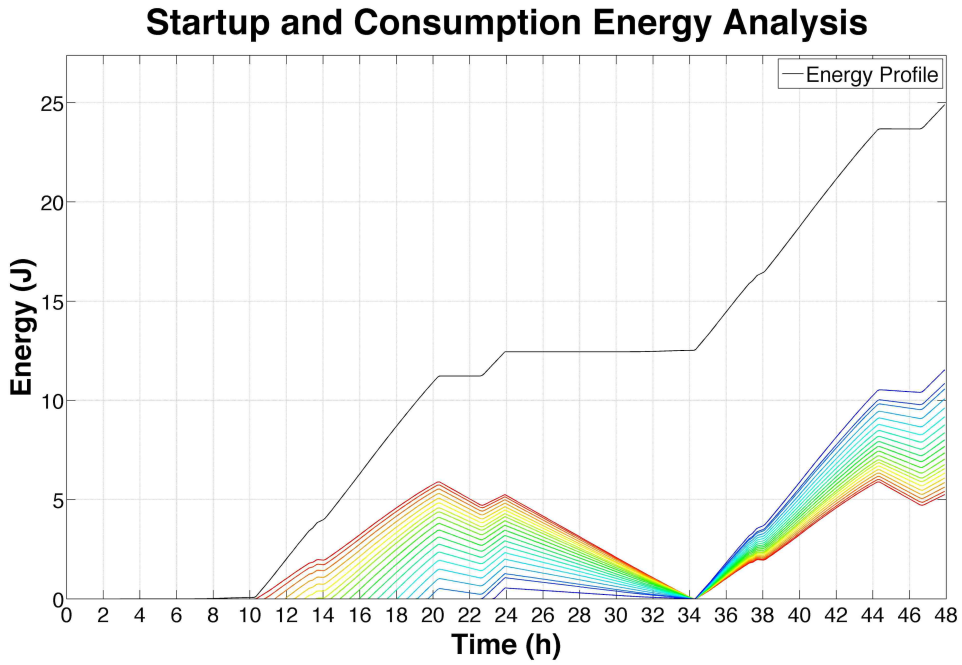


(a)

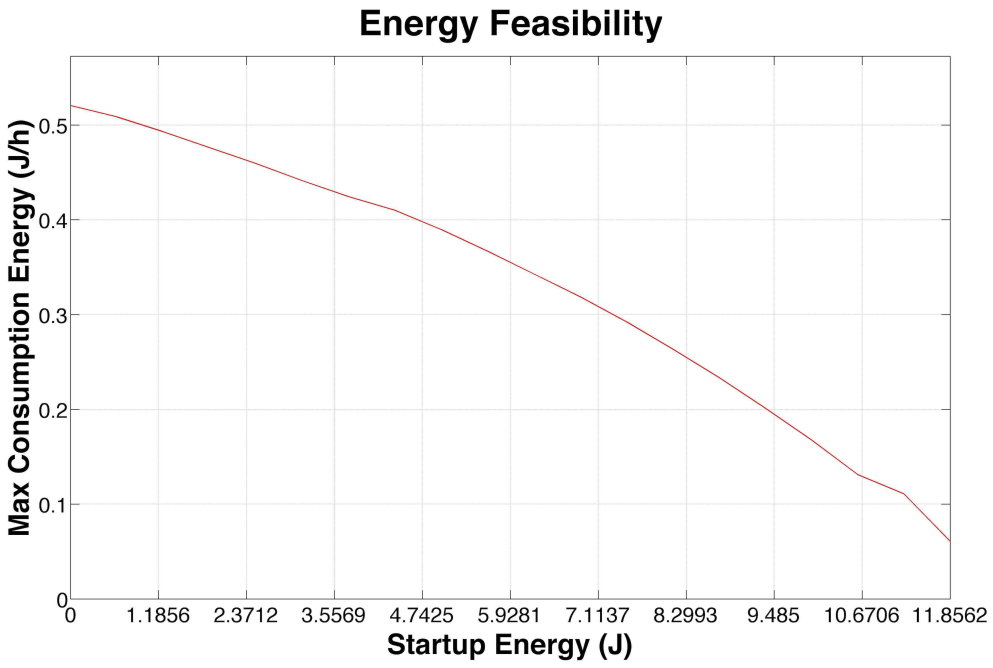


(b)

Figure D.18: Feasibility of the CYMBET CBC-PV-01N on 26th of May of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

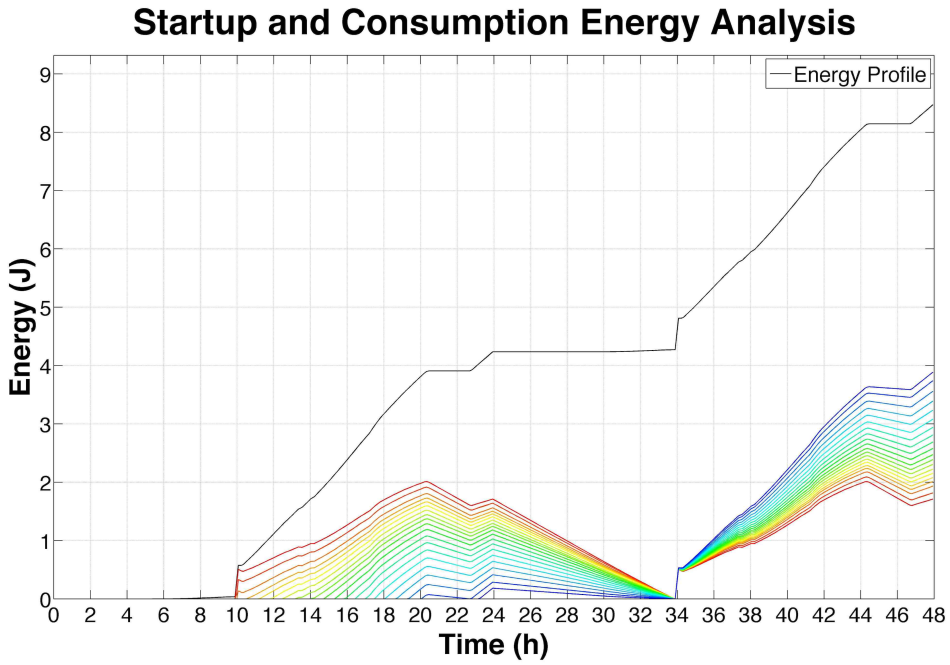


(a)

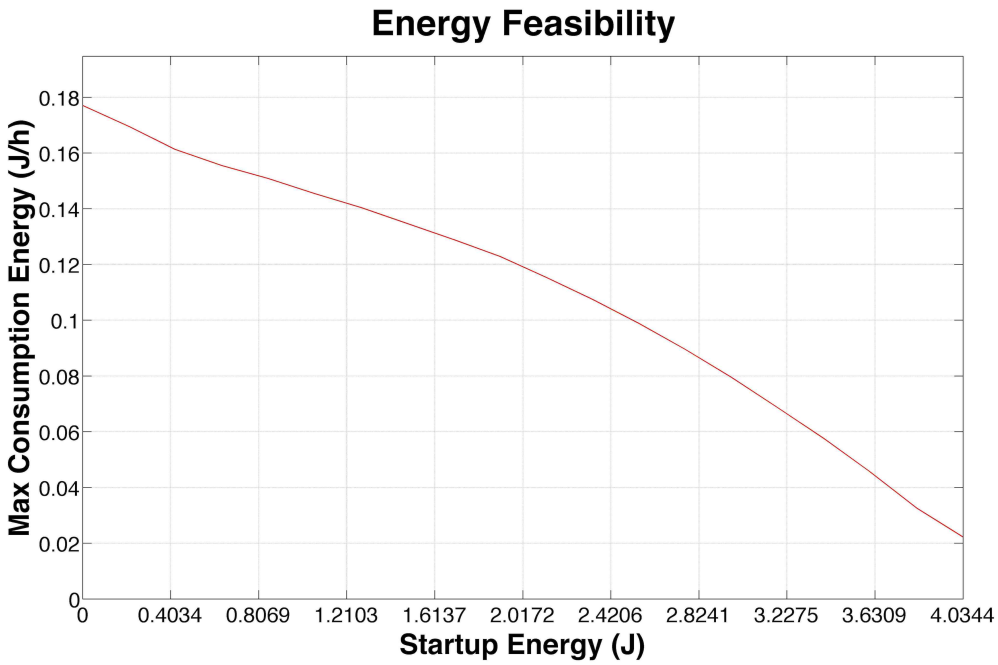


(b)

Figure D.19: Feasibility of the Amorton AM-1454 on 26th of May of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

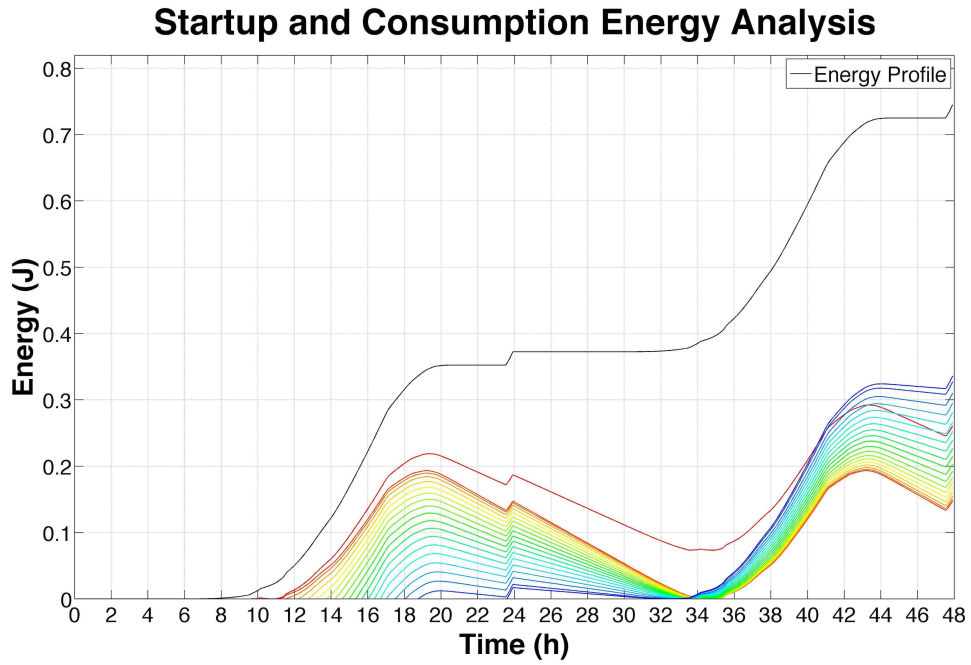


(a)

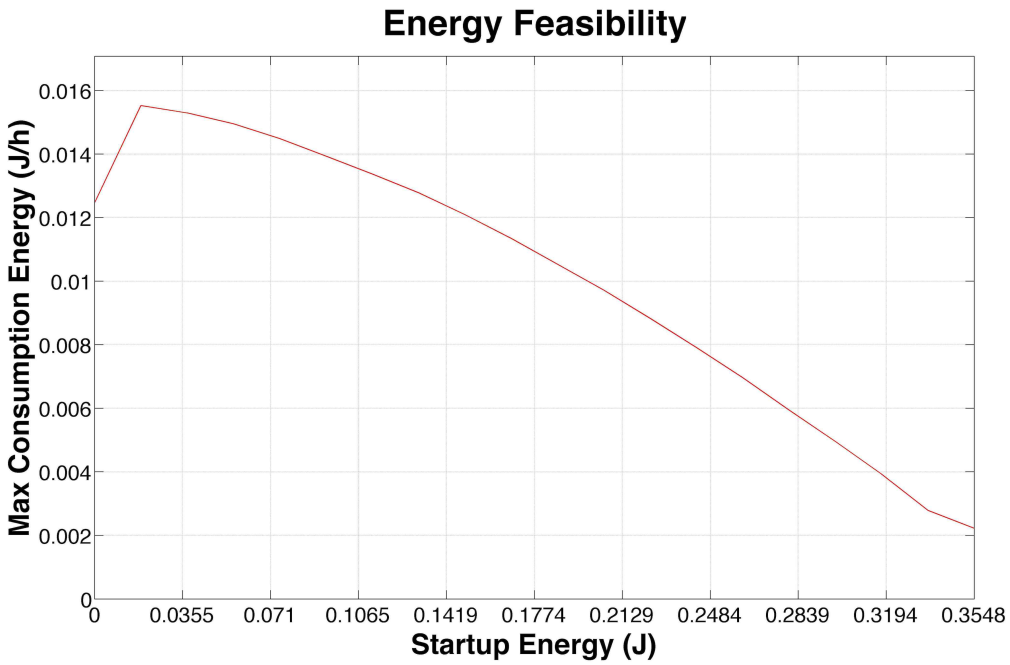


(b)

Figure D.20: Feasibility of the Amorton AM-1417 on 26th of May of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

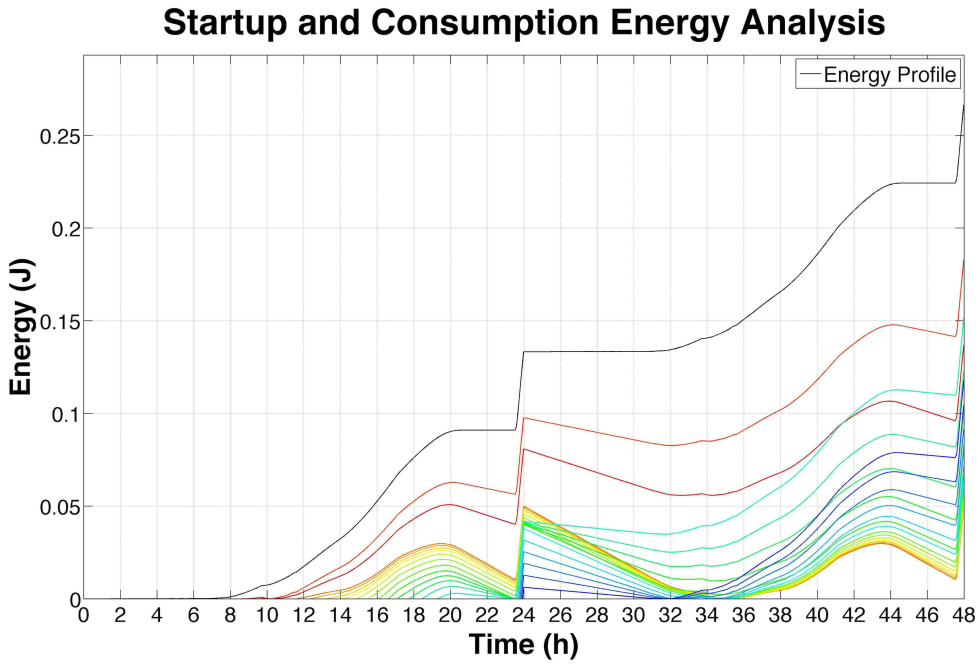


(a)

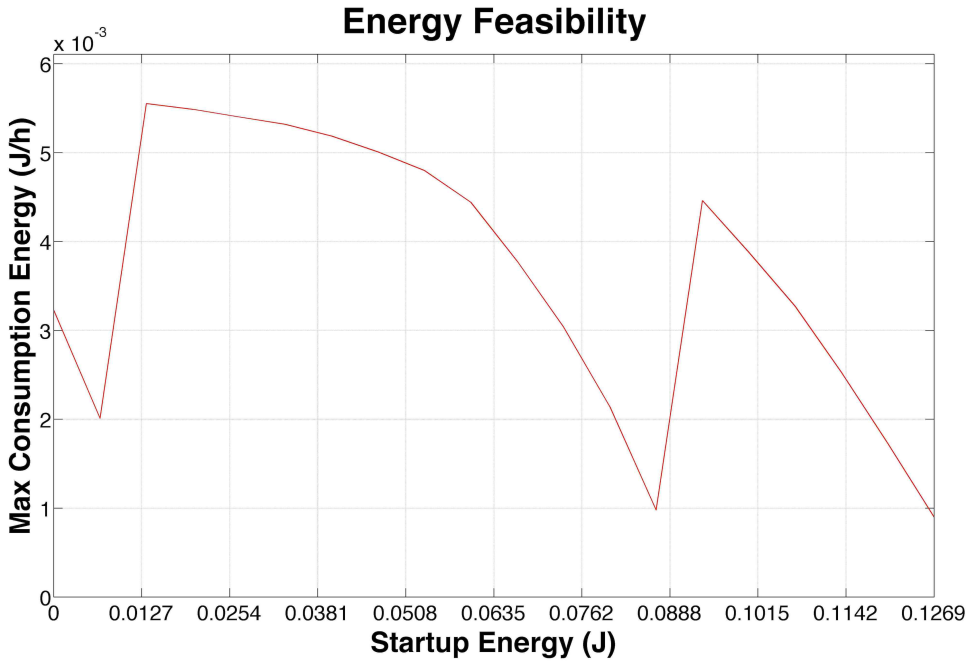


(b)

Figure D.21: Feasibility of the IXYS SLMD121H04L on 6th of June of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

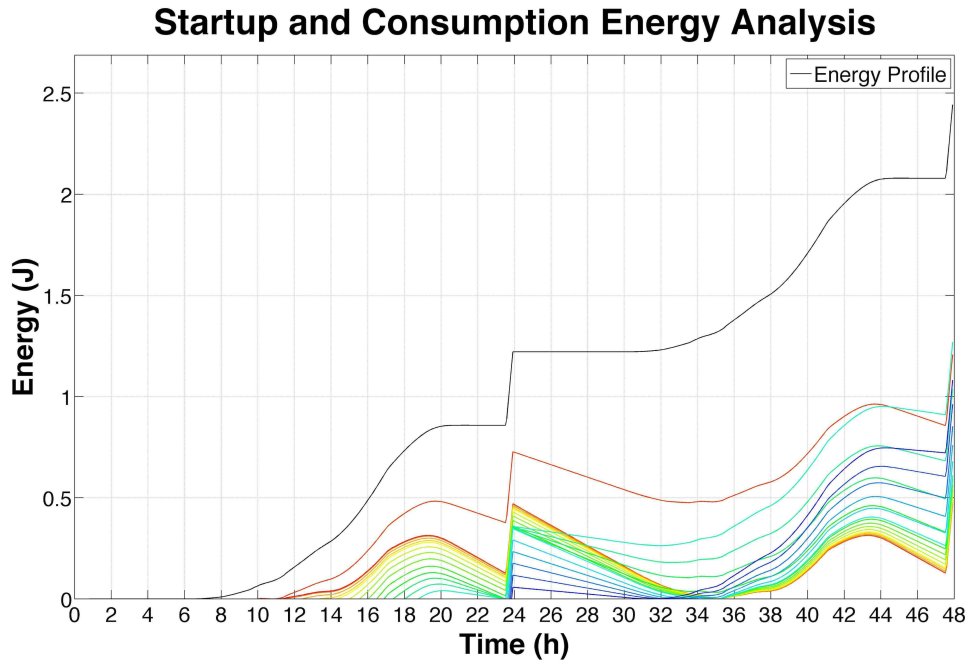


(a)

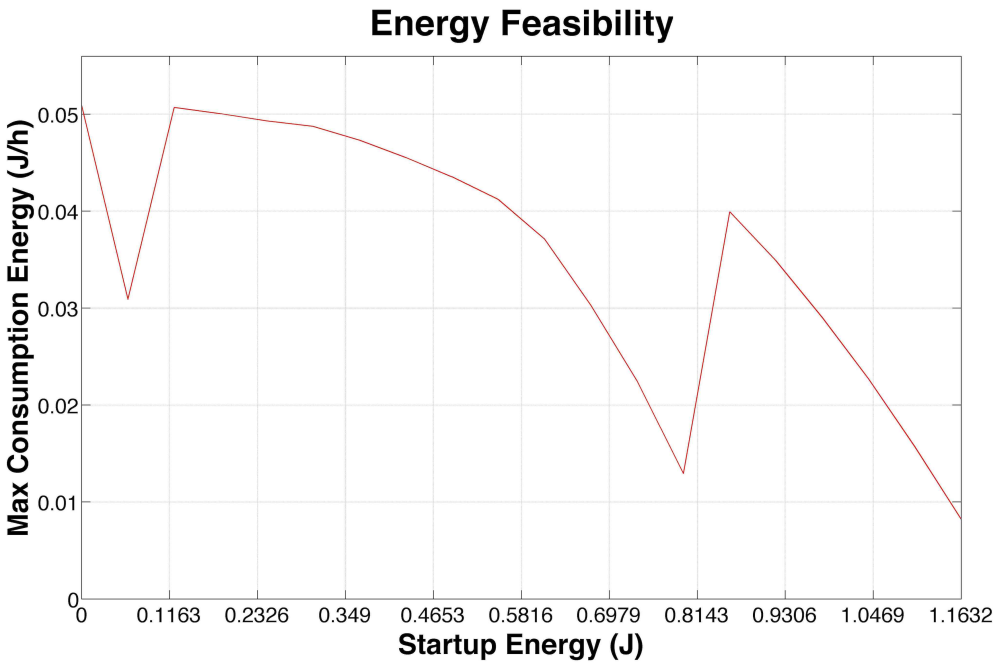


(b)

Figure D.22: Feasibility of the CYMBET CBC-PV-01N on 6th of June of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

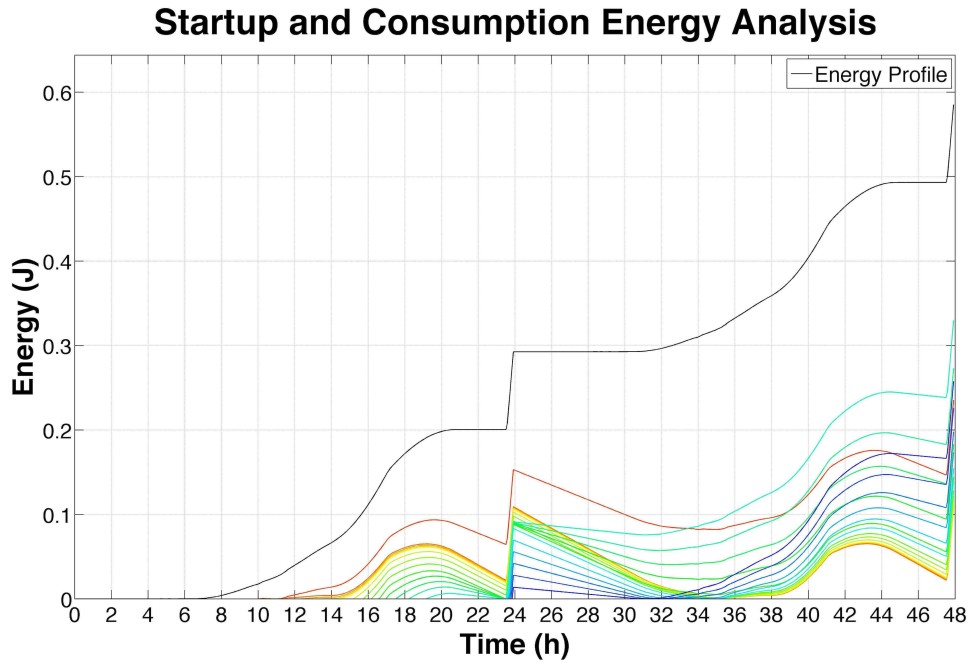


(a)

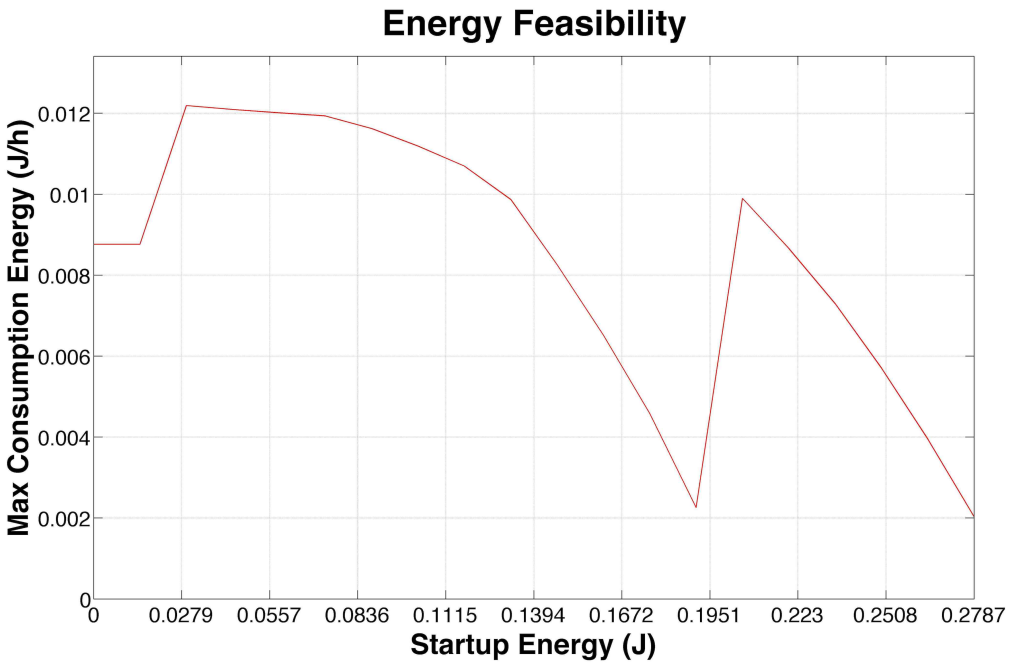


(b)

Figure D.23: Feasibility of the Amorton AM-1454 on 6th of June of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

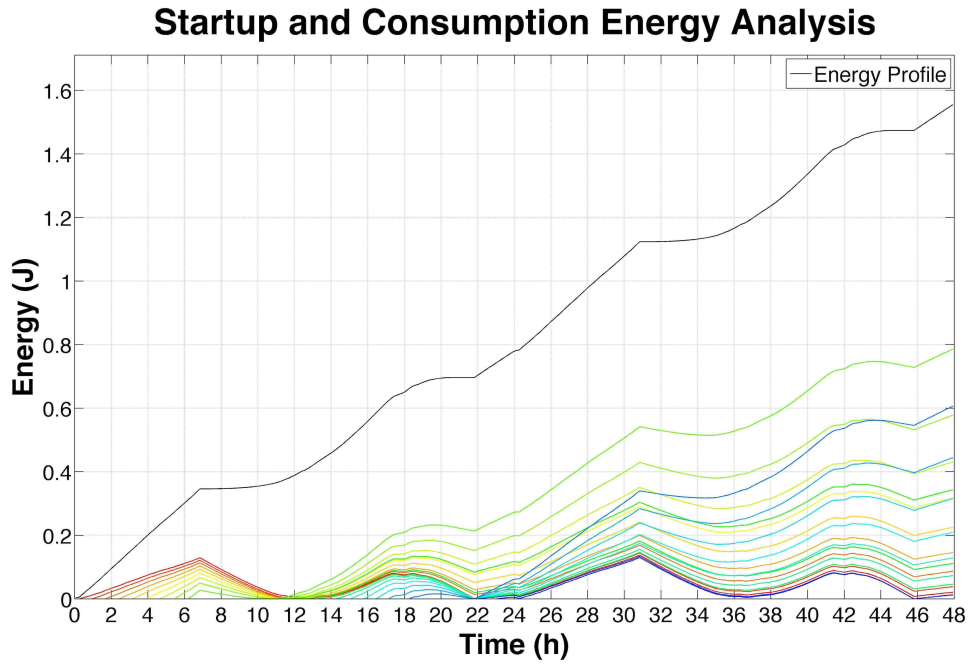


(a)

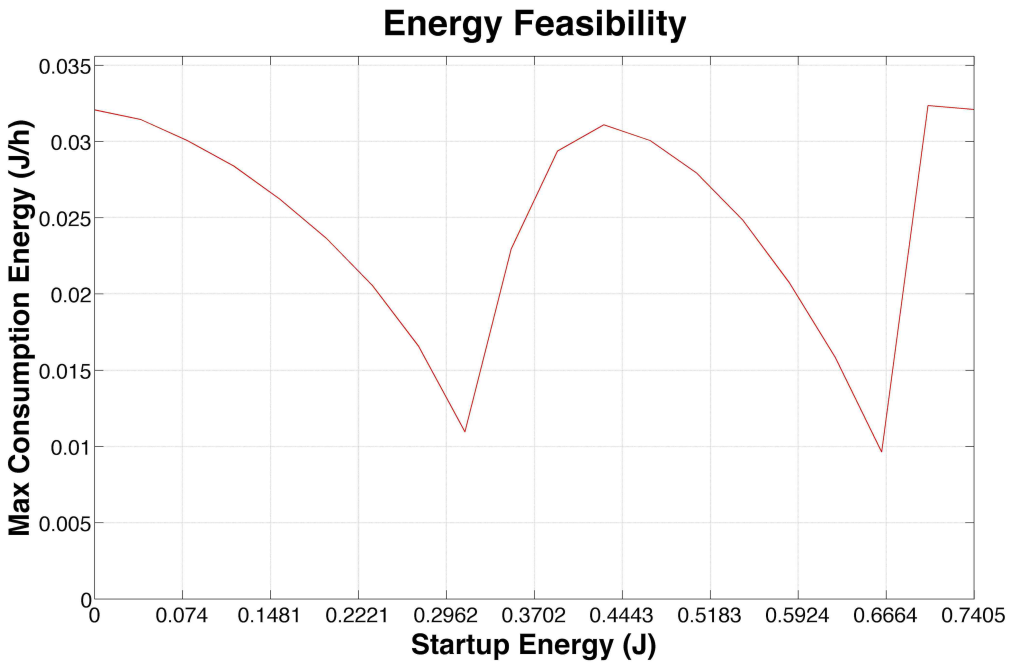


(b)

Figure D.24: Feasibility of the Amorton AM-1417 on 6th of June of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

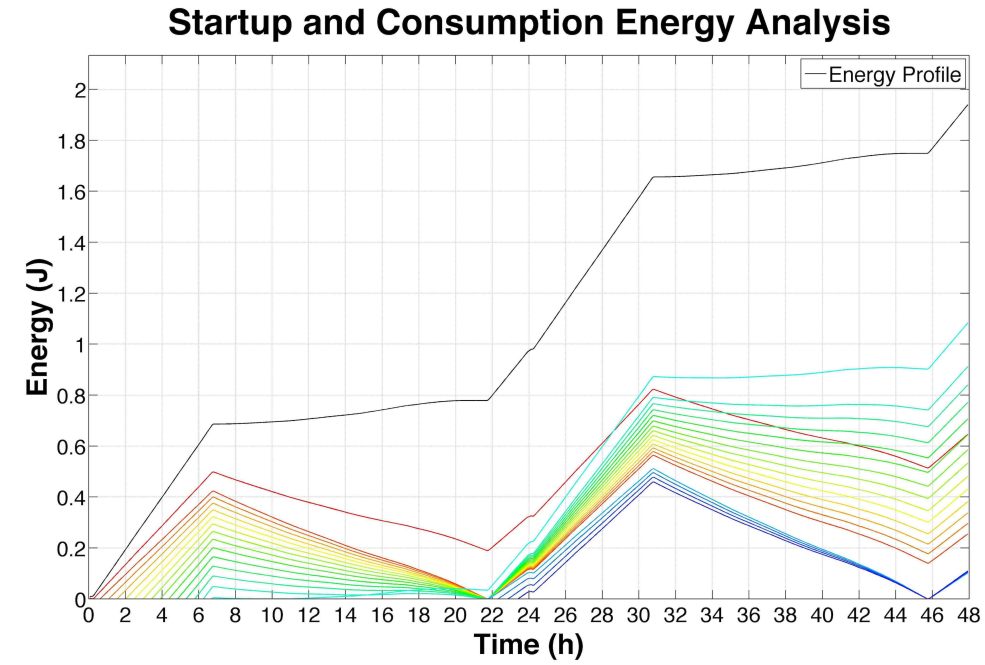


(a)

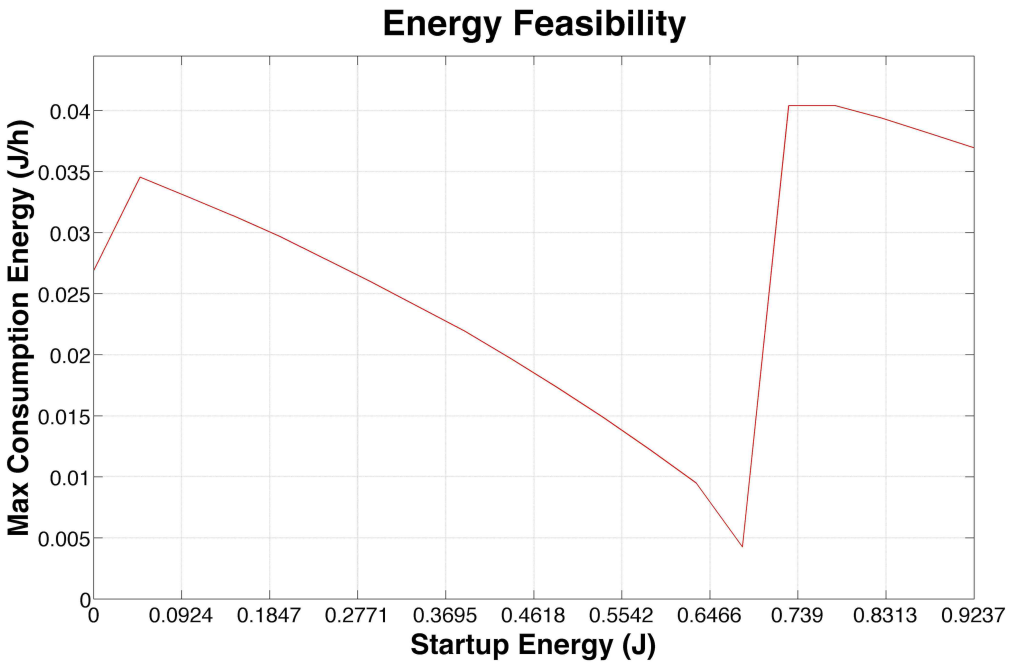


(b)

Figure D.25: Feasibility of the IXYS SLMD121H04L on 7th of June of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

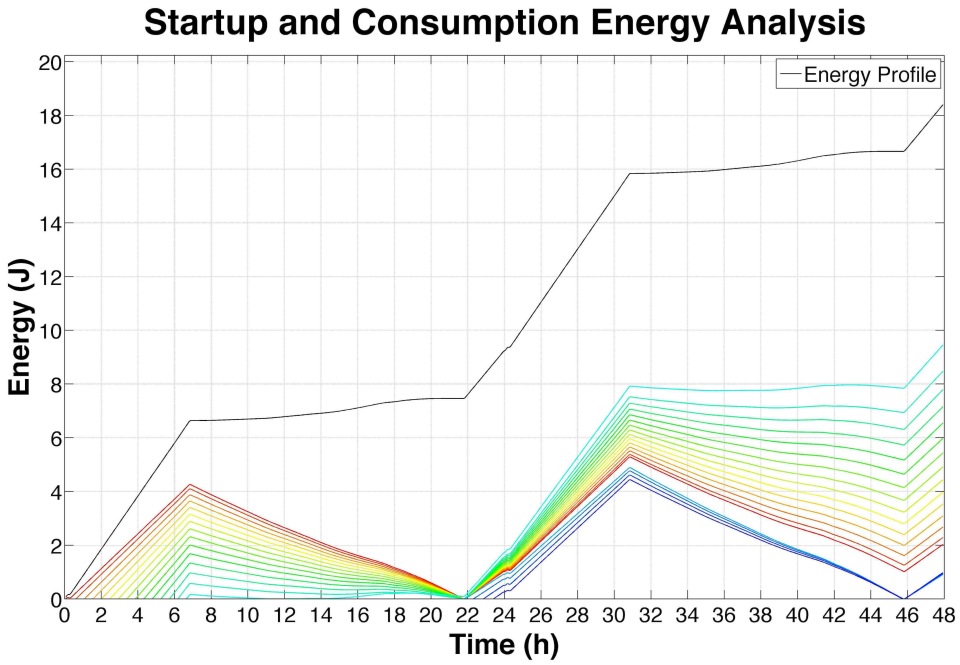


(a)

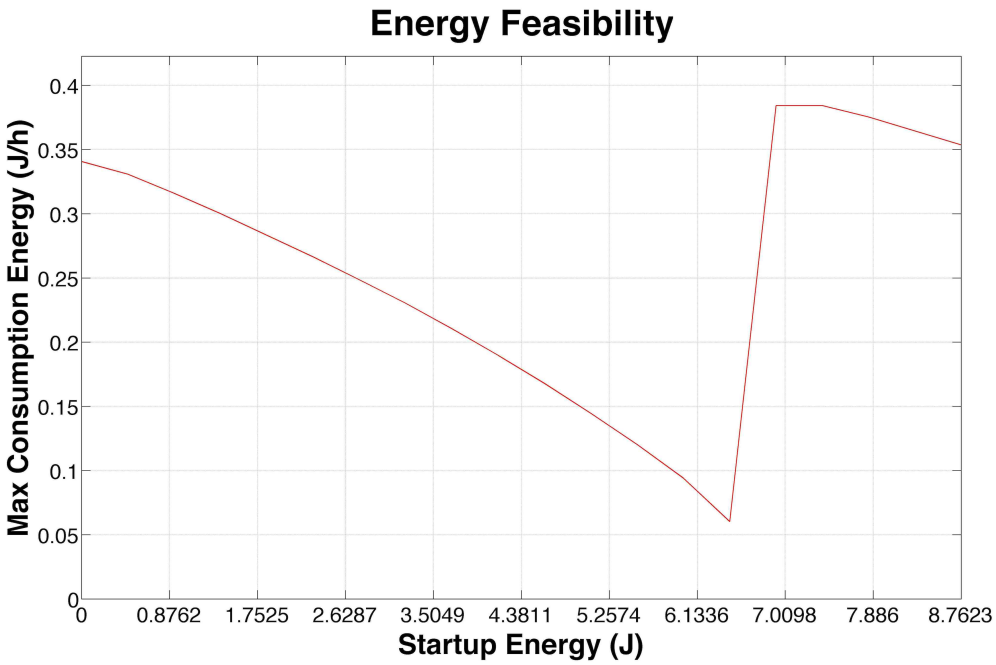


(b)

Figure D.26: Feasibility of the CYMBET CBC-PV-01N on 7th of June of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

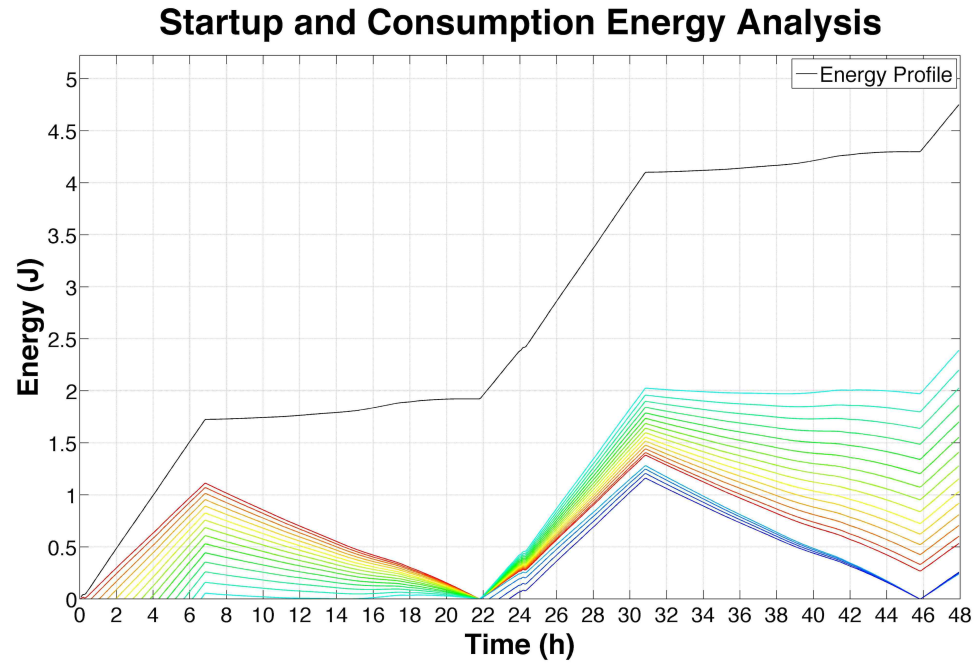


(a)

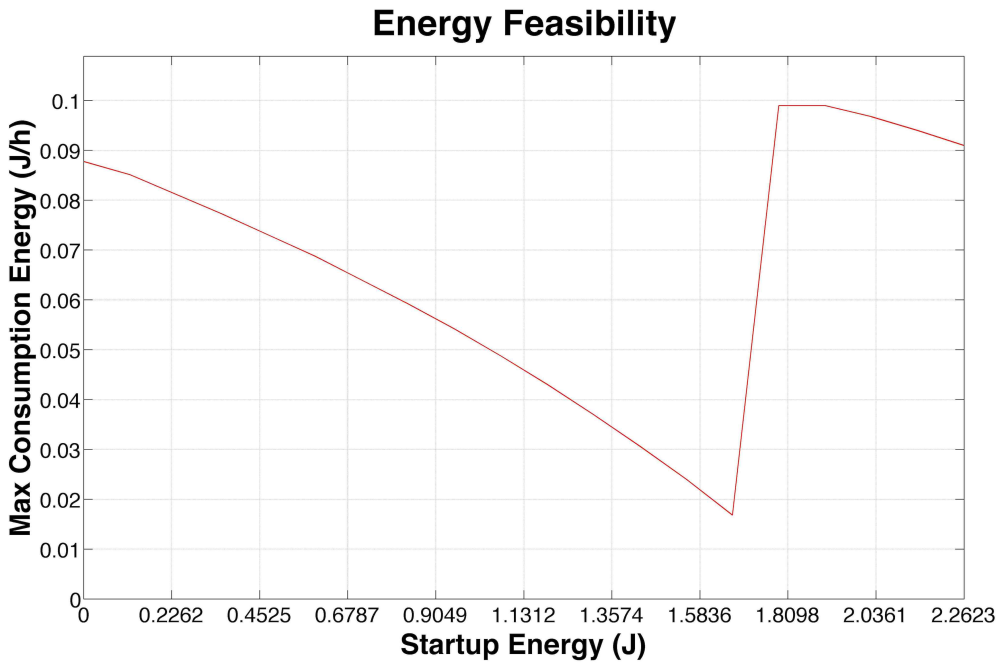


(b)

Figure D.27: Feasibility of the Amorton AM-1454 on 7th of June of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

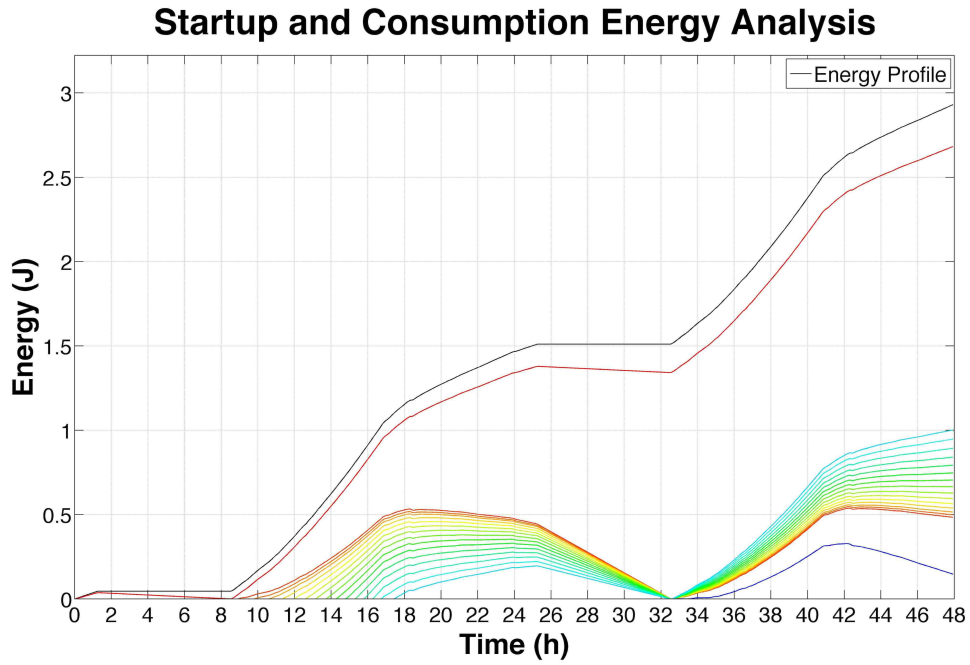


(a)

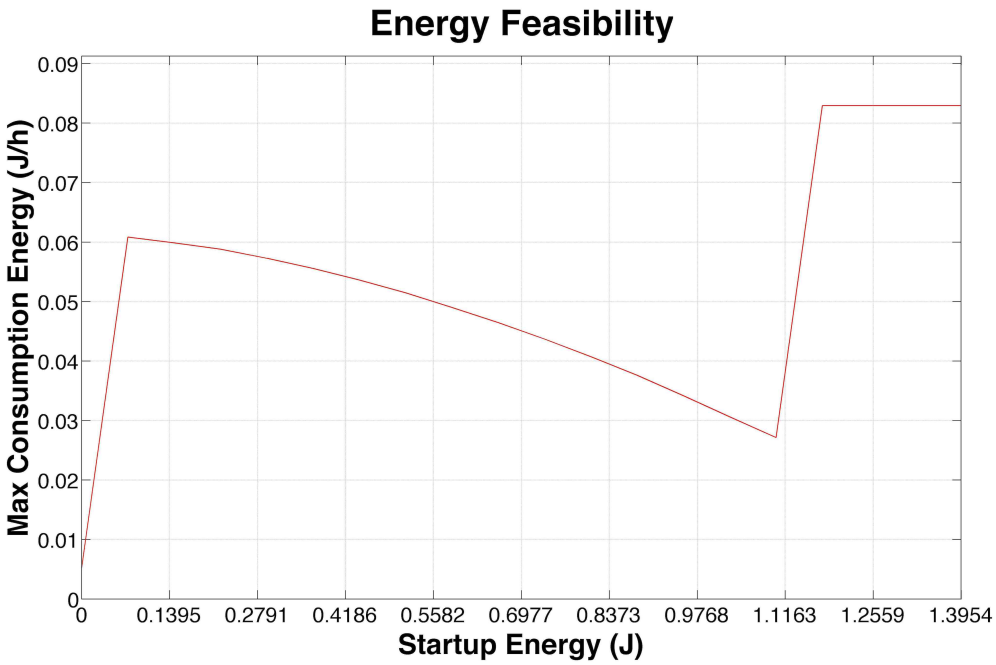


(b)

Figure D.28: Feasibility of the Amorton AM-1417 on 7th of June of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

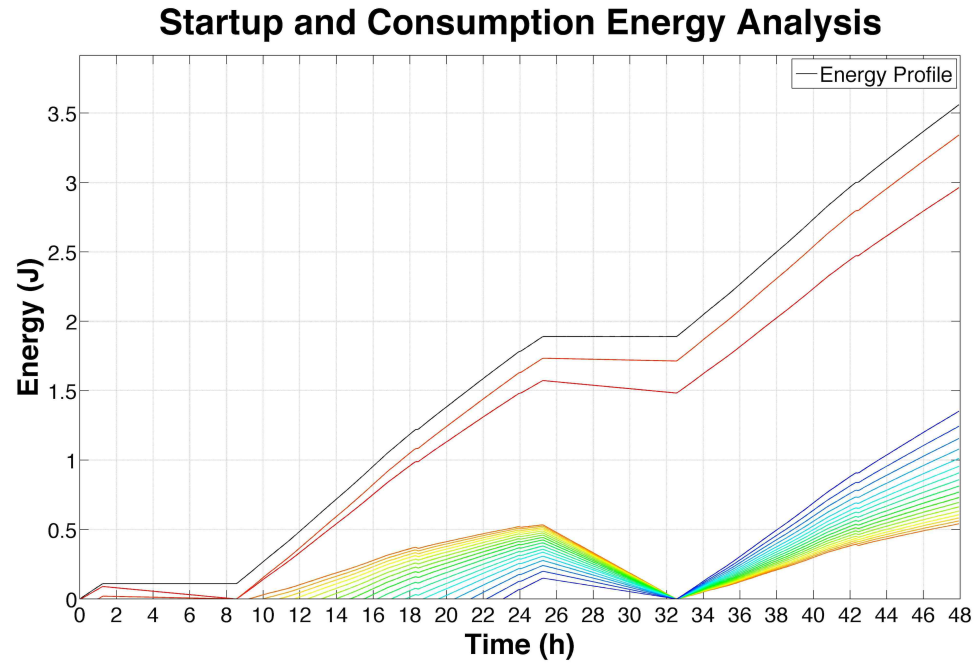


(a)

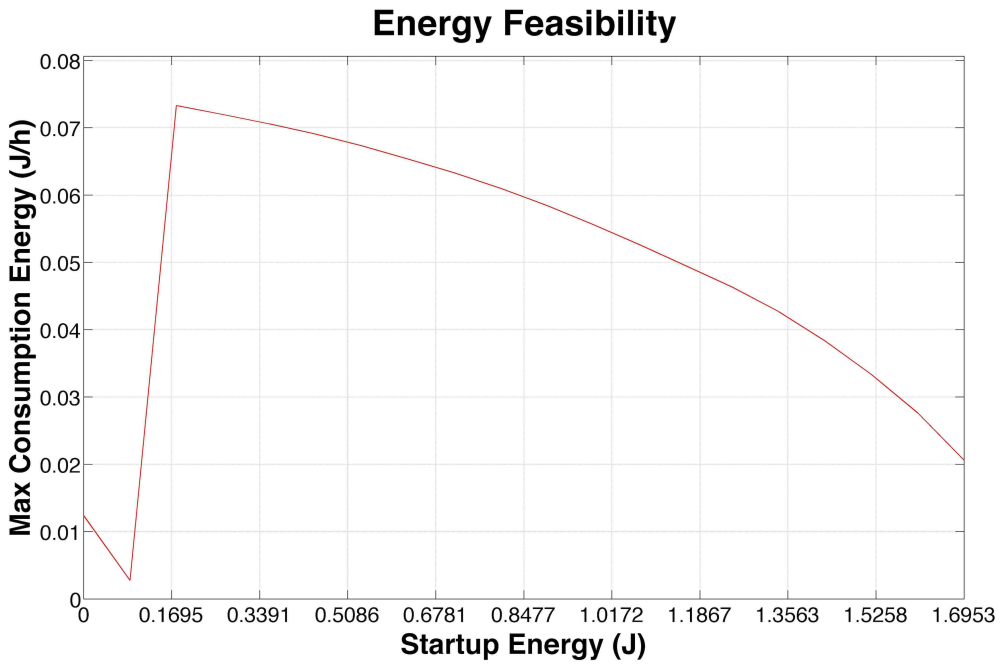


(b)

Figure D.29: Feasibility of the IXYS SLMD121H04L on 8th of June of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

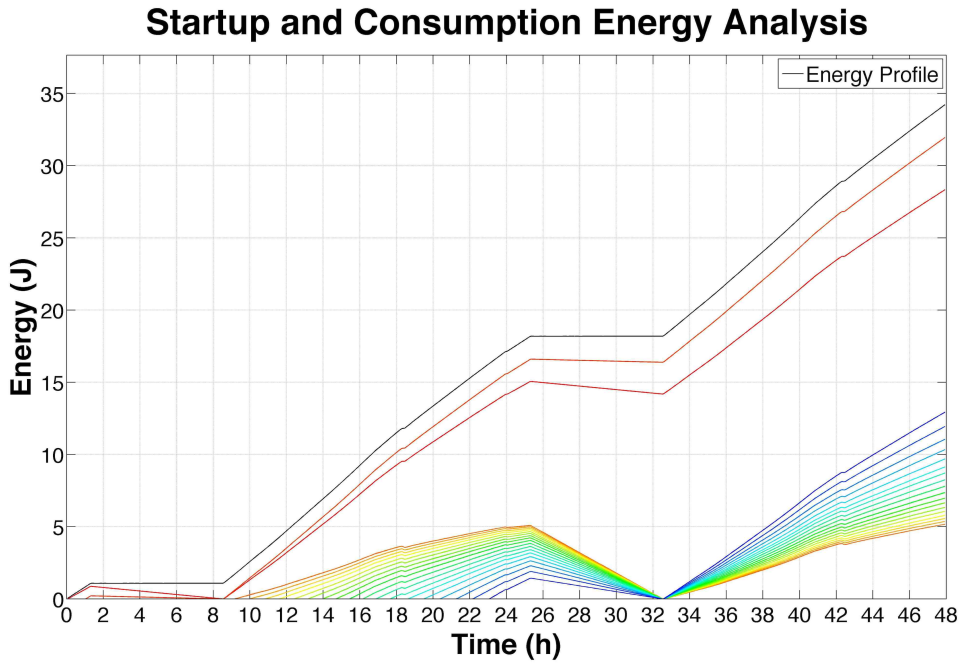


(a)

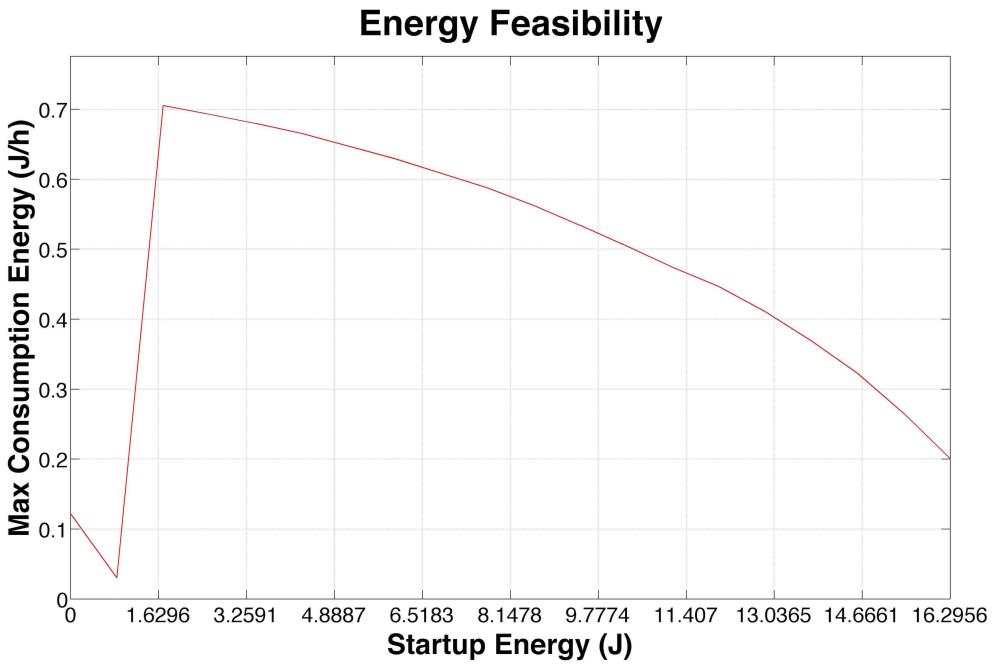


(b)

Figure D.30: Feasibility of the CYMBET CBC-PV-01N on 8th of June of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

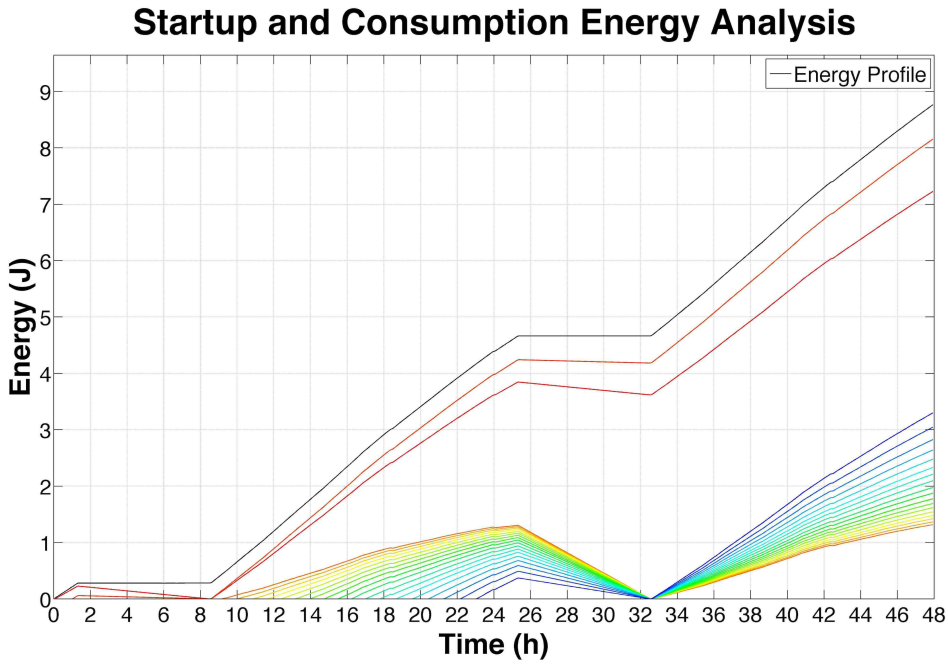


(a)

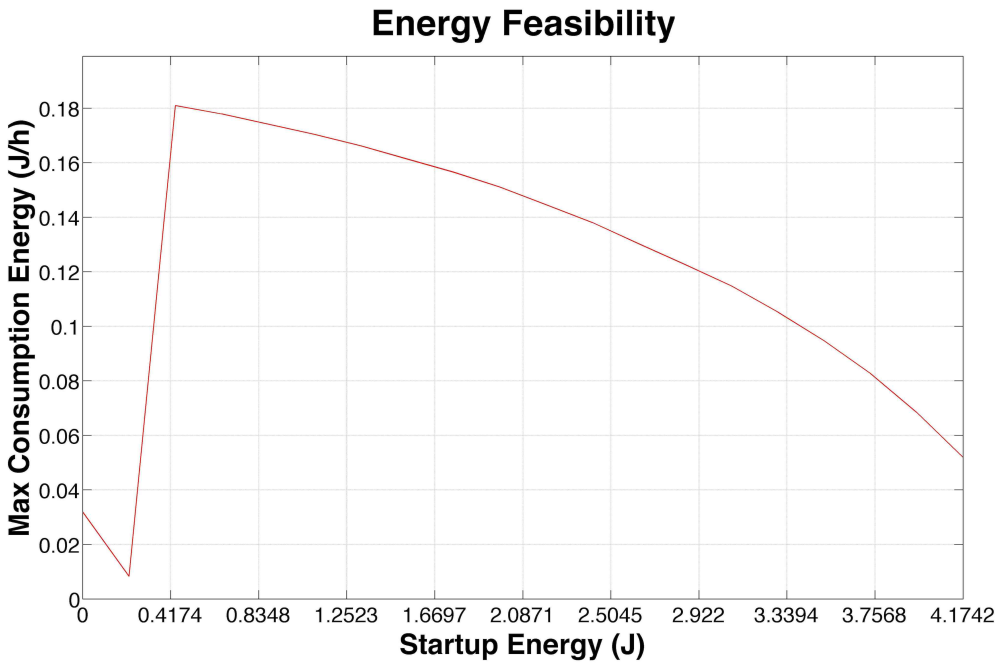


(b)

Figure D.31: Feasibility of the Amorton AM-1454 on 8th of June of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

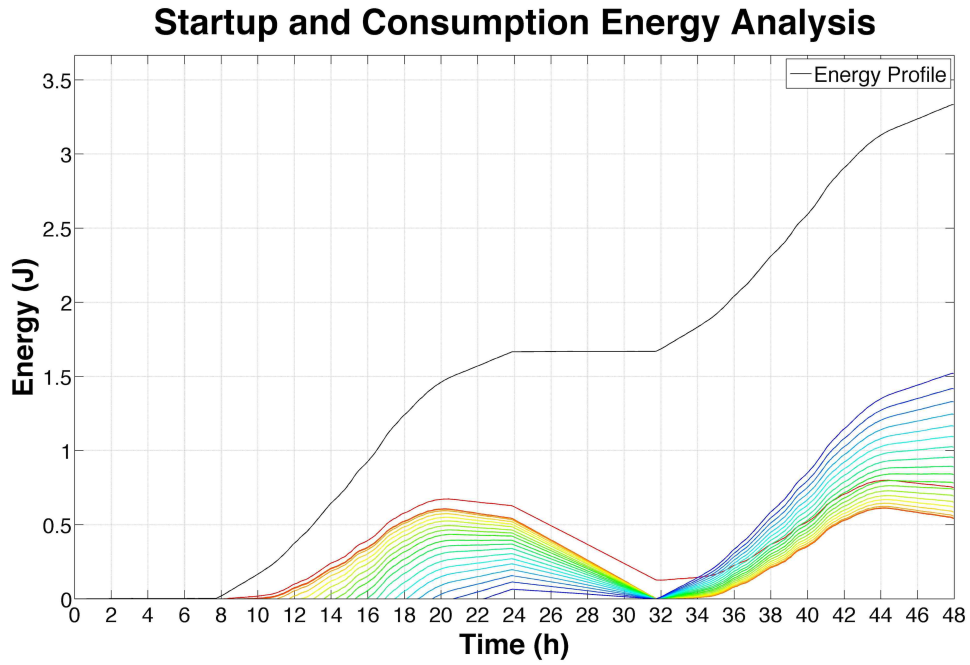


(a)

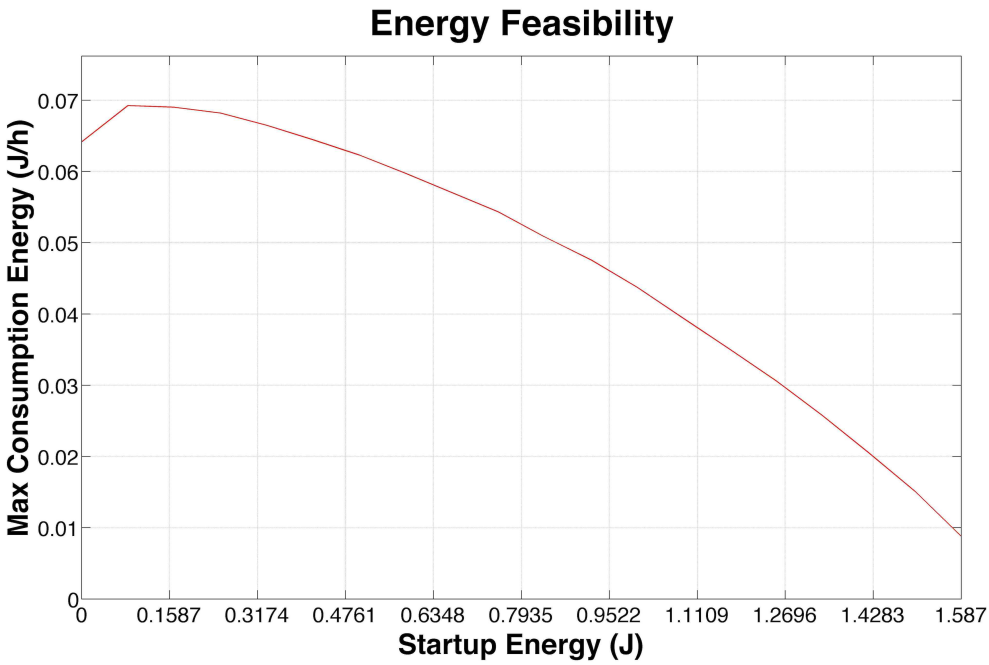


(b)

Figure D.32: Feasibility of the Amorton AM-1417 on 8th of June of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

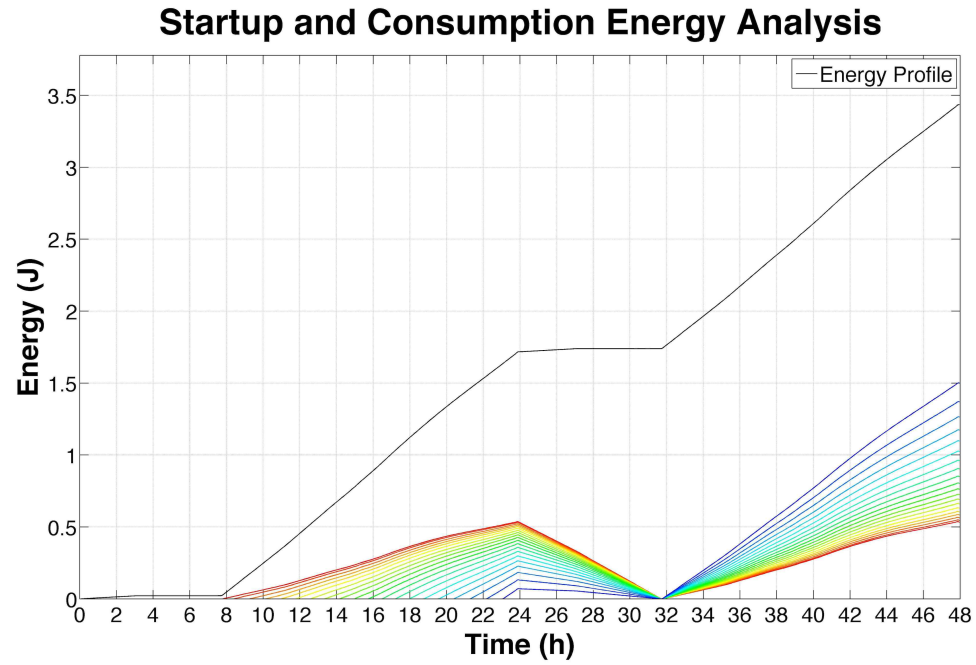


(a)

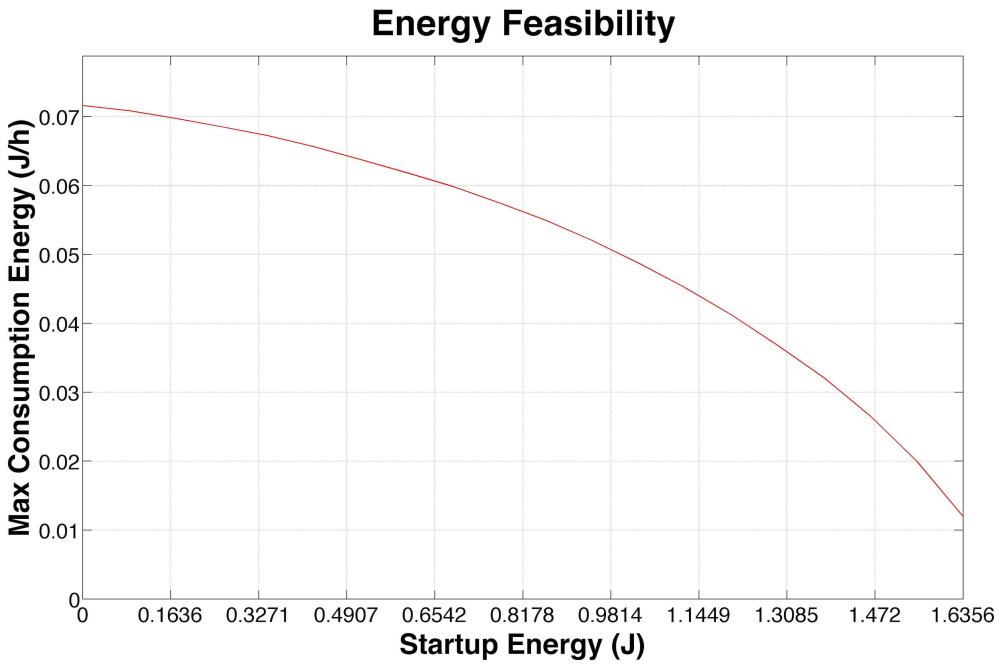


(b)

Figure D.33: Feasibility of the IXYS SLMD121H04L on 11th of June of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

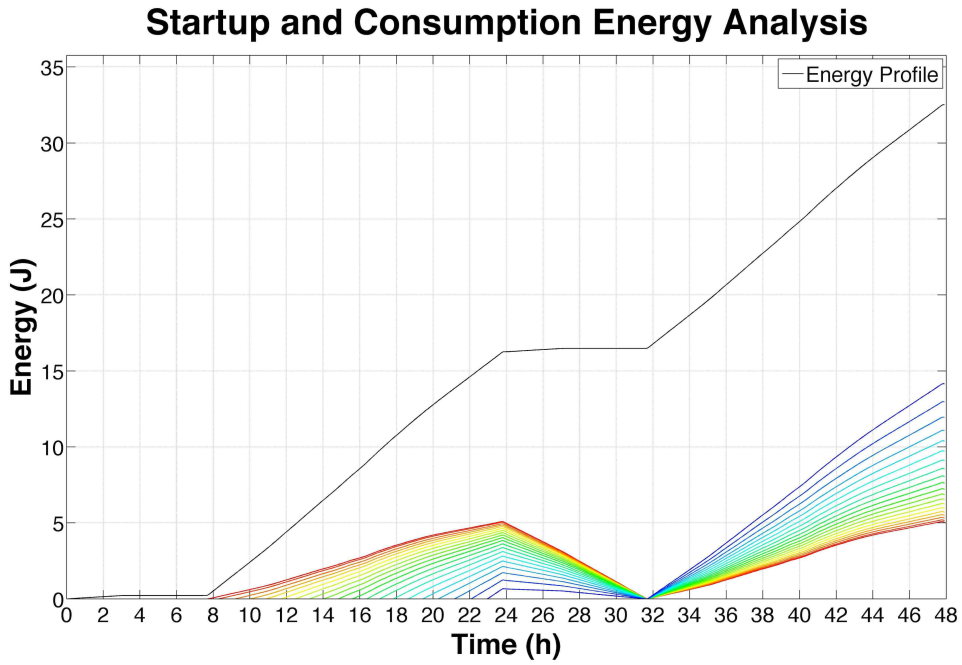


(a)

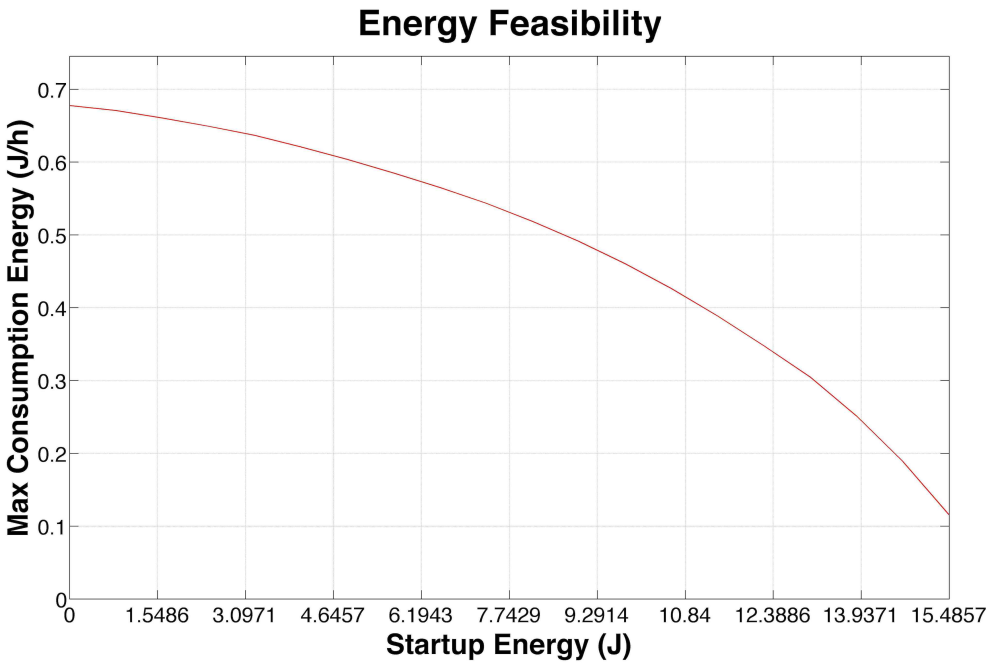


(b)

Figure D.34: Feasibility of the CYMBET CBC-PV-01N on 11th of June of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

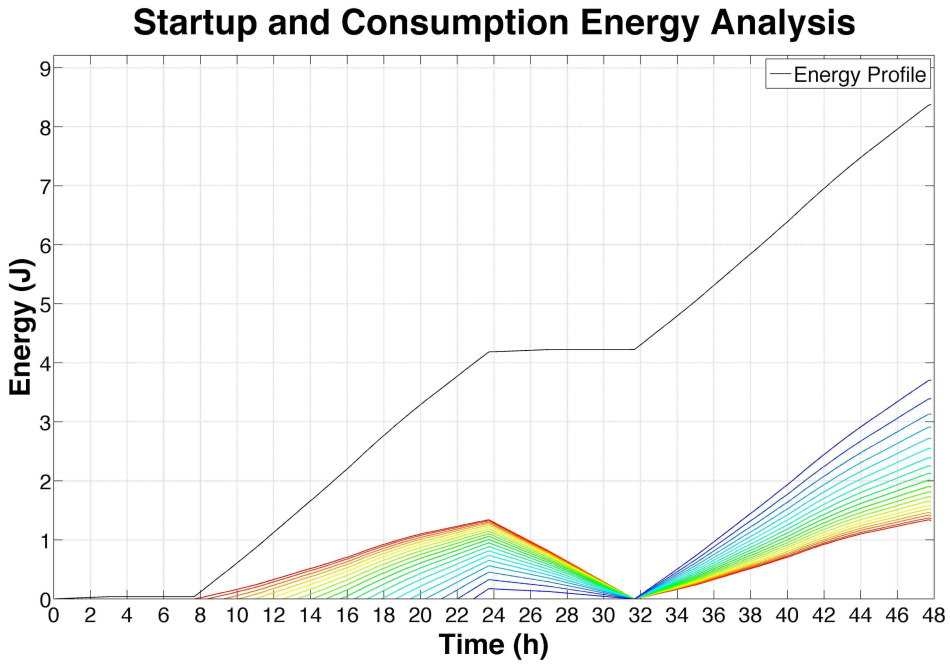


(a)

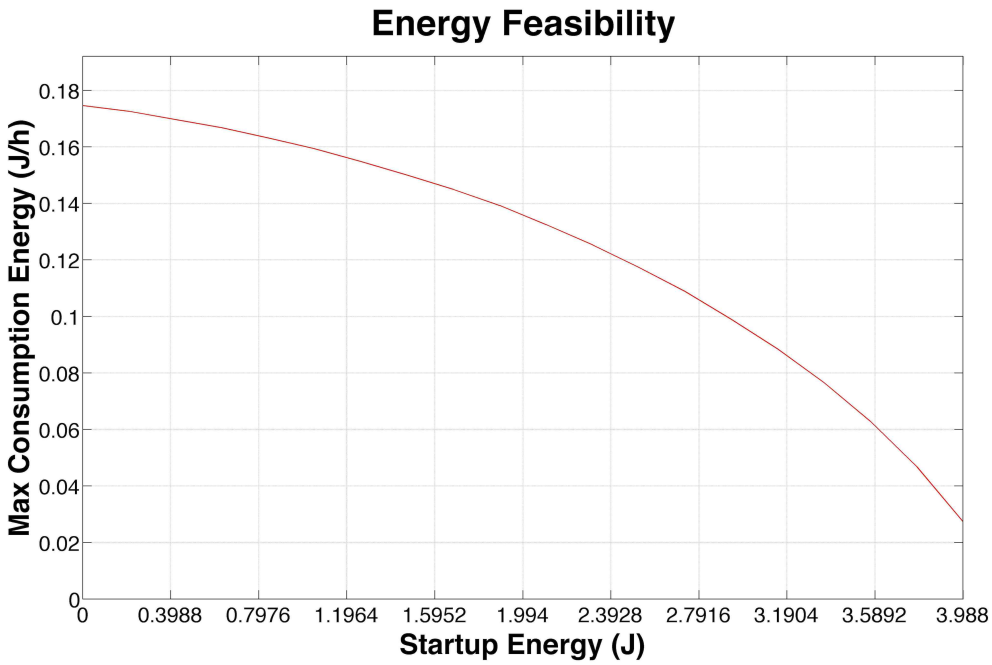


(b)

Figure D.35: Feasibility of the Amorton AM-1454 on 11th of June of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.



(a)



(b)

Figure D.36: Feasibility of the Amorton AM-1417 on 11th of June of 2015 – (a) Maximum consumption *versus* startup energy; (b) Energy feasibility.

Appendix E

PV Cell Behavioural Model

```
`include "disciplines.vams"
`include "constants.vams"

module pv_cell_math(n2, n1);
        inout n1, n2;
        electrical n2, n1;
        parameter real Isc = 40u from (0:inf);
        parameter real Voc = 0.6 from (0:inf);
        parameter real A = 0.22 from (0:inf);
analog begin
        I(n1, n2) <+ Isc/(1-exp(-Voc/A))*(1-exp( ( V(n2, n1)-Voc)/A ) );
end
endmodule
```

Appendix F

Voltage Doubler Mathematical Model

```
clear all;
% symbolic vars ----------------------------
syms Vs RL Ron Rs Cfly Cp CL f
T = 1/f;
syms s t

% phi_1 symbolic vars
syms Vinphi1 Vflyphi1 Voutphi1
syms vinphi1t1 vflyphi1t1 voutphi1t1

% phi_2 symbolic vars
syms Vinphi2 Vflyphi2 Voutphi2
syms vinphi2t2 vflyphi2t2 voutphi2t2

% @phi_1 ----------------------------------------------------------------
f1 = 1/Rs*(Vs/s-Vinphi1) - Cp*(s*Vinphi1 - vinphi1t1) + ...
            (Vflyphi1-Vinphi1)/(2*Ron);
f2 = Cfly*(s*Vflyphi1-vflyphi1t1) - (Vinphi1-Vflyphi1)/(2*Ron);
f3 = Voutphi1/RL + CL*(s*Voutphi1-voutphi1t1);

% @phi_2 ----------------------------------------------------------------
g1 = 1/Rs*(Vs/s-Vinphi2) - Cp*(s*Vinphi2-vinphi2t2) + ...
     (Voutphi2-Vflyphi2-Vinphi2)/(2*Ron);
g2 = Voutphi2/RL + CL*(s*Voutphi2-voutphi2t2) + ...
     (Voutphi2-Vflyphi2-Vinphi2)/(2*Ron);
g3 = (Voutphi2-Vflyphi2-Vinphi2)/(2*Ron) - Cfly*(s*Vflyphi2-vflyphi2t2);
```

```
% Determine time-domain functions for vin, vfly and vout ------------------
[L_Vinphi1,L_Vflyphi1,L_Voutphi1] = solve(f1==0,f2==0,f3==0, ...
                                          Vinphi1, Vflyphi1, Voutphi1);
t_Vinphi1  = ilaplace(L_Vinphi1);
t_Vflyphi1 = ilaplace(L_Vflyphi1);
t_Voutphi1 = ilaplace(L_Voutphi1);
[L_Vinphi2,L_Vflyphi2,L_Voutphi2] = solve(g1==0,g2==0,g3==0, ...
                                          Vinphi2, Vflyphi2, Voutphi2);
t_Vinphi2  = subs(ilaplace(L_Vinphi2), t, t-T/2);
t_Vflyphi2 = subs(ilaplace(L_Vflyphi2),t, t-T/2);
t_Voutphi2 = subs(ilaplace(L_Voutphi2),t, t-T/2);


% Boundary conditions ------------------------------------------------------
vinphi1_t2  = subs(t_Vinphi1,t,T/2);
vflyphi1_t2 = subs(t_Vflyphi1,t,T/2);
voutphi1_t2 = subs(t_Voutphi1,t,T/2);
vinphi2_t1  = subs(t_Vinphi2,t,T);
vflyphi2_t1 = subs(t_Vflyphi2,t,T);
voutphi2_t1 = subs(t_Voutphi2,t,T);

% Solve system of equations ------------------------------------------------
[vinphi2t2,vflyphi2t2,voutphi2t2,vinphi1t1,vflyphi1t1,voutphi1t1] = ...
      solve(vinphi1_t2  == vinphi2t2, ...
            vflyphi1_t2 == vflyphi2t2, ...
            voutphi1_t2 == voutphi2t2, ...
            vinphi2_t1  == vinphi1t1, ...
            vflyphi2_t1 == vflyphi1t1, ...
            voutphi2_t1 == voutphi1t1, ...
      vinphi2t2,vflyphi2t2,voutphi2t2, ...
      vinphi1t1,vflyphi1t1,voutphi1t1);

save doubler_bc.mat
```

Appendix G

Input Voltage Operation Range and Load Power

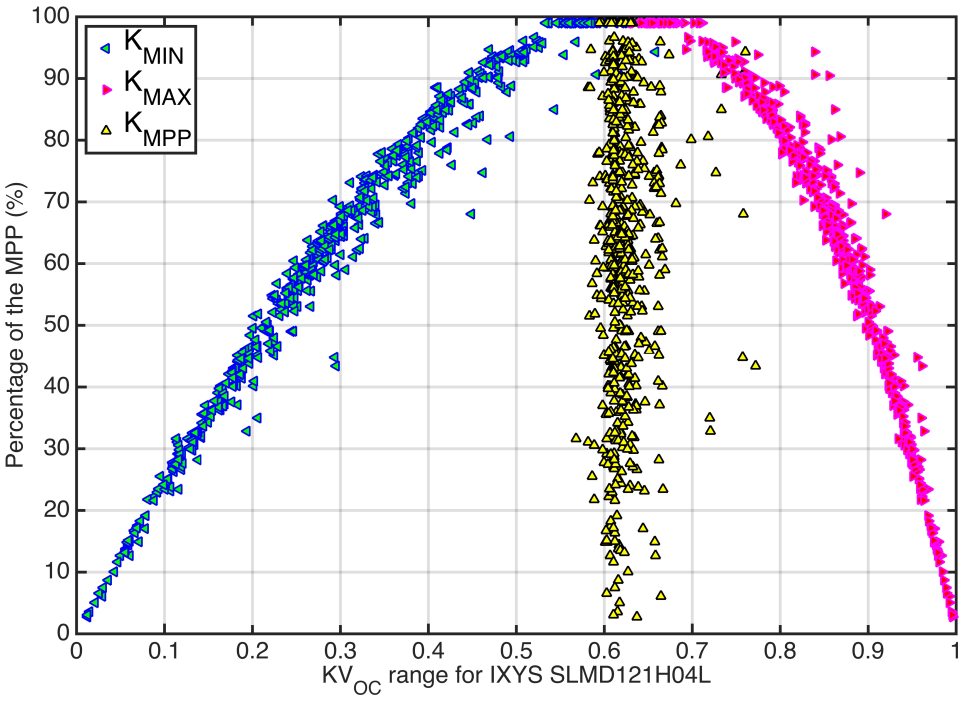


Figure G.1: Fractional V_{OC} operation ranges *versus* output power variation for the IXYX SLMD121H04L PV cell model.

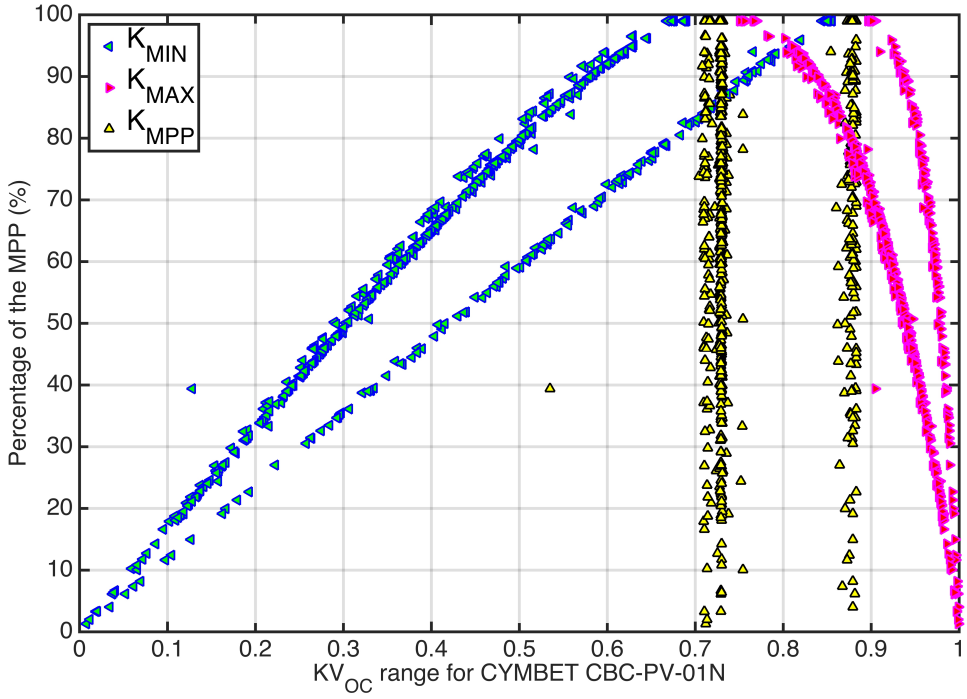


Figure G.2: Fractional V_{OC} operation ranges *versus* output power variation for the CYMBET CBC-PV-01N PV cell model.

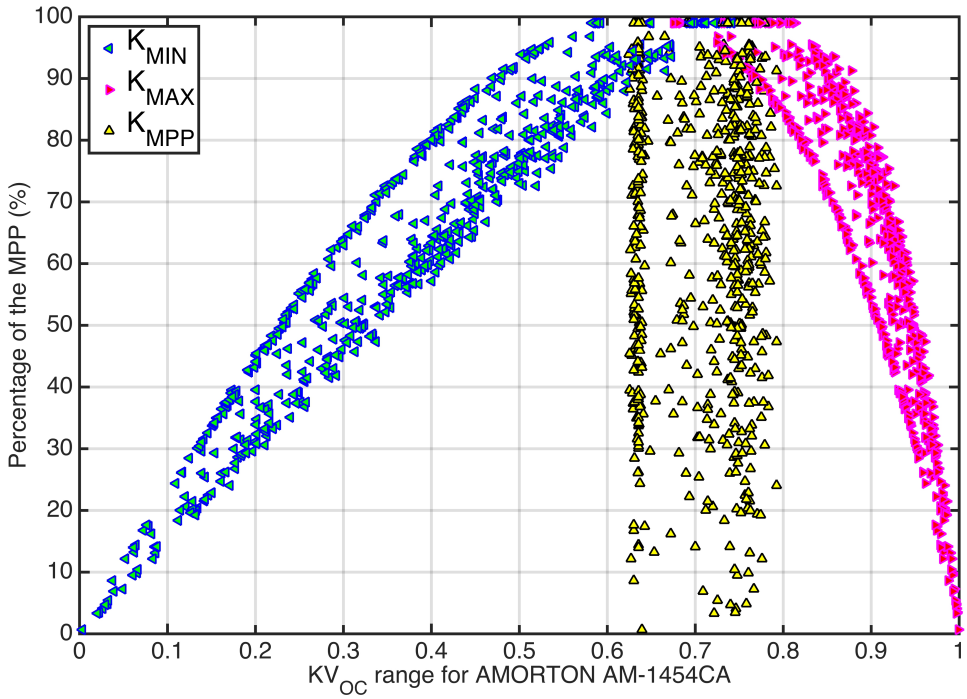


Figure G.3: Fractional V_{OC} operation ranges *versus* output power variation for the AMORTON AM-1454CA PV cell model.

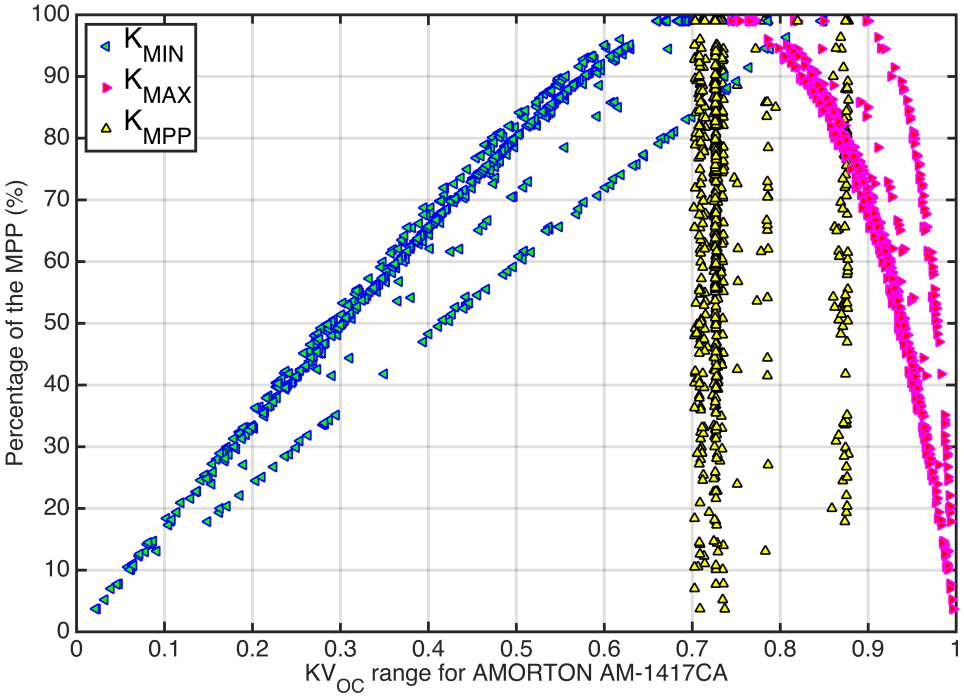


Figure G.4: Fractional V_{OC} operation ranges *versus* output power variation for the AMORTON AM-1417CA PV cell model.

Appendix H

The Open Circuit Voltage Sampler Block

```
`include "constants.vams"
`include "disciplines.vams"

module VOCsensor(in_VOC, out_En, out_disc, out_hVOC, out_ndisc);
output in_VOC;
electrical in_VOC;
output out_En;
electrical out_En;
output out_disc;
electrical out_disc;
output out_hVOC;
electrical out_hVOC;
output out_ndisc;
electrical out_ndisc;

parameter real sampleFreq = 1K;
parameter real ten=1u;
parameter real tmeas=1u;
parameter real tt=1p;

real connect_sw, sense_sw;
real inVoc, outVoc, enVoc;

real tsense,tmeasure,tnen;
real phase;
```

```
analog begin
@(initial_step) begin
        phase=-1;
        connect_sw=1.5;
        sense_sw=0;
        outVoc=0;
        enVoc=0;
end

inVoc=V(in_VOC);

if(phase<0) begin
        tsense=$abstime+(1/sampleFreq);
        phase=1;
end

@(timer(tsense)) begin
        if(phase>0) begin
                tmeasure=$abstime+tmeas;
                connect_sw=0;
                sense_sw=1.5;
        end
end

@(timer(tmeasure)) begin
        if(phase>0) begin
                outVoc=inVoc;
                enVoc=1;
                connect_sw=1.5;
                sense_sw=0;
                tnen=$abstime+ten;
        end
end

@(timer(tnen)) begin
        if(phase>0) begin
                enVoc=0;
                phase=-1;
        end
end
```

```
V(out_hVOC)<+transition(outVoc,tt,tt);
V(out_En)<+transition(enVoc,tt,tt);
V(out_disc)<+transition(sense_sw,tt,tt);
V(out_ndisc)<+transition(connect_sw,tt,tt);
end
endmodule
```

Appendix I

The Ratio Selector Block

```
`include "constants.vams"
`include "disciplines.vams"

module VOCEval(out_En, out_StepDown, out_StepUp, in_En, in_Vi,  in_VOC);
output out_En;
electrical out_En;
output out_StepDown;
electrical out_StepDown;
output out_StepUp;
electrical out_StepUp;
input in_En;
electrical in_En;
input in_Vi;
electrical in_Vi;
input in_VOC;
electrical in_VOC;

parameter real Kmin=0.6;
parameter real Kmax=0.9;
parameter real ten=1u;
parameter real tnot=1u;
parameter real vthresh=0.5;
parameter real tt=1p;

real inEn,inVi,inVOC;
real outEn,outUp,outDown;
real phase;
real tnen;
```

```
real tactive;

analog begin
        @(initial_step) begin
                phase=-1;
                outEn=0;
        end

        inEn=V(in_En);
        inVOC=V(in_VOC);
        inVi=V(in_Vi);

        if((phase<0) ) begin
                if(inVi>(Kmax*inVOC)) begin
                        tnen=$abstime+ten;
                        outEn=1;
                        outUp=1;
                        phase=1;
                end
                else if(inVi<(Kmin*inVOC)) begin
                        tnen=$abstime+ten;
                        outEn=1;
                        outDown=1;
                        phase=1;
                end
                else begin
                        //do nothing
                end
        end

        @(timer(tnen)) begin
                if(phase>0) begin
                        outEn=0;
                        outUp=0;
                        outDown=0;
                        tactive=$abstime+tnot;
                end
        end

        @(timer(tactive)) begin
```

```
                if(phase>0) begin
                        phase=-1;
                end
        end

        V(out_En)<+transition(outEn,tt,tt);
        V(out_StepUp)<+transition(outUp,tt,tt);
        V(out_StepDown)<+transition(outDown,tt,tt);

end
endmodule
```

Appendix J

Asynchronous State Machine Phase Control

J.1 Basic ASM Controller

```
`include "constants.vams"
`include "disciplines.vams"

module ASM(out_phi1, out_phi2, in_vcmp, in_vin);
        output out_phi1;
        electrical out_phi1;
        output out_phi2;
        electrical out_phi2;
        input in_vcmp;
        electrical in_vcmp;
        input in_vin;
        electrical in_vin;

        parameter real freq_Phi = 500K;
        parameter real dt = 0.495;
        parameter real tt = 1p;
        parameter real tno = 5p;

        parameter real n=2;

        parameter real T = 1/freq_Phi;
        parameter real tw = dt*T-2*tt;

        real v1,v2;
```

```
real tstart,tend,ttend,ttendd;
real inin,vv;
real phase;


analog begin

        @(initial_step) begin
                phase=-1;
                v1=1.5;
                v2=0;
        end

        vv=V(in_vcmp);
        inin=V(in_vin);

        if( phase<0 && inin>(1/n)*vv  ) begin
                v1=0;
                v2=0;
                phase=1;
                tstart=$abstime+tno;
                tend=tstart+tw;
                ttend=tend+tno;
                ttendd=ttend+tw;
        end

        @(timer(tstart)) begin
                if(phase>0) begin
                        v1=0;
                        v2=1.5;
                end
        end

        @(timer(tend)) begin
                if(phase>0) begin
                        v1=0;
                        v2=0;
                end
        end
```

```
                @(timer(ttend)) begin
                        if(phase>0) begin
                                v1=1.5;
                                v2=0;
                        end
                end

                @(timer(ttendd)) begin
                        if(phase>0) begin
                                phase=-1;
                        end
                end

                V(out_phi1)<+transition(v1,tt,tt);
                V(out_phi2)<+transition(v2,tt,tt);

        end
endmodule
```

J.2 The Phase Controller Block - Multi ratio ASM

```
`include "constants.vams"
`include "disciplines.vams"

module ASM_multiratio(out_phi1, out_phi2, out_Morph3, out_Morph4, out_notM3,
in_vcmp, in_vin, in_Up, in_Step, in_Down);
output out_phi1;
electrical out_phi1;
output out_phi2;
electrical out_phi2;
output out_Morph3;
electrical out_Morph3;
output out_Morph4;
electrical out_Morph4;
output out_N;
electrical out_N;
output out_notM3;
electrical out_notM3;
output out_notM4;
electrical out_notM4;
```

```
input in_vcmp;
electrical in_vcmp;
input in_vin;
electrical in_vin;
input in_Up;
electrical in_Up;
input in_Step;
electrical in_Step;
input in_Down;
electrical in_Down;


parameter real freq_Phi = 500K;
parameter real dt = 0.495;
parameter real tt = 1p;
parameter real tno = 5p;

parameter real n=2;

parameter real T = 1/freq_Phi;
parameter real tw = dt*T-2*tt;

parameter real vthresh=0.5;

real v1,v2;
real tstart,tend,ttend,ttendd;
real inin,vv;
real phase;
real NN, nn;
real inStep,inUp,inDown;
real outM3,outM4;
real outNM3,outNM4;


analog begin

@(initial_step) begin
        phase=-1;
```

```
        v1=1.5;
        v2=0;
        nn=0;
        NN=n+nn;
        outM3=0;
        outM4=0;
        outNM3=1.5;
        outNM4=1.5;
end

vv=V(in_vcmp);
inin=V(in_vin);
inStep=V(in_Step);
inUp=V(in_Up);
inDown=V(in_Down);

if(phase<0 && inStep>vthresh) begin
        if(inUp>vthresh && nn<2) begin
                nn=nn+1;
                NN=n+nn;
        end
        else if(inDown>vthresh && nn>0) begin
                nn=nn-1;
                NN=n+nn;
        end
        else begin
                NN=n+nn;
        end
        if(NN>1 && NN<3)  begin
                outM3=0;
                outM4=0;
                outNM3=1.5;
                outNM4=1.5;
        end
        else if(NN>2 && NN<4) begin
                outM3=1.5;
                outM4=0;
                outNM3=0;
                outNM4=1.5;
        end
```

```
        else if(NN>3) begin
                outM3=1.5;
                outM4=1.5;
                outNM3=0;
                outNM4=0;
        end
        else begin
                //do nothing
        end
end


if( phase<0 && inin>(1/NN)*vv  ) begin
        v1=0;
        v2=0;
        phase=1;
        tstart=$abstime+tno;
        tend=tstart+tw;
        ttend=tend+tno;
        ttendd=ttend+tw;
end

@(timer(tstart)) begin
        if(phase>0) begin
                v1=0;
                v2=1.5;
        end
end

@(timer(tend)) begin
        if(phase>0) begin
                v1=0;
                v2=0;
        end
end

@(timer(ttend)) begin
        if(phase>0) begin
                v1=1.5;
                v2=0;
```

```
        end
end

@(timer(ttendd)) begin
        if(phase>0) begin
                phase=-1;
        end
end

V(out_phi1)<+transition(v1,tt,tt);
V(out_phi2)<+transition(v2,tt,tt);
V(out_Morph3)<+transition(outM3,tt,tt);
V(out_Morph4)<+transition(outM4,tt,tt);
V(out_N)<+transition(NN,tt,tt);
V(out_notM3)<+transition(outNM3,tt,tt);
V(out_notM4)<+transition(outNM4,tt,tt);

end
endmodule
```

J.3 The Optimised Phase Controller Block for Constrained Power Maximisation

```
`include "constants.vams"
`include "disciplines.vams"

module ASM_multiratio(out_phi1, out_phi2, out_Morph3, out_Morph4, out_notM3,
in_vcmp, in_vin, in_Up, in_Step, in_Down, in_Ref);
output out_phi1;
electrical out_phi1;
output out_phi2;
electrical out_phi2;
output out_Morph3;
electrical out_Morph3;
output out_Morph4;
electrical out_Morph4;
output out_N;
electrical out_N;
output out_notM3;
electrical out_notM3;
```

```
output out_notM4;
electrical out_notM4;


input in_vcmp;
electrical in_vcmp;
input in_vin;
electrical in_vin;
input in_Up;
electrical in_Up;
input in_Step;
electrical in_Step;
input in_Down;
electrical in_Down;
input in_Ref;
electrical in_Ref;

parameter real freq_Phi = 500K;
parameter real dt = 0.495;
parameter real tt = 1p;
parameter real tno = 5p;

parameter real n=2;

parameter real T = 1/freq_Phi;
parameter real tw = dt*T-2*tt;

parameter real vthresh=0.5;

real v1,v2;
real ref;
real tstart,tend,ttend,ttendd;
real inin,vv;
real phase;
real NN, nn;
real inStep,inUp,inDown;
real outM3,outM4;
real outNM3,outNM4;
```

```
analog begin

@(initial_step) begin
        phase=-1;
        v1=1.5;
        v2=0;
        nn=0;
        NN=n+nn;
        outM3=0;
        outM4=0;
        outNM3=1.5;
        outNM4=1.5;
end

vv=V(in_vcmp);
inin=V(in_vin);
inStep=V(in_Step);
inUp=V(in_Up);
inDown=V(in_Down);
ref=V(in_Ref);

if(phase<0 && inStep>vthresh) begin
        if(inUp>vthresh && nn<2) begin
                nn=nn+1;
                NN=n+nn;
        end
        else if(inDown>vthresh && nn>0) begin
                nn=nn-1;
                NN=n+nn;
        end
        else begin
                NN=n+nn;
        end
        if(NN>1 && NN<3)  begin
                outM3=0;
                outM4=0;
                outNM3=1.5;
                outNM4=1.5;
        end
        else if(NN>2 && NN<4) begin
```

```
                outM3=1.5;
                outM4=0;
                outNM3=0;
                outNM4=1.5;
        end
        else if(NN>3) begin
                outM3=1.5;
                outM4=1.5;
                outNM3=0;
                outNM4=0;
        end
        else begin
                //do nothing
        end
end


if( phase<0 && inin>(1/NN)*vv && vv<ref ) begin
        v1=0;
        v2=0;
        phase=1;
        tstart=$abstime+tno;
        tend=tstart+tw;
        ttend=tend+tno;
        ttendd=ttend+tw;
end

@(timer(tstart)) begin
        if(phase>0) begin
                v1=0;
                v2=1.5;
        end
end

@(timer(tend)) begin
        if(phase>0) begin
                v1=0;
                v2=0;
        end
end
```

```
@(timer(ttend)) begin
        if(phase>0) begin
                v1=1.5;
                v2=0;
        end
end

@(timer(ttendd)) begin
        if(phase>0) begin
                phase=-1;
        end
end

V(out_phi1)<+transition(v1,tt,tt);
V(out_phi2)<+transition(v2,tt,tt);
V(out_Morph3)<+transition(outM3,tt,tt);
V(out_Morph4)<+transition(outM4,tt,tt);
V(out_N)<+transition(NN,tt,tt);
V(out_notM3)<+transition(outNM3,tt,tt);
V(out_notM4)<+transition(outNM4,tt,tt);

end
endmodule
```

J.4 The Optimised Phase Controller Block for Constrained Power Maximisation and Unitary or Step Down Reconfigurability

```
`include "constants.vams"
`include "disciplines.vams"

module ASM(out_phi1, out_phi2, out_Morph3, out_Morph4, out_notM3, out_notM4,
in_vcmp, in_vin, in_Up, in_Step, in_Down, in_Ref);
output out_phi1;
electrical out_phi1;
output out_phi2;
electrical out_phi2;
output out_Morph3;
electrical out_Morph3;
output out_Morph4;
```

```
electrical out_Morph4;
output out_N;
electrical out_N;
output out_notM3;
electrical out_notM3;
output out_notM4;
electrical out_notM4;
output out_SH;
electrical out_SH;
output out_nSH;
electrical out_nSH;
output out_stepUp;
electrical out_stepUp;
output out_stepDown;
electrical out_stepDown;


input in_vcmp;
electrical in_vcmp;
input in_vin;
electrical in_vin;
input in_Up;
electrical in_Up;
input in_Step;
electrical in_Step;
input in_Down;
electrical in_Down;
input in_Ref;
electrical in_Ref;


parameter real freq_Phi = 500K;
parameter real dt = 0.495;
parameter real tt = 1p;
parameter real tno = 5p;

parameter real n=2;

parameter real T = 1/freq_Phi;
parameter real tw = dt*T-2*tt;
```

```
parameter real twstep=tw;

parameter real vthresh=0.5;

real v1,v2;
real ref;
real tstart,tend,ttend,ttendd;
real inin,vv;
real phase;
real NN, nn;
real inStep,inUp,inDown;
real outM3,outM4;
real outNM3,outNM4;
real ttw;
real outSH,outnSH;
real outStepUp, outStepDown;



// states:
// nn=1 -> 1/4
// nn=2 -> 1/3
// nn=3 -> 1/2
// nn=4 -> 1
// nn=5 -> 2
// nn=6 -> 3
// nn=7 -> 4

analog begin

@(initial_step) begin
        phase=-1;
        v1=1.5;
        v2=0;
        nn=5;
        NN=n;
        outM3=0;
        outM4=0;
        outNM3=1.5;
        outNM4=1.5;
```

```
        ttw=tw;
        outSH=0;
        outnSH=1.5;
        outStepUp=1.5;
        outStepDown=0;
end

vv=V(in_vcmp);
inin=V(in_vin);
inStep=V(in_Step);
inUp=V(in_Up);
inDown=V(in_Down);
ref=V(in_Ref);

if(phase<0 && inStep>vthresh) begin
        if(inUp>vthresh) begin
                if(nn<7) begin nn=nn+1; end
        end
        else if(inDown>vthresh) begin
                if(nn>1) begin nn=nn-1; end
        end
        if(nn<2 && nn>0) begin // x(1/4)
                outM3=1.5;
                outM4=1.5;
                outNM3=0;
                outNM4=0;
                outSH=0;
                outnSH=1.5;
                outStepUp=0;
                outStepDown=1.5;
                NN=(1.0/4.0);
        end
        else if(nn<3 && nn>1) begin // x(1/3)
                outM3=1.5;
                outM4=0;
                outNM3=0;
                outNM4=1.5;
                outSH=0;
                outnSH=1.5;
                outStepUp=0;
```

```
            outStepDown=1.5;
            NN=(1.0/3.0);
        end
        else if(nn<4 && nn>2) begin // x(1/2)
            outM3=0;
            outM4=0;
            outNM3=1.5;
            outNM4=1.5;
            outSH=0;
            outnSH=1.5;
            outStepUp=0;
            outStepDown=1.5;
            NN=(1.0/2.0);
        end
        else if(nn<5 && nn>3) begin // x(1)
            outM3=0;
            outM4=0;
            outNM3=1.5;
            outNM4=1.5;
            outSH=1.5;
            outnSH=0;
            outStepUp=1.5;
            outStepDown=0;
            NN=1;
        end
        else if(nn<6 && nn>4) begin // x(2)
            outM3=0;
            outM4=0;
            outNM3=1.5;
            outNM4=1.5;
            outSH=0;
            outnSH=1.5;
            outStepUp=1.5;
            outStepDown=0;
            NN=2;
        end
        else if(nn<7 && nn>5) begin // x(3)
            outM3=1.5;
            outM4=0;
            outNM3=0;
```

```
                outNM4=1.5;
                outSH=0;
                outnSH=1.5;
                outStepUp=1.5;
                outStepDown=0;
                NN=3;
        end
        else if(nn>6) begin // x(4)
                outM3=1.5;
                outM4=1.5;
                outNM3=0;
                outNM4=0;
                outSH=0;
                outnSH=1.5;
                outStepUp=1.5;
                outStepDown=0;
                NN=4;
        end
end
if( phase<0 ) begin
        if(vv>ref) begin
                ttw=ttw+twstep;
        end
        if(vv<ref)begin
                if(ttw>tw) begin
                        ttw=ttw-twstep;
                end
        end
        v1=0;
        v2=0;
        phase=1;
        tstart=$abstime+tno;
        tend=tstart+ttw;
        ttend=tend+tno;
        ttendd=ttend+ttw;
end


@(timer(tstart)) begin
        if(phase>0) begin
```

```
                v1=0;
                v2=1.5;
        end
end

@(timer(tend)) begin
        if(phase>0) begin
                v1=0;
                v2=0;
        end
end

@(timer(ttend)) begin
        if(phase>0) begin
                v1=1.5;
                v2=0;
        end
end

@(timer(ttendd)) begin
        if(phase>0) begin
                phase=-1;
        end
end

V(out_phi1)<+transition(v1,tt,tt);
V(out_phi2)<+transition(v2,tt,tt);
V(out_Morph3)<+transition(outM3,tt,tt);
V(out_Morph4)<+transition(outM4,tt,tt);
V(out_N)<+transition(NN,tt,tt);
V(out_notM3)<+transition(outNM3,tt,tt);
V(out_notM4)<+transition(outNM4,tt,tt);
V(out_SH)<+transition(outSH,tt,tt);
V(out_nSH)<+transition(outnSH,tt,tt);
V(out_stepUp)<+transition(outStepUp,tt,tt);
V(out_stepDown)<+transition(outStepDown,tt,tt);

end
endmodule
```

Bibliography

[1] W. S. Wang, T. O'Donnell, N. Wang, M. Hayes, B. O'Flynn, and C. O'Mathuna, "Design considerations of sub-mW indoor light energy harvesting for wireless sensor systems," *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, vol. 6, no. 2, p. 6, 2010. Cited on pages 1, 6, 8, 9, and 20.

[2] N. Javanmard, G. Vafadar, and A. Nasiri, "Indoor power harvesting using photovoltaic cells for low power applications," in *13th European Conference on Power Electronics and Applications, 2009*. IEEE, 2009, pp. 1–10. Cited on pages 1 and 20.

[3] S. Chalasani and J. M. Conrad, "A survey of energy harvesting sources for embedded systems," in *Southeastcon, 2008. IEEE*. IEEE, 2008, pp. 442–447. Cited on pages 1, 2, and 20.

[4] U. Gangopadhyay, S. Jana, and S. Das, "State of art of solar photovoltaic technology," in *Conference Papers in Science*, vol. 2013. Hindawi Publishing Corporation, 2013. Cited on pages 1 and 7.

[5] E. Commission, "The 2020 climate and energy package," December 2014, available at http://ec.europa.eu/clima/policies/package/index_en.htm. Cited on page 1.

[6] G. W. Crabtree and N. S. Lewis, "Solar energy conversion," *Physics today*, vol. 60, no. 3, pp. 37–42, 2007. Cited on page 1.

[7] C. Perera, C. Liu, S. Jayawardena, and M. Chen, "A survey on internet of things from industrial market perspective," *Access, IEEE*, vol. 2, pp. 1660–1679, 2014. Cited on page 1.

[8] V. Raghunathan, C. Schurgers, S. Park, and M. B. Srivastava, "Energy-aware wireless microsensor networks," *IEEE Signal Processing Magazine*, vol. 19, no. 2, pp. 40–50, 2002. Cited on page 1.

[9] G. J. Pottie and W. J. Kaiser, "Wireless integrated network sensors," *Communications of the ACM*, vol. 43, no. 5, pp. 51–58, 2000. Cited on page 1.

[10] J. M. Kahn, R. H. Katz, and K. S. Pister, "Next century challenges: mobile networking for "smart dust"," in *Proceedings of the 5th annual ACM/IEEE international conference on Mobile computing and networking*. ACM, 1999, pp. 271–278. Cited on page 1.

[11] T. Starner, "Human-powered wearable computing," *IBM systems Journal*, vol. 35, no. 3.4, pp. 618–629, 1996. Cited on page 1.

[12] V. Raghunathan, A. Kansal, J. Hsu, J. Friedman, and M. Srivastava, "Design considerations for solar energy harvesting wireless embedded systems," in *Proceedings of the 4th international symposium on Information processing in sensor networks*. IEEE Press, 2005, p. 64. Cited on page 2.

[13] X. Fafoutis, T. Sørensen, and J. Madsen, "Energy harvesting-wireless sensor networks for indoors applications using IEEE 802.11," *Procedia Computer Science*, vol. 32, pp. 991–996, 2014. Cited on page 2.

[14] F. Simjee and P. H. Chou, "Everlast: long-life, supercapacitor-operated wireless sensor node," in *Proceedings of the 2006 International Symposium on Low Power Electronics and Design, 2006. ISLPED'06.* IEEE, 2006, pp. 197–202. Cited on pages 2, 16, and 18.

[15] T. Voigt, H. Ritter, and J. Schiller, "Utilizing solar power in wireless sensor networks," in *28th Annual IEEE International Conference on Local Computer Networks, 2003. LCN'03. Proceedings.* IEEE, 2003, pp. 416–422. Cited on page 2.

[16] D. S. Tudose, A. Voinescu, M. Petrareanu, A. Bucur, D. Loghin, A. Bostan, and N. Tapus, "Home automation design using 6LoWPAN wireless sensor networks," in *International Conference on Distributed Computing in Sensor Systems and Workshops (DCOSS), 2011*. IEEE, 2011, pp. 1–6. Cited on page 2.

[17] A. Nasiri, S. A. Zabalawi, and G. Mandic, "Indoor power harvesting using photovoltaic cells for low-power applications," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 11, pp. 4502–4509, 2009. Cited on pages 2 and 5.

[18] A. Chirap, V. Popa, E. Coca, and D. A. Potorac, "A study on light energy harvesting from indoor environment: The autonomous sensor nodes," in *Development and Application Systems (DAS), 2014 International Conference on*. IEEE, 2014, pp. 127–131. Cited on page 2.

[19] D. Pimentel and P. Musílek, "Power management with energy harvesting devices," in *23rd Canadian Conference on Electrical and Computer Engineering (CCECE), 2010*. IEEE, 2010, pp. 1–4. Cited on page 2.

[20] Y. K. Tan and S. K. Panda, "Energy harvesting from hybrid indoor ambient light and thermal energy sources for enhanced performance of wireless sensor nodes," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 9, pp. 4424–4435, 2011. Cited on page 2.

[21] Z. Wan, Y. Tan, and C. Yuen, "Review on energy harvesting and energy management for sustainable wireless sensor networks," in *Communication Technology (ICCT), 2011 IEEE 13th International Conference on*. IEEE, 2011, pp. 362–367. Cited on page 2.

[22] M. S. Lim, S. H. Ali, S. Jahariah, M. Islam *et al.*, "Modelling of hybrid energy harvester with DC-DC boost converter using arbitrary input sources for ultra-low-power microdevices," in *Semiconductor Electronics (ICSE), 2014 IEEE International Conference on*. IEEE, 2014, pp. 28–31. Cited on page 2.

[23] A. Pandharipande and S. Li, "Light-harvesting wireless sensors for indoor lighting control," *Sensors Journal, IEEE*, vol. 13, no. 12, pp. 4599–4606, Dec 2013. Cited on page 2.

[24] N. J. Guilar, T. J. Kleeburg, A. Chen, D. R. Yankelevich, and R. Amirtharajah, "Integrated solar energy harvesting and storage," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 17, no. 5, pp. 627–637, 2009. Cited on page 2.

[25] R. P. Foundation, "Raspberry pi," 2015, available at https://www.raspberrypi.org/. Cited on pages 3 and 28.

[26] I. The Mathworks, "Matlab, the language of technical computing," 2015, available at http://www.mathworks.com/products/matlab/. Cited on pages 3 and 44.

[27] I. Cadence Design Systems, "EDA software and verification tools," 2015, available at https://www.cadence.com/. Cited on pages 3 and 44.

[28] A. S. Sedra and K. C. Smith, *Microelectronic circuits*. Oxford University Press, 1998, vol. 1. Cited on page 5.

[29] R. Bube, *Fundamentals of solar cells: photovoltaic solar energy conversion*. Elsevier, 1983. Cited on page 5.

[30] H. S. Rauschenbach, "Solar cell array design handbook-the principles and technology of photovoltaic energy conversion," *NASA STI/Recon Technical Report A*, vol. 80, p. 34847, 1980. Cited on page 6.

[31] J. Gow and C. Manning, "Development of a photovoltaic array model for use in power-electronics simulation studies," *IEE Proceedings-Electric Power Applications*, pp. 193–200, 1999. Cited on page 6.

[32] N. Pongratananukul and T. Kasparis, "Tool for automated simulation of solar arrays using general-purpose simulators," in *IEEE Workshop on Computers in Power Electronics, 2004. Proceedings. 2004*. IEEE, 2004, pp. 10–14. Cited on page 6.

[33] S. Chowdhury, G. Taylor, S. Chowdhury, A. Saha, and Y. Song, "Modelling, simulation and performance analysis of a PV array in an embedded environment," in *42nd International Universities Power Engineering Conference, 2007. UPEC 2007.* IEEE, 2007, pp. 781–785. Cited on page 6.

[34] K. Nishioka, N. Sakitani, Y. Uraoka, and T. Fuyuki, "Analysis of multicrystalline silicon solar cells by modified 3-diode equivalent circuit model taking leakage current through

periphery into consideration," *Solar Energy Materials and Solar Cells*, vol. 91, no. 13, pp. 1222–1227, 2007. Cited on page 6.

[35] C. Carrero, J. Amador, and S. Arnaltes, "A single procedure for helping PV designers to select silicon PV modules and evaluate the loss resistances," *Renewable Energy*, vol. 32, no. 15, pp. 2579–2589, 2007. Cited on page 6.

[36] R. Miles, K. Hynes, and I. Forbes, "Photovoltaic solar cells: An overview of state-of-the-art cell development and environmental issues," *Progress in Crystal Growth and Characterization of Materials*, vol. 51, no. 1, pp. 1–42, 2005. Cited on page 7.

[37] H. Field, "Solar cell spectral response measurement errors related to spectral band width and chopped light waveform," in *Conference Record of the Twenty-Sixth IEEE Photovoltaic Specialists Conference, 1997.* IEEE, 1997, pp. 471–474. Cited on pages 6 and 8.

[38] N. National Instruments Corporation, "A Practical Guide to Machine Vision Lighting - Part I," 2014, http://www.ni.com/white-paper/6901/en/. Cited on page 8.

[39] D. Chapin, C. Fuller, and G. Pearson, "A new silicon p-n junction photocell for converting solar radiation into electrical power," *Journal of Applied Physics*, vol. 25, no. 5, pp. 676–677, 1954. Cited on page 7.

[40] W. Anderson, P. Dussinger, D. Sarraf, and S. Tamanna, "Heat pipe cooling of concentrating photovoltaic cells," in *33rd IEEE Photovoltaic Specialists Conference, 2008. PVSC'08.* IEEE, 2008, pp. 1–6. Cited on page 8.

[41] K. Woods, F. Ashrafzadeh, and H. Rathnayake, "Organic solar cell energy harvesting, control, optimization, and commercialization—challenges and opportunities," in *4th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG), 2013*. IEEE, 2013, pp. 1–7. Cited on page 8.

[42] D. Dimova-Malinovska, "The state-of-the-art and future development of the photovoltaic technologies–the route from crystalline to nanostructured and new emerging materials," in *Journal of Physics: Conference Series*, vol. 253, no. 1. IOP Publishing, 2010, p. 012007. Cited on page 8.

[43] B. S. Xakalashe and M. Tangstad, "Silicon processing: from quartz to crystalline silicon solar cells," *Chemical Technology*, 2012. Cited on page 8.

[44] K. R. Catchpole, "Nanostructures in photovoltaics," *Philosophical Transactions of the Royal Society A: Mathematical, Physical and Engineering Sciences*, vol. 364, no. 1849, pp. 3493–3503, 2006. Cited on page 8.

[45] A. Ogura, T. Morioka, P. Garcia-Linares, E. Hernandez, I. Ramiro, I. Artacho, E. Antolin, A. Marti, A. Luque, M. Yamaguchi *et al.*, "Modelling of quantum dot solar cells for concentrator PV applications," in *37th IEEE Photovoltaic Specialists Conference (PVSC), 2011*. IEEE, 2011, pp. 002 642–002 645. Cited on page 8.

[46] U. Aeberhard and R. Morf, "Microscopic nonequilibrium theory of quantum well solar cells," *Physical Review B*, vol. 77, no. 12, p. 125343, 2008. Cited on page 8.

[47] L. Bhusal and A. Freundlich, "Superlattice material for the multi-junction thermophotovoltaics lattice matched to InP," in *Conference Record of the 2006 IEEE 4th World Conference on Photovoltaic Energy Conversion*, vol. 1. IEEE, 2006, pp. 683–685. Cited on page 8.

[48] A. Goetzberger, C. Hebling, and H.-W. Schock, "Photovoltaic materials, history, status and outlook," *Materials Science and Engineering: R: Reports*, vol. 40, no. 1, pp. 1–46, 2003. Cited on page 8.

[49] C. Lu, V. Raghunathan, and K. Roy, "Efficient design of micro-scale energy harvesting systems," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 1, no. 3, pp. 254–266, 2011. Cited on pages 10 and 13.

[50] ——, "Maximum power point considerations in micro-scale solar energy harvesting systems," in *Proceedings of 2010 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2010, pp. 273–276. Cited on pages 10, 12, and 13.

[51] H. Shao, C.-Y. Tsui, and W.-H. Ki, "An inductor-less micro solar power management system design for energy harvesting applications," in *IEEE International Symposium on Circuits and Systems, 2007. ISCAS 2007.* IEEE, 2007, pp. 1353–1356. Cited on page 10.

[52] J. Kim, J. Kim, and C. Kim, "A regulated charge pump with a low-power integrated optimum power point tracking algorithm for indoor solar energy harvesting," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 58, no. 12, pp. 802–806, 2011. Cited on page 10.

[53] G. Palumbo and D. Pappalardo, "Charge pump circuits: An overview on design strategies and topologies," *IEEE Circuits and Systems Magazine*, vol. 10, no. 1, pp. 31–45, 2010. Cited on page 10.

[54] D. Hamza and P. K. Jain, "Conducted emi noise mitigation in DC-DC converters using active filtering method," in *IEEE Power Electronics Specialists Conference, 2008. PESC 2008.* IEEE, 2008, pp. 188–194. Cited on page 10.

[55] J. F. Dickson, "On-chip high-voltage generation in NMOS integrated circuits using an improved voltage multiplier technique," *IEEE Journal of Solid-State Circuits*, vol. 11, no. 3, pp. 374–378, 1976. Cited on pages 10 and 13.

[56] J. S. Witters, G. Groeseneken, and H. E. Maes, "Analysis and modeling of on-chip high-voltage generator circuits for use in EEPROM circuits," *IEEE Journal of Solid-State Circuits*, vol. 24, no. 5, pp. 1372–1380, 1989. Cited on page 10.

[57] M. S. Makowski and D. Maksimovic, "Performance limits of switched-capacitor DC-DC converters," in *26th Annual IEEE Power Electronics Specialists Conference, 1995. PESC'95 Record.*, vol. 2. IEEE, 1995, pp. 1215–1221. Cited on pages 11 and 12.

[58] B. Arntzen and D. Maksimovic, "Switched-capacitor DC/DC converters with resonant gate drive," *IEEE Transactions on Power Electronics*, vol. 13, no. 5, pp. 892–902, 1998. Cited on page 12.

[59] D. Maksimovic and S. Dhar, "Switched-capacitor DC-DC converters for low-power on-chip applications," in *30th Annual IEEE Power Electronics Specialists Conference, 1999. PESC 99.*, vol. 1. IEEE, 1999, pp. 54–59. Cited on pages 12 and 14.

[60] Y. K. Ramadass and A. P. Chandrakasan, "Voltage scalable switched capacitor DC-DC converter for ultra-low-power on-chip applications," in *IEEE Power Electronics Specialists Conference, 2007. PESC 2007.* IEEE, 2007, pp. 2353–2359. Cited on pages 12 and 14.

[61] C. Lu, S. P. Park, V. Raghunathan, and K. Roy, "Low-overhead maximum power point tracking for micro-scale solar energy harvesting systems," in *25th International Conference on VLSI Design (VLSID), 2012*. IEEE, 2012, pp. 215–220. Cited on pages 12, 13, and 24.

[62] H. Shao, C.-Y. Tsui, and W.-H. Ki, "A micro power management system and maximum output power control for solar energy harvesting applications," in *Low Power Electronics and Design (ISLPED), 2007 ACM/IEEE International Symposium on*. IEEE, 2007, pp. 298–303. Cited on page 12.

[63] F. L. Luo and H. Ye, *Advanced DC/DC converters*. crc Press, 2004. Cited on page 13.

[64] N. Mohan and T. M. Undeland, *Power electronics: converters, applications, and design*. John Wiley & Sons, 2007. Cited on page 13.

[65] P. Favrat, P. Deval, and M. J. Declercq, "A high-efficiency CMOS voltage doubler," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 3, pp. 410–416, 1998. Cited on page 13.

[66] B. H. Calhoun and A. P. Chandrakasan, "Ultra-dynamic voltage scaling (UDVS) using sub-threshold operation and local voltage dithering," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 1, pp. 238–245, 2006. Cited on page 14.

[67] L. Yang, R. P. Dick, G. Memik, and P. Dinda, "HAPPE: Human and application-driven frequency scaling for processor power efficiency," *IEEE Transactions on Mobile Computing*, vol. 12, no. 8, pp. 1546–1557, 2013. Cited on page 14.

[68] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor DC-DC converters," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 841–851, 2008. Cited on pages 14, 43, 59, 67, 111, 112, and 115.

[69] C. Lu, S. P. Park, V. Raghunathan, and K. Roy, "Analysis and design of ultra low power thermoelectric energy harvesting systems," in *ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), 2010.* IEEE, 2010, pp. 183–188. Cited on page 14.

[70] T. Van Breussegem, M. Wens, E. Geukens, D. Geys, and M. Steyaert, "Area-driven optimisation of switched-capacitor DC/DC converters," *Electronics Letters*, vol. 44, no. 25, pp. 1488–1490, 2008. Cited on page 14.

[71] I. Doms, P. Merken, R. Mertens, and C. Van Hoof, "Integrated capacitive power-management circuit for thermal harvesters with output power 10 to 1000μW," in *IEEE International Solid-State Circuits Conference-Digest of Technical Papers, 2009. ISSCC 2009.* IEEE, 2009, pp. 300–301. Cited on page 14.

[72] C. Lu, S. P. Park, V. Raghunathan, and K. Roy, "Stage number optimization for switched capacitor power converters in micro-scale energy harvesting," in *Design, Automation & Test in Europe Conference & Exhibition (DATE), 2011.* IEEE, 2011, pp. 1–6. Cited on page 14.

[73] C. M. F. Carvalho, "CMOS indoor light energy harvesting system for wireless sensing applications," Ph.D. dissertation, Faculdade de Ciências e Tecnologia, 2014. Cited on pages 14, 17, 20, 22, 36, 81, 89, and 92.

[74] P. K. Peter and V. Agarwal, "On the input resistance of a reconfigurable switched capacitor DC-DC converter-based maximum power point tracker of a photovoltaic source," *IEEE Transactions on Power Electronics*, vol. 27, no. 12, pp. 4880–4893, 2012. Cited on page 14.

[75] Z. Pan, F. Zhang, and F. Z. Peng, "Power losses and efficiency analysis of multilevel DC-DC converters," in *Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, 2005. APEC 2005.*, vol. 3. IEEE, 2005, pp. 1393–1398. Cited on page 14.

[76] O.-Y. Wong, H. Wong, W.-S. Tam, and C.-W. Kok, "Topology, analysis, and CMOS implementation of switched-capacitor DC-DC converters," *Facta Universitatis, Series: Electronics and Energetics*, vol. 27, no. 1, pp. 41–56, 2014. Cited on page 14.

[77] Y. Kim, N. Chang, Y. Wang, and M. Pedram, "Maximum power transfer tracking for a photovoltaic-supercapacitor energy system," in *Proceedings of the 16th ACM/IEEE international symposium on Low power electronics and design.* ACM, 2010, pp. 307–312. Cited on pages 16 and 17.

[78] S. Sudevalayam and P. Kulkarni, "Energy harvesting sensor nodes: Survey and implications," *IEEE Communications Surveys & Tutorials*, vol. 13, no. 3, pp. 443–461, 2011. Cited on pages 16, 17, and 18.

[79] M. Glavin, P. K. Chan, S. Armstrong, and W. Hurley, "A stand-alone photovoltaic supercapacitor battery hybrid energy storage system," in *13th Power Electronics and Motion Control Conference, 2008. EPE-PEMC 2008.* IEEE, 2008, pp. 1688–1695. Cited on page 16.

[80] J. Dunlop and B. Farhi, "Recommendations for maximizing battery life in photovoltaic systems: a review of lessons learned," *Solar Engineering*, pp. 275–280, 2001. Cited on page 16.

[81] T. Hund, "Capacity loss in PV batteries and recovery procedures," *Sandia National Labs web site, Photovoltaic System Applications Dept., http://www. sandia. gov/pv/bos/batteries. htm*, 1999. Cited on page 16.

[82] P.-O. Logerais, O. Riou, M. A. Camara, and J.-F. Durastanti, "Study of photovoltaic energy storage by supercapacitors through both experimental and modelling approaches," *Journal of Solar Energy*, vol. 2013, 2013. Cited on page 16.

[83] J. Taneja, J. Jeong, and D. Culler, "Design, modeling, and capacity planning for micro-solar power sensor networks," in *Proceedings of the 7th international conference on Information processing in sensor networks*. IEEE Computer Society, 2008, pp. 407–418. Cited on pages 17 and 18.

[84] K. Naveen and S. Manjunath, "A reliable ultracapacitor based solar energy harvesting system for wireless sensor network enabled intelligent buildings," in *2nd International Conference on Intelligent Agent and Multi-Agent Systems (IAMA), 2011*. IEEE, 2011, pp. 20–25. Cited on pages 17 and 18.

[85] H.-Y. Huang, C. O. Mocorro, J. Pinaso, and K.-H. Cheng, "Indoor energy harvesting using photovoltaic cell for battery recharging," in *IEEE 16th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS), 2013*. IEEE, 2013, pp. 224–227. Cited on page 17.

[86] R. D. Prabha and G. A. Rincón-Mora, "Battery-assisted and photovoltaic-sourced switched-inductor CMOS harvesting charger-supply," in *IEEE International Symposium on Circuits and Systems (ISCAS), 2013*. IEEE, 2013, pp. 253–256. Cited on page 17.

[87] H. Shao, C.-Y. Tsui, and W.-H. Ki, "A single inductor DIDO DC-DC converter for solar energy harvesting applications using band-band control," in *18th IEEE/IFIP VLSI System on Chip Conference (VLSI-SoC), 2010*. IEEE, 2010, pp. 167–172. Cited on page 17.

[88] T.-H. Tsai and K. Chen, "A 3.4 mw photovoltaic energy-harvesting charger with integrated maximum power point tracking and battery management," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013*. IEEE, 2013, pp. 72–73. Cited on page 17.

[89] E. O. Torres and G. A. Rincón-Mora, "Long-lasting, self-sustaining, and energy-harvesting system-in-package (SiP) wireless micro-sensor solution," in *International Conference on Energy, Environment, and Disasters (INCEED), Charlotte, NC, USA*, 2005, pp. 1–33. Cited on page 17.

[90] J. Carmo, R. Rocha, A. Silva, L. Gonçalves, and J. Correia, "Integrated thin-film rechargeable battery in a thermoelectric scavenging microsystem," in *International Conference on Power Engineering, Energy and Electrical Drives, 2009. POWERENG'09.* IEEE, 2009, pp. 359–362. Cited on page 17.

[91] W. Rieutort-Louis, L. Huang, Y. Hu, J. Sanz-Robinson, S. Wagner, J. C. Sturm, and N. Verma, "A complete fully thin-film PV harvesting and power-management system on plastic with on-sheet battery management and wireless power delivery to off-sheet loads," *Photovoltaics, IEEE Journal of*, vol. 4, no. 1, pp. 432–439, 2014. Cited on page 18.

[92] X. Jiang, J. Polastre, and D. Culler, "Perpetual environmentally powered sensor networks," in *Fourth International Symposium on Information Processing in Sensor Networks, 2005. IPSN 2005.* IEEE, 2005, pp. 463–468. Cited on page 18.

[93] J. Jeong, X. Jiang, and D. Culler, "Design and analysis of micro-solar power systems for wireless sensor networks," in *5th International Conference on Networked Sensing Systems, 2008. INSS 2008.* IEEE, 2008, pp. 181–188. Cited on pages 18 and 20.

[94] H. Mahmood, D. Michaelson, and J. Jiang, "A power management strategy for PV/battery hybrid systems in Islanded Microgrids," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 4, pp. 870–882, 2014. Cited on page 18.

[95] F. Ongaro, S. Saggini, and P. Mattavelli, "Li-ion battery-supercapacitor hybrid storage system for a long lifetime, photovoltaic-based wireless sensor network," *IEEE Transactions on Power Electronics*, vol. 27, no. 9, pp. 3944–3952, 2012. Cited on page 18.

[96] S. Saggini, F. Ongaro, C. Galperti, and P. Mattavelli, "Supercapacitor-based hybrid storage systems for energy harvesting in wireless sensor networks," in *Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2010.* IEEE, 2010, pp. 2281–2287. Cited on page 18.

[97] J. Varley, M. Martino, S. Poshtkouhi, and O. Trescases, "Battery and ultra-capacitor hybrid energy storage system and power management scheme for solar-powered wireless sensor nodes," in *IECON 2012-38th Annual Conference on IEEE Industrial Electronics Society*. IEEE, 2012, pp. 4806–4811. Cited on page 18.

[98] T. Zhou and W. Sun, "Optimization of battery–supercapacitor hybrid energy storage station in wind/solar generation system," *Sustainable Energy, IEEE Transactions on*, vol. 5, no. 2, pp. 408–415, 2014. Cited on page 18.

[99] M. Hassanalieragh, T. Soyata, A. Nadeau, and G. Sharma, "Solar-supercapacitor harvesting system design for energy-aware applications," in *27th IEEE International System-on-Chip Conference (SOCC), 2014*. IEEE, 2014, pp. 280–285. Cited on page 18.

[100] A. Fahad, T. Soyata, T. Wang, G. Sharma, W. Heinzelman, and K. Shen, "SOLARCAP: super capacitor buffering of solar energy for self-sustainable field systems," in *IEEE International SOC Conference (SOCC), 2012*. IEEE, 2012, pp. 236–241. Cited on page 18.

[101] J. Sankman, H. Chen, and D. Ma, "Supercapacitor-based reconfigurable energy management unit for autonomous wireless sensor nodes," in *IEEE International Symposium on Circuits and Systems (ISCAS), 2011*. IEEE, 2011, pp. 2541–2544. Cited on pages 18 and 22.

[102] H. Yu and Q. Yue, "Indoor light energy harvesting system for energy-aware wireless sensor node," *Energy Procedia*, vol. 16, pp. 1027–1032, 2012. Cited on page 18.

[103] H. Chen, B. Wei, and D. Ma, "Energy storage and management system with carbon nanotube supercapacitor and multidirectional power delivery capability for autonomous wireless sensor nodes," *IEEE Transactions on Power Electronics*, vol. 25, no. 12, pp. 2897–2909, 2010. Cited on page 18.

[104] A. N. A. Ali, M. H. Saied, M. Mostafa, and T. Abdel-Moneim, "A survey of maximum PPT techniques of PV systems," *IEEE Energytech, USA, Cleveland*, pp. 1–17, 2012. Cited on pages 19, 21, and 22.

[105] A. Sayal, "MPPT techniques for photovoltaic system under uniform insolation and partial shading conditions," in *Students Conference on Engineering and Systems (SCES), 2012*. IEEE, 2012, pp. 1–6. Cited on page 19.

[106] S. Vignati, "Solutions for indoor light energy harvesting," Master's thesis, School of Information and Communication Technology KTH, 2012. Cited on pages 19, 22, 23, and 24.

[107] M. A. Masoum, H. Dehbonei, and E. F. Fuchs, "Theoretical and experimental analyses of photovoltaic systems with voltage and current-based maximum power-point tracking," *IEEE transactions on Energy conversion*, vol. 17, no. 4, pp. 514–522, 2002. Cited on page 19.

[108] I. Altas and A. Sharaf, "A novel fuzzy logic controller for maximum power extraction from a PV array driving a three-phase induction motor," in *7th Mediterranean Electrotechnical Conference, 1994. Proceedings.* IEEE, 1994, pp. 853–856. Cited on pages 19 and 20.

[109] L. Zhang, A. Al-Amoudi, and Y. Bai, "Real-time maximum power point tracking for grid-connected photovoltaic systems," in *Power Electronics and Variable Speed Drives, 2000. Eighth International Conference on (IEE Conf. Publ. No. 475)*, 2000, pp. 124–129. Cited on page 19.

[110] A. Al-Amoudi and L. Zhang, "Optimal control of a grid-connected PV system for maximum power point tracking and unity power factor," in *Seventh International Conference on (Conf. Publ. No. 456) Power Electronics and Variable Speed Drives, 1998.* IET, 1998, pp. 80–85. Cited on page 19.

[111] H. M. Mashaly, A. M. Sharaf, M. Mansour, and A. A. El-Sattar, "A photovoltaic maximum power tracking using neural networks," in *Proceedings of the Third IEEE Conference on Control Applications, 1994.* IEEE, 1994, pp. 167–172. Cited on page 20.

[112] I. Y. Chung and Y. C. Liang, "A low-cost photovoltaic energy harvesting circuit for portable devices," in *IEEE Ninth International Conference on Power Electronics and Drive Systems (PEDS), 2011.* IEEE, 2011, pp. 334–339. Cited on pages 20, 21, and 23.

[113] M. A. Eltawil and Z. Zhao, "MPPT techniques for photovoltaic applications," *Renewable and Sustainable Energy Reviews*, vol. 25, pp. 793–813, 2013. Cited on page 20.

[114] Y. Jung, J. So, G. Yu, and J. Choi, "Improved perturbation and observation method (IP&O) of MPPT control for photovoltaic power systems," in *Photovoltaic Specialists Conference, 2005. Conference Record of the Thirty-first IEEE.* IEEE, 2005, pp. 1788–1791. Cited on page 20.

[115] B. Subudhi and R. Pradhan, "A comparative study on maximum power point tracking techniques for photovoltaic power systems," *Sustainable Energy, IEEE Transactions on*, vol. 4, no. 1, pp. 89–98, 2013. Cited on pages 20, 21, and 22.

[116] R. Faranda and S. Leva, "Energy comparison of MPPT techniques for PV systems," *WSEAS transactions on power systems*, vol. 3, no. 6, pp. 446–455, 2008. Cited on page 20.

[117] V. Raghunathan and P. H. Chou, "Design and power management of energy harvesting embedded systems," in *Proceedings of the 2006 international symposium on Low power electronics and design*. ACM, 2006, pp. 369–374. Cited on page 20.

[118] S. Mashohor, K. Samsudin, A. M. Noor, and A. R. A. Rahman, "Evaluation of genetic algorithm based solar tracking system for photovoltaic panels," in *IEEE International Conference on Sustainable Energy Technologies, 2008. ICSET 2008.* IEEE, 2008, pp. 269–273. Cited on page 20.

[119] N. Femia, G. Petrone, G. Spagnuolo, and M. Vitelli, "Optimization of perturb and observe maximum power point tracking method," *IEEE Transactions on Power Electronics*, vol. 20, no. 4, pp. 963–973, 2005. Cited on page 21.

[120] M. Lokanadham and K. V. Bhaskar, "Incremental conductance based maximum power point tracking (MPPT) for photovoltaic system," *International Journal of Engineering Research and Applications (IJERA)*, vol. 2, no. 2, pp. 1420–1424, 2012. Cited on page 21.

[121] H. N. Zainudin and S. Mekhilef, "Comparison study of maximum power point tracker techniques for pv systems," in *Proceedings of the 14th International Middle East Power Systems Conference (MEPCON'10)*, 2010. Cited on pages 21 and 22.

[122] S. S. Kondawar and U. Vaidya, "A comparison of two MPPT techniques for PV system in Matlab Simulink," *International Journal of Engineering Research and Development*, vol. 2, no. 7, pp. 73–79, 2012. Cited on pages 21 and 22.

[123] A. R. Reisi, M. H. Moradi, and S. Jamasb, "Classification and comparison of maximum power point tracking techniques for photovoltaic system: A review," *Renewable and Sustainable Energy Reviews*, vol. 19, pp. 433–443, 2013. Cited on page 21.

[124] B. Ankaiah and J. Nageswararao, "Enhancement of solar photovoltaic cell by using short-circuit current MPPT method," *International Journal of Engineering Sciences Invention*, vol. 2, no. 2, pp. 45–50, 2013. Cited on page 21.

[125] F. Sedaghati, A. Nahavandi, M. A. Badamchizadeh, S. Ghaemi, and M. Abedinpour Fallah, "Pv maximum power-point tracking by using artificial neural network," *Mathematical Problems in Engineering*, vol. 2012, 2012. Cited on page 21.

[126] Y.-H. Chang and C.-Y. Chang, "A maximum power point tracking of PV system by scaling fuzzy control," in *International MultiConference of Engineers and Computer Scientists, Hong Kong*. Citeseer, 2010. Cited on page 21.

[127] R. Leyva, C. Alonso, I. Queinnec, A. Cid-Pastor, D. Lagrange, and L. Martinez-Salamero, "MPPT of photovoltaic systems using extremum-seeking control," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 42, no. 1, pp. 249–258, 2006. Cited on page 21.

[128] M. H. Moradi and A. R. Reisi, "A hybrid maximum power point tracking method for photovoltaic systems," *Solar Energy*, vol. 85, no. 11, pp. 2965–2976, 2011. Cited on page 21.

[129] K. Kobayashi, I. Takano, and Y. Sawada, "A study of a two stage maximum power point tracking control of a photovoltaic system under partially shaded insolation conditions," *Solar energy materials and solar cells*, vol. 90, no. 18, pp. 2975–2988, 2006. Cited on page 21.

[130] M. A. De Brito, L. P. Sampaio, G. Luigi, C. Canesin *et al.*, "Comparative analysis of MPPT techniques for PV applications," in *International Conference on Clean Electrical Power (ICCEP), 2011*. IEEE, 2011, pp. 99–104. Cited on page 21.

[131] S. Jain and V. Agarwal, "A new algorithm for rapid tracking of approximate maximum power point in photovoltaic systems," *IEEE Power Electronics Letters*, vol. 2, no. 1, pp. 16–19, 2004. Cited on page 21.

[132] T. Esram, P. L. Chapman *et al.*, "Comparison of photovoltaic array maximum power point tracking techniques," *IEEE Transactions on Energy Conversion EC*, vol. 22, no. 2, p. 439, 2007. Cited on page 22.

[133] T. Esram, J. W. Kimball, P. T. Krein, P. L. Chapman, and P. Midya, "Dynamic maximum power point tracking of photovoltaic arrays using ripple correlation control," *IEEE Transactions on Power Electronics*, vol. 21, no. 5, pp. 1282–1291, 2006. Cited on page 22.

[134] Y. Nakase, Y. Ido, T. Oishi, T. Kumamoto, and T. Shimizu, "Wide input range from 80mV to 3V operation on-chip single-inductor dual-output (SIDO) DC-DC boost converter with self-adjusting clock duty for sensor network applications," in *IEEE Asian Solid-State Circuits Conference (A-SSCC), 2013*. IEEE, 2013, pp. 41–44. Cited on page 22.

[135] J. Kim, P. K. Mok, and C. Kim, "A 0.15 v input energy harvesting charge pump with dynamic body biasing and adaptive dead-time for efficiency improvement," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 2, pp. 414–425, 2015. Cited on page 22.

[136] H. Kim, S. Kim, C.-K. Kwon, Y.-J. Min, C. Kim, and S.-W. Kim, "An energy-efficient fast maximum power point tracking circuit in an 800-μW photovoltaic energy harvester," *IEEE Transactions on Power Electronics*, vol. 28, no. 6, pp. 2927–2935, 2013. Cited on page 22.

[137] D. Shmilovitz, "On the control of photovoltaic maximum power point tracker via output parameters," *IEE Proc.-Electr. Power Appl*, vol. 152, no. 2, p. 239, 2005. Cited on pages 22 and 23.

[138] K. S. Kumari, V. Prema, K. U. Rao, and P. Meena, "Efficient MPPT for a stand-alone photovoltaic system," in *International Conference on Renewable Energy and Sustainable Energy (ICRESE), 2013*. IEEE, 2013, pp. 213–220. Cited on page 23.

[139] E. Durán, J. Andújar, J. Enrique, and J. Pérez-Oria, "Determination of PV generator IV/PV characteristic curves using a DC-DC converter controlled by a virtual instrument," *International Journal of Photoenergy*, vol. 2012, 2012. Cited on page 23.

[140] Y. Jiang and J. Abu Qahouq, "Study and evaluation of load current based MPPT control for PV solar systems," in *IEEE Energy Conversion Congress and Exposition (ECCE), 2011*. IEEE, 2011, pp. 205–210. Cited on page 23.

[141] R. Muhida, M. Park, M. Dakkak, K. Matsuura, A. Tsuyoshi, and M. Michira, "A maximum power point tracking for photovoltaic-SPE system using a maximum current controller," *Solar energy materials and solar cells*, vol. 75, no. 3, pp. 697–706, 2003. Cited on page 23.

[142] L. Yin, X. Wu, C.-L. Chen, and L.-c. Cheng, "Dynamically self-adaptive load current maximization technique for maximum power point tracking in photovoltaic arrays," in *International Conference of Electron Devices and Solid-State Circuits (EDSSC), 2011.* IEEE, 2011, pp. 1–2. Cited on page 23.

[143] M. Miyatake, F. Toriumi, T. Endo, and N. Fujii, "A novel maximum power point tracker controlling several converters connected to photovoltaic arrays with particle swarm optimization technique," in *European conference on power electronics and applications, 2007*. IEEE, 2007, pp. 1–10. Cited on page 23.

[144] D. B. Snyman and J. H. Enslin, "Simplified maximum power point controller for PV installations," in *Conference Record of the Twenty Third IEEE Photovoltaic Specialists Conference, 1993.* IEEE, 1993, pp. 1240–1245. Cited on page 23.

[145] C. R. Sullivan and M. J. Powers, "A high-efficiency maximum power point tracker for photovoltaic arrays in a solar-powered race vehicle," in *24th Annual IEEE Power Electronics Specialists Conference, 1993. PESC'93 Record.* IEEE, 1993, pp. 574–580. Cited on page 23.

[146] A. Kislovski and R. Redl, "Maximum-power-tracking using positive feedback," in *25th Annual IEEE Power Electronics Specialists Conference, PESC'94 Record.* IEEE, 1994, pp. 1065–1068. Cited on page 23.

[147] Digi-Key, "IXYS SLMD121H04L," 2015, available at http://www.digikey.com/product-detail/en/SLMD121H04L/SLMD121H04L-ND/3463124. Cited on page 32.

[148] C. Corporation, "Cymbet CBC-PV-01," 2015, available at http://www.cymbet.com/pdfs/DS-72-24.pdf. Cited on page 32.

[149] Sanyo, "Amorphous sillicon solar cells," 2015, available at http://panasonic.net/energy/amorton/en/pdf/EP120B.pdf. Cited on page 32.