UNIVERSIDADE DO PORTO
FACULDADE DE ENGENHARIA
DEEC

CAMA DE TESTE PARA MÓDULOS E COMPONENTES ELECTRÓNICOS

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Porto, Dezembro de 1993

PRODEP

MEDIDA 4.3 - Estágios Profissionais para Bacharelatos, Licenciaturas e Pós-Graduação

PARECER

Assunto: Estágios de
(1.38) Alberto Xavier Pires Borges da Cunha
(1.42) José Carlos Lobinho Gomes
(1.44) Manuel Fernando dos Santos Silva
(1.48) Pedro Manuel Gonçalves Campelos de Sousa Lobo.

Na qualidade de supervisores dos estágios acima mencionados e em face do trabalho desenvolvido e relatado pelos estagiários pode concluir-se que:

1- Os estagiários manifestaram entusiasmo e dedicação na execução do trabalho intitulado:

" Projecto de uma cama de testes para componentes e módulos electrónicos incluindo a concepção da interface (entradas e saídas) e do sistema operativo".

O trabalho consistiu no projecto e teste em montagem experimental de vários módulos cujas responsabilidades foram distribuidas:

Software para interface com o utilizador em PC - Manuel Fernando dos Santos Silva; "device driver" para interface software/hardware - José Carlos Lobinho Gomes; hardware de teste com microcontrolador, conversão e software operativo - Manuel Fernando dos Santos Silva e Pedro Manuel Gonçalves Campelos de Sousa Lobo.

Nesta execução revelaram apreciáveis qualidades de trabalho que mais desenvolveram. Do trabalho resultou um protótipo do hardware em "breadboard" e protótipos dos módulos de software.

2- No cumprimento dos objectivos propostos, os estagiários revelaram bons conhecimentos científicos e técnicos, capacidade de aplicação desses conhecimentos e espírito de iniciativa. A metodologia seguida consistiu no estudo da proposta base, desenvolvimento por análise das especificações do sistema objecto, projecto de soluções tecnicamente adequadas eventualmente inovadoras, implementação de protótipos e validação do projecto.

pelo que somos do parecer que foram cumpridos os objectivos que o estágio se propunha atingir.

Prof. Doutor António Maria da Rocha Quintas
Centro de CIM do Porto

Prof. Doutor Diamantino Rui da Silva Freitas
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0 INDÍCE

1 INTRODUÇÃO

Foi feito um estudo de uma cama de testes para componentes e circuitos electrónicos. Com esta é possível analisar circuitos (ou componentes) electrónicos pela injecção de sinais, através de agulhas, em pontos específicos escolhidos pelo utilizador, e receber sinais de volta através de um outro conjunto de agulhas. Pela análise desses sinais é possível estudar o comportamento dos elementos em observação. Assim é permitido o teste de componentes ou circuitos à distância, sem necessidade de os retirar dos sistemas maiores em que possam estar inseridos.

2 DESCRIÇÃO BREVE DAS OUTRAS PARTES

Este trabalho foi dividido em três grandes grupos que são:

- geração e processamento de sinais
- driver de interface entre o computador e o hardware exterior
- circuito responsável pela gestão e encaminhamento dos sinais

A geração e processamento de sinais é responsável pela interface com o utilizador, criar os sinais que irão ser enviados para o circuito que está a ser testado, recepção das amostras com origem nele e análise dos resultados. Estes sinais são enviados para o driver que se encarrega da transmissão série, via RS232C, para o hardware exterior.

O utilizador tem à sua disposição o menú principal:

Qual a operação que pretende executar?

0- Gerar sinal
1- Enviar sinal
2- Receber sinal
3- Enviar e receber simultâneamente um sinal
4- Visualizar um sinal
5- Somar sinais
6- Subtrair sinais
7- Multiplicar sinais
8- Introduzir componente contínua no sinal
9- Aumentar a amplitude de um sinal
10- Convolução de sinais
11- FFT de sinais
12- Espectro de densidade de potência
13- Alterar intervalo de visualização
14- Fazer o reset de sinais
15- Abandonar o programa

Qual a sua opção?

A opcão 0 tem o seguinte sub-menú:

Que tipo de onda pretende gerar?

1- Onda sinusoidal
2- Onda quadrada
3- Onda tringular
4- Onda dente de serra
5- Seno cardinal
6- Impulso rectangular
7- Impulso Gaussiano
8- Componente contínua
9- Impulso de Dirac
10- Degrau de Heaviside
11- Onda exponêncial

Qual a sua opção?

A opção 4 tem o seguinte sub-menú:

Que tipo de visualização pretende efectuar?

1- Visualizar uma onda
2- Visualizar uma onda e a sua FFT
3- Visualizar duas ondas
4- Visualizar duas ondas e as respectivas FFTs
5- Visualizar uma FFT
6- Visualizar o resultado de uma convolução

Qual a sua opção?

O driver de interface com o exterior tem como função tornar a comunicação, com o hardware de gestão e encaminhamento dos sinais, transparente ao programa responsável pela interface com o utilizador. Ou seja, o programa anterior, vê o driver como um simples ficheiro no qual escreve os sinais. O driver é que se encarrega de os configurar e fazer a transmissão série. Na recepção faz o processo inverso, ou seja, recebe os sinais via porta série, configura-os e quando o programa do nível superior os pretende receber limita-se a ler como se fosse um ficheiro. O driver comunica com a placa de hardware através de uma das portas série (COM1,..., COM4).

O circuito responsável pela gestão e encaminhamento dos sinais vem descrito em seguida.

3 ENCAMINHAMENTO DOS SINAIS

A sequência de acções é despoletada por um comando enviado pelo PC via RS232C. Se este comando for o de início de mensagem então são executadas as seguintes acções:

- lê uma mensagem através da porta série, oriunda do PC, e armazena-a na memória de dados

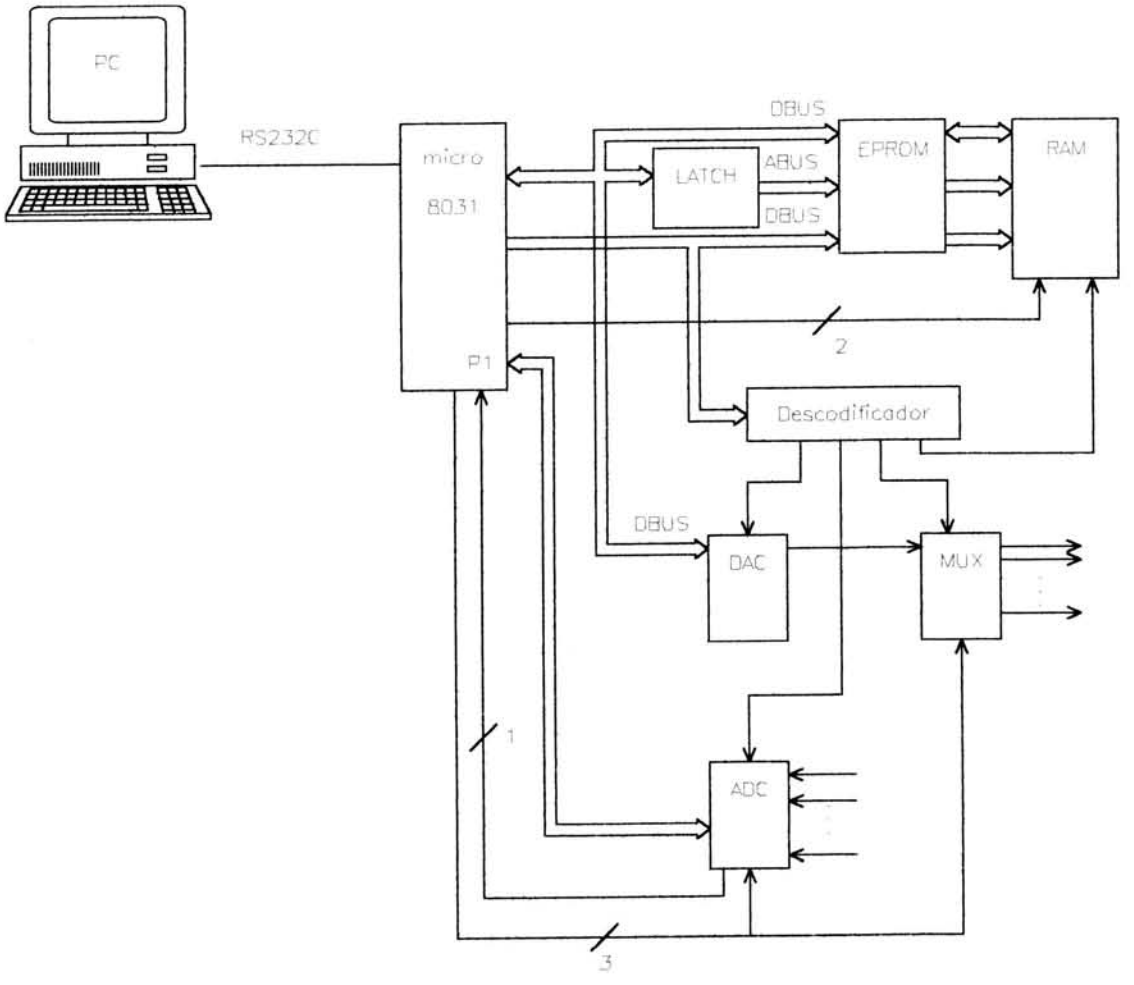
- a mensagem é descodificada para um formato "legível" pelo DAC, rearmazenada na memória, compactando a informação e ficando apta para transmissão imediata

- estas amostras são enviadas para as agulhas de saída, através do DAC e MUX. "Simultâneamente" são lidos os sinais de entrada via ADC e as amostras são armazenadas na memória. A gestão destas acções é efectuada pelo micro através do descodificador.

- quando todas as amostras são enviadas para a saída, procede-se à codificação das amostras recolhidas com o posterior envio para o PC via RS232C

Em seguida procede-se a uma análise mais detalhada do hardware e software usados.

3.1 DESCRIÇÃO DO HARDWARE



3.1.1 Bloco de memória

Este é constituido por 2 memórias. Uma Eprom onde vai ser guardado o programa a executar e uma RAM de 32 Kbytes para dados.

A memória RAM tem de ser de 32 Kbytes para ser possível armazenar ao mesmo tempo 8 sinais de entrada, amostrados 1000 vezes cada um, e 8 sinais de saida, amostrados tambem 1000 vezes cada um. Isto só e possivel porque apesar de as amostras virem em grupos de três caractéres ASCII, o programa vai fazer a sua conversão para binário antes de começar a injectar os sinais no circuito, armazenando tambem as amostras em binário. Quando for a enviar os dados para o PC faz a operação inversa convertendo os dados de binário para ASCII. Para mais detalhes ver parte do fluxograma.

Para termos memória superior a 8 bits de endereçamento há que compartilhar o barramento de dados usando para isso um latch.

3.1.2 Bloco de descodificação

Este bloco teve de ser criado para resolver o problema do número de linhas de controlo. Isto porque se quisessemos usar linhas de controlo dedicadas, seriam precisas:

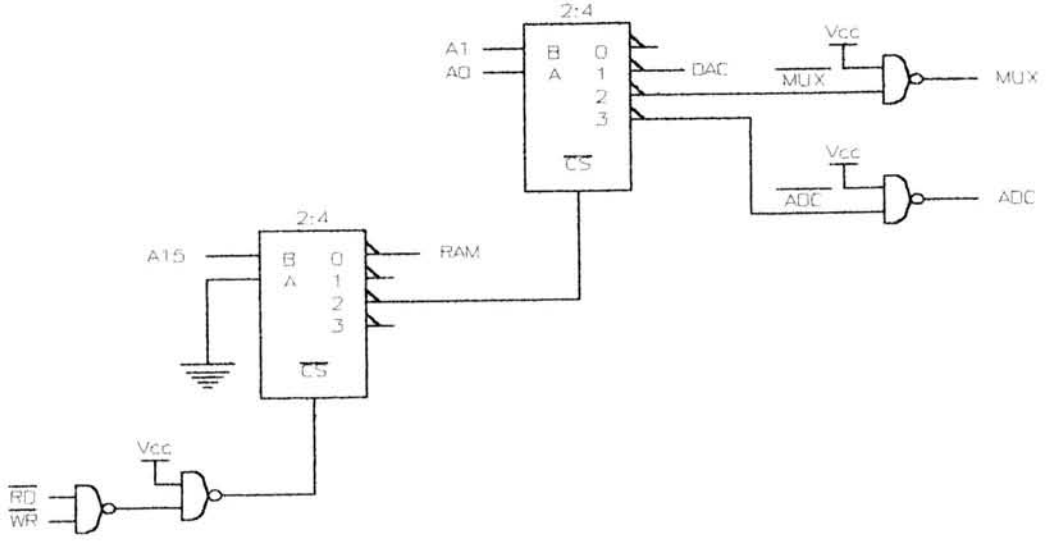
2 linhas para as memórias	/RD e /WR
1 linha para o D/A	/CS ou /WR
3 linhas de endereçamento para o MUX	INB, A, B e C
5 linhas para o controlo do A/D	/CS, /RD, /WR, AO e /EOC
2 linhas de comunicação série	Txd e Rxd

O que dá um total de 14 linhas. Como, para além destas vão ser usadas mais as 8 da porta P1 como barramento de dados para o A/D, e as portas P0 e P2 estão reservadas como barramento de dados e endereços para a memória, sobra a porta P3 com 8 linhas o que é manifestamente pouco.

Para resolver este problema fomos obrigados a compartilhar algumas das linhas. Como quatro linhas de P3 estão reservadas (Txd, Rxd, /RD e /WR) sobram quatro, como /EOC é a única de entrada apenas podemos compartilhar três (/RD, /WR e AO do A/D e A, B e C do MUX), isto obriga-nos a ter um só bloco activo de cada vez tornando obrigatória a existência de duas linhas de selecção independentes. O número de linhas necessárias foi reduzido para 11, sendo ainda assim demasiado elevado. Para solucionarmos isto recorremos a um artificio que é a habilitação/desabilitação de cada componente através do acesso a uma posição de memória para cada um. O mapeamento da memória é o seguinte:

	A_{15}	A_{14}	A_{13}	...	A_2	A_1	A_0
RAM	**0**	0	0	...	0	0	0
	0	1	1		1	1	1
D/A	**1**	1	1	...	1	**0**	**1**
MUX	**1**	1	1	...	1	**1**	**0**
A/D	**1**	1	1	...	1	**1**	**1**

O circuito de descodificação está descrito em baixo e efectua descodificação parcial.



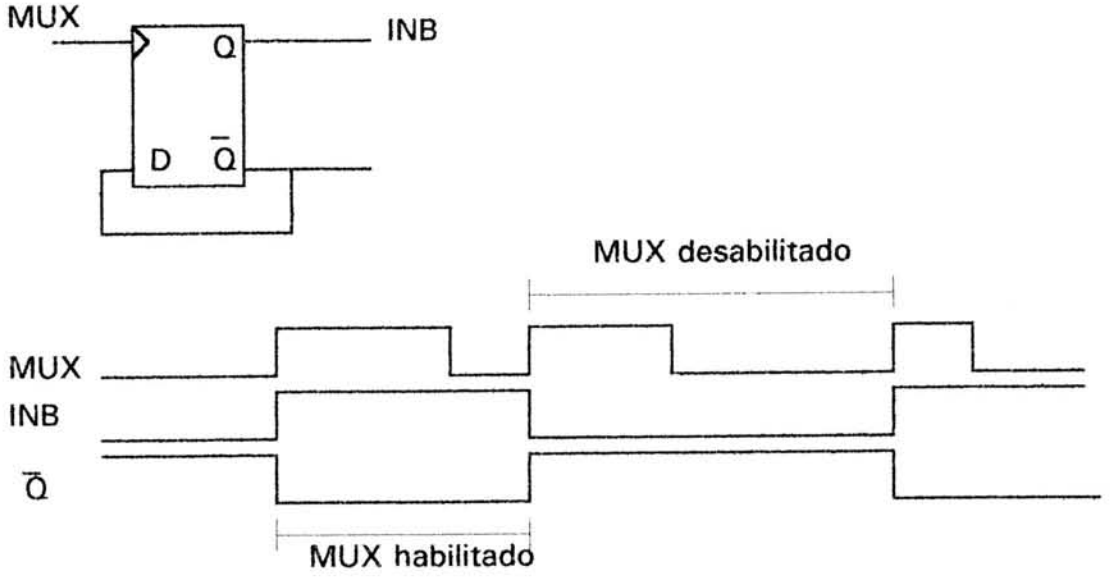
Mais adiante, na descrição dos blocos de entrada e saída, veremos de uma forma mais detalhada como este controlo é efectuado na prática.

3.1.3 Bloco de saída

Aqui temos dois componentes principais, um conversor D/A de 8 bits e um Multiplexer/Desmultiplexer analógico.

O conversor possui um latch de entrada sendo feita a sua actualização pela linha /WR e sua inibição pela linha /CS. Assim que as saídas do latch são actualizadas é feita a conversão e, enquanto este estiver habilitado, o valor é mantido fixo na saída até à próxima actualização. O multiplexer/desmultiplexer analógico só vai funcionar como desmultiplexer já que se pretende o encaminhamento de uma entrada para uma das saídas. A selecção do canal de saída é feita por 3 linhas e além destas, existe mais uma de inibição.

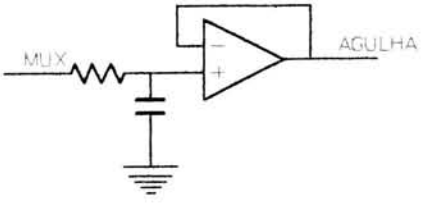
Para além destes dois componentes principais, é necessário um flip-flop tipo D, no nosso caso com linhas de set, reset e disparo ao flanco ascendente. A função do flip-flop é guardar o sinal de habilitação do MUX pois a sua activação é feita por um acesso à memória, na posição $FFFE_H$, e este está activo apenas durante o acesso. Com o flip-flop ligado da seguinte maneira e inicializando-o com um reset, a sequência dos sinais é a que se pode observar.



O programador tem de ter o cuidado de verificar que o 1° acesso a essa memória habilita o MUX, o 2° desabilita-o, e assim sucessivamente.

Quanto ao DAC este foi mapeado na posição $FFFD_H$. Para fazer a conversão D/A basta escrever nesta posição de memória a palavra a descodificar. Pode-se fazer isto pois o tempo de conversão é inferior a um ciclo de acesso à memória.

Cada saída do multiplexer está ligada a um circuito Sample&hold cuja missão é manter o sinal num nível o mais constante possível até à próxima actualização do valor dessa agulha.



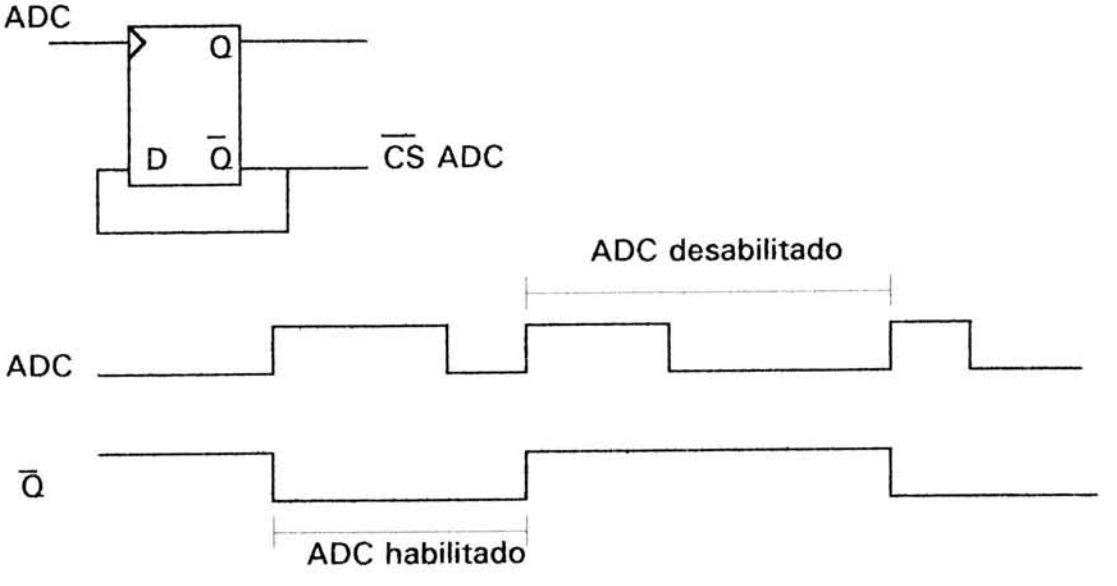
Este é um circuito muito simples, mas eficaz. Caso se pretendessem melhores características, poder-se-ia optar pela utilização de um dos seguintes integrados; o SHC76, o SHC85, o LF398H, etc.

3.1.4 Bloco de entrada

O elemento principal é o conversor μPD7004 . É um conversor A/D de 10 bits, que usa o método das aproximacões sucessivas e contém 8 canais analógicos de entrada multiplexados, bem como um circuito de interface para microcomputador. Além disso é programável permitindo dois modos de comunicação série e uma comunicação paralela de 8 bits com saída em binário normal ou em complemento para dois. O controlo é feito por 4 linhas (MC, AO, /RD, /WR), mais uma de handshake (/EOC).

É necessário fazer a inicialização do conversor que no modo paralelo é feita pelo barramento de dados, onde o bit 2 escolhe o tipo de saída (Binário ou Complemento para dois) e os bits 1 e 0 escolhem a frequência interna do clock. A selecção do canal de entrada também é feita através do barramento de dados. No modo série a inicialização é feita alterando valores de certos pinos de entrada. Para mais detalhes ver folha de características em anexo. Como no nosso caso vamos trabalhar somente em modo paralelo o pino MC está directamente ligado a Vcc.

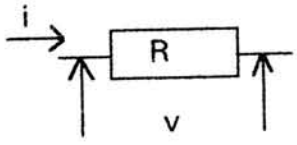
A habilitação do conversor A/D faz-se com um acesso à posição de memória $FFFF_H$. Temos assim um caso idêntico ao do multiplexer, onde mesmo depois de se aceder à memória é preciso manter o sinal. Uma vez mais resolve-se o problema usando um flip-flop tipo D (ver figura ....).



Da parte do hardware deve-se ter especial cuidado na escolha dos flip-flop's da familia 74 porque não é possivel utilizar o L74 pois este tem um tempo de set-up demasiado elevado, só lhe permitindo trabalhar a uma frequência máxima de 3MHz.

Entre a agulha e o DAC poderá ligar-se em caso de necessidade um circuito condicionador de sinal, tanto para amplificar ou atenuar sinais. Para amplificar o sinal poder-se ia utilizar o integrado AD625 que consiste num amplificador de instrumentação com ganho regulável.

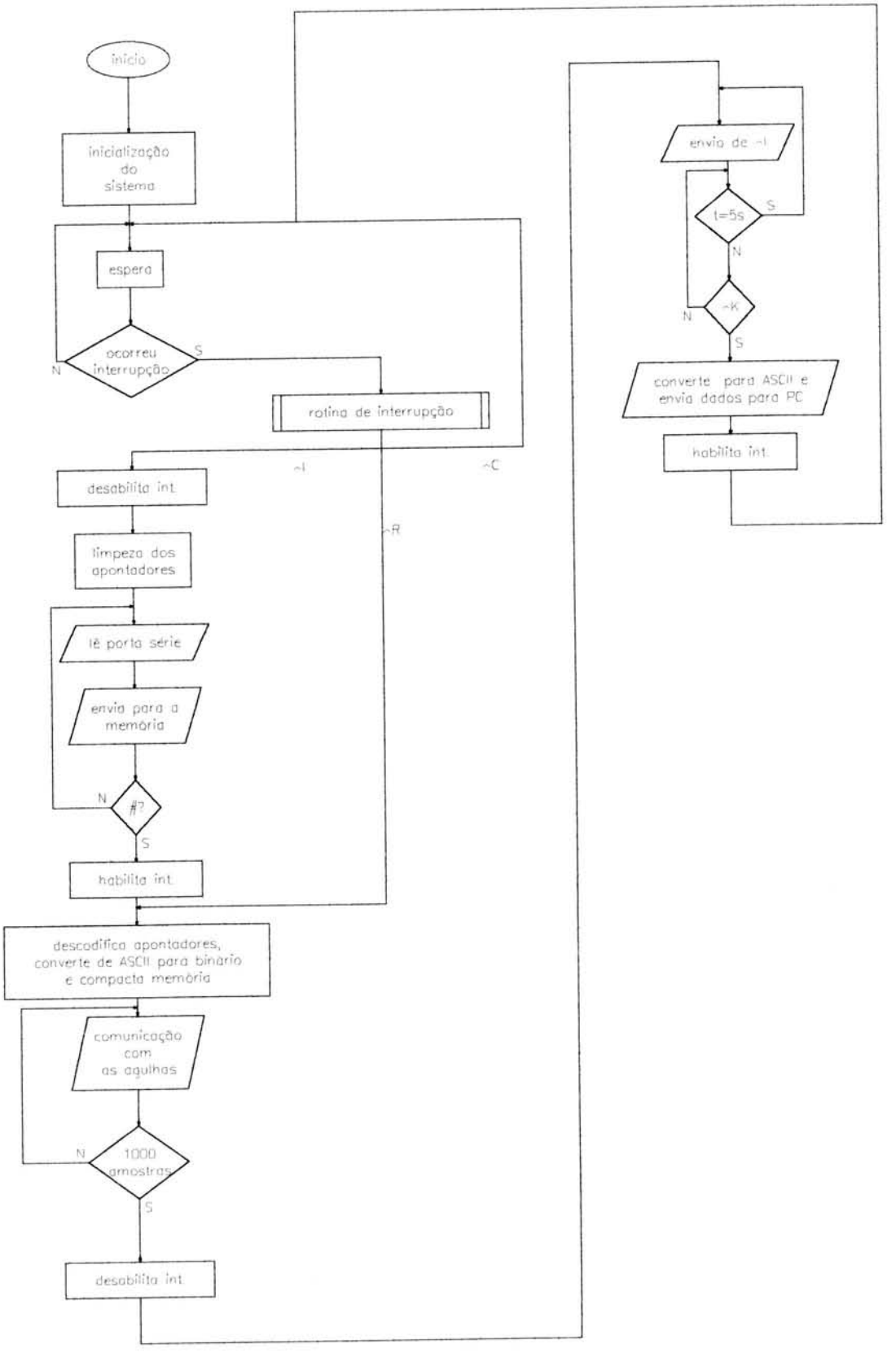
Este bloco apenas permite ler sinais em tensão. Para se ler valores em corrente é necessário fazer primeiro a transformação do sinal em tensão, isto através do uso de uma resistência inserida no circuito do seguinte modo:



Esta resistência interessa ser de valor muito pequeno, tanto para diminuir a dissipação como para atenuar o efeito de carga. Assim neste caso será fundamental o uso de um circuito de amplificação como o descrito acima.

As agulhas de entrada estão isoladas do circuito através do uso de buffer's de isolamento.

3.2 DESCRIÇÃO DO SOFTWARE DO 8031



3.2.1 Inicialização do sistema

Neste conjunto de instruções é feita a inicialização do microcontrolador 8031 e do conversor A/D μPD 7004.

O A/D é inicializado enviando pelo barramento de dados, durante um ciclo de escrita no componente e com o AO activo, a palavra 04_H. Este valor configura o A/D para trabalhar com um clock interno de 1/1 do externo, bem como o formato de saída binário em complemento para dois.

3.2.2 Limpeza dos apontadores

Temos um conjunto de apontadores Apx (com x = 1..8). Cada um deles guarda o endereço da primeira amostra do sinal a ser enviado pela agulha x. Aqui eles vão ser limpos colocando-os a zero.

3.2.3 Descodifica apontadores, converte de ASCII para binário e compacta memória

O formato da mensagem enviada pelo PC é a seguinte:

N°envios	:	N°agulha	;	1000amostras	:	N°agulha	...	N°envios	:	N°agulha	;	...	#		

Os dados estão em código ASCII. Cada amostra é constituida por quatro bytes, sendo o primeiro de sinal e os três últimos dão a amplitude em permilagem da alimentação do circuito a ser testado (± 0-999). Este método torna o sinal independente da alimentação do circuito que está a ser testado.

Além desta mensagem existem outras, de controlo, que são:

^R - **R**eset
^C - **C**lear
^S - **S**top
^I - **I**nicialização
^r - **r**esume
^K - **OK**

Neste bloco de instruções a mensagem é lida sequencialmente até ao **#.**

- Quando encontra **N° agulha** actualiza apontador respectivo com endereço X. Em que o X = 1H para a primeira amostra.

- Lê quatro caracteres (de um byte cada) e converte-os para binário em complemento para dois.
- Guarda-os sequencialmente a partir da posição de memória indicada pelo apontador Apx.

- Estes dois últimos passos são executados 1000 vezes.

- Actualiza apontador correspondente à próxima agulha com X+1000.

- Estes ciclos são executados um número de vezes correspondente ao **Nº envios**.

- Finalmente lê a segunda parte da mensagem correspondente às agulhas por onde vão ser recebidos os sinais. Guarda os números delas em registos internos.

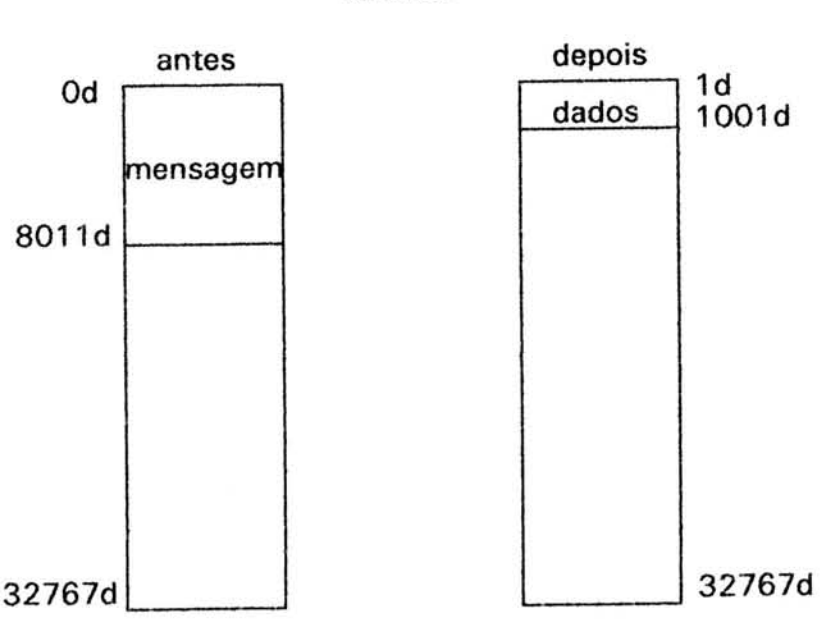
Consideremos a seguinte mensagem como exemplo:

2:3;.....:1;.....:1:1#

Neste caso os apontadores ficam com os seguintes valores:

- Ap2=Ap4=Ap5=Ap6=Ap7=Ap8=0
- Ap3=1_D
- Ap1=1001_D

Assim esta mensagem que ocupava inicialmente 8012 bytes passou a ocupar apenas 2000 bytes.



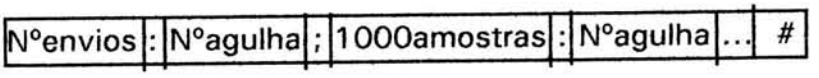
Foi feita esta compactação por duas razões:

- Para ser possível ter em simultâneo até um máximo de oito sinais de entrada e oito de saída. De facto se esta compactação não fosse feita, para oito entradas seria necessário ter $8 \times 4 \times 1000 = 32000$ bytes só para as amostras.

- Após esta compactação os dados de saída estão prontos para envio imediato para o bloco de saída optimizando tempos de transmissão. Assim o sample&hold não precisa de ter uns requisitos tão apertados.

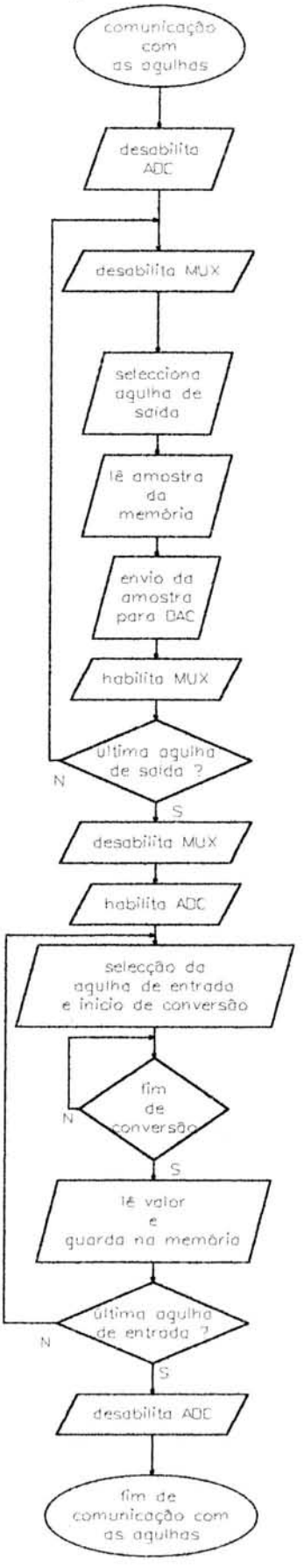
3.2.4 Converte para ASCII e envia para PC

A mensagem enviada para o PC tem o seguinte formato:



Neste conjunto de instruções cada amostra, em complemento para dois, é lida; convertida para 4 códigos ASCII (sendo o primeiro de sinal) e enviados directamente para o PC. Isto é, não há armazenamento na memória em códigos ASCII.

3.2.5 Comunicação com as agulhas

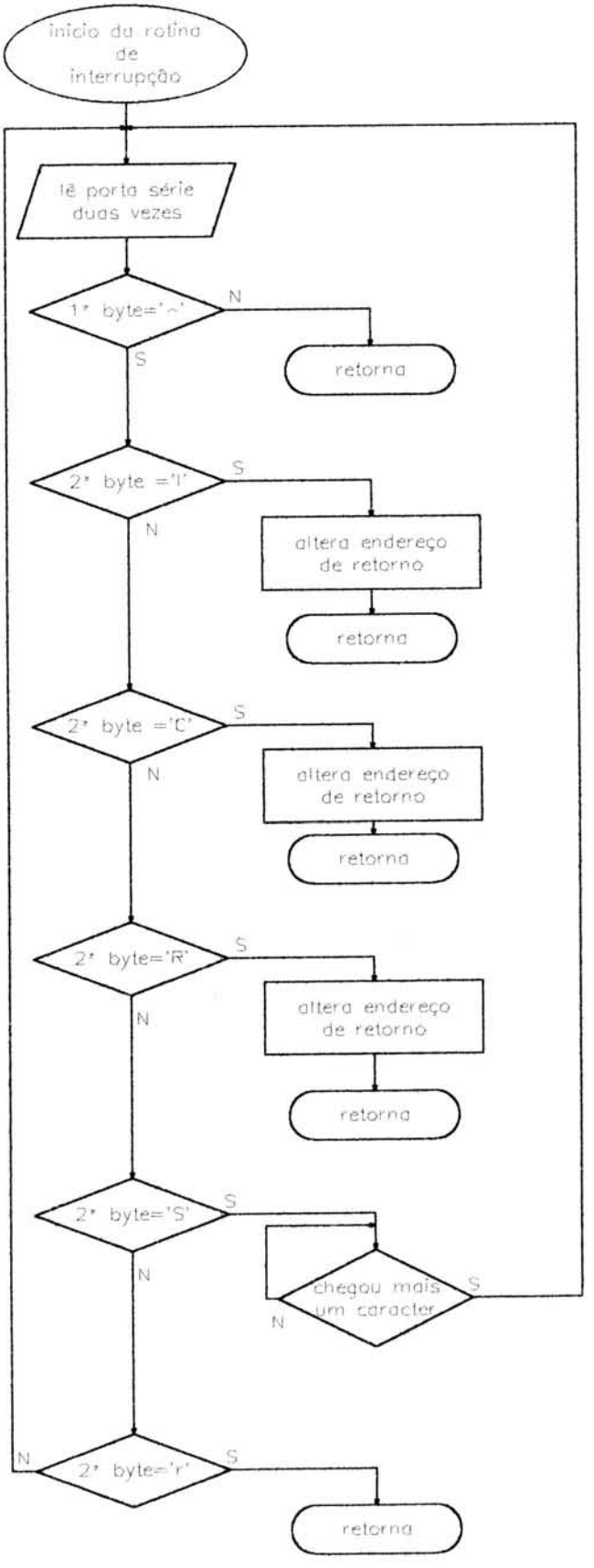


O conversor A/D é de 10 bits, no entanto apenas vamos aproveitar os 8 bits mais significativos, o que vai implicar uma diminuição da resolução de um valor equivalente a 4 LSB. Isto é equivalente a usar um conversor de 8 bits. Se fossem usados os 10 bits teriamos que fazer duas leituras ao conversor. Na primeira obtêm-se os 8 bits mais significativos, na segunda os restantes (para uma descrição mais pormenorizada ver as folhas fornecidas pelo fabricante que se encontram em anexo).

Os valores lidos de cada uma das agulhas de entrada são armazenados em blocos de memória pré-definidos que são:

Nº de agulha	Ínicio	Fim
1	3FFFh	43E7h
2	43E8h	47CFh
3	47D0h	4BB7h
4	4BB8h	4F9Fh
5	4FA0h	5387h
6	5388h	576Fh
7	5770h	5B57h
8	5B58h	5F3Fh

3.2.6 Rotina de interrupção



Para se alterar o endereço de retorno é preciso fazer dois pop's à stack para retirar o endereço de retorno anterior, e em seguida fazer dois push's com o novo valor de retorno. Este valor é conhecido e é o endereço da primeira instrução do bloco que desejamos executar. Este valor vai, no entanto, depender da localização do programa na memória.

4 LISTA DE MATERIAL

1- Microcontrolador 8031

1- ADC μPD7004

1- DAC AD7524

1- MUX/DEMUX CD4052B

1- RAM 51256 (32 Kbytes)

1- EPROM 2764 (8 Kbytes)

1- 74LS00 (NAND's)

1- 74LS04 (NOR's)

1- 74LS74 (FLIP-FLOP)

1- 74LS139 (conversor 2:4)

1- 74LS373 (LATCH)

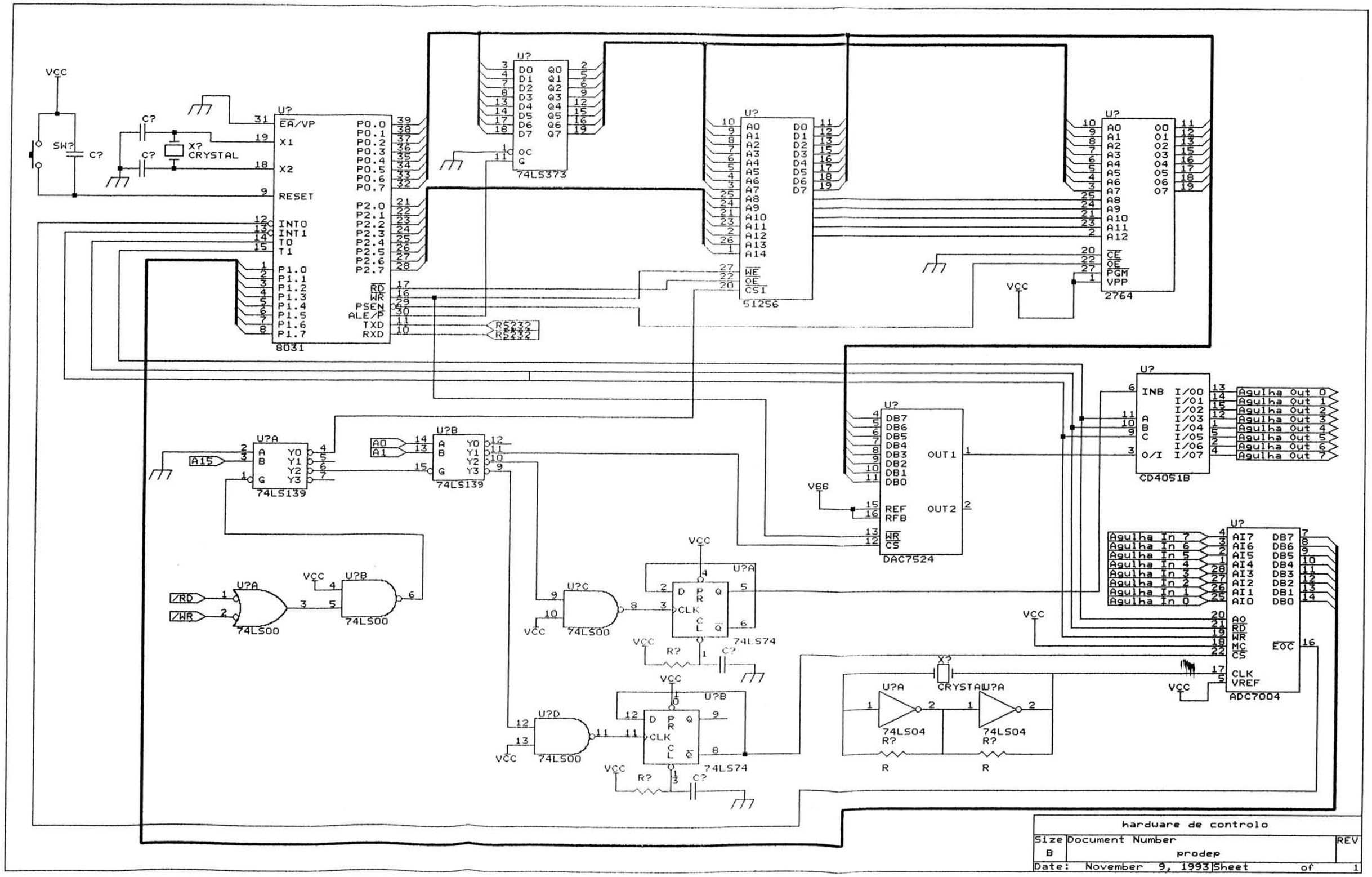
1- CRISTAL de

1- CRISTAL de

CONDENSADORES

RESISTÊNCIAS

ANEXOS


VCC
SW?
C?
C?
C?
X?
CRYSTAL
U?
8031
EA/VP
X1
X2
RESET
INT0
INT1
T0
T1
P1.0
P1.1
P1.2
P1.3
P1.4
P1.5
P1.6
P1.7
P0.0
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P0.2
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P2.3
P2.4
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P2.6
P2.7
RD
WR
PSEN
ALE/P
TXD
RXD
RS232
74LS373
D0
D1
D2
D3
D4
D5
D6
D7
Q0
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A13
A14
WE
OE
CS1
2764
CE
OE
PGM
VPP
U?A
74LS139
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/WR
74LS00
74LS74
D
CLK
R?
C?
U?C
U?D
DAC7524
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
OUT1
OUT2
REF
RFB
WR
CS
VEE
CD4051B
INB
A
B
C
O/I
I/00
I/01
I/02
I/03
I/04
I/05
I/06
I/07
Agulha Out 0
Agulha Out 1
Agulha Out 2
Agulha Out 3
Agulha Out 4
Agulha Out 5
Agulha Out 6
Agulha Out 7
ADC7004
AI7
AI6
AI5
AI4
AI3
AI2
AI1
AI0
AO
RD
WR
MC
CS
CLK
VREF
EOC
Agulha In 7
Agulha In 6
Agulha In 5
Agulha In 4
Agulha In 3
Agulha In 2
Agulha In 1
Agulha In 0
CRYSTAL
74LS04
R
hardware de controlo
Size
B
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Date: November 9, 1993
Sheet
of
1

```
        ;Rotina RECEPT
        ;Recebe 1 byte da porta serie
        ;Parametro de saida : A com valor do byte recebido

RECEPT: MOV     A,PCON
        CLR     ACC.7
        MOV     PCON,A
        MOV     A,ADCON
        SETB    ACC.7
        MOV     ADCON,A

        MOV     SCON,#50h
MESSMA: MOV     A,SCON
        ANL     A,#01H
        JZ      MESSMA
        CLR     RI

SERIEF: MOV     A,SBUF

        RET

;-------------------------------------------------------------------------------
        ;Rotina  TRANSM
        ;Transmite 1 byte da porta serie
        ;Parametro de entrada : A com valor do byte a transmitir

TRANSM: PUSH    ACC

        MOV     A,PCON
        CLR     ACC.7
        MOV     PCON,A
        MOV     A,ADCON
        SETB    ACC.7
        MOV     ADCON,A

        MOV     SCON,#40H
        POP     ACC
        PUSH    ACC
        MOV     SBUF,A

TRANS:  MOV     A,SCON
        ANL     A,#02H
        JZ      TRANS
        CLR     TI

        POP     ACC
        RET
```

CMOS 10-BIT SUCCESSIVE APPROXIMATION A/D CONVERTER

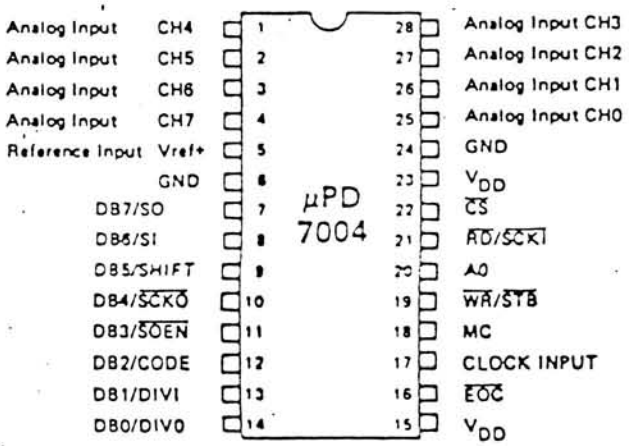
DESCRIPTION

The μPD7004 is a single-chip, 10-bit successive approximation A/D converter containing an 8-channel analog input multiplexer and a microcomputer interface circuit. The microcomputer interface circuit has two kinds of serial modes and an 8-bit parallel mode, which enables the 7004 to be easily connected to various kinds of microprocessors and microcomputers, such as the signal processor μPD7720 or devices of the μCOM75, μCOM84/85/87 and V-Series families.

FEATURES

- Single-chip CMOS A/D converter
- 8-channel analog input multiplexer
- Serial/parallel interface available
- Resolution 10 bits
- Linearity 1 LSB MAX. (@ T_a = 25°C)
- Analog input voltage range: 0 . . . V_{DD}
- Conversion time 104 μs (f_{CKI} = 1 MHz)
- 28-pin slim (400-mil width) DIP, plastic
- Single power supply (5 V ± 10 %)

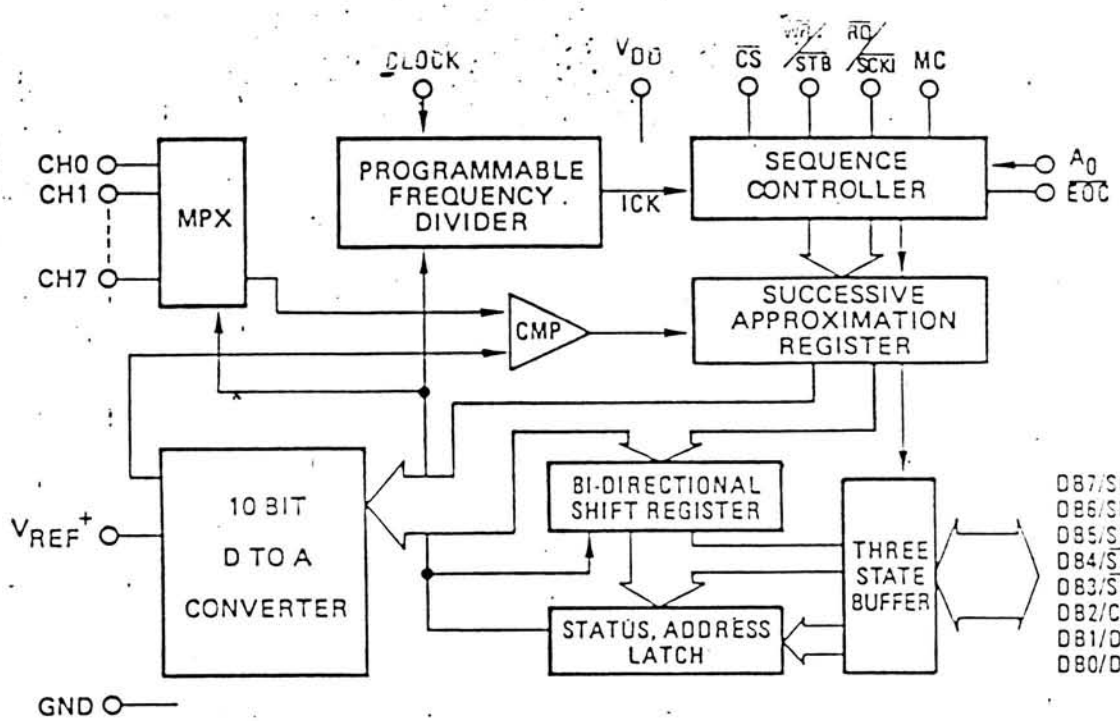
PIN CONFIGURATION (Top View)



PIN FUNCTIONS

PIN NO	SYMBOL	PARALLEL MODE FUNCTION	SERIAL MODE FUNCTION
1	CH4	Analog Input CH4	
2	CH5	Analog Input CH5	
3	CH6	Analog Input CH6	
4	CH7	Analog Input CH7	
5	Vref+	Positive Reference Voltage Input	
6	GND	Ground Digital	
7	DB7/SO	Data Bus (MSB)	Serial Output
8	DB6/SI	Data Bus (2nd)	Serial Input
9	DB5/SHIFT	Data Bus (3rd)	First Bit Select (LSB/MSB)
10	DB4/$\overline{SCKO}$	Data Bus (4th)	Serial Clock Output
11	DB3/$\overline{SOEN}$	Data Bus (5th)	Serial Output Enable
12	DB2/CODE	Data Bus (6th)	Code Select
13	DB1/DEV1	Data Bus (7th)	Freq. Divide Ratio Set
14	DB0/DEV0	Data Bus (LSB)	Freq. Divide Ratio Set
15	VDD	Power Supply Digital	
16	$\overline{EOC}$	End of Conversion (Active Low)	
17	CLOCK	Clock Input (f_{CLK})	
18	MC	MODE Select (H = Parallel, L = Serial)	
19	$\overline{WR}/\overline{STB}$	Write	Address Write Strobe
20	A0	Control Address	Internal/External Shift Clock
21	$\overline{RD}/\overline{SCKI}$	Read	Serial Clock Input
22	$\overline{CS}$	Chip Select	
23	VDD	Power Supply Analog	
24	GND	Ground Analog	
25	CH0	Analog Input CH0	
26	CH1	Analog Input CH1	

BLOCK DIAGRAM



INTERNAL BLOCK PERFORMANCE

SEQUENCE CONTROLLER

The sequence controller controls the performance of the comparator, the internal sequence of the serial conversion register, and the 3-state buffers. The A/D conversion starts in the parallel mode when the MPX address is written, and in the serial mode when the $\overline{CS}$ signal changes to the high level. After a complete conversion the sequence issues an end-of-conversion signal ($\overline{EOC}$) which can be used for external environment.

SERIAL COMPARISON REGISTER

The serial comparison register sends signals to the decoder of the internal 10-bit D/A according to the control signals from the sequence controller and then decides to set or reset the signals for the decoder, starting with the MSB, with the help of the results from the comparator.

TWO-WAY SHIFT REGISTER

This is the register into which the contents of the serial conversion register are shifted. It outputs the converted data via 3-state buffers when in the parallel mode.

In serial mode 1, it outputs the converted data from the SO pin when the $\overline{SCKI}$ signal falls and the $\overline{CS}$ signal is low, and fetches serial data (MPX address selector data) from the SI pin when the $\overline{SCKI}$ signal rises.

In serial mode 2, 10-bit converted data accompanied by 6-bit high data are output from the SO terminal synchronously during the fall time of the $\overline{SCKO}$ signal.

STATUS ADDRESS LATCH

The Status Address Latch is 3-bit register to latch the selection data for division ratio, conversion type and MPX address.

It reads the data entered from the data buses (DB_{0-7}) in the parallel mode. In serial mode, it latches the division ratio selector data and code selector data specified by the multi-function pins (DB_0/DEV_0, DB_1/DEV_1, DB_2/CODE) and also the MPX address data entered through the SI terminal.

Note, however, that the MPX address is fixed at CH_7 and cannot be selcted in serial mode 2.

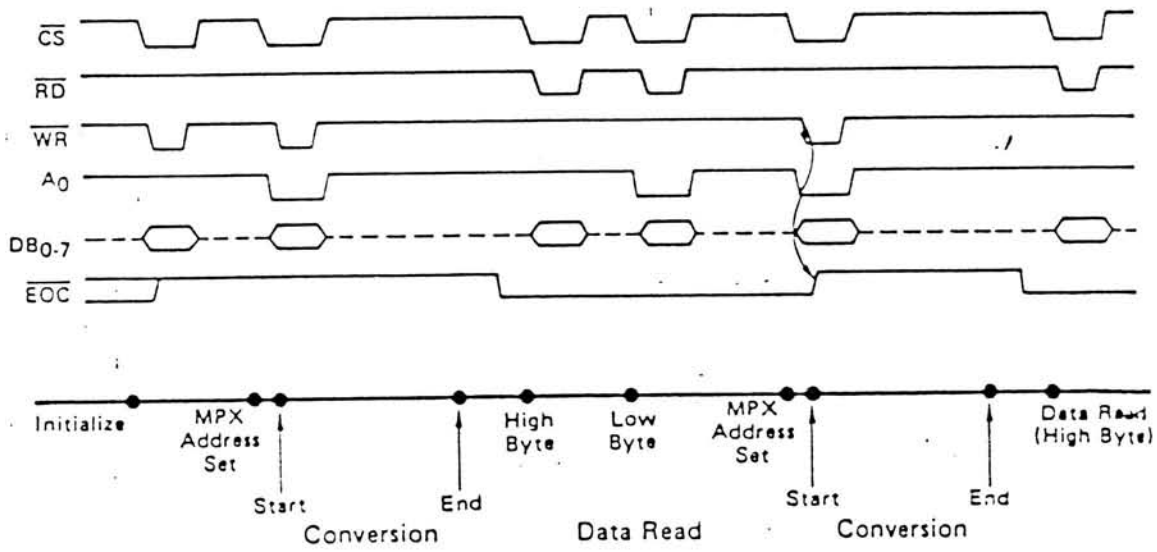
PROGRAMMABLE DIVIDER

An external clock can be divided by one of the ratios 1/1, 1/2, 1/4, 1/8 for internal use.

OPERATING MODES

PARALLEL MODE

The parallel mode allows a direct connection to the microprocessor data buses. An example of the basic operation sequence is shown below.



During initialization the data for clock division ratio and the selection of A/D conversion data code (Binary/2's complement) is stored until next initialization. Writing the MPX Address Set into the μPD7004 (A_0 must be low) the first conversion starts with the rising edge of the write signal.

The A/D conversion requires 96 to 104 cycles of the internal clock ($f_{ICK} = f_{CLK}$ x division ratio. The $\overline{EOC}$ signal changes to the low level when the A/D conversion is complete to notify this to the external environment. The 10-bit converted data is read out from the μPD7004 eight bits at a time. The low byte has valid data in its two high-order bits, followed by six "0"s in the rest (DB_5–DB_0).

Resetting the MPX address starts the next A/D conversion, changing the $\overline{EOC}$ signal to the high level when the $\overline{WR}$ signal rises.

DATA BUS PERFORMANCE

CONTROL PIN $\overline{CS}$	$\overline{WR}$	$\overline{RD}$	A_0	PERFORMANCE	DATA BUS INFORMATION
H	x	x	x	No effect	High-impedance State
L	H	H	x		
L	L	H	H	Initialize	Code Select, Clock division Ratio Input
L	L	H	L	Address Set	Analogue Channel Select Data Input
L	H	L	H	High-byte Read	High-byte Data Output
L	H	L	L	Low-byte Read	Low-byte Data Output
L	L	L	x	Not Allowed	—

NITIALIZE

In the parallel mode, the initialization data for the clock division ratio and the A/D conversion data codes are written into the μPD7004 through the data bus.

DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
x	x	x	x	x	CODE	DEV_1	DEV_0

High-impedence state

DEV_1	DEV_0	CLOCK DIVISION RATIO
L	L	1/1
L	H	1/2
H	L	1/4
H	H	1/8

CODE	CODE SELECT
L	Binary Data
H	2's Complement Data

Data written at the initialization is held afterwards.

ADDRESS SET

The analog input channel is written into the μPD7004 by the bits DB_0 . . . DB_2.

DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
x	x	x	x	x	SEL_2	SEL_1	SEL_0

High-impedence state

SEL_2	SEL_1	SEL_0	MPX CHANNEL
L	L	L	CH_0
L	L	H	CH_1
L	H	L	CH_2
L	H	H	CH_3
H	L	L	CH_4
H	L	H	CH_5
H	H	L	CH_6
H	H	H	CH_7

READ DATA

The converted data is read from the μPD7004 in two bytes.

	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
High-byte	MSB	2ND	3RD	4TH	5TH	6TH	7TH	8TH
Low-byte	9TH	LSB	L	L	L	L	L	L

UNCTIONS

SYMBOL	PIN NO.	SERIAL MODE 1 (EXTERNAL SERIAL CLOCK, A_0 = L) I/O	SERIAL MODE 1 PERFORMANCE	SERIAL MODE 2 (SIGNAL PROCESSOR MODE, A_0 = H) I/O	SERIAL MODE 2 PERFORMANCE
SO	7	Output	Serial Output (3-state) To be output synchronously during the fall time of the $\overline{SCKI}$ or $\overline{SCKO}$ signal.		
SI	8	Input	Serial Input To be read synchronously during the rise time of the $\overline{SCKI}$ signal.	Input	To be connected to V_{DD}
SHIFT	9	Input	Shift Select (H: LSB frist, L: MSB first)		
$\overline{SCKO}$	10	—	To be connected to ground potential	Output	Serial Clock Output (= Internal Clock)
$\overline{SOEN}$	11	—	To be connedted to ground potential	Output	Serial-Out Enable (= Active Low)
CODE	12	Input	Code Select (H = 2's complement, L = Binary)		
DEV_1	13	Input	Division Ratio Set		
DEV_0	14	Input			
$\overline{STB}$	19	Input	Address Strobe Signal Reads address data to the address latch during the rise time.	Input	To be connected to ground potential
$\overline{SCKI}$	21	Input	Control signal for the Interface Shift Register To be output during the fall time and input during the rise time.	—	To be connected to V_{DD}
$\overline{CS}$	22	Input	Chip Select Signal Resets the internal sequence. Serves as an interface at the low-level, thereby allowing data input/output.	Input	Internal Sequence Reset Signal Resets the sequence controller at the low-level, starts the A/D conversion at the rise time.

DEV_1	L	L	H	H
DEV_0	L	H	L	H
Division Ratio	1/1	1/2	1/4	1/8

Notes: 1. In serial mode 1, the following signals are strobed by the $\overline{CS}$ signal. Therefore, the output signals are ignored and the output pins become high impedance when $\overline{CS}$ = HIGH.

Input pin: SI, $\overline{STB}$, $\overline{SCKI}$
Output pin: SO

2. In serial mode 2, the internal sequence reset signal $\overline{CS}$ specifies CH_7.

RIAL MODE 1

Serial Mode 1 supports serial data I/O when $\overline{CS}$ signal is at the low level. The device outputs the serial data during the fall time of the serial clock signal ($\overline{SCKI}$), that comes from the external environment. It fetches the serial input data during the rise time of the $\overline{SCKI}$ signal.

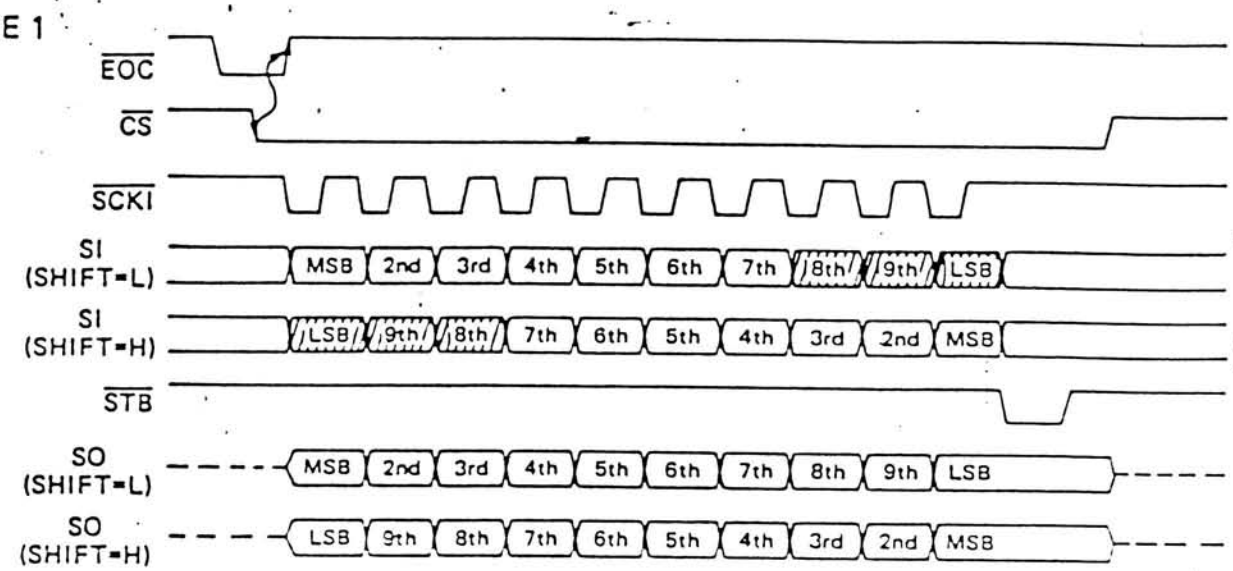
If the MSB-first data is specified (SHIFT = L), the last three bits of the 10-bit serial input data for the MPX address selection contain valid data. If the LSB-first data is specified (SHIFT = H), the first three bits of the 10-bit data contain valid data.

This MPX address data latch in the μPD7004 is selected the trailing edge of the $\overline{STB}$ signal starts. The latch can also be achieved when the $\overline{CS}$ signal starts to rise and the $\overline{STB}$ signal is **fixed at the low level.**

The A/D conversion starts with the trailing edge of the $\overline{CS}$ signal. The $\overline{EOC}$ signal changes to the low-level at the end of the conversion to notify this to the external environment. The time required for the A/D conversion is the same as that required in the parallel mode. The $\overline{EOC}$ signal changes to the high level when the $\overline{CS}$ signal starts to fall.

The A/D conversion is repeated if the $\overline{CS}$ signal stays in the high-level and the $\overline{EOC}$ signal remains in the low-level.

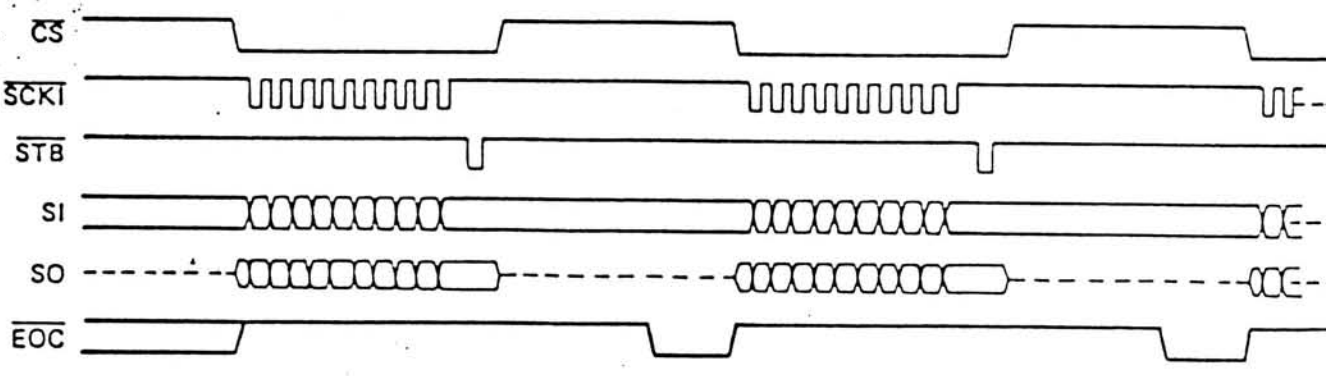
SERIAL MODE 1 TIMING

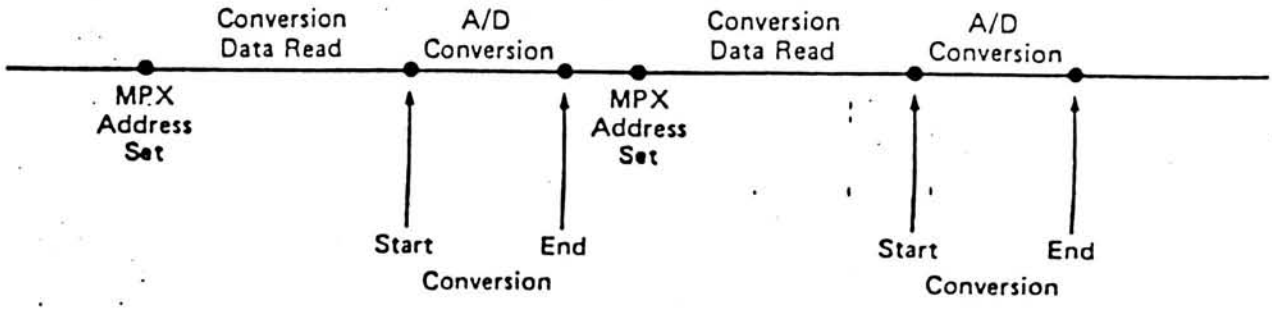


The 3 low-order bits of the serial input data serve as channel selection data.

8th	L	L	L	L	H	H	H	H
9th	L	L	H	H	L	L	H	H
LSB	L	H	L	H	L	H	L	H
Channel	CH_0	CH_1	CH_2	CH_3	CH_4	CH_5	CH_6	CH_7

SERIAL MODE 1 SEQUENCE TIMING



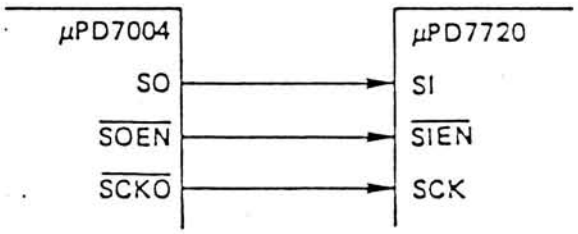


SERIAL MODE 2

Serial mode 2 allows direct connection to the serial interface of the signal processor μPD7720.

Shown on the right is an example of connecting principal terminals between the μPD7004 and μPD7720.

The difference to the other serial mode is the fixed, input channel CH_7.



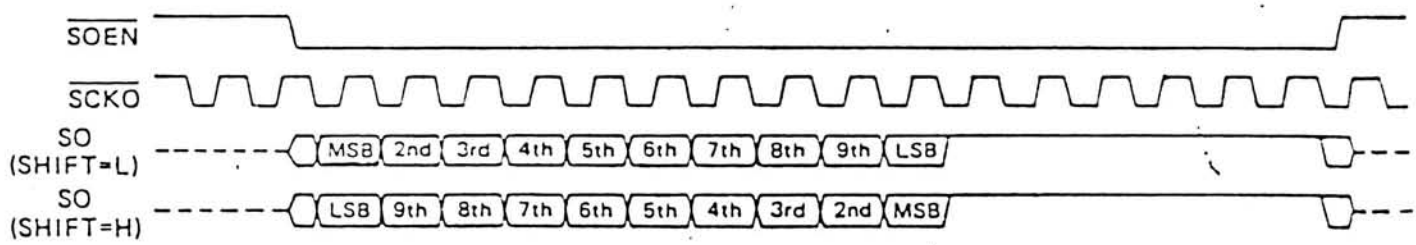
Although the data through the A/D conversion consists of 10 bits, it is followed by six bits of high data when it is output as serial data. These six bits of high data always follow the converted data for MSB-first or LSB-first (see timing diagram).

The A/D conversion sequence starts upon the initialization. The initialization is performed by holding the $\overline{CS}$ signal at the low-level for more than eight clock cycles. The A/D conversion starts when the $\overline{CS}$ signal changes to the high-level. The A/D conversion requires 104 clock pulses (f_{ICK}).

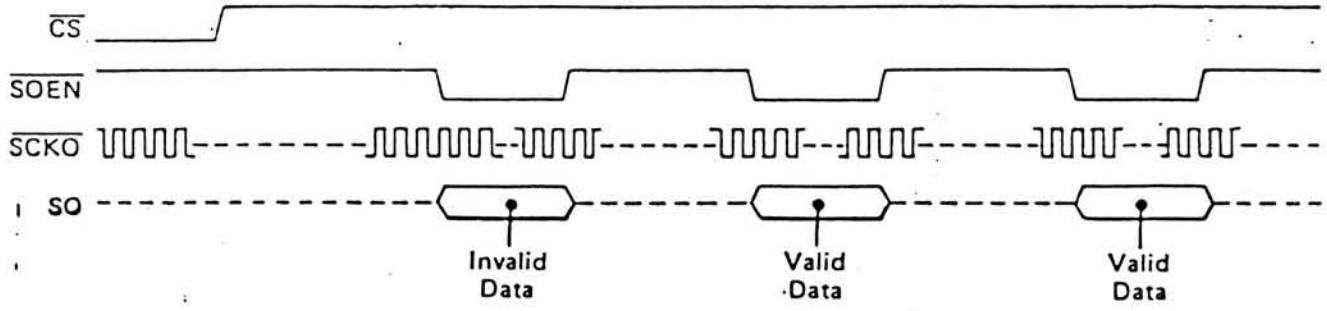
The $\overline{EOC}$ signal, as in the other modes, changes to the low-level to notifiy the end of the conversion to the external environment. The $\overline{EOC}$ signal remains at the low-level until the initialization is implemented.

Note, however, that the converted data are output immediately after the initialization is invalid. Valid data is available from the second output. This is because the MPX address is fixed at CH_7 for the converted data output which is performed right after the initialization. The A/D conversion and the converted data output are repeatedly performed while the $\overline{CS}$ signal is in the high-level (see sequence timing diagram).

ERIAL MODE 2
IMING



ERIAL MODE 2
EQUENCE TIMING



OLUTE MAXIMUM TINGS

(T_a = 25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	−0.3 to +7.0	V
Input Voltage	V_I	−0.3 to V_{DD} +0.3	V
Reference Voltage	V_{REF}	−0.3 to V_{DD} +0.3	V
Operating Temperature	T_{opt}	−40 to +85	°C
Storage Temperature	T_{stg}	−65 to +125	°C

COMMENDED ERATINGS NDITIONS

(T_a = −20 . . . 80°C)

PARAMETER	SYMBOL	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Reference Voltage	V_{REF}		4.0		V_{DD}	V
Analog Input Voltage	V_I		0.0		V_{REF}	V
High Level Input Voltage	V_{IH}		2.4			V
Low Level Input Voltage	V_{IL}				0.8	V
Clock Frequency	f_{CLK}		0.4		8.8	MHz
Internal Clock Frequency	f_{ICK}	$f_{ICK} = f_{CK}$ x Devide Ratio	0.4	1.0	1.1	MHz
PARALLEL MODE (MC = HIGH)						
Address Setup Time	t_{AW}	$\overline{CS}$ ↓, A0 → $\overline{WR}$ ↓	50			ns
	t_{AR}	$\overline{CS}$ ↓, A0 → $\overline{RD}$ ↓	50			ns
Address Hold Time	t_{WA}	$\overline{WR}$ ↑ → $\overline{CS}$ ↑, A0	50			ns
	t_{RA}	$\overline{RD}$ ↑ → $\overline{CS}$ ↑, A0	50			ns
$\overline{WR}$ Pulse Width	t_{WW}		400			ns
$\overline{RD}$ Pulse Width	t_{RR}		400			ns
Data Setup Time	t_{DW}	DB → $\overline{WR}$ ↑	300			ns
Data Hold Time	t_{WD}	$\overline{WR}$ ↑ → DB	100			ns
SERIAL MODE 1 (MC = LOW, A0 = LOW; External Serial Clock)						
EOC Hold Time	t_{HECS}	$\overline{EOC}$ ↓ → $\overline{CS}$ ↓	0			µs
CS Setup Time	t_{SCSK}	$\overline{CS}$ ↓ → $\overline{SCKI}$ ↓ (Note 1)	1			µs
Serial Input Setup Time	t_{SIK}	SI → $\overline{SCKI}$ ↑	150			ns
Serial Input Hold Time	t_{HKI}	$\overline{SCKI}$ ↑ → SI	100			ns
Low Level Serial Clock Pulse Width	t_{WLK}		400			ns
High Level Serial Clock Pulse Width	t_{WHK}		400			ns
Strobe Pulse Width	t_{WLST}		200			ns
Strobe Hold Time	t_{HKST}	$\overline{SCK}$ ↑ → $\overline{STB}$ ↑	200			ns
Chip Select Hold Time	t_{HKCS}	$\overline{SCK}$ ↑ → $\overline{CS}$ ↑	100			ns

Note: 1 f_{CLK} = 1 MHz

ONVERSION HARACTERISTICS

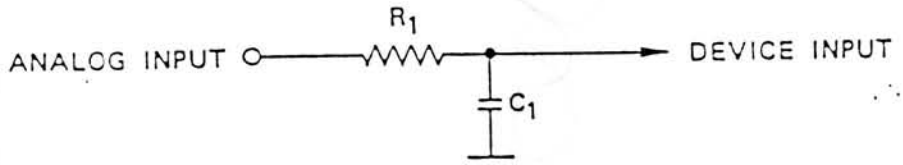
(T_a = 25°C, V_{DD} = V_{REF} = 4.5 . . . 5.5V, f_{ICK} = 1 MHz)

PARAMETER	SYMBOL	CONDITION	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Resolution		T_a = −40 . . . +85°C	10	10	10	Bit
Linearity		T_a = −20 . . . +80°C			± 1.0	LSB
Linearity		T_a = −40 . . . +85°C			± 2.0	LSB
Zeroscale Error					± 0.5	LSB
Zeroscale Temperature Coefficient		T_a = −40 . . . +85°C		2		ppm/°C
Fullscale Error					± 0.5	LSB
Fullscale Temperature Coefficient		T_a = −40 . . . +85°C		2		ppm/°C
Conversion Time		. . . Serial Mode 1	96		104	µs

CHARACTERISTICS ($V_{DD} = V_{REF} = 5 \pm 0.5V$, $T_a = -40 \ldots +85°C$, $f_{ICK} = 1$ MHz)

PARAMETER	SYMBOL	CONDITION	LIMITS			UNIT
			MIN	TYP	MAX	
High Level Output Voltage	V_{OH}	$I_O = -1.6$ mA	3.5			V
Low Level Output Voltage	V_{OL}	$I_O = 1.6$ mA			0.4	V
Digital Input Leakage Current	I_{ID}	$V_I = 0 \ldots V_{DD}$			± 10	μA
Floating Output Leakage Current	I_{FO}	$V_O = 0 \ldots V_{DD}$			± 10	μA
Analog Input Resistance (DC)	RI (DC)	$V_I = 0 \ldots V_{DD}$	2			MΩ
Reference Input Resistance	R_{REF}		5		50	KΩ
Power Dissipation	P_d			5	15	mW

Note: Recommended Analog Input filter



R_1 = 10kΩ

C_1 = 100pF

ATTENTION: When the multiplexer's power is turned on, a charging/discharging voltage is generated. Therefore, connect a capacitor greater than 0.01 μF to the analog input terminal in case the driving side has a high impedance.

C CHARACTERISTICS

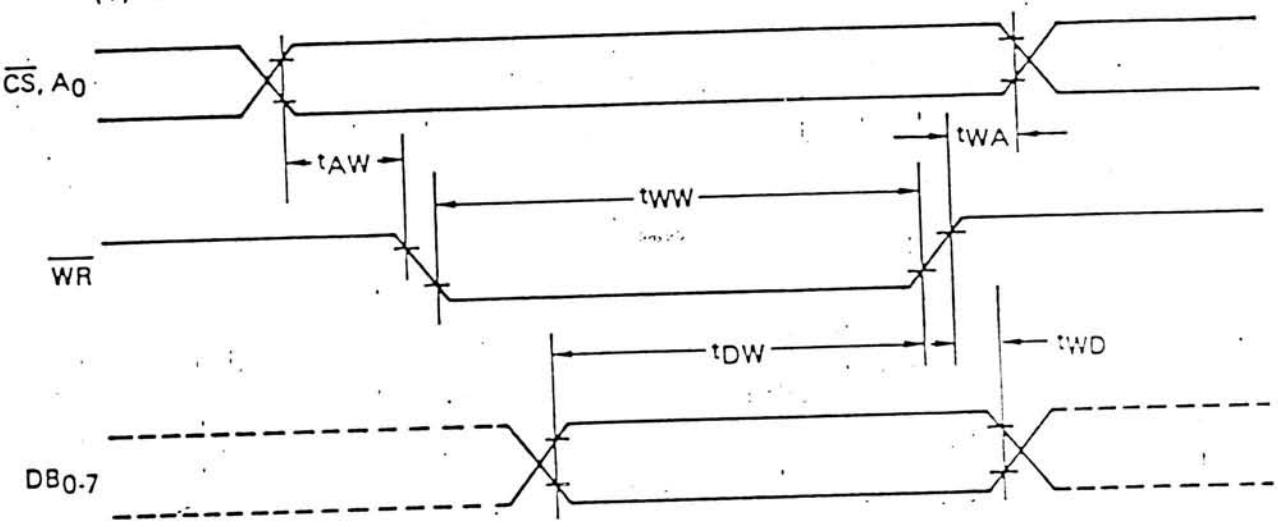
($V_{DD} = V_{REF} = 5 \pm 0.5V$, $T_a = -40 \ldots +85°C$, $f_{ICK} = 1$ MHz)

PARAMETER	SYMBOL	CONDITION	LIMITS			UNIT
			MIN	TYP	MAX	
Output Delay Time	t_{RD}	RD ↓ → DB (Parallel mode)			250	ns
	t_{DKO}	SCKI ↓, SCKO ↓ → SO (Serial mode)			250	ns
Output Floating Delay Time	t_{DR}	RD ↑ → DB Floating (Parallel mode)			150	ns
	t_{FCSO}	CS ↑ → SO Floating (Serial mode 1)			150	ns
Serial Clock Output Delay Time	t_{SKS}	SCKO ↑ → SOEN ↓ (Serial mode 2)	40		200	ns
Serial Output Enable Delay Time	t_{HKS}	SCKO ↓ → SOEN ↑ (Serial mode 2)	0		200	ns
Serial Clock Output Cycle	t_{CYK}	(Serial mode 2)		$1/f_{ICK}$		ns
High Level Serial Clock Pulse Width	t_{WHK}	(Serial mode 2)	400			ns
Low Level Serial Clock Pulse Width	t_{WLK}	(Serial mode 2)	400			ns
Serial Clock Rise Time	t_{rsc}	(Serial mode 2)		20		ns
Serial Clock Fall Time	t_{fsc}	(Serial mode 2)		20		ns

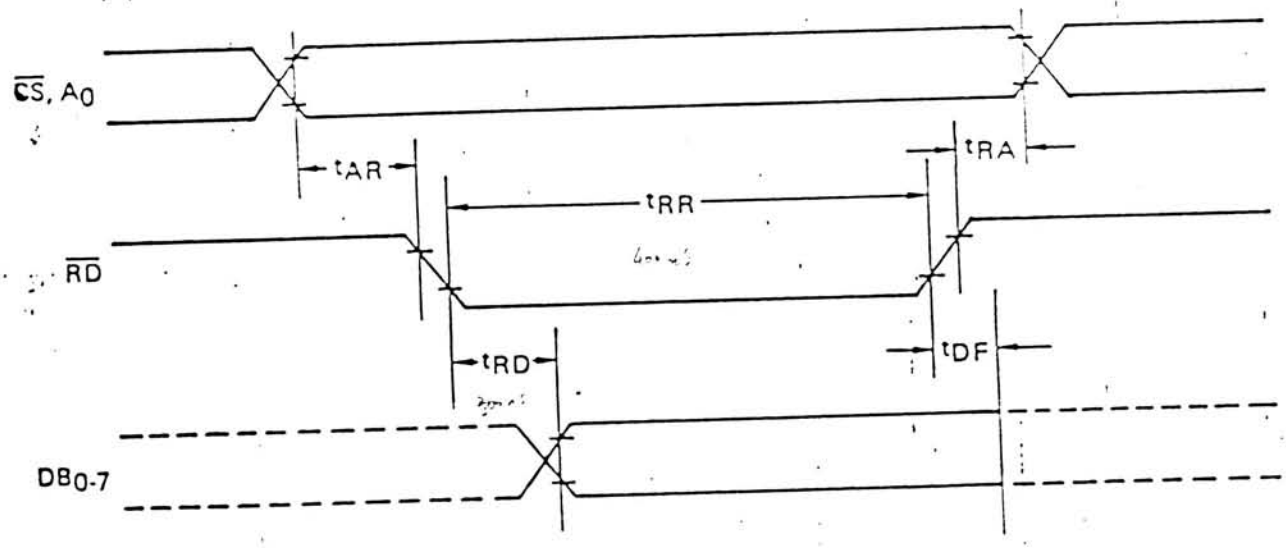
MING DIAGRAMS

PARALLEL MODE

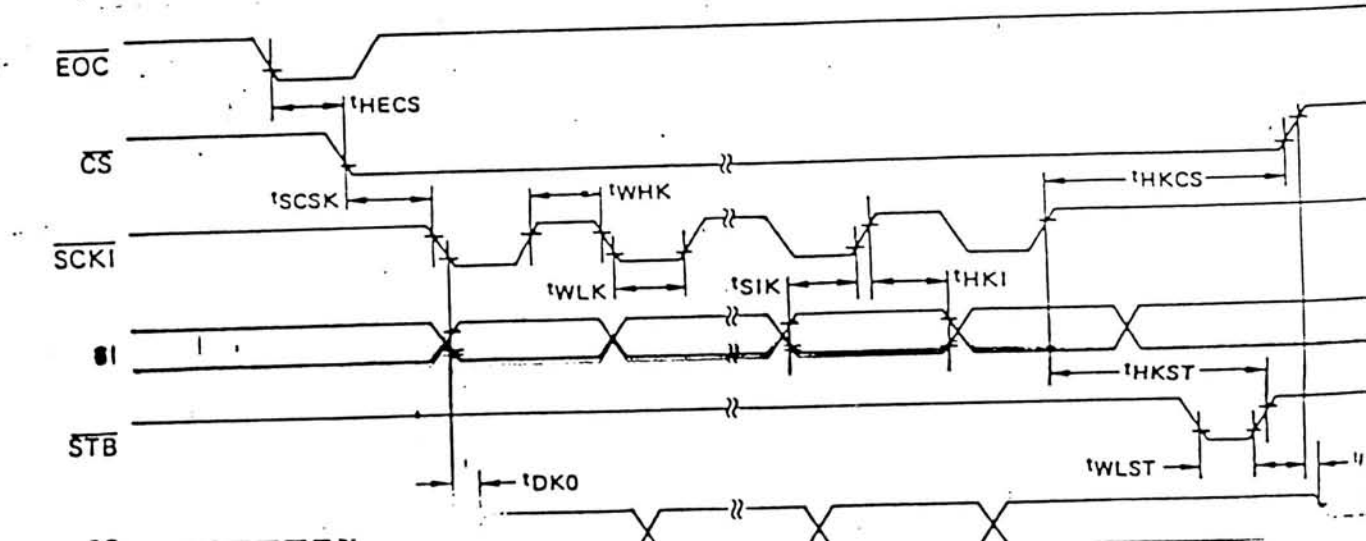
(1) WRITE MODE



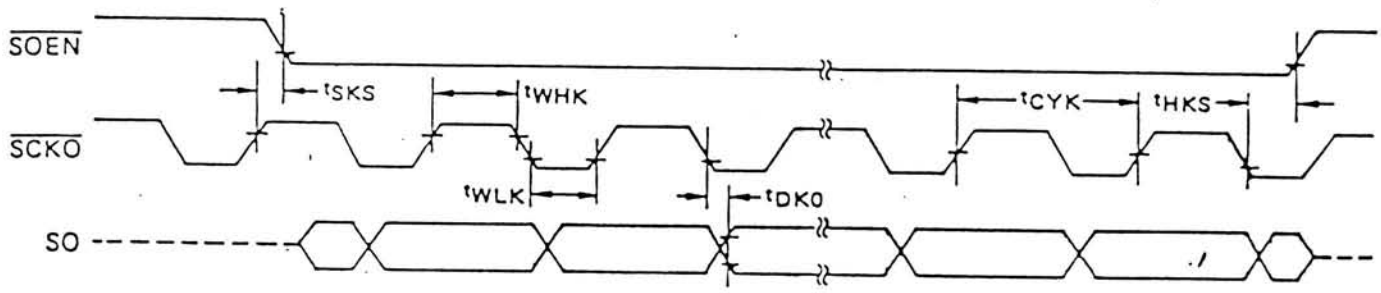
(2) READ MODE



2. SERIAL MODE 1



SERIAL MODE 2



KAGE OUTLINE
7004C
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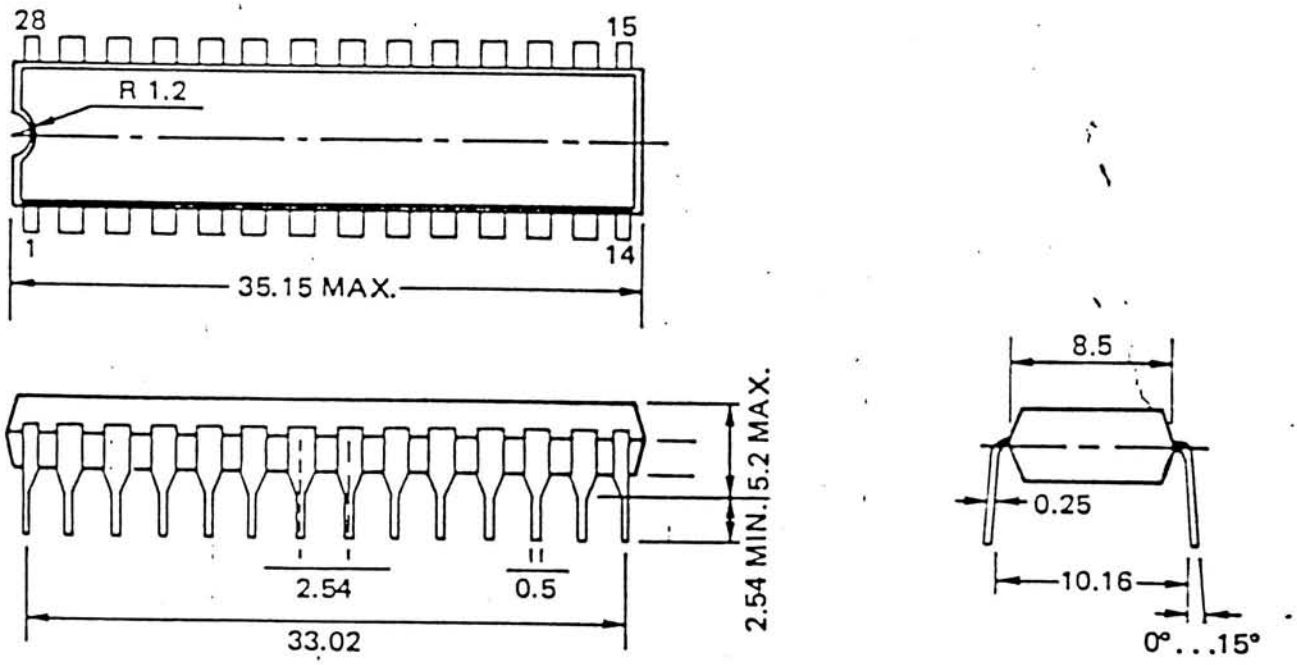


CMOS Analog Multiplexers/Demultiplexers*

With Logic-Level Conversion

High-Voltages Types (20-Volt Rating)

CD4051B — Single 8-Channel
CD4052B — Differential 4-Channel
CD4053B — Triple 2-Channel

RCA-CD4051B, CD4052B, and CD4053B analog multiplexers/demultiplexers are digitally controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20 V peak-to-peak can be achieved by digital signal amplitudes of 4.5 to 20 V (if V_{DD}-V_{SS} = 3 V, a V_{DD}-V_{EE} of up to 13 V can be controlled; for V_{DD}-V_{EE} level differences above 13 V, a V_{DD}-V_{SS} of at least 4.5 V is required). For example, if V_{DD} = +4.5V, V_{SS} = 0, and V_{EE} = −13.5 V, analog signals from −13.5 V to +4.5 V can be controlled by digital inputs of 0 to 5 V. These multiplexer circuits dissipate extremely low quiescent power over the full V_{DD}-V_{SS} and V_{DD}-V_{EE} supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the inhibit input terminal all channels are off.

The CD4051B is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4052B is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053B is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

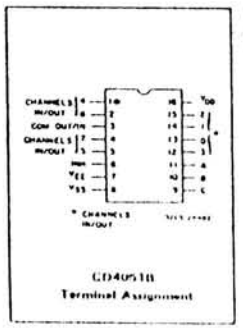
The CD4051B, CD4052B, and CD4053B are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead plastic dual-in-line packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

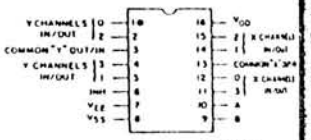
Applications:

- Analog and digital multiplexing and demultiplexing
- A/D and D/A conversion
- Signal gating

Features:

- Wide range of digital and analog signal levels: digital 3 to 20 V, analog to 20 V_{p-p}
- Low ON resistance: 125 Ω (typ.) over 15 V_{p-p} signal-input range for V_{DD}-V_{EE} = 15 V
- High OFF resistance: channel leakage of ±100 pA (typ.) @ V_{DD}-V_{EE} = 18 V
- Logic-level conversion for digital addressing signals of 3 to 20 V (V_{DD}-V_{SS} = 3 to 20 V) to switch analog signals to 20 V p-p (V_{DD}-V_{EE} = 20 V); see introductory text
- Matched switch characteristics: R_{ON} = 5 Ω (typ.) for V_{DD}-V_{EE} = 15 V
- Very low quiescent power dissipation under under all digital-control input and supply conditions: 0.2 μW (typ.) @ V_{DD}-V_{SS} = V_{DD}-V_{EE} = 10 V
- Binary address decoding on chip
- 5-, 10-, and 15-V parametric ratings
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Break-before-make switching eliminates channel overlap



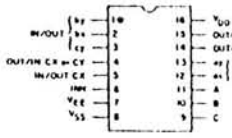


RECOMMENDED OPERATING CONDITIONS AT T_A = 25°C (Unless Otherwise Specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges. Values shown apply to all types except as noted

CHARACTERISTIC	V_{DD}	Min.	Max.	Units
Supply-Voltage Range (T_A = Full Package-Temp. Range)	–	3	18	V
Multiplexer Switch Input Current Capability*	–	–	25	mA
Output Load Resistance	–	100	–	Ω

* In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown in ELECTRICAL CHARACTERISTICS CHART). No V_{DD} current will flow through R_L if the switch current flows into terminal 3 on the CD4051, terminals 3 and 13 on the CD4052, terminals 4,14, and on the CD4053.



* When these devices are used as demultiplexers, the "CHANNEL IN/OUT" terminals are the outputs and the "COMMON OUT/IN" terminals are the inputs.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} or V_{EE}, whichever is more negative)	-0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max	+265°C

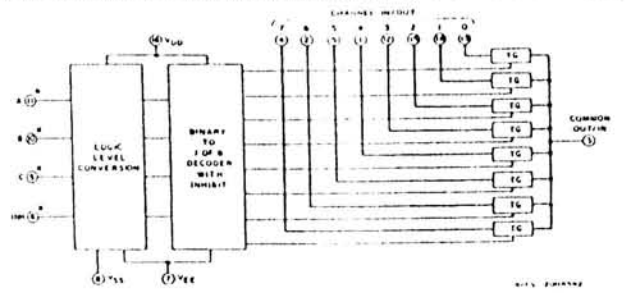


Fig. 1 – Functional diagram of CD4051B.

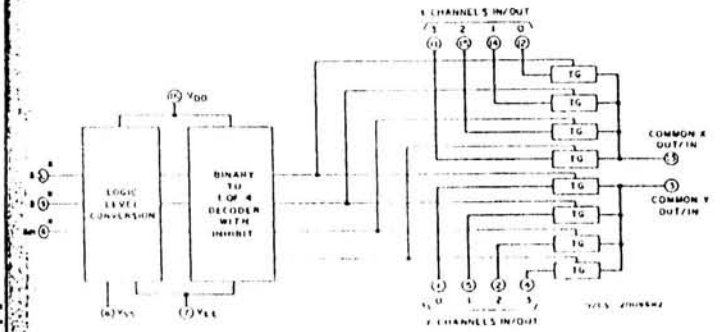


Fig. 2 – Functional diagram of CD4052B.

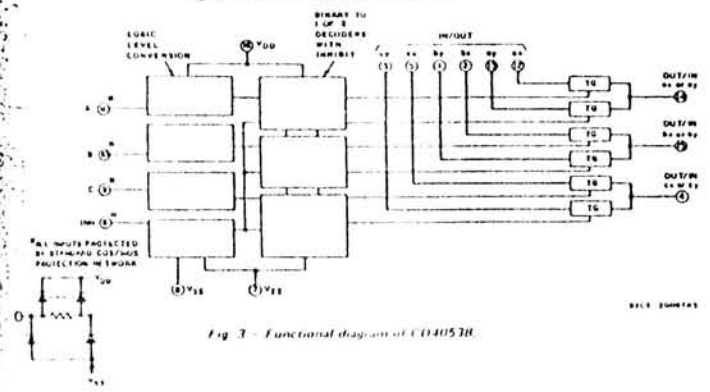


Fig. 3 – Functional diagram of CD4053B.

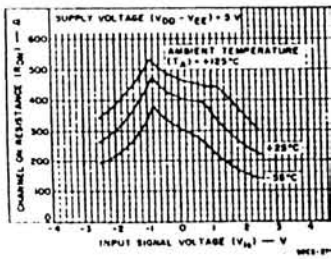


Fig. 4 – Typical channel ON resistance vs input signal voltage (all types).

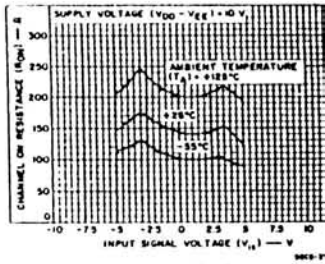


Fig. 5 – Typical channel ON resistance vs. input signal voltage (all types).

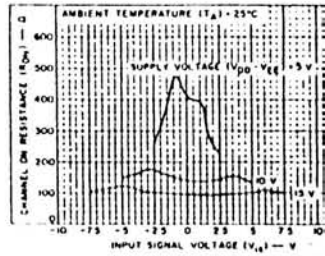


Fig. 6 – Typical channel ON resistance vs. input signal voltage (all types).

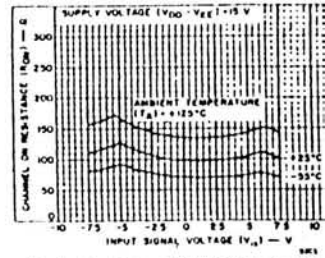


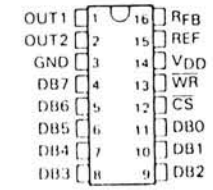
Fig. 7 – Typical channel ON resistance vs. input signal voltage (all types).

AD7524
Advanced LinCMOS™ 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

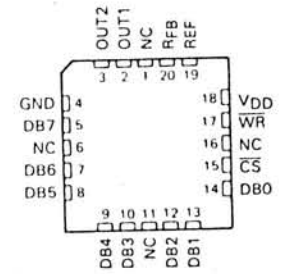
D3100, APRIL 1988

- Advanced LinCMOS™ Silicon-Gate Technology
- Easily Interfaced to Microprocessors
- On Chip Data Latches
- Monotonicity Over Entire A/D Conversion Range
- Segmented High Order Bits Ensure Low Glitch Output
- Designed to be Interchangeable with Analog Devices AD7524, PMI PM-7524, and Micro Power Systems MP7524
- Fast Control Signaling for Digital Signal Processor Applications Including Interface with TMS320

N PACKAGE
(TOP VIEW)



AD7524J . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 Bits
Linearity error	½ LSB Max
Power dissipation at V_{DD} = 5 V	5 mW Max
Settling time	100 ns Max
Propagation delay	80 ns Max

description

The AD7524 is an Advanced LinCMOS™ 8-bit digital-to-analog converter (DAC) designed for easy interface to most popular microprocessors.

The AD7524 is an 8 bit multiplying DAC with input latches and with a load cycle similar to the "write" cycle of a random access memory. Segmenting the high-order bits minimizes glitches during changes in the most-significant bits, which produce the highest glitch impulse. The AD7524 provides accuracy to ½ LSB without the need for thin-film resistors or laser trimming, while dissipating less than 5 mW typically.

Featuring operation from a 5-V to 15-V single supply, the AD7524 interfaces easily to most microprocessor buses or output ports. Excellent multiplying (2 or 4 quadrant) makes the AD7524 an ideal choice for many microprocessor-controlled gain-setting and signal-control applications.

The AD7524A is characterized for operation from −25°C to 85°C, and the AD7524J is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE
DEVICE	PACKAGE SUFFIXES	
AD7524A	N	−25°C to 85°C
AD7524J	N, FN	0°C to 70°C

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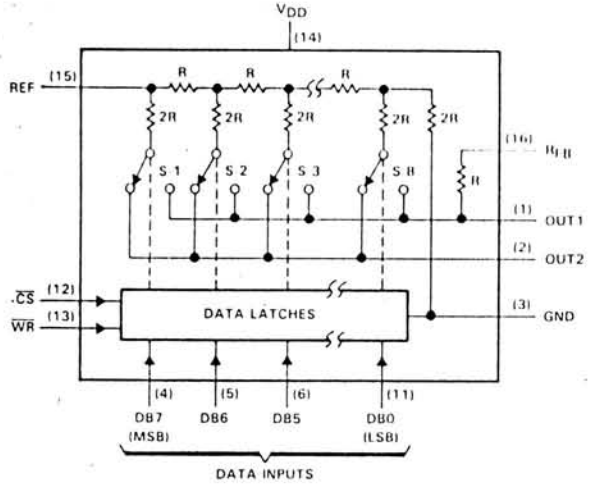
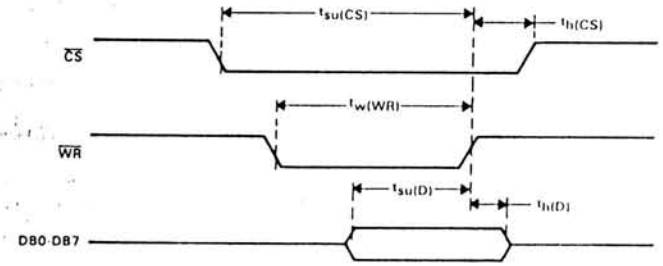
functional block diagram



operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} . . . . . 0.3 V to 17 V
Voltage between R_{FB} and GND . . . . . ±25 V
Digital input voltage, V_I . . . . . −0.3 V to V_{DD} + 0.3 V
Reference voltage, V_{ref} . . . . . ±25 V
Peak digital input current, I_I . . . . . 10 μA
Operating free-air temperature range: AD7524A . . . . . −25°C to 85°C
AD7524J . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

recommended operating conditions

		V_{DD} = 5 V			V_{DD} = 15 V			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4.75	5	5.25	14.5	15	15.5	V
Reference voltage, V_{ref}			±10			±10		V
High level input voltage, V_{IH}		2.4			13.5			V
Low level input voltage, V_{IL}				0.8			1.5	V
CS setup time, $t_{su(CS)}$		40			40			ns
CS hold time, $t_{h(CS)}$		0			0			ns
Data bus input setup time, $t_{su(D)}$		25			25			ns
Data bus input hold time, $t_{h(D)}$		10			10			ns
Pulse duration, WR low, $t_{w(WR)}$		40			40			ns
Operating free-air temperature, T_A	AD7524A	−25		85	−25		85	°C
	AD7524J	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range, V_{ref} = 10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER			TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{IH}	High level input current		$V_I = V_{DD}$	Full range			10			10	μA
				25°C			1			1	
I_{IL}	Low level input current		$V_I = 0$	Full range			−10			−10	μA
				25°C			−1			−1	
I_{lkg}	Output leakage current	OUT1	DB0-DB7 at 0, WR and CS at 0 V, V_{ref} = ±10 V	Full range			±400			±200	nA
				25°C			±50			±50	
		OUT2	DB0-DB7 at V_{DD}, WR and CS at 0 V, V_{ref} = ±10 V	Full range			±400			±200	
				25°C			±50			±50	
I_{DD}	Supply current	Quiescent	DB0-DB7 at V_{IH} min or V_{IL} max	Full range			2			2	mA
				25°C			1			2	
		Standby	DB0-DB7 at 0 V or V_{DD}	Full range			500			500	μA
				25°C			100			100	
k_{SVS}	Supply voltage sensitivity, $\Delta g_{fs}/\Delta V_{DD}$		ΔV_{DD} = 10%	Full range		0.01	0.16		0.005	0.04	%/%
				25°C		0.002	0.08		0.001	0.02	
C_I	Input capacitance, DB0-DB7, WR, CS		$V_I = 0$				5			5	pF
C_o	Output capacitance	OUT1	DB0-DB7 at 0, WR and CS at 0 V				30			30	pF
		OUT2					120			120	
		OUT1	DB0-DB7 at V_{DD}, WR and CS at 0 V				120			120	
		OUT2					30			30	
	Reference input impedance (REF to GND)				5		20	5		20	kΩ

operating characteristics over recommended operating free-air temperature range, V_{ref} = 10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC} = 5 V		V_{DD} = 15 V		UNIT
			MIN	MAX	MIN	MAX	
Linearity error				±0.2		±0.2	%FSR
Gain error	See Note 1	Full range		±1.4		±0.6	%FSR
		25°C		±1		±0.5	
Settling time (to 1/2 LSB)	See Note 2			100		100	ns
Propagation delay from digital input to 90% of final analog output current	See Note 2			80		80	ns
Feedthrough at OUT1 or OUT2	V_{ref} = ±10 V (100 kHz sinewave), $\overline{WR}$ and $\overline{CS}$ at 0, DB0-DB7 at 0	Full range		0.5		0.5	%FSR
		25°C		0.25		0.25	
Temperature coefficient of gain	T_A = 25°C to t_{min} or t_{max}			±0.004		±0.001	%FSR/°C

NOTES: 1. Gain error is measured using the internal feedback resistor. Nominal Full Scale Range (FSR) = V_{ref} − 1 LSB.
2. OUT1 load = 100 Ω, C_{ext} = 13 pF, $\overline{WR}$ at 0 V, $\overline{CS}$ at 0 V, DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.

PRINCIPLES OF OPERATION

The AD7524 is an 8-bit multiplying D/A converter consisting of an inverted R-2R ladder, analog switches, and data input latches. Binary weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state. The high-order bits are decoded and these decoded bits, through a modification in the R-2R ladder, control three equally weighted current sources. Most applications only require the addition of an external operational amplifier and a voltage reference.

The equivalent circuit for all digital inputs low is seen in Figure 1. With all digital inputs low, the entire reference current, I_{ref}, is switched to OUT2. The current source I/256 represents the constant current flowing through the termination resistor of the R-2R ladder, while the current source I_{lkg} represents leakage currents to the substrate. The capacitances appearing at OUT1 and OUT2 are dependent upon the digital input code. With all digital inputs high, the off-state switch capacitance (30 pF maximum) appears at OUT2 and the on-state switch capacitance (120 pF maximum) appears at OUT1. With all digital inputs low, the situation is reversed as shown in Figure 1. Analysis of the circuit for all digital inputs high is similar to Figure 1; however, in this case, I_{ref} would be switched to OUT1.

Interfacing the AD7524 D/A converter to a microprocessor is accomplished via the data bus and the $\overline{CS}$ and $\overline{WR}$ control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the AD7524 analog output responds to the data activity on the DB0-DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0-DB7 inputs are latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When CS is high, the data inputs are disabled regardless of the state of the $\overline{WR}$ signal.

The AD7524 is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant or 4-quadrant multiplication are shown in Figures 2 and 3. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.

PRINCIPLES OF OPERATION

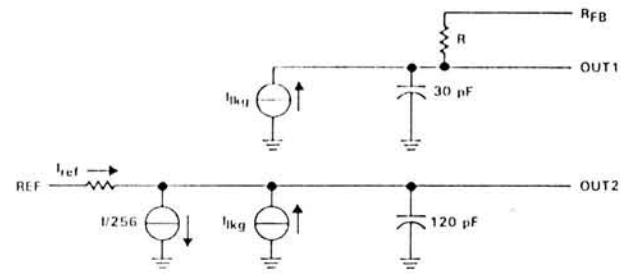


FIGURE 1. AD7524 EQUIVALENT CIRCUIT WITH ALL DIGITAL INPUTS LOW

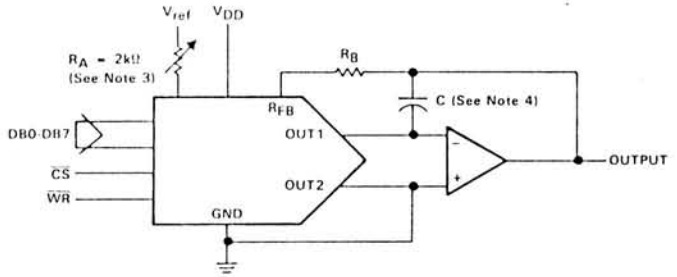


FIGURE 2. UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)

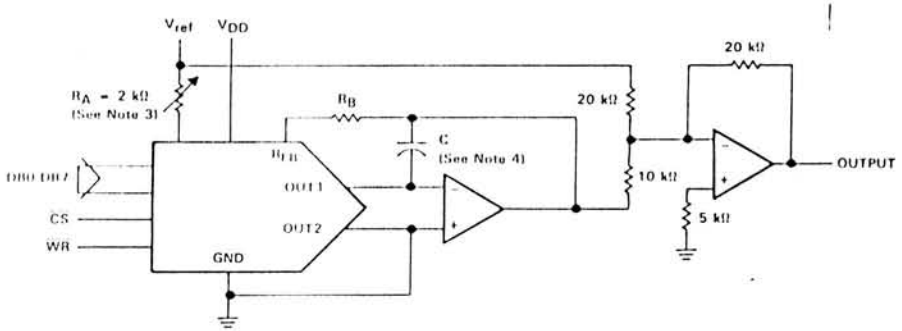


FIGURE 3. BIPOLAR OPERATION (4-QUADRANT OPERATION)

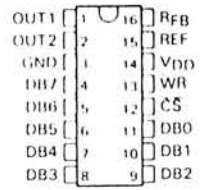
NOTES: 3. R_A and R_B used only if gain adjustment is required.
4. C phase compensation (10-15 pF) is required when using high speed amplifiers to prevent ringing or oscillation.

AD7524M
Advanced LinCMOS™ 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

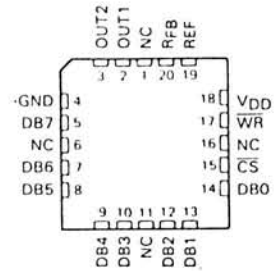
D3320, SEPTEMBER 1989

- Advanced LinCMOS™ Silicon-Gate Technology
- Easily Interfaced to Microprocessors
- On-Chip Data Latches
- Monotonicity Over Entire A/D Conversion Range
- Segmented High-Order Bits Ensure Low-Glitch Output
- Designed to be Interchangeable with Analog Devices AD7524, PMI PM-7524, and Micro Power Systems MP7524
- Fast Control Signaling for Digital Signal Processor Applications Including Interface with SMJ320

J PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 Bits
Linearity error	½ LSB Max
Power dissipation at V_{DD} = 5 V	5 mW Max
Settling time	100 ns Max
Propagation delay	80 ns Max

description

The AD7524M is an Advanced LinCMOS™ 8-bit digital-to-analog converter (DAC) designed for easy interface to most popular microprocessors.

The AD7524M is an 8-bit multiplying DAC with input latches and with a load cycle similar to the "write" cycle of a random access memory. Segmenting the high-order bits minimizes glitches during changes in the most-significant bits, which produce the highest glitch impulse. The AD7524M provides accuracy to ½ LSB without the need for thin-film resistors or laser trimming, while dissipating less than 5 mW typically.

Featuring operation from a 5-V to 15-V single supply, the AD7524M interfaces easily to most microprocessor buses or output ports. Excellent multiplying (2 or 4 quadrant) makes the AD7524M an ideal choice for many microprocessor-controlled gain-setting and signal-control applications.

The AD7524M is characterized for operation from −55°C to 125°C.

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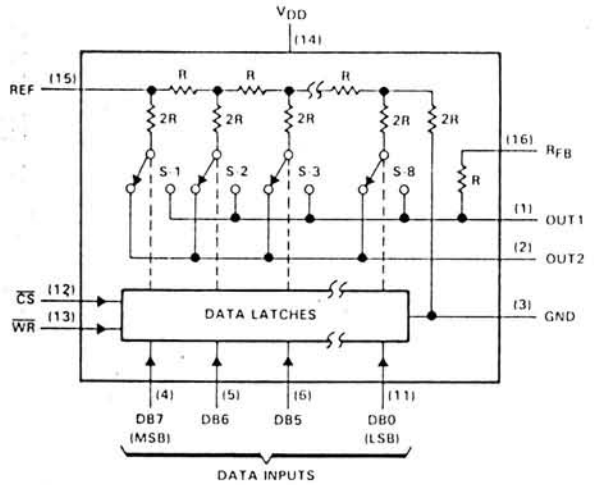
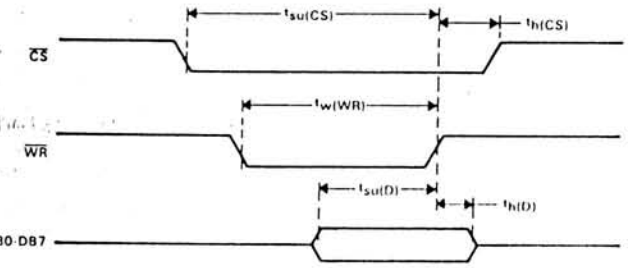
functional block diagram



operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} ..... −0.3 V to 17 V
Voltage between R_{FB} and GND ..... ±25 V
Digital input voltage, V_I ..... −0.3 V to V_{DD} + 0.3 V
Reference voltage, V_{ref} ..... ±25 V
Peak digital input current, I_I ..... 10 μA
Operating free-air temperature range ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

AD7524M
Advanced LinCMOS™ 8-BIT MULTIPLYING
DIGITAL-TO-ANALOG CONVERTER

recommended operating conditions

	V_{DD} = 5 V			V_{DD} = 15 V			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}	4.75	5	5.25	14.5	15	15.5	V
Reference voltage, V_{ref}		±10			±10		V
High level input voltage, V_{IH}	2.4			13.5			V
Low level input voltage, V_{IL}			0.8			1.5	V
$\overline{CS}$ setup time, $t_{su(CS)}$	40			40			ns
$\overline{CS}$ hold time, $t_{h(CS)}$	0			0			ns
Data bus input setup time, $t_{su(D)}$	25			25			ns
Data bus input hold time, $t_{h(D)}$	10			10			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$	40			40			ns
Operating free-air temperature, T_A	−55		125	−55		125	°C

electrical characteristics over recommended operating free-air temperature range, V_{ref} = 10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER			TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{IH}	High level input current		$V_I = V_{DD}$	Full range			10			10	μA
				25°C			1			1	
I_{IL}	Low level input current		V_I = 0	Full range			−10			−10	μA
				25°C			−1			−1	
I_{lkg}	Output leakage current	OUT1	DB0-DB7 at 0, $\overline{WR}$ and $\overline{CS}$ at 0 V, V_{ref} = ±10 V	Full range			±400			±200	nA
				25°C			±50			±50	
		OUT2	DB0-DB7 at V_{DD}, $\overline{WR}$ and $\overline{CS}$ at 0 V, V_{ref} = ±10 V	Full range			±400			±200	
				25°C			±50			±50	
I_{DD}	Supply current	Quiescent	DB0-DB7 at V_{IH} min or V_{IL} max				2			2	mA
		Standby	DB0-DB7 at 0 V or V_{DD}	Full range			500			500	μA
				25°C			100			100	
k_{SVS}	Supply voltage sensitivity, $\Delta g_{fsm}/\Delta V_{DD}$		ΔV_{DD} = 10%	Full range			0.16			0.04	%/%
				25°C		0.002	0.02		0.001	0.02	
C_i	Input capacitance, DB0-DB7, $\overline{WR}$, $\overline{CS}$		V_I = 0				5			5	pF
C_o	Output capacitance	OUT1	DB0-DB7 at 0, $\overline{WR}$ and $\overline{CS}$ at 0 V				30			30	pF
		OUT2					120			120	
		OUT1	DB0-DB7 at V_{DD}, $\overline{WR}$ and $\overline{CS}$ at 0 V				120			120	
		OUT2					30			30	
	Reference input impedance (R1 to GND)				5		20	5		20	kΩ

operating characteristics over recommended operating free-air temperature range, V_{ref} = 10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC} = 5 V		V_{DD} = 15 V		UNIT
			MIN	MAX	MIN	MAX	
Linearity error				±0.2		±0.2	%FSR
Gain error	See Note 1	Full range		±1.4		±0.6	%FSR
		25°C		±1		±0.5	
Settling time (to 1/2 LSB)	See Note 2			100		100	ns
Propagation delay from digital input to 90% of final analog output current	See Note 2			80		80	ns
Feedthrough at OUT1 or OUT2	V_{ref} = ±10 V (100 kHz sinewave), $\overline{WR}$ and $\overline{CS}$ at 0, DB0-DB7 at 0	Full range		0.5		0.5	%FSR
		25°C		0.25		0.25	
Temperature coefficient of gain	T_A = 25°C to t_{min} or t_{max}			±0.004		±0.001	%FSR/°C

NOTES: 1. Gain error is measured using the internal feedback resistor. Nominal Full Scale Range (FSR) = V_{ref} − 1 LSB.
2. OUT1 load = 100 Ω, C_{ext} = 13 pF, $\overline{WR}$ at 0 V, $\overline{CS}$ at 0 V, DB0-DB7 at 0 V to V_{DD} or V_{DD} to 0 V.

PRINCIPLES OF OPERATION

The AD7524M is an 8-bit multiplying D/A converter consisting of an inverted R-2R ladder, analog switches, and data input latches. Binary weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state. The high-order bits are decoded and these decoded bits, through a modification in the R-2R ladder, control three equally weighted current sources. Most applications only require the addition of an external operational amplifier and a voltage reference.

The equivalent circuit for all digital inputs low is seen in Figure 1. With all digital inputs low, the entire reference current, I_{ref}, is switched to OUT2. The current source I/256 represents the constant current flowing through the termination resistor of the R-2R ladder, while the current source I_{lkg} represents leakage currents to the substrate. The capacitances appearing at OUT1 and OUT2 are dependent upon the digital input code. With all digital inputs high, the off-state switch capacitance (30 pF maximum) appears at OUT2 and the on-state switch capacitance (120 pF maximum) appears at OUT1. With all digital inputs low, the situation is reversed as shown in Figure 1. Analysis of the circuit for all digital inputs high is similar to Figure 1; however, in this case, I_{ref} would be switched to OUT1.

Interfacing the AD7524M D/A converter to a microprocessor is accomplished via the data bus and the $\overline{CS}$ and $\overline{WR}$ control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the AD7524M analog output responds to the data activity on the DB0-DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0-DB7 inputs are latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled regardless of the state of the $\overline{WR}$ signal.

The AD7524M is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant or 4-quadrant multiplication are shown in Figures 2 and 3. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.

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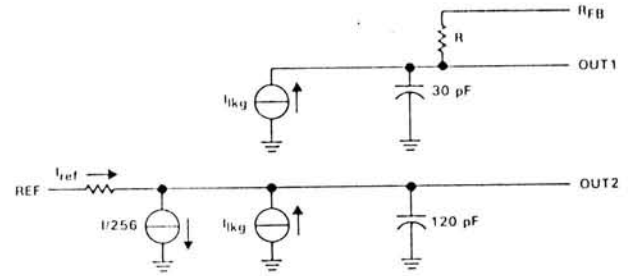


FIGURE 1. AD7524M EQUIVALENT CIRCUIT WITH ALL DIGITAL INPUTS LOW

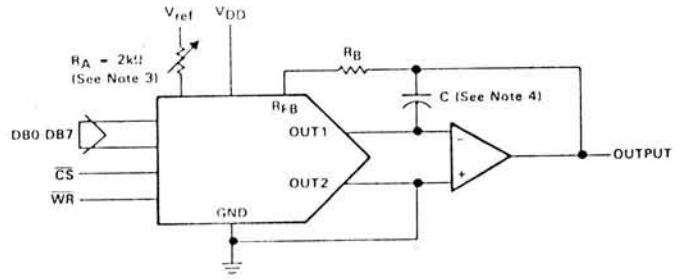


FIGURE 2. UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)

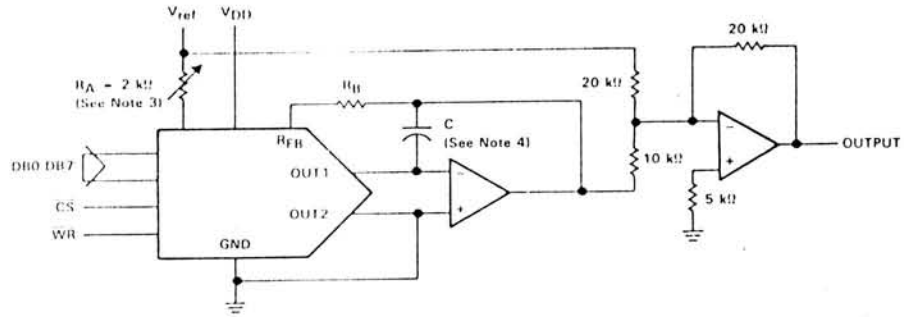


FIGURE 3. BIPOLAR OPERATION (4-QUADRANT OPERATION)

NOTES: 3. R_A and R_B used only if gain adjustment is required.
4. C phase compensation (10-15 pF) is required when using high-speed amplifiers to prevent ringing or oscillation.

PRINCIPLES OF OPERATION

Table 1. Unipolar Binary Code

DIGITAL INPUT (SEE NOTE 5) MSB LSB	ANALOG OUTPUT
11111111	$-V_{ref}$ (255/256)
10000001	$-V_{ref}$ (129/256)
10000000	$-V_{ref}$ (128/256) = $-V_{ref}/2$
01111111	$-V_{ref}$ (127/256)
00000001	$-V_{ref}$ (1/256)
00000000	0

Table 2. Bipolar (Offset Binary) Code

DIGITAL INPUT (SEE NOTE 6) MSB LSB	ANALOG OUTPUT
11111111	V_{ref} (127/128)
10000001	V_{ref} (1/128)
10000000	0
01111111	$-V_{ref}$ (1/128)
00000001	$-V_{ref}$ (127/128)
00000000	$-V_{ref}$

NOTES: 5. LSB = 1/256 (V_{ref}).
6. LSB = 1/128 (V_{ref})

microprocessor interfaces

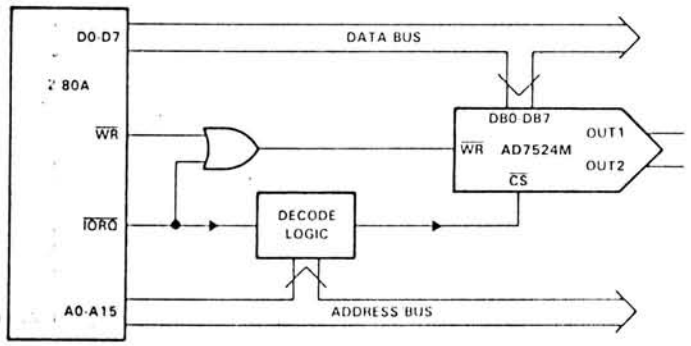


FIGURE 4. AD7524M–Z-80A INTERFACE

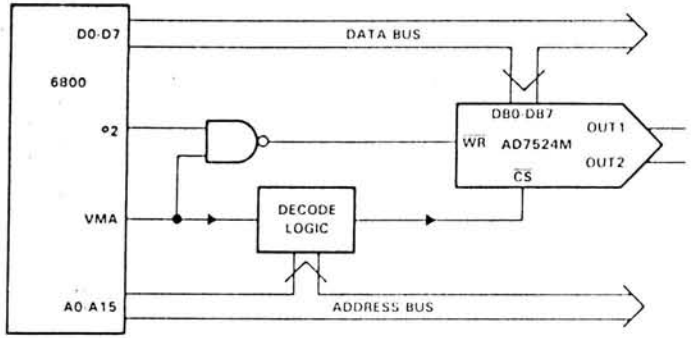


FIGURE 5. AD7524M–6800 INTERFACE

microprocessor interfaces (continued)

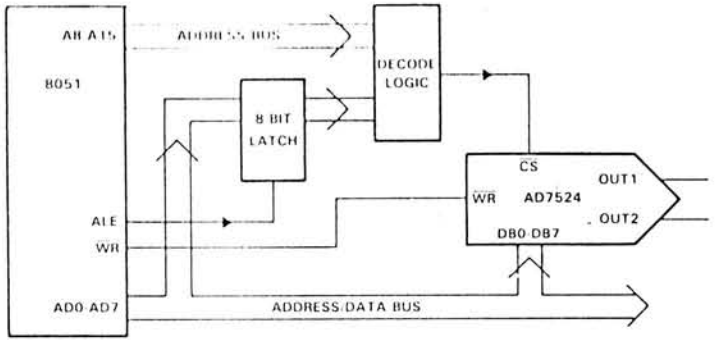


FIGURE 6. AD7524M–8051 INTERFACE

M5M5178P-35,-45,-55

PRELIMINARY
Notice: This is not a final specification
Some parametric limits are subject to change

65536-BIT (8192-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

This is a family of 8192 word by 8-bit static RAMs, fabricated with the high performance CMOS silicon gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible.

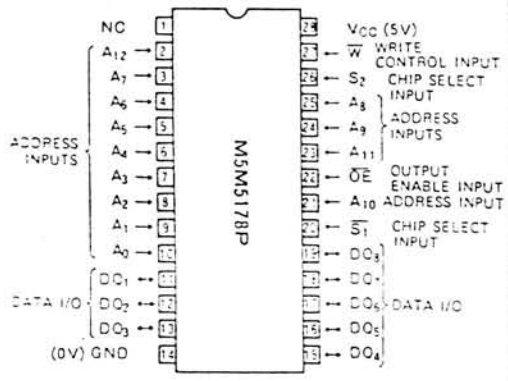
FEATURES

- Fast access time M5M5178P-35 . . . . . 35ns (max.)
  M5M5178P-45 . . . . . 45ns (max.)
  M5M5178P-55 . . . . . 55ns (max.)
- Single +5V Power Supply
- Fully Static Operation: No Clocks, No Refresh
- Directly TTL Compatible: All Inputs and Outputs
- Three-State Outputs: OR-tie Capability
- Simple Memory Expansion by $\overline{S_1}$, S_2
- $\overline{OE}$ Prevents Data Contention in The I/O Bus
- Common Data I/O
- 300 mil package

APPLICATION

High speed memory system

PIN CONFIGURATION (TOP VIEW)



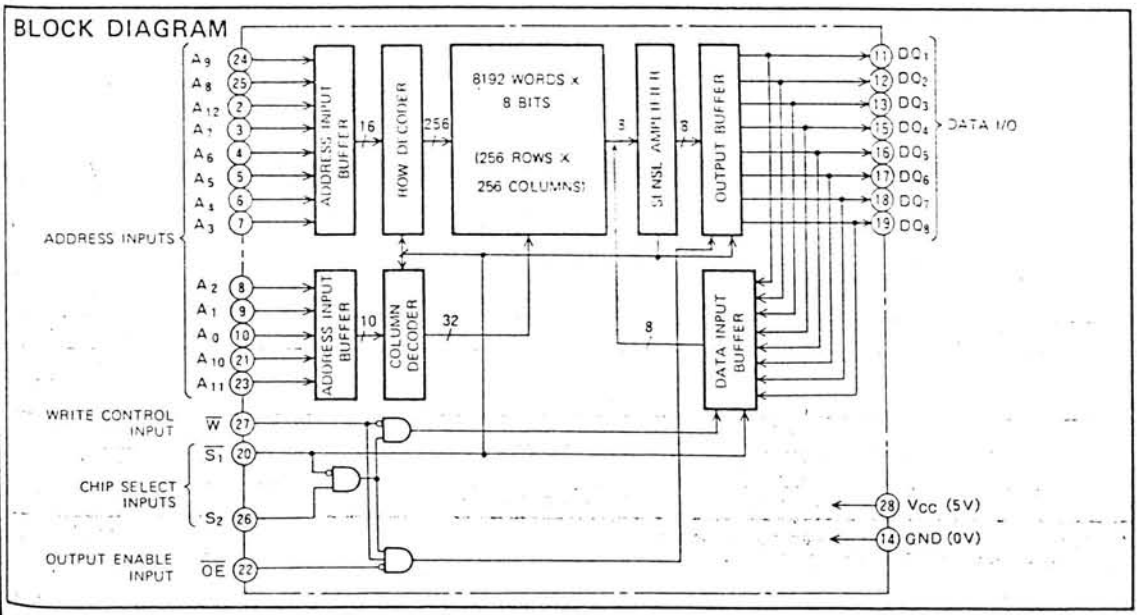
Outline 28P4Y

FUNCTION

The operation mode of the M5M5178P is determined by a combination of the device control inputs $\overline{S_1}$, S_2, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table. (see next page)

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S_1}$ and the high level S_2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S_1}$ or S_2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

BLOCK DIAGRAM



A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S_1}$ and S_2 are in an active state ($\overline{S_1}$ = L, S_2 = H)

When setting $\overline{S_1}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expantion by $\overline{S_1}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC2} or I_{CC3}.

FUNCTION TABLE

$\overline{S_1}$	S_2	$\overline{W}$	$\overline{OE}$	Mode	DQ	I_{CC}
L	L	X	X	Non selection	high-impedance	Active
H	X	X	X	Non selection	high-impedance	Standby
L	H	L	X	Write	D_{IN}	Active
L	H	H	L	Read	D_{OUT}	Active
L	H	H	H		high-impedance	Active

RECOMMENDED OPERATING CONDITIONS (T_a = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
GND	Supply voltage		0		V
V_{IL}	Low input voltage	−0.3		0.8	V
V_{IH}	High input voltage	2.2		V_{CC}+0.3	V

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3 ~ 7	V
V_I	Input voltage		−0.3 ~ V_{CC}+0.3	V
V_O	Output voltage		0 ~ V_{CC}	V
Pd	Power dissipation	T_a = 25°C	1000	mW
Topr	Operating temperature		−10 ~ 85	°C
Tstg	Storage temperature		−65 ~ 150	°C

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ±10%, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low input voltage			−0.3		0.8	V
V_{OH}	High output voltage		I_{OH} = −4mA	2.4			V
V_{OL}	Low output voltage		I_{OL} = 8 mA			0.4	V
I_I	Input current		V_I = 0 ~ V_{CC}			±1	μA
I_{OZH}	High level output current in off state		$\overline{S_1}$ = V_{IH} or S_2 = V_{IL} or $\overline{OE}$ = V_{IH}			1	μA
I_{OZL}	Low level output current in off state		$V_{I/O}$ = 0 − V_{CC}			−1	μA
I_{CC1}	Active supply current		$\overline{S_1}$ = V_{IL} or S_2 = V_{IH} Output open Other inputs = V_{IH}			120	mA
I_{CC2}	Stand by supply current		S_2 = V_{IL}, $\overline{S_1}$ = V_{IH}, Other inputs = 0 ~ V_{CC}			25	mA
I_{CC3}	Stand by supply current		$\overline{S_1} \geq V_{CC} - 0.2V$ Other inputs ≤ 0.2V or V_{CC} − 0.2V			2	mA
C_I	Output capacitance (T_a = 25°C)	$\overline{S_1}$, S_2, $\overline{OE}$, $\overline{W}$	V_I = GND, V_i = 25mVrms, f = 1MHz			7	pF
		A_0 ~ A_{12}				6	
C_O	Output capacitance (T_a = 25°C)		V_O = GND, V_O = 25mVrms, f = 1MHz			8	pF

Note 1 Direction for current flowing into IC is indicated as positive (no mark)
2 Typical value is V_{CC} = 5V, T_a = 25°C

SWITCHING CHARACTER
Read cycle

Symbol	Param
t_{CR}	Read cycle time
$t_{a(A)}$	Address access time
$t_{a(S1)}$	Chip select 1 access time
$t_{a(S2)}$	Chip select 2 access time
$t_{a(OE)}$	Output enable access time
$t_{dis(S1)}$	Output disable time after S
$t_{dis(S2)}$	Output disable time after S
$t_{dis(OE)}$	Output disable time after O
$t_{en(S1)}$	Output enable time after S
$t_{en(S2)}$	Output enable time after S
$t_{en(OE)}$	Output enable time after
$t_{v(A)}$	Data valid time after addr

TIMING REQUIREMENT
Write cycle

Symbol	P
t_{cw}	Write cycle time
$t_{w(w)}$	Write pulse width
$t_{su(A)}$	Address set up time
$t_{su(S1)}$	Chip select 1 set up tim
$t_{su(S2)}$	Chip select 2 set up tim
$t_{su(D)}$	Data set up time
$t_{h(D)}$	Data hold time
$t_{rec(w)}$	Write recovery time
$t_{dis(w)}$	Output disable time af
$t_{dis(OE)}$	Output disable time a
$t_{en(w)}$	Output enable time af
$t_{en(OE)}$	Output enable time af

DO	Icc
High-impedance	Active
High-impedance	Standby
DIN	Active
DOUT	Active
High-impedance	Active

Ratings	Unit
−0.3 ~ 7	V
−0.3 ~ Vcc+0.3	V
0 ~ Vcc	V
1000	mW
−10 ~ 85	°C
−65 ~ 150	°C

Limits			Unit
	Typ	Max	
2.2		Vcc+0.3	V
0.3		0.8	V
2.4			V
		0.4	V
		±1	μA
		1	μA
		−1	μA
		120	mA
		25	mA
		2	mA
		7	pF
		6	
		8	pF

SWITCHING CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Read cycle

Symbol	Parameter	Limits									Unit
		M5M5178P-35			M5M5178P-45			M5M5178P-55			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	35			45			55			ns
$t_{a(A)}$	Address access time			35			45			55	ns
$t_{a(S1)}$	Chip select 1 access time			35			45			55	ns
$t_{a(S2)}$	Chip select 2 access time			15			20			25	ns
$t_{a(OE)}$	Output enable access time			15			20			25	ns
$t_{dis(S1)}$	Output disable time after $\overline{S_1}$ high			20			25			35	ns
$t_{dis(S2)}$	Output disable time after S_2 low			20			25			35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			20			25			35	ns
$t_{en(S1)}$	Output enable time after $\overline{S_1}$ low	5			5			5			ns
$t_{en(S2)}$	Output enable time after S_2 high	3			3			3			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	3			3			3			ns
$t_{v(A)}$	Data valid time after address change	3			3			3			ns

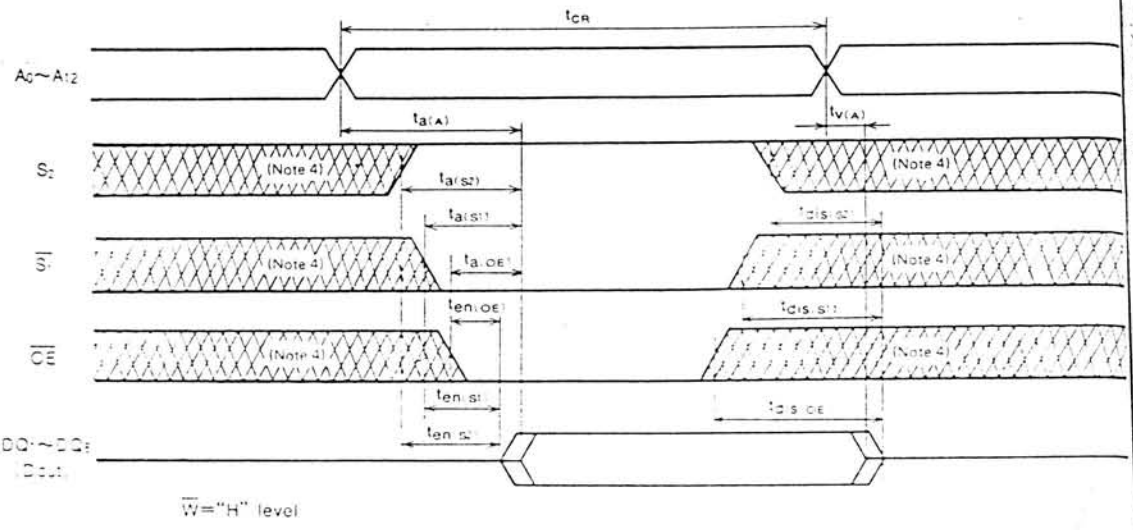
TIMING REQUIREMENTS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Write cycle

Symbol	Parameter	Limits									Unit
		M5M5178P-35			M5M5178P-45			M5M5178P-55			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{cw}	Write cycle time	35			45			55			ns
$t_{w(W)}$	Write pulse width	20			25			30			ns
$t_{su(A)}$	Address set up time	0			0			0			ns
$t_{su(S1)}$	Chip select 1 set up time	30			40			45			ns
$t_{su(S2)}$	Chip select 2 set up time	20			25			30			ns
$t_{su(D)}$	Data set up time	17			20			30			ns
$t_{h(D)}$	Data hold time	0			0			0			ns
$t_{rec(W)}$	Write recovery time	3			3			3			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low			15			20			20	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			20			25			25	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	0			0			0			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	3			3			3			ns

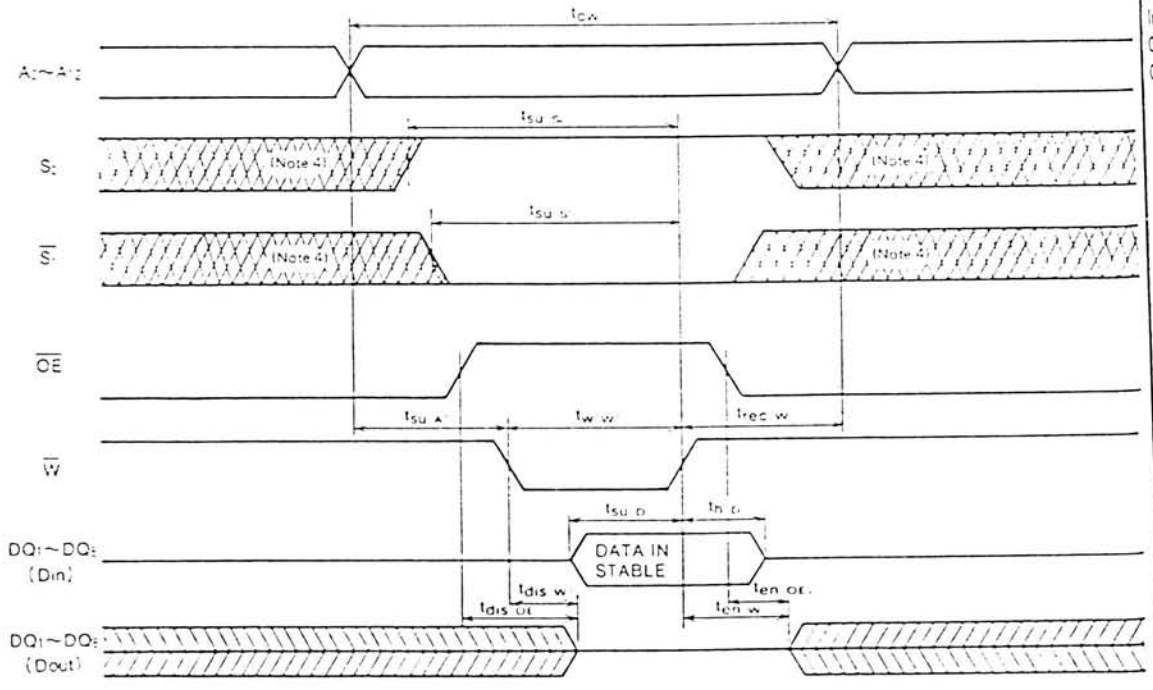
TIMING DIAGRAM

Read cycle

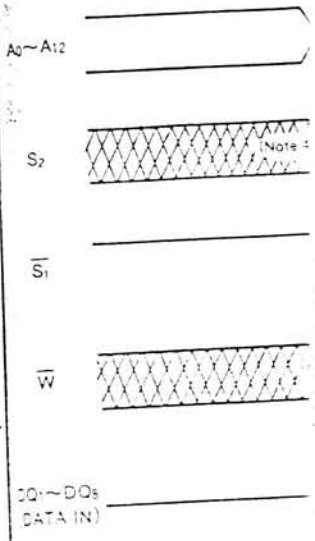


W="H" level

Write cycle (W control)



Write cycle (S control)



CONDITIONS

Input pulse levels . . . . . .
Input rise and fall time . . . . .
Input timing reference level . . .
Output timing reference level . .
Output loads . . . . . .

Note 4 Hatching indicates the sta
5 Writing is executed while
6 If S goes low at the same
impedance state
7 Don't apply inverted pha

M5M5256P-10, -12, -15, -10L, -12L, -15L

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

This M5M5256P is a 262,144-bit CMOS static RAM organized as 32,768 words by 8 bits which is fabricated using high-performance double polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periferals result in a high-density and low-power static RAM. It is ideal for the memory systems which require simple interface.

The stand-by current is low enough for a battery back-up application. It is mounted in a standard 28 pin package and configured in an industrial standard 32K x 8-bit pinout.

FEATURES

Type	Access time (max)	Power supply current (typical)	
		Active (max)	Stand-by (max)
M5M5256P-10	100ns	70mA	2mA
M5M5256P-12	120ns		
M5M5256P-15	150ns		
M5M5256P-10L	100ns		100μA
M5M5256P-12L	120ns		
M5M5256P-15L	150ns		

- Single +5V Power Supply
- No Clocks, No Refresh
- Data-Hold on +2V Power Supply
- Directly TTL Compatible: All Inputs and Outputs
- Three-State Outputs: OR-tie Capability
- Simple Memory Expantion by $\overline{S}$
- $\overline{OE}$ Prevents Data Contention in the I/O Bus
- Common Data I/O

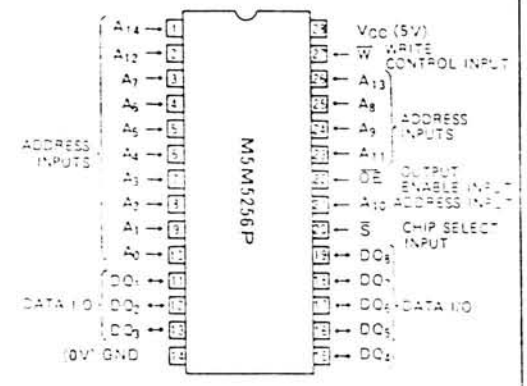
APPLICATION

Small Capacity Memory Units.

FUNCTION

The operation mode of the M5M5256P is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$.

PIN CONFIGURATION (TOP VIEW)



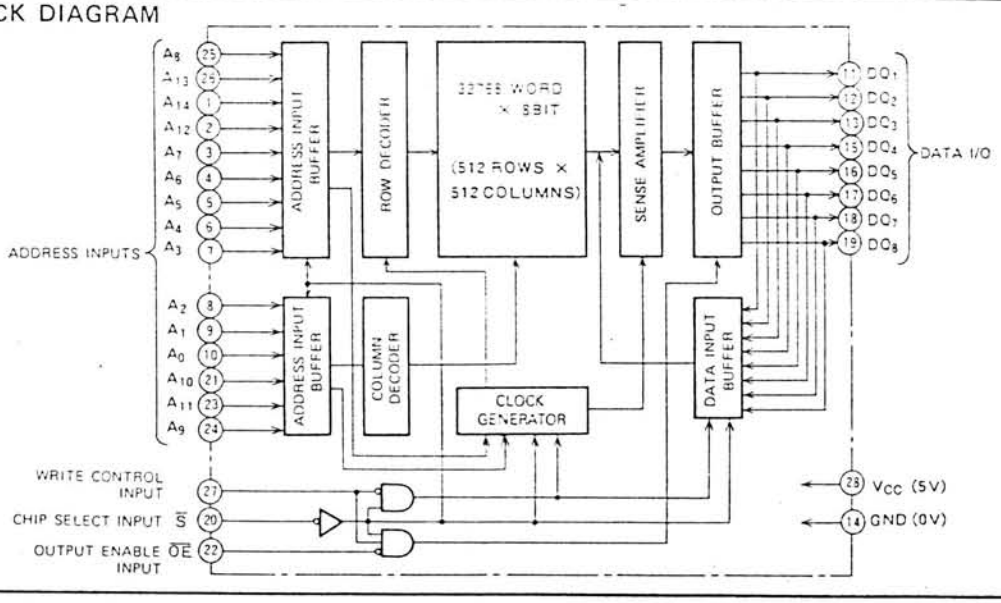
Outline 28P4

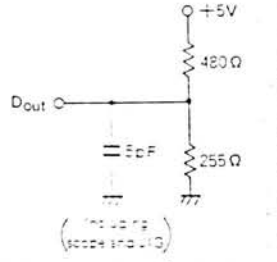
Each mode is summarized in the function table. (see next page)

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state.

BLOCK DIAGRAM





ig. 2 Output load for t_{en} t_{dis}

M5M5256P-10, -12, -15, -10L, -12L, -15L

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

When setting $\overline{S}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expantion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CCS} or I_{CC6}, and the memory data can be held +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	I_{CC}
H	X	X	Non selection	high-impedance	Standby
L	L	X	Write	D_{IN}	Active
L	H	L	Read	D_{OUT}	Active
L	H	H		high-impedance	Active

RECOMMENDED OPERATING CONDITIONS (T_a = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
GND	Supply voltage		0		V
V_{IL}	low input voltage	−0.3		0.8	V
V_{IH}	high input voltage	2.2		V_{CC}+0.3	V

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3 ~ 7	V
V_I	Input voltage		−0.3 ~ V_{CC}+0.3	V
V_O	Output voltage		0 ~ V_{CC}	V
P_D	Power dissipation	T_a = 25°C	700	mW
T_{opr}	Operating temperature		0 ~ 70	°C
T_{stg}	Storage temperature		−65 ~ 150	°C

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High input voltage		2.2		V_{CC}+0.3	V
V_{IL}	Low input voltage		−0.3		0.8	V
V_{OH}	High output voltage	I_{OH} = −1mA	2.4			V
V_{OL}	Low output voltage	I_{OL} = 2 mA			0.4	V
I_I	Input current	V_I = 0 ~ V_{CC}			±1	μA
I_{OZH}	High level output current in off state	$\overline{S}$ = V_{IH} or $\overline{OE}$ = V_{IH}			1	μA
I_{OZL}	Low level output current in off state	$V_{I/O}$ = 0 ~ V_{CC}			−1	μA
I_{CC1}	Active supply current (DC, MOS level)	$\overline{S}$ < 0.2, $\overline{W}$ > V_{CC} − 0.3 output open other input < 0.2 or > V_{CC} − 0.3 tcycle = 1μs		15	25	mA
I_{CC2}	Active supply current (AC, MOS level)	$\overline{S}$ < 0.2, $\overline{W}$ > V_{CC} − 0.3 output open other input < 0.2 or > V_{CC} − 0.3 Min cycle		30	65	mA
I_{CC3}	Active supply current (DC, TTL level)	$\overline{S}$ = V_{IL}, $\overline{W}$ = V_{IH} output open other input = V_{IL} or V_{IH} tcycle = 1μs		20	30	mA
I_{CC4}	Active supply current (AC, TTL level)	$\overline{S}$ = V_{IL}, $\overline{W}$ = V_{IH} output open other input = V_{IL} or V_{IH} Min cycle		35	70	mA
I_{CCS}	Stand by supply current	$\overline{S}$ ≥ V_{CC} − 0.2V Other inputs = 0 ~ V_{CC}			2(P)	mA
I_{CC6}	Stand by supply current				100(P-L)	μA
C_I	Input capacitance (T_a = 25°C)	$\overline{S}$ = V_{IH}, Other inputs = 0 ~ V_{CC}			3	mA
C_O	Output capacitance (T_a = 25°C)	V_I = GND, V_I = 25mVrms, f = 1MHz			6	pF
		V_O = GND, V_O = 25mVrms, f = 1MHz			8	pF

Note 1 Direction for current flowing into IC is indicated as positive (no mark)
2 Typical value is V_{CC} = 5V, T_a = 25°C

SWITCHING CHARACTER

Read cycle

Symbol	Para
t_{cR}	Read cycle time
$t_{a(A)}$	Address access time
$t_{a(S)}$	Chip select access time
$t_{a(OE)}$	Output enable access time
$t_{dis(S)}$	Output disable time after
$t_{dis(OE)}$	Output disable time after
$t_{en(S)}$	Output enable time after
$t_{en(OE)}$	Output enable time after
$t_{v(A)}$	Data valid time after add

TIMING REQUIREMEN

Write cycle

Symbol	
t_{cW}	Write cycle time
$t_{w(W)}$	Write pulse width
$t_{su(A)}$	Address set up time
$t_{su(A-\overline{W}H)}$	Address set up time w
$t_{su(S)}$	Chip select set up time
$t_{su(D)}$	Data set up time
$t_{h(D)}$	Data hold time
$t_{rec(W)}$	Write recovery time
$t_{dis(W)}$	Output disable time af
$t_{dis(OE)}$	Output disable time af
$t_{en(W)}$	Output enable time af
$t_{en(OE)}$	Output enable time af

E

	DO	ICC
n	High-impedance	Standby
	DIN	Active
	DOUT	Active
	High-impedance	Active

Ratings	Unit
−0.3 ~ 7	V
−0.3 ~ VCC+0.3	V
0 ~ VCC	V
700	mW
0 ~ 70	°C
−65 ~ 150	°C

Limits			Unit
Min	Typ	Max	
2.2		VCC+0.3	V
−0.3		0.8	V
2.4			V
		0.4	V
		±1	μA
		1	μA
		−1	μA
	15	25	mA
	30	65	mA
	20	30	mA
	35	70	mA
		2(P)	mA
		100(P-L)	μA
		3	mA
		6	pF
		8	pF

SWITCHING CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Read cycle

Symbol	Parameter	Limits									Unit
		M5M5256P-10 M5M5256P-10L			M5M5256P-12 M5M5256P-12L			M5M5256P-15 M5M5256P-15L			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
tcR	Read cycle time	100			120			150			ns
ta(A)	Address access time			100			120			150	ns
ta(S)	Chip select access time			100			120			150	ns
ta(OE)	Output enable access time			50			60			75	ns
tdis(S)	Output disable time after $\overline{S}$ high			35			40			45	ns
tdis(OE)	Output disable time after $\overline{OE}$ high			35			40			45	ns
ten(S)	Output enable time after $\overline{S}$ low	10			10			10			ns
ten(OE)	Output enable time after $\overline{OE}$ low	10			10			10			ns
tv(A)	Data valid time after address change	20			20			20			ns

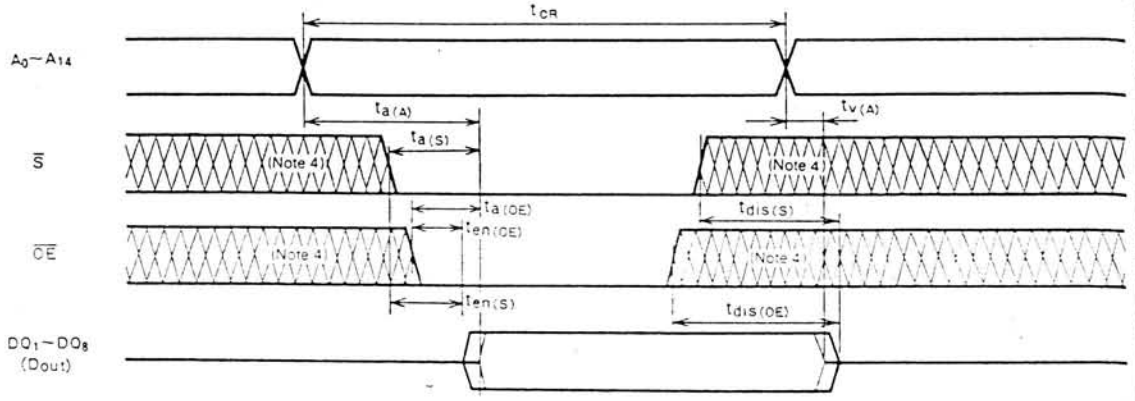
TIMING REQUIREMENTS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Write cycle

Symbol	Parameter	Limits									Unit
		M5M5256P-10 M5M5256P-10L			M5M5256P-12 M5M5256P-12L			M5M5256P-15 M5M5256P-15L			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
tcw	Write cycle time	100			120			150			ns
tw(W)	Write pulse width	60			70			80			ns
tsu(A)	Address set up time	0			0			0			ns
tsu(A-$\overline{W}$H)	Address set up time with respect to $\overline{W}$ high	80			85			90			ns
tsu(S)	Chip select set up time	80			85			90			ns
tsu(D)	Data set up time	35			40			50			ns
th(D)	Data hold time	0			0			0			ns
trec(W)	Write recovery time	0			0			0			ns
tdis(W)	Output disable time after $\overline{W}$ low			35			40			45	ns
tdis(OE)	Output disable time after $\overline{OE}$ high			35			40			45	ns
ten(W)	Output enable time after $\overline{W}$ high	10			10			10			ns
ten(OE)	Output enable time after $\overline{OE}$ low	10			10			10			ns

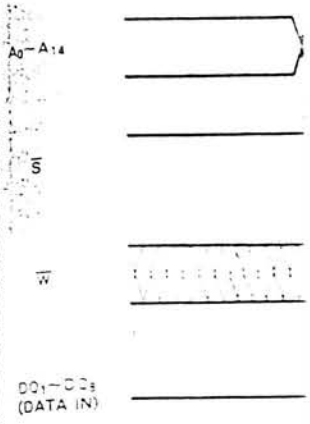
TIMING DIAGRAM

Read cycle



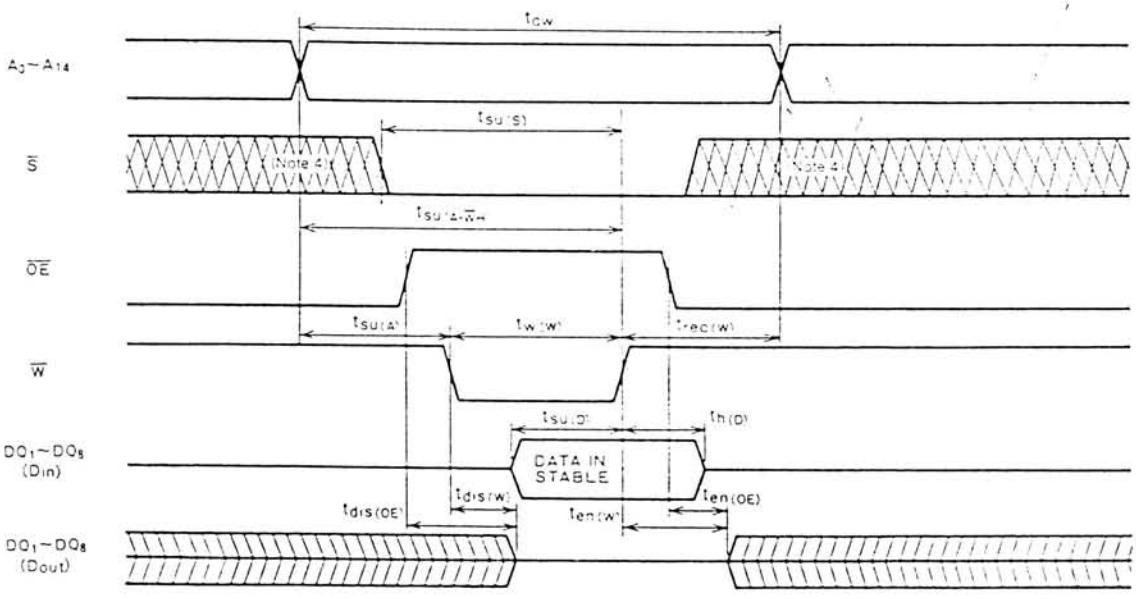
$\overline{W}$ = "H" level

Write cycle ($\overline{S}$ control)



Note 3: "test conditions"

Write cycle (WE control)



POWER DOWN CHARAC

ELECTRICAL CHARACT

Symbol	Para
$V_{CC(PD)}$	Power
$V_{I(\overline{S})}$	
$I_{CC(PD)}$	Power

TIMING REQUIREMEN

Symbol	Pa
$t_{su(PD)}$	Power
$t_{rec(PD)}$	Power

POWER DOWN CHARA