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Integrated System for a High Resolution MEMS Accelerometer

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Resumo

Só com os enormes desenvolvimentos na tecnologia de fabricação de circuitos integrados, como tecnologias CMOS, é que a miniaturização de dispositivos micro electrónicos foi possível. Com este decréscimo no tamanho desses circuitos, e a crescente utilização desta tecnologia numa vasta área de aplicações, o preço desta tecnologia caiu, permitindo a integração desta tecnologia dispendiosa em produtos electrónicos comuns. Os sensores inerciais são, hoje em dia, aplicados em bastantes produtos dos quais no passado nem seria possível de imaginar.

O desenvolvimento de um sistema de sensores inerciais, capaz de detectar a menor das acelerações e amplifica-la com o intuito de ser convertidas digitalmente para futuro processamento, usando o menor espaço possível e atingindo a melhor das performances é o objectivo deste trabalho.

Este relatório discute um sistema integrado para leitura de um Acelerómetro MEMS de Elevada Resolução. O sistema irá permitir a medição da aceleração de um dispositivo, amplificando o sinal e convertendo o sinal para digital, de modo a ter uma maior facilidade de manipulação e calcular, digitalmente, a sua aceleração

O amplificador de carga totalmente diferencial foi desenvolvido de modo a amplificar o sinal enviado pelo sensor. A diferença de capacidade resultante de uma aceleração é convertida numa variação de tensão que será posteriormente amplificada. Como essas variações são extremamente pequenas, ao fazer a amplificação do sinal, será adicionado ruído (ruído 1/f). O amplificador precisará de um circuito para cancelar esse ruído. O circuito escolhido para o cancelar é o *Correlated Double Sampling*.

Depois de o sinal ser amplificado, precisa de ser convertido para digital. Um modelador Sigma Delta de segunda ordem foi desenvolvido. O sinal de saída do modelador é digital, mas ainda não foi decimado. O modelador tem uma estrutura de condensadores comutados, com circuito de redução de ruído CDS.

Este projecto foi desenvolvido no ano 2009/2010 na Faculdade de Engenharia da Universidade do Porto, como a dissertação final do Mestrado Integrado em Engenharia Electrotécnica e Computadores.

Abstract

Only with the enormous developments in Integrated circuits fabrication techniques, such as CMOS technologies, the miniaturization of microelectronics devices was possible. By this decrease in the size of the circuits, and the use of these technologies in a wide range of applications, the price of these technologies dropped allowing the integration of technology, in common personal electronics.

This project aims the development of a inertial sensor system, capable of sensing the smallest acceleration and amplify it in order to be digitally converted for forward processing, using the least space possible and having the best achievable performance. Inertial sensors are, nowadays, applied in many products that in the past were not even thought possible.

This report discusses an Integrated System for a High Resolution MEMS Accelerometer. The system will enable the measurement of acceleration of a device, will amplify the signal and will convert the signal to digital, in order to be easier to manipulate its information and to digitally calculate the acceleration.

The system is composed by a MEMS capacitive accelerometer, a fully differential charge amplifier and a sigma delta modulator. The main goal of this project was to develop a Fully Differential Charge Amplifier and a Sigma Delta Modulator for a high resolution MEMS Accelerometer already developed in [6].

The fully differential charge amplifier amplifies the signal sent by the sensor. The capacity difference is converted in a voltage variation and then amplified. Since these variations are very small, the amplification adds noise to the signal (1/f type). In order to cancel that noise, the amplifier needs a circuit to reduce it. The technique chosen for this noise reduction is the Correlated Double Sampling.

After signal amplification, it needs to be converted to digital. A 2^{nd} order Sigma Delta Modulator was developed. The output signal is digital, although not yet decimated. The Modulator is also a Switched Capacitor structure, with CDS noise reduction technique.

This project is being developed in the year 2009/10 at the Faculty of Engineering of the University of Porto, as the final Dissertation for the Integrated Master in Electrical and Computers Engineering.

Agradecimentos

Ao longo destes meses todos de desenvolvimento da dissertação tive a ajuda de várias pessoas, quer ao nível técnico, quer ao nível espiritual que nestes momentos se torna imprescindível.

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Finalmente queria agradecer à minha família por ter paciência comigo, nos momentos de maior preocupação e stress por que passei, e também por acreditar em mim ao longo destes anos.

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Acronyms and symbols

AC	Alternating Current
ADC	Analogue to Digital Converter
CDS	Correlated Double Sampling
CHS	Chopper Stabilization
CMFB	Common Mode Feedback
CMOS	Complementary Metal-Oxide-Semiconductor
DAC	Digital to Analogue Converter
DC	Direct Current
EMI	Electromagnetic Interference
FFT	Fats Fourier Transform
LPF	Low Pass Filter
MEMS	Micromechanical Systems
MSPS	Mega Samples Per Second
Op-Amp	Operational Amplifier
SC	Switched Capacitors
S&H	Sample and Hold
SNR	Signal to Noise Ratio
SOI	Silicon On Insulator
VCMO	Output Common Mode Voltage
VCVS	Voltage Controlled Voltage Source

Chapter 1

Introduction

Nowadays, we have more and more present in our daily lives inertial sensors: pressure, optical and others. They are in most of our normal professional tools or in our gadgets. MEMS (Microelectromechanical Systems) technologies are present in most of these sensors. One of the most used, still with an enormous development margin, are the MEMS accelerometers. MEMS accelerometers are used in automotive applications, such as airbags and stability systems; in biomedical systems, like activity monitoring; in our consumer electronics like mobile phones and camcorders or even gamepads. The intense use of these products demands a development of the technology and a huge decrease of sensor costs, as they are being integrated in our daily use devices, either to improve performance or to enable features that they were not yet capable of doing.

1.1 - Problem Statement

The challenge posed to this dissertation was the development of an Integrated System for an Inertial Sensor, in this case, a MEMS accelerometer. The system is to be fully integrated. It needs to read the acceleration of a movement through the MEMS sensor, having for that a precise measuring circuit. After this measure, the system needs an analogue to digital converter (ADC) to convert the information for an easier manipulation and post processing.

The integrated system to be developed consists of three major parts. The sensor itself, which as been previously designed [6], a device that amplifies the sensors readings (charge amplifier), and an analogue to digital converter, to convert the analogue signal to digital, so that it can be post-processed digitally. Figure 1 presents a block diagram of the system to be designed.

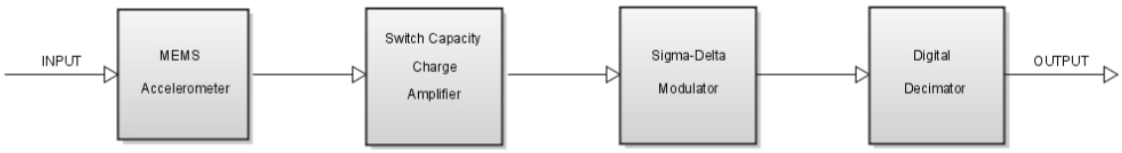


Figure 1 - Block Diagram of the System

1.2 - Adopted solution

The accelerometer, as referred earlier, was previously built and is presented in [6]. It is a MEMS capacitive accelerometer fabricated in a SOI process and uses a novel time measurement approach. As the variations of the capacitor values, due to acceleration, are too small (in the order of fF to pF), there is a need to amplify these variations with extreme care. To amplify them, a switched capacitor (SC) charge amplifier, with differential input and output, will be developed. This architecture will result in an amplifier more immune to external noise and with a higher output voltage swing. The modulator that will be developed is a 2nd Order Sigma Delta modulator.

The goal of this project then consists on the development of the readout chain of the system, which is composed by a Fully Differential Charge Amplifier and Sigma Delta Modelator. A fully differential charge amplifier, with chopper stabilisation (CHS), has already been developed in [19]. In order to improve its performance, the chopper stabilization technique used for reducing the effects of the Op-Amp (operational amplifier) imperfections, will be substituted by Correlated Double Sampling technique (CDS). The difference between these two techniques will be further studied in chapter 2 section 2.3.1. A new fully differential switched capacitor amplifier with CDS will also be developed. The Sigma Delta Modulator will convert the signal from the sensor, already amplified, and make it ready to be used by a digital machine. The converter must be a 2nd order Sigma Delta modulator in order to diminish the quantization noise [25]

1.3 - Organisation of this paper

This thesis is divided into 5 chapters. The first chapter will give the reader an overview of the main theme, the integrated system for a high resolution MEMS accelerometer. It presents the problem and the thought solution. It will also present the organisation of this paper.

Chapter 2 gives the background information about Inertial Sensors and the Readout Chain. It presents several types of sensors available. The main focus are Capacitive MEMS Accelerometers. The MEMS Capacitive Accelerometer used in this project is presented thoroughly. Also an introduction of fully differential amplifiers and Sigma Delta modulators is made. An introduction to fully differential amplifiers is also presented, along with an overview to the advantages of using switched capacitors circuits, and a comparison between

techniques for reducing amplifier imperfections such as correlated double sampling and chopper stabilization. The several types of modulators are presented, exposing the advantages and disadvantages of each one. The Sigma Delta modulation is explained in more detail.

Chapter 3 presents some projects, already developed but related to this work. Those projects were the foundations for the development of this dissertation. They are presented and explained in some detail.

In chapter 4, the developed fully differential SC amplifier with CDS is presented. The schematic is showed and described. Also in this chapter, a presentation of the 2^{nd} order Sigma Delta modulator is made and its structure is explained. The results of all simulations are presented.

In chapter 5 conclusions are taken. A general summary of the entire work for this dissertation is made. Future work ideas are written at the end.

Finally, some of the figures, due to their size, are remitted to the Appendix. This allows a better visualization of them.

Chapter 2

Background

2.1 – Micro-Electro-Mechanical Systems – Micromachined Inertial Sensors

Micro-Electro-Mechanical Systems (Micromachined Sensors) combine an electrical and a mechanical device, which are fabricated using integrated circuit batch-processing technologies. This integration is made in a common silicon substrate. While the electronic elements are fabricated using integrated circuit layers processes, the mechanical components are fabricated using compatible fabrication processes that etch away parts of the silicon wafer or add new structural layers, in order to build the desired component [1]. These types of systems have a characteristic length between 1μm and 1 mm [2]. They have a wide range of application, such as inertial, force/torque and flow sensors.

MEMS inertial sensors are a very important group of silicon-based sensors. They can measure linear (accelerometers) or angular (gyroscopes) accelerations. The constant development of the technology is improving the resolution of the systems, and reducing the fabrication costs, enabling a wider use of this technology. This reduction of costs is leading to an integration of this technology in a wider range of electronic equipment, to improve its performance or features.

MEMS inertial sensors technology is not exclusive of powerful companies that develop state of the art and costly electronic for use in military or aerospace applications. This technology is mostly used in automotive applications, where they are integrated in safety systems like airbags, stability systems or suspension. The constant feature size reduction, associated with a less or more effective cost, opens a wide range of applications. Biomedical use, consumer application, industrial application, navigation systems, seismography and earthquake prevention are a few areas that the sensors are now being used.

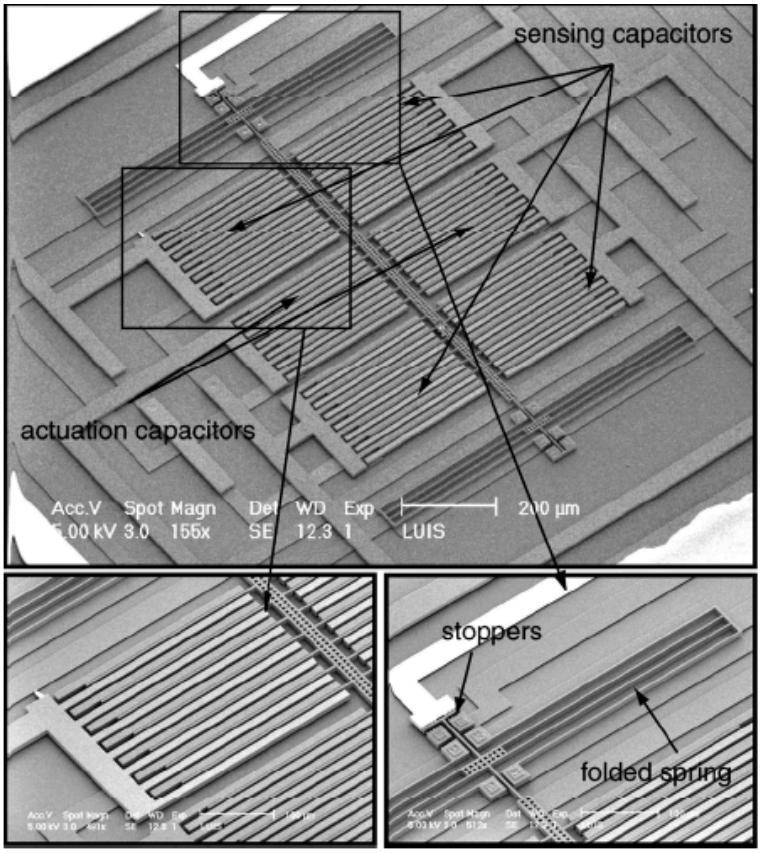


Figure 2 - Capacitive Accelerometer (reproduced from [2])

In this project we will discuss in particular MEMS. In figure 2, a capacitive accelerometer is shown.

In table 1 we have some of the applications where MEMS accelerometers are used.

Table 1 - Use of MEMS Accelerometers [3]

Measurement	Application
Acceleration	Front and side airbag crash sensing Electrically controlled car suspension Safety belt pretensioning Vehicle and traction control systems Inertial measurement, object positioning, and navigation Human activity for pacemaker control
Vibration	Engine management Condition-based maintenance of engines and machinery Security devices Shock and impact monitoring Monitoring of seismic activity
Angles of inclination	Inclinometers and tilt sensing Vehicle stability and roll Headlight leveling Computer peripherals (e.g., joystick, head mounted displays) Handwriting recognition (e.g., SmartQuill from British Telecom plc) Bridges, ramps, and construction

All accelerometers have the same basic mechanical equivalent model. This model is based on a proof mass that is suspended by a spring and a damper that are attached to a fixed frame. The next figure shows that model. When an external acceleration is applied to the system described, the proof mass is dislocated by x from its initial equilibrium point. This dislocation makes the spring distend and also forces the damper to oppose to this movement, until an equilibrium between the forces is reached. By measuring the dislocation of the proof mass, in a certain period of time, it is possible to measure the acceleration applied to the system.

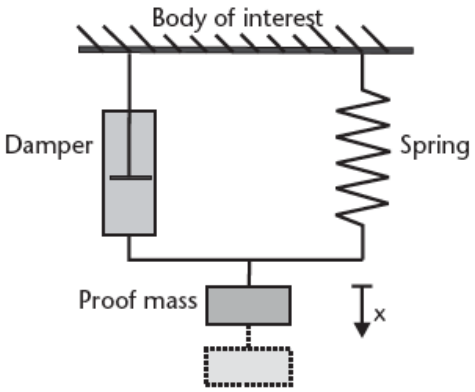


Figure 3 - Mechanical Model of an Accelerometer (reproduced from [4])

Like any other system, the accelerometer has a set of figures of merit that can be defined as:

- Sensitivity
- Frequency Response
- Operation Range
- Resolution

The operation range and bandwidth, for example, varies with the purpose of the application. For automotive airbag system, the operation range is about ±50g (g stands for gravity acceleration) and a bandwidth of 1KHz. In the case of devices that measure engine vibrations they require a range of 1g, but must resolve small accelerations (<100μg) over a bandwidth higher than 10KHz [3].

The next table presents some of the specifications of accelerators used in different applications.

Table 2 - Specification of a few Inertial Accelerometer Systems [4]

Application	Bandwidth	Resolution	Dynamic Range
Automotive Airbag Release	0-0.5 KHz	<0.5mg	±100g
Inertial Navigation	0-100Hz	<5μg	±1g
Medical Applications	0-100Hz	<10mg	±100g
Shipping of fragile goods	0-1KHz	<100mg	±1kg
Virtual Reality(head-mounted displays and data gloves)	0-100Hz	<1mg	±10g

2.1.1 – MEMS Capacitive Accelerometer model

There are many types of sensing mechanisms such as capacitive and piezoresistive. In this project a capacitive accelerometer is used. The main advantages of measuring the mass displacement with a capacitive circuit instead of a piezoresistive circuit are [4]:

- Large output signal
- Good steady state response
- Better sensitivity due to low noise performance

As with all designs, the capacitive accelerometer has its drawbacks, being the most important the susceptibility to electromagnetic interference (EMI), since their sense node is high impedance. This problem can be solved with the use of a proper packaging and shielding, making these interferences insignificant.

The next figure presents a model for a capacitive accelerometer. The tethers, as it can be seen in figure 4a, are holding the proof mass (the proof mass (M) is only connected by the tethers), acting as spring (K) in figure 4b, and the air surrounding the tethers acts as the dumper (D). The electrode and proof mass fingers act as the two parallel plates of a capacitor, and the air between them acts as the dielectric. When there is a movement between these 2 structures, the air space (dielectric) between them suffers variation, increasing or decreasing, according to the direction of the acceleration. The movement of the proof mass is also proportional to the acceleration felt by the accelerometer; the more intense the acceleration, the bigger the proof mass dislocation. Combining these last two features it is possible to measure the acceleration as follows. By measuring the variation in the capacitance, that is proportional to the acceleration, and further converting this capacitance variation into voltage variation, the acceleration value can be found. Normally, an accelerometer has more than one pair of tether/electrode, which improves the precision of the system.

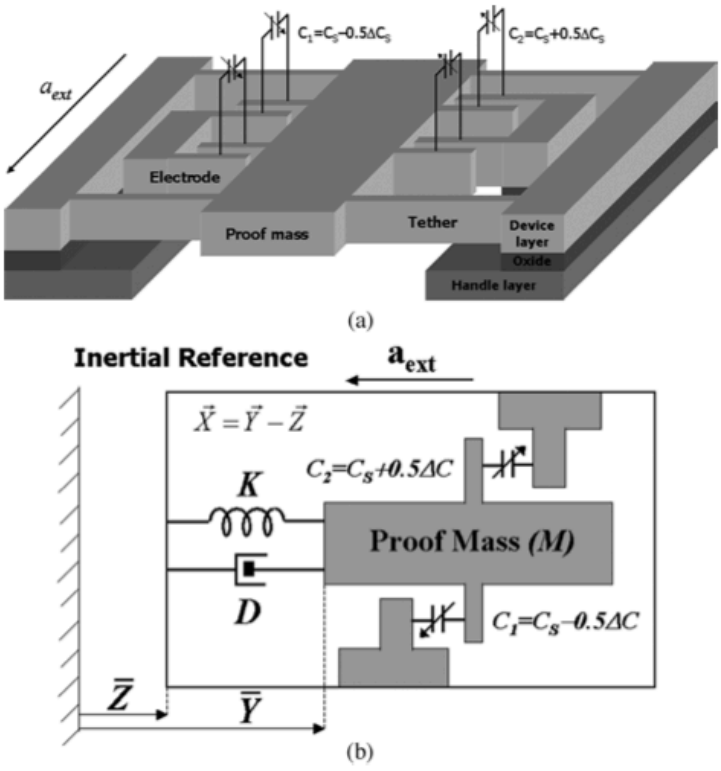


Figure 4 - (a) Schematic of a differential capacitive accelerometer. (b) Lumped elements model of the accelerometer (reproduced from [5])

2.2 - MEMS Capacitive Accelerometer [6]

The MEMS Capacitive Accelerometer used in this dissertation is presented in [6]. It has a different approach concerning acceleration detection from previous developed capacitive accelerometers. It includes time sensing instead of the normal capacity displacement sensing. This new approach has low noise and low requirements for the capacity sensing circuit; on the other hand, it will have a more complex and low bandwidth system.

To have a general idea of the operation of this accelerometer, a block diagram is presented in figure 5.

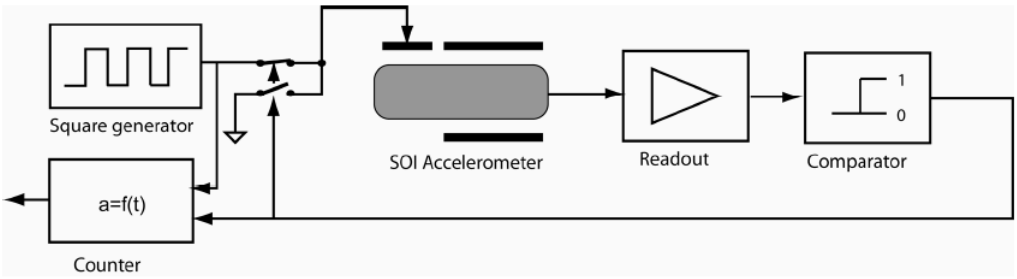


Figure 5 - Microaccelerometer block diagram (reproduced from [6])

The main block is the Silicon On Insulator (SOI) accelerometer with a separate sensing and actuation electrode. A square wave generator actuates the accelerometer. The period of the signal must be larger than the nominal pull-in-time in order to measure the full transition pull-in-time. The changes in capacity are converted to changes in voltage through the readout block. After, the signal is fed to a comparator that, as soon as the threshold is reached, the time measurement is stopped and grounded, to prevent the accelerometer movable electrode to reach the counter electrode. At the end, the counter will measure the pull-in-time. The changes of the pull-in-time are proportional to the external acceleration sensed by the accelerometer. The schematic of the accelerometer structure and a photo of a SOI accelerometer are presented in figures 6 and 7.

After simulating the accelerator model, it was possible to have some results of the accelerometer performance. The sensitivity of the accelerometer is 2.6us/ug and has a nominal pull in time of 34.5ms.

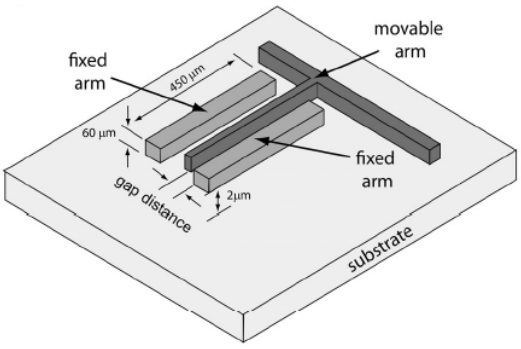


Figure 6 - Schematic of the accelerometer structure (reproduced from [6])

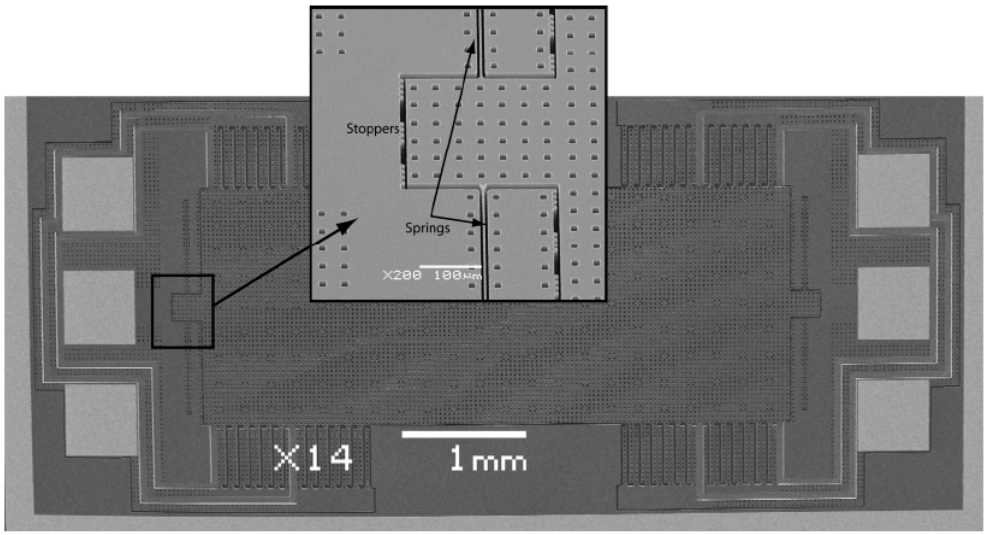


Figure 7 - SOI fabricated microaccelerometer (reproduced from [6])

A model of the physical MEMS capacitive accelerometer was used in the development of this project (refer to Figure 8), to simulate its behaviour. As it can be seen, the output of the system is differential. Observing the circuit, it can be seen the MEMS Capacitors (C+dC and C-dC) and a reference capacitor (Cr1 and Cr2). These reference capacitors are not part of the accelerometer and have the same value. The dC represents the capacitor value variation due to the acceleration. We can calculate the output voltage Vo of the two branches separately, and then of the entire circuit.

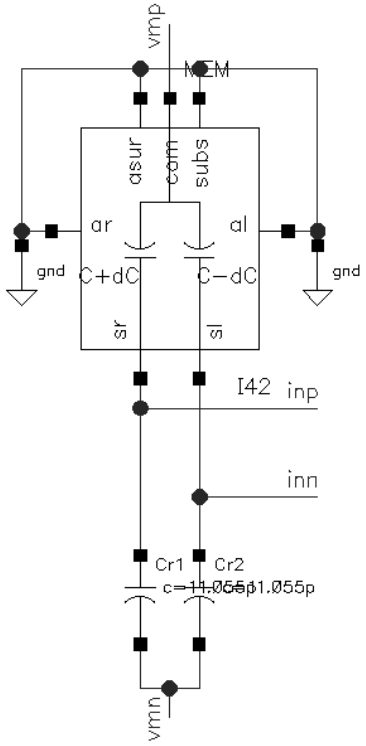


Figure 8 - Electric model of the MEMS capacitive accelerometer

We have V_{mp} (V_{m+}) and V_{mn} (V_{m-}). We know, by the Thevenin equivalent that, in the left branch:

and that:

$$V_{o2} = \frac{C_{1p}}{C + dC + C_r} * (-Vm)$$

leading to:

$$V_{Th} = V_{o1} + V_{o2} = \frac{C + dC - C_r}{C + dC + C_r} * Vm$$

In the right branch we have:

$$V_{o1} = \frac{C - dC}{C - dC + C_r} * (+Vm)$$

and,

$$V_{o2} = \frac{C_{1p}}{C - dC + C_r} * (-Vm)$$

leading to:

$$V_{Th} = V_{o1} + V_{o2} = \frac{C - dC - C_r}{C - dC + C_r} * Vm .$$

These are the range of tensions that the MEMS Capacitive Accelerometer will have in the output and that the Fully Differential SC Amplifier will receive at its input.

2.3 – Readout Chain

In this section the readout chain after a MEMS accelerometer will be presented. The chain is normally composed by an Amplifier and after by an analogue to digital converter (see figure 1). The choice of the topology will be explained subsequently.

2.3.1 – Amplifier

The amplifier is the first block of the readout chain. Due to the fact that the accelerometer output is differential, the input of the amplifier will also be differential. The amplifier has a differential input/output topology. Fully differential amplifiers are repeatedly used in integrated circuits instead of the single ended circuits. The improved immunity to power supply noise, greater output voltage swing, better linearity, are the main reasons to favour this type of amplifier in many applications.

The architecture of a fully differential amplifier is similar to a standard voltage amplifier. The difference between these topologies is shown in Figure 9. The fully differential amplifier has a differential input that leads to a differential output. It is not the case of a standard architecture amplifier, as it has the differential input, but the output is single ended. Also another difference is the output common mode voltage (VOCM) that can be

controlled independently in a fully differential amplifier. The VOCM input controls that value. In a standard amplifier, with single ended output, the signal and the output common mode voltage are the same.

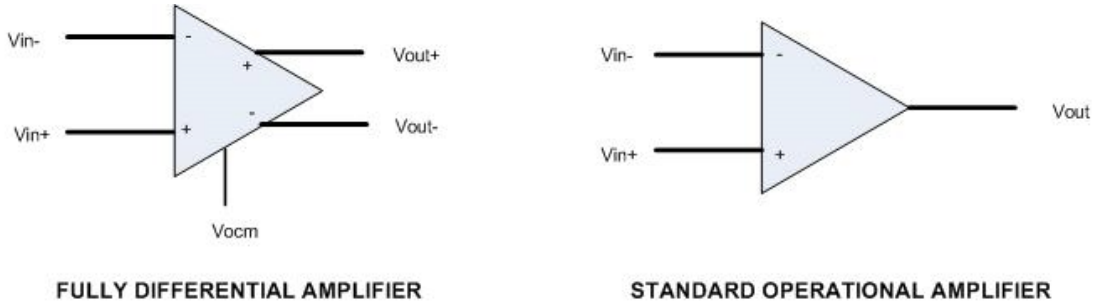


Figure 9 - Differences between Fully Differential Amplifier and Standard Operational Amplifier

2.3.1.1 - Switch Capacitor Amplifier

Nowadays, the interest in fabricating low power consuming and low supply voltage ICs has grown. The main purpose for this development interest is the integration of this ICs in portable equipment, where the use of batteries is mandatory. Also, due to the integration of more complex systems in the same physical space than before, drives the necessity to have low voltage and low power ICs.

The switched capacitor techniques are very easy to implement in CMOS technology, as its structure is composed by capacitors, switches and Op-Amps. Also, these techniques can be used in low power and low supply voltage circuits, as capacitors are not strongly affected by supply voltage reductions [7]. These techniques can also replace the use of resistors in circuits, component that in CMOS technologies waste a quite significant amount of space. A capacitor switched between two nodes in a circuit, at a sufficiently high rate, is equivalent to a resistor connecting the same nodes [8]. Figure 10 shows a switched capacitor amplifier model.

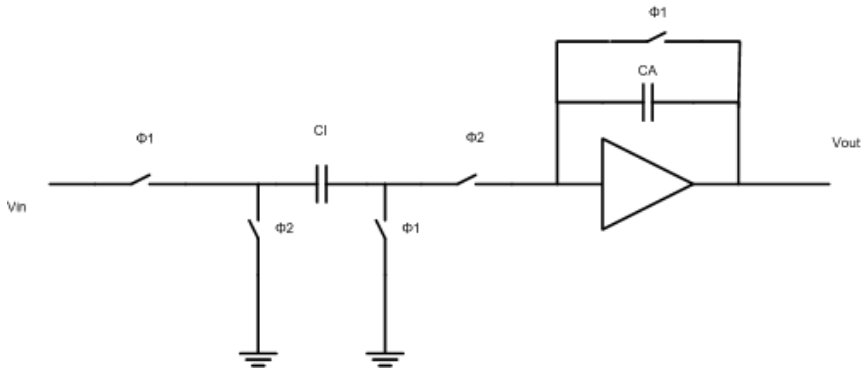


Figure 10 - Switched Capacitor Amplifier Model

2.3.1.2 - CDS and CHS as noise reduction techniques [9]

Operational amplifiers are normally affected by non-ideal effects. The effects can be 1/f noise, thermal noise, nonlinearity or input referred dc offset. These imperfections affect the purity of the input signal and, as a result, the output of the signal. In order to improve Op-Amp efficiency, by reducing these signals imperfections, two techniques are presented. These techniques were used in this project. Their integration can be applied normally to building blocks such as voltage amplifiers, ADCs and DACs, sample and hold (S&H) circuits and comparators. They are perfect for our current application, a fully differential SC charge Amplifier and Sigma Delta Modulator. The techniques are the Correlated Double Sampling (CDS), being a sampling technique, and Chopper Stabilization (CHS), a modulation technique. We then compare both techniques and choose the most suitable for our specific application.

The Correlated Double Sampling is in fact a particular case of the auto-zeroing technique, where the amplifier noise and offset is sampled twice in each clock phase. The amplifier needs to be disconnected in phase 1 (refer to Figure 11), so that the capacitor C_{cds} stores its offset and noise. In the next phase, the sampled value will be available to be amplified. The amplifier can be auto-zeroed while the voltages are stored in the capacitor and then connected back again in the following phase. After the auto-zeroing phase, the output is sampled by the next stage. In our case these stages are the SC charge amplifier and SC integrator.

A model of an SC amplifier with CDS is presented in figure 11. The noise and offset of the amplifier are sampled when Φ1 is high. Also the value of the input is sampled during this phase. The noise and offset are then subtracted to the input sample, when Φ2 is high, and then integrated.

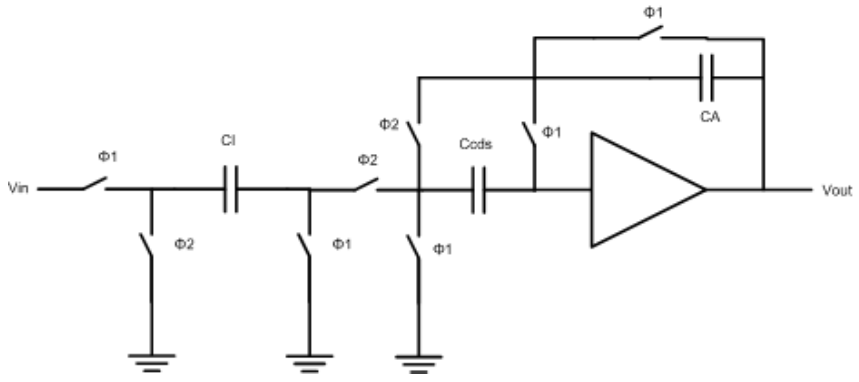


Figure 11 - Switched Capacity Amplifier model with CDS

The Chopper Stabilization is based on a modulation technique. The frequency of the input is converted to a higher range, so that the 1/f noise has no influence on the signal and then it suffers a demodulation to take the frequency back to the baseband after demodulation. The principle is shown in the next figure.

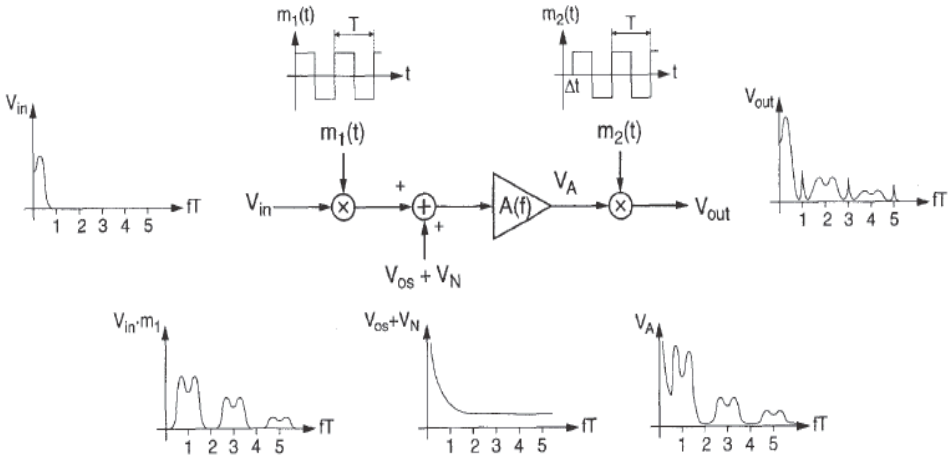


Figure 12 - Chopper Stabilization Principle (reproduced from [9])

If we have an input signal, with a spectrum limited to half of the chopper frequency, no signal aliasing occurs. For the analysis, the amplifier is considered ideal, meaning no noise or offset, these non-ideal effects are actually posted outside as an independent signal $V_{os}+V_N$, as seen in figure 12, for sake of analysis. The input signal will be multiplied by m1(t), a square-wave carrier signal with period T=1/Fchop. After this modulation, the signal will be transposed to the odd harmonic frequencies of the modulation signal (which is as square wave in this example). Subsequently, it suffers an amplification and demodulation back to the original band, which pushes the noise present in the signal to higher frequencies. If we assume that we have a dc input signal Vin in the chopper amplifier, we will have at the output a square wave signal with amplitude Vin. Assuming that the amplifier has a Gain A_O, infinite bandwidth and does not introduce any delay, the output after demodulation will be a dc signal of a value equal to $A_O V_{IN}$ [9].

After the presentation of both techniques to reduce Op-Amp imperfections, we will present a comparison between these two techniques [9]:

- CDS is a sampled-data method, while CHS is a modulation-based method and it can be used for continuous time signals.
- CDS reduces the low-frequency noise by doing high-pass filtering, while CHS translates the noise to some out-of-band frequency, without really filtering it.
- The output noise of a CDS stage is normally dominated by an undersampled wideband noise; in a continuous time CHS stage the noise spectrum is not folded, and hence 1/f noise remains dominant in the baseband before the down conversion, which will interchange the noises, pushing 1/f to higher frequencies and putting the thermal noise in the baseband. The chopping frequency needs to be much larger than the

flicker noise corner frequency, then the baseband white noise in the output is only slightly larger than it was without CHS (as referred in[9]).

- CDS can improve the effective gain of the Op-Amps used in signal processing. In contrast, CHS systems cause the Op-Amp to amplify higher frequency signals, where it normally have a reduced effective gain.

These characteristics will make CDS a better technique to use in our project. It is a technique used preferably in sampled-data circuits, like our SC Amplifier and in our Sigma Delta Modulator, where the baseband noise behaviour is not worst due to noise aliasing. In addition, this will eliminate dc (direct current) offsets, not just modulating it to higher frequency. This may improve the allowable signal swing, in contrast with CHS. To finish, an advantage of CDS may be the ability to improve the gain of the circuit. Taking into account these reasons, we conclude that the best technique to reduce Op-Amps imperfections is the Correlated Double Sampling.

2.3.2 – ADC

The analogue to digital conversion is a very important feature in electronics. The signals we have in the real world are analogue, like temperature changes in a system, position changes and, in our case, acceleration variation. The advantages of converting these analogue measurements into digital are, mostly, the flexibility, robustness and reliability of the digital signal. The signal can be transmitted and manipulated easily, without loss of the information content. In this accelerometer, the ADC will receive the amplified signal from the fully differential SC charge amplifier and it will convert the signal to digital, for further processing.

2.3.2.1 - Analogue-Digital Converter Types

When we refer to an ADC, two characteristics are important, speed and resolution. These characteristics are taken into account when deciding which type of ADC is the most suitable for the application. There are 4 main common types of ADC architectures available with different characteristics:

- Flash type ADC
- Pipeline ADC
- Successive Approximations ADC
- Oversampled ADC

These architectures will be discussed and explanations will be given supporting the use Sigma Delta ADC architecture in this project.

The Flash ADC architecture uses the distributed sampling to achieve a high conversion speed. This ADC type will provide a high speed and simple architecture. They are ideal for applications demanding a very large bandwidth. Nevertheless, they consume more power than any other ADC architecture. The next figure presents the architecture for a Flash ADC. As can be observed, the architecture is very simple, but for high resolutions the complexity rises significantly. An n bit converter requires 2^{n-1} comparators. This will increase its complexity, power consumption, size and consequently its fabrication costs, according to n. These ADCs are normally limited to a top 8 bits resolution. Also the large number of comparators will raise problems such as dc and ac deviation of the reference voltages generated by the ladder, large nonlinear input capacitance, and noise at the analogue input [11].

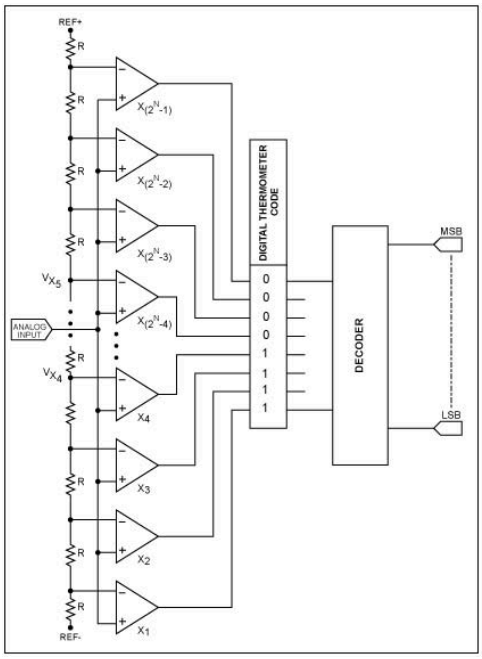


Figure 13 - Flash ADC Architecture (reproduced from [10])

The pipeline ADCs became one of the most popular architectures for sampling rates from few megasamples per second (MSPS) up to 100 MSPS+ [12]. In these ADCs (refer to figure 14), each stage carries out an operation in each sample, providing an input for the following sampler, and after the next stage has received this sample, it begins preparing the next one. Every stage incorporates a S&H circuit, so that the analogue data can be preserved, allowing each stage to process different samples concurrently. Therefore, the conversion rate only depends on one stage, normally the front-end stage.

The main advantage of pipeline ADCs is that, after an initial delay of N clock cycles, one conversion will be available per clock cycle, making it a high throughput ADC. On the

other end, this delay of some clock cycles is a disadvantage. If an error occurs in the first stages, it will be propagated through the converter and the final result will have a much higher error rate.

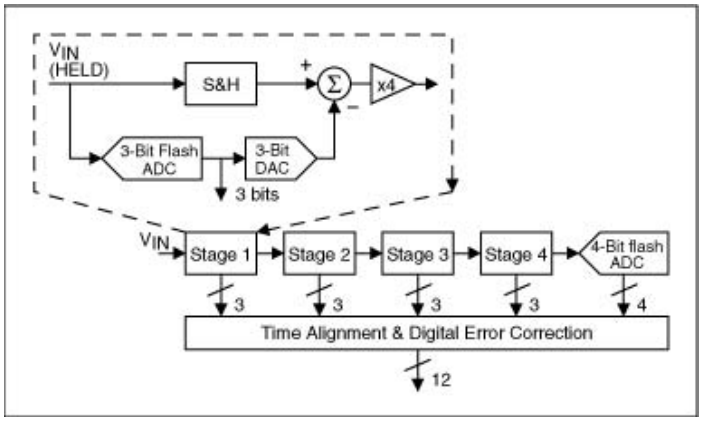


Figure 14 - Pipeline ADC with 3 stages (reproduced from [12])

The Successive Approximations architecture is frequently used in medium-to-high resolution applications with sample rates of 5 MSPS. Due to its resolution range between 8 to 16 bits and its low power consumption, this ADC is used in a wide range of applications, such as portable/battery powered instruments, pen digitizers, industrial controls, etc.

This ADC architecture converts through a binary search algorithm. The register, called successive approximation register, tries all values of bits, starting from the most significant bit (half of the converter range) to the least significant bit, in a successive form. During this process, the register checks the comparator output to see if the binary count is greater or equal to the input analogue signal, adjusting the values accordingly [13]. The advantage of this counting method is the low consumption, high resolution and accuracy. These characteristics enable this type of architecture to be integrated with larger or more complex circuits. On the other hand, its low sampling rate is a disadvantage, along with the requirements for its building blocks, which need to be as accurate as the overall system [14].

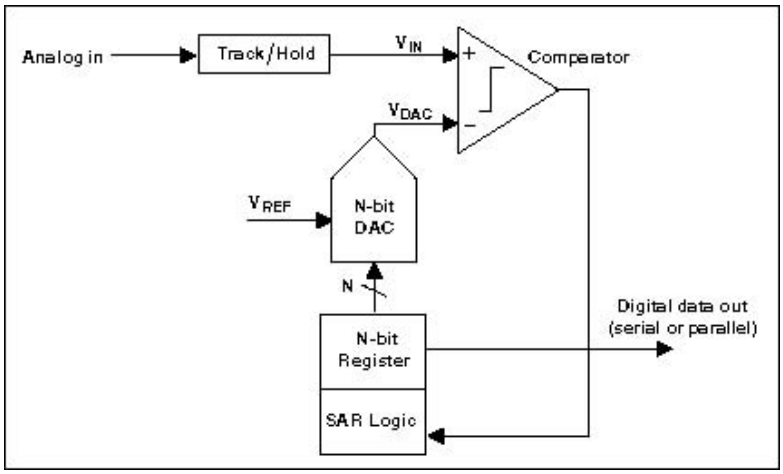


Figure 15 - N-Bit Successive Approximations ADC (reproduced from [14])

Sigma-Delta ADCs were presented in the 60s, but only in the 80s, with the increase of development in the area of silicon technology, it became widespread and used for many purposes. This type of converters offer high resolution, high integration and low cost fabrication, enabling them to be ideal for applications such as process control, weighting scales, inertial sensors, etc. More details on its structure and functioning will be discussed below.

2.3.2.2 - Why Sigma Delta

The choice of a sigma delta ADC was made due to the easy implementation of this type of ADC in an IC and its high resolution. This type of ADC has been known for many years but only now the technology can provide low cost Integration. Sigma Delta ADCs are used in applications where the main requirements are low cost, low bandwidth, low power and high resolution.

In the next figure, a comparison between 4 types A/D techniques is shown.

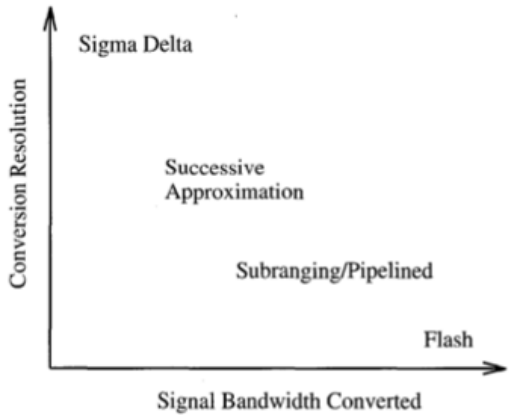


Figure 16 - Bandwidth Resolution Tradeoffs (reproduced from [15])

Figure 16 shows the difference between these ADC techniques regarding bandwidth and resolution. The Sigma Delta ADC is the one that has higher conversion resolution for low signal bandwidth. They are mostly used in applications that demand a very high resolution in data conversion with a low signal bandwidth, like speech applications where the signal bandwidth is low, approximately 4 KHz, but where the resolution needs to be high, typically 14 bits. Also in audio applications, where the bandwidth needed is approximately 20-24 KHz and the resolution, in high fidelity audio applications, is 16-18 bits or higher. Opposite to the Sigma Delta ADCs, the Flash ADCs are mostly used in applications that require a high bandwidth, but low resolution, such as broadcast video applications.

Table 3 presents some more characteristics of different types of conversions.

Table 3 - Comparison between various ADC techniques. N stands for resolution and f_{CLK} for clock frequency [16]

A/D Converter Technique	Maximum Resolution (bit)	Conversion Time	Suitable for Microsensors
Nyquist Rate ADC			
Flash ADC	6	$1/f_{clk}$	-
Subranging and Pipeline ADC	12	$<N/f_{clk}$	=
Folding ADC	10	$<N/f_{clk}$	-
Successive Approximation ADC	12	N/f_{clk}	=
Algorithmic ADC	12	N/f_{clk}	=
Oversampled ADC			
Dual Slope ADC	20	$2^{N+1}/f_{clk}$	+
Incremental ADC	>16	$2^{N}/f_{clk}$	++
ΣΔ ADC	>18	$<2^{N}/f_{clk}$	++

The data in the table 3 shows that Sigma Delta ADCs are the most suitable for our purpose, an ADC for our MEMS Accelerometer, due to its high resolution. They are also more suitable for use with microsensors due to its low cost integration.

2.3.2.3 - Structure of the Sigma Delta ADC

The block diagram of a 1st order Sigma Delta ADC is presented below. It is divided in two parts: the first order ΣΔ modulator and the Digital Decimator.

An integrator, a quantizer (1-bit ADC) and a negative feedback DAC makes the Sigma Delta modulator. A dc signal at the input (Vin) passes through the integrator and the quantizer. The output of the quantizer is fed back to the input by a negative 1-bit DAC. This loop will force the average dc voltage at the output of the 1-bit DAC to be equal to Vin. As

the input voltage increases, and becomes more similar to $+V_{REF}$, the quantizer output exhibits more 1s and less 0s. In the other hand, when the voltage decreases to $-V_{REF}$, the number of zeros increases and the number of 1 decreases. In the end, the digital decimator, composed by a low pass filter and a down-sampler, will process the signal and produce the final output.

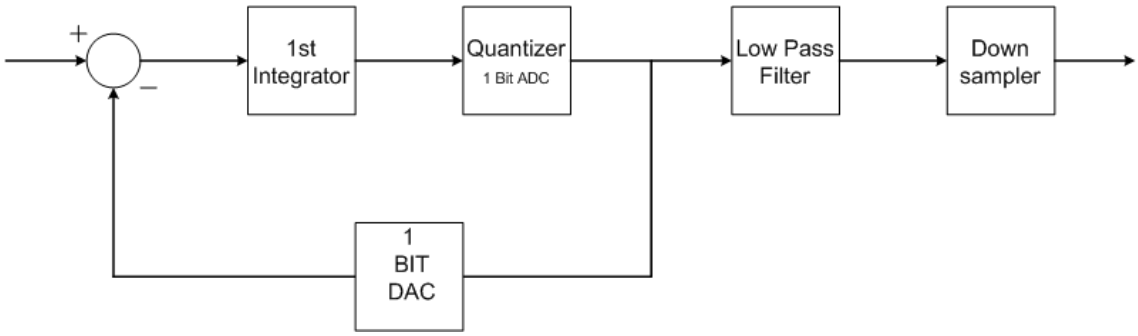


Figure 17 - First Order Sigma Delta ADC

A second order Sigma Delta ADC provides a higher resolution and a better noise-shaping characteristic while being robust in terms of loop stability. The block diagram of a second order Sigma Delta ADC only varies with the increment of another Integrator and a feedback gain (C and K), specific for the 1st and 2nd modulator. The block diagram of a 2nd order Sigma Delta ADC is presented in the next figure.

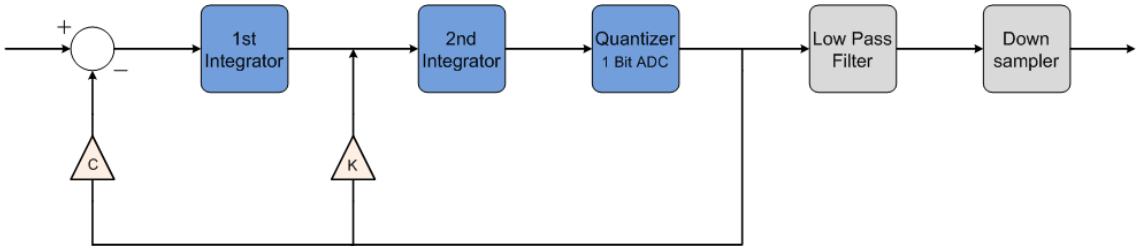


Figure 18 - Second Order Sigma Delta ADC

For understanding the sigma delta ADC completely, an explanation of some concepts, such as signal sampling and decimation, will be made, as well as a more detailed explanation of the block diagram.

The analogue signal at the input passes through an integrator. The signal will be sampled here. The signal sampling is the transformation of a continuous time signal to a discrete time signal. This sampling is made according to the sampling theorem. It guarantees that the sampled signal can be recovered without distortion, and states that the sampling frequency must be equal or higher than two times the signal frequency. When sampling occurs, the signal spectrum is copied and mirrored at multiples of the sampling frequency. If the sampling frequency is not equal or higher than two times the signal frequency, aliasing

can occur and the signal will suffer a distortion. Figure 19 presents a sampled signal spectrum where aliasing occurs (continuous signal), due to the fact that the sampling frequency was lower than two times the signal frequency (undersampling).

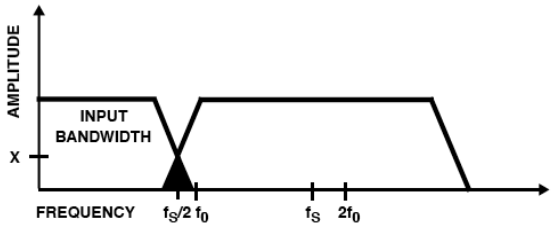


Figure 19 - Undersampled Signal Spectrum (reproduced from [17])

In figure 20, the opposite occurs. The sampling frequency is equal or greater than two times the signal frequency (oversampling). Aliasing does not occur in this case.

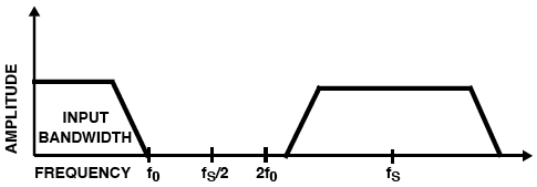


Figure 20 - Oversampled Signal Spectrum (reproduced from [17])

After the signal being sampled, it needs to be quantized. The quantizer will give a digital value to each of the samples that it receives from its input. This quantization normally will add some noise to the signal. One of the main concerns in converters is to avoid this noise. The quantizer introduces noise in the system, called Quantization noise. For an easier understanding, an example will be presented (refer to [17]). Assume a 2-bit ADC with a 3 V full-scale value. As we have 2-bit resolution (00,01,10,11) we can divide the 3 V scale into 4 steps, 0V, 1V, 2V and 3V respectively. If at the input, a signal of 1.75V appears, at the output of the ADC will appear a 10, which converted to voltage corresponds to a 2V signal. The difference between the output signal (2V) and the input signal (1.75V) is the quantization noise (0.25V).

After that, the discrete time signal will pass through the Digital Decimator. It is composed by a low-pass filter and a down-sampler. The signal, at the input of the digital decimator, is oversampled. Oversampling spreads quantizing noise over a bandwidth larger than the signal band, meaning that it is pushing this noise to higher frequencies. The sigma-delta filtering serves to high-pass this noise, still in the analogue amplitude domain, decreasing even further its power in the signal band. In the digital side, the high frequency noise that remains is filtered by a low pass filter (LPF). It filters the quantizing noise that is

already in high frequencies. After the low-pass filter, we have the down-sampler. The sampling theorem states that the sampling frequency should be, at least, two times the signal frequency so that the signal can be reconstructed without distortion. But, as it was also said before, the signal suffers an oversampling to push the quantization noise to higher frequencies. This will produce lots of redundant data. This data can be eliminated by the down-sampler, without introducing distortion to the output. The focus of this dissertation is however, on the sigma-delta modulator part of the ADC.

2.4 Summary

This chapter presented the background of the main themes of this dissertation. The accelerometer used is a MEMS Capacitive Accelerometer. The development of a fully differential SC charge amplifier enabled us to amplify the signal from the accelerometer and send it to the ADC. With the fully differential architecture, the common mode interferences are reduced and by integrating a CDS topology, the low frequency noise is cancelled as well as the offset. The modulator used is a Sigma Delta, a modulation perfect for SC topologies with high resolution and easy integration. The ADC has also a CDS circuit in order to cancel offset and low frequency noise.

Chapter 3

State of Art – MEMS Readout Chain

3.1 Fully Differential Charge Amplifiers

The first part of this project is to develop a fully differential charge amplifier in order to amplify the small variation of signal coming from the accelerometer. In order to start developing the charge amplifier, an extensive search was made with the goal of discovering similar projects, or projects with useful information. In this section, some of these important projects are presented.

3.1.1 - A MEMS capacitive accelerometer system, with a SC charge amplifier and a 1st order Sigma-Delta ADC [5]

An important feature looked for in similar projects, was the integration of a fully differential amplifier with an inertial sensor. The first project presented in this section is very similar the one developed in this dissertation. A MEMS capacitive accelerometer system, with a SC charge amplifier and a 1st order Sigma-Delta ADC [5]. The front-end block (refer to figure 21) of this project is presented here, while the back end block is presented in the following section. The front-end block is composed by a SC charge amplifier and a sample and hold circuit (S&H).

In case of acceleration, the proof mass will move, making a capacity change in the capacitive bridge. This change will be converted to voltage and will be amplified by the SC charge amplifier. Figure 22 presents the schematic for the MEMS circuit and the front-end block.

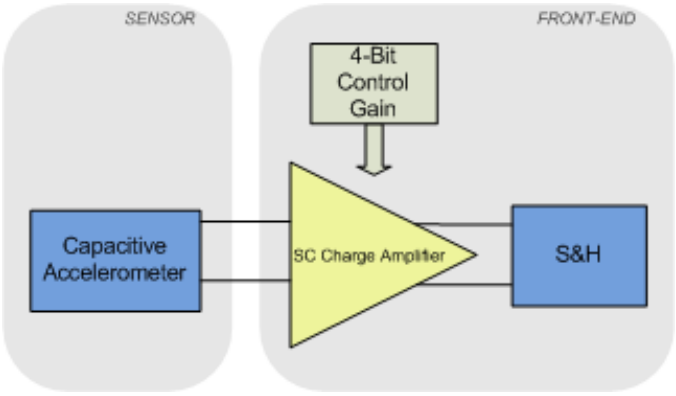


Figure 21 - Sensor and Front End Block Diagram

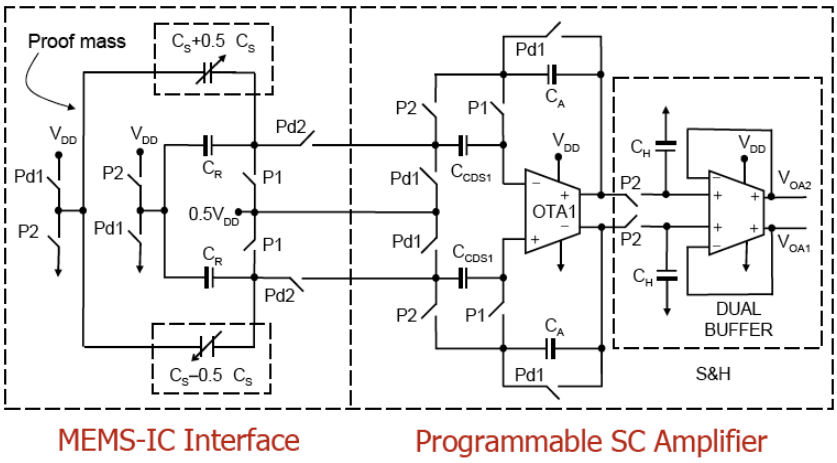


Figure 22 - MEMS-IC and Front End Block Schematic (reproduced from [5])

The amplifier has a fully differential topology. The changes in the capacity of $C_S \pm \Delta C_S$ will be amplified by the SC amplifier and then converted in a digital output by the back end block. The amplification capacitors C_A and reference capacitors C_R can be set by an 8-bit digital word, to allow the gain to be programmable. There are 2 clock phases, P1 and P2. The sampling phase P1 charges de capacitors C_S and C_R with $V_{DD}/2$. The correlated Double Sampling capacitors will save the offset and the low-frequency noise. When p2 is high, amplification phase, the charge stored in capacitors C_S and C_R will be transmitted to the amplification capacitor C_A, and C_{CDS} will cancel the offset and low frequency noise. The S&H circuit will act as an impulse sampler, which will interpolate the sample data and provide a smooth signal at its output. This amplifier has low noise, low power consumption and high accuracy. The schematic of this circuit divided by the two clock phases is presented in figure 23.

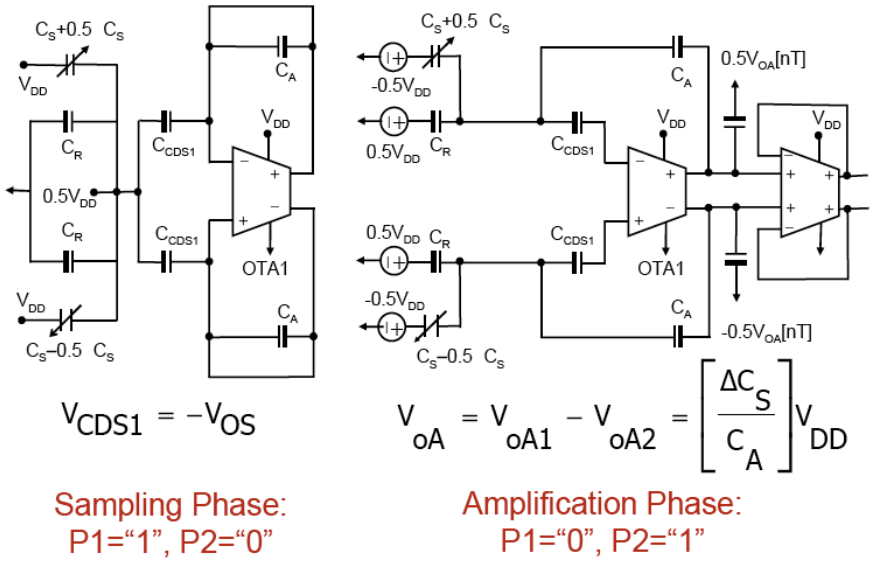


Figure 23 - Sampling Phase and Amplifying Phase (reproduced from [5])

3.1.2 - Fully differential Op_Amp for use as a readout chain of a Accelerometer [18]

Another useful project for the guidance of this dissertation is presented in [18]. Unlike the previous project, that a complete system for the MEMS accelerometer was developed, in the project presented below only the fully differential Op-Amp is developed. This Op-Amp is suitable for use in very low voltage SC circuits in CMOS technology MEMS accelerometers. It has two stages, where CMFB (Common Mode Feedback) is only required for the second stage. The CMFB is implemented using bootstrapped switches, in order to reduce supply voltage.

Figure 24 shows a fully differential integrator using bootstrapped switches where the fully differential Op-Amp can be used.

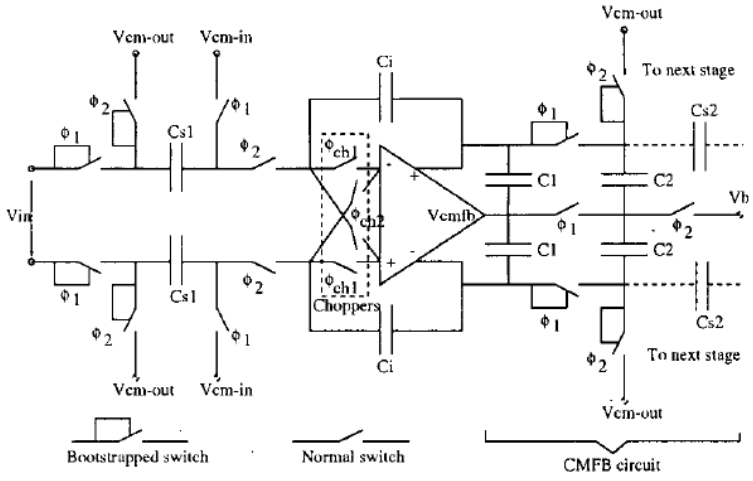


Figure 24 - Fully Differential Charge amplifier (reproduced from [18])

This Op-Amp has a differential architecture, meaning that both input and output are differentials. In order to regulate the common mode output voltage, a CMFB has to be implemented. The next figure shows the fully differential Op-Amp schematic.

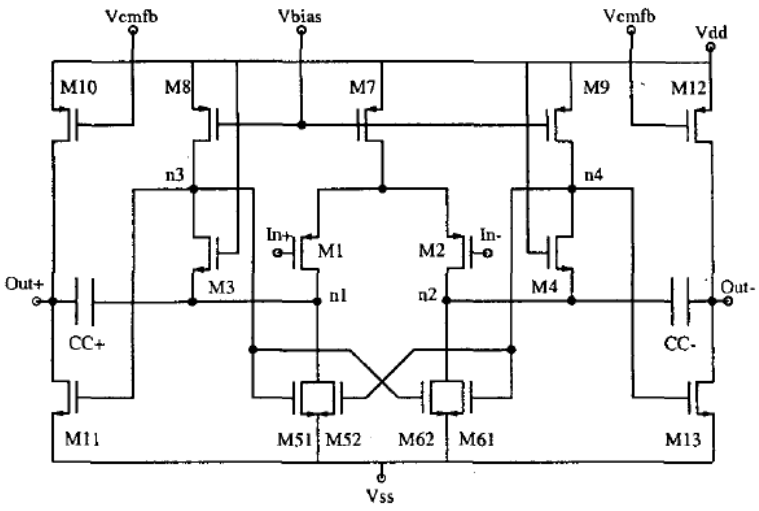


Figure 25 - Fully Differential Op-Amp Schematic (reproduced from [18])

The NMOS current source splits its current through the equally sized cross-coupled transistors, M51/M52 and M61/M62, which have their gates connected to the output of the first stage (n3 and n4). This negative feedback causes the differential signal in n3/n4 to have high load impedance. In the second stage there is a common source amplifier, M11/M13 with active load M10/M12.

The compensation scheme, applied in this Op-Amp, was done by connecting two capacitors CC-/CC+ to the source of the cascode devices, nodes n1 and n2. These low impedance points decouple the gate of the output stage amplifier (M11/M13) from the compensation capacitor. This scheme improves the power-supply rejection rate (PSRR).

One main concern when developing an Op-Amp is the influence of noise. Thermal noise and 1/f noise are very common in these circuits. To reduce thermal noise in this Op-Amp, a higher input current is inserted in the differential pair M1 and M2 (refer to figure 25). 1/f noise can be reduced by increasing the size of the transistors that contribute for it (M1, M2, M5, M6, M8, M9, referring to 24). Nevertheless, by reducing 1/f noise, the circuit size gets bigger and also its fabrication cost. In order to reduce noise of this circuit, without increasing its size or input currents, CHS technique can be used. The input is chopped using four input n-switches. This scheme is shown in figure 24. The output of the first stage is chopped as shown in figure 26. Only two more elements were added to the circuit, preventing a growth of the circuit's size. The elements added were 2 cascode transistor, M32 and M42, in parallel to transistor M31 and M42. The sources of these transistors are connected

to node 1 and 2, consecutively. The gates of these added transistors are connected to the two clock phases used by CHS. The clock phase's frequency is half of the sampling frequency. This arrangement will reduce 1/f noise for all transistors except M8/M9, where a larger transistor length must be used.

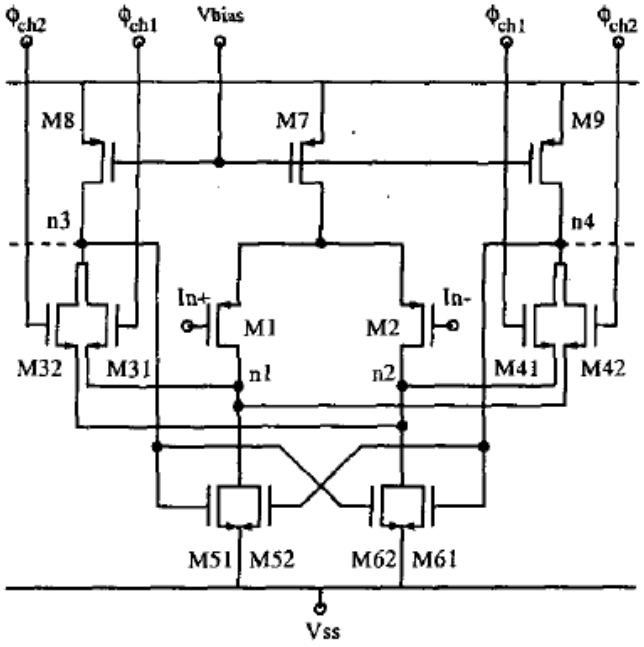


Figure 26 - CHS Schematic (reproduced from [18])

Tests were made to this schematic and the dc gain was 63 dB. Its dynamic range is 88dB [18].

3.1.3 – Fully Fifferential Charge Amplifier with CHS [19]

This dissertation is part of a project currently under development. The main goal is to develop the complete system for a high resolution MEMS Accelerometer. As previously stated, the MEMS Accelerometer was already built in [6]. There was also a Fully Differential Charge Amplifier developed, by Américo Dias, in [19]. This dissertation, aims to improve this amplifier, by switching from CHS to CDS technique.

The charge amplifier developed by Américo Dias amplifies the capacitive changes that the MEMS accelerometer is subjected to. The main characteristics that were looked for, in the amplifier, are:

- Low offset
- Good Bandwidth
- Good noise Immunity

The Fully Differential Operational Amplifier, developed in [19], is shown in figure 27. Transistors MP51 and MP52 make the differential input of the Op-Amp. They have an active charge made by MP50. Transistors MP51, MP52, MN2 and MN8 are polarized by transistors MN4 to MN7. They also increase the CMRR. MN2 and MN8 have a common base configuration, having as active charges transistors MP1, MP2, MP9 and MP10. The project developed in [18] is for a 1V operation Op-Amp. Since this project requires a higher voltage, transistors MP2 and MP10 were added to increase the load in the drain of MN2 and MN8, thus increasing the gain. The last stage of the Op-Amp is formed by MN0 and MN9. MP0 and MP11 provide the active load in this stage allowing the common mode voltage (VCM) to change by adjusting the polarizing voltage VCM_{bias} [19].

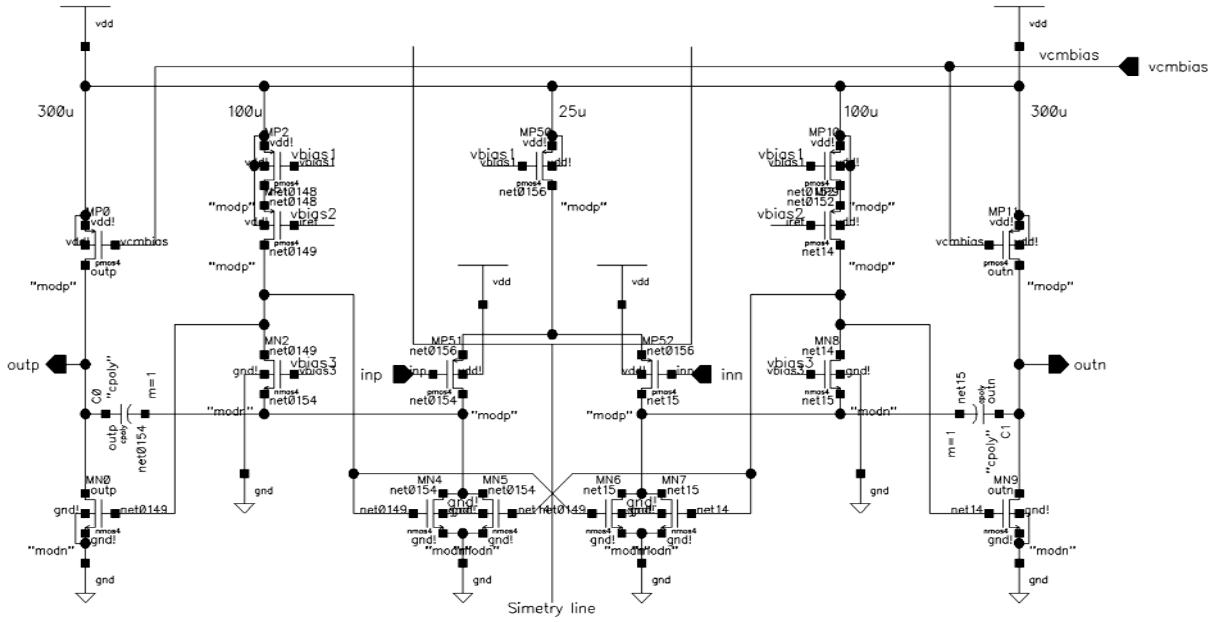


Figure 27 - Fully Differential Op-Amp (reproduced from [19])

After the presentation of the schematic of the Op-Amp, the circuit of the Charge Amplifier, with the electric model of the MEMS Capacitive Accelerometer is shown.

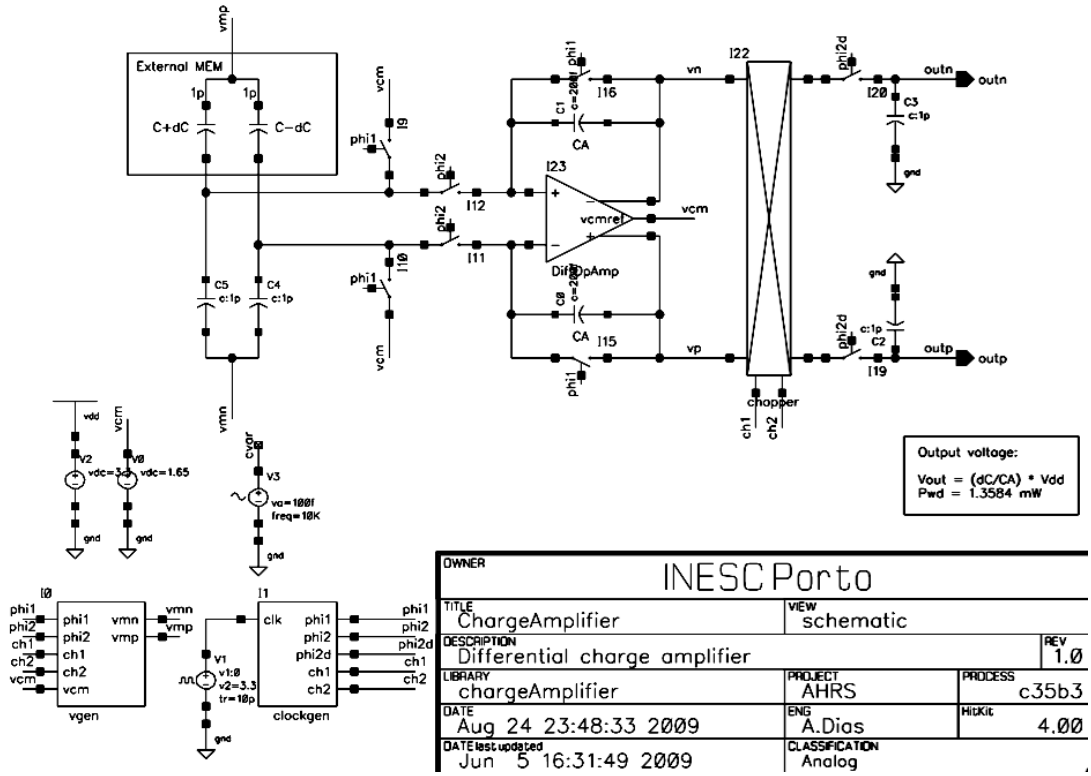


Figure 28 - Charge Amplifier schematic and MEMS Accelerometer electric equivalent circuit (reproduced from [19])

Since we have a differential input and a differential output, the amplifier needs a Common Mode Feedback (CMFB) to regulate the common mode voltage of both stages. This is made by a Switched Capacitor Common mode Feedback.

After the Differential Amplifier, we have a Chopper Stabilization circuit. It is based on a modulation technique. The frequency of the input is converted to a higher range, so that the 1/f noise has no influence on the signal. After that, it suffers a demodulation to take the frequency back to the baseband.

This circuit has two clock phases, phi1 and phi2. When phi1 is high and phi2 is low, the vcm polarizes the MEMS circuit and measures the changes in the capacity and, consequently, in the voltage. In phi2, this change in voltage is going to be amplified by the Fully differential charge amplifier. The amplified voltage will be then transmitted through the differential output.

The gain of the amplifier can be controlled digitally and can be calculated by $V_{OUT} = (\Delta C_1 + \Delta C_2 / C_A) V_{DD}$.

The layout of this Fully Differential Charge Amplifier with CHS has already been made. It was tested thoroughly. The DC gain is 87.58 dB and with a bandwidth of approximately 40 MHz. The Differential Amplifier has a consumption of only 1mW.

3.2 Sigma Delta Modulators for Capacitive Sensors

The second part of this dissertation is to develop a 2nd order Sigma Delta Modulator, in order to convert the analogue output data into digital, making its manipulation and interpretation easier. To gather information of sigma delta modulators, several projects were reviewed, not only 2nd order Sigma Delta Modulators, but also 1st order. Three projects are presented here, which helped understanding the modulator's structure.

3.2.1 – 1st Order Sigma Delta Modulator [5]

This section presents once more a circuit that has been already used for a MEMS Accelerometer, a "2.5V 14-Bit ΣΔ CMOS SOI Capacitive Accelerometer" [5]. The block diagram for this system is presented below. The accelerometer has a differential output that follows to the switched capacitor charge amplifier, as explained in the previous chapter. After that it follows to the modulator. At the input of the sigma delta Modulator there is an AAF (Anti Aliasing Filter), and a 1st order sigma delta modulator, that includes an integrator, a 1-bit ADC (quantizer) and a negative feedback network (1-bit DAC).

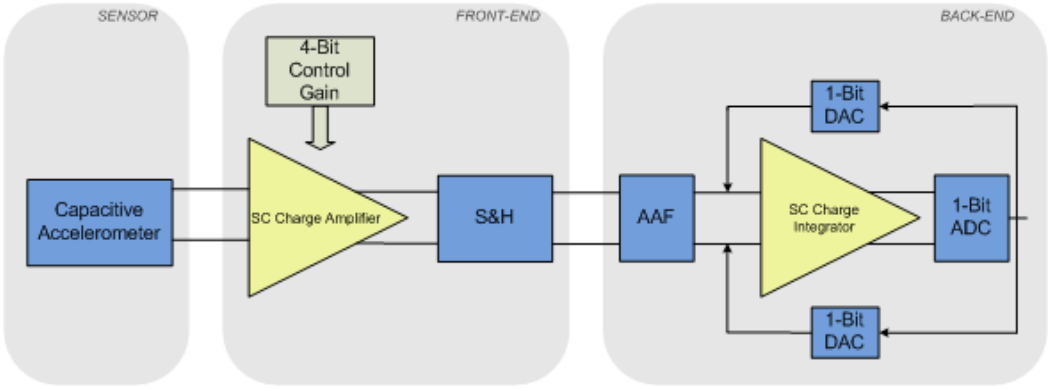


Figure 29 - Block Diagram for the Capacitive Accelerometer System

The back-end sigma delta modulator will be discussed now. The AAF is a Low pass filter that prevents aliasing, after the Modulator. In the next figure, the schematic of the back end is showed.

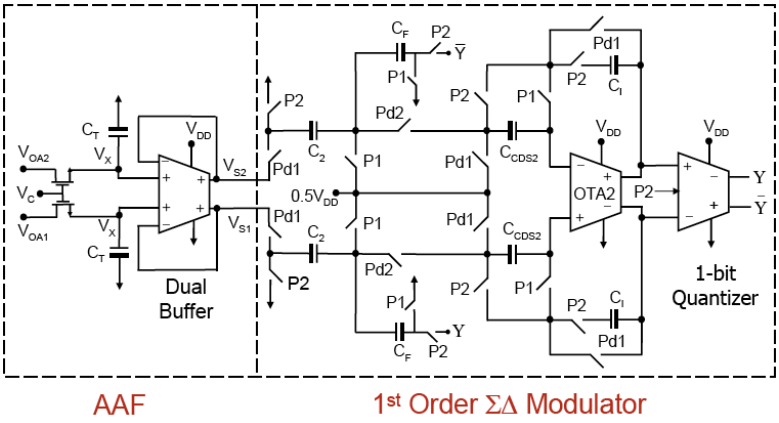


Figure 30 - Back End Schematic (reproduced from [5])

This block has two clock phases, P1 and P2. When P1 = HIGH and P2 = LOW (sampling phase), the capacitors C_2 are charged with the output of the Amplifier circuit, and the feedback capacitors C_f are charged with $V_{DD}/2$. Also during P1, the CDS capacitors C_{CDS} are charged with the offset and 1/f noise of the amplifier. When P1 = LOW and P2 = HIGH (Integration phase), the difference between the input signal and the feedback signal, provided by the 1-bit DAC, is going to be integrated through the SC Voltage Integrator. The noise and offset of the amplifier are also subtracted to the system. The output of the amplifier passes through the quantizer. At the output of the 1-bit quantizer will be the digital signal. The schematic divided by the two clock phases is presented below.

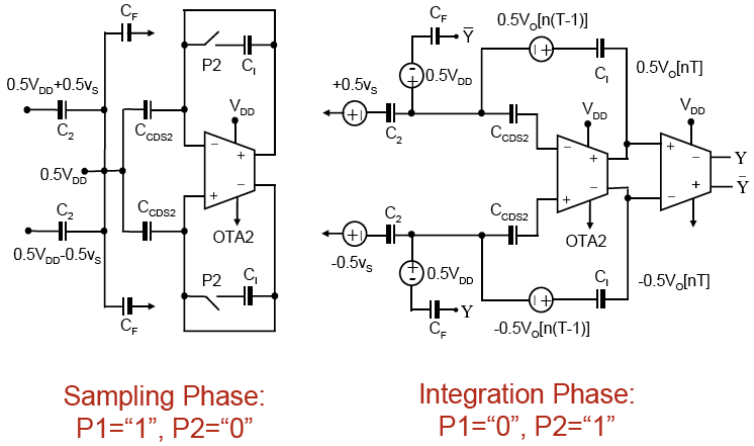


Figure 31 - Sampling Phase and Integration Phase (reproduced from [5])

This system has been tested. It has the ability of interfacing with different capacitive sensors with a good performance. The low frequency noise cancelation technique used, the CDS, has proved its effectiveness, reducing the noise significantly (up to 10dB) [5]. A resolution of 14 bits was achieved.

3.2.2 – 2nd Order Sigma Delta Modulator integrated in a readout chain [20]

The project "4.5V SC ΔΣ CMOS interface circuit for closed loop operation of a lateral capacitive microgravity Silicon On Insulator (SOI) accelerometer" (refer to [20]) is another possible route for the readout circuit. The interface circuit is composed by a SC Charge Amplifier, as a front-end circuit, and a 2nd order ΔΣ modulator, as a back-end circuit. The front-end circuit is very similar to the one presented previously in [5], as it was developed by the same authors. The 2nd order sigma delta ADC will be presented. The block diagram of the entire system in presented in the next figure.

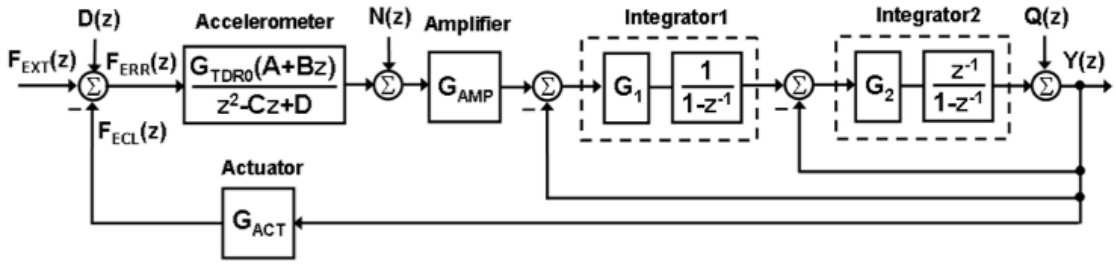


Figure 32 - Z-Domain model of the system (reproduced from [20])

As we can see, the difference between a 1st order sigma delta modulator and a 2nd order sigma delta modulator is the number of integrators. The 2nd order modulator has two integrators, with a digital feedback, in this case without feedback gain.

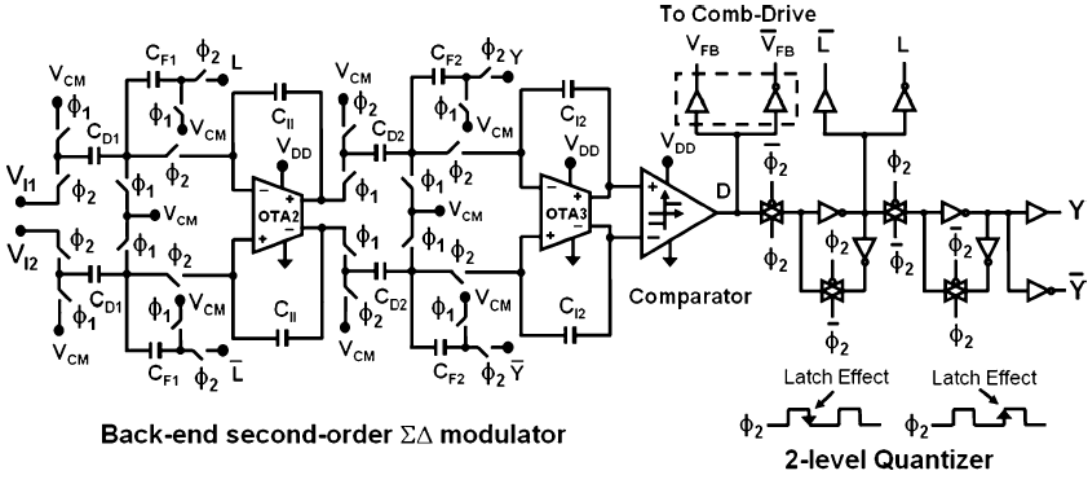


Figure 33 - Back End Schematic (reproduced from [20])

Figure 33 shows the schematic of the ADC. After the integrators, and in similarity to the 1st order ΔΣ ADC in section 3.1, there is the quantizer, composed by a comparator and a transmission gate D latch. During the fall of ϕ2, the output is latched. This is the moment to make the decision about the output of the 1-bit-DAC. By a combination of non-inverting and

inverting sigma delta Integrators, delay time is added as required by the Z domain model of the $\Delta\Sigma$ modulator. A non-inverting integrator generates a half delay, while an inverting integrator generates no delay. The integration capacities interpolate subsequent samples data and generated the analogue output. The output of the comparator is fed back to the accelerometer comb drive, in order to make the proof mass to go into the stand-by position. The signal in the transmission latch will be fed back to the integrators, in order to provide the 1-bit DAC.

The whole system was tested. By using a closed loop system, a noise reduction of 22 dB was noticeable, corresponding to an output dynamic range of 95dB and 15 bits of resolution at 20Hz.

3.2.3 – 2nd Order Sigma delta Modulator as an interface circuit of a capacitive accelerometer

Finally, a project developed as an interface circuit for SOI Accelerometer [21], presents an interesting approach for the readout chain. The aim of this work was to design an interface circuit capable of reading capacity changes, due to accelerations, and a signal processing circuits to convert its input to a digital output. The sigma delta architecture for the ADC was chosen for its wide dynamic range, inherent linearity and relaxed accuracy requirements on analogue circuits. The fully differential topology reduces the common mode errors such as substrate and power supply noise [21].

The block diagram for the ADC is presented in the next figure.

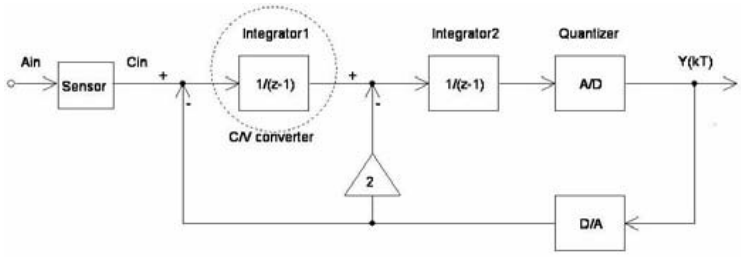


Figure 34 - Block Diagram for Sigma Delta ADC for SOI Accelerometers [21]

We can notice that in this architecture there is no need for a fully differential charge amplifier. The sensor in connected directly to the ADCs first integrator. It acts as a capacitance to voltage converter. In figure 35, the 1st integrator schematic is shown, with the accelerometer sensing capacitors. The sensing capacitors have a common electrode connected to $V_{ref}/2$. The integrator has two clock phases, P1 and P2, in similarity to other projects presented previously. When P1 is high, the other capacitor electrodes are connected to V_{ref}, zero, V_{ref} and Zero. This is called the pre-charge phase. When P2 is high (integration phase), the right electrode of the sensing capacitors is connected to the input of the Op-

Amp. The common-mode charges of the sensing capacitors are cancelled by each other, setting the common mode voltage of $V_{ref}/2$ and improving the CMRR of the op-amp.

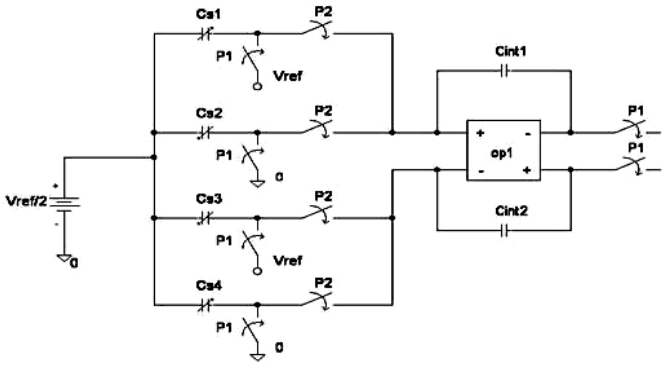


Figure 35 - Fully Differential Charge Integrator (reproduced from [21])

To reduce flicker noise (1/f noise) present in this circuit, a method compatible with the switched capacitor circuits was implemented, called autozeroing. This subtracts a recent sample of a time varying noise from the same noise, thus cancelling dc and low frequency noise [21]. Figure 36 shows us the fully differential SC charge amplifier with autozeroing.

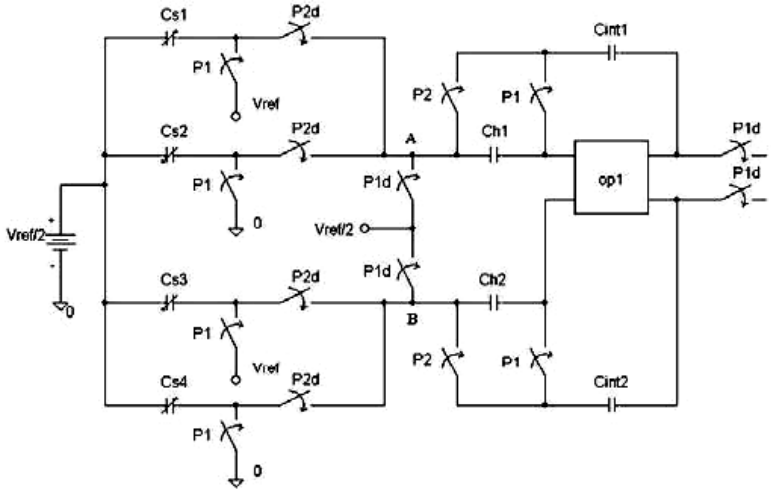


Figure 36 - Fully Differential Charge Integrator with Autozeroing (reproduced from [21])

The circuit adds two more capacitors (Ch1 and Ch2), which will save the sample of noise. When P1 is high, the sensing capacitors are connected as in the circuit without autozeroing. The flicker noise is stored in capacitors Ch1-2. When P2 is high, the voltage stored in these capacitors remains the same and will cancel the present flicker noise.

The 1-bit DAC is shown in the next figure. The outputs A and B will be connected to the input of the Op-Amp. The output of the comparator, Y+ and Y-, will control the switches in the DAC. The right electrodes of the capacitors C_{fb1-2} are connected to $V_{ref}/2$. When P1 is high, the left electrode of C_{fb1} is connected to V_{ref}, and C_{fb2} will be connected to zero. When

P2 is high, the right electrode of the capacitors will connect to the Op-Amp. The output of the comparator will decide if C_{int1} and C_{int2} will receive a positive or negative reference charge. If Y+ is high, C_{int1} will receive a positive reference charge and C_{int2} will receive the negative, while C_{int1} will receive a negative reference charge and C_{int2} will receive the positive reference charge, if Y+ is low. In this project, a feedback gain of 2 is imposed to the second integrator (refer to figure 34).

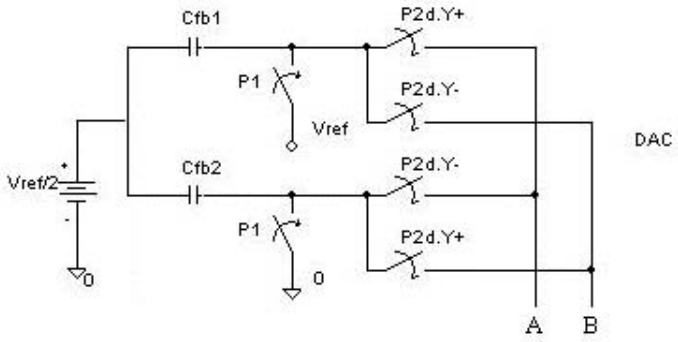


Figure 37 - 1-Bit DAC (reproduced from [21])

The second integrator of the ADC is equal to the first integrator. In order to reduce the consumption, the capacitors are 2.5 times smaller than the first integrator [21].

The simulation results of this circuit were very positive. It was proved that the autozeroing circuit reduces the flicker noise. The dynamic range is 84 dB, with 14 bits resolution, at a 2KHz signal Bandwidth.

3.3 Summary

The projects presented in this chapter were related to the development of inertial accelerometers. These are the most important source of information used for the development of the project presented in this dissertation. Section 3.1 presented different projects focusing on Fully Differential Charge Amplifiers. Previous work developed in the aim of this project was presented (refer to [19]). A Fully Differential Amplifier and its Charge Amplifier, with the noise reduction technique CHS were presented and the Fully Differential Amplifier was based on the work presented in [18]. A fully differential charge amplifier is also presented in [5]. The whole project was developed for a capacitive accelerometer. The noise reduction technique used is CDS. The project developed in this dissertation is a follow up of previously developed Fully Differential Charge Amplifier in [19], with the CDS technique presented in [5]

In section 3.2 the projects about Sigma Delta ADCs are presented. A 1st order sigma delta ADC structure is presented in [5]. The remaining projects presented in this section are

related to the development of a 2nd order sigma delta ADCs that are or can be integrated in an accelerometer system.

Chapter 4

Implementation and results

4.1 Fully Differential SC Charge Amplifier with CDS

The main target for this part of the project was to improve the previous developed Fully Differential Charge Amplifier with CHS made in [19] by Américo Dias. In order to improve it, the CHS technique had to be replaced for the CDS technique. As explained thoroughly in section 2.1.3, CDS technique is more suitable to use in applications that use sampled-data circuits, such as this Fully Differential SC Charge Amplifier and our Sigma Delta Modulator. The dc offset is eliminated, possibly improving the allowable signal swing, in contradiction to CHS, which modulate it to higher frequencies.

The changes made in the schematic were based on the project presented in [5]. The SC amplifier presented in figure 30 has the topology chosen for our project. The Fully differential Op-Amp was kept from [19], also as the SC CMFB. The schematic of the whole system is shown in Appendix A1, including the MEMS accelerometer model.

The front-end circuit, the MEMS accelerometer and Fully Differential SC amplifier schematics, will now be explained.

The Amplifier requires two clock phases, due to its Switch Capacitor architecture, one called sampling phase phi1 and an amplifying phase phi2. It has also two additional phases phi1d and phi2d, which are the same as phi1 and phi2 but with a slight delay. This delay is given in order to, when phi1d is high, all the other phi1 switches are already on. If that was not the case, interference could affect the signal. For phi2d is exactly the same reason. The block, which provides these clock phases, is called clockgen and its schematic is presented in figure 38. It is obvious that signal phi1-2 and phi1d-2d are the same signal, but the last ones have two inverters in order to provide a slight delay.

Figure 38 - Clock generator schematic

The inputs vmp and vmn of the accelerometer will control the voltage in its extremities (refer to figure 39). The block that controls the voltage in vmp and vmn is called vgen. It has two inputs, ch1 and ch2. These are connected by phi1 and phi2 consecutively. The outputs of this block are vmp and vmn that will be connected to the extremities of the accelerometer. When phi1 (ch1) is high, the voltage vmp is set by vgen block as V_{DD}, and vmn is set as ground. When phi2 (ch2) is high, the opposite occurs, vmp is grounded and vmn is V_{DD}. Figure 40 shows the vgen module.

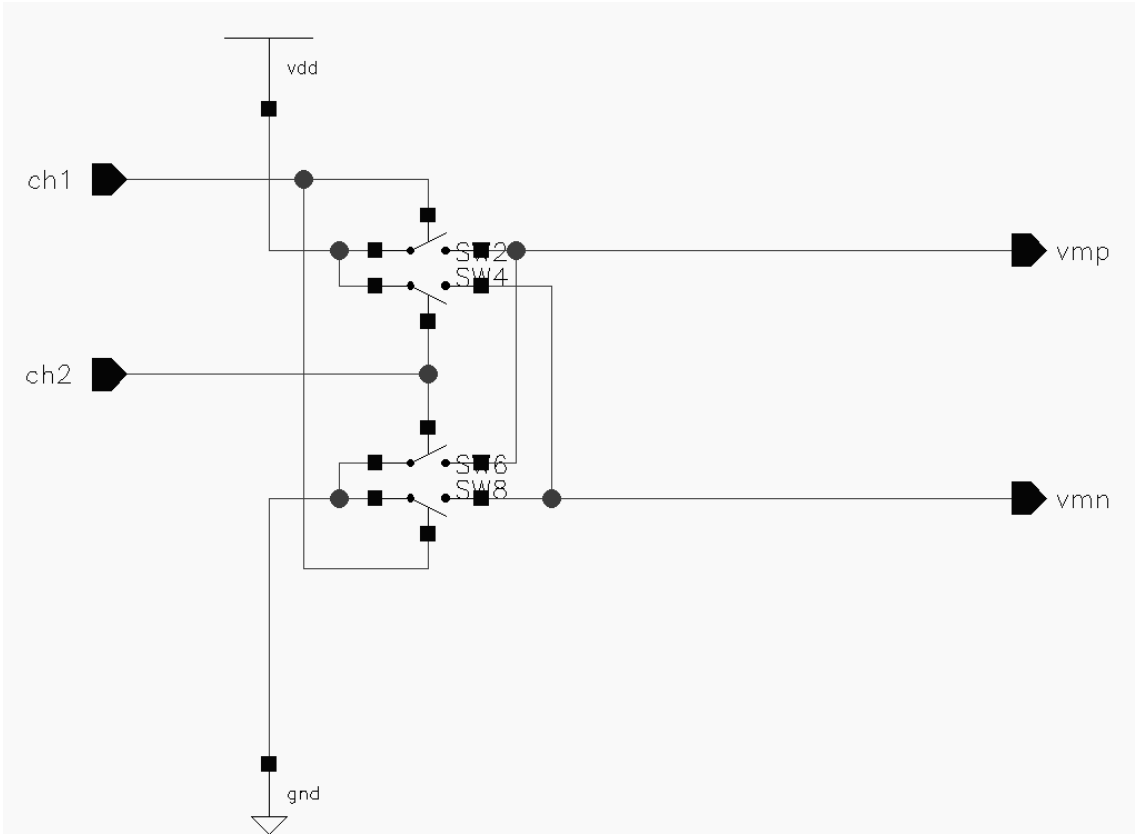


Figure 39 - MEMS Voltage generator schematic

The next figure shows how the vgen and clockgen blocks are connected together.

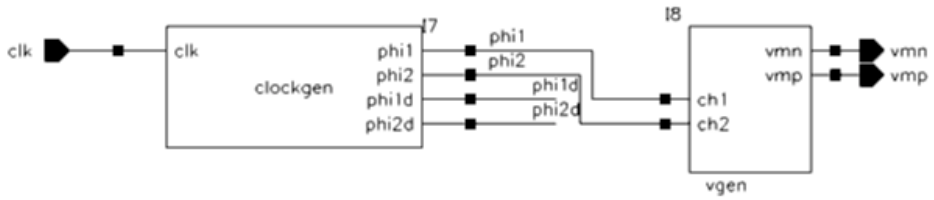


Figure 40 - Clockgen and Vgen Blocks

After presenting the blocks above, it is time to explain how the fully differential charge amplifier works. The schematic of the MEMS accelerometer and the amplifier divided by phases is shown in the figures 41 and 42.

During the sampling phase phi1, the MEMS capacitors C_{S1-2} are charged with vcmi ($V_{DD}/2$) and the reference capacitors C_{R1-2} are grounded. The CDS capacitors C_{CDS1-2} save the offset and low frequency noise. In the amplification phase phi2, the values saved in capacitors C_{S1-2} and C_{R1-2} will the transmitted to its output. The values are $V_{DD}/2$ from capacitor C_{R1-2}, which are connected to VDD and vcmi at the moment, plus the variation in voltage due to acceleration stored in capacitors C_{S1-2}. These values are transmitted through their outputs to C_{A1-2} where amplification is made. The capacitors C_{CDS1-2} cancel the offset and low frequency noise.

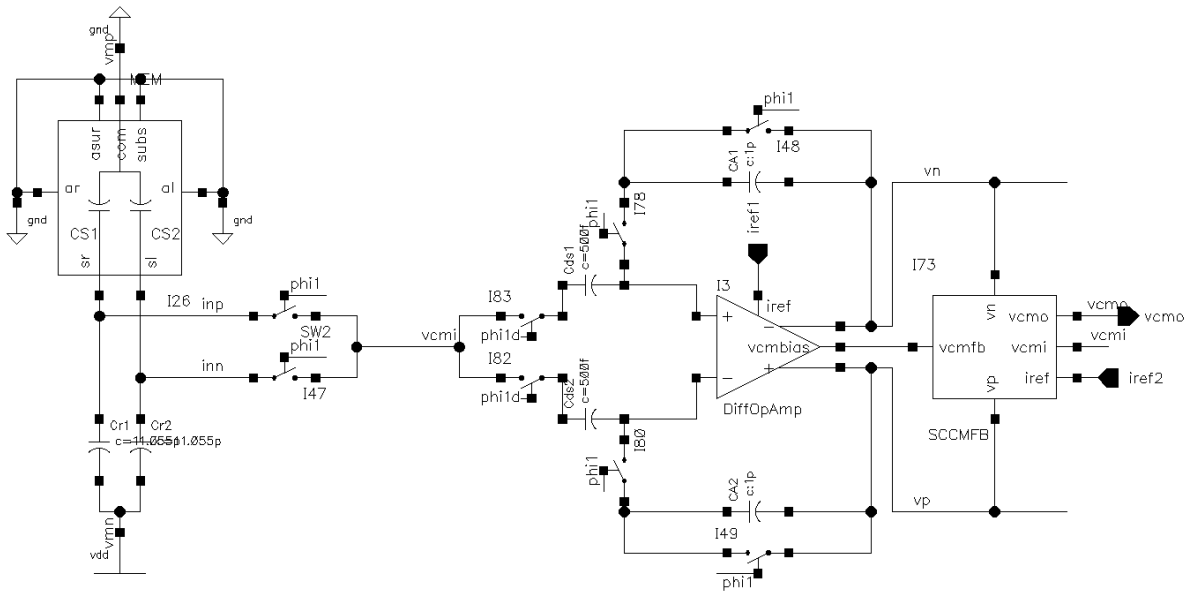


Figure 41 - Sampling Phase Phi1

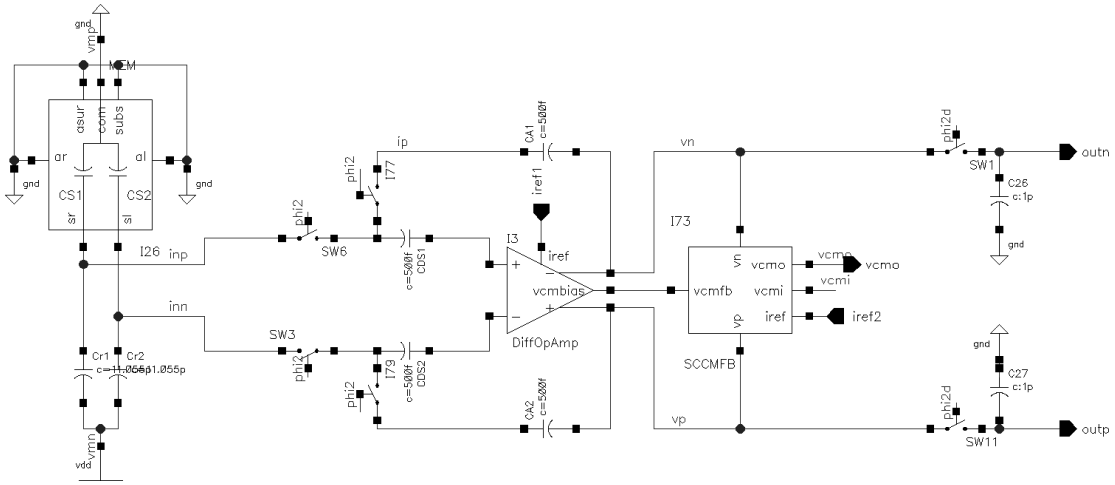


Figure 42 - Amplification Phase Phi2

Also during the amplification phase phi2, the S&H circuit, presented in figure 43, is active. This circuit takes the sampled signal and charge the S&H capacitors. They put the saved signal in the output after phi2d is low.

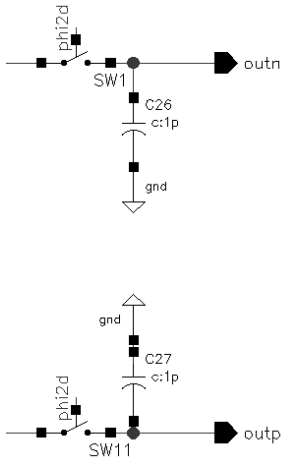


Figure 43 - Sample and Hold circuit

Similarly to the work developed in [19], the amplification capacitors $C_{A1\text{-}2}$ were substituted by a more complex circuit that enables the change in capacity by selecting a 3-bit digital input. The capability of switching these capacities will enable the user to change the amplification of the circuit. Remember that the Gain of this amplifier can be determined by

$$V_{OUT} = \left(\frac{(\Delta C_{S1} + \Delta C_{S2})}{C_A} \right) V_{DD}$$

The block for this capacity switch and schematic are presented in the next two figures.

The capacity can be switched by the inputs C0, C1 and C2. These switches will connect the capacities to V_{DD}, if on or off, if connected to ground. The combination of

capacitors in parallel will add the capacity that is seen at the output. Note that in phi1d, the amplifying Capacity is substituted by a short circuit.

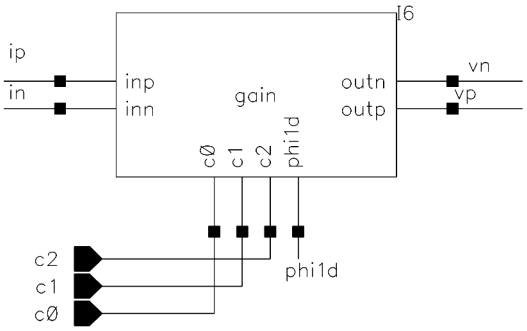


Figure 44 - Amplifying Capacity Switch

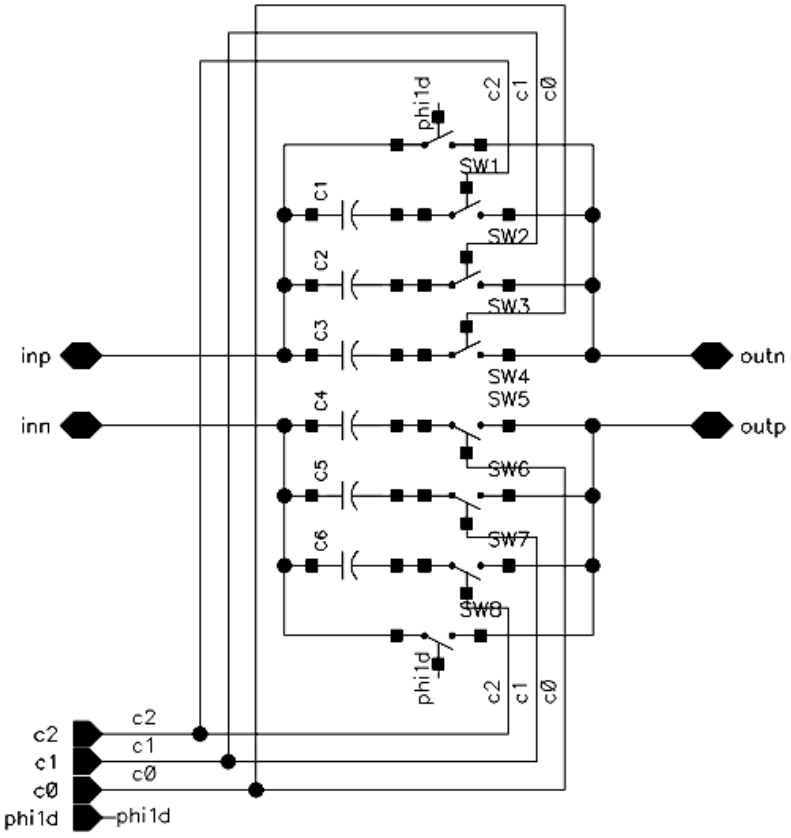


Figure 45 - Amplifying Capacity Switch Schematic

With the combination of these inputs, the amplifier can have 8 different values for the gain (refer to table 4). Capacitors value are C1/6=19.9pF, C2/5=9.95pF and C3/4=4.97pF. These changes in capacity are done digitally.

Table 4 - 3 Bit amplifying capacity change

C2	C1	C0	Total Capacity (pF)
0	0	0	0
0	0	1	4.97
0	1	0	9.95
0	1	1	14.9
1	0	0	19.9
1	0	1	24.9
1	1	0	29.9
1	1	1	34.8

The tests performed to the Fully Differential Op-Amp were made by Américo Dias. He developed a "Differential Amplifier Automated Testbench" [22], based on [23]. This testbench was performed in a post-layout phase of the Op-Amp. These results are more accurate than simulations made to the schematics and are presented in the results section.

4.2 Sigma Delta ADC

This section presents the development of the Sigma Delta modulator used for this Integrated System for a High Resolution MEMS Accelerometer.

Initially a 1st order Sigma Delta modulator was developed. In order to understand the structure and behaviour of the modulator, a schematic of an ideal single ended 1st order sigma delta modulator was built. The schematic is shown in Appendix A2.

The schematic is similar to the one presented in [5], without the CDS noise reduction capacity. It has two clock phases, sampling phase phi1 and integration phase phi2. In phi1, the value of the input signal is stored in capacitor C_D. Also in phi1, the output value is fed back to the input of the Op-Amp and then stored in the feedback capacitor C_F. In phi2, the feedback value stored in C_F is going to be subtracted to the input value stored in C_D. The resulting value of this operation will be integrated and then it will go through the comparator to the output. In order to use ideal components, it was used a VCVS (Voltage Controlled Voltage Source) as an amplifier. It was set to have a high gain. The amplifier has an inverting topology, as the input is negative, and its output is positive. The comparator will invert the signal. It is also built with the same VCVS with high gain as well, but with a maximum and minimum voltage of ±1.5V, avoiding the signal to have the maximum 3.3V (pike-to-pike) amplitude. The 1 bit DAC has the clock phases of the two switches different than the circuit in [5]. This is done since this ideal modulator does not have a transmission latch. This

transmission latch holds the value of the output in phi2, and then feeds it back to the amplifier input, only in -phi2. That is the reason why the 1-bit DAC has the clock phases of the switches swapped.

After developing the schematic of the 1st order ideal ADC, the 2nd order ideal sigma delta modulator was built. Its structure is very similar to a 1st order Sigma Delta ADC. The modulator has to be repeated twice and the comparator has to be connected at the output of the second modulator, instead of being connected to the output of the first modulator. The feedback is made from the output of the comparator to both integrators. The values of the capacitors are the same, with the exception of the feedback transistor C_{F2} that is twice the value of C_{A2} so that the feedback gain of the second modulator can be 2 [21]. The figure of the schematic is presented in Appendix A3.

Now the same architectures, but with non-ideal components and with a fully differential architecture will be presented.

Initially, The 1st order ADC will be presented. Its structure is very similar to the ideal ADC (refer Appendix A4 and A5). Switches made with transistors have replaced the ideal switches (refer to [19]) and the amplifier used in the modulator is the Fully Differential Op-Amp used in the previous section. A figure of the switches model is shown next.

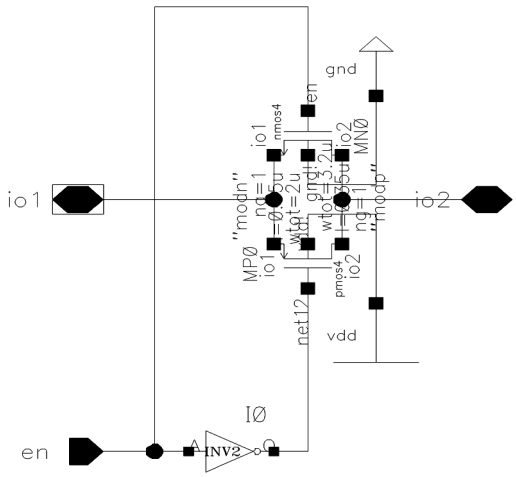


Figure 46 - Switches model [19]

At the output of the amplifier, a S&H saves the signal to be transmitted to the comparator. The comparator used in this ADC is also composed by VCVS. As the topology used is fully differential, two inputs and outputs are needed. This time, after the comparator is a transmission gate D-latch. It is connected to one of the comparator outputs. The other is simply an inverted signal version of the first. Before the input of the transmission latch, four invertors are added to impose a slight delay, to avoid meta-stability problems in the latch. The latch outputs are fed back to the circuit, as a 1-bit DAC. This time the switches are not swapped as in the ideal structure. To finish , two capacities C_{CDS1-2} were added in the circuit to reduce the low frequency noise.

As usual, the circuit has two main clock phases, phi1 and phi2. There are also other clock phases, the same as phi1 and phi2 but with slight delays. The next two figures show the difference between these phases.

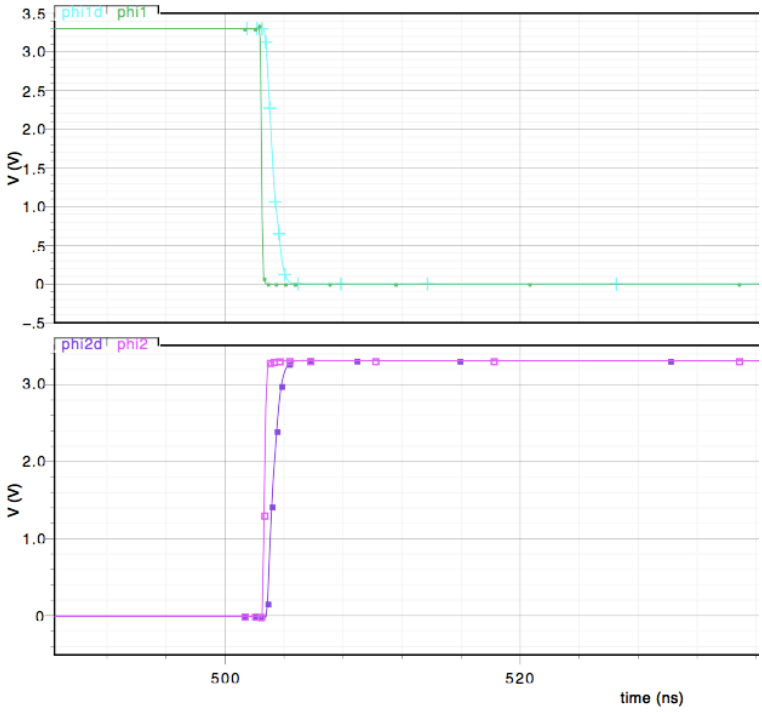


Figure 47 -Clock phases phi1-phi1d-phi2-phi2d

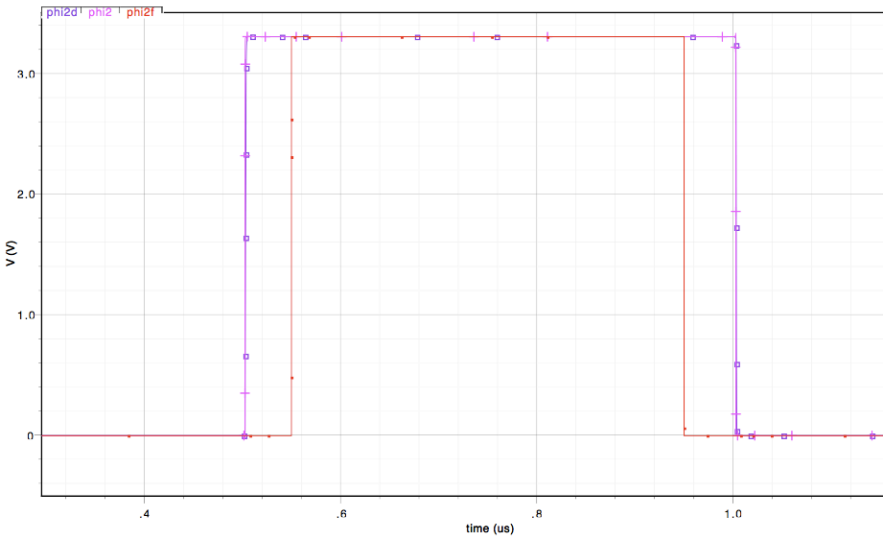


Figure 48 - Clock phases phi2-phi2d-phi2f

In phi1, the input capacitors $C_{D1\text{-}2}$ are charged with the input signal and the feedback capacitors $C_{F1\text{-}2}$ are charged with the output signal. They both have a common node that is connected to vcmi, which acts as a ground in this circuit. Also, the capacitors $C_{CDS1\text{-}2}$ store the

offset and low frequency noise. The switches phi1d have this delay to insure that the other switches are already on. They are the most important switches, so they wait until the others are already on, reducing clock feedthrough. When phi2 is open, these signals are subtracted and integrated through the SC integrator. The offset and low frequency noise are cancelled. The phi2d switches are the same case as in phi1d. For the same reasons, they wait until the other switches are on, and then they open.

The 2nd order ADC is very similar to the 1st order ADC, as in the ideal case (refer to A6, A7 and A8). The two modulators are connected to each other. The S&H circuit is only available in the first integrator, in order to hold the first integrator output value that is lost when the CDS phase is activated. At the output of the 2nd integrator, the comparator is set. This time an Op-Amp was developed to work as a comparator. The Op-Amp has a differential input and a single ended output. If the input value is higher than zero, it will saturate it and will set it with V_{DD}. Otherwise, it will ground it. The figure below shows the Comparator schematic.

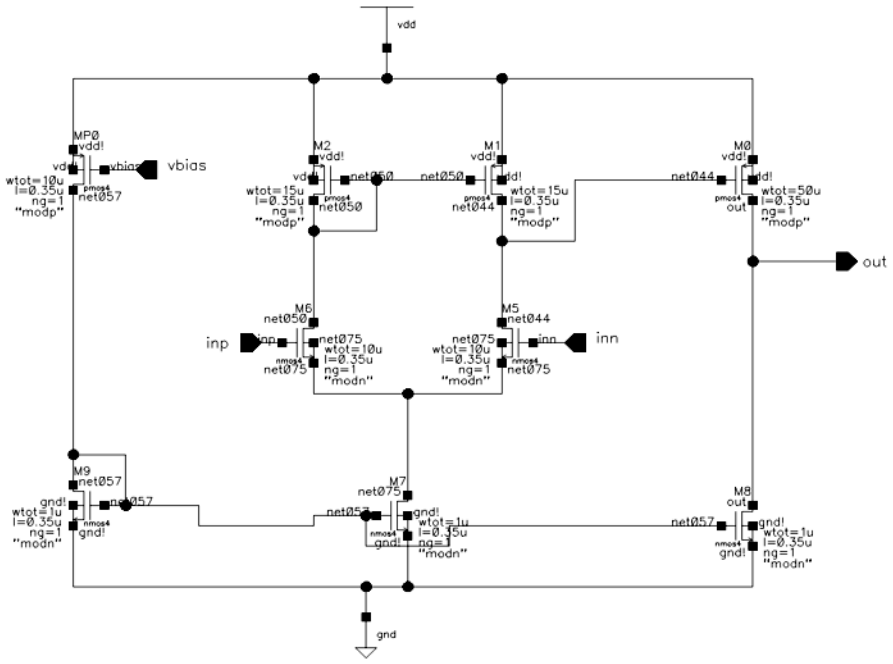


Figure 49 - Comparator Schematic

After the comparator, the transmission gate D-latch is set, as in the 1st order modulator. It will synchronize the output with the feedback connection, enabling the feedback to be made in the right time. After the transmission latch, a VCVS is set to reduce

the amplitude of the output wave, enabling the feedback not to saturate the integrators Op-Amps.

As the gain value of the feedback connection needed to be set, a Matlab model of a 2nd order Sigma Delta Modulator was made. Many simulations were performed to see how the modulator could be improved. As the output of the 1st and 2nd integrator saturated for some portion of the wave, the feedback capacitors were diminished to prevent saturation, setting the feedback gain of the 1st integrator to 1/5 and the 2nd integrator to 2/5. These values were implemented to the real 2nd order modulator.

4.4 Results discussion

4.4.1 Fully Differential Amplifier schematic results

The simulation results of the Differential Op-Amp are presented here. The "Differential Amplifier Automated Testbench" prints out the results of some tests.

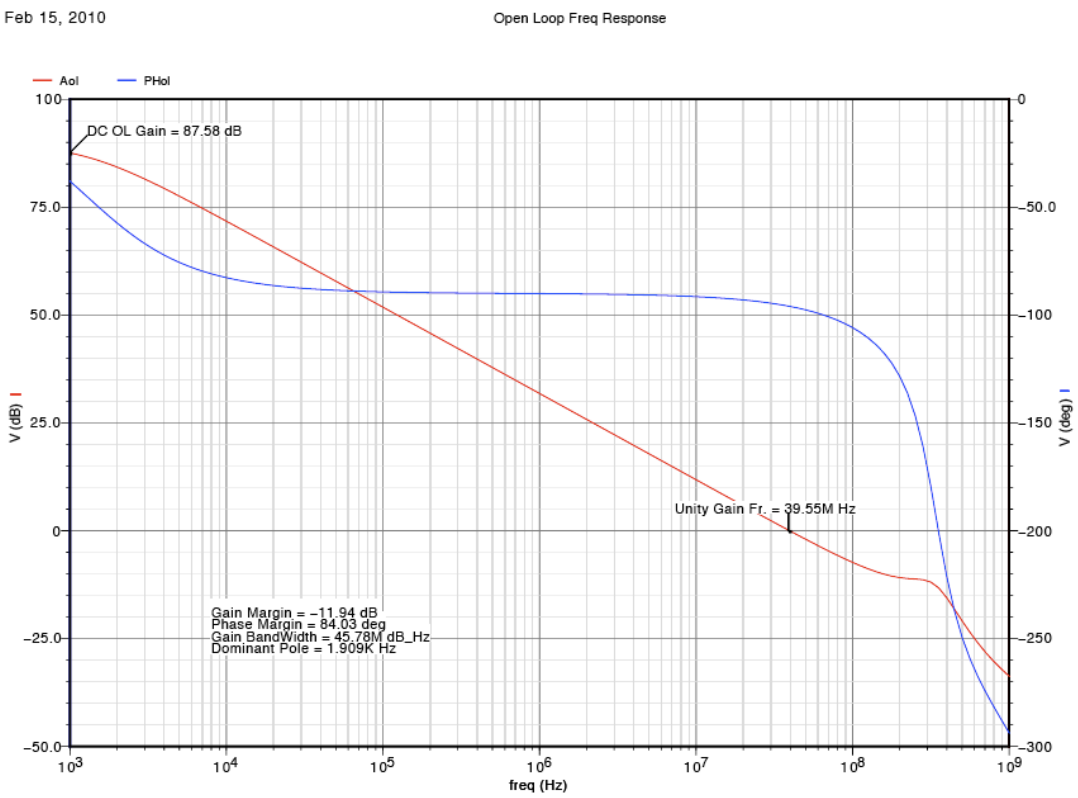


Figure 50 - Open Loop Frequency Responce

The figure above shows the frequency response of the open loop Op-Amp. The test is made by a frequency variation of the input signal. By making the frequency span, the open loop gain of the Op-Amp can be determined, and many other characteristics of this device.

The Op-Amp Open Loop gain is 87.58 dB. It falls rapidly with the increase of the frequency, as expected in an Open Loop Differential Op-Amp.

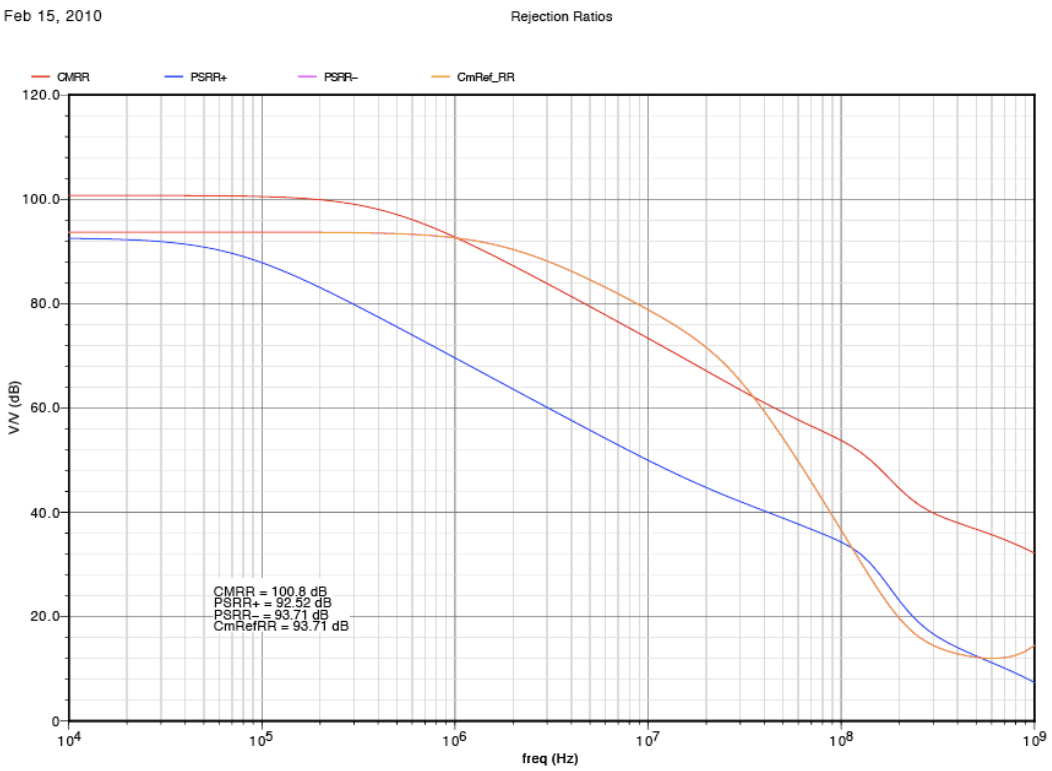


Figure 51 - Rejection Rates

In the figure 51, the rejection rates of the amplifier were measured. The Common Mode Rejection Ratio measures the ability of a circuit to keep its output constant with common mode perturbation at the inputs [24]. Low CMRR means that the perturbation effects at the output will be large. The value achieved by this Op-Amp is 100.8 dB. This value means that this amplifier can reject common mode perturbation quite well, not passing this perturbation to the output signal. The common mode rejection ratio of the reference voltage was also measured. Its value was 93.71dB. The Power Supply Rejection Ratio measures the effect at the output of the amplifier, of a perturbation on the power supply. If the PSRR value is high, means that the amplifier output is proportionally less affected to these perturbations. As the value measured is high on both positive and negative output, 92.52dB and 93.71dB respectively, the amplifier has good rejection rate for this type of perturbations.

After the Fully Differential Op-Amp being tested, the Fully Differential charge amplifier was tested. For that, we connected the MEMS Accelerometer model at its input. This model simulates the variation in capacity with two sensing capacitors. They have 20.619pF of capacitance; however only with 2.529pF they are at rest, being their equilibrium point. During the tests, the capacitors were set to a mean value of 11.055pf. Also the

reference transistors C_R have the same value, to minimize the output error voltage [5]. A variation in the sensing capacitors was made in order to simulate acceleration. This variation had the frequency of f_{SIG}=10KHz and a change in capacity of ±9.564pF, making a variation of 1.491pF<$C_{SENSING}$<20.619pF. This variation produced a variation in voltage in the amplifier inputs. The reference voltage vcmi has the value of 1.65V (V_{DD}/2). The reference currents for polarizing the Op-Amp are iref=50uA and iref2=300uA

The next figure is the differential output of the amplifier. The CDS capacities were set with 500fF, as in [5].

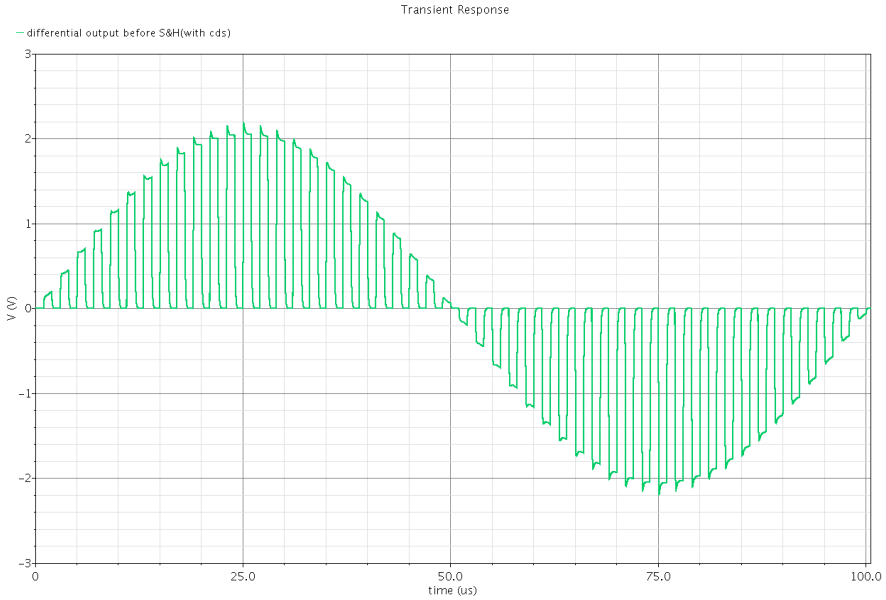


Figure 52 - Differential Output before S&H

A S&H circuit was implemented at the output of the amplifier. The reason for its implementation is very simple. During phi2, amplifying phase, the signal is amplified and the output is sent to the ADC. As the input of the ADC opens at phi1d, it would not receive the amplified signal. A S&H stores the amplified signal when phi2d is high, in its capacitor. When phi2d is low, the switch closes and stops any possible interference from the output of the Op-Amp. The S&H capacitor is connected to the input of the ADC, sending the stored signal, as the input switch of the ADC is closed.

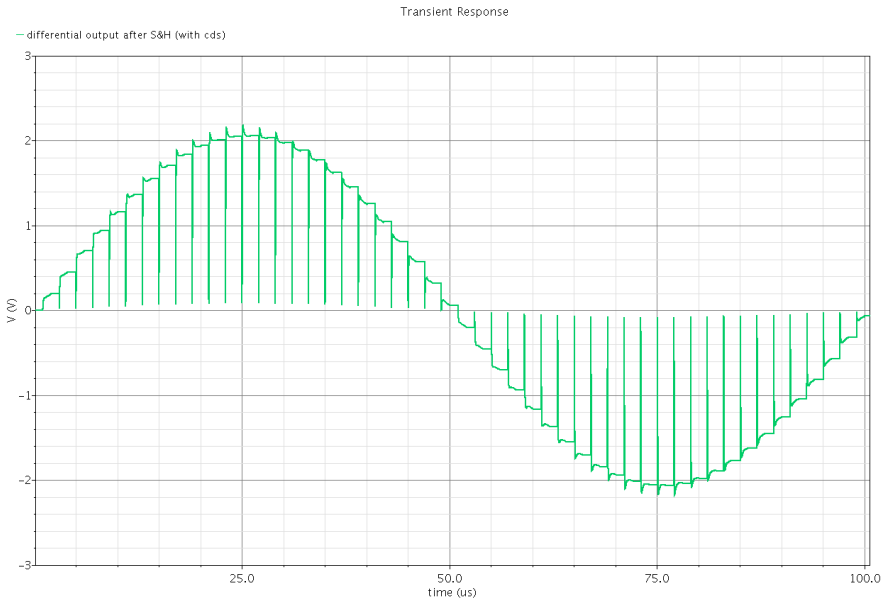


Figure 53 - Differential Output after S&H

Finally, the output after the S&H and a LPF is shown. The signal has a slight delay imposed by the LPF. Its cut frequency is 50KHz.The signal has more than 2V amplitude.

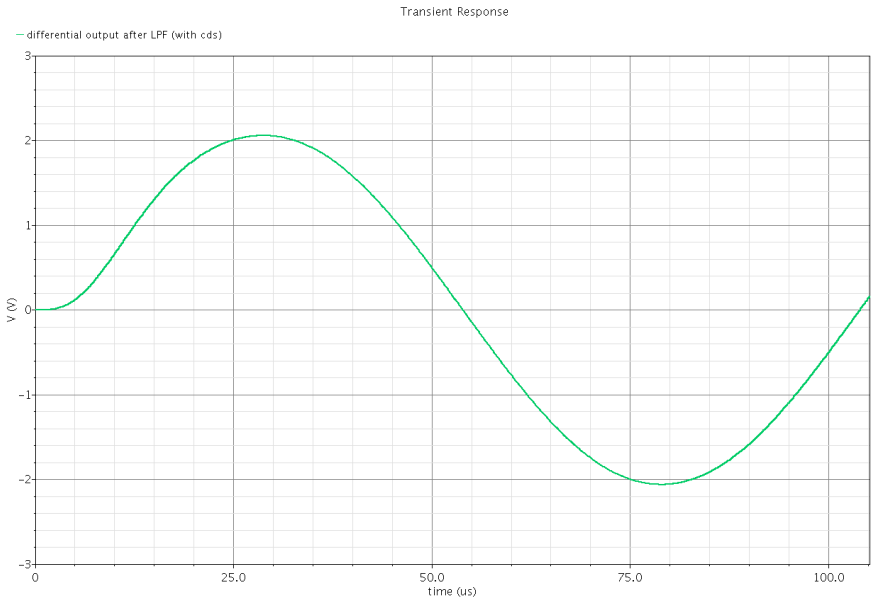


Figure 54 - Differential Output after LPF

4.4.2 Sigma Delta Modulator simulation results

In this section, the 2nd order Sigma Delta modulator simulations are being presented (refer to Appendix A5). As the final schematic of the 2nd Order Sigma Delta Modulator was concluded, it was time to perform some simulations. The main goal was to prove that it was

functioning properly. The circuit has a 3.3V supply. The reference currents, used to polarize both Op-Amps, are 50uA (iref1 and iref3) and 300uA (iref2 and iref4). The reference voltage vcmi was set to 1.65V. The clock frequency was set to 1MHz. the input signals inp and inn are set by sin wave with frequency of 10KHz, dc voltage of 1.65 and 1V amplitude. The input waves are out of phase by 180°.

The figure below shows the Sigma Delta Modulator output (just one side, the other is symmetrical). First, when the input signal is high positive, the wave has a duty cycle higher than 50%. When the input wave is high negative, the duty cycle of the output wave is less than 50%. When it crosses the middle point, 1.65V, the duty cycle is about 50% (refer to [5]), as expected and so the circuit is working properly.

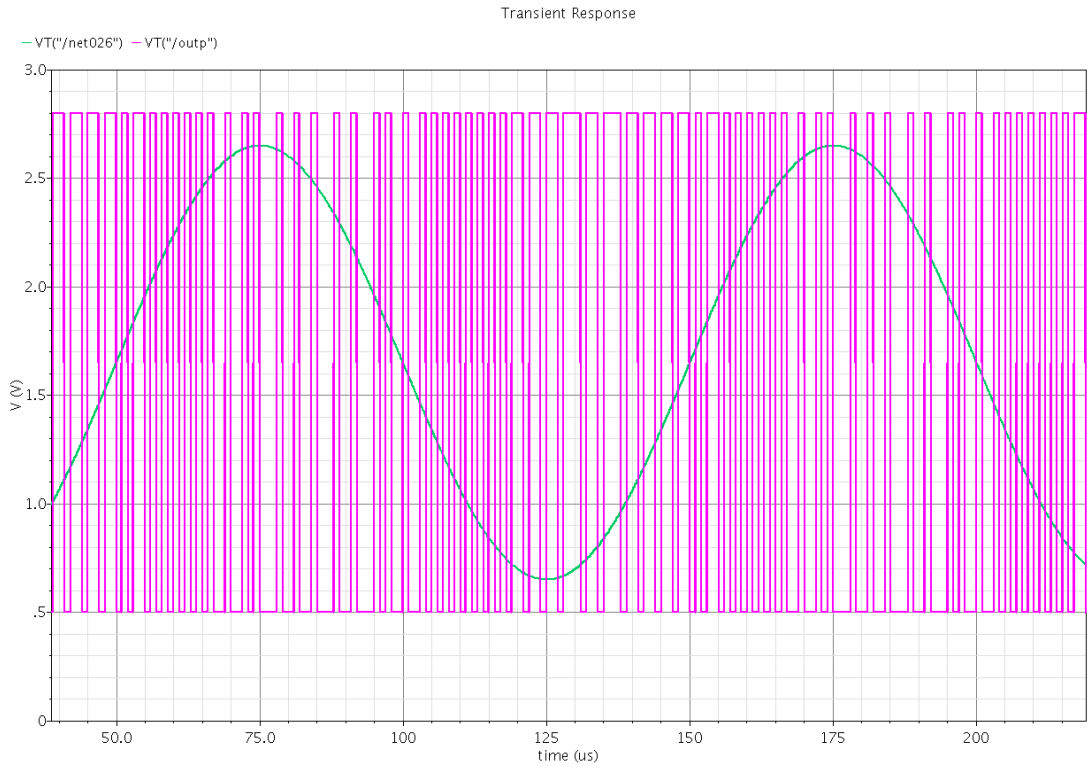


Figure 55 - Sigma Delta Output and Input

After, an FFT was made to see the resolution of the modulator. It is presented below.

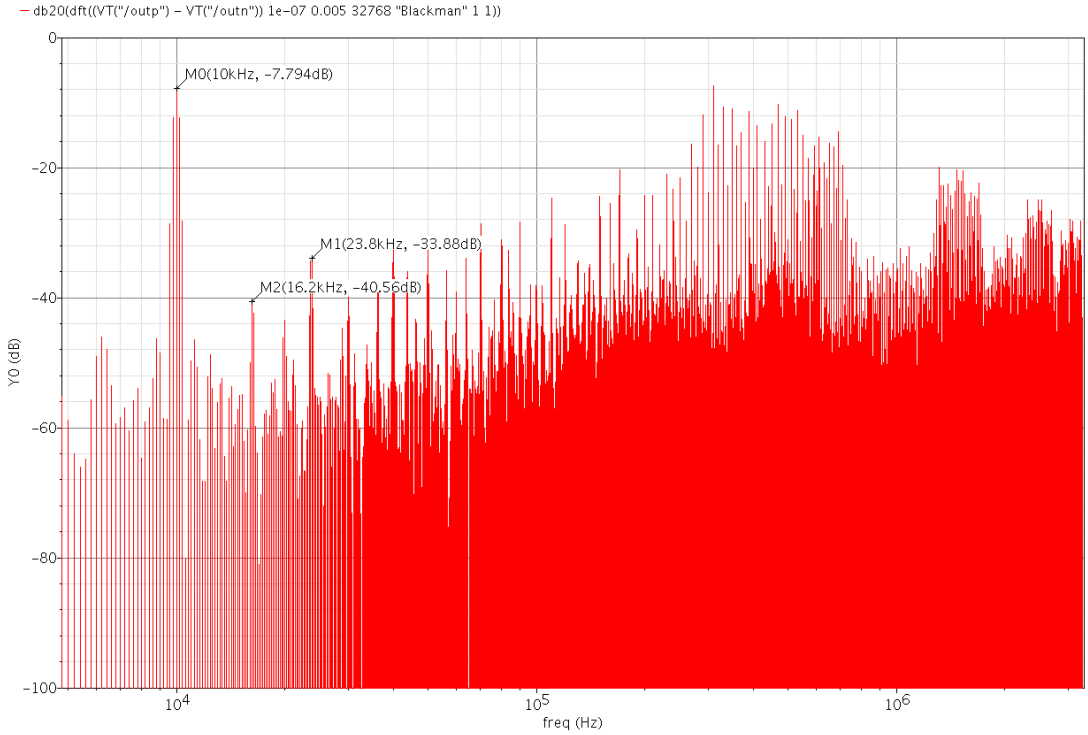


Figure 56 - 2nd order Sigma Delta Modulator FFT

For a previously defined bandwidth of 10KHz, the SNR is 32.77 dB, having a resolution of 5bits.

Chapter 5

Conclusion

5.1 Final Conclusion

An integrated system for a High Resolution MEMS Accelerometer was proposed in this dissertation. The background information search was made regarding all the main themes of this project, specifically Fully Differential SC Charge Amplifiers and Sigma Delta ADC. In this research, the advantages of the SC circuits and fully differential topology were explained. A comparison between noise reduction techniques was made, concluding that the Correlated Double Sampling technique, which was considered the most appropriate technique to integrate the system. The background information research includes several projects about charge amplifiers or differential Op-Amps. The schematic for the Fully Differential Charge Amplifier was made. One major component of this Charge Amplifier is the fully differential Op-Amp developed in [19]. Some tests were made, showing that this Fully Differential Charge Amplifier is working properly and as expected.

Also background information about Sigma Delta ADCs was searched. An introduction to several types of modulation was made. The benefits of integrating sigma delta ADCs were shown. The modulator that was developed is a 2^{nd} order Sigma Delta. Many previous developed projects on Sigma Delta ADCs for Accelerometer systems were used for gathering information.

The schematic of the Sigma Delta modulator was built. First ideal modulators, 1^{st} and 2^{nd} order, were built. After non-ideal 1^{st} and 2^{nd} order modulator were built. The 2^{nd} order modulator was tested. The modulator is working as expected. The resolution of the 2^{nd} order modulator was not as high as expected. This is due to lack of tuning of the feedback gain parameters and switches.

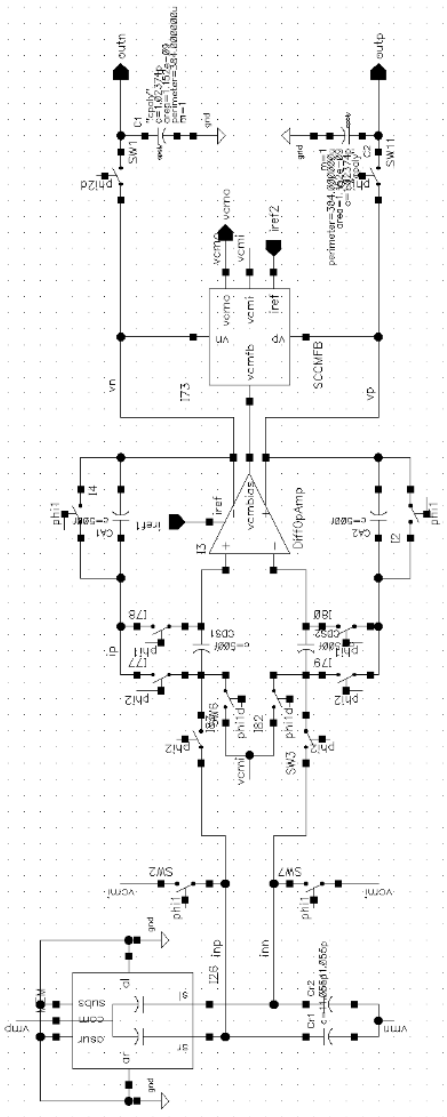
In conclusion, the Amplifier developed is working as expected and the Sigma Delta modulator is working properly, but with low resolution.

5.2 Future Work

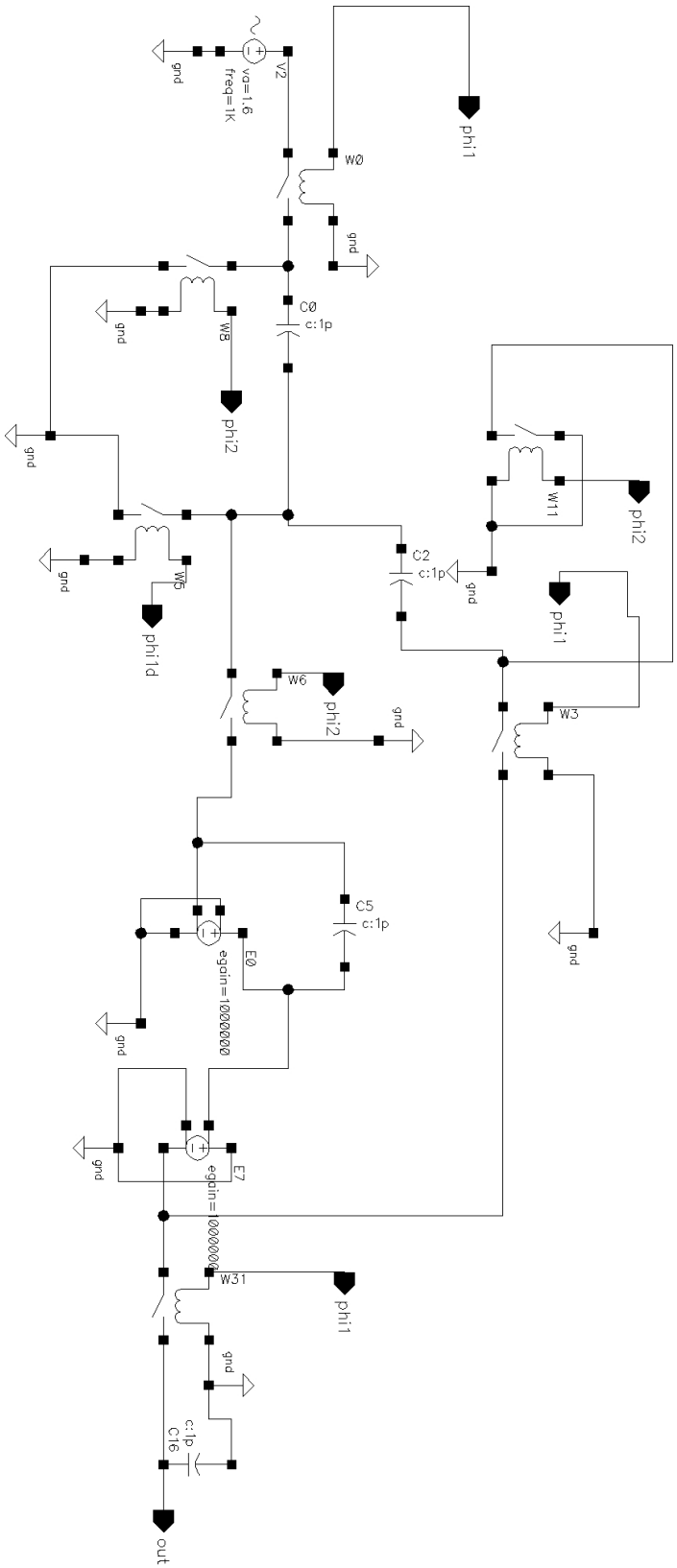
Noise analysis has to be made to the Fully Differential Amplifier. After that, the layout should be developed and the IC should be made. In the last step, the amplifier IC should be tested with the MEMS Accelerometer IC, already built.

Finally, the 2^{nd} order modulator needs some adjustments in order to improve its performance. By using the Matlab model of a 2^{nd} order Modulator, the feedback gain parameters should be tuned in order to improve resolution, as well as some adjustment in the switches. After that, the layout of the modulator should be developed, and the DSP.

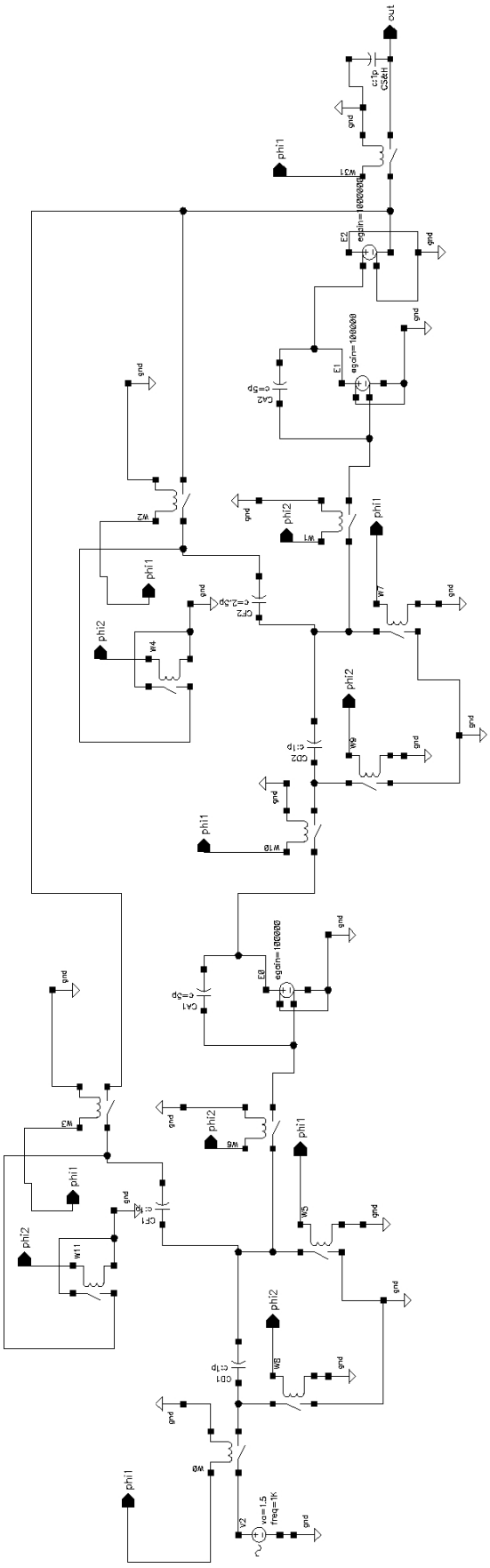
Appendix A



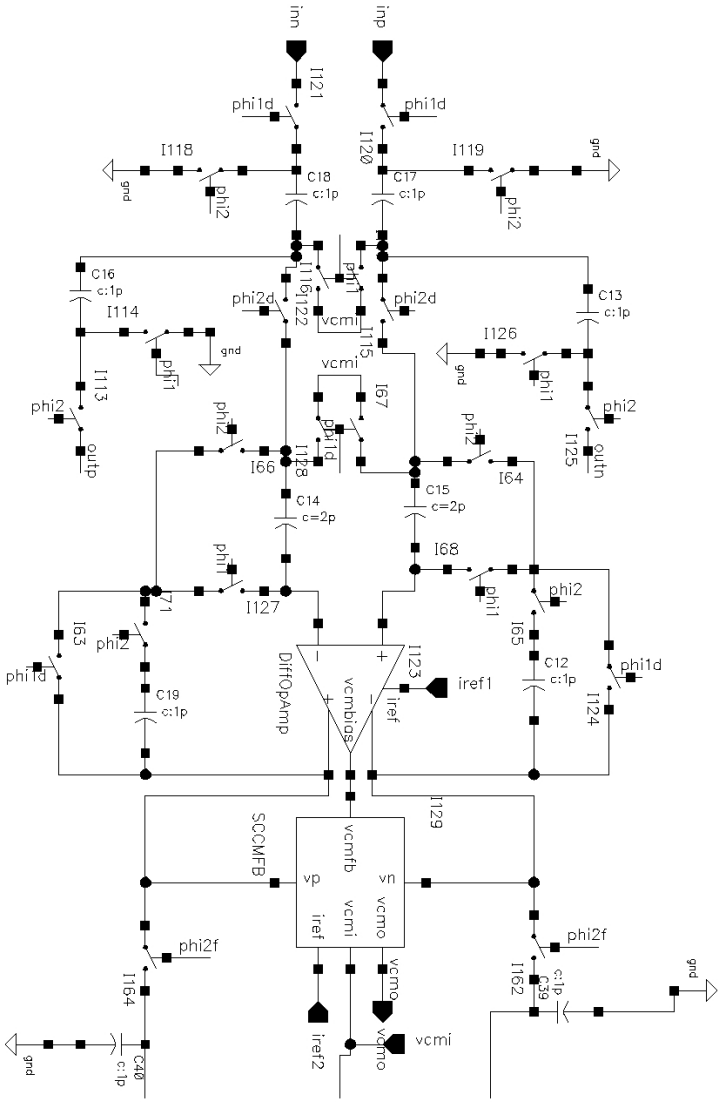
Appendix A1 –Accelerometer and Fully Differential Amplifier



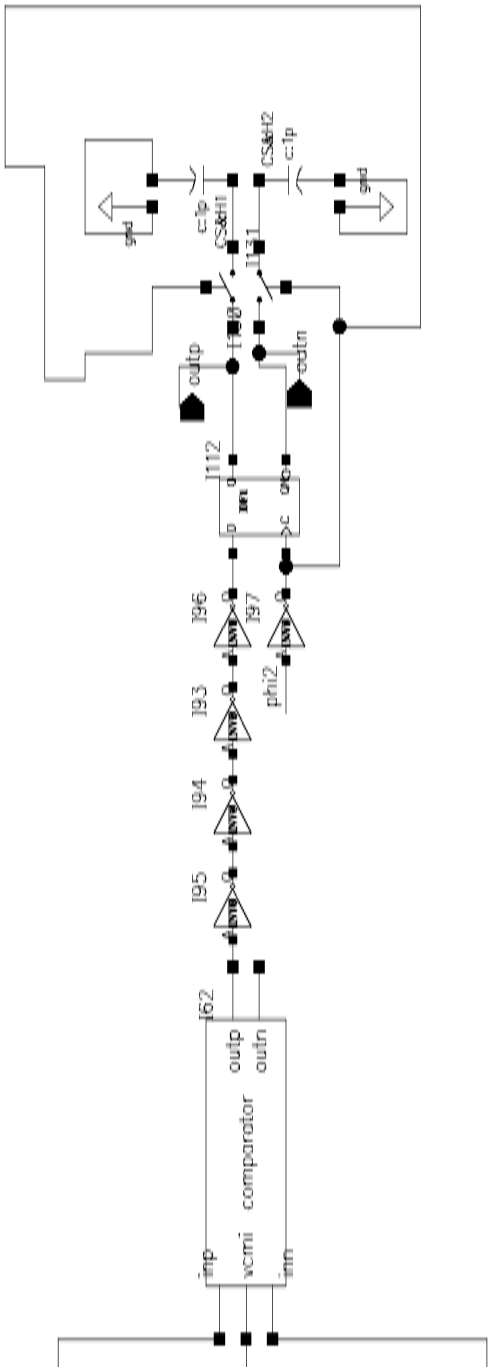
Appendix A2 – Ideal 1st order Modulator



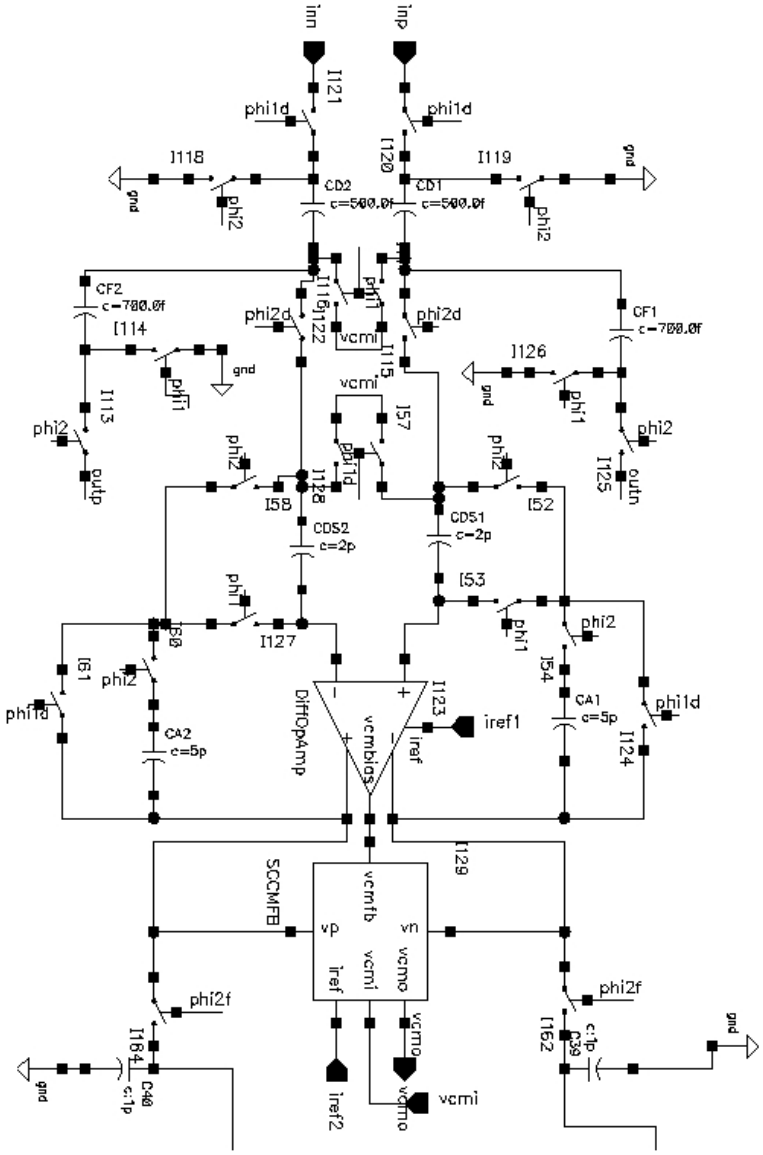
Appendix A3 – Ideal 2nd order Modulator



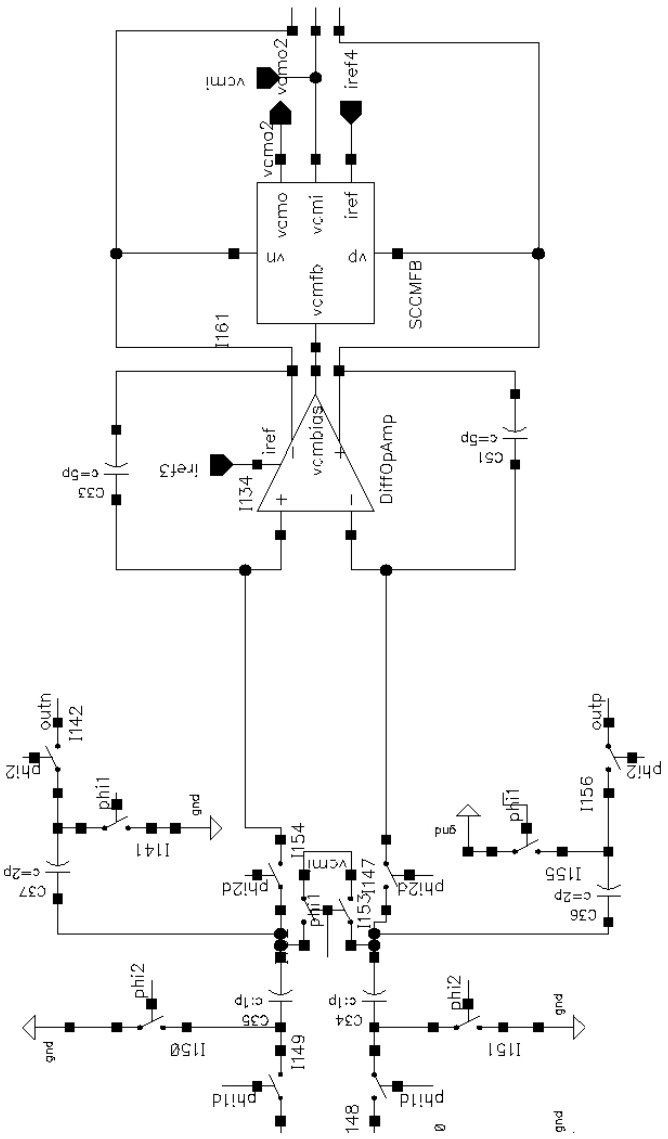
Appendix A4 – First order Modulator



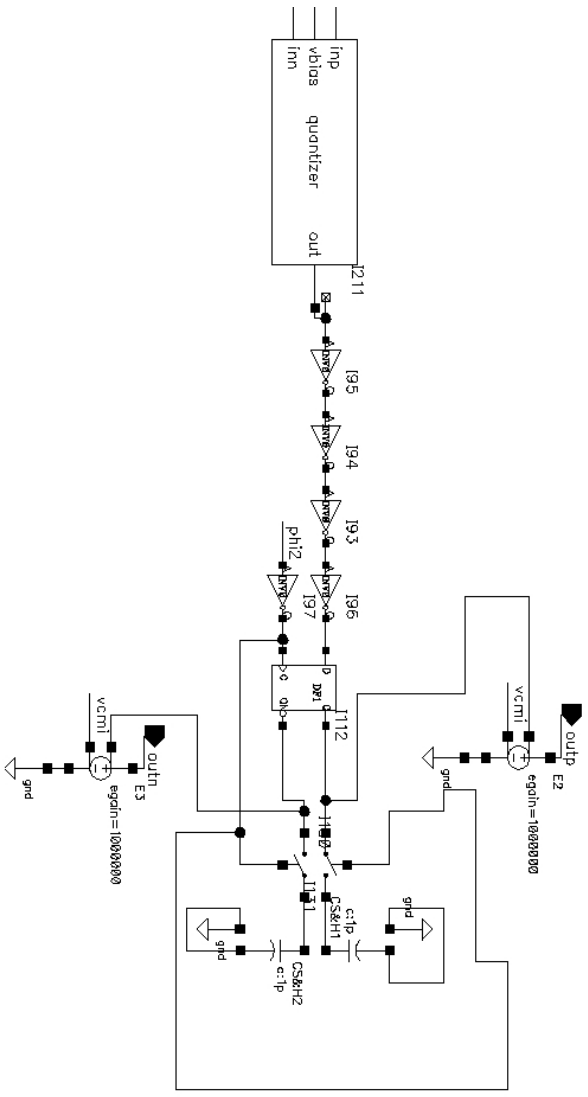
Appendix A5 – First order Modulator Quantizer



Appendix A6 - 1st integrator of 2nd order Modulator



Appendix A7 – 2nd integrator of 2nd order Modulator



Appendix A8 – Quantizer of 2nd order Modulator

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