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Radiation Tolerant Low Power 12 bit ADC in 130 nm CMOS Technology

Filipe José Pereira Alves de Sousa

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Supervisor: Prof. José A. P. Machado da Silva (FEUP)
Supervisor: Dr. Paulo Rodrigues Simões Moreira (CERN)

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Presidente Professor Doutor José Carlos dos Santos Alves
Professor Associado do Departamento de Engenharia Electrotécnica e de Computadores da Faculdade de Engenharia da Universidade do Porto

Professor Doutor Luís Alexandre Machado Rocha
Professor Convidado Equiparado a Professor Associado da Escola de Engenharia da Universidade do Minho

Professor Doutor José Alberto Peixoto Machado da Silva
Professor Associado do Departamento de Engenharia Electrotécnica e de Computadores da Faculdade de Engenharia da Universidade do Porto

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Autor - **FILIPE JOSÉ PEREIRA ALVES DE SOUSA**

Faculdade de Engenharia da Universidade do Porto

Abstract

Electronic circuits submitted to high doses of radiation may suffer some undesirable effects. To avoid those effects some particular design techniques can be used to harden their sensitivity to radiation. Currently available radiation hard technologies are very expensive. Another approach, yet a less costly one, is to design hardened circuits in commercial-grade technologies, using specific methodologies, which involve both design and layout techniques.

With the arrival of new and smaller CMOS technology nodes, that in fact show better tolerance to radiation, it's been good practice to redesign circuits previously fabricated in larger geometry processes. However if a smaller geometry dimension means more protection against Total Ionizing Dose effects, it also means lower V_{DD} voltage, which tends to turn the circuits more sensitive to Single Event Upsets.

In this work the design of a radiation tolerant low power 12 bit analogue to digital converter (ADC) in 130 nm CMOS technology, which will replace a previous one made within 250 nm technology, is presented.

An overview on the radiation effects in electric circuits is presented as well as the most common errors originated by radiation. Later on and after deciding which ADC architecture should be implemented, the design of the dual slope architecture is discussed. The Enclosed Layout Transistor (ELT), which eliminates the radiation induced parasitic currents between drain and source is presented. Some recommendations are also made for the layout phase, which are intended to provide the circuit with radiation tolerance characteristics.

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Acronyms and Symbols

ADC	Analogue to Digital Converter
ALICE	A Large Ion Collider Experiment
ATLAS	A Toroidal LHC ApparatuS
CERN	European Organization for Nuclear Research
CMOS	Complementary Metal–Oxide–Semiconductor
CMS	Compact Muon Solenoid
DAC	Digital to Analogue Converter
DCU	Detector Control Unit
DNL	Differential Nonlinearity
ELT	Enclosed Layout Transistor
FEUP	Faculdade de Engenharia da Universidade do Porto
GDI	Inside Output Conductance
GDO	Outside Output Conductance
GND	Ground
LHC	Large Hadron Collider
LHCb	Large Hadron Collider beauty
LSB	Least Significant Bit
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
NMOS	Negative Channel Metal Oxide Semiconductor
OpAmp	Operational Amplifier
PMOS	Positive Channel Metal Oxide Semiconductor
SAR	Successive Approximations
SEB	Single Event Burnout
SEE	Single Event Effects
SEGR	Single Event Gate Rupture
SEL	Single Event Latch-up
SES	Single Event Snapback
SEU	Single Event Upset

SHE	Single Hard Error
TID	Total Ionizing Dose

Chapter 1

Introduction

The work developed in this thesis has been carried out in the Microelectronics Group of the European Organization for Nuclear Research (CERN) in Genebra, Switzerland, in the framework of an agreement established between FEUP and these laboratories.

This chapter introduces the CERN which is the place where the work was developed. The objectives and the motivation of this project are also presented. And finally an overview of the following chapters is made.

1.1 - Introduction to CERN

Founded in 1954, the European Organization for Nuclear Research (CERN) Laboratory sits across the Franco–Swiss border near Geneva.

CERN is one of the largest and most respected centers for scientific research in the world and has now 20 member states, participating co-operatively.

Particle accelerators and detectors are used to study the fundamental particles of the universe. Physicists study the basic constituents of matter to learn about the laws of Nature and trying to find an answer about how universe works and what is made of.

As the name implies, accelerators speed up particles to high energies to then analyze the several thousand particles that result from their collision. These collisions must be observed at dedicated the detectors to later let physicists study the results. Experiment is the name given to a detector and its infrastructure. [1]

1.1.1 - The Large Hadron Collider (LHC)

The Large Hadron Collider (LHC) is the world's most advanced particle physics instrument. It is located about 100 m deep underground and it has a circular form with a perimeter of 27Km.

Sub atomic particles called "Hadrons"- either protons or lead ions – will travel in opposite ways inside a 27 Km long circular accelerator speeding up each lap. When particles reach high state of energy they will be brought into collision in four different experiments, each one installed in a large underground cavern.

These experiments produce large amounts of data that are later distributed by a grid computing system. With this distributed computing system it is possible to process data all over the world instead of using only CERN processors [2].

Two of the experiments, ATLAS and CMS, are general purpose experiments and aim to solve some of the unresolved aspects of the standard model:

- **ATLAS** aims exploring the fundamental nature of matter.
- **CMS** aims seeking new physics at high energies, trying to find the Higgs boson particle.

The other two experiences have a more dedicated aim:

- **ALICE** aims studying the physics of high energy particles.
- **LHCb** aims trying to justify the asymmetric relation between matter and antimatter since the birth of the universe [3].

The ADC which is meant to be redesigned in the present project is implemented on the silicon tracker inside the CMS set-up.

1.1.2 – Compact Muon Solenoid (CMS)

The CMS experiment aims exploring a wide range of physics phenomena, including the search for the Higgs boson, extra dimensions, and particles that could make up dark matter. It may have the same purpose of the ATLAS experiment but it uses unique solutions and designs to achieve the same goal [4].

The CMS detector is built around a very large solenoid magnet looking like an onion fill up with layers of detectors. These detectors are subject to high radiation levels (10MRads) and also in low temperatures (- 30 degrees).

The inner tracker community in CMS decided that all its electronics would be fabricated using a deep sub-micron technology with a feature size of 0.25 μm [5].

This was in the beginning of the construction of the CMS and now with the arrival of 0.13μm technology, new versions of the circuits being used, such as the ADC of this project must be made.

1.1.3 - Detector Control Unit (DCU) of the CMS Silicon Tracker

Electric circuits that are exposed to high level of radiation suffer aging effects and therefore it is necessary to maintain a reliable supervision about critical parameters such as leakage currents, local temperatures and supply voltages. To monitor these parameters with accuracy there is the need for a radiation hard detector control unit (DCU) capable of measuring the parameters and transfer that data to a processor unit.

In order to maintain safe operating conditions the silicon tracker - inner layer of CMS – is monitored by a DCU such as that described above.

All the parameters monitored by the DCU are measured by an A/D converter preceded by an analogue multiplexer. This A/D converter is to be re-designed in this project using a 130 nm technology. At least the same conversion characteristics must be achieved, that is: a

conversion time shorter than 100 µs, a gain between 2.18 and 2.20 LSB/mV that corresponds to a resolution of 500 uV/LSB and RMS noise around 0.25 LSB [6,7].

1.2 - Objectives and motivation

The objective of this work is to design a radiation hard 12-bit A/D converter to be used in the sensors of the DCU of the CMS silicon tracker. The converter will be exposed to high doses of radiation (10MRads) derived from the LHC experience. In environments like this electronics circuits may suffer critical deviations on their correct operation. To avoid those effects radiation-hard materials could be used on the manufacture of those exposed circuits. However, such materials are very expensive and do not use state-of-the-art technology. Another way of reducing the effects of radiation is using circuit design and layout specific methodologies that minimize those effects.

This work intends to use a 130 nm commercial technology (not radiation-hard specific) to design this ADC. As the technology by itself presents more robustness to radiation, one can say this approach is "hardening by design" (HBD) and because it is done with state-of-art technology it is also possible to benefit of the low power, high yield and low cost of such technologies.

1.3 - Structure of the document

This thesis is structured as follows:

- Chapter 2 introduces the energy particles and mechanisms which are responsible for radiation matter interactions. Then the most critical effects of radiation on circuits' behaviour are examined, particularly at the gate oxide because that is the most likely radiation sensitive part in a MOS transistor. The commonest radiation induced errors are also explained.
- Chapter 3 analyses the main characteristics of analogue to digital converters to allow a better understanding of the description of some ADC architectures. The specifications of the ADC to be designed are presented and used to justify the option for designing a dual slope architecture in this work and therefore a more detailed description of its operation principle is made.
- Chapter 4 looks in detail at designing the 12 bit dual slope converter. The building blocks for the analogue part are presented. The problems that occurred during the designing are also described as well as the solution adopted to circumvent them. Because of the fact that the architecture implemented suffered some modifications comparing to a typical dual slope, a phase to phase description of the conversion cycle is made.
- Chapter 5 presents some of the radiation hard devices that should be used in a radiation "hardening by design" approach. A special attention is made to the Enclosed Layout Transistor (ELT), which prevents the post irradiation leakage current inside the n-channel transistor. Radiation hardening techniques for digital circuits are also

presented. Later some recommendations on how to design radiation hard circuits are summarized.

- Chapter 6 presents the conclusions and suggests further developments.

Chapter 2

Radiation effects on electronic circuits

This chapter presents an overview on the most critical effects of radiation on circuits' performance. The main mechanisms which are responsible for these effects are described and the respective consequences on the main electrical parameters are highlighted. This description helps identifying how hardening can be improved by design.

2.1 - Radiation-matter interaction

The way in which radiation interacts with materials depends on several aspects, namely the type, kinetic energy mass and charge of the incident particle as well as of the mass, atomic number and density of the material. The moving particles in a semiconductor structure can be divided in two groups: charged particles and neutral particles.

2.1.1 - Charged particles

Charged particles interact mainly through coulomb attraction or repulsion with the target atoms. The charged particles of interest are protons, heavy ions and electrons.

Protons can interact in three different forms, by a) Coulomb interaction which can induce ionization or atomic excitation; b) collisions with the nuclei, which can cause excitation or displacement; or c) by nuclear reaction which can occur for protons energies higher than 10MeV.

Heavy ions give origin, qualitatively, to phenomena similar to those induced by protons.

Electrons can interact in two different manners, by a) coulomb interaction with the same results as for the case of protons; or b) scattering with nuclei, which can cause their displacement if the energy of the incoming electron is high enough and if it is transferred to the nucleus.

2.1.2 - Neutral particles

The main characteristic that distinguishes neutral particles from charged particles is the fact that neutral particles do not experience Coulomb force. Neutrons and photons are neutral particles.

Neutrons can be divided in three categories depending on their energy level. a) Slow neutrons for energy levels lower than 1eV; b) Intermediate neutrons which show energy between 1eV to 100keV; And c) Fast neutrons with energy above 100KeV.

Different reactions can occur when a neutron interacts with the atomic nuclei namely:

- Nuclear reaction, that is, the neutron is absorbed by the nucleus, which emits other particles (protons, α particles, γ photons);
- Elastic collisions which occurs when the incident neutron collides with the nucleus and continues its path. If the energy given to the nucleus is sufficient it may cause displacement of the nucleus and consequently cause ionisation or nuclear displacement;
- Inelastic collision, this reaction is similar to the elastic collision but in addition there is excitation of the nucleus which will emit gamma rays on its decay.

The reaction probability of these three interactions depends strongly on the energy level of the neutron. Slow neutrons give origin to nuclear reaction or elastic collision. Elastic collisions occur mainly with fast neutrons and for very high energies the inelastic collisions dominate.

Photons can interact with matter in three different ways: a) In the photoelectric effect, the incident photon ionizes the target atom and is completely absorbed while a photoelectric electron is emitted. The lack of the electron will make that other electron in an outer orbit fall into the spot vacant causing a low energy photoelectric photon to be emitted. b) Compton effect, in which the energy of the incident photon is divided between an electron of the target that is set free and a photon that is emitted. c) Annihilated creating an electron-positron pair. This last case only happens for energies greater than 1.024 MeV.

The interaction probability depends of the energy and also of the atomic number of the target as shown in Figure 2.1.

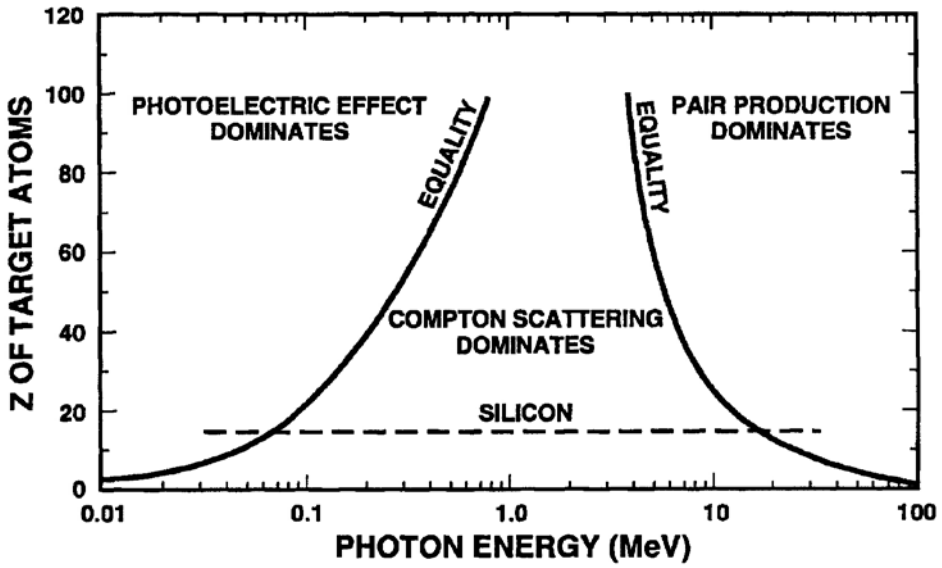

Figure 2.1 - Relative importance of the photoelectric effect, Compton scattering and pair production as a function of photon energy. Image drawn from [8 p. 16]

2.1.3 - Resume

The effects of both charged and neutral particles on matter can be grouped in two: ionization effects and nuclear displacement. Neutrons, will give origin mainly to nuclear displacement, whereas photons and electrons are responsible for ionization effects.

Ionization in a semiconductor or in an insulating material creates electron-hole pairs. The number of pairs created is proportional to the quantity of energy deposited in the material, which is expressed through the total absorbed dose.

Atomic displacement gives origin to the so called Frenkel defect, which occurs when an atom leaves its place creating a vacancy and stays in a nearby location not usually occupied by atoms (interstitial atom). This induced radiation pairs of interstitial atoms and vacancies recombine within a minute after the end of irradiation.

2.2 - Radiation effects in the SiO2 on transistors

CMOS devices are almost entirely insensitive to displacement damage, since they are devices whose conduction is based on the flow of majority carriers (holes in p-types semiconductors and electrons in n-types) and the major effect of the displacement damage is the reduction of minority charges lifetime.

When an ionizing particle goes through an MOS transistor, electron-hole pairs are generated. They quickly disappear in the gate (metal or polysilicon) and substrate because of the small resistance that these materials offer. In the other hand, in the oxide, which is an insulator, electrons and holes behave in different ways, being the electrons faster by five to twelve orders of magnitude than holes. In fact only a fraction of the radiation induced electron-hole pairs will recombine immediately after being created. The other pairs are separated in the oxide by the electric field and in the case of a positive bias applied to the gate, the electrons drift to the gate in a very short time (picoseconds) whereas the holes move towards the SiO_2-Si interface. Close to the interface but still in the oxide, some of the holes may be trapped, giving origin to a fixed positive charge in the oxide. Ionizing radiation also induces the creation of traps at the SiO_2-Si interface. An illustration can be seen in Figure 2.2.

2.2.1 - Transport of holes in SiO_2

When the gate is positive biased, the holes which do not recombine start to drift, due to the electric field, towards the SiO2-Si interface. This transport phenomenon is not regular, due to the fact that there is a very wide distribution of the transit times through the oxide.

2.2.2 - Positive charged trapped in SiO_2

After crossing the oxide the holes can be trapped close to the SiO_2-Si interface or to the SiO_2-gate interface. The trapping of holes in the oxide gives origin to a negative threshold voltage shift ΔV_{OX} that is not sensitive to surface potential in the silicon and which can stay for a period of time varying from milliseconds to years. The amount of trapped holes is proportional to the number of defects in the silicon dioxide.

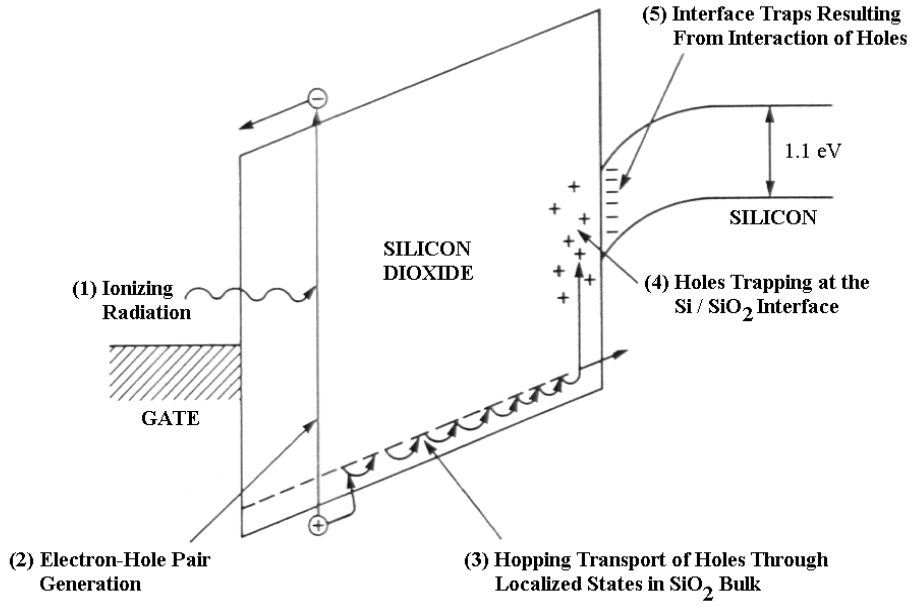

Figure 2.2 - Schematic illustration of the effects induced by ionizing radiation in an MOS device, when the gate is positively biased. Image drawn from [9 p. 39].

2.2.3 - Radiation induced traps at the Sio_2-Si interface

Another effect of radiation on MOS devices is the increase by several orders of magnitude of the trap density at the interface SiO_2-Si. As an example, in an n-channel transistor working in inversion, the acceptor-like traps in the upper part of the gap, being below the Fermi level, will be filled by electrons and then negatively charged, making necessary an higher gate voltage to have the same channel inversion (i.e. the threshold voltage is higher).

2.3 - Consequences of radiation on the electric parameters of a MOS transistor

The objective of this section is to present the consequences of hole trapping in the oxide and of interface traps generation on some electrical parameters of a CMOS transistor such as threshold voltage V_T, the subthreshold current and the leakage current, the carrier mobility μ and the transconductance g_m.

2.3.1 - Threshold voltage shift

The threshold voltage of a MOS transistor changes when the device is irradiated. This change ΔV_T is a combination of two factors, one related to the hole trapping in the silicon dioxide (ΔV_{OX}) and the other to the charge state of the interface traps (ΔV_{it}).

2.3.2 - Threshold shift due to the oxide charges

The charges trapped in the oxide give origin to a shift in the flat-band voltage and therefore in the threshold voltage. It could be expressed as [10]

$$\Delta V_{OX} = -\frac{1}{C_{OX}} \cdot \int_0^{t_{OX}} \frac{x}{t_{OX}} \rho(x) dx \quad (2.1)$$

Where t_{OX} is the gate oxide thickness, C_{OX} is the capacitance per unit area and $\rho(x)$ is the charge distribution in the oxide per unit volume as a function of the distance from the gate-oxide interface x.

It can be seen that the voltage shift that results from this contribution is negative when the charge is positive. For example for a p-channel transistor the positive charge trapped in the oxide repels the holes in the channel. This means that to re-create the same inversion condition one will need to apply a more negative potential to the gate, i.e. the threshold voltage is lower (higher in absolute value). The effect of the oxide charge on the voltage shift is weighted by its position in the oxide: the closer the charge to the SiO_2-Si interface, the higher the threshold voltage shift.

2.3.3 - Threshold shift due to the charges at the oxide-silicon interface

The charge distribution at the oxide can be considered bidimensional and simply expressed as $\Delta V_{it} = -\frac{\Delta Q_{it}}{C_{ox}}$ where ΔQ_{it} is the difference of the charge (per unit area) which fills the interface states after and before irradiation. This means that for an n-channel transistor the threshold voltage shift will be positive, and for a p-channel the shift will be negative. This is, the threshold voltage shift will increase, in absolute value, for both n-channel and p-channel transistors.

The interface states increase is a slower process than the build-up of positive charge in the oxide. For this reason ΔV_{it} can start to play a role later than ΔV_{ox}. This also explains why the threshold voltage shift for an n-channel transistor as a function of the total dose or the annealing time can be negative at the beginning and becomes positive. This effect is known as rebound.

The slower temporal evolution of the radiation-induced interface states also plays an important role in the annealing of the irradiated circuits, since this will decrease ΔV_{ox} but will probably increase ΔV_{it} both for n-channel and for p-channel transistors, affecting in this way the bias conditions of the circuit.[9]

2.4 - Increase of subthreshold and parasitic currents

For a $VGS = 0V$ there is a small current which flows from drain to source and it is called "off-state" current or "leakage current". When an n-channel transistor is irradiated the "off-state" current increases. This increase is related to the increase of the subthreshold current and to the generation of parasitic currents.

2.4.1 - Increase of the subthreshold current

The increase of the subthreshold current is linked with two factors. One is the decreasing of the threshold voltage and the other is the decrease of the subthreshold slope due to the radiation effect. **Figure 2.3** shows these two factors. The pre-irradiation solid line will shift after irradiation towards the y axis (dotted line), because V_t goes from V_{t1} to V_{t2} (decreasing

the threshold voltage). Also, after radiation the slope will decrease and becomes the solid line after radiation thus increasing the subthreshold leakage current from I_2 to I_3.

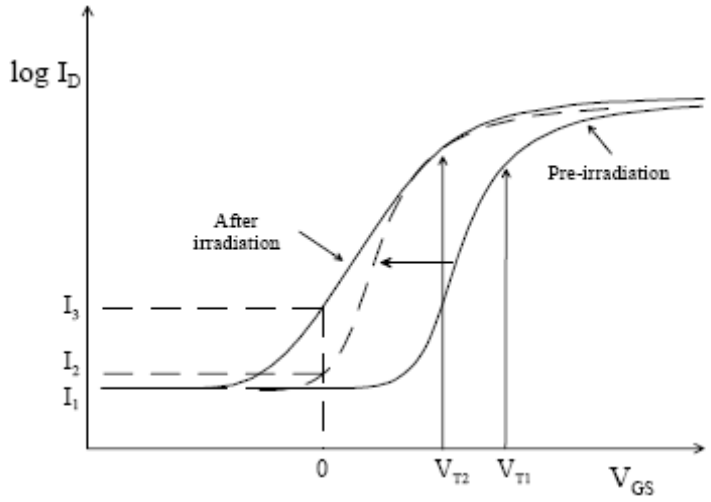

Figure 2.3 - Increase of the subthreshold current in a n-channel transistor given by a decrease in the threshold voltage and in the subthreshold slope. Image drawn from [9].

It was supposed that radiation-induced threshold voltage shift of an n-channel transistor is negative. And in fact, that is true for technologies with relatively thick gate oxide (>10 nm). For these technologies the negative contribution to the threshold voltage shift given by holes trapped in the oxide was generally higher than the positive one given by the charged interface states.

However for new and thinner technologies (deep submicron) the gate oxide is so thin that the contribution $|\Delta V_{ox}|$ can be smaller than $|\Delta V_{it}|$. This happens because there is a smaller volume where one can generate holes and also because the annealing of trapped holes plays an important role already during irradiation.

So it is difficult to predict the sign of the radiation-induced threshold voltage shift in an n-channel device. Often it can be only checked with measurements on the technology of interest.

2.4.2 - Increase of the parasitic currents

Other contribution to the post radiation “off-state” current in an n-channel transistor is the creation of two parasitic paths. They consist of the corner/sidewall leakage current path from source to drain (path 1 in Figure 2.4) in the n- channel transistor and the n+ to well leakage path beneath the trench (path 2).

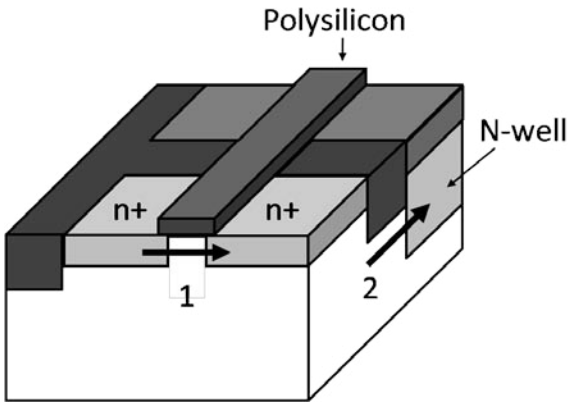

Figure 2.4 - Arrows indicate two possible parasitic-leakage current paths in a shallow trench technology.[11]

Also, after irradiation, degradation of mobility of the carrier occurs, due to the increase of the interface traps. This degradation of mobility gives origin to a degradation in the transconductance, which is proportional to μ in the linear and to $\mu^{1/2}$ (for a constant current) in saturation. As result the driving capability of the device is decreased. [9]

2.5 - Radiation effects in electric circuits

As stated before radiation environments can have undesired effects on electronic circuits. These effects could change a logic state or in the worst case leave the circuit to destruction.

Radiation effects could be characterized into three different types taking into account their effect on electronic devices.

2.5.1 - Total Ionizing Dose (TID)

As radiation particles pass through the electronic circuit, they produce electron-hole pairs within the gate and field oxides of MOS structures. Electrons have high mobility in the oxide and are quickly swept out. The holes, which have less mobility, will be trapped in the oxide. This will change the threshold voltage and mobility of the gate and field-oxide transistors' active regions, modifying their characteristics. Since the total charge from a single particle interaction is generally too low to cause damage in circuit, total ionizing dose results only from the aggregate interactions of a large number of protons or electrons within the regions of CMOS devices.

Total Ionizing Dose effect could cause leakage current created by the trapped charges. These leakage currents are generated by the "escape" of those trapped charges by tunneling effects or on the edges of NMOS transistors. Leakage currents will increase the current consumption of the circuit until they reach the point where the basic circuit functionality is lost. Modern sub-micron technologies tend to be more resistant to TID effects because the space to get charges trapped is smaller than that that used to be seen in older and larger technologies. Total ionizing dose degradation usually results from the aggregate interactions of a large number of protons or electrons within the regions of CMOS devices.

2.5.2 - Displacement Damage

Hadrons may displace atoms (therefore called displacement effect) in the silicon lattice of active devices and thereby affect their function. Bipolar devices and especially optical devices (e.g. Lasers, LEDs, optical receivers, opto-couplers) may be very sensitive to this effect. CMOS integrated circuits are normally not considered to suffer degradation by displacement damage.[12]

2.5.3 - Single Event Effects (SEE)

Single event effects are transient phenomena, triggered by a single high-energy particle interacting with p-n junctions within a semiconductor. Highly ionizing particles can directly deposit enough charge locally in the silicon causing internal latches or registers to switch states. This will introduce random errors in sequential logic circuits or memories or/and disturbing the correct function of electronic circuits, namely in the analogue ones.

The new generation circuits, using down-scaled technologies, have become more sensitive to SEEs because they require less switching energy as they use less voltage, and operate with smaller biasing currents.

The different SEE effects are normally characterized by an energy threshold and a sensitivity cross-section at energies well above the threshold. These effects can be divided into two groups those where errors are reversible (i.e. non destructive), in which they are called soft errors, and those with non reversible errors (i.e. destructive) in which case they are called hard errors. An example of a soft error is the SEU (Single Event Upset), and for hard errors there are SEL (Single Event Latch-up), SES (Single Event Snapback), SHE (Single Hard Error), SEGR (Single Event Gate Rupture), and SEBO (Single Event Burn Out).

2.5.3.1 - Single Event Upset (SEU)

A high-energy ion induces a short-duration pulse of current in a p-n junction, such as the drain region. If the charge collected at the drain of a CMOS storage element (e.g., memory or flip-flop) is sufficient to flip the value of a digital signal, it will change state, and the information that was previously stored will be lost. Energetic Hadrons (> ~20 Mev) cannot deposit enough charge to upset state-of-the-art devices by direct ionization. Nevertheless, their nuclear interactions within the component itself generate recoils that also deposits sufficient charge locally to disturb the correct function.

Single Event Upsets normally refer to bit flips in memory circuits (RAM, latch, flip-flop) but may also in some cases produce transient output pulses in combinational logic circuits. These transients are usually of short duration (about 1 ns), but may indirectly produce changes in the state of other circuits if they occur at critical time periods, such as during clock or data transitions.

Some ways to harden a circuit against SEUs are:

- Reduce the charge that the node can collect by using processes such as SOI (silicon-on-insulator), SOS (Silicon On Sapphire), or bulk epitaxial substrates.[13]
- Increase the charge necessary to upset a memory or latch cell (increasing the capacitance of sensitive nodes).

- Using a modified cell architecture that uses redundancy. A special need is required to guarantee that with smaller transistors the total cell area is not within the strike of a single ionizing particle.
- Reduce sensitivity of analogue circuits to threshold voltage and intrinsic transconductance.

2.5.3.2 - Single Event Snapback (SES)

In an n-channel MOS transistor carrying a large drain current, the parasitic NPN bipolar transistor which has an emitter, base and collector respectively source, substrate and drain of the MOS transistor can be turned on by an avalanche mechanism, which is initiated in the drain junction by an ionizing particle. This will increase the current intensity reinforcing the avalanche mechanism and closing the feedback loop. SES is in most cases related to high supply voltages.

2.5.3.3 - Single Hard Error (SHE)

If a highly energetic particle crosses the gate oxide layer of an MOS transistor, it can deposit a sufficiently large total dose to induce a threshold voltage shift. In an SRAM cell, for example, the subthreshold current of the n-channel transistors can become high enough to block the stored information in the high or low logic state.[14]

2.5.3.4 - Single Event Gate Rupture (SEGR)

This kind of irreversible event consists of the destruction of the gate oxide by an ionizing particle. This problem is especially important in the situation where there is a high electric field on the gate oxide, as for example during the writing or erasing phase of EEPROM (Electrically Erasable Programmable Read-Only Memory) or in power MOSFET devices

2.5.3.5 - Single Event Latch-up (SEL)

The triggering effect resulting from the result of a passing particle could generate a short-circuit (latch) between the power supply and ground. This short-circuit consist on the turning of a parasitic PNPN structure (called thyristor) which can short the power lines. Once latch-up occurs, the node will remain in the high current latched condition until power is removed. This high current may permanently damage devices due to the heat generated by the short-circuit. If power is removed, the circuit can be saved from destruction and can be returned back to the operational condition. Single event latch-up may be limited to a small local region or may propagate to affect large parts of a chip.

However latch-up is only possible if some condition are satisfied [15]:

- The parasitic thyristor must be present (SOI technologies are therefore latch-up free);
- The two parasitic bipolar devices which make a parasitic thyristor must be forward biased;
- The product between the gain of the two parasitic bipolar ($\beta_{npn} \times \beta_{pnp}$) must be higher than one;

- The power supply must be able to furnish the current which is required by the parasitic thyristor.

2.5.3.6 - Single Event Burnout (SEB)

Single event burnout happens when a latch-up occurs and the resulting internal currents heat the latched region to a very high temperature. Such temperature may be sufficient to cause permanent and destructive effects such as electro-migration, burnout of metallization, or degradation of MOS contacts. These effects depend on processing details (such as metallization width, step coverage, and contact technology), and the specific location of the latch-up path [16].

2.5.4 - Resume

Due to the fact that this work will use a sub-micron technology, many of these effects can be discarded. SES need high supply voltages, SHE was a problem in older technologies with thick gate oxide, SEBO is an issue only for power MOSFETs. Also, sub-micron technologies have an intrinsic tolerance to TID effects and CMOS transistors are almost immune to displacement radiation damage. Therefore, in this work the radiation effect that will be most considered most is the single event upset due to being the most likely effect to happen on sub-micron technologies.

2.6 - Summary

In this chapter the effects of charged and neutral particles on matter were discussed. Between the ionizing effects and displacement damage it was seen that in a MOS device ionizing effect was the most damaging. The most sensitive part of a MOS transistor is the gate oxide. After exposure to ionizing radiation electron-hole pairs and new interface states are induced in the Sio2-Si interface. The trapped hole induces a negative threshold voltage shift for both p-channel and n-channel transistors. The radiation induced interface states will degrade the transconductance and the subthreshold slope and will also give origin to a threshold voltage shift. This voltage shift is positive for n-channel devices and negative for p-channel devices thus increasing in module the threshold voltage. For the n-channel transistor the shift and the slope degradation of the threshold caused by the trapped holes can increase the “off-state” current of the device. However, if the shift caused by the new interface traps is higher than the shift caused by the trapped holes, then the overall voltage shift is positive, and therefore the “off-state” current might not increase. On the other hand what gives origin to an increase in the “off-set” current of an n-channel transistor is the creation of parasitic conductive path from source to the drain.

The most common errors induced by Single Event Effects (SEEs) were also presented. SEE generate an immediate malfunction of one or more transistors. These errors can be reversible or non reversible. In the scope of this thesis the most important SEE is the single event upset, which originates non destructive errors. The single event upset causes the modification of the information stored in an elementary memory cell.

Chapter 3

Selection of ADC architecture

Different analogue to digital converter (ADC) architectures are currently available which trade-off performance characterization parameters such as resolution, conversion time, power consumption, and implementation area (and consequently cost). This chapter starts with a brief description of quantization and the A/D converters characteristics. The characteristics and operating principles of different ADCs' architectures, as well as, of the respective domains of application are overviewed with the objective of highlighting then the respective most important figures of merit which are critical to be considered in the selection process. The operating principle and main figures of merit of dual-slope integrating ADCs are presented in detail as this is the architecture that was selected for the converter to be designed.

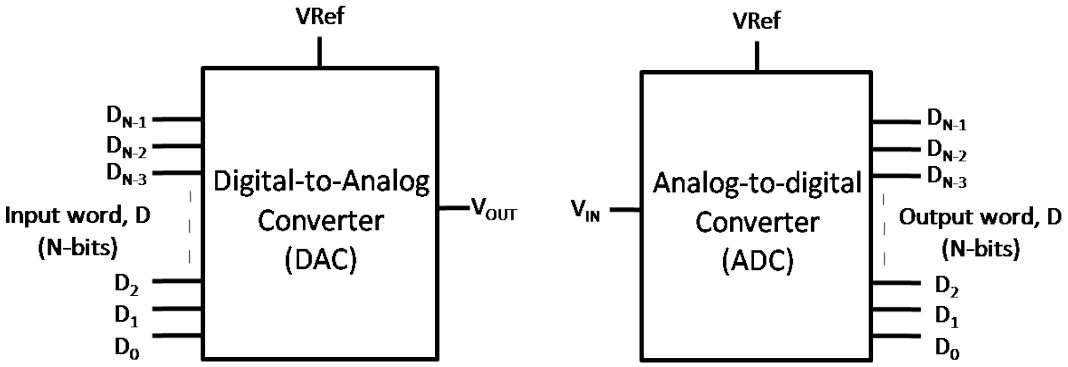

Figure 3.1 – Generic symbol of D/A and A/D converters

Data converters (ADC and DAC) are widely spread functional blocks in practically all electronic systems. They are responsible for translating information between the analogue "real-world" and the most commonly used digital processing domain. For example one of the most popular conversion applications is the digital audio compact disc (CD) players, where stored digital information is converted into audible (analogue) music.

Concerning A/D conversion, the most well known architectures are: flash, two-step sub-ranging, two-step parallel feed-forward, pipeline, algorithmic or cyclic (which actually are similar to pipeline converters but which recycle conversion residues within a single M bit

stage), successive approximation, sigma-delta (or delta-sigma), and integrating. A brief description of their operating principles is presented in section 3.2.

3.1 - Quantization and the A/D converters characteristics

In an A/D conversion process the analogue input signal is quantized into discrete segments, being the number of quantization levels equal to 2^N, where N is the number of output bits. This is not a simple process as it means that a, e. g., 12 bit ADC must be able to detect changes in the input of 1 part in 4096.

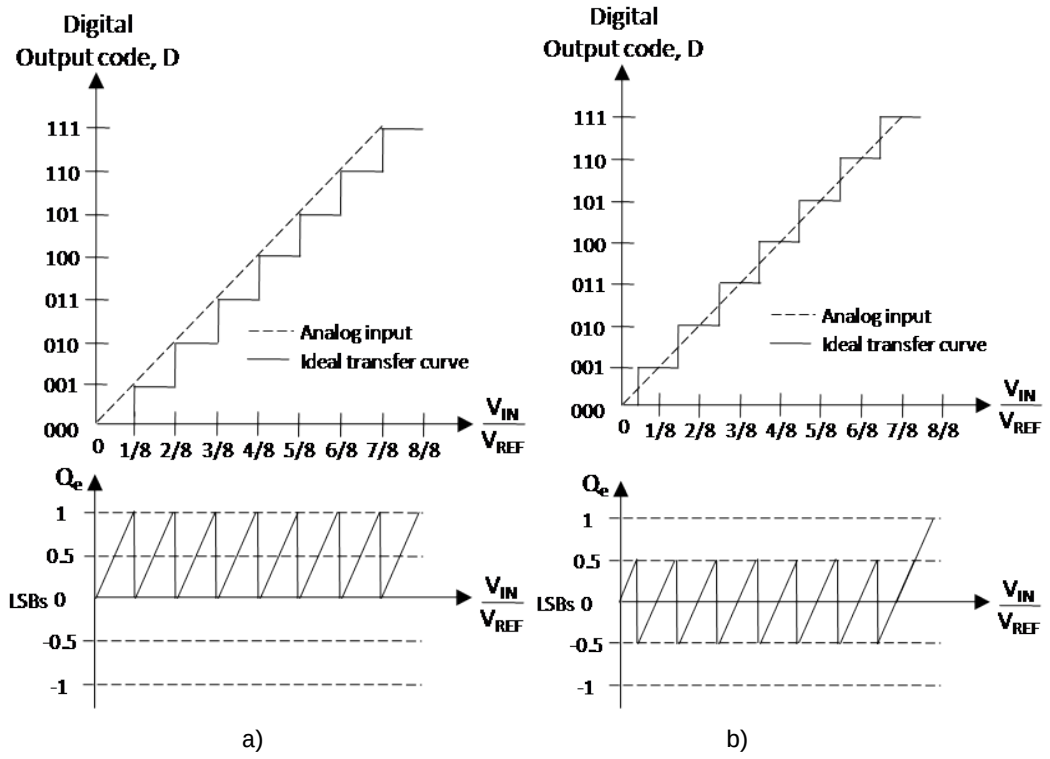

Figure 3.2 - Transfer curve and quantization error for an ideal ADC without (a) and with quantization error centered around zero (b).

Figure 3.2 shows the transfer characteristic, i. e., the digital output code versus the analogue input, Vin, of an ideal unipolar 3 bit ADC. As one can see, the quantization process generates an error (Q_e) whose amplitude is defined by the code-bin width of the Least Significant Bit (LSB). The LSB amplitude represents the smallest change in the analogue input voltage that will modify the output code and can be calculated using

$$1LSB = \frac{V_{REF}}{2^N} \tag{3.1}$$

where V_{REF} defines the quantization range. For example, with V_{REF} equal to 1 Volt and N equal to 3 the LSB is equal to 125mV.

The quantization error (Qe) is thus defined as the difference between the actual analogue input and the discrete analogue value corresponding to the resulting digital output code

$$Q_e = V_{IN} - V_{out} \tag{3.2}$$

with,

$$V_{out} = D.\frac{V_{REF}}{2^N} = D.V_{LSB} \tag{3.3}$$

where D represents the digital output code, and V_{LSB} is the value of 1 LSB in volts.

The quantization error waveform of the 3 bit ADC in figure 3.2 a) shows a sawtooth waveform centered about 0.5 LSB. Ideally, for a linear transfer characteristic, it should be no greater than +1 LSB and no less than 0. However if the Q_e is centered on zero the Q_e would be at most ± ½ LSB and that would be better than the +1LSB. This can be easily achieved by shifting the transfer curve to the left by ½ LSB, as shown in figure 3.2. b).

3.1.1 - Differential Nonlinearity (DNL)

An ADC with non-ideal components may cause the output code differ from the ideal value. This can be seen as a change in the step width of the transfer curve.

The difference between the step width of a non-ideal converter and the ideal step width is known as differential nonlinearity, DNL.

$$DNL = Actual\ step\ width - Ideal\ step\ width \tag{3.4}$$

The DNL indicates how well a DAC can generate a digital output word from uniform changes of multiples of LSBs in the input.

When DNL is equal to -1 LSB it is guaranteed that the ADC will have a missing code, that is, a code that will never be shown at the output. In other hand, an ADC with a DNL greater than +1 LSB may not have a missing code, though in all probability a missing code will occur (figure 3.3) An ADC is said to be monotonic if doesn't have a missing code and increasing input values lead to increasing output codes.

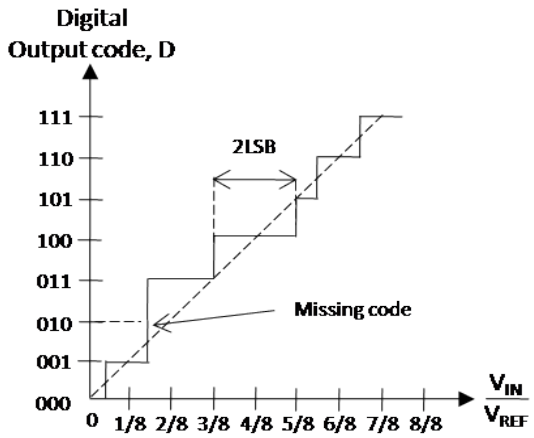

Figure 3.3 Transfer curve of a nonideal ADC, with a missing code.

3.1.2 - Integral nonlinearity

Another ADCs performance characterization parameter is the so called integral nonlinearity or simply INL, which expresses the linearity of the overall transfer curve.

It is defined as the difference between the data converter code transition points and a reference straight line drawn trough the first and last output codes transition.

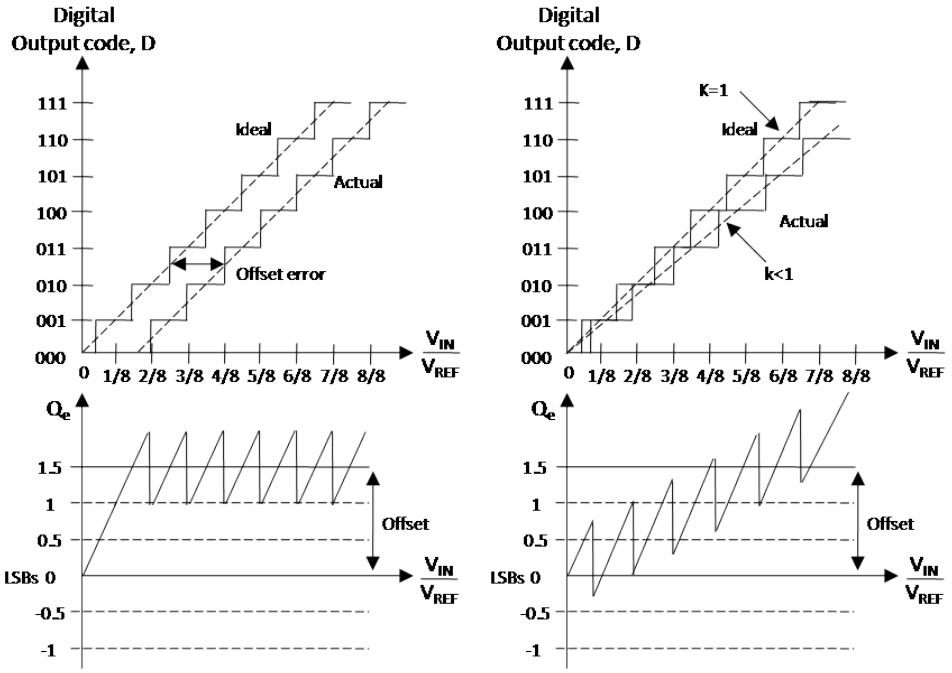

Figure 3.4 - Tranfer characteristic of a non-ideal ADC with offset error and gain error respectively

3.1.3 - Offset and gain error

Offset is the difference between the value of the input for the first code transition and the ideal value of ½ LSB. The quantization error becomes ideal after the initial offset voltage is overcome.

The gain error or scale factor is the difference in the slope of a straight line drawn through the transfer characteristic and the slope of 1 of an ideal ADC. The quantization error will increase over the input range.

3.1.4 - Signal-to-Noise ratio

The signal to noise ratio compares the value of the largest RMS input signal that can be applied to the converter to the RMS value of the output noise.

$$SNR = 20\log\left(\frac{V_{IN\,(max\,)}}{V_{noise}}\right) \tag{3.5}$$

For a sine wave with peak to peak value equal to the reference voltage of the converter the RMS value for Vin(max) is:

$$V_{in(max)} = \frac{V_{REF}}{2\sqrt{2}} = \frac{2^N(V_{LSB})}{2\sqrt{2}} \tag{3.6}$$

The value of the noise for an ideal ADC will be equivalent to the RMS value of the error signal, Q_e

$$Q_{e,RMS} = \frac{V_{LSB}}{\sqrt{12}} \tag{3.7}$$

Therefore the SNR for an ideal ADC can be written

$$SNR = 20\log\left(\frac{\frac{2^N(V_{LSB})}{2\sqrt{2}}}{Q_{e,RMS}}\right) \tag{3.8}$$

Which can be written in terms of N as $SNR = 20N\log(2) + 20\log(\sqrt{2}) - 20\log(2\sqrt{2}) = 6.02N + 1.76$. This equation assumes that the quantization error shows the same sawtooth waveform shown before even when the input signal is not a ramp, however, for a number of bits higher than 8 this approach can be assumed valid as the error is smaller than about 2%.

3.2 - Brief overview of common ADC architectures

The detailed description of the operating principles of each one of the existing ADCs' architectures is avoided here as this is not the purpose of this work and they can be easily found in widely available literature [10, 17]. Nevertheless, it is recommendable to highlight the most relevant aspects which have to be considered when specifying the architecture to be used.

3.2.1 - Flash

Flash or parallel converters are the fastest ones to convert analogue signals into digital of any type of ADC. This architecture utilizes one comparator per quantization level, 2^N resistors and one digital thermometer decoder circuit, where N is the number of bits. The reference voltage is divided into 2^N values, each of which is fed into a comparator. Concurrently, each comparator will compare the input signal with the respective reference and the result renders a thermometer code. The thermometer code will exhibit ones if the input signal is higher than a certain reference and zeros if lower. On each clock pulse the thermometer decoder will produce a new digital coded word that represents the analogue input.

The speed of each conversion is an obvious advantage of this converter, however for each bit of increased resolution the area will double. For a 12-bit converter the number of required comparators is 4095 [17].

3.2.2 - Two Step Flash

The two step flash converter is separated into two complete flash ADCs with feed-forward. The conversion process starts with a first rough estimation of the value of the input, which provides the most significant bits (MSB). Then the result is converted back to an analogue value and subtracted to the original input; the result of the subtraction known as the residue is multiplied and input into the second ADC; this second flash ADC will perform a fine conversion and therefore calculating the least significant bits.

This architecture reduces significantly the area used by an N-bit converter compared to a flash converter. The disadvantage is that the conversion process takes two steps instead of one.

3.2.3 - Logarithmic

Logarithmic circuits are useful in many applications that require nonlinear signal compression, such as in speech recognition front-ends or bionic ears.

Logarithmic circuits are the best option when the input signal source represents physical measurements performed over quantities that can vary over several orders of magnitude and no a priori information is available about their distribution.

The architecture could be divided in three groups. The first can be viewed as the cascade connection of a logarithmic information converter that operates on analogue variables and produces analogue variables, and a conventional (linear) ADC. In the second, the logarithmic converter follows the ADC and, therefore, its input and output are digital signals. In the third, the logarithmic conversion and the A/D conversion are performed by the same structure and cannot be easily distinguished.

More about this subject could be seen in [18, 19, 20].

3.2.4 - Algorithmic or cyclic

Cyclic or algorithmic converters have one comparator, a reference subtracter, and a multiplier with a factor of two. On the first step the input signal is compared with half of the input voltage range. If it is higher it will be subtracted half of the full-scale voltage and then the value will be multiplied by two and the MSB is set to one. In other hand if the signal is in the lower half the MSB is set to zero. In the next cycle the remainder of the previous cycle is used as the input and the process is repeated and in every cycle a new bit is defined.

The conversion time will take N conversion cycles for N bit of resolution.

The cyclic or algorithmic architecture occupy a small die size, and has a very low power consumption with a relative high resolution (in each iteration a new bit is set) but with a drawback of a lower conversion rate [21, 22].

3.2.5 - Pipelined

The pipelined architecture uses the same principle of the cyclic architecture but replicates the cyclic circuit to allow a constant flow of data through each circuit.

For a pipelined converter with a resolution of N-bits only N comparators are needed. The pipelined converter consists therefore of N stages, each one having its own comparator, a

sample-and-hold, a summer, and a gain of two amplifier. Each comparator's output represents a final value of the digital word of the analogue signal.

The main advantage of this kind of converter is that it produces, after an initial latency, a new output value each clock cycle. However this converter must have very accurate comparators to avoid error on the final word.

3.2.6 - Integrating ADC

An integrating converter integrates the input signal and correlates the integration time with a digital counter. At the end of the conversion the counter value is proportional to the input signal and represents the digital value of its amplitude.

3.2.6.1 - Single Slope

The single slope architectures implement a single integration. When a new sample is made the counter is reset and the integration starts. Since the reference value is DC, the integration value will linearly increase with a slope that depends on the gain of the integrator. When the output of the integrator exceeds the sample voltage the counter value is submitted to the output of the converter. And therefore one can read the converted digital word.

Reducing the reference voltage it is possible to achieve very high resolution. However the high resolution is counterbalanced by the time need for such resolution, bigger resolutions needs more conversion time. To conclude a conversion in a timely manner, the clock frequency for the counter must be much higher than the bandwidth of the input signal.

The disadvantage of this architecture is that the output value of the integrator depends not only of the input signal but also on the value of R, C and clock frequency. Such dependency leaves to accuracy problems due to frequency jitters and nonlinearities of integrator's amplifier.

3.2.6.2 - Dual Slope

The dual slope architecture is an upgrade of the previous architecture. It eliminates most of the problems encountered on the single slope.

The conversion process is divided in two, in the first part the input signal is integrated for a stated period of time (2^N clocks cycles, N being the converter's resolution). Then the reference voltage, with opposite sign, is connected to the input of the integrator. The integrator will discharge back down to zero at a constant slope defined by the reference voltage. The time need to discharge the integrator is measured by the counter and it represents the digital output.

Using two slopes that are generated by the same integrator and by the same clock, any non-idealities will essentially be cancelled.

A 12-bit dual slope integration ADC would comprise one operational amplifier, one comparator and a 4096 long counter.

3.2.7 – Successive Approximations

This kind of converter uses a binary search to converge into the digital value of the analogue input. To implanting a successive approximation ADC it is needed one N-bit shift register, one successive approximation register (SAR), a N-bit DAC, and one comparator.

The input signal is sampled and compared to the output of the DAC. The result is then used to indicate the search direction. The input of the DAC is defined by the value of the SAR. At each clock cycle one bit of the output is calculated and can be seen at the output of the SAR.

The successive approximations architecture has become a popular converter architecture because of its simplicity, relatively high speed (one clock for each bit of resolution), good resolution and also a small footprint. One special care must be taken when developing such architecture concerning DAC's accuracy, because if an early error is made by the DAC the converter will attempt to search the quantization level in the wrong half of the binary tree.

A 12-bit successive-approximation ADC would comprise one comparator amplifier, a 13 capacitor array and a 12 bit SAR.

3.2.8 – Sigma-delta Oversampling

Sigma-delta oversampling converters, sample at a rate much higher than the input signal bandwidth. For that reason its use is limited to signals with low bandwidth and when it is required high-resolution. Sigma-delta oversampling converters use digital processing techniques instead of complex analogue components to do the conversion. Derived of the high frequency, switched-capacitor circuits are used and therefore there is no need for sample-and-hold circuits.

This architecture is divided into two separated components: a sigma-delta modulator and a decimating digital filter. The sigma-delta modulator will provide the quantization level in the form of a serial bit stream representing the oversampled signal. This bit stream is then processed. This processing has two main purposes: to filter any quantization noise and to attenuate any false out-of-band signals. Then a decimator removes the oversampled data producing an N-bit serial stream that represents the analogue value.

The advantage of this architecture is that it does not imply the use of an accurate comparator, because the error will be averaged out with the sum of the samples. Other advantage is that the quantization noise is pushed out of the signal bandwidth allowing for obtaining high signal to noise ratios with relatively simple analogue circuitry.

A 12-bit oversampling ADC would comprise one operational amplifier (integrator), 1 bit ADC and a 1 bit DAC and a decimating digital filter.

3.3 – Application domains and figures of merit

In order to get a full perception of each architecture relative position some graphics are now presented.

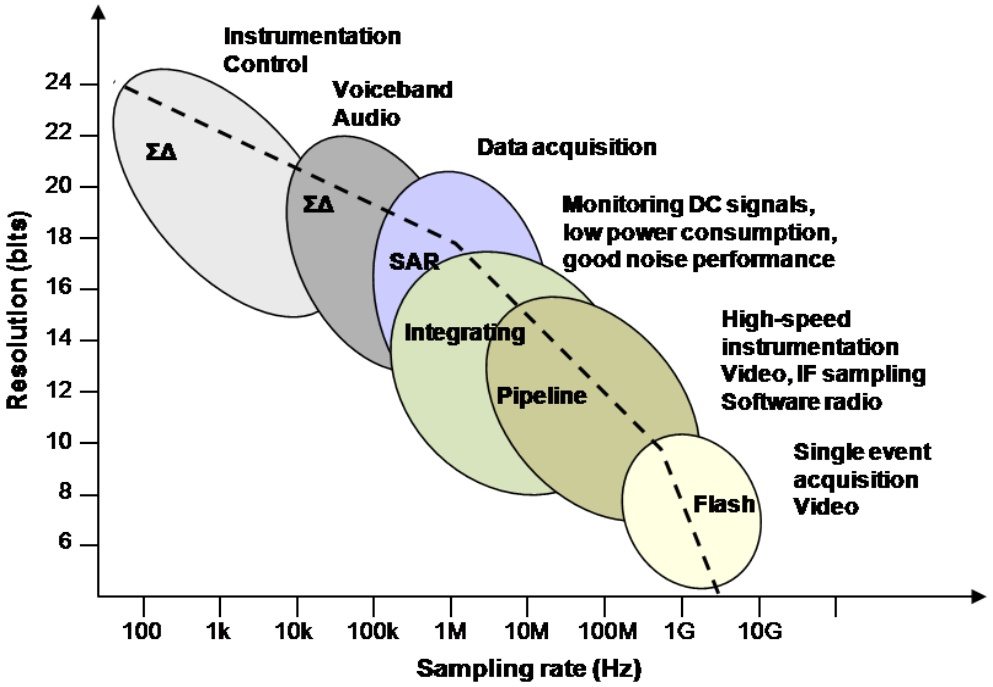

Figure 3.5 - ADC architectures and their position in terms of resolution and sampling rate used in real applications

Figure 3.5 shows the areas of application in terms of resolution and sampling rate of the most widely used ADC architectures.

The successive approximation is mainly used in multiplexed data acquisition systems and also in many instrumentation applications. The sigma-delta architecture is applied in many industrial measurements applications that can go from energy-monitoring to motor control applications. The sigma delta is also utilized in voice band audio application due to the ease of adding digital function to this architecture. Examples of such application are the stereo compact disc or even for DVD audio.

Pipelined architectures can be seen in applications like high definition TVs, digital cameras and also radar and telecommunication applications.

Integrating ADCs are expected to be found in noisy industrial environments and applications for which high update rates are not required due to their ability to reject high-frequency noise and fixed low frequencies such as 50Hz or 60Hz.[23].

More information about this subject can be found in [24].

Some graphical representations of some figures of merit are now presented.

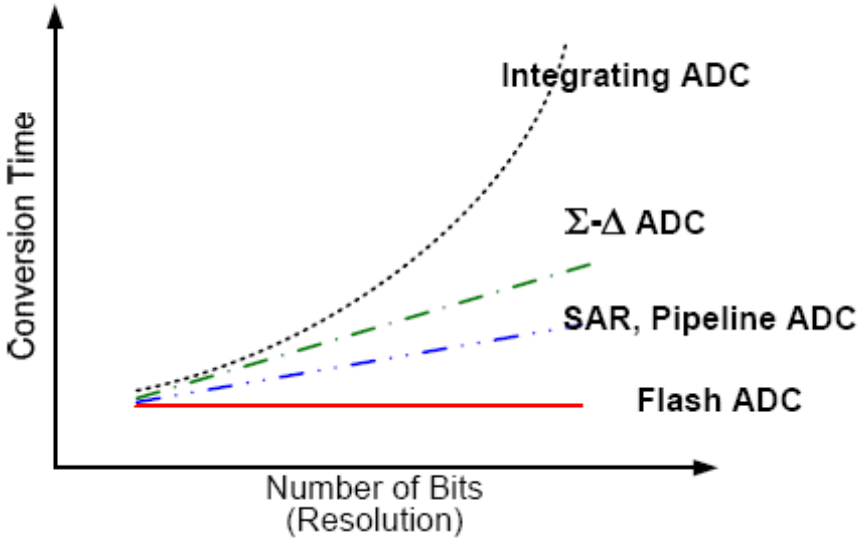

Figure 3.6 - Conversion time versus resolution of different ADCs' architectures

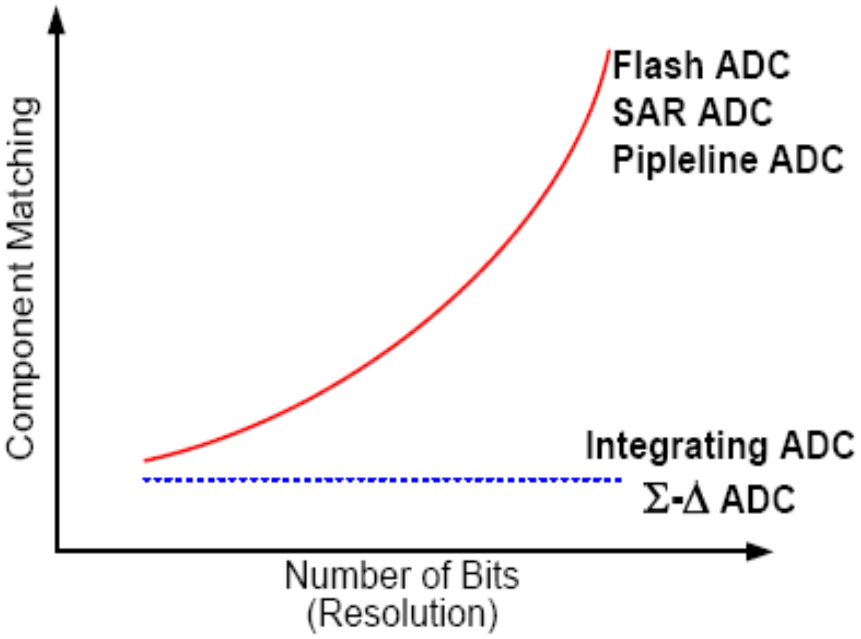

Figure 3.7 - Requirements in terms of accuracy and components' matching

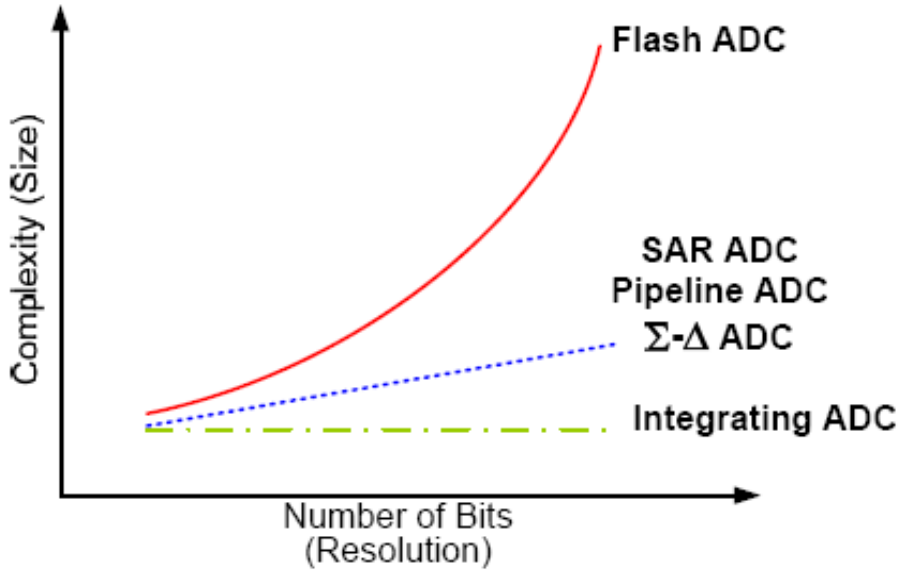

Figure 3.8 - Implementation complexity of different ADCs' architectures.

3.4 - Specifications

The circuit to be designed should present the specifications in table 3.1. It will be designed with a 130 nm commercial technology with radiation hard techniques applied during the schematic and layout phases.

Table 3.1 - Circuit specifications.

Resolution	12 bits
Supply voltage	0 – 1.2V
Clock	40Mhz
Temperature	30°C to 80°C
Input range	GND - 1 Volt
Input channels	17

3.5 - Architecture decision

After knowing the specifications of the ADC to be designed and using the information above it was decided to implement a dual slope architecture in this work. That decision was taken due the high accuracy that can be achieved for low frequency inputs [25], the good noise rejection of a dual slope architecture [26] the inherent offset cancellation and the low complexity (Figure 3.8) and the low matching concern (Figure 3.7) of the circuit. This ADC architecture will be presented now in more detail.

3.6 - Operating principle of the dual-slope integrating converter

In this section the main operating principles of the chosen dual slope architecture are explained, as well as an identification of some of the critical issues that are expected to be present during the design process.

3.6.1 - High level description of the conversion process

A circuit schematic of typical dual slope converter like those presented in [27, 28, 29] is shown in Figure 3.9.

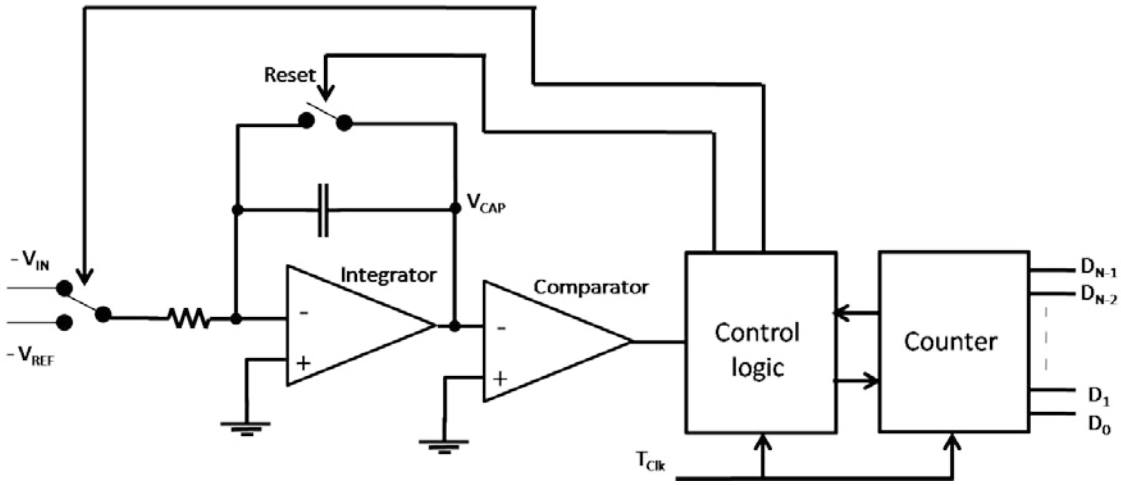

Figure 3.9 - Schematic of a typical dual slope ADC converter.

As it can be seen the circuit is composed by a first block where the input signal is integrated and by a second block where the result of the integration is compared with ground. The product of this comparison will command the control logic which has as objective to control the switches and the counter.

To better understand the conversion process Figure 3.10 shows the capacitor output waveform of the node V_{CAP} during one conversion cycle.

The conversion is divided in two distinct phases. On the first phase, charging phase, the input signal is applied to the integration block producing a voltage ramp whose slope is proportional to the input voltage. This phase has a specific duration which corresponds to the time needed for the counter to reach is maximum value.

$$T_1 = 2^N T_{CLK} \tag{3.9}$$

And the voltage at V_{CAP} at the end of the charging phase can be written as:

$$V_{CAP} = \frac{|V_{in}| \cdot T_1}{RC} \tag{3.10}$$

At this point the counter is reset and the second phase starts.

During the discharging phase a constant voltage, with opposite signal, is applied into the integration block. This will cause the voltage in the V_{CAP} to drop with a constant slope. Eventually after some time (T_2) it will reach the ground, changing the comparator output. The change at the comparator output will make the control logic to stop the counter.

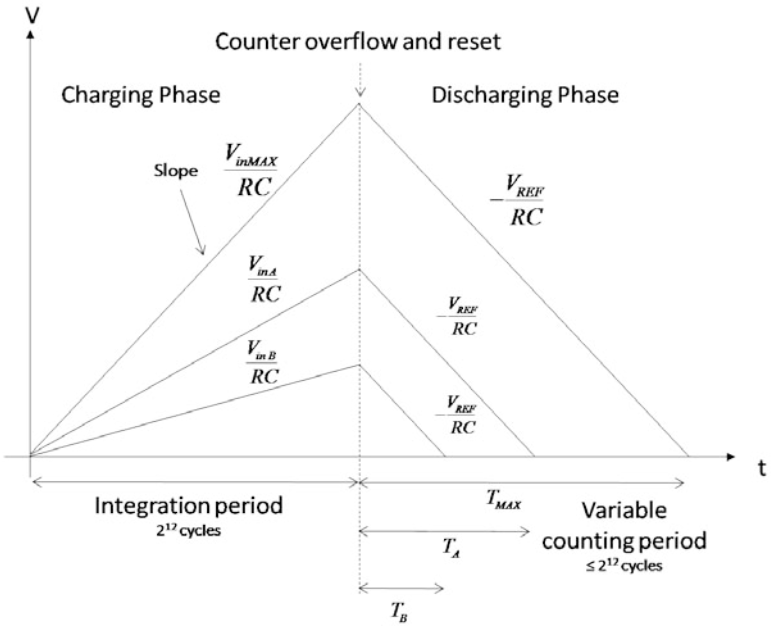

Figure 3.10 - Capacitor output waveform

When V_{CAP} reaches ground,

$$V_{CAP} = \frac{|V_{in}| \cdot T_1}{RC} - \frac{V_{REF} \cdot T_2}{RC} = 0 \tag{3.11}$$

which can be simplified to,

$$T_2 = T_1 \cdot \frac{|V_{in}|}{V_{REF}} \tag{3.12}$$

Because of the fact that the first phase has a constant time T_1, the time of the second phase will be directly proportional to the input signal as can be seen with equation (3.12). Furthermore the counter which has incremented 2^N during T_1 and D during T_2 will represent, at the end of T_2, the digital word of the analogue input signal, as equation (3.13) shows.

$$\frac{D}{2^N} = \frac{|V_{in}|}{V_{REF}} \tag{3.13}$$

where D is the counter output value at the end of a conversion cycle.

3.6.2 - Identification of critical issues in the design process

The dual slope architecture is an improvement from the single slope architecture. Due to the fact that it uses a single integration block for both charging and discharging phases nonlinearities that may appear due to capacitor and resistor deviations are cancelled as the values of these components do not affect the final counting.

Nevertheless the dual slope has some peculiar problems that will be exposed in this section.

For each conversion cycle the comparator must change its state twice, one in the beginning when the voltage V_{CAP} starts to rise, and at the end when the V_{CAP} returns to zero. This will work for any input voltage between GND and VDD. However, for Vin equal to zero no current will be applied. If the current in the capacitor is zero V_{CAP} will not change its value and therefore does not change the value of the comparator. To circumvent this problem a current offset that will flow continuously must be added.

Other problem is the nonlinearity of the amplifier for low input voltages. To avoid this nonlinearity an amplifier with a common mode input range that covers all input swing must be chosen.

Capacitive charges with a nonlinear behavior must be minimized. One example of where those nonlinear capacitances might appear is at the transmission gates that will control de current flow from and to the capacitor. Therefore one must be aware when designing the transmission gates.

Chapter 4

Design of the 12 bit Dual-Slope Integrating Converter

In this chapter the design of the converter is presented. First a block diagram of the circuit is drawn. Later the working parameters such as charging current, maximum VRAMP voltage, discharge current are idealized. The conversion cycle is fully described.

4.1 - The 130 nm CMOS Technology

This project will be implemented in a commercial CMOS technology of 130 nm lithography.
With each scaling down of the technology it is possible to achieve for the same amount of logic a smaller circuit, i.e. cheaper and faster circuits, with lower power consumption and as it was seen earlier, that can provide some radiation tolerance. The drawbacks are a slightly increase in the 1/f noise, a higher leakage and a reduced voltage swing due to the lower supply voltage. The basic features of the technology are given in Table 4.1

Table 4.1 - Technology features.

VDD	1.2V
Gate oxide thickness	2.2nm
Process	Twin-well CMOS
Device isolation	Shallow trench isolation
Interconnectivity	5 to 8 levels of metal
Polysilicon gates doping	Dual (n+ and p+)

4.2 - Building Blocks

In this section the schematic of the ADC is presented. To simplify that task the circuit was divided in small building blocks. The design of each block is explained in the following sections.

4.2.1 - Overall Block Diagram

The architecture implemented does not follow the typical dual slope architecture that was shown in Figure 3.9. The reason is that in the typical architecture to create the down slope, a voltage reference (VREF) with the opposite signal of the maximum input voltage is needed. In the technology used in this work such reference voltage (in this case should be of -1V) was impossible to apply due to the fact that the supply voltage is 0 to 1.2V. Other reason is that the in typical architecture the input node must be able to provide the charging current. In this case and to minimize the introduction of nonlinearities, it was chosen to apply the input voltage directly in the block responsible for driving the charging current.

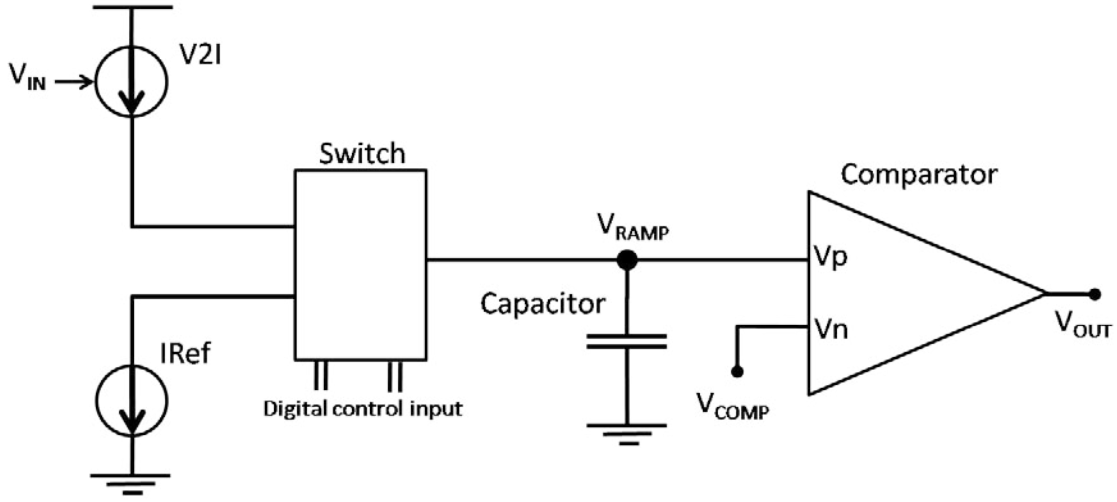

Figure 4.1 - Block diagram of the analogue part of the converter

As can be seen in the Figure 4.1 the circuit is made of a 5 blocks/elements. The V2I (voltage to current) block (Section 4.2.2) is responsible for generating a current proportional to the input voltage. Another block, IRef (Section 4.2.3) will deliver a constant discharge current. A switch (Section 4.2.4) will provide a soft change between currents. Those currents will charge and discharge a capacitor (Section 4.2.5) creating a voltage ramp (V_{RAMP}) at the capacitor input node. A comparator (Section 4.2.6) will compare the value of the V_{RAMP} node with a reference voltage V_{COMP}.

The circuit was design to be mainly one source dependent, i.e., all the signals are referred to ground. This was intended to minimize the effects of any variation in the source voltage. Naturally, for PMOS mirrors VDD is used as reference.

4.2.2 - V2I Block

This block has the function of generating a current proportional to the input voltage and it must maintain it constant despite the voltage variation at the output.

In typical dual slope architectures this block corresponds to the integration block, whereas the input voltage is applied to a resistor creating a current that eventually will be applied to a capacitor. The problem of that configuration is that the input signal should be able to provide the charge current while maintaining its value unchangeable. In this case the input voltage is applied to a high impedance node, i.e. the input of the amplifier.

In Figure 4.2 it can be seen the first schematic of this block and it is shown to allow a better understanding of main operating principles and then to compare the evolution made during the project.

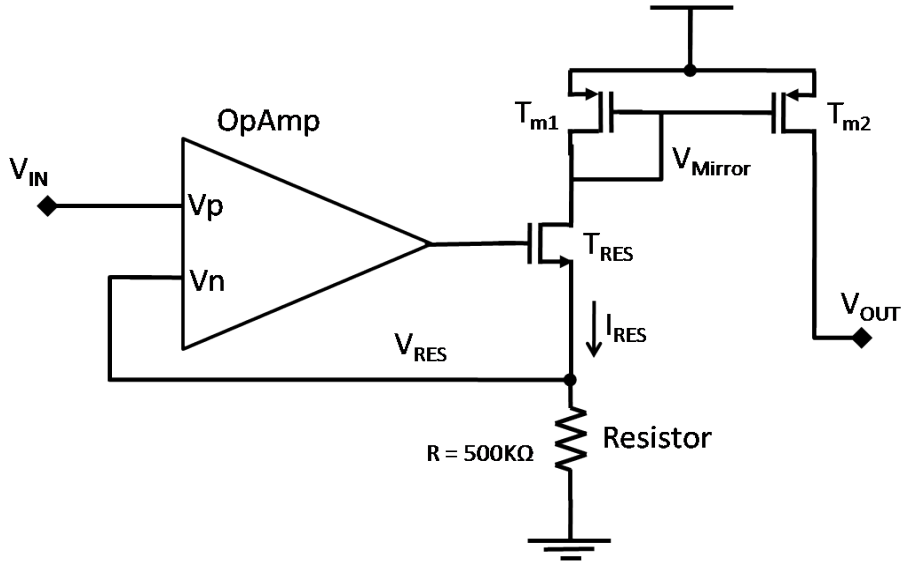

Figure 4.2 - First schematic of V2I block.

The amplifier in a voltage follower configuration will reproduce at the node V_{RES} the input voltage. A current $I_{RES}=V_{RES}/R$ will flow from V_{RES} to ground through the resistor and since $V_{RES} = V_{IN}$ the current will be directly proportional to V_{IN}.

The V_{RAMP} voltage must increase with the current generated in this block, however the I_{RES} current flows in the opposite way to do that. A current mirror (T_{m1} and T_{m2}) was therefore implemented thus generating the current (I_{V2I}) necessary to charge the capacitor.

This was the first draft of the circuit, but some problems were identified then. These are described below as well as the adopted solutions.

- The output of this circuit will be connected to the capacitor input whose voltage V_{RAMP} is expected to swing from 0 to 1 Volt. Such swing will affect significantly the current generated by the mirror (T_{m1} and T_{m2}). The current I_{V2I} will decrease with the increase of the V_{OUT} voltage. This happens because the drain to source voltage will start to differ between the two mirror transistors (T_{m1} and T_{m2}). To avoid such difference a regulated cascode was implemented [30].
- Other problem was the nonlinearity of the amplifier for voltages very close to ground. The solution was to insert an offset to the input voltage in the order of a few tens of milivolts just to allow a small current to flow through the resistor and to switch on the transistor (T_{RES}). The way that was found to offset the input voltage was to introduce a single stage amplifier known as common drain or source follower

amplifier. To obtain an offset voltage of just a few tens of milivolts, a low threshold voltage transistor was used. The drawback of this implementation was that it introduced a nonlinearity, i.e., the offset failed to be maintained constant with the increasing input voltage. The offset voltage decreased roughly 40mV for an input swing from 0 to 1Volt.

- To try correcting this nonlinearity and because the important was to maintain the linear relationship between V_{IN} and V_{RES}, another source follower amplifier was introduced between the node V_{RES} and the inverting input of the amplifier (V_N) reducing thus the offset nonlinearity to a few hundreds of microvolts along the whole input swing.
- Resuming, this offset generator has two transistors in the source follower configuration, one connected between to V_{IN} and V_P and the other linking V_{RES} to the V_N node. This offset allows the amplifier to working in the linear region.
- With the add of the second transistor it was also possible to add an offset current (already mentioned in 3.6.2). This offset current will allow the correct operation of the dual slope conversion when V_{IN} equals zero. The change needed to introduce such current was to make the offset of the V_{RES} voltage just a little lower than the other offset. Because of the voltage follower configuration of the operational amplifier the inverting and noninvertig will have the same voltage. So for a V_{IN} voltage equal to zero an offset voltage will be applied at the inverting input setting thus the same voltage in the noninverting input. Because of the fact that the T_{ofsRES} transistor has an offset lower than the T_{ofsIN} transistor the voltage in V_{RES} will be higher than the input voltage. This will generate an offset current even for an input voltage V_{IN} equal to zero.
- In a common drain configuration the value of the offset is the value for V_{GS}. Thus accordingly to equation 4.1, which is a rearrangement of the I_D-V_{DS} characteristic in the saturation region for a CMOS transistor, it is possible to conclude that are two ways of lowing VGS.

$$VGS = \sqrt{ID * \frac{L}{W} * \frac{1}{2} * \mu_n * Cox} + V_t \qquad (4.1)$$

- One possibility is decreasing the drain current (ID) and the other is modifying the aspect ratio of the transistor. To minimize eventually mismatched effects the option chosen was to reduce the drain current on the T_{ofsRES} transistor.

- Another problem was to set the current on a fixed value due to eventual mismatches occurred during the fabrication process. To circumvent this problem the resistor will have several small resistors in parallel with fuses. This will allow for adjusting a more accurate and desired value for the charging current after fabrication

Figure 4.3 shows the actual schematic of converter.

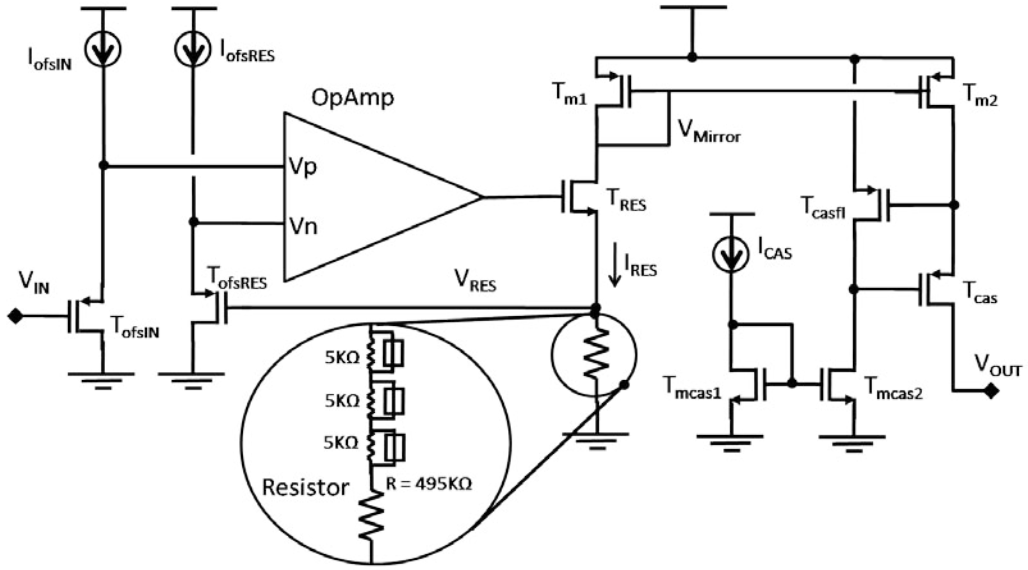

Figure 4.3 - Actual schematic design of the V2I block

This block has also some unsolved problems. On the first's corner simulations where supply voltages of 1.08 V and 1.65 V and temperatures of -20 degrees and 100 degrees were applied the linearity achieved for ideal condition was affected. Some modifications in the transistor aspect ratios were made and some improvement was achieved, at least the current generated was starting to have a linear behavior for input signals in the middle of the full range swing. In the far end, i.e. for input voltages lower than 100 mv, the voltage VREF was not following Vin. This is still far away from the acceptable and therefore more work should be done.

Some research about rail-to-rail OpAmp had been carried out [31, 32, 33] in order to change for the dual stage OpAmp. It was not changed yet because a rail-to-rail OpAmp has a more complex architecture which may lead to more nonlinear effects and because every improvement on the existent circuit is welcome.

4.2.3 - IRef block

This block will generate the constant current that will discharge the capacitor. The current I_{cref} is a reference current which will be copied by the current mirror T_{mi1}, T_{mi2} generating the discharge current I_{REF}. Like the V2I block this circuit should maintain the current I_{REF} constant while the output voltage decreases from 1 Volt to 150 mV. Such constant current is achieved by the cascode transistor T_{REF} and the OpAmp which keeps the drain voltage V_{REF} close to the V_{MIR} voltage.

The schematic of the circuit IRef is presented in Figure 4.4.

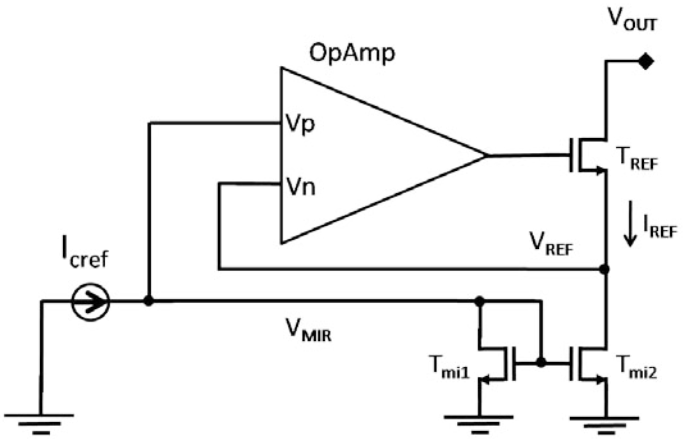

Figure 4.4 - Iref schematic

This block has shown a good performance within DC simulations. In fact the decrease in the DC current when the Vout voltage was swept from 1 to 100mV was only of 100pA.

The strength of the dual slope architecture is on using the same current generator and capacitor for both charging and discharging phases. Until now the V2I block was incapable of obtaining the performance of the IREF block. If despite the efforts to achieve it the V2I doesn't improve it will be necessary to change this IREF block for one capable of reproducing a current similar to V2I current.

4.2.4 - Switch block

This block has the function of swapping between the currents which are applied to the capacitor. On the first approach to this block it was used four transmission gates that would swap the charge current (I_{V2I}) from the capacitor input to ground, and the discharge current (I_{REF}) from VDD to the capacitor input. This was made to minimize the voltage variation when changing the switches between the nodes V_{RAMP} of each current generator and the capacitor input voltage (V_{RAMP}). The first schematic can be seen in Figure 4.5.

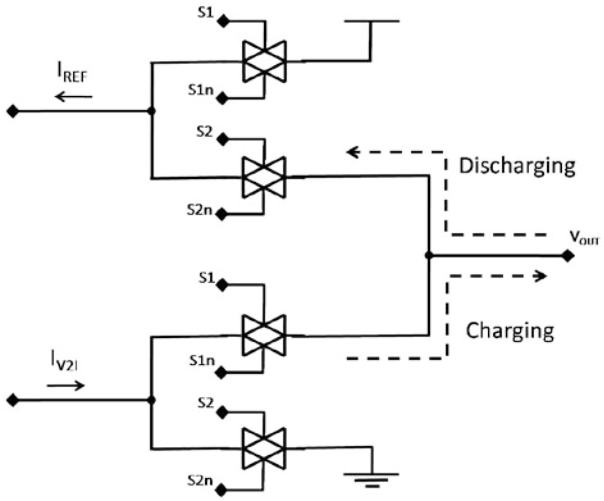

Figure 4.5 - First schematic of the switch block

However after the first simulations the V_{OUT} voltages variation at the moment of changing the state of the transmission gates was still large, roughly 2 mVolts

To decrease further the voltage variation another scheme was implemented. This new circuit allow the current to follow the V_{RAMP} voltage even when it is not directly connected. This improvement was made by connecting an OpAmp in a voltage follower configuration between the V_{RAMP} node and the I_{REF} node, as it can be seen in the Figure 4.6. The OpAmp was only inserted in the discharging node because the other node is switched outside the conversion time not influencing the conversion process. With this circuit a soft transition with a step of only 140microvolts was achieved.

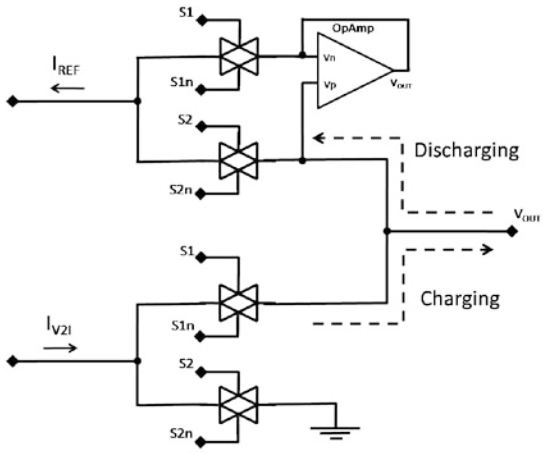

Figure 4.6 - Final schematic of the switch block

4.2.5 - Capacitor block

This block has only one component, a capacitor. A high capacitance is needed to allow the charging during the whole time. Because of that and to try minimizing the area the capacitor will be made by using a dual metal to metal capacitor.

4.2.6 - Comparator block

To avoid the non-linearity of the current source when the output voltage is near ground, the reference voltage of the comparator will not be 0V precisely but a little higher around 100-150mV, just enough to maintain the current source on the linear range.

This comparator will be a clocked based comparator like the one presented in [17 p. 919]

4.3 - Dual slope function

In this section a more detailed description of the implemented dual slope conversion process is presented.

The conversion process is divided in three different phases. In the pre-charge phase the capacitor is charged until the V_{RAMP} voltage is near to V_{COMP}. The second phase, the integration phase, the capacitor is charged with a current that is directly proportional to the input voltage. During the last phase, the discharge phase, the capacitor is discharged with a

constant current until V_{RAMP} crosses the reference voltage. A graphical representation of the conversion process for two different inputs is shown in Figure 4.7.

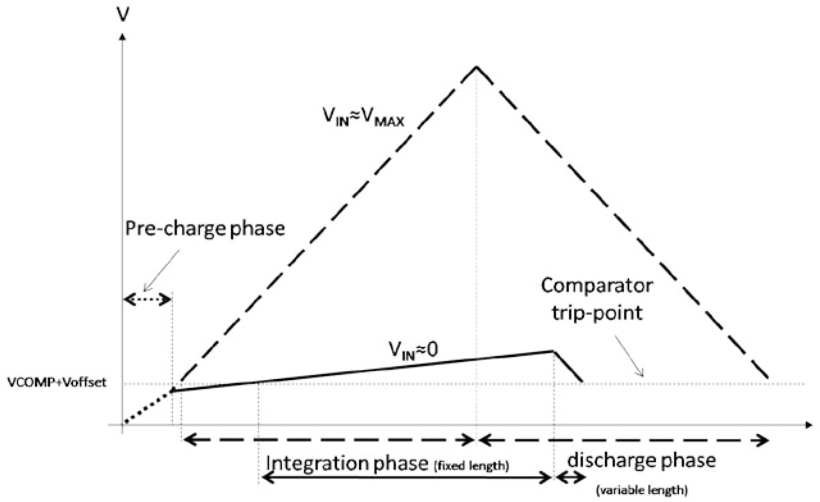

Figure 4.7 - Graphical representation of the conversion process for two different inputs.

4.3.1 - Pre-charge phase

The objective of this phase is to set the V_{RAMP} voltage near the trip point of the comparator, which is the reference voltage V_{COMP} plus the offset voltage (V_{offset}) of the comparator. This step is essential to minimize the conversion time because if the input voltage is close to ground the current generated by the V2I block will be small and therefore it will take a long time just to get to the trip point and effectively start the conversion. The details of this phase are now described.

It is assumed that at start the voltage at the capacitor is equal or close to zero. A reference "charge voltage" is then applied to the input of the V2I block generating a constant current, which is proportional to the applied voltage. This current will charge the capacitor increasing the V_{RAMP} voltage until it is near but still below to the trip point value of the comparator (V_{COMP}+V_{offset}).

The value for the number of clocks used in this phase is stored in a register in the digital part of the circuit. This register will be updated after the first calibration. The proceedings of this first calibration are: 1) apply the current defined by the reference charge voltage to the capacitor; 2) count the number of clocks needed to achieve the comparator trip point; 2) Subtract to that number some cycles to guarantee that the trip point is not reached during these phase; 3) the result is stored at the register. If in the following conversion cycles and during the time defined in the stored value the trip point is reached the time spent until that point is stored into the register and the phase is interrupted. To start again the conversion process V_{RAMP} must be set to ground by using the discharge current.

To avoid the case where the value stored in the register is low enough to still increase considerably the conversion time, a maximum time is defined to the between the end of this phase until the trip point of the comparator. After counting the clocks stored in the register and if the trip point is not reached then the second phase begins.

4.3.2 - Integration phase

During this phase the input signal is applied to the V2I block thus generating a proportional current that will charge the capacitor. Since in the last phase the V_{RAMP} voltage was set to a value close to the trip point of the comparator, any current generated by the V2I block should change the comparator state in a reduced amount of time. If that does not occur in a defined time it means that the time for the pre-charge phase was too short and therefore all conversion cycle must be restarted.

Only after the trip point is crossed the counter will start counting a fixed number of clock cycles, 2^{12}= 4096 clocks to be precise. During this period the current is continuously applied to the capacitor, increasing the V_{RAMP} voltage with a slope proportional to the input voltage. At the end of this integration phase the V_{RAMP} voltage will be an integrated value of the input voltage.

4.3.3 - Discharge phase

In this phase the constant current generated by the IRef block will discharge the capacitor leading to a constant slope decrease in the V_{RAMP} voltage. A counter will count the clock cycles needed until the V_{RAMP} voltage passes through the trip point of the comparator.

It is straightforward to see that for different V_{RAMP} values the time to reach the trip point will vary and it will be directly proportional to the input voltage.

In the end the value presented at the counter will represent the input voltage plus an offset value, created by the offset current generated in the V2I block. Therefore one more step must be accomplished before having the correct digital representation of the input signal.

This last step will remove from the counter value the corresponding digital value of the offset voltage created by the offset current. This value was previously calculated and stored in a register.

4.3.4 - Working parameters

During the first approach to determine the working parameters it was decided that the maximum charge current and discharge current (with opposite signal) would be of 2 µA and the V_{RAMP} voltage would vary between 0 to 1V. However and because it was impossible to keep constant currents with a voltage swing reaching the rail voltage, it was decided to define the comparator reference voltage to 100mV.

A high V_{RAMP} swing will ease the job of designing the comparator because one LSB will be higher and therefore easier to detect by the comparator.

$$1LSB = \frac{\Delta V}{2^{12}} = \frac{0.9}{2^{12}} = 219.72\mu V \tag{4.2}$$

Using equation 4.3 derived from the capacitor charging equation it was possible to calculate the capacitance needed to make differences of 1 LSB voltages in V_{RAMP} appear spaced by one clock cycle at the end of the discharging phase.

$$C = \frac{I \times \Delta t}{\Delta V} \tag{4.3}$$

where C is the capacitance of the capacitor, I the discharge current, Δt the clock period and ΔV is the voltage corresponding to 1 LSB at the V_{RAMP} node.

The calculated value for the capacitance was 227.56pF. This value was not suitable for a metal to metal capacitor because the area needed would be greater than permitted. However the technology has the option of a dual metal to metal capacitor which has the double capacitance per area thus reducing the area to the allowed range. Otherwise the charge current would be increased.

The introduction of the offset current will create an offset voltage in the V_{RAMP} node at the end of the integration phase. The voltage V_{RAMP} should not be higher than 1 Volt due to the fact that for higher voltages the p-type current mirror which charges the capacitor will start to behave in a nonlinear way. The voltage V_{RAMP} at that moment can be described as

$$V_{RAMP} = V_{COMP} \pm V_{offset} + \Delta Vin + \Delta offset \tag{4.4}$$

where V_{offset} is the comparator offset voltage, ΔVin is the voltage that corresponds to the integration of the input signal and Δoffset is the voltage caused by the integration of the offset current.

V_{COMP} and the V_{offset} voltage can be seen as constants because they are established before the integration cycle.

The ΔVin can be calculated as

$$\Delta Vin = \frac{Vin \times t}{RC} \tag{4.5}$$

where t is duration of the integration phase. The term Δoffset is simply

$$\Delta offset = \frac{Voff \times t}{RC} \tag{4.6}$$

where Voff is the V_{RES} voltage when the input signal is equal to zero.

After fabrication the only way to adjust ΔVin and therefore calibrate the converter is by changing the R value (by fusing the fuses). However it can be seen that changing R will also affect Δoffset in the same way. This can have a negative impact since with the increase of Δoffset the increase of ΔVin swing is limited. To avoid this problem the current responsible to set the offset voltage in the T_{ofsRES} transistor will also be configurable.

4.4 - Calibration algorithm

After fabrication and due to the mismatches the converter may not be working properly. A simple way to calibrate the currents was proposed in section 4.2.2. Now a calibration algorithm is presented:

1. The input signal is set to ground and a conversion starts. This will give the offset created by the offset current. This offset should be around 200 clock cycles if it is lower jump to 4.
2. The input signal is set to its maximum and another conversion cycle starts. At the end and after subtracting the offset calculated in the previous step, the value obtained should be equal to the maximum value. However, initially that might not happen and the value will be greater than 2^{12} clock cycles. This occurs because of the mismatches and because the resistor was projected to have an initial small but changeable value. If the value is higher than 2^{12} clock cycles jump to three if it is equal jump to five.
3. The resistor must be increased by fusing one of the fuses thus generating a lower current. Return to the step one.
4. Increase the current in the T_{ofsRES} transistor and thus increasing the offset. Jump to the step one.
5. The converter is calibrated!!

Chapter 5

Implementation details and layout

The layout phase was not reached during this work. However some research was made to find out which radiation hardening techniques should be applied during this phase. Those techniques will be explained in this chapter. Some radiation hard devices are presented in Section 5.5. Later in section 5.6 some techniques for digital logic are listed.

For a radiation effect point of view the commercial 130 nm technology is not very sensitive to some radiation effects, however to increase the radiation tolerance of the circuit various recommendations are made in section 5.7. More detailed information can be found in [34]

5.5 - Radiation hard devices

In this section some transistors with a radiation hard topology are presented. These transistors are intended to reduce or even eliminate the post-irradiation parasitic leakage current. This current path could either be inside the N-channel devices or between adjacent transistors. An effective way of cancelling the NMOS device-to-device leakage current is implementing systematically guard rings. Two types of guard-rings can be seen in [35]

5.5.1 - "Gate surround transistor"

A new NMOS layout structure for radiation tolerance has been proposed in [36] where the polysilicon gate is doped with different types (N or P-types). Using the two doping types available for poly it is possible to change the threshold of the transistor and in that way creating an isolation. They suggest the use in the edges of NMOS gate p-type doping rather than n-type. That means that to turn on and start to contribute to the transistor current the region under P-type doping needs a gate bias higher than the one in region under the N-type doping. Then it is possible to apply a gate voltage that only turns on the central region covered by N-type poly leaving the edges (P-type doped region) turned off. For such gate voltage and if the P-type doped region surrounds the transistor source and drain, it will isolate the drain and source from their surroundings, preventing radiation induced leakage currents. One important fact is that to maintain the radiation tolerant characteristic the gate

voltage cannot be higher than the threshold voltage needed to turn on the P-doped gate region. An image of this transistor can be seen in Figure 5.1.

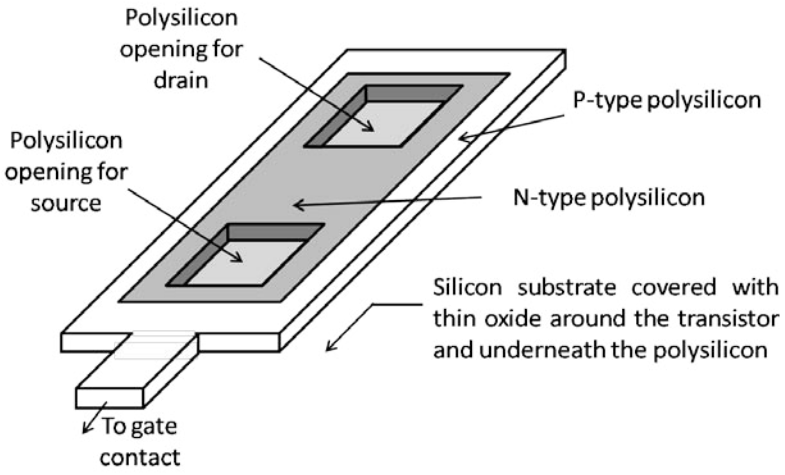

Figure 5.1 – Layout of the gate surround transistor. The opposite type of polysilicon at the edge of the polysilicon gate provides a means to eliminate radiation induced transistor leakage. The thin oxide underneath the polysilicon limits radiation induced threshold shifts and will guarantee continued correct operation after ionization.

5.5.2 - Enclosed Layout Transistor (ELT)

In the Enclosed Layout Transistor or edgeless transistor, the parasitic path which connects the drain to the source is eliminated. Figure 5.2 represent a NMOS ELT layout.

The ELTs have been used since the early days of CMOS, and their effectiveness in preventing leakage currents in irradiated circuits is well known. However this kind of layout has some drawbacks that are now listed below.

- Consume of area (less density);
- Increase in the gate and source or drain capacitances;
- Difficulties in modelling the W/L ratio;
- Lack of symmetry;
- Limitations in the choice of the W/L ratio

5.5.2.1 - Modelling the W/L ratio

ELTs can have many different shapes, e.g. square, octagonal, square with the corners cut at 45 degrees. In [37] a model for the layout shown in Figure 5.2 is presented.

This particular layout, with the corners cut at 45 degree, is compatible with the design rules of many commercial deep submicron technologies. The dimension c is kept small and constant varying L, making the current flowing mainly in two orthogonal directions and ensuring a better uniformity.

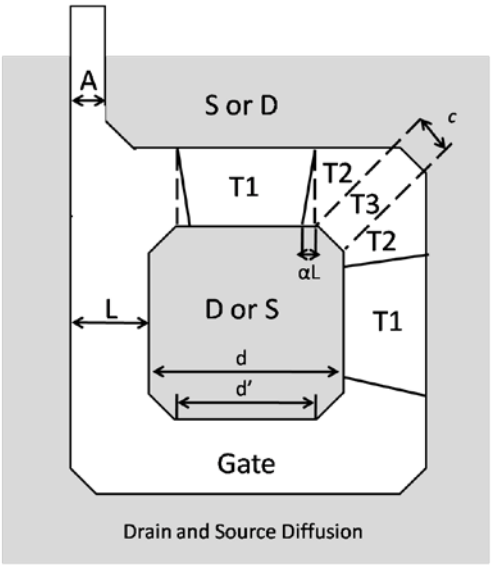

Figure 5.2 - ELT shape. The transistor can be thought of as being formed by three kind of transistors (T1,T2,T3) in parallel.

The following formula is used to know the right dimensions to layout an ELT transistor with a given aspect ratio,

$$\left(\frac{W}{L}\right)_{eff} = 4\cdot\overbrace{\frac{2\alpha}{\ln\frac{d'}{d'-2\alpha L_{eff}}}}^{T1} + 2K\cdot\overbrace{\frac{1-\alpha}{\frac{1}{2}\sqrt{\alpha^2+2\alpha+5}\cdot\ln\frac{1}{\alpha}}}^{T2} + 3\cdot\overbrace{\frac{\frac{d-d'}{2}}{L_{eff}}}^{T3} \qquad (5.1)$$

where c, d, d' = d – c·√2 and α are shown in Figure 5.2. L_{eff} is used in the formula to take into account for the gate length shortening due to under-diffusion, photolithography and etching. K is a geometry dependent parameter, used to take into account the number of transistor T2 present in the ELT (Figure 5.2), as it will better explained later. α is a fitting parameter which is needed to identify the borderline between transistors T1 and T2. It is not possible to know a priori the value of α and its value is only extrapolated after fitting with the experimental data however after some tests made in different technologies α has been found to be almost technology independent with a value of 0,05.

The formula is divided in three parts (T1, T2 and T3) and each one correspond to the different three areas T1 T2 T3 which are represented in the Figure 5.2.

The first term T1 corresponds to the linear edges of the transistors, the second to the corners without the 45 degrees cut, which is taken into account separately from the third part. Due to the presence of the polysilicon strip (length A in the figure), necessary to integrate the gate contact to the outside of the thin gate oxide region, the third term is only multiplied by 3. The parameter K, geometry depended, have the value 7/2 for short channel devices (L< 0.5μm) and 4 for longer devices.

5.5.2.2 - Limitations in the choice of the W/L ratio

It should be notice that ELTs can't have aspect ratios lower than a certain value. This is due to the fact that the only way to lower the aspect ratio is to increasing L keeping d at its minimum. It can be seen that after a certain value of L, term 2 dominates over terms 1 and 3, thus not allowing lower aspect ratios than 2.26. Furthermore values close to this also imply a considerable waste of area in comparison to standard transistors, and should in fact be avoid by using different circuit topologies. For high aspect ratios it is sufficient to stretch the device in one or two dimensions without changing the corners, and therefore the calculation of the aspect ratio will be straightforward (only T1 term is affected).

5.5.2.3 - Lack of symmetry

In an ID vs VDS plot of a saturated transistor where it should be a flat line it can be seen a certain slope. This slope is due to the fact that the drain current depends on the drain voltage along the effective channel lengths – the channel length modulation effect. This slope corresponds to the transistor's output conductance.

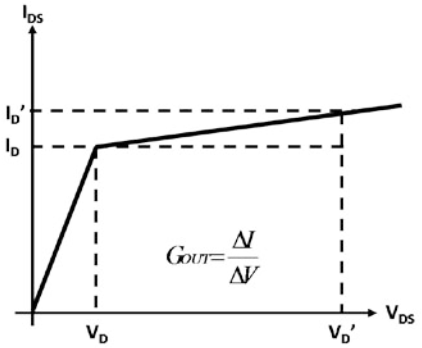

Figure 5.3 - ID vs VDS and definition of the output conductance.

In Figure 5.3 it can be seen an idealized output characteristic of a MOS device, where V_D is the drain voltage which has to be applied to put the device in saturation mode and ID is the correspondent drain current. As shown in the figure the output conductance Gout can be expressed by the ratio between ΔI and ΔV. Since the drain current is inversely proportional to the gate length, it can be easily shown that Gout is can be expressed by the equation

$$G_{out} = \frac{I_D}{\Delta V} \cdot \frac{\Delta L}{L - \Delta L} \tag{5.2}$$

It is possible to conclude from equation 5.2 that, for the same drain current and drain voltage, increasing L decreases the output conductance which means a more stable saturation current.

Due to the fact that the ELT gate is annular, the drain contacts can be chosen inside or outside of the ring gate, and the same is obviously applied to the source. However the non-symmetrical geometry between the drain and source will cause an asymmetric output conductance. Measurements have shown that the drain inside output conductance (GDI) is higher than the drain outside output conductance (GDO). This can be explained by the fact that the distance ΔL between the pinch off point and the drain, due to the conservation of the space charge region for the same bias potentials, is smaller when the drain is outside. The

asymmetry between GDI and GDO increases with L as the outer perimeter increases while the outside doesn't. The GDO and GDI of ELTs were also compared with the output conductance of linear devices GDL. The conclusion show that for L < 0,5 μm GDL ≈ GDI, while for larger gate lengths GDL values are near the arithmetic mean of GDI and GDO values. Therefore the output conductance achievable with ELTs is smaller (i.e. better) than for normal devices when the drain is connected outside. Other important asymmetry is the inner terminal capacitance which is smaller than the one of the outer terminal. This results in a trade-off between speed and gain in designing amplifiers with ELTs. One final remark is that the extra capacitances in the outer terminal decrease the sensitivity to SEU.

5.5.3 - Other transistors approaches

The ELT transistor is the safest layout for a radiation tolerant approach, nevertheless others layout schemes have been used in the past. In Figure 5.4 it can be seen two of those schemes in pair with the "traditional" layout of a NMOS transistor and the parasitic leakage path of each one.

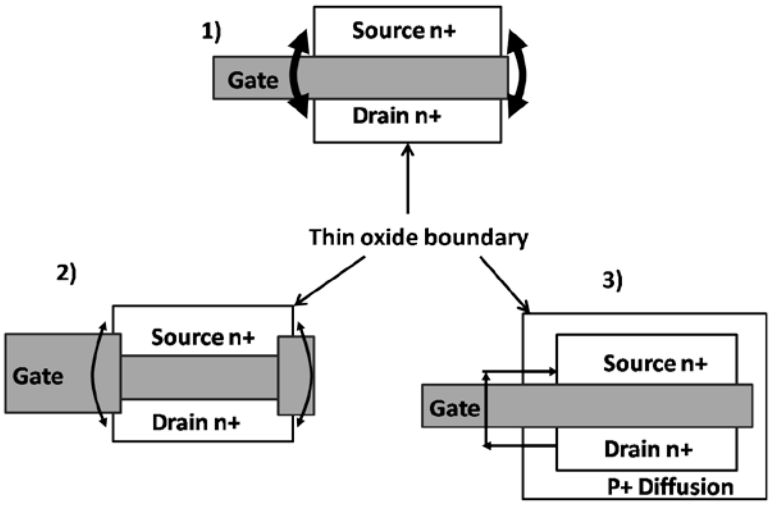

Figure 5.4 - Layouts of the standard transistors, and two others radiation tolerance approaches

Solution 2 consist of the increasing the length at the edges of the gate, therefore increasing the distance between the drain and the source for the parasitic devices thus decreasing the leakage current. In solution 3 the area of the thin oxide is defined by a mask (p+ in the figure) and only inside this thin oxide region the transistor is defined. This approach allows keeping the transistor geometry similar to the traditional transistor, but it is not suited to be used in commercial processes since it violates some design rules and it does not eliminate the leakage current path. More about these approaches can be seen in [38, 39]

5.5.4 - Resume

For this work and more specifically in the layout phase it will be used the ELT transistor presented in section 5.5.2. The formula to deduct the W/L ratio will be very useful to lay out transistors with the characteristics specified in the schematic phase. In order to improve the

gain or the speed of the transistor it should be taken into account the asymmetries present in the ELT.

5.6 - Radiation hard techniques in digital circuits

Three radiation hard techniques that can be implemented when designing digital circuits are described here.

5.6.1 - Charge dissipation

Charge dissipation is one of the techniques that could lower the risk of SEU effects. In this technique one should increase the transistor bias current. The principle is that higher currents will dissipate the effect of a charged particle therefore not allowing a high voltage shift. This technique has the drawback of increase substantially the power consumption which when multiplied by several digital cells in a digital circuit could have a significant negative impact in the overall power. To avoid such scaling in the power consumption instead of increasing power it is possible to increase the sensitive nodes capacitances. The capacitance only needs to be high enough to absorb the energy without increasing too much the voltage, keeping in that way the same logic state. This second approach will obviously decrease the speed of the circuit but with the advantage of low power consumption.

5.6.2 - Spatial redundancy

Another technique, so called spatial redundancy, relies on the use of redundant logic. This implies the use of at least three or more copies of the sensitive block plus a voting block. The result of the voting block is equal to the value of the majority of the inputs. So if a radiation induced particle hit one of the sensitive nodes changing its value the change will not affect the correct behaviour of the circuit because the value will be discarded in the voting block. Therefore this does increase the effective tolerance to radiation by reducing the probability of multiple nodes being hit by one particle. However more space has to be used to allocate extra blocks.

5.6.3 - Temporal filtering

In the temporal filtering technique a voting block is needed as in the last technique. However, instead of copying the same logic block to obtain independent inputs for the voting block, the logic state of the sensitive node is delayed by different paths. By delaying differently each path a radiation induced voltage shift will arrive at different times at the voting block thus keeping the output with the correct state. The drawback is the increase of the time to voting due to the delay in the logic path.

5.7 - Radiation tolerance Layout guidelines

In this section some guidelines are presented under a form of recommendation and should be taken into account when designing analogue circuits. These recommendations are a

summary of the results presented in [34] where the commercial 130 nm technology used in this work was tested in order to clarify how much radiation tolerant it is.

5.7.1 - Core transistors

Due to transistors' thin oxide layer a good tolerance to total dose is achieved, still NMOS transistors show some degradation in their subthreshold regime. This degradation affects the characteristics of the weak/moderate inversion and the leakage current. To minimize this problem one should follow these guidelines:

- Do not use lengths smaller than 0.8 µm (NMOS) and 0.4 µm (PMOS), and remember that narrower transistors have a larger voltage threshold shift;
- Limit the use of linear transistors in weak/moderate inversion, replacing them with ELTs;
- When designing ELTs keep it in mind that equation (7.1) can be use but has an accuracy of 10%;
- Small aspect ratios NMOS transistors that are for example used in current mirrors should have linear layout rather than "ringed" layout.

5.7.2 - Transistors with very low currents

The leakage currents between NMOS transistors is very small, thus only transistors with very low currents (10-100 nA) should be surrounded by a guard ring.

5.7.3 - N-wells

The N-wells that should have a guard ring are those which are not connected to Vdd, those which have an inside PMOS transistor carrying a small current, and even those whose neighbour NMOS transistors are carrying a small current. Any other N-wells don't need a guard ring.

5.7.4 - Resistors

The diffusion resistor can safely be used, and guard ring must be provided only if they are projected to carrying small currents.

5.7.5 - Forward-biased diodes

Forward-biased diodes should be STI-bound, should be used at maximum possible current density and should be laid out with the maximum area/perimeter ratio.

5.7.6 - I/O transistors

This type of transistors is very sensitive to total dose radiation. More precisely when both NMOS and PMOS (linear or "ringed") are exposed to larger doses they show significant threshold voltage shift. Therefore the considerations for I/O transistors are:

- Do not use transistors narrower than 1 µm;

- Avoid linear transistors in weak/moderate inversion;
- Avoid I/O transistors for applications where the expected total dose exceeds 1-2 Mrads.

Chapter 6

Conclusion

Radiation environments such as those found in space missions, satellites, advanced weaponry, instrumentation for nuclear power plants and high energy physics applications can alter the behaviour of electronic devices. The reason for that is that radiation induced particles interact with the materials of the devices changing their characteristics. Therefore one should take special care when designing electronic circuits for radiation environments to avoid the damages caused by radiation effects. Such protection can be provided by using dedicated radiation tolerant manufacture processes. However these radiation tolerant processes are more expensive and less developed than state of art commercial technologies. Furthermore, the scaling down of the technology improved the radiation tolerance of the circuits due to the decreasing of the gate oxide thickness.

This had motivated the study of radiation tolerant design and layout techniques to be used in deep submicron commercial technologies. Those studies have revealed that using such techniques not only radiation tolerant circuits were achieved but they do also benefit from the low power, low cost, high density and high yield that state of art technologies have to offer.

The scope of this work was the designing of a 12-bit analogue to digital converter built in a 130 nm deep sub-micron technology using radiation tolerant techniques. The dual slope ADC architecture was chosen amongst others to be implemented. The reasons that lead to this choice were the high accuracy for inputs with low frequency, the good noise rejection ratio, the offset cancellation scheme and the low complexity.

To ease the designing phase, the circuit was divided in small blocks, and each block was projected draw and tested separately before the integration in the top level.

When projecting the schematic some problems start to appear, some were related with nonlinearities (current mirrors) and others due to the impossibility of cascading several transistors (rail-to-rail OpAmps). The solution was to use low threshold voltage transistors and to apply low power techniques.

However this designing phase took more time than expected and in fact the project had only recently moved to the corners simulation. It was seen that the first approach didn't work in extreme conditions like those in the corners simulation. Despite the fact that a great improvement was made to limit the nonlinearities the point where the nonlinearities might be acceptable was not yet reached. Therefore more work should be done.

Looking at the start of the project and considering the objectives proposed then one can conclude that some objectives were not accomplished. However the main objective was to learn which are the best ways of improving the ADC's radiation tolerance characteristics, using a commercial CMOS technology. And in fact not only that was achieved but knowledge about low power operation and radiation effects was also acquired. This knowledge will be very useful on the following steps of the design of the radiation tolerant 12 bit analogue to digital converter.

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