FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO

Study of an electrolyzer as a Grid-Forming Load

Ivo Manuel Salgado Mendes



Mestrado em Engenharia Eletrotécnica e de Computadores

Supervisor: Prof. Rui Esteves Araújo

October 31, 2026

© Ivo Manuel Salgado Mendes, 2026

Study of an electrolyzer as a Grid-Forming Load

Ivo Manuel Salgado Mendes

Mestrado em Engenharia Eletrotécnica e de Computadores

October 31, 2026

Resumo

O panorama energético global nos países mais desenvolvidos atravessa atualmente uma profunda transição, a qual é caracterizada pela integração massiva de Fontes de Energia Renováveis Variáveis e pelo desmantelamento de centrais convencionais baseadas em combustíveis fósseis. Esta mudança de paradigma origina nas redes elétricas uma massificação de interfaces eletrónicas, tendo como consequência uma redução significativa da inércia típica dos sistemas de energia elétrica tradicionais. Estas mudanças tecnológicas na rede elétrica tornam a operação do sistema elétrico mais suscetível a fenómenos de instabilidade e ao risco de colapso do sistema. Embora a produção de hidrogénio (H_2) verde via eletrólise da água seja um vetor possível para a descarbonização do setor energético, os sistemas de eletrólise atuais operam predominantemente como cargas passivas, não contribuindo ativamente para a estabilidade da rede elétrica.

Esta dissertação propõe o estudo e a validação de um eletrolisador com controlo do tipo *Grid-Forming* (GFM), posicionando a carga como um dispositivo ativo capaz de contribuir para estabilizar a rede elétrica. Os trabalhos de investigação mais recentes consideram a tecnologia de Membrana de Troca de Protões (PEM, do inglês *Proton Exchange Membrane*) com mais potencial para o fornecimento de serviços de rede, devido à maior dinâmica de operação face à tecnologia assente na eletrólise alcalina. A arquitetura de conversão de potência proposta consiste num par de conversores *Active Front End* em configuração *master–slave* para o estágio AC/DC e um conversor abaixador entrelaçado para o estágio DC/DC, o qual foi dimensionado para cumprir com os requisitos de corrente elevada e baixa ondulação (*ripple*) da corrente contínua que alimenta o eletrolisador.

A metodologia de investigação baseia-se em simulação, com o objetivo de analisar o comportamento dinâmico do sistema de conversão de potência, sob controlo GFM, que alimenta um eletrolisador PEM.

Os resultados obtidos evidenciam que a arquitetura de controlo GFM com coordenação *master–slave*, na qual apenas o conversor *master* executa o controlo por *droop* e partilha a sua referência de corrente com o conversor *slave*, permite que os dois conversores operem de forma coordenada e acompanhem as referências de potência ativa e reativa em toda a gama de operação. Perante perturbações de tensão e de frequência na rede, o sistema responde de acordo com o previsto pelas leis de *droop*, contribuindo para o suporte da rede.

Palavras-chave: Controlo *grid-forming*; Carga *grid-forming*; Hidrogénio verde; Eletrolisador PEM; Controlo por *droop*; Conversor abaixador entrelaçado

Abstract

In the most developed countries, the energy landscape is currently undergoing a profound transition, which is characterized by the massive integration of Variable Renewable Energy Sources (VRES) and the decommissioning of conventional fossil-fuel-based power plants. This paradigm shift brings a widespread deployment of power electronic interfaces into electrical grids, resulting in a significant reduction of the inertia typical of traditional power systems. These technological changes make power system operation more susceptible to instability phenomena and to the risk of system collapse. Although green hydrogen (H_2) production via water electrolysis is a possible vector for the decarbonization of the energy sector, current electrolysis systems predominantly operate as passive loads, without actively contributing to grid stability.

This dissertation proposes the study and validation of an electrolyzer with Grid-Forming (GFM) type control, positioning the load as an active device capable of contributing to grid stability. The most recent research considers Proton Exchange Membrane (PEM) technology to have greater potential for the provision of grid services, owing to its faster operating dynamics compared with Alkaline Electrolysis (AEL) technology. The proposed power conversion architecture consists of a master–slave pair of Active Front End (AFE) converters for the AC/DC stage and an Interleaved Buck Converter (IBC) for the DC/DC stage, which was sized to meet the high-current and low-ripple requirements of the DC current supplying the electrolyzer.

The research methodology is based on simulation, aimed at analyzing the dynamic behavior of the grid-forming-controlled power conversion system feeding a PEM electrolyzer.

The results show that the GFM control architecture with master–slave coordination, in which only the master converter executes the droop control and shares its current reference with the slave converter, enables both converters to operate in a coordinated manner and to track the active and reactive power references across the full operating range. Under grid voltage and frequency disturbances, the system responds as predicted by the droop laws, contributing to grid support.

Keywords: Grid-forming control; Grid-forming load; Green hydrogen; PEM electrolyzer; Droop control; Interleaved buck converter

UN Sustainable Development Goals

The United Nations Sustainable Development Goals (SDGs) provide a global framework to achieve a better and more sustainable future for all. It includes 17 goals[1] to address the world's most pressing challenges, including poverty, inequality, climate change, environmental degradation, peace, and justice.

In the context of this dissertation, the study of grid-forming control strategies for power converters interfacing a hydrogen-producing electrolyzer system contributes directly to the fulfillment of the global targets established by the United Nations, with particular relevance to the following specific goals:

SDG 7 Ensure access to affordable, reliable, sustainable and modern energy for all

SDG 9 Build resilient infrastructure, promote inclusive and sustainable industrialization and foster innovation

SDG 13 Take urgent action to combat climate change and its impacts

SDG	**Target**	**Contribution**	**Performance Indicators and Metrics**
7	7.2	Improving the grid-supporting capabilities of converter-interfaced hydrogen production facilitates the integration of renewable energy sources.	Renewable energy share in the total final energy consumption.
9	9.4	Proposes a control architecture that supports the retrofit of hydrogen production infrastructure with cleaner, grid-friendly technology.	CO_2 emission per unit of value added.
13	13.2	Supporting the reliable integration of renewable-fed hydrogen production contributes to reducing dependence on fossil fuels.	Total greenhouse gas emissions per year.

[1] `https://sdgs.un.org/goals`

Acknowledgements

I would like to begin by thanking Prof. Dr. Rui Esteves Araújo, for recognizing my potential and for the guidance and dedication with which he supervised this dissertation from its earliest stages to its conclusion.

I am equally grateful to FEUP, which was my second home for five years of my life, and which shaped not only my technical formation but also who I am today, always assuring me an education of the highest excellence.

To my colleagues at Lab 205, thank you for all the support and companionship throughout this journey, and for making the long hours in the lab feel considerably shorter. A special word of thanks goes to Miguel Canas, MSc, who, beyond that companionship, was always available to help and offer scientific advice whenever it was needed.

To my parents, thank you for your unconditional support, for always believing in me even when I doubted myself, and for giving me the roots and confidence to pursue this path. I would also like to thank the rest of my family, for their support along the way.

Finally, to my friends, thank you for being part of this beautiful journey and for making it so much lighter, one step at a time.

Ivo Manuel Salgado Mendes

"Develop a passion for learning. If you do, you will never cease to grow."

Anthony J. D'Angelo

Contents

1 Introduction **1**
- 1.1 The Paradigm Shift in Power Systems . . . 1
- 1.2 Green Hydrogen Production and Electrolyzer Technologies . . . 2
- 1.3 Motivation: The Concept of Grid-Forming Loads . . . 2
- 1.4 Objectives . . . 3
- 1.5 Dissertation Structure . . . 4

2 State of the Art **5**
- 2.1 Electrolyzer Technologies and Dynamic Modeling . . . 5
  - 2.1.1 Water Electrolysis and the PEM Technology . . . 5
  - 2.1.2 Static and Dynamic Modeling of PEM Electrolyzers . . . 7
- 2.2 Power Electronic Conversion Stages for Hydrogen Electrolyzers . . . 8
  - 2.2.1 The AC/DC Stage: Converter Topologies for Grid-Connected Electrolyzers 8
  - 2.2.2 The DC/DC Stage: Converter Topologies for Electrolyzer Interfacing . . 10
- 2.3 Control of Inverter-Based Resources: Grid-Following and Grid-Forming . . . 13
  - 2.3.1 Grid-Following and Grid-Forming Control Paradigms . . . 13
  - 2.3.2 Grid-Forming Control Strategies . . . 15
  - 2.3.3 Comparative Analysis of Control Strategies . . . 18
- 2.4 Ancillary Services and Grid Codes . . . 19
  - 2.4.1 Ancillary Services Overview . . . 19
  - 2.4.2 Fast Frequency Response (FFR) . . . 20
  - 2.4.3 Virtual Inertia . . . 20
  - 2.4.4 Low-Voltage Ride-Through (LVRT) Requirements . . . 21
  - 2.4.5 Feasibility of Ancillary Services Analysis . . . 22

3 System Design and Control Implementation **23**
- 3.1 System Architecture Overview . . . 23
  - 3.1.1 Test Scenario Definition . . . 24
- 3.2 Grid and Transformer Model . . . 24
- 3.3 AC/DC Stage: Grid-Forming Converter and Master–Slave Operation . . . 26
  - 3.3.1 Power Measurements and Passive Component Sizing . . . 26
  - 3.3.2 Droop Control . . . 29
  - 3.3.3 Virtual Impedance for Current Limitation . . . 31
  - 3.3.4 Voltage and Current Control . . . 33
  - 3.3.5 Master–Slave Coordination . . . 36
- 3.4 DC/DC Stage: Interleaved Buck Converter Design and Control . . . 37
  - 3.4.1 Electrolyzer-Equivalent Load Characterization . . . 38
  - 3.4.2 Component Sizing . . . 39

3.4.3 Control Architecture 43
3.5 Final Model 45

4 Results and Analysis **46**
4.1 Control Validation of the AC/DC Master–Slave Operation using a DC Source . . 46
4.1.1 Objective 46
4.1.2 Initialization 47
4.1.3 Test Setup 48
4.1.4 Test Results 49
4.2 Current-Control Validation of the DC/DC Stage 52
4.2.1 Objective 52
4.2.2 Initialization 53
4.2.3 Test Setup 53
4.2.4 Test Results 55
4.3 Full System Operation 58
4.3.1 Normal Operation 58
4.3.2 Voltage Fault 62
4.3.3 Frequency Event 67

5 Conclusions and Future Work **71**
5.1 Conclusions 71
5.2 Future Work 73

References **75**

List of Figures

1.1 Green hydrogen production scheme. 2

2.1 Schematic representation of a PEM electrolysis cell. 6
2.2 Dynamic EEC of a PEM electrolyzer cell including the double-layer capacitance effect. 8
2.3 Schematic representation of the typical topology of the AFE. 10
2.4 Schematic representation of an IBC with 3 parallel phases connected with the electrolyzer [17]. 13
2.5 Representation of Grid-Following control architecture. 14
2.6 Representation of Grid-Forming control architecture. 15
2.7 Simulated response of a GFM electrolyzer to a load step. The red dashed curve illustrates the virtual inertial response, where the electrolyzer rapidly reduces its power consumption proportional to the RoCoF, effectively dampening the frequency deviation (blue curve). 21
2.8 Equivalent circuit of a GFM electrolyzer during a grid voltage dip. 22

3.1 System architecture overview. 24
3.2 Simulink implementation of the AC grid representation. 25
3.3 Block diagram of dq-component and power computation from the master converter's three-phase measurements. 29
3.4 Implementation of the P–f droop control loop. 30
3.5 Implementation of the Q–V droop control loop. 31
3.6 Implementation of the Virtual Impedance control for current limitation, adapted from [31]. 32
3.7 Implementation of the outer voltage control loop, including low-pass filtering of the measured voltages and PI controllers used to regulate the d- and q-axis voltage components. 34
3.8 Implementation of the inner current control loop, including decoupling and feedforward terms, as well as PI controllers used to generate the d- and q-axis modulating voltages. 35
3.9 Implementation of the current follower strategy for the slave converter. 36
3.10 Simulated waveforms of the Interleaved Buck Converter: (top) the three interleaved branch currents, i_{LP1}, i_{LP2}, and i_{LP3}; (middle) the electrolyzer stack voltage, V_h^{dc}; and (bottom) the combined output current, I_h^{dc}. 42
3.11 Control architecture of the Interleaved Buck Converter. 43
3.12 Final model developed on Simulink. 45

4.1 Simulink implementation of the isolated AC/DC test setup. 48

4.2 Time-domain tracking of the scripted active power reference, $P_{ref,script}$, by the combined master and slave converter output, $P_{meas,total}$, throughout the four-quadrant test of Table 4.1. The converter pair accurately tracks each of the four commanded active power levels ($+0.6$, $+0.2$, -0.5, and -0.2 pu). 49
4.3 Time-domain tracking of the scripted reactive power reference, $Q_{ref,script}$, by the combined master and slave converter output, $Q_{meas,total}$, throughout the four-quadrant test of Table 4.1. The reactive power reference is commanded through four distinct levels ($+0.2$, $+0.5$, -0.2, and -0.4 pu), each combined with a different active power set-point, allowing the Q–V droop response to be assessed independently of the active power operating point. 50
4.4 Grid frequency, f_{grid}, measured from the voltage at the PCC throughout the four-quadrant test. Despite the large active power reference transitions commanded to the master converter (Table 4.1), the frequency remains within 20 mHz of nominal, $f_{nom} = 50$ Hz, confirming that grid synchronism is preserved across the full P–Q operating envelope. 51
4.5 Summary of the seven steady-state operating points commanded during the four-quadrant test (Table 4.1), plotted on the P–Q plane and colored by quadrant (Q1–Q4). 52
4.6 Simulation of the isolated DC/DC test. 53
4.7 Power circuit of the Interleaved Buck Converter, showing the three parallel buck branches (DC-DC Phase 1–3) and their gating signals (G_{P1}–G_{P3}). 54
4.8 Current-control structure of the IBC. 54
4.9 Output-current tracking over the full run. 55
4.10 Detail of the output-current response to the initial $0 \rightarrow 625$ A reference step. . . . 56
4.11 The three interleaved branch currents, i_{LP1}, i_{LP2}, and i_{LP3}, over a short, switching-period-scale window at a steady-state operating point. 56
4.12 Output current under the $\pm 20\%$ load steps, over the full run. 57
4.13 Detail of the output-current response to the load steps. (a) corresponds to the $+20\%$ increase and (b) to the -20% decrease. 58
4.14 Three-phase terminal voltages of the converters under the constant reference $P_{ref,script} =$ 0.5 pu. (a) corresponds to the master (Star) and (b) is related to the slave (Delta). 59
4.15 Three-phase terminal currents of the converters under the constant reference $P_{ref,script} =$ 0.5 pu. (a) corresponds to the master (Star) and (b) is related to the slave (Delta). 59
4.16 Modulation index of the master converter. 60
4.17 Combined active power delivered by the master and slave converters, $P_{meas,total}$, tracking the scripted reference $P_{ref,script} = 0.5$ pu, with no discernible steady-state error. 60
4.18 DC measurements at the DC bus, which corresponds to the input of the IBC. (a) represents the voltage and (b) represents the current. 61
4.19 Voltage (a) and current (b) at the terminals of the electrolyzer-equivalent load. V_h^{dc} settles close to the intended 400 V design value. 61
4.20 (a) Power at the DC bus, $P_t^{dc} = V_t^{dc} \cdot I_t^{dc}$, and (b) at the electrolyzer-equivalent load, $P_h^{dc} = V_h^{dc} \cdot I_h^{dc}$. 62
4.21 Voltage fault simulated. 63
4.22 Measured voltage reference, V_d^*, after the voltage fault. 63
4.23 Measured value of total reactive power after the voltage fault. 64
4.24 Measured value of total active power after the voltage fault. 65
4.25 (a) DC bus voltage, V_t^{dc}, against its reference $V_{dc,ref}$, and (b) DC bus current, I_t^{dc}, at the input of the Interleaved Buck Converter, under the simulated voltage fault. . 65

4.26 (a) Voltage, V_h^{dc}, and (b) current, I_h^{dc}, at the terminals of the electrolyzer-equivalent load, under the simulated voltage fault. 66
4.27 (a) Power at the DC bus, $P_t^{dc} = V_t^{dc} \cdot I_t^{dc}$, and (b) at the electrolyzer-equivalent load, $P_h^{dc} = V_h^{dc} \cdot I_h^{dc}$. 66
4.28 Frequency event simulated. 67
4.29 Measured value of total active power after the frequency event. 68
4.30 (a) DC bus voltage, V_t^{dc}, against its reference $V_{dc,ref}$, and (b) DC bus current, I_t^{dc}, at the input of the Interleaved Buck Converter, under the simulated frequency event. 68
4.31 (a) Voltage, V_h^{dc}, and (b) current, I_h^{dc}, at the terminals of the electrolyzer-equivalent load, under the simulated frequency event. 69
4.32 (a) Power at the DC bus, $P_t^{dc} = V_t^{dc} \cdot I_t^{dc}$, and (b) at the electrolyzer-equivalent load, $P_h^{dc} = V_h^{dc} \cdot I_h^{dc}$. 69

List of Tables

3.1 Peak per-unit base values adopted for the Star (master) and Delta (slave) converters. 28
3.2 Vd and Vq controller gains. 34
3.3 Id and Iq controller gains used on the master converter. 36
3.4 Id and Iq controller gains used on the slave converter. 37
3.5 IBC branch sizing: input parameters, ripple criteria, and resulting component values. 41
3.6 IBC controller gains. 44

4.1 Steady-state (P_{ref}, Q_{ref}) operating points commanded during the four-quadrant test, in chronological order. 48
4.2 Power balance across the AC/DC and DC/DC conversion stages under normal operation. 62

List of Acronyms

AC	Alternating Current
AC/DC	Alternating Current to Direct Current
AEL	Alkaline Electrolysis
AFE	Active Front End
CSA	Current Saturation Algorithm
DAB	Dual Active Bridge
DC	Direct Current
DC/DC	Direct Current to Direct Current
EEC	Electrical Equivalent Circuit
ENTSO-E	European Network of Transmission System Operators for Electricity
FFR	Fast Frequency Response
FRT	Fault Ride-Through
GFL	Grid-Following
GFM	Grid-Forming
HIL	Hardware-in-the-Loop
HVDC	High-Voltage Direct Current
IBC	Interleaved Buck Converter
IBR	Inverter-Based Resources
IGBT	Insulated-Gate Bipolar Transistor
LVRT	Low-Voltage Ride-Through
MEA	Membrane Electrode Assembly
MMC	Modular Multilevel Converter
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPPT	Maximum Power Point Tracking
NPC	Neutral Point Clamped
PCC	Point of Common Coupling
PEM	Proton Exchange Membrane
PI	Proportional-Integral
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
RoCoF	Rate of Change of Frequency
SCR	Short-Circuit Ratio
SG	Synchronous Generator
THD	Total Harmonic Distortion
VI	Virtual Impedance
VOC	Virtual Oscillator Control
VRES	Variable Renewable Energy Sources
VSC	Voltage Source Converter
VSM	Virtual Synchronous Machine

List of Symbols

Notation conventions

v, i	Lowercase letters denote instantaneous values (e.g. v_{abc}, i_L) and dq-frame components (e.g. v_d, i_q)
V, I	Uppercase letters denote RMS values of AC quantities, DC or average values, magnitudes and powers
$\hat{V}$, $\hat{I}$	Peak values
x^{pu}	Value expressed in per unit; AC per-unit quantities are referred to the peak bases $\hat{V}_b$, $\hat{I}_b$ and to S_b (Table 3.1). Quantities given in pu are also identified in the Unit column below
x^*	Reference generated within a control loop
x_{ref}	Setpoint imposed externally by the test scenario script
x^Y, x^Δ	Quantity of the master (Star) and slave (Delta) converter, respectively
x^{dc}	DC-side quantity
x_t, x_h	DC bus side (input of the IBC) and electrolyzer side (output of the IBC), respectively
x_d, x_q	Direct- and quadrature-axis components in the synchronous reference frame
x_{abc}	Three-phase quantity
Δx	Peak-to-peak ripple or deviation of x
$x_{t,dc}$, $x_{h,dc}$	Notation used in the axis labels of the simulation figures of Chapter 4, equivalent to x_t^{dc} and x_h^{dc} (e.g. $V_{t,dc} \equiv V_t^{dc}$, $P_{h,dc} \equiv P_h^{dc}$, $V_{dc,ref} \equiv V_t^{dc*}$)

Latin symbols

C	Output capacitance of each IBC branch	F
C_{dc}	DC bus capacitance	F
C_{dl}	Double-layer capacitance of the PEM cell	F
C_f, C_f^Y, C_f^Δ	AC filter capacitance (master, slave)	F
D	Duty cycle of the IBC	–
d_1–d_3	Duty cycles of the IBC branches	–
D_p	Damping factor of the VSM	–
E_{inv}	Internal voltage of the GFM converter	V
E_k	Kinetic energy of a rotating mass	J
f	Frequency	Hz
f_{grid}	Grid frequency	Hz
f_{nom}	Nominal frequency	Hz
f_s	Switching frequency	Hz

$G_p(s)$, $G_q(s)$	Low-pass filters of the active and reactive power measurements	–
G_{P1}–G_{P3}	Gate signals of the IBC branches	–
H	Inertia constant	s
$\hat{I}_b^Y$, $\hat{I}_b^\Delta$	Peak base current (master, slave)	A
I_{cell}, i_{cell}	Cell current (steady-state, instantaneous)	A
I_{ff}^{dc}	Feedforward current of the IBC control	A
I_h^{dc}	Output current of the IBC (electrolyzer-equivalent load current)	A
I_h^{dc*}	Output current reference of the IBC	A
I_L	Nominal (average) branch current of the IBC	A
I_{max}	Maximum allowable converter current	pu
I_n	Current threshold for the activation of the Virtual Impedance	pu
I_{PI}^{dc}	Output of the DC bus voltage PI controller	A
I_{spike}	Fault current through the coupling reactance	A
I_{stack}	Nominal stack current	A
I_t^{dc}	DC bus current at the input of the IBC	A
ΔI	Peak-to-peak ripple of the AC converter current	A
δI	Current excess above the Virtual Impedance activation threshold	pu
i_{abc}, i_{abc}^Y, i_{abc}^Δ	Three-phase converter currents	A, pu
i_d, i_q	dq components of the converter current	pu
i_d^*, i_q^*	dq current references	pu
i_{gd}, i_{gq}	dq components of the output current used by the Virtual Impedance	pu
i_{LP1}–i_{LP3}	Inductor currents of the IBC branches	A
Δi_L	Peak-to-peak branch inductor current ripple	A
J	Virtual moment of inertia	kg m^2
K	Gain converting the grid voltage profile into volts	V
K_p, K_i	Proportional and integral gains of the PI controllers	–
k_{VI}	Proportional gain of the Virtual Impedance	–
L	Inductance of each IBC branch	H
L^Y, L^Δ	AC filter inductance (master, slave); denoted L in the decoupling terms $\omega L i_d$, $\omega L i_q$	H
m_p	Active power–frequency (P–f) droop gain	pu
N	Number of IBC branches	–
N_{cells}	Number of series-connected cells of the stack	–
n_q	Reactive power–voltage (Q–V) droop gain	pu
P	Active power	W, pu
P^{dc}	Power delivered by the AC/DC stage to the DC bus	W
P_{AC}	Total AC-side active power	W
P_{el}	Rated electrolyzer power	W
P_h^{dc}	Power at the electrolyzer-equivalent load	W
P_t^{dc}	Power at the DC bus (input of the IBC)	W
P_{meas}, P_{meas}^Y, P_{meas}^Δ	Measured active power (master, slave)	W
$P_{meas,total}$	Total measured active power of the AC/DC stage	W, pu
P_{ref} ($P_{ref,script}$)	Active power setpoint	pu
$\Delta P_{inertia}$	Active power exchanged by virtual inertia	pu

Q	Reactive power	var, pu
Q_{meas}, Q^{Y}_{meas}, Q^{Δ}_{meas}	Measured reactive power (master, slave)	var
$Q_{meas,total}$	Total measured reactive power of the AC/DC stage	var, pu
Q_{ref} ($Q_{ref,script}$)	Reactive power setpoint	pu
R_{act}	Activation resistance of the PEM cell	Ω
R_{eq}	Electrolyzer-equivalent resistance	Ω
R_{mem}	Membrane resistance of the PEM cell	Ω
R_{total}	Total ohmic resistance of the PEM cell	Ω
R_{VI}, X_{VI}	Virtual resistance and virtual reactance	pu
S	Apparent power	VA, pu
S_b	Base apparent power	VA
s	Laplace variable	–
T_s	Switching period	s
T_{vi}	Equivalent virtual inertia time constant	s
t	Time	s
$t_{delay,i}$	Carrier delay of IBC branch i	s
$\hat{V}^{Y}_{b}$, $\hat{V}^{\Delta}_{b}$	Peak base voltage (master, slave)	V
V_{act}, V_{ohm}, V_{conc}	Activation, ohmic and concentration overpotentials	V
V_{cell}	Cell voltage	V
V^{*}_{d}, V^{*}_{q}	dq voltage magnitude references generated by the droop control	pu
V_{grid}	Grid voltage magnitude	V, pu
$V_{grid,LL}$	Nominal line-to-line RMS voltage of the grid	V
V^{dc}_{h}	Output voltage of the IBC (electrolyzer-side voltage)	V
ΔV^{dc}_{h}	Peak-to-peak output voltage ripple of the IBC	V
V_{LL}	Nominal line-to-line RMS voltage of the converter-side windings	V
V_{nom}	Nominal voltage magnitude	pu
V_{rev}	Reversible cell voltage	V
V_s, V^{Y}_{s}, V^{Δ}_{s}	RMS voltage across each filter capacitor branch (master, slave)	V
V_{stack}	Stack voltage	V
V^{dc}_{t}	DC bus voltage	V
V^{dc*}_{t}	DC bus voltage reference	V
v_{abc}, v^{Y}_{abc}, v^{Δ}_{abc}	Three-phase converter voltages	V, pu
v_d, v_q	dq components of the converter voltage	pu
$v_{d,ref}$, $v_{q,ref}$	dq voltage references after the Virtual Impedance	pu
δv_d, δv_q	dq voltage drops introduced by the Virtual Impedance	pu
$v_{m,d}$, $v_{m,q}$	dq modulating voltages	pu
$v_{PI,d}$, $v_{PI,q}$	Outputs of the dq current PI controllers	pu
X_L	Coupling reactance between converter and grid	Ω

Greek symbols

δ	Phase angle of the converter internal voltage	rad
Δf^{pu}	Frequency deviation	pu

$\eta_{AC/DC}$, $\eta_{DC/DC}$	Efficiency of the AC/DC and DC/DC stages	%
η_{global}	Overall AC-to-electrolyzer efficiency	%
θ, θ_{master}	Voltage angle of the master converter	rad
θ_{grid}	Grid voltage angle	rad
θ_{pll}	Angle estimated by the PLL	rad
θ_{slave}	Synchronization angle of the slave converter	rad
θ_{vsm}	Virtual rotor angle of the VSM	rad
$\sigma_{X/R}$	X/R ratio of the Virtual Impedance	–
τ_p, τ_q	Time constants of the power measurement filters	s
ω	Angular frequency	rad/s
ω_c^*	Angular frequency reference generated by the P–f droop	rad/s, pu
ω_{grid}	Grid angular frequency	rad/s
ω_{nom}	Nominal angular frequency	rad/s, pu
ω_{vsm}	Virtual rotor speed of the VSM	rad/s

Correspondence with the Simulink labels

Symbol	**Simulink label**	**Figure**
P_{ref}, Q_{ref}	Pref, Qref	3.4, 3.5
$P_{meas,total}$, $Q_{meas,total}$	Pmeas, Qmeas	3.4, 3.5
m_p	kp	3.4
ω_{nom}	wn	3.4
ω_c^* (pu)	droop	3.4
θ	Theta	3.4
n_q	QVoltDroop	3.5
V_{nom}	voltreference	3.5
V_d^*, V_q^*	Vd, Vq	3.5
i_{gd}, i_{gq}	Igd, Igq	3.6
I_n	Inominal	3.6
k_{VI}	Resistance coefficient	3.6
$\sigma_{X/R}$	oX/R	3.6
R_{VI}, X_{VI}	R_VI, X_VI	3.6
δv_d, δv_q	delVd, delVq	3.6
$v_{d,ref}$, $v_{q,ref}$	Vdref, Vqref	3.7, 3.8, 3.9
v_d, v_q	Measured Vd, Measured Vq	3.7
i_d^*, i_q^*	idref, iqref	3.7, 3.8, 3.9
i_d, i_q	Measured id, Measured iq, delta Id, delta Iq	3.8, 3.9
ω	Angfreq	3.9
ωL	wL	3.8, 3.9
$v_{m,d}$, $v_{m,q}$	Modulation Vd, Modulation Vq	3.8
	Vd, Vq	3.9
I_h^{dc*}	ihStep	4.8
V_t^{dc}, I_t^{dc}, P_t^{dc}	$V_{t,dc}$, $I_{t,dc}$, $P_{t,dc}$	Chapter 4
V_h^{dc}, I_h^{dc}, P_h^{dc}	$V_{h,dc}$, $I_{h,dc}$, $P_{h,dc}$	Chapter 4
V_t^{dc*}	$V_{dc,ref}$	Chapter 4

Chapter 1

Introduction

1.1 The Paradigm Shift in Power Systems

The global energy landscape is currently undergoing a deep transition, driven by the urgent need to decarbonize economies and mitigate climate change. This shift is characterized by the massive integration of Variable Renewable Energy Sources (VRES), such as wind and solar, into the electrical grid. While essential for a sustainable future, VRES introduce significant challenges to power system stability due to their inherent uncertainty and variability, driven by factors like solar irradiance and wind speed fluctuations [1].

In traditional power systems, grid stability and flexibility were predominantly ensured on the supply side. Conventional fossil-fuel-based power plants employed large synchronous machines that naturally provided rotational inertia to the system [1]. This physical inertia is a critical parameter for grid stability, as it inherently dampens frequency deviations immediately following a disturbance, such as sudden loss of generation or a load step. Furthermore, these synchronous generators were capable of regulating voltage and frequency through well-established control mechanisms.

However, modern power systems are becoming increasingly "inverter-dominated". VRES are typically interfaced with the grid through power electronic converters (inverters) rather than direct synchronous connections. As conventional plants are decommissioned and replaced by these inverter-based resources, the total inertia of the power system decreases drastically. This reduction in inertia makes the grid more susceptible to rapid frequency changes, i.e., a high Rate of Change of Frequency (RoCoF) and potential instability events. Consequently, the traditional approach of relying only on generation for flexibility is becoming insufficient [1]. To maintain a secure and reliable power system, flexibility must now be harvested from each source, including energy storage and, crucially, the demand side.

1.2 Green Hydrogen Production and Electrolyzer Technologies

Within the context of decarbonization, green hydrogen (H_2) has emerged as a critical energy vector, capable of coupling the electrical sector with "hard-to-abate" industries such as heavy transport and chemical manufacturing [2]. Produced via the electrochemical splitting of water using renewable electricity, green hydrogen offers a zero-emission pathway for long-term energy storage, effectively addressing the seasonal variability of renewable generation [3]. Figure 1.1 illustrates this process in a simplified manner, highlighting the key components of a water electrolyzer system.

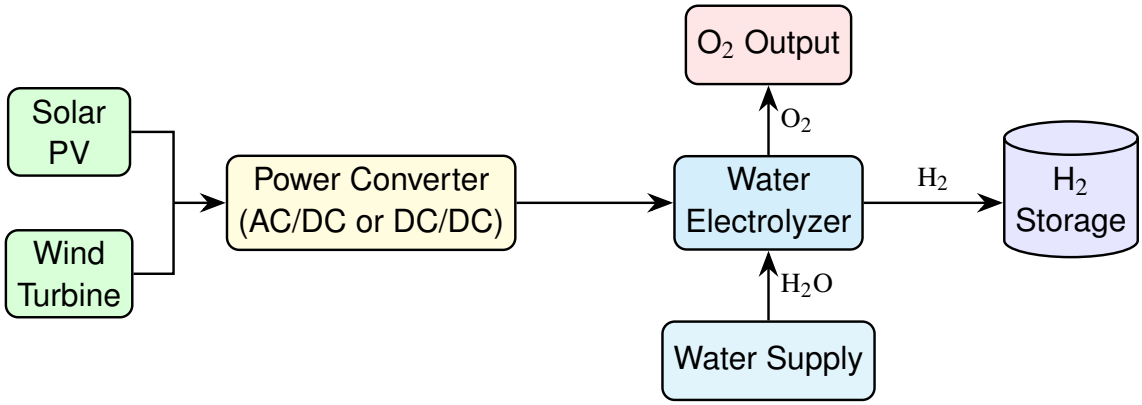


Figure 1.1: Green hydrogen production scheme.

Currently, the two main technologies for water electrolysis are Alkaline Electrolysis (AEL) and Proton Exchange Membrane (PEM) electrolysis. While AEL is the most mature and commercially established technology, favored for its lower capital costs and proven durability, its application in modern grids faces dynamic limitations. The physical inertia associated with the liquid electrolyte and diaphragm separators constrains its ability to respond rapidly to power fluctuations, making it less suitable for fast frequency support [4].

In contrast, PEM electrolysis utilizes a solid polymer electrolyte, allowing for a compact design and high current densities. Although currently more capital-intensive, PEM systems exhibit superior dynamic capabilities, including rapid ramp rates and a wide partial load operating range. It is this high dynamic capability that positions the PEM electrolyzer not merely as a passive load, but as a controllable asset. In inverter-dominated grids, the fast response time of the PEM stack, when interfaced with appropriate power electronics, enables the implementation of advanced control strategies, such as the Grid-Forming control proposed in this dissertation, allowing the load to actively contribute to system stability.

1.3 Motivation: The Concept of Grid-Forming Loads

The transition to an inverter-dominated power system necessitates a fundamental re-evaluation of grid control strategies. Current grid codes and control architectures predominantly rely on

Grid-Following (GFL) inverters [5]. These devices operate as current sources, synchronizing their output current to the local grid voltage angle (θ_{grid}) estimated by a Phase-Locked Loop (PLL). While effective in stiff grids, GFL units do not inherently contribute to grid stability, that is, they merely "follow" the existing frequency and voltage. In low-inertia systems, this reliance on a stable external voltage reference can lead to instability and synchronization loss during severe transient events [6].

To mitigate these risks, Grid-Forming (GFM) control has emerged as a superior alternative. GFM inverters behave as ideal voltage sources, actively controlling the voltage magnitude and frequency at their terminals without relying on a PLL for synchronization [6]. By emulating the physical behavior of synchronous machines, more precisely their inertia and damping properties, GFM units can instantaneously counter frequency deviations, a concept often referred to as the Virtual Synchronous Machine (VSM) [7].

However, the majority of existing research on GFM control focuses on battery energy storage systems or generation units. The application of GFM control to loads, such as large-scale electrolyzers, remains an under-explored yet promising frontier [8]. This dissertation explores the concept of a **Grid-Forming Load**, where the electrolyzer actively participates in forming the grid voltage and frequency, rather than acting as a passive responsive load.

A critical distinction in this approach is the physical constraint of the electrolyzer. Unlike a battery, which can source and sink active power symmetrically, an electrolyzer is a unidirectional load: it can rapidly decrease its power consumption to support under-frequency events, but its ability to increase consumption for over-frequency support is inherently limited by its rated capacity. This dissertation aims to contribute to the research being conducted by the group at the laboratory in the context of electrolyzer research.

1.4 Objectives

The main objective of this dissertation is to study, through simulation, the behavior of a grid-forming controlled electrolyzer that supports the grid by providing Fast Frequency Response and voltage support through droop-based active and reactive power control, and that maintains stable operation under grid frequency and voltage disturbances.

To achieve this goal, the specific objectives have been defined as follows:

- **Study of the power converter solution:** Study the power converter chain required to feed the electrolyzer and interface it with the grid under GFM control.
- **Simulation studies:** Conduct computational analyses to model the behavior of the proposed solution under realistic conditions.
- **Development of the controller:** Design a control strategy, based on P–f and Q–V droop control, that enables the electrolyzer to operate in a grid-forming mode, providing frequency and voltage support to the grid.

1.5 Dissertation Structure

Following the definition of the objectives in the previous Section 1.4, this document is organized into five main chapters designed to guide the reader from the theoretical problem to the proposed methodological solution:

- **Chapter 1 (Introduction)** establishes the motivation for the research, defines the problem statement regarding low-inertia grids, and outlines the scope and objectives of the work.
- **Chapter 2 (State of the Art)** provides the theoretical foundation for the dissertation. It reviews the operating principles of PEM electrolysis, compares power electronic topologies, and details the control architectures for grid-forming converters, comparing the Virtual Synchronous Machine against the Droop-based control strategy ultimately adopted for the converter implementation. Furthermore, it defines the critical ancillary services, such as Fast Frequency Response, Synthetic Inertia, and Low-Voltage Ride-Through (LVRT).
- **Chapter 3 (System Design and Control Implementation)** presents the resulting system architecture. It describes the implementation of the grid-forming AC/DC stage, virtual impedance, and voltage/current control loops, as well as the characterization and sizing of the electrolyzer-equivalent load and the design and control of the Interleaved Buck Converter that interfaces it with the DC bus.
- **Chapter 4 (Results and Analysis)** presents and discusses the results obtained from the different simulation scenarios performed on the developed model. It first validates the master–slave AC/DC control architecture against an ideal DC source across the full four-quadrant P–Q operating envelope, before assessing the behavior of the complete system, including the DC bus, DC/DC stage, and electrolyzer-equivalent load, under normal operation, voltage and frequency disturbances.
- **Chapter 5 (Conclusions and Future Work)** demonstrates the fulfillment of the dissertation's objectives and proposes directions for future work.

Chapter 2

State of the Art

To implement a robust grid-forming control strategy, it is essential to first understand the physical and electrical characteristics of the load and the necessary conversion stages. This chapter establishes the theoretical foundation required to transform an electrolyzer from a passive industrial consumer into an active grid-supporting asset.

It begins by analyzing PEM technology, justifying its selection for fast-response applications. Subsequently, the power conversion stage is discussed, focusing on the Active Front End (AFE) and Interleaved Buck Converter topology necessary for the interface. The core control philosophy is then examined, contrasting traditional methods with Grid-Forming control, and comparing the Virtual Synchronous Machine against the Droop-based architecture ultimately adopted for the converter implementation. Finally, the chapter defines critical ancillary services, such as Synthetic Inertia and LVRT, which dictate the system's performance requirements.

2.1 Electrolyzer Technologies and Dynamic Modeling

To implement a grid-forming control strategy, it is essential to first understand the physical and electrical characteristics of the load. This section reviews the dominant electrolysis technologies and presents the mathematical models required to simulate their static and dynamic behavior in power system studies.

2.1.1 Water Electrolysis and the PEM Technology

Water electrolysis is the electrochemical process by which water is split into hydrogen and oxygen gas by passing a Direct Current (DC) through it. In practical terms, water is supplied to a stack of electrochemical cells, a DC voltage is applied across the cell, and the resulting current drives the reaction, producing hydrogen at one electrode and oxygen at the other. This process forms the basis of so-called "green hydrogen" production, where the electricity used to drive the reaction comes from renewable sources, and is the core operating principle shared by all electrolyzer technologies discussed in this work.

While several electrolyzer technologies exist, AEL and PEM electrolysis are the most relevant for industrial applications, and their suitability for grid support services differs significantly due to their physical construction and operational characteristics [9]. AEL is currently the standard for large-scale hydrogen production, owing to its mature status and lower investment costs, but it relies on a liquid alkaline electrolyte and a porous diaphragm, which limit its dynamic response and partial-load flexibility [3], [9]. PEM electrolysis, in contrast, is a comparatively more recent and capital-intensive technology, but offers a markedly faster and more flexible dynamic response, making it the technology selected for this work and discussed in detail below.

PEM electrolysis is based on a solid polymer electrolyte, typically a perfluorosulfonic acid polymer such as Nafion, instead of the liquid electrolyte used in AEL [3]. This solid membrane conducts protons (hydrogen ions, H^+) while electronically insulating the electrodes and physically separating the product gases [9]. The electrodes are bonded directly to the membrane in a compact "zero-gap" configuration, forming a Membrane Electrode Assembly (MEA), as illustrated in Figure 2.1.

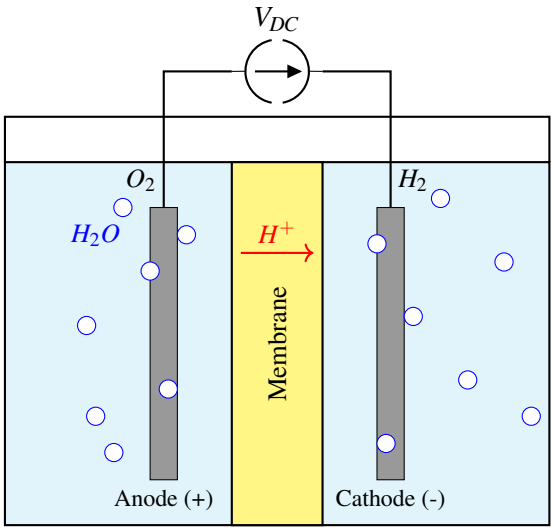


Figure 2.1: Schematic representation of a PEM electrolysis cell.

This construction is directly responsible for PEM's main advantages over AEL. The thin solid electrolyte allows PEM electrolyzers to operate at much higher current densities, and the low gas crossover of the membrane allows safe operation across a wide partial-load range, with the ability to follow load changes in the order of milliseconds to seconds [3], [10]. This combination of high current density and fast, flexible dynamic response is what makes PEM electrolysis particularly well suited to coupling with VRES [11] and, more specifically for this work, to providing fast-response grid services.

This high dynamic capability, however, comes with a specific demand on the electrical power supply side. PEM stacks operate at very low cell voltages but require very high current densities, and they are particularly sensitive to current ripple, which accelerates membrane degradation and

reduces operational lifetime. Consequently, an electric power supply capable of delivering a stable, low-ripple, high-current DC source, while still being able to follow fast power variations imposed by grid-forming operation, is essential to fully exploit PEM's dynamic potential. This requirement directly motivates the power conversion chain discussed in the following section.

2.1.2 Static and Dynamic Modeling of PEM Electrolyzers

2.1.2.1 Static Electrical Characteristics

While the Nernst equation defines the thermodynamic minimum voltage, the actual operating voltage of the electrolyzer cell (V_{cell}) is always higher when current flows. This increase is caused by irreversible losses known as overpotentials. The steady-state voltage-current (V–I) characteristic is governed by the sum of the reversible voltage and three distinct overpotential terms [12]:

$$V_{cell} = V_{rev} + V_{act} + V_{ohm} + V_{conc} \tag{2.1}$$

where:

- **Activation Overpotential (V_{act}):** This loss dominates at low current densities and represents the energy barrier that must be overcome to initiate the electrochemical reaction at the catalytic surfaces (anode and cathode). It is non-linear and typically modeled using semi-empirical logarithmic relationships derived from the Tafel equation [3].
- **Ohmic Overpotential (V_{ohm}):** As the current density increases, the resistive losses become dominant. This term follows Ohm's law ($V_{ohm} = I_{cell} \cdot R_{total}$) and is caused primarily by the proton conductivity resistance of the polymer membrane, as well as the contact resistances of the electrodes and bipolar plates [12].
- **Concentration Overpotential (V_{conc}):** At very high current densities, the rate of reaction exceeds the rate at which reactants (water) can be supplied or products (gas bubbles) removed from the reaction sites. This mass transport limitation leads to a rapid, non-linear voltage increase, limiting the maximum achievable power [3].

2.1.2.2 Dynamic Electrical Equivalent Circuit

For grid stability studies, specifically for Grid-Forming control where sub-second response is critical [13], a static model is insufficient as it ignores non-linear overvoltages and dynamic parameter shifts [12], [13]. The electrochemical interface between the electrode and the electrolyte exhibits a "double-layer" effect, where charges accumulate effectively acting as a capacitor [13].

To capture these transient behaviors, the PEM electrolyzer is modeled as an Electrical Equivalent Circuit (EEC). A widely adopted dynamic model, shown in Figure 2.2, consists of a voltage source (V_{rev}) in series with an ohmic resistance (R_{mem}), and one or more parallel RC (Resistor-Capacitor) branches [12].

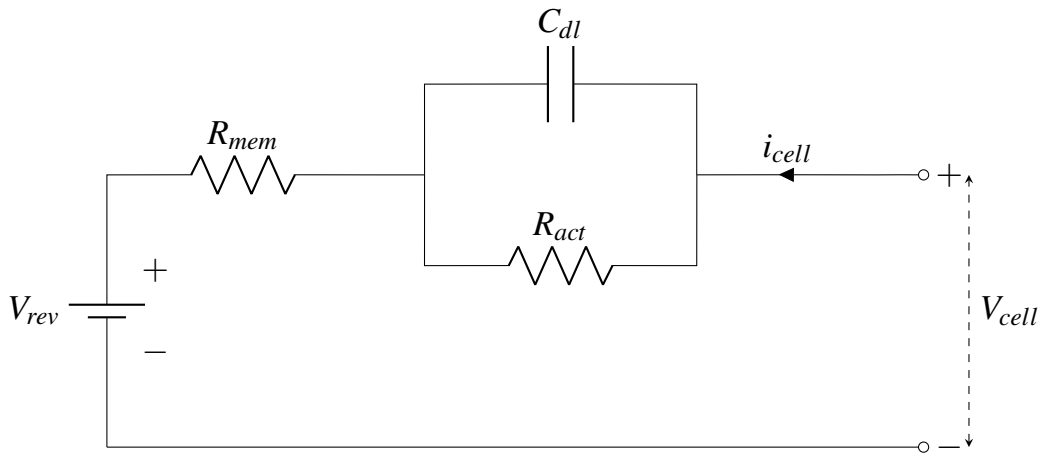


Figure 2.2: Dynamic EEC of a PEM electrolyzer cell including the double-layer capacitance effect.

In this model, R_{mem} represents the ohmic value of the membrane, while the $R_{act}||C_{dl}$ branch represents the activation dynamics. The capacitor C_{dl} (Double-Layer Capacitance) introduces a time delay in the voltage response when current changes rapidly. This dynamic impedance is crucial for the design of the control loops, as it implies that the electrolyzer does not behave as a purely resistive load during the fast frequency transients associated with grid-forming operation [12].

2.2 Power Electronic Conversion Stages for Hydrogen Electrolyzers

The integration of PEM electrolyzers into the electrical grid requires a robust power conditioning system capable of bridging the high-voltage Alternating Current (AC) grid and the low-voltage DC characteristics of the electrolyzer stack. While traditional industrial applications often rely on thyristor-based rectifiers due to their low cost and robustness, the strict requirements of modern smart grids, specifically regarding power quality and ancillary services, necessitate advanced active topologies.

In [14], the authors present a narrative review of the AC/DC and DC/DC power electronic structures for hydrogen production, concluding that an active rectifier followed by an interleaved DC/DC stage offers good current control characteristics together with high-quality grid integration, enabling the provision of grid services such as grid-forming operation. Based on this review, this section outlines the two-stage conversion architecture employed in this work, justifying the selection of an AFE AC/DC stage and an Interleaved Buck DC/DC stage.

2.2.1 The AC/DC Stage: Converter Topologies for Grid-Connected Electrolyzers

The power electronic interface plays a central role in the integration of hydrogen electrolyzers into electrical power systems, as it is responsible for converting the grid-side AC voltage into a regulated DC current suitable for electrochemical hydrogen production. The performance of this

stage directly affects grid power quality, system controllability, and the operational lifetime of the electrolyzer stack [15].

According to the literature, AC/DC converter topologies for electrolyzer applications can be broadly classified into two main categories: line-commutated rectifiers, based on thyristors or diodes, and fully controlled converters, based on semiconductor switches such as Insulated-Gate Bipolar Transistors (IGBTs) or Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) [14], [15], [16]. Line-commutated rectifiers (thyristor- or diode-based) remain the traditional choice for high-power electrolysis due to their robustness and low cost, but they introduce significant harmonic distortion, a poor power factor, and substantial DC-side current ripple, which accelerates PEM membrane degradation [14], [15]. At the opposite end, multilevel topologies (e.g., Neutral Point Clamped (NPC), Modular Multilevel Converter (MMC)) offer excellent power quality but at the cost of a much higher component count and control complexity, making them less suited to system-level grid-forming studies [15]. Fully controlled two-level converters, in the form of an AFE, occupy the practical middle ground adopted in this work and are discussed in detail below.

2.2.1.1 Active Front End (AFE) Converters

To address the power quality and controllability limitations of passive rectifiers, AFEs, also referred to as Voltage Source Converters (VSCs), have been increasingly adopted in hydrogen production systems [15]. These converters employ fully controlled semiconductor devices, as can be observed in Figure 2.3, enabling sinusoidal grid currents and near-unity power factor operation without the need for extensive passive filtering [15].

Historically, high-current electrolysis has been supplied by diode and thyristor rectifiers, whose conversion is dictated by the grid voltage waveform: diode bridges offer no control over the DC output, while thyristor bridges regulate it only through the firing angle, at the cost of a power factor strongly dependent on the operating point and high-amplitude current harmonics on the AC side [14]. The two-level six-switch (2L-B6) AFE, depicted in Figure 2.3, overcomes these limitations by replacing the line-commutated devices with six fully controlled switches, combined with AC-side inductors (or an LCL filter) and a DC bus capacitor. Operated under Pulse Width Modulation (PWM) and closed-loop current control, it regulates both the magnitude and the phase of the grid current relative to the grid voltage, a capability absent in line-commutated rectifiers. As a result, properly designed 2L-B6 systems achieve power factors close to unity and grid-current Total Harmonic Distortion (THD) below 5%, within the limits of IEEE 519 [14]. Its main limitations arise from its two voltage levels, which produce a relatively high AC-side current ripple and therefore require larger input inductors, and from the fact that each switch must block the full DC bus voltage [14]. Nevertheless, its simple and robust structure, which can be implemented with commercial bridge modules, together with its maturity and effective DC current control, make it currently the most widely adopted AFE topology in industrial electrolyzer solutions [14].

A key advantage of AFEs is their capability to independently regulate active (P) and reactive (Q) power through decoupled current control [5], [15], [16], which allows the electrolyzer

interface to contribute to grid support functions such as voltage regulation and reactive power compensation [15], [16]. This functionality is particularly relevant in the context of increasing penetration of converter-dominated generation and reduced system inertia [15].

However, in electrolyzer applications characterized by low DC voltage and high current levels, an AFE stage alone may not be sufficient to provide the precise voltage and current conditioning required by the electrolysis stack [15]. In such cases, an additional DC/DC conversion stage is typically required to ensure adequate current regulation and ripple mitigation [15].

2.2.1.2 Topology Selection and Justification

Based on the review in [14], a two-stage power conversion structure consisting of an AFE rectifier followed by a DC/DC buck-type converter (discussed in Subsection 2.2.2) was identified as a suitable reference topology for this work.

From a grid-integration perspective, the AFE stage enables controlled interaction with the electrical network through decoupled regulation of active and reactive currents in the synchronous reference frame. This capability is essential for supporting grid-oriented functionalities, including voltage regulation and grid-forming operation, which cannot be readily achieved using passive rectifier solutions [15].

Overall, this topology represents a balanced compromise between controllability, power quality, and modeling complexity, making it well suited for system-level studies of grid-supporting and grid-forming operation of PEM electrolyzers [15].

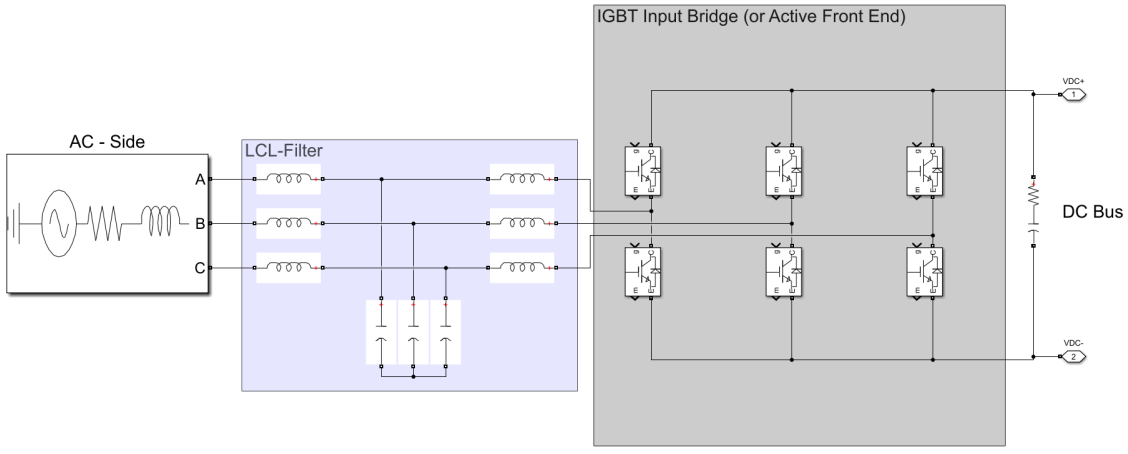


Figure 2.3: Schematic representation of the typical topology of the AFE.

2.2.2 The DC/DC Stage: Converter Topologies for Electrolyzer Interfacing

The second stage of the power conversion system must step down the regulated DC bus voltage to specific levels required by the electrolyzer stack. PEM electrolyzers are characterized by low cell voltages (typically 1.8–2.2 V per cell) but require very high current densities, often exceeding

2 A/cm^2 [3], [10]. Accurate current control at this stage is essential to ensure stable operation, high efficiency, and long-term durability of the electrolysis process.

Electrolyzers are inherently low-voltage, high-current loads, whereas the conversion performed by an AC/DC rectifier results in a DC bus voltage significantly higher than the stack voltage. A step-down conversion stage is therefore required, and the fundamental choice for this purpose lies within the family of Buck converters. However, a conventional single-phase Buck topology presents significant limitations at the power levels and current densities required by PEM stacks: increased semiconductor stress and substantial output current ripple, which accelerates membrane degradation [3]. To address these limitations, the literature also explores other multiphase or isolated topologies, such as Stacked Interleaved Buck, Quadratic Buck, and Dual Active Bridge (DAB) converters, but these introduce trade-offs in structural complexity, voltage stress, or the need for a high-frequency transformer that make them less suited to this study [14], [15]. The Interleaved Buck Converter (IBC) is identified instead as the reference solution adopted in this work, being a structure increasingly adopted by industry owing to its simplicity, its excellent current control, and its natural ripple minimization mechanisms [14], and is discussed in detail below.

2.2.2.1 Interleaved Buck Converter (IBC)

To overcome the limitations of the conventional Buck converter, the literature consistently identifies the IBC as a reference solution for hydrogen production systems, as illustrated in Figure 2.4. This topology places multiple buck converter phases in parallel, switching them with a phase shift (typically $360^\circ/N$, where N is the number of phases). This approach provides several technical justifications for PEM integration [14], [15], [17].

Comparative analyses of a wide range of DC/DC converter topologies indicate that the IBC offers a favorable balance between complexity, efficiency, and output current quality. Its main advantages can be summarized as follows:

- **Output Current Ripple Reduction:** The primary motivation for adopting an interleaved topology is the significant reduction of output current ripple. By phase-shifting the switching signals of parallel converter channels, the inductor current ripples partially cancel at the output node. This results in a smoother DC current supplied to the electrolyzer stack, which is particularly important for PEM electrolyzers, as excessive current ripple accelerates membrane degradation and reduces operational lifetime [14], [15], [17].

- **High Current Handling and Reduced Semiconductor Stress:** PEM electrolyzers operate at low voltage and very high current levels, often reaching several kiloamperes in megawatt-scale systems. The interleaved structure distributes the total current among multiple parallel phases, thereby reducing thermal and electrical stress on individual semiconductor devices and passive components. This enables the use of commercially available power devices and improves overall system scalability [14], [15], [17].

- **Reliability and Fault Tolerance:** The interleaved topology inherently enhances system reliability. In the event of a failure in one converter phase, the remaining phases can continue to operate in a degraded mode, supplying reduced power without causing a complete system shutdown. This level of fault tolerance is particularly relevant in industrial hydrogen production systems, where high availability and continuity of operation are critical [14], [15], [17].

By using an IBC, the system achieves the high voltage conversion ratio required for the DC bus and the low-voltage stack while maintaining the strict power quality standards required by sensitive electrochemical loads [17].

2.2.2.2 Topology Selection for Simulation Studies

For the purposes of this work, a multiphase IBC is selected as the reference DC/DC topology for simulation-based analysis. This choice is motivated by the specific requirements associated with grid-supporting and grid-forming operation of PEM electrolyzers.

First, the IBC topology enables accurate and high-bandwidth current control, which is essential when studying the dynamic modulation of electrolyzer power consumption [18], [19]. Such capability is particularly relevant for the emulation of inertia-like behavior and for responding to rapid frequency variations in low-inertia power systems [19].

Second, the interleaved structure ensures effective mitigation of output current ripple, thereby protecting the electrolyzer stack under dynamic operating conditions. Minimizing current ripple is critical for preserving membrane integrity and maximizing the operational lifetime of PEM electrolyzers, especially when the load profile is intentionally varied to support grid services.

Finally, the IBC represents a technically viable and industrially mature solution, widely reported in the literature and adopted in practical hydrogen production systems. This ensures that the simulation results obtained in this work remain representative of realistic system behavior, rather than being limited to idealized or unconventional converter configurations.

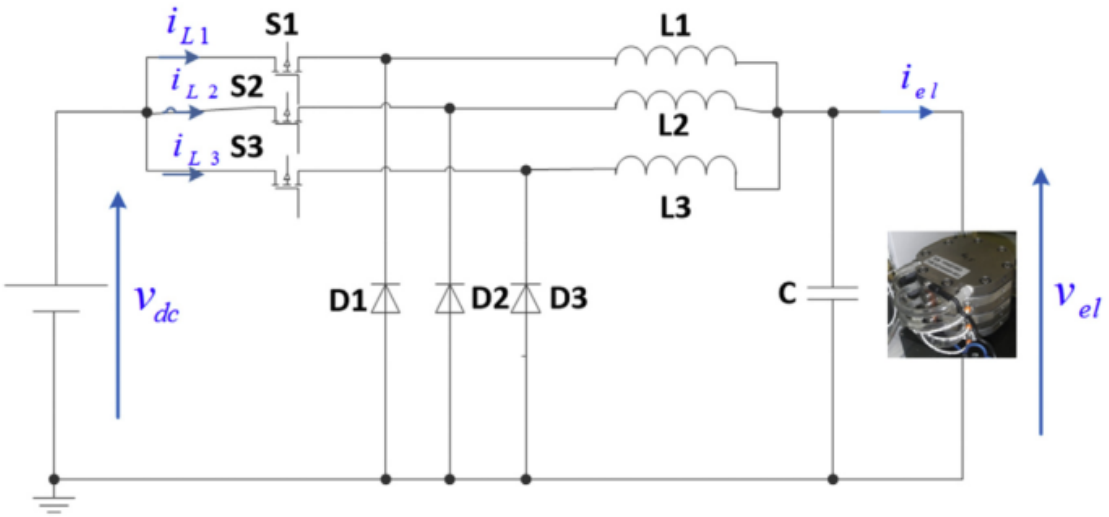


Figure 2.4: Schematic representation of an IBC with 3 parallel phases connected with the electrolyzer [17].

2.3 Control of Inverter-Based Resources: Grid-Following and Grid-Forming

The massive integration of VRES and Inverter-Based Resources (IBR) is fundamentally changing the dynamics of modern power systems. Unlike traditional Synchronous Generators (SGs), which inherently provide inertia and frequency support through their rotating masses, IBRs lack these physical properties. The system experiences a reduction in rotational inertia, leading to faster frequency dynamics and reduced stability margins [5], [20]. To address these challenges, the control philosophy of power electronic converters must evolve from merely injecting power to actively supporting and forming the grid voltage and frequency.

2.3.1 Grid-Following and Grid-Forming Control Paradigms

The classification of converter control strategies is primarily determined by how the converter interacts with the AC grid voltage and how it achieves synchronization [21].

2.3.1.1 Grid-Following Converter (GFL)

Currently, the standard control strategy for grid-connected converters is the Grid-Following, also referenced as grid-feeding [5]. In this architecture, the converter is controlled as a stiff current source connected to the grid in parallel with a high impedance, as illustrated in Figure 2.5. They can be considered as current sources, which adjust their output by varying output voltage to obtain a certain output power [5], [20], [22]. They inject active (P) and reactive (Q) power according to their setpoints, which are derived from maximum power point tracking (MPPT) or high-level controllers [20].

The GFL relies on a PLL to estimate the phase angle (θ_{pll}) and frequency of the grid voltage at the Point of Common Coupling (PCC) [5], [20]. It "follows" the grid voltage to inject a controlled current at the correct phase angle [21]. As GFL converters assume a stiff grid voltage is maintained by synchronous generators or by other sources that actively form the grid voltage and frequency references, they cannot operate in standalone mode or during grid faults where voltage collapses [5], [22]. Furthermore, GFL converters can suffer from instability in "weak grids", characterized by a low Short-Circuit Ratio (SCR), typically below 3, where the interaction between PLL dynamics and the high grid impedance can lead to loss of synchronism [21]. In addition, converter protections trip at considerably lower overcurrent levels, which may lead to the disconnection of the converter from the grid during disturbances; for this reason, LVRT capability (Section 2.4.4) is relevant even for grid-following converters. Crucially, standard GFL converters do not provide an inertial response, and therefore do not contribute to the frequency stability of the system [20], [23].

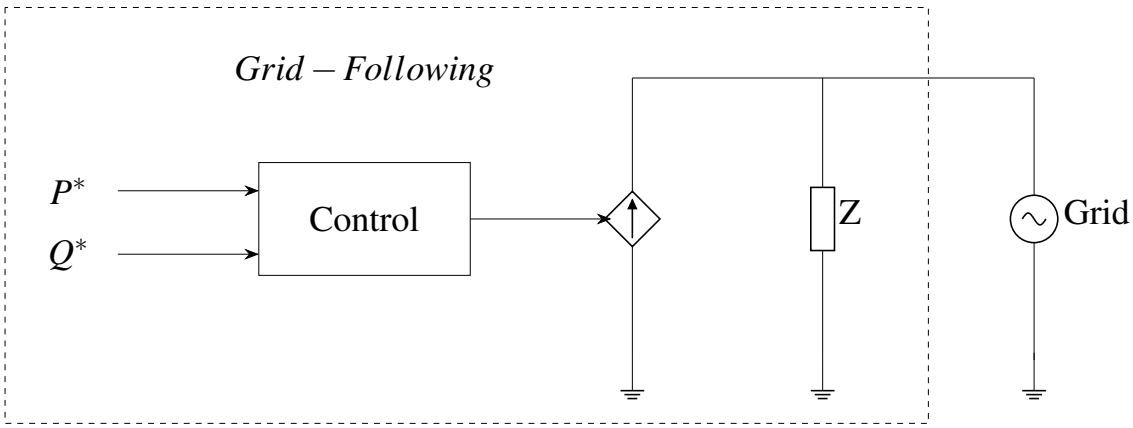


Figure 2.5: Representation of Grid-Following control architecture.

2.3.1.2 Grid-Forming Converter (GFM)

To overcome the limitations of GFL, Grid-Forming converters have been proposed. This topology is essential for achieving 100% power electronics-based transmission systems [20], [21]. A GFM converter behaves as a controllable voltage source behind a low output impedance [20], [21], [23]. Instead of controlling current directly, it regulates the voltage magnitude (V) and frequency (ω) at its terminals. Figure 2.6 gives a visual idea of this topology. This allows the converter to emulate the behavior of a synchronous machine [22]. The fundamental difference between GFL and GFM is synchronization. While GFL requires a PLL to align with the grid, a GFM converter self-synchronizes through active power control loops, similar to how a synchronous machine synchronizes via power-angle interactions [21]. While a PLL may still be present in some GFM architectures, it is often used for measurement or damping rather than essential synchronization, allowing the converter to operate stably even if the PLL dynamics are slow [21].

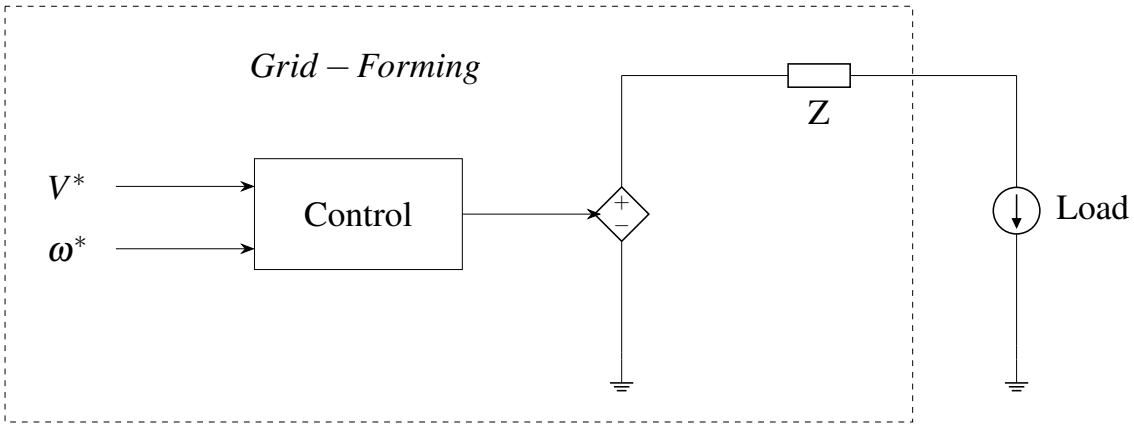


Figure 2.6: Representation of Grid-Forming control architecture.

Benefits and Justification for Selection:

Unlike GFL, GFM converters remain stable in weak grids and effectively strengthen the grid, since they impose the voltage magnitude and frequency at their terminals rather than following them [20], [21].

Because it controls voltage directly, GFM allows the electrolyzer system to support islanded operation and black start, which is the ability to restart and restore the electrical network from a blackout without relying on the external electric power transmission network [16]. However, being a load that lacks a prime mover, the electrolyzer cannot initiate the black start or energize the network on its own [8]. Instead, it can operate in tandem with a nearby renewable generation unit: both are started in grid-forming mode and jointly establish the network voltage and frequency, after which the renewable unit may switch to maximum power point tracking, while the electrolyzer maintains voltage and frequency by adjusting its active power consumption and reactive power exchange [8].

GFM enables the provision of "Virtual Inertia", allowing the electrolyzer to resist rapid frequency changes (RoCoF), a critical ancillary service for modern grids [20].

2.3.2 Grid-Forming Control Strategies

Within the GFM paradigm, various control strategies exist, such as Droop Control, Virtual Oscillator Control (VOC), and Virtual Synchronous Machine (VSM) [20], [23]. This section presents the two strategies most relevant to this work, the VSM and Droop Control, before Section 2.3.3 compares them and justifies the control strategy ultimately adopted for the converter implementation.

2.3.2.1 Virtual Synchronous Machine (VSM)

The VSM concept aims to emulate the dynamic characteristics of a traditional SG using the control software of the VSC. By mimicking the electromechanical behavior of an SG, the VSM provides

the grid with "synthetic" or "virtual" inertia, damping, and voltage regulation properties that are familiar to grid operators and compatible with existing power systems [20].

The core of the VSM control is the emulation of the Swing Equation (or equation of motion), which governs the dynamics of a synchronous machine's rotor. The control algorithm calculates a virtual rotor speed (ω_{vsm}) and phase angle (θ_{vsm}) based on the power balance [20], [23]:

$$J \cdot \omega \cdot \frac{d\omega}{dt} = P_{ref} - P_{meas} - D_p(\omega - \omega_{grid}) \tag{2.2}$$

where:

- J (or H) represents the Virtual Inertia. It determines how much energy the "virtual rotor" releases or absorbs during a frequency disturbance. A higher inertia limits the RoCoF [20], [21].
- P_{ref} represents the power setpoint.
- P_{meas} represents the measured electrical power.
- D_p represents the Damping Factor, which mimics the damper windings of a machine to suppress power oscillations [23].

While typically applied to generation, the VSM concept is equally applicable to the AFE of an electrolyzer. In this context, the electrolyzer acts as a Grid-Forming Load [13]. By modulating the DC bus power consumption according to the swing equation, the electrolyzer provides inertial support to the grid, stabilizing frequency dips by momentarily reducing its power consumption [13], thereby providing the frequency reserves explored for PEM electrolyzers in [19]. This control strategy ensures that the electrolyzer not only consumes power for hydrogen production but also provides essential stability services to the AC network.

2.3.2.2 Droop Control

Droop Control is a steady-state-oriented strategy, widely employed for power sharing among parallel sources in microgrids and, more generally, as a synchronization mechanism in grid-forming converters [5], [16]. Rather than emulating a rotor's equation of motion, conventional P–f droop control directly maps a frequency deviation to a proportional power correction. Following the formulation adopted for grid-forming hydrogen electrolyzers in [8], [13], the active power droop is expressed as:

$$\omega_c^* = m_p \left(P_{ref} - G_p(s)\, P_{meas}\right) + \omega_{nom} \tag{2.3}$$

where:

- m_p represents the droop gain, which determines the steady-state frequency deviation per unit of power imbalance, analogous to the inverse of a synchronous generator's governor droop characteristic [16].

- P_{ref} and P_{meas} represent, respectively, the active power setpoint and the measured electrical power, as in the VSM formulation.
- ω_{nom} is the nominal (base) angular frequency, and ω_c^* is the resulting operating frequency of the converter.
- $G_p(s) = 1/(\tau_p s + 1)$ is a low-pass filter, with time constant τ_p, placed on the power measurement feedback [8], [13].

An analogous droop relationship is used to regulate the AC voltage magnitude from the reactive power, following the same reference [8], [13]:

$$V_d^* = n_q \left(Q_{ref} - G_q(s)\, Q_{meas}\right) + V_{nom} \tag{2.4}$$

where n_q is the reactive power droop gain, Q_{ref} and Q_{meas} are the reactive power setpoint and measurement, V_{nom} is the nominal AC voltage magnitude, and $G_q(s) = 1/(\tau_q s + 1)$ is the corresponding low-pass filter on the reactive power measurement.

Unlike a purely proportional droop law, the low-pass filter $G_p(s)$ already embedded in Equation 2.3 reintroduces an inertia-like dynamic into the active power loop: as shown in [8], [13], the resulting equivalent inertial time constant is given by $T_{vi} = \tau_p/m_p$, which should be tuned to be slower than the response time of the electrolyzer stack to ensure the converter does not request power changes faster than the stack can physically follow. This allows the Droop architecture to reproduce a frequency response qualitatively similar to that of the VSM Swing Equation, while retaining a simpler structure with fewer tuning parameters [16], [21]. This filtered Droop formulation, for both active and reactive power loops, is the strategy adopted for the converter control implementation in this dissertation, including the master–slave parallel converter architecture discussed in later chapters, where a single Droop loop generates the shared virtual angle from the combined measured power of both converters.

2.3.2.3 Voltage and Current Control Cascade

Regardless of whether the synchronization and power-sharing references are generated by a VSM or by a Droop law, neither strategy directly imposes the converter's output voltage. The frequency reference (ω_{vsm} or ω_c^*) is only used to build the virtual angle θ, via integration, while the voltage-droop output (V_d^*, given by Equation 2.4) defines only the magnitude reference in the d-axis. In practice, GFM converters realize the controllable voltage source behind a low output impedance through a cascaded control structure, commonly composed of an outer AC voltage control loop and an inner current control loop [5], [13].

The outer AC voltage control loop regulates the converter's output voltage, v_d and v_q, towards the references generated by the active and reactive power droops (or, equivalently, by the VSM), producing the current references, i_d^* and i_q^*, that the converter must supply to achieve that voltage [13]. The inner current control loop, in turn, regulates the converter's output current, i_d and i_q, at these references, generating the modulation signal used to synthesize the converter's switching

pattern [13]. Because the current dynamics are considerably faster than the voltage dynamics, the current control loop is typically designed with a bandwidth at least one order of magnitude higher than that of the voltage loop, ensuring a clean separation between the two control timescales and allowing each loop to be tuned independently using standard Proportional-Integral (PI) design methods [5], [13].

This cascaded structure is independent of the specific power-sharing strategy adopted at the outer synchronization level (VSM or Droop), and is therefore treated in this work as a common building block of the converter's grid-forming control, rather than as a distinguishing feature between the two strategies compared in Section 2.3.3.

2.3.3 Comparative Analysis of Control Strategies

Having introduced both the VSM and Droop Control formulations, it is necessary to compare their dynamic performance, alongside that of physical SGs and VOC, in order to justify the control strategy ultimately adopted for the grid-connected electrolyzer.

2.3.3.1 Control Strategy Selection and Justification

A purely proportional P–f droop law reacts only to the frequency error, not its derivative, and therefore has no direct effect on the RoCoF during the initial moments of a disturbance [16]. By contrast, the VSM incorporates the Swing Equation, which includes an explicit inertia term ($J\frac{d\omega}{dt}$), allowing it to dampen rapid frequency oscillations without requiring auxiliary loops [16], [20].

This distinction, however, is not as strict in practice. As shown in Section 2.3.2.2, the Droop formulation adopted in this work already embeds a low-pass filter, $G_p(s)$, on the power measurement path (Equation 2.3), which reintroduces an inertia-like time constant ($T_{vi} = \tau_p/m_p$) into the control loop, making it mathematically close to a VSM response [13], [16], [21]. Given this equivalence, and the reduced parameterization and tuning effort required by a Droop-based architecture compared to a full Swing Equation implementation, Droop Control was selected as the control strategy adopted for the converter implementation in this dissertation. This choice prioritizes a simpler, more robust control structure, particularly relevant when extending the architecture to the parallel converter configuration discussed in later chapters, while still allowing frequency-support behavior to be shaped through the droop gain and the power-measurement filtering.

2.3.3.2 Droop Control vs. Physical Synchronous Generators

Both VSM and Droop-based grid-forming control aim to emulate certain aspects of an SG, but offer superior dynamic performance due to the absence of physical limitations.

- **Response Speed:** Physical SGs are limited by the slow dynamics of mechanical turbines, valves, and governors. Time-domain simulations demonstrate that Grid-Forming converters, whether VSM- or Droop-based, react much faster to power imbalances than traditional SGs,

reaching steady-state frequency support within seconds compared to the slower mechanical response of SGs [23].

- **Flexibility:** Unlike the fixed inertia of a rotating mass, the droop gain and any auxiliary filtering parameters are software parameters. These can be tuned or made adaptive in real-time to optimize stability margins, offering "extended support" that exceeds the capabilities of physical machines [16].

2.3.3.3 Droop Control vs. Virtual Oscillator Control

- **Operator Familiarity and Integration:** Droop-based control mimics the steady-state power-sharing behavior long established in conventional power systems, making it straightforward to integrate into existing grid codes and operational practices [16].
- **Simplicity and Implementation Effort:** Research indicates that VOC is often mathematically equivalent to conventional Droop Control in a small-signal sense [21], while requiring a comparatively more elaborate oscillator-based implementation. Given this near-equivalence, Droop Control was preferred as the more direct and easily parameterized option for the converter control loops developed in this work [20], [21].
- **Established Analysis Principles:** By using a power-frequency droop gain, possibly combined with a measurement filter to shape the transient response, the converter can still be analyzed using established power system stability principles, facilitating its integration alongside existing transmission system practices [7], [16].

2.4 Ancillary Services and Grid Codes

Beyond the converter control architecture itself, a GFM electrolyzer is expected to actively participate in a defined set of ancillary services, whose requirements are increasingly formalized through grid codes as system inertia decreases [5], [20]. This section reviews three ancillary services commonly associated with the Grid-Forming Load paradigm: Fast Frequency Response, Virtual Inertia, and Low-Voltage Ride-Through, together with the grid-code requirements that define their expected performance, before closing with an assessment of which of these services are addressed within the scope of this dissertation.

2.4.1 Ancillary Services Overview

Ancillary services are the specific functions provided by grid-connected assets to maintain the reliability, stability, and security of the electrical system. Historically, power systems relied on SGs to naturally provide services such as frequency regulation, voltage support, and black-start capability [16]. However, the massive integration of VRES and the displacement of thermal machines are reducing the system's rotational inertia, leading to faster frequency dynamics and reduced stability

margins [16], [20]. Consequently, IBRs and large flexible loads like electrolyzers must now explicitly synthesize these services to compensate for the reduction in synchronous generation [23].

Key ancillary services relevant to this work include:

- **Frequency Regulation:** Maintaining the balance between generation and load to keep frequency within nominal limits [20].
- **Voltage Support:** Injecting or absorbing reactive power (Q) to maintain voltage stability [16].

2.4.2 Fast Frequency Response (FFR)

In low-inertia grids, the RoCoF following a disturbance can be too fast for traditional primary frequency control to arrest before safety limits are reached [16], [20]. FFR refers to the rapid injection or reduction of active power (P) by inverter-based resources to arrest frequency excursions in the sub-second timeframe.

Unlike mechanical governors which have time constants in the range of seconds [16], power converters can adjust their power setpoints much faster [23]. This allows electrolyzers to provide FFR by rapidly reducing power consumption (load shedding) during under-frequency events [13].

FFR acts as a bridge between the immediate inertial response and the slower primary control, stabilizing the Frequency Nadir (the lowest frequency point reached during a disturbance) and preventing unintentional load shedding [16], [20].

2.4.3 Virtual Inertia

Virtual Inertia (also referred to as Synthetic Inertia) is defined by ENTSO-E (European Network of Transmission System Operators for Electricity) as "a facility provided by a Power Park Module or HVDC System to replace the effect of Inertia of a Synchronous Power Generating Module to a prescribed level of performance" [24].

While physical inertia relies on the kinetic energy stored in a rotating mass ($E_k = \frac{1}{2}J\omega^2$), synthetic inertia relies on energy buffers, such as DC bus capacitors, batteries, or the hydrogen production process itself, to exchange power proportional to the RoCoF [16], [20].

This is achieved by implementing the Swing Equation in the converter's control software [16], [20]. This forces the electrolyzer to dynamically emulate the mechanical characteristics of a synchronous machine:

$$\Delta P_{inertia} = -2H\frac{df}{dt} \tag{2.5}$$

This behavior is illustrated in Figure 2.7.

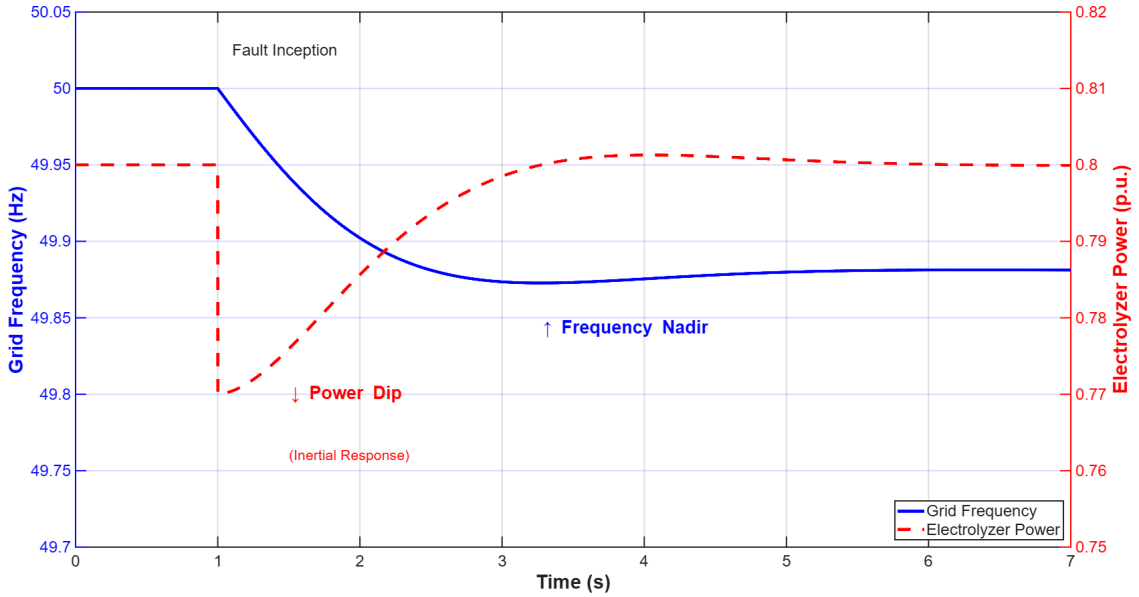


Figure 2.7: Simulated response of a GFM electrolyzer to a load step. The red dashed curve illustrates the virtual inertial response, where the electrolyzer rapidly reduces its power consumption proportional to the RoCoF, effectively dampening the frequency deviation (blue curve).

By providing this service, the electrolyzer limits the initial slope of frequency decline (RoCoF) during grid faults, mimicking the "resistance to change" inherent in synchronous machines [20], [23].

2.4.4 Low-Voltage Ride-Through (LVRT) Requirements

Grid codes require that generators and large connected loads remain connected to the grid during short-duration voltage dips (faults) to prevent a cascading collapse of the power system. This capability is known as Low-Voltage Ride-Through, a specific type of Fault Ride-Through (FRT) [16], [23].

However, the implementation of Grid-Forming control presents a significant hardware challenge. Since a GFM electrolyzer behaves as a voltage source behind a low output impedance, it attempts to maintain its internal voltage magnitude even when the grid voltage collapses (e.g., during a short-circuit fault). This creates a large instantaneous voltage difference between the converter and the grid, resulting in a massive current spike that can easily exceed the thermal limits of the semiconductors (IGBTs) [21]. This situation is represented in Figure 2.8: the converter attempts to maintain E_{inv} while the grid voltage V_{grid} collapses, driving a massive current spike through the low filter impedance X_L.

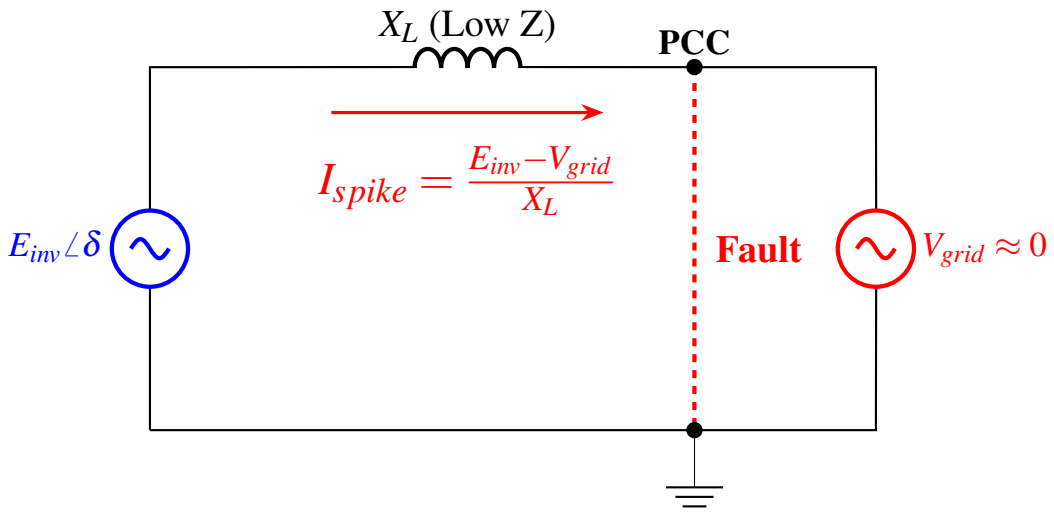


Figure 2.8: Equivalent circuit of a GFM electrolyzer during a grid voltage dip.

To comply with LVRT requirements without damaging the hardware, GFM electrolyzers must implement current limiting strategies. Two primary methods are Current Saturation Algorithms (CSA) and Virtual Impedance (VI) [21]. While CSA provides strict current limiting by saturating the reference, Virtual Impedance emulates a physical impedance drop to lower the voltage reference during faults, which is often preferred for maintaining transient stability and ensuring successful post-fault synchronization [21]. For this reason, Virtual Impedance was the Fault Ride-Through method adopted in the converter implementation of this work, favoring smooth post-fault recovery and synchronization over the harder current-clamping behavior of a saturation-based approach.

2.4.5 Feasibility of Ancillary Services Analysis

The ancillary services and grid-code-related functionalities discussed in the previous subsections differ significantly in terms of modeling complexity and validation requirements. As such, not all of them can be addressed with the same level of depth within the scope of a master's dissertation based primarily on simulation.

In this work, frequency-related services, including inertial response emulation and fast frequency support through active power modulation, are identified as the most suitable candidates for quantitative analysis in simulation. These services can be evaluated using reduced-order system models and allow a direct assessment of the dynamic interaction between the electrolyzer and the electrical grid.

Voltage-related services and detailed compliance with grid codes, such as Low-Voltage Ride-Through requirements, typically require detailed converter models, protection systems, and validation against specific grid standards. Consequently, these aspects are addressed only at a qualitative level in this dissertation and are identified as topics for future work.

This distinction ensures that the selected research focus remains feasible and that the simulation results obtained are both meaningful and achievable within the available timeframe.

Chapter 3

System Design and Control Implementation

The objective of this chapter is to present the architecture of the developed system and describe the implementation of each of its subsystems. To this end, the overall architecture and the grid and transformer model are presented first, after which each block of the system is divided into sections: the AC/DC stage, where the droop control, virtual impedance, and the voltage and current control loops of the master and slave converters are described, and the DC/DC stage, where the sizing and control of the Interleaved Buck Converter are presented. With the aim of building a detailed model tailored to the objectives of the present work, the study and modification of a MATLAB/Simulink model [25] was undertaken.

3.1 System Architecture Overview

This section presents the overall architecture of the proposed GFM electrolyzer model before describing each subsystem individually. The AC grid feeds a three-winding transformer in Yd1 configuration, whose two secondary windings, in star and delta connections (denoted Y and Δ in Figure 3.1), supply two Grid-Forming AC/DC converters operating in parallel. These converters are coordinated in a master–slave configuration: the converter connected to the Star secondary acts as the master, implementing the complete grid-forming control chain, while the converter connected to the Delta secondary acts as the slave, operating as a current follower driven by references generated by the master. Both converters feed a shared DC bus, whose voltage, V_t^{dc}, is tightly regulated at its nominal value by the outer voltage control loop of the IBC. The DC voltage at the electrolyzer side, V_h^{dc}, is allowed to deviate within a permissible range to provide flexibility in power consumption. The electrolyzer is represented by an equivalent resistive load at its nominal operating point.

The resulting architecture is depicted in Figure 3.1. On the AC side, the master converter computes its frequency and voltage references through the active and reactive power droops, which are then processed by the AC voltage and AC current controllers and converted to the *abc* frame to

generate the modulation signals. The slave converter receives the current references generated by the master and processes them only through its own AC current controller. On the DC side, the DC voltage controller, together with the feedforward term, defines the current reference of the IBC, which is tracked by the DC current controller to generate the duty cycle applied to the converter supplying the load.

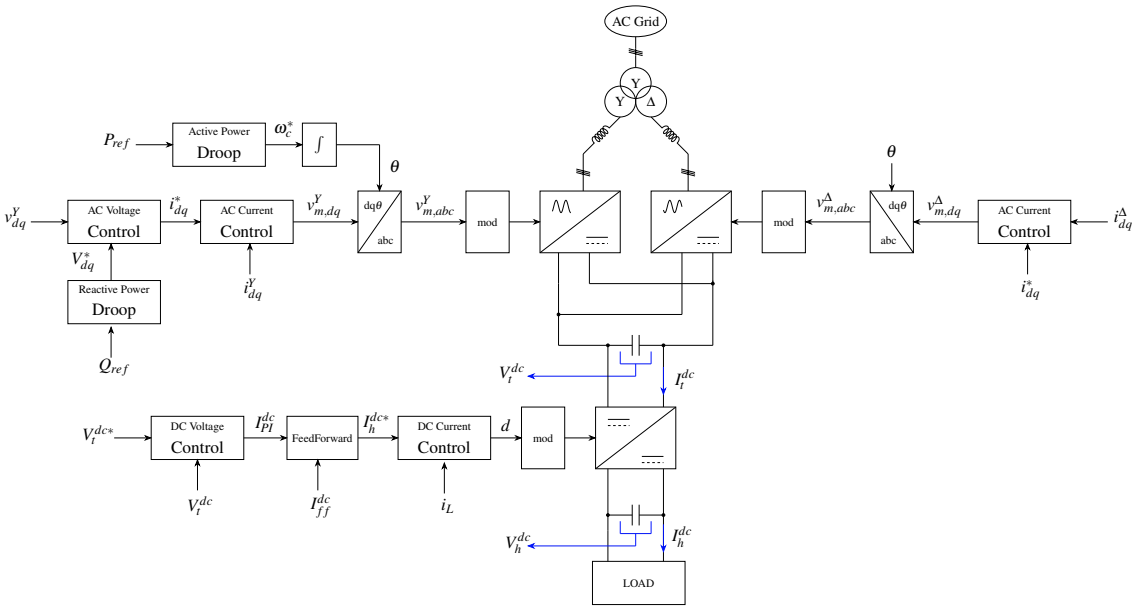


Figure 3.1: System architecture overview.

3.1.1 Test Scenario Definition

The operating conditions under which the system is simulated, including the active and reactive power references commanded to the master converter, P_{ref} and Q_{ref}, and the disturbances applied to the grid, such as voltage sags and frequency events, are defined in a dedicated test scenario script, external to the Simulink model itself. This script specifies the reference values and disturbance profiles for each simulated case, which are then fed into the model as workspace inputs prior to execution. Throughout this chapter, P_{ref} and Q_{ref}, also referred to as $P_{ref,script}$ and $Q_{ref,script}$, are accordingly treated as externally imposed quantities, set by the operator through this script, rather than as outputs computed by the converter's internal control logic.

The following sections describe each subsystem following the same power flow, beginning with the representation of the AC grid and concluding with the DC/DC stage, and the final model implemented and developed in this work.

3.2 Grid and Transformer Model

The AC grid is represented by a Simscape block as a controlled three-phase voltage source, whose magnitude, phase, and frequency are imposed by three scripted profiles read from the

MATLAB workspace: "testCondition.gridVoltageProfile" (magnitude, in per unit), "testCondition.gridPhaseProfile" (phase), and "testCondition.gridFrequencyProfile" (frequency). This structure allows the grid's operating condition to be scripted as a time-varying test input. Figure 3.2 shows the corresponding Simulink implementation.

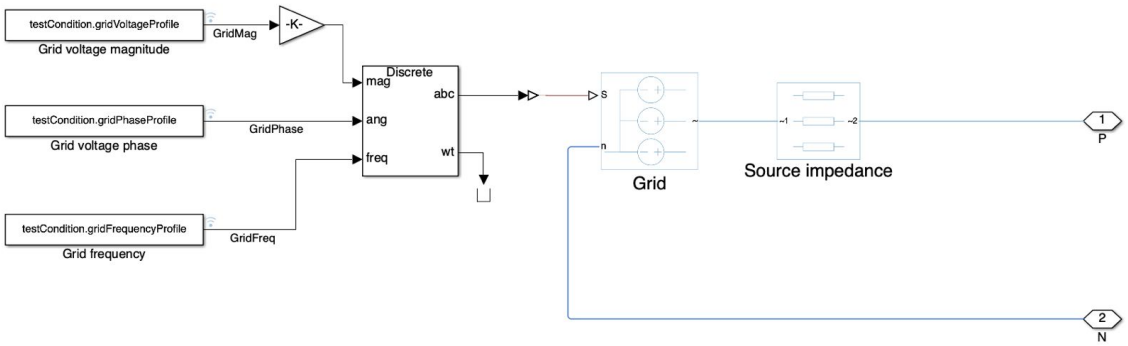


Figure 3.2: Simulink implementation of the AC grid representation.

The per-unit voltage magnitude profile is converted to an instantaneous peak phase-to-neutral voltage, in volts, through the gain

$$K = V_{grid,LL} \cdot \sqrt{\frac{2}{3}}, \tag{3.1}$$

where $V_{grid,LL}$ is the grid's nominal line-to-line RMS voltage. The factor $\sqrt{2/3}$ converts the nominal RMS line-to-line voltage to a peak phase-to-neutral amplitude ($V_{grid,LL} \cdot \sqrt{2}/\sqrt{3}$), as required by the input of the Sine Wave Generator (Three-Phase) block.

The scaled magnitude, together with the phase and frequency profiles, feeds the Sine Wave Generator (Three-Phase) block, which generates the instantaneous three-phase reference waveform. This reference drives the Controlled Voltage Source (Three-Phase) block, representing the ideal upstream grid voltage. The source is followed by a fixed Source Impedance block, parameterized directly in terms of SCR and X/R ratio, representing the finite short-circuit strength of the upstream network – these are the same grid strength parameters reported in the Test Setup of Section 4.1.3.

The transformer used in the simulation is a "Three-Winding Transformer (Three-Phase)" block from Simulink. The predefined parameters were retained for the winding resistances and inductances, and the only modifications made were to the winding voltages, 11 kV at the primary winding (star-connected to the grid) and 415 V at both secondary windings (connected to the converters, one in Star and the other in Delta), the nominal frequency, 50 Hz, and the rated power,

500 kVA.

The selection of a three-winding transformer with a Yd1 vector group provides necessary galvanic isolation and a clean baseline for static phase compensation. As stated in Section 3.1, each winding will be connected to a different converter to form a parallel master–slave configuration. This power conditioning topology is highly beneficial for green hydrogen applications. According to recent literature, advanced multi-converter architectures are essential to handle the high current and stable DC voltage demands of industrial electrolyzers [26]. By interfacing this parallel system with a downstream DC-DC stage, the configuration actively minimizes current ripple on the common DC bus [26]. This tight current regulation is crucial to prevent cell degradation, extend the operational lifetime of the electrolyzer stack, and optimize overall energy efficiency [26].

3.3 AC/DC Stage: Grid-Forming Converter and Master–Slave Operation

This section describes the implementation of the AC/DC stage, which consists of two Grid-Forming converters connected in parallel and sharing a common DC bus. The converters operate according to a master–slave architecture, in which the master converter, connected to the Star secondary winding of the transformer, implements the complete Grid-Forming control strategy. The slave converter, connected to the Delta secondary winding, operates as a current follower by tracking the current references generated by the master converter. The objective of this section is to present the implementation of the proposed Grid-Forming control architecture together with the master–slave coordination strategy adopted for the parallel operation of both converters.

Both converters are implemented in Simulink using the "Converter (Three-Phase)" block. The block is configured with the "Detailed model – switching devices" fidelity level, using the Ideal Semiconductor Switch as the switching device. This configuration constitutes the physical realization of the AFE rectifier stage identified in Section 2.2.1: its six gate-controlled switches, driven through PWM, provide the decoupled dq-frame current regulation capability that distinguishes an AFE from a passive diode or thyristor rectifier, exploited here by the cascaded voltage–current control loops described in Section 3.3.4.

3.3.1 Power Measurements and Passive Component Sizing

One of the key requirements for the proposed Grid-Forming control strategy is the accurate measurement of the instantaneous AC capacitor voltages, v_{abc} and converter currents, i_{abc}, for proper calculation of the active and reactive power exchanged between the Grid-Forming converter and the AC grid. These measurements are essential for the proper operation of the control loops, as they provide the necessary feedback to regulate the converter's output voltage and current [27]. In the present work, the converter currents will be replacing the grid currents for simplification purposes, since the grid is considered stiff and the converter currents are expected to be very close to the grid currents.

Both Grid-Side Converters employ LC output filters to attenuate the switching harmonics generated by the PWM process, ensuring smooth voltage and current waveforms at the converter terminals before their injection into the transformer and the upstream grid. Although both converters are designed according to the same per-unit ripple criterion, the differing peak base currents associated with the Star and Delta transformer windings (Table 3.1) result in different converter-side inductance values for the master (Star) and slave (Delta) converters.

The converter-side inductance is selected to limit the switching current ripple. A commonly adopted design criterion is to restrict the peak-to-peak current ripple to less than 40% of the converter rated current [28]. The corresponding current ripple is given by Equation 3.2 [28]:

$$\frac{\Delta I}{\hat{I}_b} = \frac{V_t^{dc}}{4 L f_s \hat{I}_b}, \tag{3.2}$$

For the master converter, using $\hat{I}_b^Y = 1475.68$ A and $L^Y = 0.7$ mH,

$$\frac{\Delta I}{\hat{I}_b^Y} = \frac{800}{4 \times 0.7 \times 10^{-3} \times 5000 \times 1475.68} \approx 3.87\%. \tag{3.3}$$

For the slave converter, the inductor is designed to achieve the same current ripple ratio, using the corresponding peak base current $\hat{I}_b^\Delta = 852.03$ A. Solving Equation 3.2 for L^Δ,

$$L^\Delta = \frac{V_t^{dc}}{4 f_s \left(\frac{\Delta I}{\hat{I}_b}\right) \hat{I}_b^\Delta} = \frac{800}{4 \times 5000 \times 0.0387 \times 852.03} \approx 1.212 \text{ mH}. \tag{3.4}$$

Both resulting current ripples remain well below the adopted 40% design limit, confirming that the selected inductances provide adequate attenuation of the switching harmonics for both converters.

The filter capacitor is selected to attenuate the switching voltage harmonics while limiting the reactive power absorbed at the fundamental frequency. A widely adopted criterion is to limit the reactive power absorbed by the capacitor to less than 5% of the converter rated apparent power [28]. The corresponding upper limit is given by Equation 3.5 [28]:

$$C_f \leq \frac{0.05 S_b}{3 V_s^2 \omega_{nom}}, \tag{3.5}$$

For the Star (master) converter, the relevant voltage is the phase-to-neutral RMS voltage, $V_s^Y = V_{LL}/\sqrt{3} \approx 239.6$ V, which yields

$$C_f^Y \leq 462 \ \mu\text{F}. \tag{3.6}$$

For the Delta (slave) converter, since the converter windings are delta-connected, the voltage across each filter branch corresponds to the line-to-line RMS voltage, $V_s^\Delta = V_{LL} \approx 415$ V, which yields the more restrictive limit

$$C_f^\Delta \leq 154 \ \mu\text{F}. \tag{3.7}$$

The selected capacitance of 31.8 μF is common to both converters and lies well below both calculated upper limits, satisfying the adopted reactive power criterion for the Star and Delta output filters alike.

For the calculation of the instantaneous active and reactive power, a "Power Measurement (Three-Phase)" Simulink block uses v_{abc}, in volts, and i_{abc}, in amperes, as inputs to compute the instantaneous active and reactive power of the converters, generating both Star and Delta measurements, P^{Y}_{meas}, Q^{Y}_{meas}, P^{Δ}_{meas}, and Q^{Δ}_{meas}, respectively, expressed directly in SI units (W and var). With the purpose of feeding the Active Power and Reactive Power droop control loops, these SI-unit measurements are summed to obtain the total active and reactive power exchanged between the AC/DC stage and the grid,

$$P_{meas,total} = P^{Y}_{meas} + P^{\Delta}_{meas}, \qquad Q_{meas,total} = Q^{Y}_{meas} + Q^{\Delta}_{meas}, \tag{3.8}$$

both expressed in SI units. It is only after this summation that the resulting totals are converted to per-unit, by dividing them by the base power of the system, S_b, as defined in Table 3.1. The resulting quantities, $P_{meas,total}/S_b$ and $Q_{meas,total}/S_b$, are then used as inputs to the respective droop control loops.

This SI-based summation is not to be confused with the per-unit conversion applied to v_{abc} and i_{abc} prior to the Park transformation described above. Since the Star and Delta secondary windings of the transformer present different voltage relationships with respect to the system's line voltage, V_{LL}, their instantaneous voltage and current measurements cannot be converted to per-unit using a common base. The Star winding is star-connected, so its phase quantities correspond to the phase-to-neutral voltage; the Delta winding, in contrast, is delta-connected, so its phase quantities correspond directly to the phase-to-phase (line) voltage. Consequently, two distinct sets of peak per-unit bases are defined, one for each converter, sharing the same base power $S_b = 500$ kVA. These are summarized in Table 3.1.

Table 3.1: Peak per-unit base values adopted for the Star (master) and Delta (slave) converters.

Base Quantity	**Winding**	**Expression**	**Value**
Base power, S_b	Star / Delta	—	500 kVA
Base voltage (peak), $\hat{V}^{Y}_{b}$	Star	$V_{LL}\sqrt{2}/\sqrt{3}$	338.85 V
Base current (peak), $\hat{I}^{Y}_{b}$	Star	$S_b/\hat{V}^{Y}_{b}$	1475.68 A
Base voltage (peak), $\hat{V}^{\Delta}_{b}$	Delta	$V_{LL}\sqrt{2}$	586.90 V
Base current (peak), $\hat{I}^{\Delta}_{b}$	Delta	$S_b/\hat{V}^{\Delta}_{b}$	852.03 A

The Star base voltage, $\hat{V}^{Y}_{b}$, reflects the peak phase-to-neutral voltage seen by the star-connected converter, while the Delta base voltage, $\hat{V}^{\Delta}_{b}$, reflects the peak phase-to-phase voltage seen by the delta-connected converter, the two differing by a factor of $\sqrt{3}$. Each base set, $\hat{V}^{Y}_{b}/\hat{I}^{Y}_{b}$ and $\hat{V}^{\Delta}_{b}/\hat{I}^{\Delta}_{b}$, is used exclusively to convert the corresponding converter's v_{abc} and i_{abc} measurements to per-unit prior to the Park transformation illustrated in Figure 3.3; the active and reactive power totals used

by the droop loops, by contrast, are computed entirely in SI units, as given by Equation 3.8, and are converted to per-unit only once, after summation, using the common base power S_b.

The block diagram of the power measurement implementation is shown in Figure 3.3. The left blocks transform the three-phase AC voltages, v_{abc}, and currents, i_{abc}, into their individual dq components, v_d, v_q, i_d, and i_q, while the right block computes the instantaneous active and reactive power of each converter, P_{meas} and Q_{meas}, from the three-phase measurements.

At the same time, it is necessary to transform the AC into the dq synchronous reference frame using the Park transformation block present in the software. This transformation simplifies the analysis and control of three-phase systems by converting the three-phase quantities into two orthogonal components, d and q. The block receives, as inputs, the three-phase AC voltages and currents in pu, and the angle θ, which will be discussed in Section 3.3.2, in radians. To achieve that, the AC variables are transformed to pu by dividing them by their respective base values, as defined in Table 3.1. The resulting dq components, v_d, v_q, i_d, and i_q, are then computed and used in the subsequent control calculations.

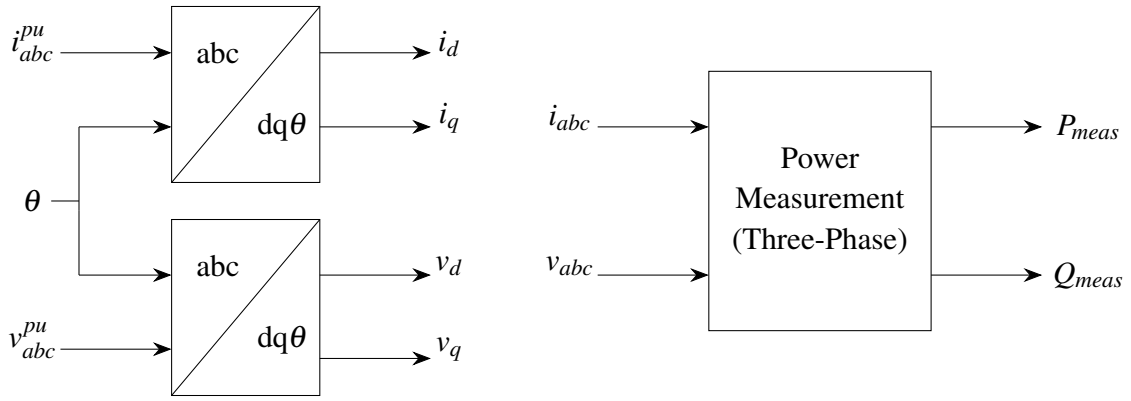


Figure 3.3: Block diagram of dq-component and power computation from the master converter's three-phase measurements.

3.3.2 Droop Control

Consistent with the comparative analysis and control strategy selection presented in Section 2.3.3, the Grid-Forming control architecture implemented in this work is based on the filtered active and reactive power droop strategy presented in Section 2.3.2.2. Since the AC/DC stage consists of two converters operating in a master–slave configuration, only the master converter executes the complete Grid-Forming control algorithm. The implementation of the active power droop control loop is illustrated in Figure 3.4.

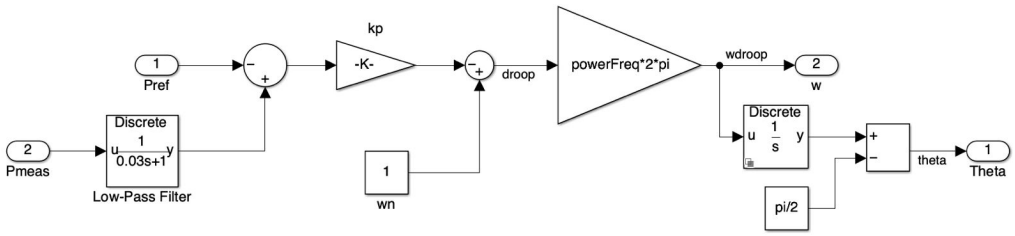


Figure 3.4: Implementation of the P–f droop control loop.

The active power control loop determines the converter operating frequency from the mismatch between the total active power reference, P_{ref}, and the total measured active power, $P_{meas,total}$. The measured power is filtered through a first-order low-pass filter before being processed by the active power droop law,

$$\omega_c^* = m_p \left(P_{ref} - G_p(s) P_{meas,total}\right) + \omega_{nom}, \tag{3.9}$$

where

$$G_p(s) = \frac{1}{\tau_p s + 1} \tag{3.10}$$

is the low-pass filter applied to the active power measurement, with a time constant $\tau_p = 0.03$ s. The resulting angular frequency is integrated to generate the converter voltage angle used by the inner control loops.

The reactive power control loop follows the same implementation principle. The total measured reactive power, $Q_{meas,total}$, is filtered through a first-order low-pass filter, and a droop gain, n_q, generates the voltage reference in the d-axis from its deviation with respect to the total reactive power reference, Q_{ref}, following the reactive power droop law,

$$V_d^* = n_q \left(Q_{ref} - G_q(s)\, Q_{meas,total}\right) + V_{nom}, \tag{3.11}$$

while the q-axis voltage reference is set to zero, $V_q^* = 0$. The filter

$$G_q(s) = \frac{1}{\tau_q s + 1} \tag{3.12}$$

sets the speed at which the voltage reference reacts to variations in the measured reactive power: a larger time constant produces a slower and smoother response, whereas a smaller one allows the droop to react faster, at the cost of a weaker attenuation of the measurement ripple. In this work,

$\tau_q = 0.001$ s was adopted, so that the Q–V droop responds quickly to voltage disturbances, with the filter acting mainly to attenuate the high-frequency ripple of the measured reactive power. This contrasts with the active power loop, in which the larger time constant $\tau_p = 0.03$ s is deliberately chosen to introduce the inertia-like behavior discussed in Section 2.3.2.2.
In that way, if the grid's voltage goes higher or lower than the nominal value, the converters will absorb or inject reactive power, respectively, to provide voltage support to the grid [8]. The following Figure 3.5 illustrates the implementation of the Q–V droop control loop [8], [13], [29].

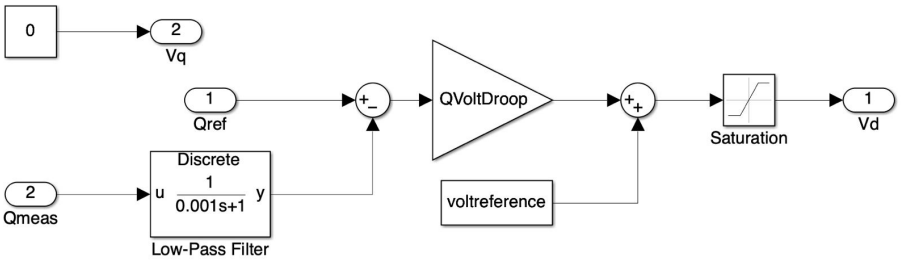


Figure 3.5: Implementation of the Q–V droop control loop.

To limit the voltage at which the converter can operate, a saturation block is applied to the control output. This limit corresponds to the ratio between the maximum peak phase voltage that the two-level converter can synthesize in the linear modulation region, $V_t^{dc*}/2$, and the peak phase-to-neutral base voltage, $\sqrt{2/3}V_{LL}$ (Table 3.1), preventing the droop from requesting a voltage that the available DC bus voltage cannot provide:

$$\pm \frac{V_t^{dc*}/2}{\sqrt{\frac{2}{3}}V_{LL}} \tag{3.13}$$

For $V_t^{dc*} = 800$ V, this corresponds to ± 1.18 pu.

Together, the active and reactive power droop loops define the frequency and voltage magnitude references used to synthesize the converter AC voltage.

The frequency and voltage references generated by the master controller are subsequently supplied to the inner voltage and current control loops described in the following subsection.

3.3.3 Virtual Impedance for Current Limitation

As referred in Section 2.4.4, Virtual Impedance is the selected method to act on the current limitation. This method aims to modify the voltage reference seen by the inner control loops when the output current exceeds its normal value. By adjusting the voltage magnitude, the converter can effectively limit the output current to keep it within a predefined limit. This method introduces a

VI into the system that dynamically adjusts based on the output current. When the current exceeds a certain threshold, the VI is modified to increase the effective impedance seen by the grid [30], [31]. Hence, the VI control proposed in [31], [32] is adopted in this work, as shown in Figure 3.6. The VI is implemented in three main phases. The first phase relies on the overcurrent detection and activation, which is triggered when the current exceeds a predefined threshold (I_n). The second phase involves the calculation of the VI, which is based on the current deviation from the threshold and the desired impedance characteristics. Finally, the third phase applies the calculated VI to adjust the output voltage magnitude, effectively limiting the output current.

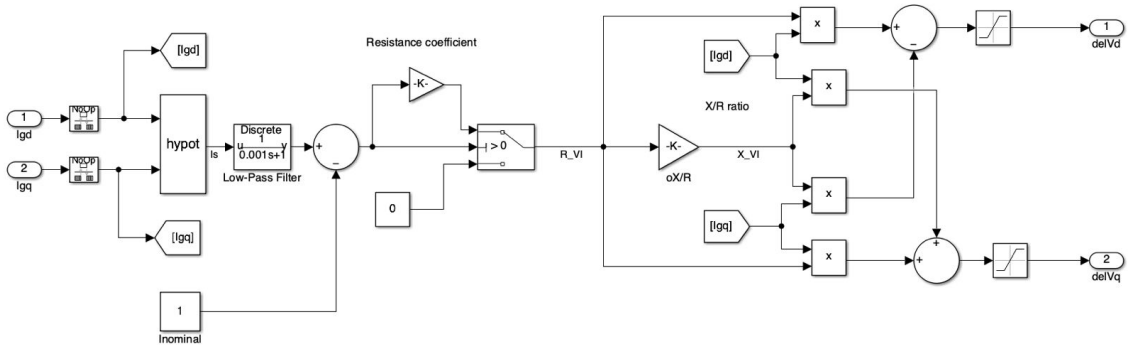


Figure 3.6: Implementation of the Virtual Impedance control for current limitation, adapted from [31].

The expressions of X_{VI}, and R_{VI} are given by Equations 3.14 and 3.15, respectively:

$$X_{VI} = \begin{cases} k_{VI}\,\sigma_{X/R}\,\delta I, & \text{if } \delta I > 0, \\ 0, & \text{if } \delta I \leq 0, \end{cases} \tag{3.14}$$

$$R_{VI} = \frac{X_{VI}}{\sigma_{X/R}} \tag{3.15}$$

The proportional gain k_{VI} defines the magnitude of the VI and, consequently, the level to which the converter current is limited during overcurrent conditions, keeping it below the maximum allowable value, I_{max}. The parameter $\sigma_{X/R}$, in turn, sets the X/R ratio of the virtual impedance, shaping its dynamic response.

When the VI is triggered, control calculates the deviation values, δv_d and δv_q, which will be later used in the new master's AC voltage reference calculation. The expressions for δv_d and δv_q are given by the following equations [30], [31], [32]:

$$\delta v_d = R_{VI}\, i_{gd} - X_{VI}\, i_{gq} \tag{3.16}$$

$$\delta v_q = R_{VI}\, i_{gq} + X_{VI}\, i_{gd} \tag{3.17}$$

3.3.4 Voltage and Current Control

The Grid-Forming droop controllers presented in Section 3.3.2 generate the voltage magnitude and frequency references required to regulate the converter output. These references are subsequently processed by cascaded voltage and current control loops. The outer voltage loop regulates the converter output voltage, whereas the inner current loop provides fast current regulation through the converter-side inductor, ensuring accurate reference tracking and a stable dynamic response.

The cascaded voltage–current control architecture adopted in this work is based on the implementation proposed in [8], [13]. This architecture is widely employed in Grid-Forming converters because it provides instantaneous voltage regulation while enabling fast current control and inherent current-limiting capability through the inner control loop. Although simplified single-loop implementations have been reported in the literature, the absence of a dedicated voltage control loop may compromise voltage quality under nonlinear or unbalanced loading conditions, whereas removing the current loop requires additional considerations regarding current limitation and controller design [27]. Consequently, the cascaded voltage–current structure represents a robust and well-established solution for Grid-Forming applications.

3.3.4.1 Voltage Outer Loop Control

As discussed in the literature, the activation of the VI modifies the voltage references in the synchronous dq reference frame in order to limit the converter output current. The resulting voltage references are given by Equations 3.18 and 3.19,

$$v_{d,ref} = V_d^* - \delta v_d \tag{3.18}$$

$$v_{q,ref} = V_q^* - \delta v_q \tag{3.19}$$

Once the adjusted voltage references have been obtained, they are compared with the measured converter voltages, v_d and v_q, to determine the corresponding voltage errors, as can be seen in Figure 3.7. Before entering the control loop, the measured voltages are filtered using first-order low-pass filters to attenuate the high-frequency switching ripple and measurement noise. This prevents high-frequency components from propagating to the PI controllers, improving the robustness of the control system while preserving the fundamental-frequency component of the measured signals.

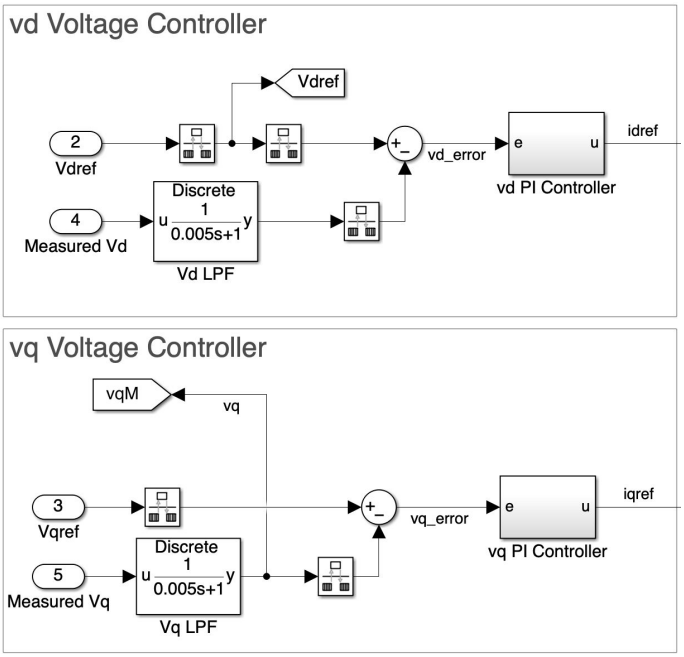


Figure 3.7: Implementation of the outer voltage control loop, including low-pass filtering of the measured voltages and PI controllers used to regulate the d- and q-axis voltage components.

The following Table 3.2 shows the values used for the gains in Vd and Vq controller, which were tuned to obtain a stable and well-damped tracking of the voltage references.

Table 3.2: Vd and Vq controller gains.

Controller	**Parameter**	**Value**
Vd PI Controller	K_p	3
	K_i	180
Vq PI Controller	K_p	3
	K_i	180

3.3.4.2 Current Inner Loop Control

The filtered voltage errors are then processed by PI controllers, whose outputs define the current references, i_d^* and i_q^*. These references are subsequently compared with the measured converter currents, i_d and i_q, forming the inner current control loop.

To compensate for the cross-coupling introduced by the synchronous rotating reference frame, decoupling terms are incorporated into the current control loop [30], [31]. Specifically, the terms $+\omega L i_q$ and $-\omega L i_d$ compensate the coupling between the d- and q-axis current dynamics, allowing each current component to be regulated independently while improving the controller dynamic response during fast transients.

In addition, the voltage references given by Equations 3.18 and 3.19 are introduced as feed-forward terms. A feedforward term injects into the control action a signal derived from a known

reference or measurable quantity, so that its effect is compensated before an error appears at the feedback loop, which then only has to correct the residual deviation [33]. Here, this reduces the control effort required from the PI current controllers and improves the transient response of the converter. Consequently, the voltage references applied to the PWM modulator are given by Equations 3.20 and 3.21:

$$v_{m,d} = v_{PI,d} + \omega L i_q + v_{d,ref}, \tag{3.20}$$

$$v_{m,q} = v_{PI,q} - \omega L i_d + v_{q,ref}, \tag{3.21}$$

where $v_{PI,d}$ and $v_{PI,q}$ denote the outputs of the PI current controllers, $v_{d,ref}$ and $v_{q,ref}$ are the voltage references given by Equations 3.18 and 3.19, and $v_{m,d}$ and $v_{m,q}$ are the resulting modulating voltages.

The following Figure 3.8 demonstrates the implementation of the inner current control loop, including the decoupling and feedforward terms, as well as the PI controllers used to regulate the d- and q-axis currents.

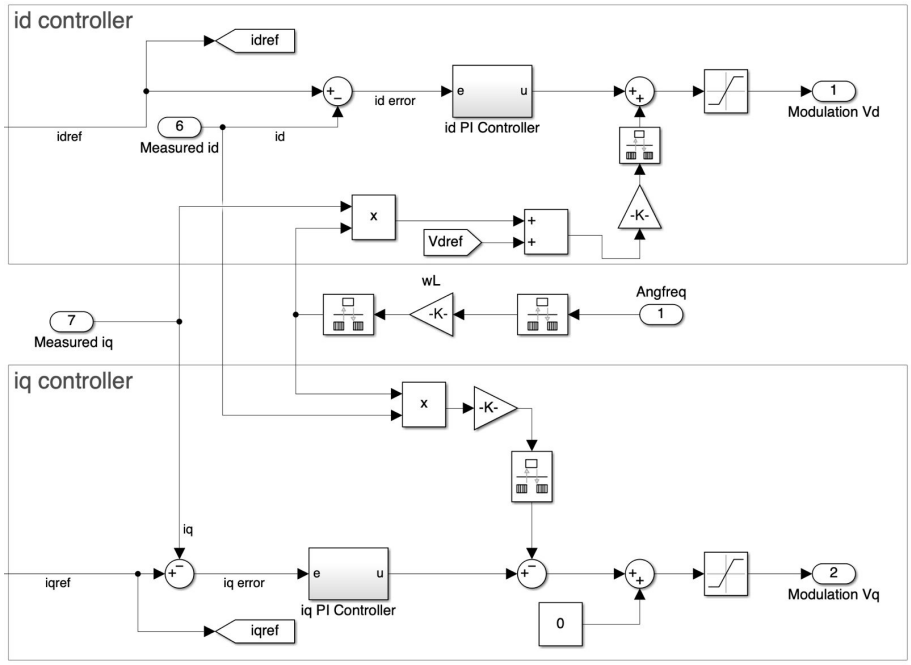


Figure 3.8: Implementation of the inner current control loop, including decoupling and feedforward terms, as well as PI controllers used to generate the d- and q-axis modulating voltages.

The gains presented in Table 3.3 were tuned following the same methodology described in Section 3.3.4.1.

Table 3.3: Id and Iq controller gains used on the master converter.

Controller	Parameter	Value
Id PI Controller	K_p	1.5
	K_i	10
Iq PI Controller	K_p	1.5
	K_i	10

Finally, the decoupled voltage references are normalized with respect to the DC bus voltage and supplied to the "Inverse Park Transform" block, which converts the dq voltage references back to the three-phase abc reference frame. The resulting three-phase voltage references are then provided to the PWM modulator, which generates the gating signals applied to the converter switching devices.

3.3.5 Master–Slave Coordination

Once the master converter establishes the AC subgrid voltage and frequency through its GFM control scheme [34], its inner voltage controller generates the current references (i_d^* and i_q^*) [34]. These reference signals are transmitted to the slave converter, which operates as a current follower [34], [35]. Figure 3.9 shows the implementation of that strategy:

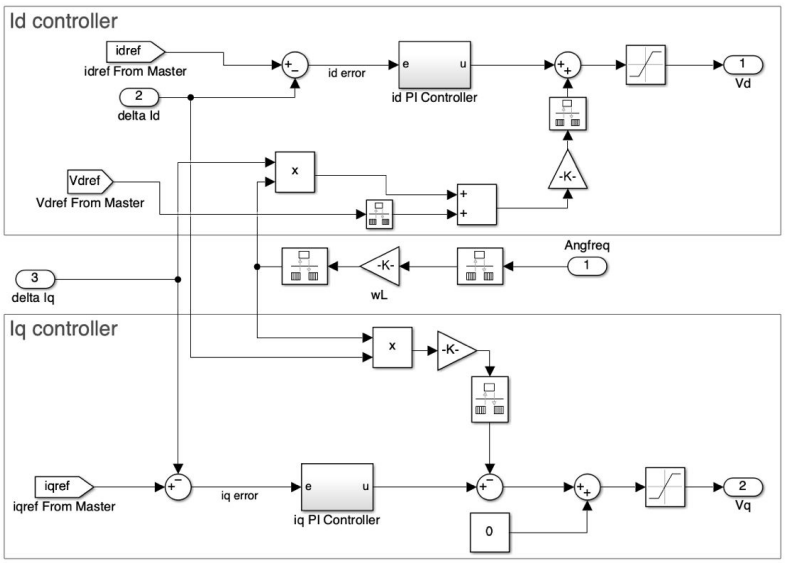


Figure 3.9: Implementation of the current follower strategy for the slave converter.

To ensure absolute coordinate frame consistency ($\Delta\theta = 0$) while accounting for the physical phase shift introduced by the three-winding transformer connection, a static phase-shift compensation is implemented. The master converter is connected to the Star winding, serving as the system's phase reference, whereas the slave converter is connected to the Delta winding. For

a standard Yd1 vector group, the positive-sequence fundamental voltage on the delta-connected winding (LV side) lags the star-connected winding (HV side) by exactly 30° (or $\pi/6$ rad).

Therefore, instead of employing a local dynamic PLL at the slave unit, which is highly susceptible to phase-tracking delays, grid harmonic distortion, and control loop interactions [35], the slave's synchronization angle (θ_{slave}) is directly and instantaneously calculated using static feedforward:

$$\theta_{slave} = \theta_{master} - \frac{\pi}{6} \tag{3.22}$$

Using this mathematically compensated reference angle, the slave's local measurement stage projects its measured output currents into its own synchronous dq-frame (i_d and i_q). The current tracking errors are subsequently processed by decoupled PI current controllers. To ensure symmetrical dynamic behavior, the cross-coupling decoupling terms and voltage feedforward compensation are structured identically to the master's inner loop shown in Section 3.3.4.2.

The resulting dq control voltages are then transformed back to the stationary frame utilizing the same compensated angle (θ_{slave}) and forwarded to the slave's PWM block. This tightly coordinated, feedforward-aligned reference frame alignment guarantees highly accurate current tracking, preventing circulating active and reactive currents between the transformer windings [34], [35].

The proportional and integral gains of the slave's current controller, detailed in Table 3.4, were empirically tuned to guarantee an optimal trade-off between fast dynamic tracking and robustness under step-load changes in the downstream DC/DC converter and simulated electrolyzer load.

Table 3.4: Id and Iq controller gains used on the slave converter.

Controller	**Parameter**	**Value**
Id PI Controller	K_p	1.5
	K_i	10
Iq PI Controller	K_p	1.5
	K_i	10

3.4 DC/DC Stage: Interleaved Buck Converter Design and Control

This section describes the design and control of the DC/DC stage, which interfaces the shared DC bus, regulated by the AC/DC converters described in Section 3.3, with the electrolyzer load. This interface is realized through an IBC, tasked with stepping down the DC bus voltage to the level required by the electrolyzer while limiting the current ripple delivered to it. The objective of this section is to present the equivalent load used to represent the electrolyzer, the sizing of the IBC's passive components, and the control architecture adopted to regulate the DC bus voltage while ensuring balanced current sharing among the converter's parallel branches. Section 3.4.1 introduces the electrolyzer-equivalent load and the reasoning behind its adopted value; Section 3.4.2 details the sizing of the branch inductors and output capacitor from the converter's ripple equations; and

Section 3.4.3 presents the cascaded voltage–current control structure, including the disturbance feedforward term and the interleaving strategy adopted to minimize the output current ripple.

3.4.1 Electrolyzer-Equivalent Load Characterization

As discussed in Section 2.1, the steady-state voltage-current characteristic of a PEM electrolyzer stack is governed by a non-linear combination of activation, ohmic, and concentration overpotentials, while its transient response is further shaped by the double-layer capacitance of the electrode-electrolyte interface. Reproducing this behavior in full detail, however, is not required to meet the objectives of this dissertation, which center on validating the proposed Grid-Forming control strategy and the interaction between the electrical subsystems of the converter chain, rather than on characterizing the electrochemical behavior of the electrolyzer itself. This characteristic curve can nonetheless be evaluated at a single, fixed operating point, at which the stack's terminal voltage and current admit a well-defined ratio, a reduction consistent with the practice, adopted in recent PEM electrolyzer power-electronics literature, of deriving a control-oriented equivalent resistance directly from the stack's static polarization curve, given that the double-layer capacitance dynamics exhibit time constants several orders of magnitude slower than the converter's control bandwidth [12], [19]. Accordingly, the electrolyzer is represented in this work by an equivalent resistance, R_{eq}, corresponding precisely to this operating point on the voltage-current characteristic introduced above, rather than to an independently assumed or arbitrary value. Unlike the operating-point-dependent, adaptively recalculated resistance used for control design in [19], the value adopted here is kept fixed at the nominal operating point throughout, consistent with the dissertation's focus on validating the grid-forming control architecture rather than the electrolyzer's own operating-point-dependent dynamics.

The value of R_{eq} is obtained from a simplified sizing of the electrolyzer stack, based on the nominal DC voltage at the electrolyzer side, $V_h^{dc} = 400$ V, and the rated electrolyzer power, $P_{el} = 250$ kW, adopted throughout Section 3.4.2. Assuming a stack composed of N_{cells} cells connected in series, each operating at a nominal cell voltage $V_{cell} = 1.84$ V, the required number of cells is

$$N_{cells} = \frac{V_h^{dc}}{V_{cell}} = \frac{400}{1.84} \approx 217.4, \tag{3.23}$$

which is rounded to the nearest integer, $N_{cells} = 217$, yielding an actual stack voltage of $217 \times 1.84 = 399.28$ V, within 0.2% of the nominal design value and therefore adopted as $V_{stack} \approx V_h^{dc} = 400$ V for consistency with the remainder of this chapter.

The nominal stack current is obtained from the rated electrolyzer power and the nominal stack voltage,

$$I_{stack} = \frac{P_{el}}{V_h^{dc}} = \frac{250\,000}{400} = 625 \text{ A}, \tag{3.24}$$

consistent with the nominal branch current adopted for the IBC sizing in Section 3.4.2 ($I_L =$ 208.33 A per branch, i.e. $I_{stack}/3$). The equivalent resistance is then obtained directly from these nominal values as

$$R_{eq} = \frac{V_h^{dc}}{I_{stack}} = \frac{400}{625} = 0.64\ \Omega, \tag{3.25}$$

which is the value adopted for the resistive load throughout the simulations presented in Chapter 4, and against which the measured equivalent resistance is later compared in Section 4.3.1.

Being represented as a purely resistive equivalent, this load draws only positive active power, $P_h^{dc} = (V_h^{dc})^2/R_{eq} \geq 0$, at unity power factor, and therefore reverse active power flow or capacitive/inductive reactive power exchange is, by construction, not possible under normal operation.

3.4.2 Component Sizing

Before discussing the control architecture of the IBC, the passive components of each branch, the inductance L and the output capacitance C, must be sized. These values are determined from the converter's ripple equations and a maximum admissible ripple criterion, and are validated afterwards against the combined output current ripple resulting from the interleaving of the three branches.

3.4.2.1 Conversion Ratio and Ripple Equations

Each branch of the IBC is, individually, a conventional step-down (buck) converter. Its steady-state conversion ratio between the output voltage (V_h^{dc}) and the input DC voltage (V_t^{dc}) is given by the duty cycle D, as shown in Equation 3.26 [17], [36]:

$$\frac{V_h^{dc}}{V_t^{dc}} = D \tag{3.26}$$

The peak-to-peak inductor current ripple, Δi_L, of each branch is given by Equation 3.27 [17], [36]:

$$\Delta i_L = \frac{(1-D)V_h^{dc}}{Lf_s} \tag{3.27}$$

In the system studied in this work, however, it is the shared DC bus voltage V_t^{dc} that is regulated and held approximately constant, while the duty cycle D is the variable adjusted by the control loop to set the operating point. Equation 3.27 is therefore rewritten in terms of V_t^{dc}, substituting $V_h^{dc} = DV_t^{dc}$ from Equation 3.26:

$$\Delta i_L = \frac{D(1-D)V_t^{dc}}{Lf_s} \tag{3.28}$$

where f_s is the switching frequency. The corresponding output capacitance required to limit the peak-to-peak output voltage ripple, ΔV_h^{dc}, for an inductor ripple Δi_L, is given by Equation 3.29 [37]:

$$\Delta V_h^{dc} = \frac{(1-D)V_h^{dc}}{24LCf_s^2} \tag{3.29}$$

Applying the same substitution of V_h^{dc} in terms of V_t^{dc}, Equation 3.29 becomes:

$$\Delta V_h^{dc} = \frac{D(1-D)V_t^{dc}}{24LCf_s^2} \tag{3.30}$$

These expressions are used below to size L and C from a maximum admissible ripple, treating each branch as an independent buck converter operating at the system's nominal duty cycle.

3.4.2.2 Worst-Case Duty Cycle

From Equation 3.28, the ripple is proportional to $D(1-D)$, which reaches its maximum at $D = 0.5$, as shown in Equation 3.31.

$$\frac{d}{dD}\left[D(1-D)\right] = 1-2D = 0 \quad \Rightarrow \quad D = 0.5, \tag{3.31}$$

shows that the branch current ripple is maximized at $D = 0.5$, for a fixed V_t^{dc}. This worst case coincides with the system's nominal operating point ($V_t^{dc} = 800$ V, $V_h^{dc} = 400$ V), so the sizing below is carried out for $D = 0.5$.

3.4.2.3 Inductance and Capacitance Sizing

The branch inductance is sized for a maximum peak-to-peak current ripple of 5% of the nominal branch current, $\Delta i_L < 0.05\, I_L$ [15]. Solving Equation 3.27 for L:

$$L \geq \frac{(1-D)V_h^{dc}}{\Delta i_L f_s} = \frac{(1-D)V_h^{dc}}{0.05\, I_L f_s} \tag{3.32}$$

The output capacitance is sized for a maximum peak-to-peak voltage ripple of 1% of the output voltage, $\Delta V_h^{dc} < 0.01\, V_h^{dc}$ [37]. Solving Equation 3.29 for C, and using the inductance value obtained from Equation 3.32:

$$C \geq \frac{(1-D)V_h^{dc}}{24Lf_s^2\,\Delta V_h^{dc}} = \frac{(1-D)V_h^{dc}}{24Lf_s^2 \cdot 0.01\, V_h^{dc}} \tag{3.33}$$

Using the system's nominal operating point, Equation 3.32 and Equation 3.33 give the inductance and capacitance values adopted for each of the three branches of the IBC. The nominal branch current, I_L, is obtained from the electrolyzer's rated power, $P_{el} = 250$ kW, assuming equal current sharing among the three branches:

$$I_L = \frac{P_{el}}{3V_h^{dc}} = \frac{250\,000}{3 \times 400} = 208.33 \text{ A} \tag{3.34}$$

Table 3.5 summarizes the input parameters, the adopted ripple criteria, and the resulting component values.

Table 3.5: IBC branch sizing: input parameters, ripple criteria, and resulting component values.

Parameter	**Value**	**Source**
Input DC voltage, V_t^{dc}	800 V	Operating point
Output voltage, V_h^{dc}	400 V	Operating point
Duty cycle, D	0.5	Worst case (Eq. 3.31)
Switching frequency, f_s	10 kHz	Operating point
Nominal branch current, I_L	208.33 A	$P_{el}/(3V_h^{dc})$, $P_{el} = 250$ kW
Current ripple criterion	5% of I_L	Adopted criterion
Voltage ripple criterion	1% of V_h^{dc}	Adopted criterion
Branch current ripple, Δi_L	10.42 A	Eq. 3.32
Branch inductance, L	1.92 mH	Eq. 3.32
Output voltage ripple, ΔV_h^{dc}	4.00 V	Eq. 3.33
Output capacitance, C	10.85 μF	Eq. 3.33

3.4.2.4 Simulation-Based Validation

The previous sizing procedure considers each branch independently and therefore predicts the ripple at the branch inductors rather than the ripple delivered to the electrolyzer stack. To verify the overall converter behavior, the simulated waveforms shown in Figure 3.10 are analyzed. The top panel shows the three interleaved branch currents, i_{LP1}, i_{LP2}, and i_{LP3}; the middle panel shows the electrolyzer stack voltage, V_h^{dc}; and the bottom panel shows the combined output current, I_h^{dc}, delivered to the stack after the three branches recombine.

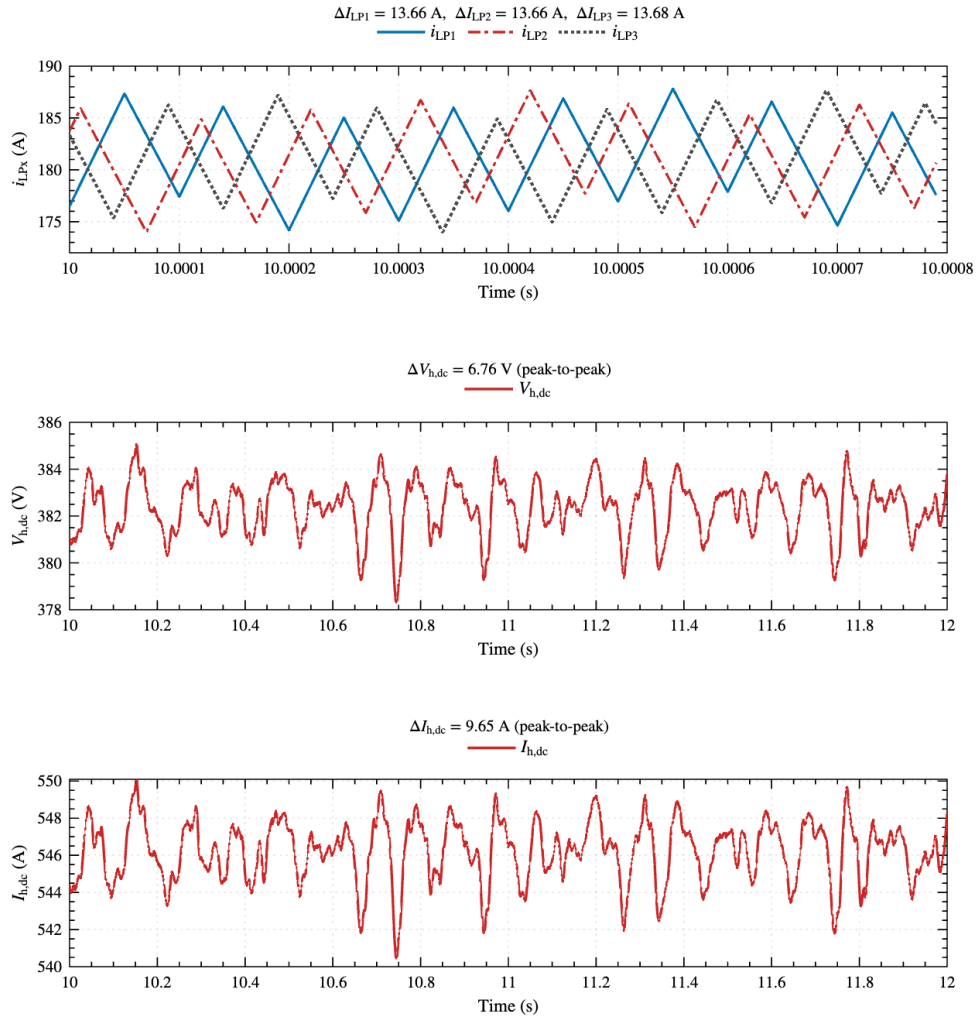


Figure 3.10: Simulated waveforms of the Interleaved Buck Converter: (top) the three interleaved branch currents, i_{LP1}, i_{LP2}, and i_{LP3}; (middle) the electrolyzer stack voltage, V_h^{dc}; and (bottom) the combined output current, I_h^{dc}.

At the simulated operating point, the electrolyzer stack voltage and output current settle around $V_h^{dc} \approx 382$ V and $I_h^{dc} \approx 550$ A, respectively. Both values are slightly below the nominal design point ($V_h^{dc} = 400$ V and $I_h^{dc} = 625$ A), so the power delivered to the electrolyzer-equivalent load is approximately 210 kW rather than the electrolyzer rated power of 250 kW.

The measured peak-to-peak ripple values are $\Delta I_h^{dc} = 9.65$ A and $\Delta V_h^{dc} = 6.76$ V, corresponding to:

$$\frac{\Delta I_h^{dc}}{I_h^{dc}} = \frac{9.65}{549.7} \approx 1.76\%, \qquad \frac{\Delta V_h^{dc}}{V_h^{dc}} = \frac{6.76}{382} \approx 1.77\% \tag{3.35}$$

The output current ripple corresponds to approximately 1.76% of the average current and therefore remains well below the 5% criterion adopted for the inductance sizing. The output voltage ripple reaches approximately 1.77%, exceeding the 1% target adopted during the capacitance sizing stage. Nevertheless, the resulting voltage variation remains limited in absolute magnitude

(6.76 V) and does not adversely affect converter operation. Overall, the ripple components remain at a low percentage of their respective nominal values, indicating that the selected values of L and C provide acceptable performance under the simulated operating conditions.

3.4.3 Control Architecture

The control architecture adopted for the IBC is shown in Figure 3.11. Its objective is to regulate the shared DC bus voltage, V_t^{dc}, represented by the capacitor C_{dc}, while ensuring balanced current sharing among the three converter branches.

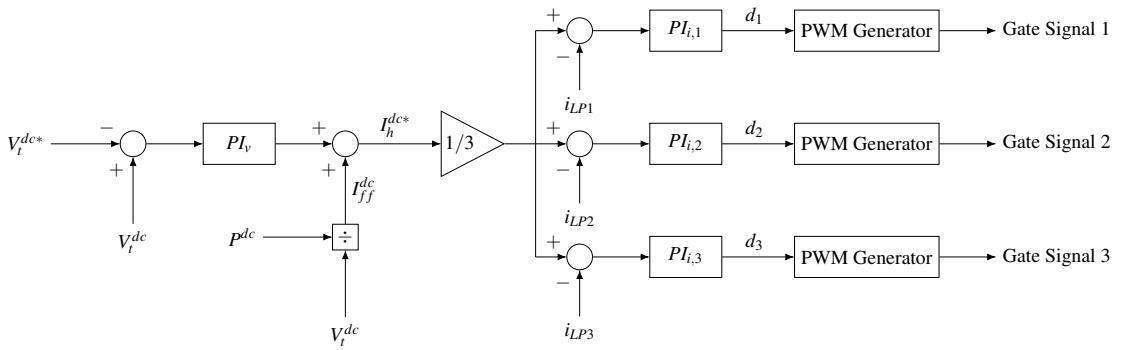


Figure 3.11: Control architecture of the Interleaved Buck Converter.

The converter employs a cascaded voltage–current control structure consisting of an outer voltage loop and three identical inner current loops. The outer loop regulates the DC bus voltage by comparing the measured capacitor voltage, V_t^{dc}, with its reference, V_t^{dc*}. The resulting voltage error is processed by a PI controller, whose output defines the corrective current required from the IBC to restore the DC bus voltage to its reference value.

To improve the dynamic response during changes in the power exchanged between the grid and the DC bus, a feedforward term is added to the output of the voltage controller. Also known as predictive compensation, this term is intended to act in the control variable before the error is detected by the feedback loop, thereby reducing the response time of the system [33].

In this context, the term is obtained from the division of the power delivered by the AC/DC stage to the DC bus, P^{dc}, by the measured DC bus voltage, V_t^{dc}. Assuming negligible losses in the AC/DC stage, P^{dc} is estimated from the total active power measured at the AC side of the Grid-Forming converters, $P^{dc} \approx P_{meas,total}$, and converted into an equivalent DC current according to

$$I_{ff}^{dc} = \frac{P^{dc}}{V_t^{dc}}. \tag{3.36}$$

The feedforward term therefore provides an estimate of the current that the IBC must draw from the DC bus to accommodate the instantaneous power delivered by the Grid-Forming Converter.

This estimated current is added to the output of the voltage PI controller, yielding the total output current reference,

$$I_h^{dc*} = I_{PI}^{dc} + I_{ff}^{dc}, \tag{3.37}$$

where I_{PI}^{dc} denotes the output of the voltage PI controller.

The total current reference is equally distributed among the three converter branches, providing the reference current for each branch inductor. For each branch, the measured inductor current is compared with its corresponding reference, and the resulting current error is processed by an inner PI controller. The output of each controller is applied to the corresponding PWM modulator, which determines the duty cycle of the associated switching device [37].

The three PWM carriers are phase-shifted by $360^\circ/N = 120^\circ$ of the switching period in order to minimize the output current ripple and reduce the required passive component size [36]. Since the PWM generators in Simulink accept this shift as a time delay rather than an angle, the phase shift is converted into an equivalent delay of a fraction of the switching period, $T_s = 1/f_s$:

$$t_{delay,i} = \frac{i-1}{N} T_s = \frac{i-1}{N f_s}, \quad i = 1,2,3, \tag{3.38}$$

where $N = 3$ is the number of converter branches. For $f_s = 10$ kHz, this yields delays of 0, 33.3 and 66.7 μs for the three branches, respectively. As a result, the branch current ripples partially cancel at the converter output, reducing the ripple of the current delivered to the electrolyzer stack.

3.4.3.1 Controller Tuning

The controller gains were determined by iterative tuning in simulation. The tuning process aimed to achieve a stable transient response while maintaining the current control loop approximately one order of magnitude faster than the outer voltage loop, following the conventional bandwidth separation adopted in cascaded control structures.

Table 3.6 summarizes the proportional and integral gains adopted for the voltage and current PI controllers of the IBC control structure.

Table 3.6: IBC controller gains.

Controller	Parameter	Value
Voltage PI	K_p	2
	K_i	8
Current PI	K_p	0.005
	K_i	0.1

3.5 Final Model

Figure 3.12 shows the complete Simulink model resulting from the integration of the subsystems described throughout this chapter.

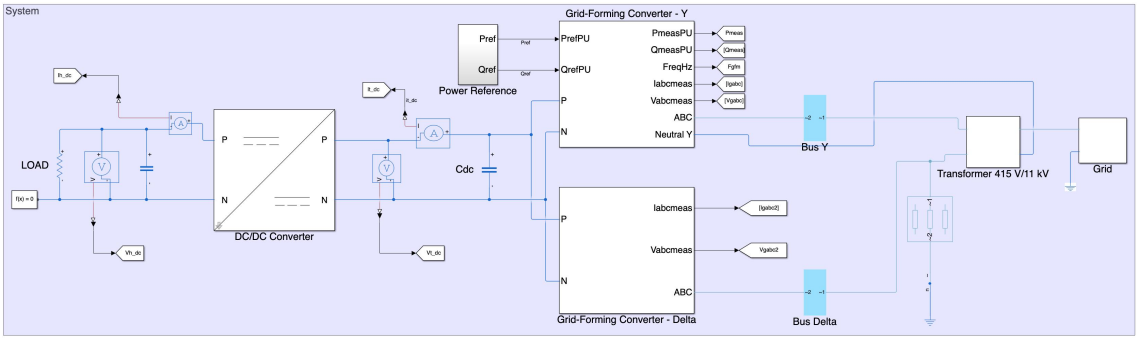


Figure 3.12: Final model developed on Simulink.

The model is organized into three main stages, corresponding to the power path from the grid to the electrolyzer: the AC-side grid-forming stage, the shared DC bus, and the DC/DC conversion stage supplying the electrolyzer load.

The "Grid-Forming Converter – Y", "Grid-Forming Converter – Delta", and "DC/DC Converter" blocks each contain the control subsystems described in the previous sections: the master–slave droop control for the two AC/DC converters, and the interleaved buck converter control for the DC/DC stage.

The AC/DC converters interface with the Star and Delta windings of the transformer through the "Bus Y" and "Bus Delta" connections, respectively. On the DC side, the capacitor C_{dc} represents the shared DC bus, with voltage and current measurements taken at both the input (V_t^{dc}, I_t^{dc}) and output (V_h^{dc}, I_h^{dc}) of the DC/DC converter. The electrolyzer stack is represented by its resistive equivalent R_{eq}, connected at the output of this stage.

A small implementation detail is the high-value resistor (1 MΩ) connected between the Delta winding and ground. Since the delta configuration has no physical neutral, this resistor provides a grounding reference for the solver, without affecting the behavior of the system.

Overall, this model constitutes the complete simulation model used to obtain the results presented in Chapter 4.

Chapter 4

Results and Analysis

This chapter presents and analyzes the simulation results obtained for the grid-forming droop-controlled AC/DC–DC/DC system developed in this work. The chapter is organized into three parts, following the same incremental validation strategy adopted throughout the model's development: each stage is first validated in isolation, before the complete system is assembled and evaluated. Section 4.1 validates the AC/DC master–slave control architecture on its own, using an ideal DC voltage source in place of the DC bus and electrolyzer load, through a four-quadrant test that exercises the P–f and Q–V droop control across the converter's full active and reactive power operating envelope. Section 4.2 then validates the DC/DC stage in isolation, assessing the Interleaved Buck Converter's current-tracking loop and the balanced current sharing among its three interleaved branches. Finally, Section 4.3 evaluates the complete system, with the DC bus, Interleaved Buck Converter, and electrolyzer-equivalent load in place, under normal operating conditions and under grid disturbances, assessing both the AC-side power tracking and the resulting DC-side voltage, current, and power balance across the full conversion chain.

4.1 Control Validation of the AC/DC Master–Slave Operation using a DC Source

Before evaluating the complete converter chain, the AC/DC master–slave control architecture is first validated in isolation, using an ideal DC voltage source in place of the DC/DC stage and electrolyzer-equivalent load. This isolates the droop-based Grid-Forming control and the master–slave current-sharing strategy from the additional dynamics introduced by the IBC and its control, allowing the four-quadrant P–Q operating envelope of the AC/DC stage to be validated on its own terms before the full system is assembled in Section 4.3.

4.1.1 Objective

The AC/DC stage's control architecture is validated independently of the downstream DC/DC and electrolyzer stages, with the converters fed from an ideal, controllable DC voltage source in

place of the full DC bus and Interleaved Buck Converter chain. In this architecture, the master converter's outer control loop combines active power–frequency (P–f) and reactive power–voltage (Q–V) droop, followed by a virtual impedance stage, with cascaded voltage and current control loops that track the resulting reference. The current reference generated by this chain is shared with the slave converter, which does not implement its own droop or virtual impedance logic but instead tracks the shared current reference through its own voltage/current control loop.

Because $P_{ref,script}$ and $Q_{ref,script}$ are commanded exclusively to the master converter, while the total delivered active and reactive power, $P_{meas,total}$ and $Q_{meas,total}$, reflects the combined contribution of both converters, this test validates not only the master's droop-based reference generation but also the slave's ability to correctly follow the shared current reference across the full operating envelope.

Building on the reference test-scenario provided for grid-forming converter validation in Simscape, in which the active and reactive power references are each treated as independent test variables to assess tracking ability, response time, and output voltage fluctuations, the present test extends this principle to a single continuous simulation in which $P_{ref,script}$ and $Q_{ref,script}$ are commanded sequentially through seven steady-state operating points, collectively covering all four quadrants of the P–Q plane (P > 0, Q > 0; P < 0, Q > 0; P < 0, Q < 0; P > 0, Q < 0). Quadrants Q1, Q2 and Q3 are each exercised at two distinct reactive power levels while active power is held fixed, providing a more thorough assessment of the Q–V droop response than a single representative point per quadrant would allow.

As noted in Section 3.4.1, reverse active power flow or capacitive/inductive reactive exchange is not possible for the electrolyzer load in normal operation. The purpose of the four-quadrant test is therefore not to reproduce a condition expected from the electrolyzer, but to validate the master–slave AC/DC control chain as a whole.

4.1.2 Initialization

The simulation begins at $t = 0$ with $P_{ref,script}$ and $Q_{ref,script}$ being also zero, ramping to the first operating point over the interval $[0, 1]$ s. Transitions between all subsequent operating points are likewise commanded as ramps, rather than idealized instantaneous steps, applied directly to $P_{ref,script}$ and $Q_{ref,script}$ in the test script, with a duration of 1 s for all transitions except that between operating points 2 and 3, where the reactive power reference ramp was extended to 4 s. Both the use of ramped (rather than stepped) transitions and their specific durations are implementation choices made for clarity in the resulting transient plots, and are not dictated by any physical constraint (e.g. current-limiting or rate-limiting requirement) of the reference-generation block itself, which is not rate-limited.

The ideal DC voltage source is fixed at its nominal value, $V_t^{dc} = 800$ V, for the entire duration of the simulation, so that the only excitation applied to the system is the sequence of reference changes described in Section 4.1.3.

4.1.3 Test Setup

Both the master and slave converters are connected to a common ideal DC voltage source fixed at $V_t^{dc} = 800$ V, as described in Section 4.1.1. On the AC side, the grid is represented by an ideal voltage source held constant throughout the entire test at its nominal values of $V_{grid} = 1.0$ pu and $f_{grid} = 50$ Hz, with SCR = 2.5 and X/R ratio = 4 also held fixed. This ensures that the sequence of transitions observed in Section 4.1.4 is attributable solely to the commanded changes in $P_{ref,script}$ and $Q_{ref,script}$, and not to any variation in the AC- or DC-side boundary conditions.

Figure 4.1 shows the Simulink implementation of this test setup.

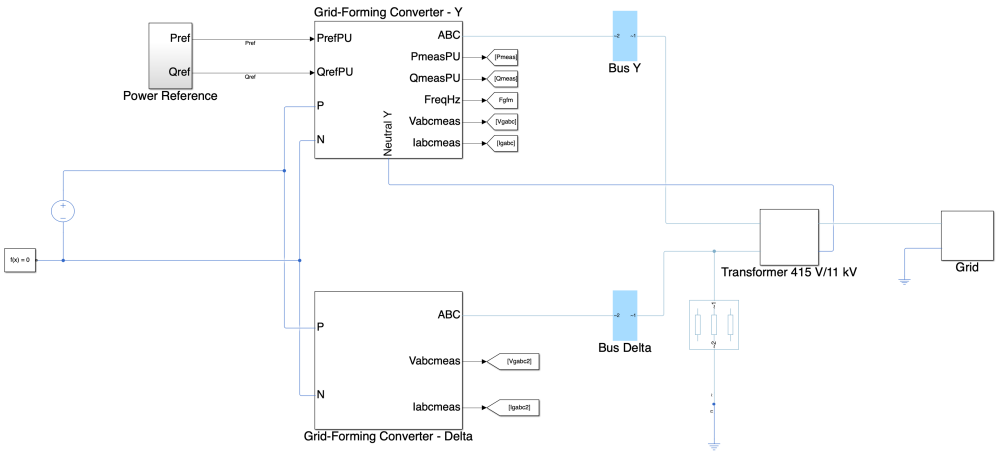


Figure 4.1: Simulink implementation of the isolated AC/DC test setup.

Table 4.1 summarizes the seven steady-state operating points commanded to the converter within the single, continuous 40 s simulation, each maintained for a sufficient interval to allow the converter to reach steady state before the following transition is applied.

Table 4.1: Steady-state (P_{ref}, Q_{ref}) operating points commanded during the four-quadrant test, in chronological order.

Point	Time window (s)	P_{ref} [pu]	Q_{ref} [pu]	Quadrant
1	[1, 5]	+0.6	+0.2	Q1
2	[6, 10]	+0.6	+0.5	Q1
3	[15, 20]	+0.2	−0.2	Q4
4	[21, 25]	−0.5	+0.2	Q2
5	[26, 30]	−0.5	+0.5	Q2
6	[31, 35]	−0.5	−0.2	Q3
7	[36, 40]	−0.2	−0.4	Q3

The measured total active and reactive power ($P_{meas,total}$, $Q_{meas,total}$), reflecting the combined output of the master and slave converters, along with converter frequency and dq-axis voltages/currents, are recorded throughout the full 40 s simulation, allowing both the transition transients and the steady-state tracking accuracy at each of the seven operating points to be evaluated in Section 4.1.4.

4.1.4 Test Results

Having defined the active and reactive power reference values and carried out the respective tests, it can be observed that the master converter is able to accurately control the desired power values and impose the references necessary for both the master and the slave to operate in a coordinated manner. Figure 4.2 shows the system's active power response to the reference changes over time, demonstrating the converter's ability to accurately track the four commanded active power levels, both in transient and steady-state conditions.

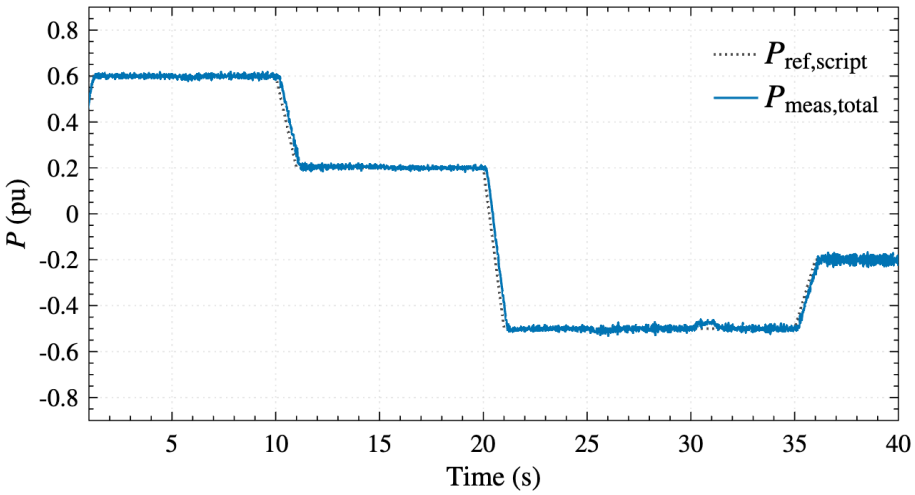


Figure 4.2: Time-domain tracking of the scripted active power reference, $P_{ref,script}$, by the combined master and slave converter output, $P_{meas,total}$, throughout the four-quadrant test of Table 4.1. The converter pair accurately tracks each of the four commanded active power levels ($+0.6$, $+0.2$, -0.5, and -0.2 pu).

As shown in Figure 4.2, $P_{meas,total}$ tracks $P_{ref,script}$ closely throughout the four active power levels, with no discernible steady-state error at any of the four operating points. During the 1 s ramped transitions, the measured power follows the commanded ramp without overshoot, settling to the target value shortly after each ramp's completion. The visible high-frequency ripple superimposed on $P_{meas,total}$ is consistent with switching-related measurement noise rather than a control deficiency, as its amplitude does not correlate with the reference transitions.

Similarly, Figure 4.3 illustrates the system's reactive power response to the reference changes over time, demonstrating the converter's ability to accurately track the four commanded reactive power levels. It should be noted that, in three of the four test segments (Table 4.1), the reactive power reference is changed while the active power reference is held constant, which allows the Q–V droop response to be assessed in isolation, without interference from active power transitions.

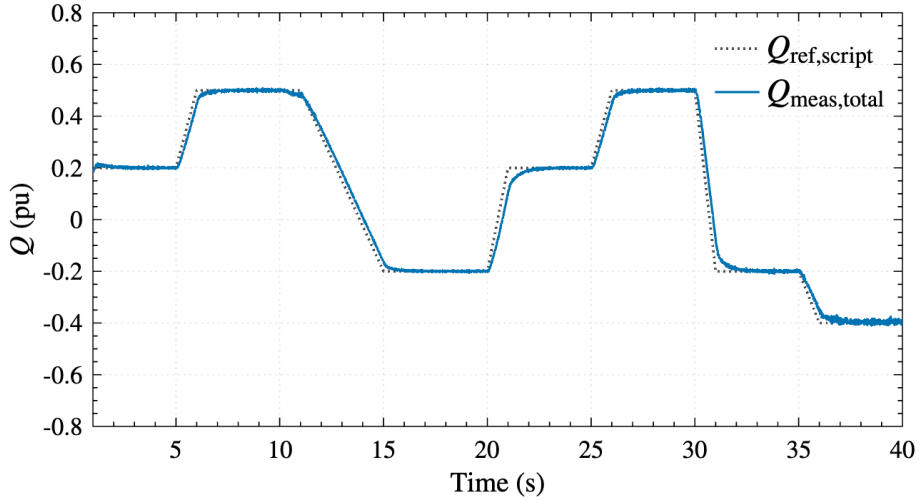


Figure 4.3: Time-domain tracking of the scripted reactive power reference, $Q_{ref,script}$, by the combined master and slave converter output, $Q_{meas,total}$, throughout the four-quadrant test of Table 4.1. The reactive power reference is commanded through four distinct levels ($+0.2$, $+0.5$, -0.2, and -0.4 pu), each combined with a different active power set-point, allowing the Q–V droop response to be assessed independently of the active power operating point.

As with the active power response, $Q_{meas,total}$ tracks $Q_{ref,script}$ closely across all four reactive power levels, with no discernible steady-state error. The transition between the second and third operating points (Table 4.1) uses an extended 4 s ramp rather than the 1 s ramp applied elsewhere; the measured response follows this slower ramp smoothly, confirming that the Q–V droop response is not rate-limited by the control implementation itself, but only by the commanded reference profile.

Given the P–f droop relationship implemented in the master converter's outer control loop (Section 3.3.2), the accurate tracking of the active power reference shown in Figure 4.2 is expected to be reflected in a correspondingly stable grid frequency. Figure 4.4 confirms this: despite active power reference transitions of up to 1.1 pu (between the -0.5 pu and $+0.6$ pu operating points), the measured grid frequency remains within 20 mHz of nominal throughout the test, with brief transient deviations coinciding with each reference transition before settling back to $f_{nom} = 50$ Hz. This confirms that the droop-based frequency response remains within a tight band around nominal across the full range of commanded active power, without sustained oscillation or drift.

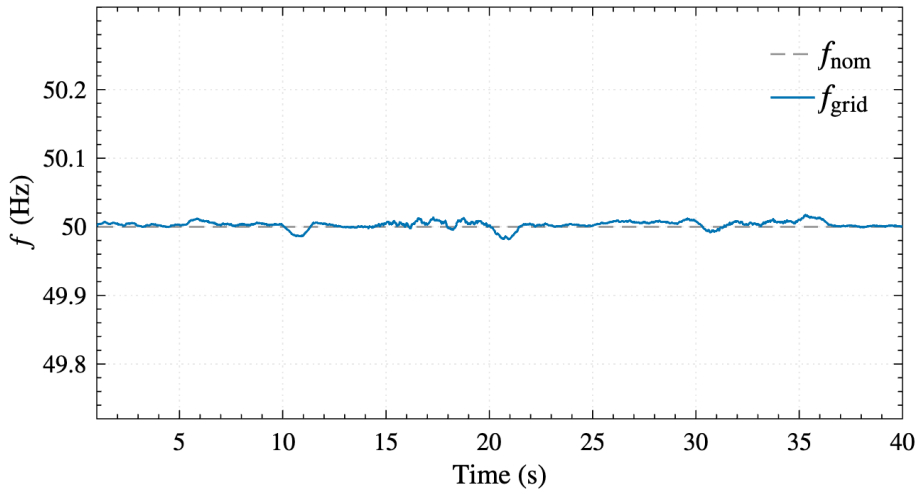


Figure 4.4: Grid frequency, f_{grid}, measured from the voltage at the PCC throughout the four-quadrant test. Despite the large active power reference transitions commanded to the master converter (Table 4.1), the frequency remains within 20 mHz of nominal, $f_{nom} = 50$ Hz, confirming that grid synchronism is preserved across the full P–Q operating envelope.

Figure 4.5 summarizes the seven steady-state operating points of the test on the P–Q plane, directly comparing the commanded reference (Ref) against the corresponding measured point for each quadrant. The close agreement between reference and measured markers across all four quadrants, including the two additional reactive power levels tested within quadrants Q1, Q2 and Q3, confirms that the master–slave converter pair tracks both active and reactive power references accurately and without directional bias, regardless of the sign combination of P and Q. All measured operating points remain within the converter pair's rated apparent power limit ($|S| = 1$ pu), confirming that no operating point commanded during the test exceeds the converter's rated capability. Taken together, Figures 4.2–4.5 validate the correct implementation of the P–f and Q–V droop control laws described in Section 3.3.2, as well as the slave converter's ability to accurately follow the current reference shared by the master, across the full four-quadrant operating envelope.

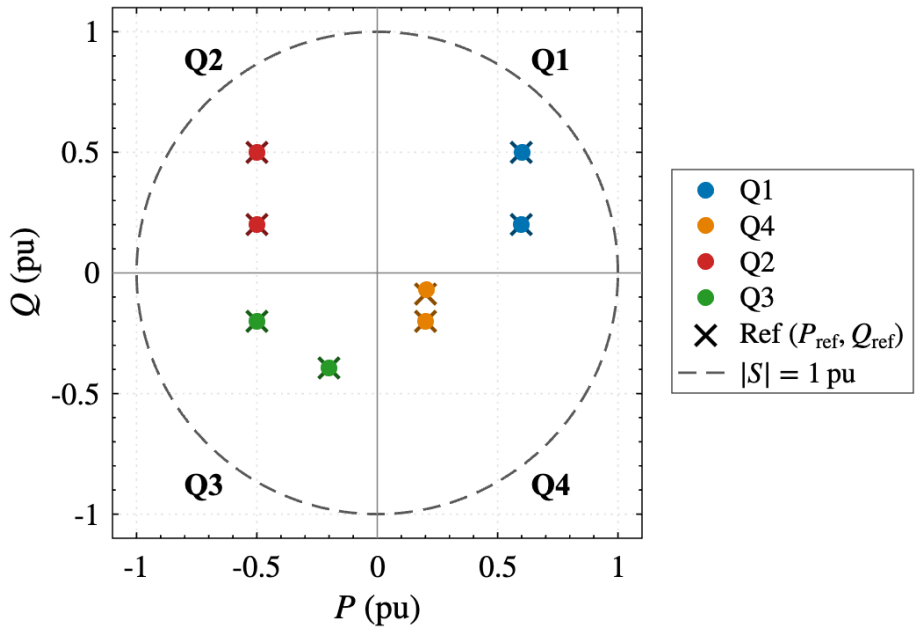


Figure 4.5: Summary of the seven steady-state operating points commanded during the four-quadrant test (Table 4.1), plotted on the P–Q plane and colored by quadrant (Q1–Q4).

4.2 Current-Control Validation of the DC/DC Stage

Having validated the AC/DC master–slave control in isolation (Section 4.1), the DC/DC stage is now validated on its own terms, before the two stages are assembled into the complete system in Section 4.3. This follows the same incremental validation strategy: each subsystem is exercised independently, so that its behavior is understood in isolation before the additional dynamics of the full conversion chain are introduced.

4.2.1 Objective

The objective of this test is to validate the current-control loop of the IBC, whose design is described in Section 3.4.3. Specifically, the test assesses the converter's ability to track an imposed output-current reference, I_h^{dc*}, across its operating range, the dynamic response of the loop to a step change in that reference, and the balanced current sharing among the three interleaved branches.

In the complete system, the current reference is generated internally by the DC bus voltage loop, which drives the IBC to regulate V_t^{dc} by adjusting the power it draws from the bus. Validating that voltage-regulation function requires the bus to be supported by an energy source whose dynamics the IBC acts against, a role played by the AC/DC stage in the full system. It is therefore not reproducible with the IBC in isolation, and is assessed instead in Section 4.3. Accordingly, the present test isolates the inner current loop: the DC bus is held at its nominal value by an ideal voltage source, and the current reference I_h^{dc*} is imposed externally. This mirrors the validation approach adopted for interleaved buck converters supplying PEM electrolyzers in the literature [18], where the current-tracking loop and branch current sharing are the quantities of interest.

4.2.2 Initialization

The simulation begins at $t = 0$ with $I_h^{dc*} = 0$, stepping to the rated stack current at $t = 0.2$ s and subsequently between two operating levels, so that both the initial start-up transient and the tracking across the operating range can be assessed within a single continuous run. In the simulation model, this reference is identified as ihStep, the name reflecting the stepped profile through which it is applied to test the loop's dynamic response. The reference profile is imposed as a sequence of steps rather than ramps, since the purpose here is precisely to characterize the dynamic response of the current loop to abrupt reference changes. The commanded levels correspond to the full stack current, $I_h^{dc*} = 625$ A (100%), and a reduced level of 300 A ($\approx 48\%$), applied in the sequence $0 \rightarrow 625 \rightarrow 300 \rightarrow 625$ A. The full level coincides with the nominal branch current adopted for the IBC sizing in Section 3.4.2 ($I_{stack} = 625$ A, i.e. 208.33 A per branch).

4.2.3 Test Setup

The DC/DC stage is exercised in isolation, decoupled from the AC/DC converters and the shared DC bus. Figure 4.6 shows the overall arrangement: the IBC is supplied on its high-voltage side by an ideal DC voltage source fixed at the nominal bus voltage $V_t^{dc} = 800$ V, in parallel with the DC bus capacitor C_{dc}, and delivers current to the electrolyzer-equivalent load R_{eq} characterized in Section 3.4.1. Voltage and current measurements are taken on both sides of the converter (V_t^{dc}, I_t^{dc} on the bus side; V_h^{dc}, I_h^{dc} on the load side).

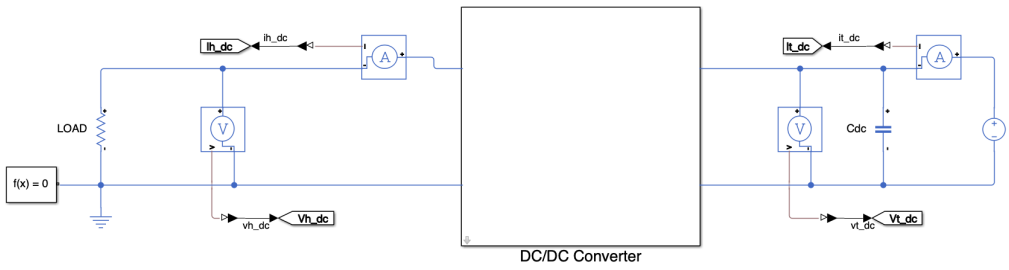


Figure 4.6: Simulation of the isolated DC/DC test.

The power circuit of the converter itself is shown in Figure 4.7. The three interleaved buck branches share the same input and output DC nodes, each with the branch inductance and output capacitance sized in Section 3.4.2 (Table 3.5) and driven by its own gating signal (G_{P1}, G_{P2}, G_{P3}) from the control block. The three branch currents recombine at the output node to form the total current delivered to the load.

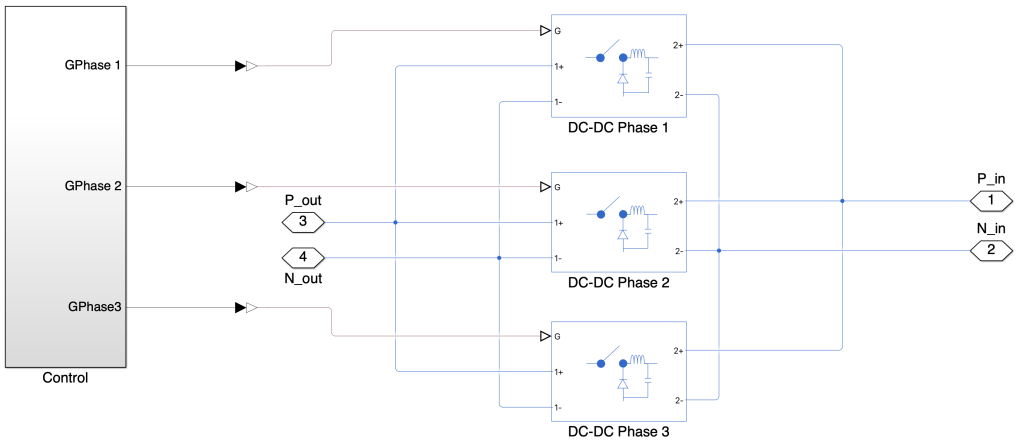


Figure 4.7: Power circuit of the Interleaved Buck Converter, showing the three parallel buck branches (DC-DC Phase 1–3) and their gating signals (G_{P1}–G_{P3}).

The current-control structure is shown in Figure 4.8. The externally imposed reference I_h^{dc*} is divided by the number of branches and compared against each branch's measured inductor current (i_{LP1}, i_{LP2}, i_{LP3}). Each resulting error drives an independent discrete PI controller, whose output feeds the corresponding branch PWM generator. As described in Section 3.4.3, the three PWM carriers are phase-shifted by 120° to achieve the interleaving that reduces the combined output current ripple, and each branch closes its own current loop on its respective inductor current. Since the three branches are identical and share the same reference, their PI controllers converge to the same duty cycle in steady state, which is what produces the balanced sharing of the total current among the branches.

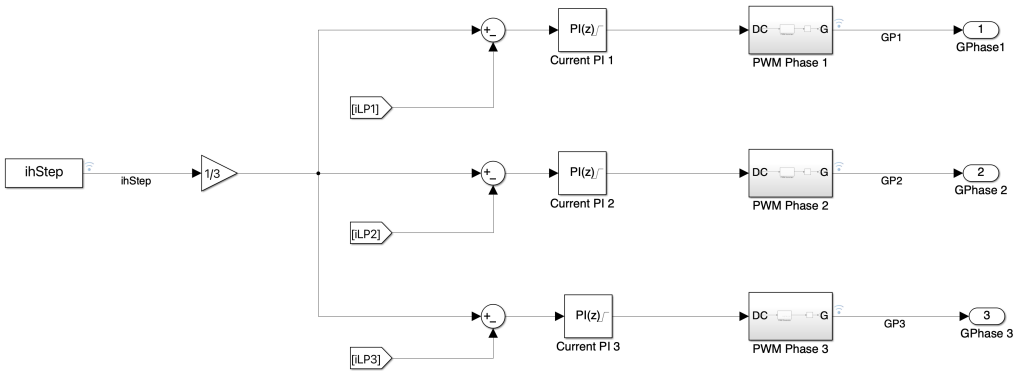


Figure 4.8: Current-control structure of the IBC.

4.2.4 Test Results

Figure 4.9 shows the measured output current, I_h^{dc}, tracking the imposed reference, I_h^{dc*}, throughout the full run. The controller follows each of the commanded levels (625 A and 300 A) with no discernible steady-state error, and reproduces both the $0 \rightarrow 625$ A start-up step and the subsequent transitions between operating levels. This confirms that the current loop tracks its reference accurately across the operating range, consistent with the tracking behavior reported for interleaved buck converters in comparable electrolyzer applications [18].

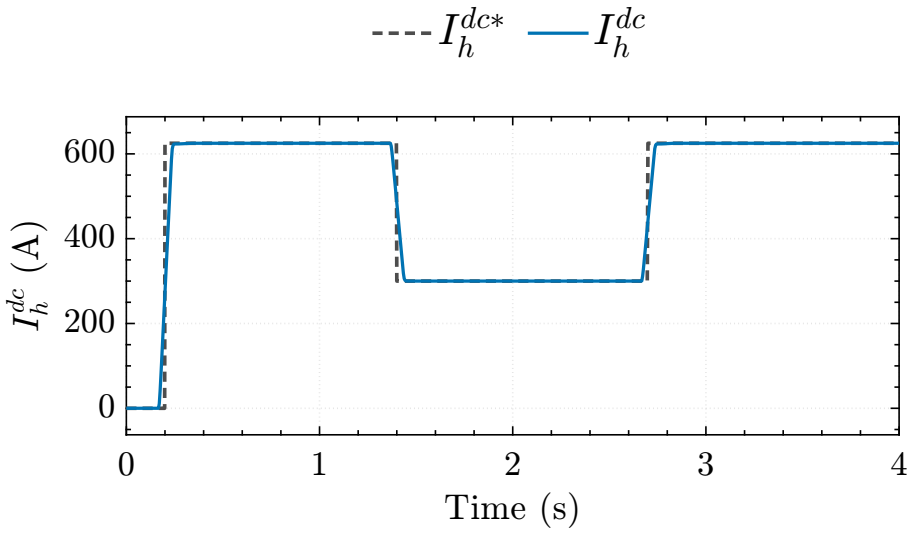


Figure 4.9: Output-current tracking over the full run.

The dynamic response of the loop is examined in Figure 4.10, which shows a detail of the initial $0 \rightarrow 625$ A step. The measured current rises to the commanded level without significant overshoot, settling to the reference shortly after the step is applied. This confirms that the current loop is adequately damped and that its bandwidth is sufficient to follow the imposed reference changes.

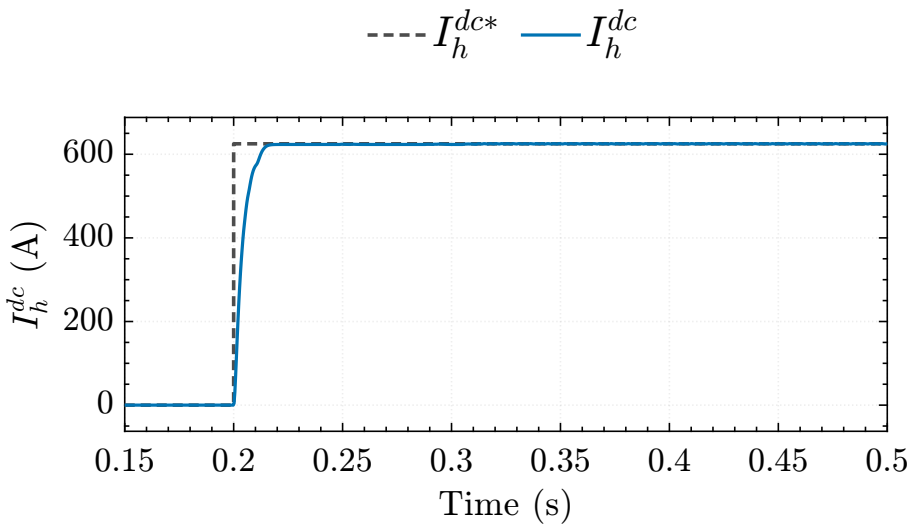


Figure 4.10: Detail of the output-current response to the initial $0 \rightarrow 625$ A reference step.

Finally, Figure 4.11 shows the three interleaved branch currents, i_{LP1}, i_{LP2}, and i_{LP3}, over a short, switching-period-scale window at a steady-state operating point. The three branches carry equal average currents and are mutually phase-shifted by 120°, confirming the balanced current sharing and the interleaving on which the combined-output ripple attenuation depends. The switching ripple delivered to the electrolyzer stack, resulting from the recombination of these three branch currents, was already quantified against the sizing criteria in Section 3.4.2 (Figure 3.10); the present figure instead confirms that the branches remain balanced under active current control, which is the quantity of interest here.

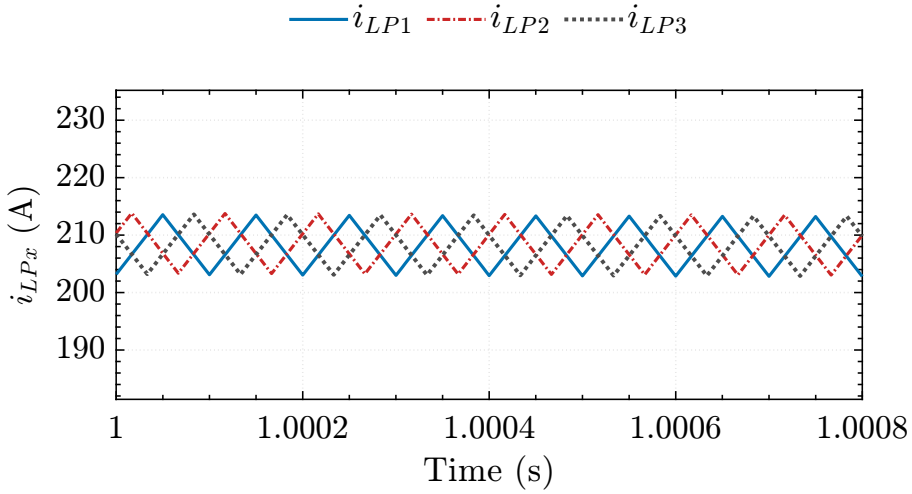


Figure 4.11: The three interleaved branch currents, i_{LP1}, i_{LP2}, and i_{LP3}, over a short, switching-period-scale window at a steady-state operating point.

The preceding results validate the loop against changes in its reference. A complementary test assesses the opposite case, its ability to reject disturbances originating in the load. Here the current reference is held fixed at the full stack current, $I_h^{dc*} = 625$ A, while the load resistance is stepped

by $\pm 20\%$ about its nominal value, with each step applied only once the current has reached steady state. A $+20\%$ increase is applied at $t = 1.4$ s and returned to the nominal load at $t = 2.4$ s; a -20% decrease is then applied at $t = 3.4$ s and held until the end of the run. Because the reference is constant throughout, any transient in the output current can be attributed unambiguously to the load change rather than to a change in the commanded value.

Figure 4.12 shows the output current over the full run. The current remains at its 625 A reference throughout, with only brief transients at the instants where the load changes, confirming that the loop rejects the load disturbances and holds the commanded current. Three load transitions are visible as small deviations from the otherwise flat response: the $+20\%$ step at $t = 1.4$ s, the return to the nominal load at $t = 2.4$ s, and the -20% step at $t = 3.4$ s.

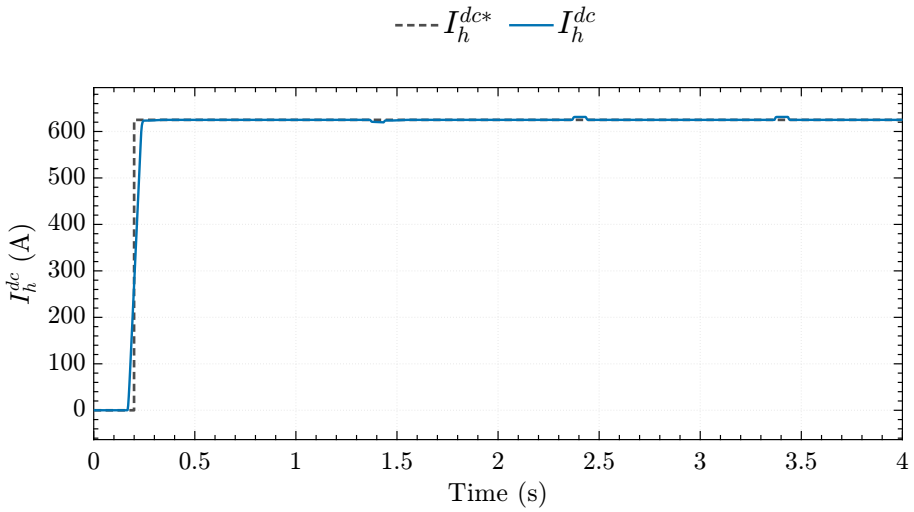
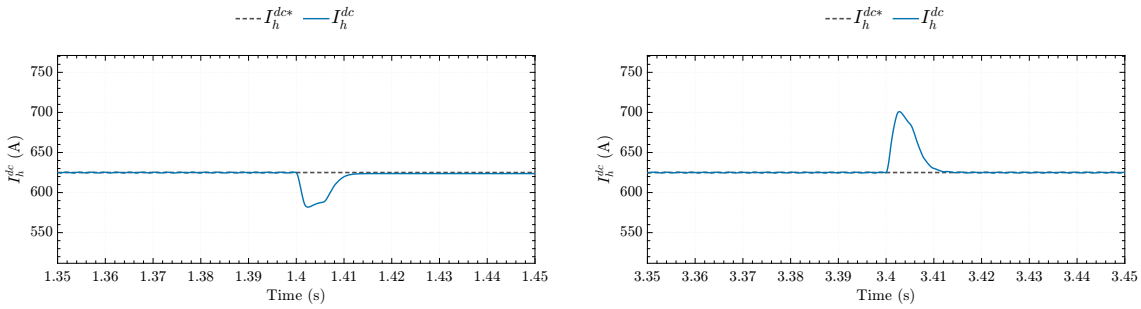


Figure 4.12: Output current under the $\pm 20\%$ load steps, over the full run.

The two disturbance instants are detailed in Figure 4.13. In both cases the current departs briefly from the reference at the instant the load changes and is driven back to 625 A within a few milliseconds, with no steady-state error once the transient has settled. The response is not symmetric between the two steps: the -20% load decrease produces a larger transient excursion than the $+20\%$ increase. This reflects the dependence of the converter's small-signal dynamics on the operating point, so that a fixed-gain PI controller does not respond identically to load increases and decreases of the same relative magnitude. In both cases, however, the loop recovers the reference current cleanly, confirming its robustness to the load variations expected of the electrolyzer.



(a) $+20\%$ load step at $t = 1.4$ s

(b) -20% load step at $t = 3.4$ s

Figure 4.13: Detail of the output-current response to the load steps. (a) corresponds to the $+20\%$ increase and (b) to the -20% decrease.

Taken together, the results of this section validate the IBC current-control loop in isolation: the loop tracks the imposed current reference across its operating range with no steady-state error (Figures 4.9–4.10), maintains balanced current sharing among the three interleaved branches (Figure 4.11), and rejects $\pm 20\%$ load disturbances, recovering the commanded current within a few milliseconds (Figures 4.12 and 4.13). With the current loop thus validated, the complete system, in which the DC bus voltage loop generates this current reference to regulate V_t^{dc}, is assembled and evaluated in Section 4.3.

4.3 Full System Operation

With the AC/DC master–slave control validated in isolation, the complete converter chain, comprising the master–slave AC/DC stage, shared DC bus, Interleaved Buck Converter, and electrolyzer-equivalent load, is now assembled and evaluated as a whole. Three operating scenarios are considered: normal steady-state operation, a grid voltage fault, and a grid frequency event, each assessing a different aspect of the system's Grid-Forming behavior.

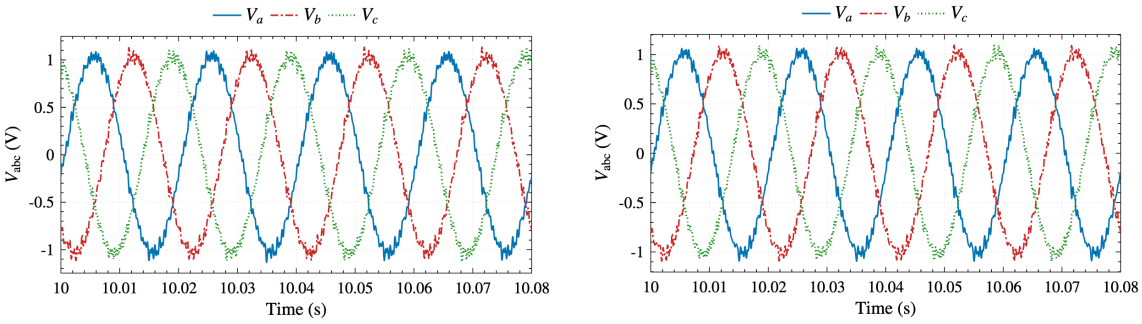
4.3.1 Normal Operation

As established in Section 3.4, the DC bus voltage is intended to stabilize at 800 V and, under normal operation, produce a voltage close to 400 V at the terminals of the electrolyzer-equivalent load. This subsection aims to show that this idealized operation is achieved. To this end, a value of $P_{ref,script} = 0.5$ pu was set. The results correspond to the steady-state condition reached under this constant reference. The AC waveforms are shown over a few cycles, sufficient to illustrate their behavior. The remaining figures are shown from $t = 3$ s onward, by which point the system has already reached steady state.

4.3.1.1 AC-Side Results

Figures 4.14a–4.14b show the three-phase voltage waveforms at the AC terminals of the master and slave converters, respectively, each expressed in per unit of its own voltage base ($\hat{V}_b^Y$ and $\hat{V}_b^\Delta$,

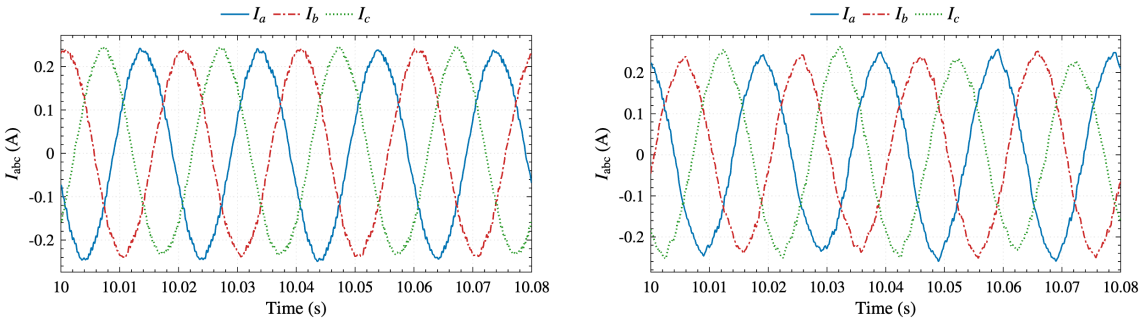
Table 3.1) due to their differing winding configuration.



(a) Voltage v^{Y}_{abc} (b) Voltage v^{Δ}_{abc}

Figure 4.14: Three-phase terminal voltages of the converters under the constant reference $P_{ref,script} = 0.5$ pu. (a) corresponds to the master (Star) and (b) is related to the slave (Delta).

Figures 4.15a–4.15b show the corresponding three-phase currents, expressed in per unit of the respective current base of each converter, $\hat{I}^{Y}_{b}$ and $\hat{I}^{\Delta}_{b}$ (Table 3.1).



(a) Current i^{Y}_{abc} (b) Current i^{Δ}_{abc}

Figure 4.15: Three-phase terminal currents of the converters under the constant reference $P_{ref,script} = 0.5$ pu. (a) corresponds to the master (Star) and (b) is related to the slave (Delta).

Figure 4.16 shows the modulation index of the master converter. The peak value of approximately 0.96 confirms that the converter operates within the linear modulation region, without overmodulation, and makes efficient use of the available DC bus voltage.

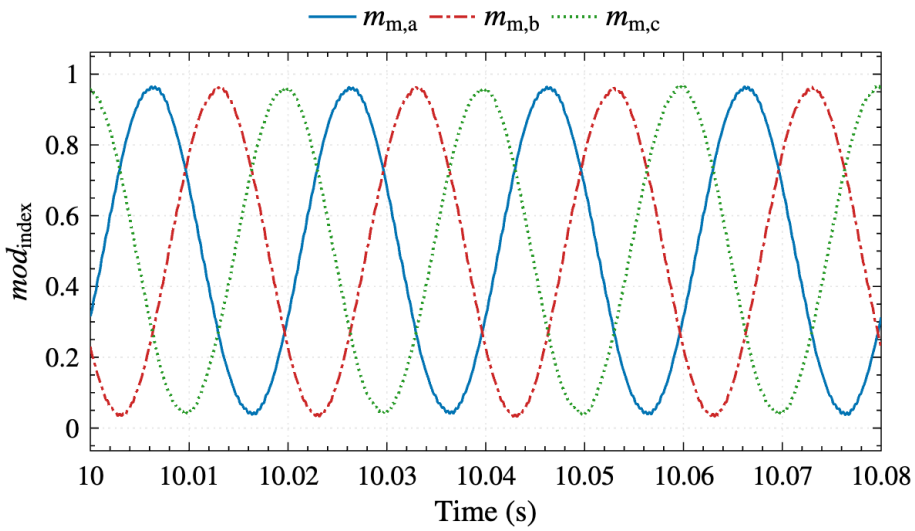


Figure 4.16: Modulation index of the master converter.

Figure 4.17 confirms that the combined active power delivered by the master and slave converters, $P_{meas,total}$, tracks the scripted reference $P_{ref,script} = 0.5$ pu with no discernible steady-state error.

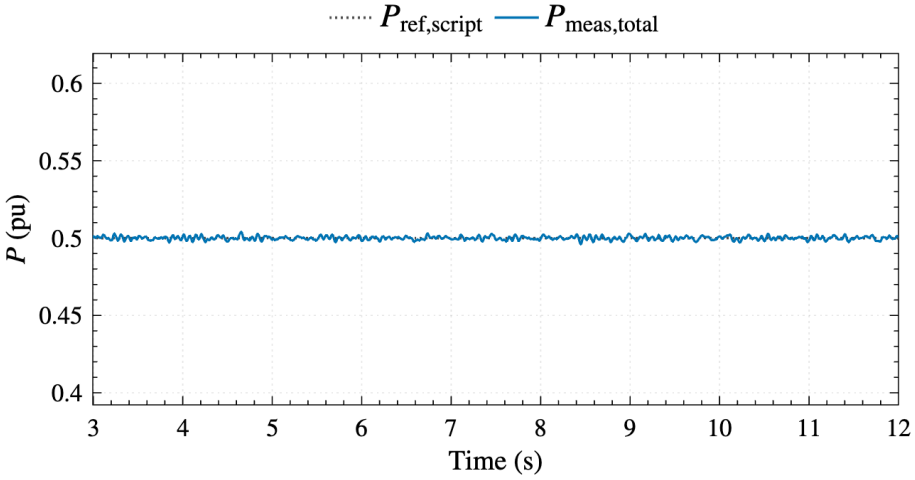
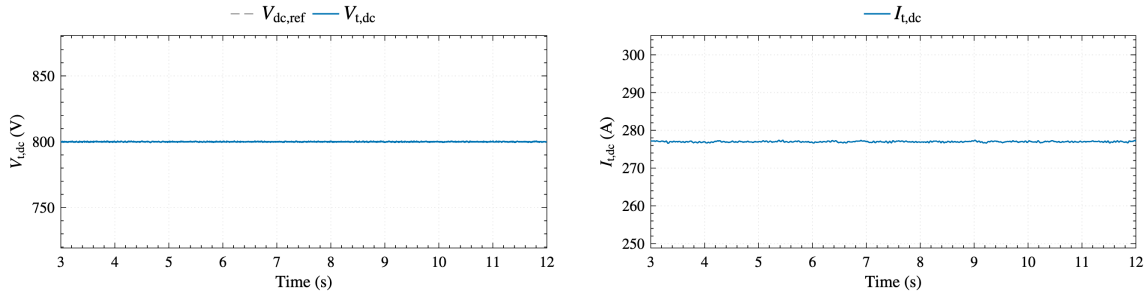


Figure 4.17: Combined active power delivered by the master and slave converters, $P_{meas,total}$, tracking the scripted reference $P_{ref,script} = 0.5$ pu, with no discernible steady-state error.

4.3.1.2 DC-Side Results

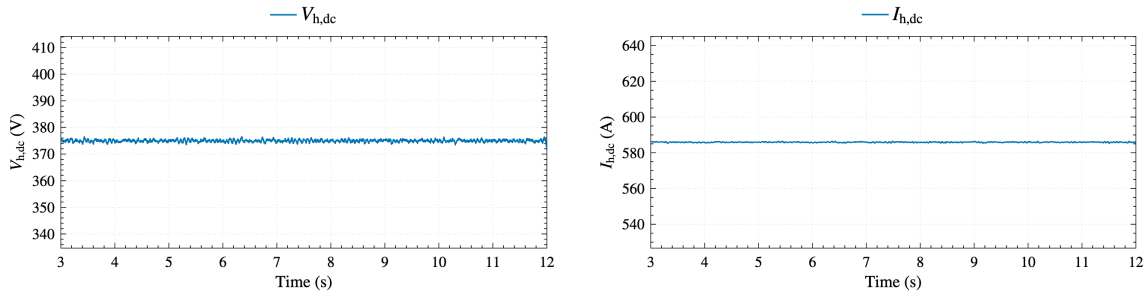
Figure 4.18 shows the DC bus voltage and current, V_t^{dc} and I_t^{dc}, at the input of the Interleaved Buck Converter. V_t^{dc} settles tightly at its 800 V reference, confirming correct regulation of the DC bus.



(a) V_t^{dc} (b) I_t^{dc}

Figure 4.18: DC measurements at the DC bus, which corresponds to the input of the IBC. (a) represents the voltage and (b) represents the current.

Figure 4.19 shows the corresponding voltage and current at the terminals of the electrolyzer-equivalent load, V_h^{dc} and I_h^{dc}.



(a) V_h^{dc} (b) I_h^{dc}

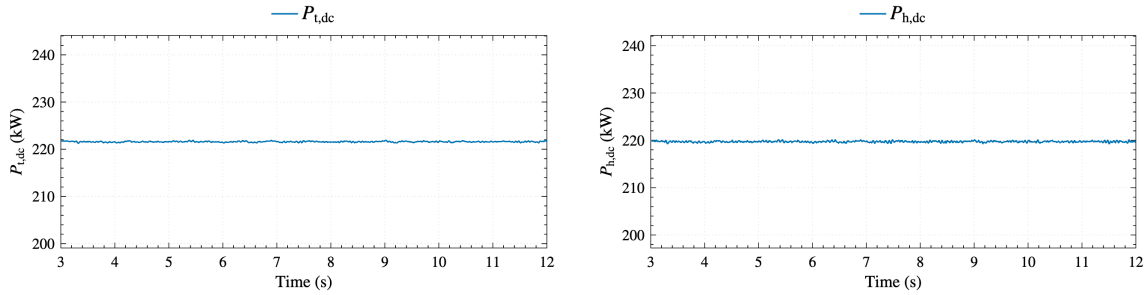
Figure 4.19: Voltage (a) and current (b) at the terminals of the electrolyzer-equivalent load. V_h^{dc} settles close to the intended 400 V design value.

From the steady-state values of V_h^{dc} and I_h^{dc}, the equivalent resistance presented by the electrolyzer-side load can be computed as

$$R_{eq} = \frac{V_h^{dc}}{I_h^{dc}} \approx 0.640\,\Omega. \tag{4.1}$$

This value serves as a reference operating point for the equivalent-resistance check performed under the disturbance scenarios examined in Sections 4.3.2 and 4.3.3.

Figure 4.20 shows the power at the DC bus, P_t^{dc}, and at the electrolyzer-equivalent load, P_h^{dc}, computed as $P_t^{dc} = V_t^{dc} \cdot I_t^{dc}$ and $P_h^{dc} = V_h^{dc} \cdot I_h^{dc}$.



(a) P_t^{dc} (DC bus) (b) P_h^{dc} (electrolyzer)

Figure 4.20: (a) Power at the DC bus, $P_t^{dc} = V_t^{dc} \cdot I_t^{dc}$, and (b) at the electrolyzer-equivalent load, $P_h^{dc} = V_h^{dc} \cdot I_h^{dc}$.

4.3.1.3 Power Balance

The overall power balance across the AC/DC and DC/DC stages is summarized in Table 4.2. Since the converter models were not parameterized for loss estimation and the assessment of conversion efficiency lies outside the objectives of this work, these values are presented for completeness only and are not used to draw conclusions about the conversion chain. The AC-side active power, $P_{AC} = P_{meas,total} \times S_b \approx 250$ kW, is reduced to $P_t^{dc} \approx 221.6$ kW at the DC bus, corresponding to an AC/DC conversion efficiency of $\eta_{AC/DC} \approx 88.6\%$. The DC/DC stage further converts P_t^{dc} to $P_h^{dc} \approx 220$ kW, corresponding to $\eta_{DC/DC} \approx 99.3\%$. The overall AC-to-electrolyzer efficiency is therefore $\eta_{global} = \eta_{AC/DC} \times \eta_{DC/DC} \approx 88\%$.

Table 4.2: Power balance across the AC/DC and DC/DC conversion stages under normal operation.

Stage	Power	Efficiency
AC (total)	≈ 250 kW	–
DC bus (P_t^{dc})	≈ 221.6 kW	$\eta_{AC/DC} \approx 88.6\%$
Electrolyzer (P_h^{dc})	≈ 220 kW	$\eta_{DC/DC} \approx 99.3\%$
Global (AC→electrolyzer)	–	$\approx 88\%$

4.3.2 Voltage Fault

A grid voltage step from $V_{nom} = 1$ pu to 0.8 pu (a 20% sag) is applied at $t = 5$ s. Figure 4.21 confirms the applied disturbance, imposed as an instantaneous step rather than a ramped transition.

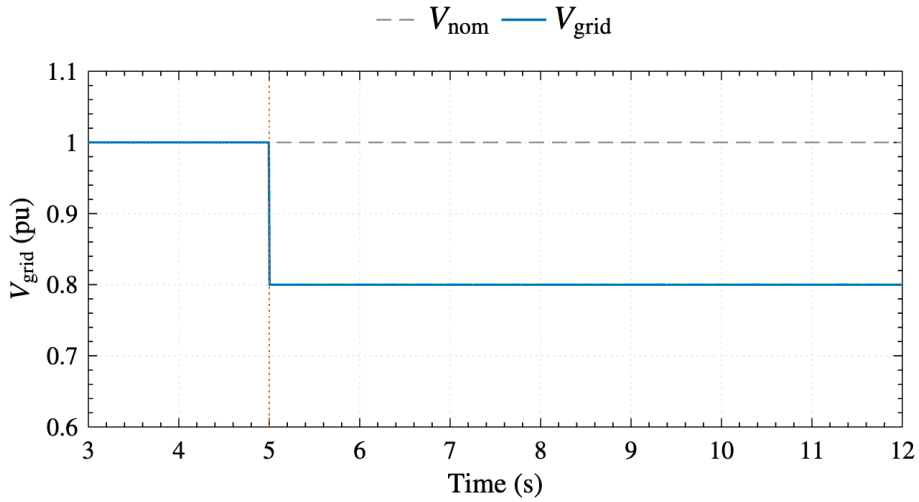


Figure 4.21: Voltage fault simulated.

The steady-state voltage reference generated by the Q–V droop loop can be predicted analytically from Equation 3.11, using the measured $Q_{meas,total}$ as input. With $Q_{ref} = 0$ pu, $n_q = 0.3$ pu, and $Q_{meas,total}$ approximately 0.2 pu measured post-fault (Figure 4.23), this predicts $V_d^* \approx 0.94$ pu, compared to the measured steady-state value of $V_d^* \approx 0.94$ pu (Figure 4.22), which corresponds to the expected result. This close agreement confirms the correct implementation of the Q–V droop control.

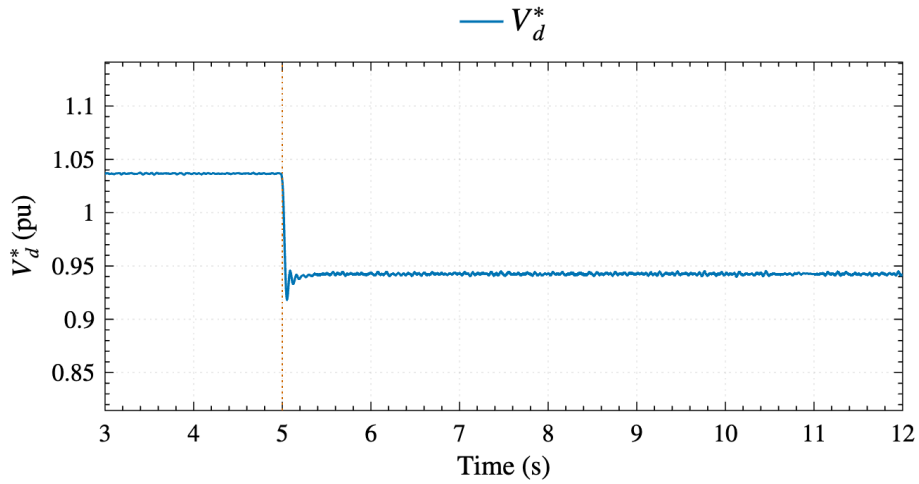


Figure 4.22: Measured voltage reference, V_d^*, after the voltage fault.

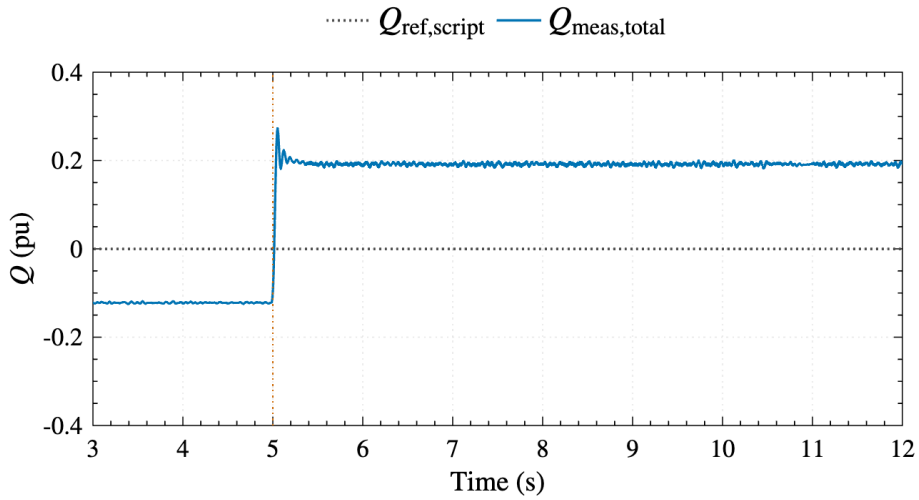


Figure 4.23: Measured value of total reactive power after the voltage fault.

Figure 4.23 also shows a change in the sign of $Q_{meas,total}$ at the instant of the fault. Following the voltage sag, the grid-forming converter, which imposes its own voltage at its terminals, is left with a terminal voltage above that of the grid and therefore injects reactive power, raising $Q_{meas,total}$ to approximately 0.2 pu. This change of sign corresponds to the expected voltage-support behavior of the converter, to which the Q–V droop responds by lowering the voltage reference to $V_d^* \approx 0.94$ pu, as predicted above. The lower-than-nominal $Q_{meas,total}$ observed relative to a naive prediction based solely on ΔV_{grid} is attributable to the voltage drop across the coupling impedance under load.

It should be noted, however, that before the fault $Q_{meas,total}$ settles at approximately -0.12 pu despite $Q_{ref} = 0$ pu. This offset was not present in the four-quadrant validation of Section 4.1, in which the AC/DC stage was supplied by an ideal DC source, and appeared only once the DC/DC stage was integrated. This indicates that, when loaded by the DC/DC converter, the AFE controller no longer regulates the reactive power with the same accuracy, a limitation of the developed control system that is further discussed in Section 5.2.

In contrast to $Q_{meas,total}$, the total active power reference is unaffected by this disturbance, since the P–f droop loop only responds to frequency deviations, which are absent in this test. Figure 4.24 confirms this: following a brief transient at $t = 5$ s, $P_{meas,total}$ recovers to approximately its pre-fault value of ≈ 0.5 pu (≈ 250 kW).

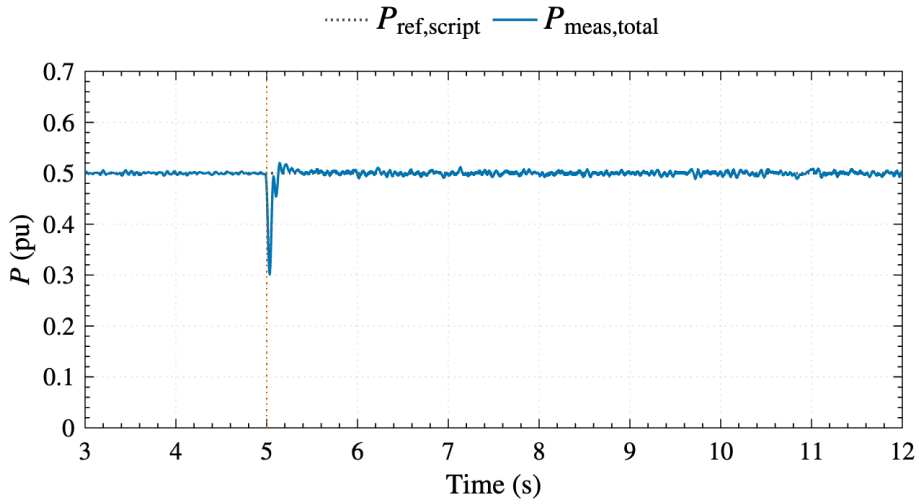
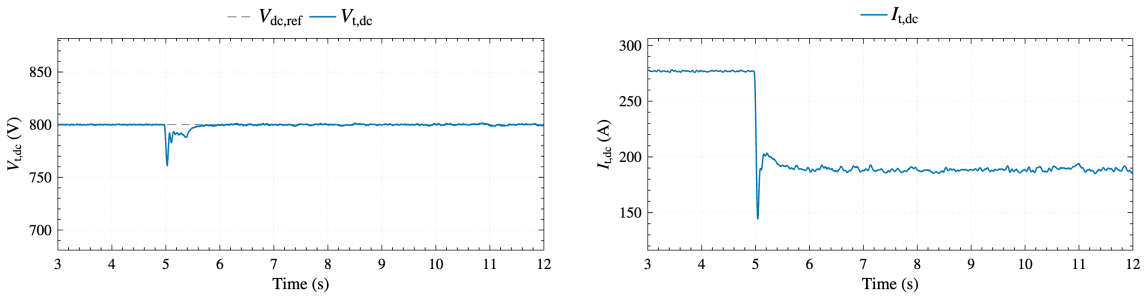


Figure 4.24: Measured value of total active power after the voltage fault.

The corresponding DC-side response is presented in Figures 4.25–4.27, spanning the DC bus (V_t^{dc}, I_t^{dc}, P_t^{dc}) and the electrolyzer-equivalent load (V_h^{dc}, I_h^{dc}, P_h^{dc}). Figure 4.25 shows the DC bus voltage and current. At the instant of the voltage step ($t = 5$ s), both quantities exhibit a sharp transient, consistent with the abrupt change in AC-side power delivery. Following this transient, V_t^{dc} remains regulated at its 800 V reference, while I_t^{dc} settles at approximately 190 A, down from approximately 275 A pre-fault.



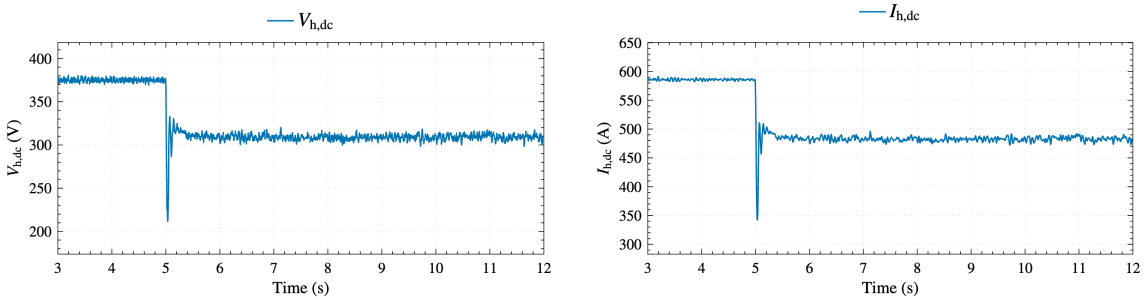
(a) V_t^{dc} (b) I_t^{dc}

Figure 4.25: (a) DC bus voltage, V_t^{dc}, against its reference $V_{dc,ref}$, and (b) DC bus current, I_t^{dc}, at the input of the Interleaved Buck Converter, under the simulated voltage fault.

Figure 4.26 shows the corresponding voltage and current at the electrolyzer-equivalent load. Both quantities settle to new steady-state values following the same transient: V_h^{dc} near 310 V, down from approximately 375 V pre-fault, and I_h^{dc} near 485 A, down from approximately 585 A. This new load operating point provides a further independent check of the equivalent load resistance already established in Section 4.3.1: evaluating

$$R_{eq} = \frac{V_h^{dc}}{I_h^{dc}}, \tag{4.2}$$

gives approximately 0.639 Ω post-fault, consistent with the ≈ 0.64 Ω established under normal operation.

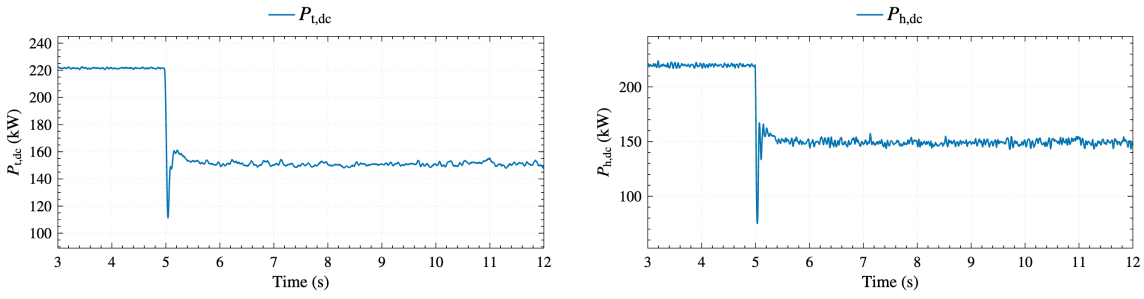


(a) V_h^{dc} (b) I_h^{dc}

Figure 4.26: (a) Voltage, V_h^{dc}, and (b) current, I_h^{dc}, at the terminals of the electrolyzer-equivalent load, under the simulated voltage fault.

Finally, Figure 4.27 shows the power at the DC bus and at the electrolyzer-equivalent load, falling from approximately 220 to approximately 150 kW, for both, after the fault, consistent with the reduced voltage and current at the load terminals shown in Figure 4.26. However, $P_{meas,total}$ recovers to approximately its pre-fault value of ≈ 0.5 pu (≈ 250 kW) (Figure 4.24). Since the DC bus voltage remains regulated, the AC-side active power and the power delivered to the DC bus should remain consistent with the relation observed under normal operation (Table 4.2). The difference between them indicates that this power is either being dissipated somewhere in the model or that an inconsistency exists in the complete model. Identifying its origin proved to be one of the main difficulties encountered in this work.

This difficulty is closely related to how the control system was developed. The AC/DC and DC/DC controllers were designed and tuned separately, each validated in isolation (Sections 4.1 and 4.2), and no integrated controller for the complete conversion chain was developed. The discrepancies observed under the voltage fault therefore reflect a limitation of the developed control system when both stages are integrated, and show that the operation of the complete chain requires further study.



(a) P_t^{dc} (DC bus) (b) P_h^{dc} (electrolyzer)

Figure 4.27: (a) Power at the DC bus, $P_t^{dc} = V_t^{dc} \cdot I_t^{dc}$, and (b) at the electrolyzer-equivalent load, $P_h^{dc} = V_h^{dc} \cdot I_h^{dc}$.

Taken together, Figures 4.25–4.27 show that the DC bus voltage control loop absorbs the transient without loss of regulation and that the resistive load characteristic remains consistent at a different power level, while the reactive power offset and the active power discrepancy identified above reveal the limitations of the developed control system when the two conversion stages operate together.

4.3.3 Frequency Event

A grid frequency step from $f_{nom} = 50$ Hz to 49.8 Hz is applied at $t = 8$ s. Figure 4.28 confirms the applied disturbance, showing a smooth transition with no overshoot, consistent with the first-order dynamics of the droop low-pass filter.

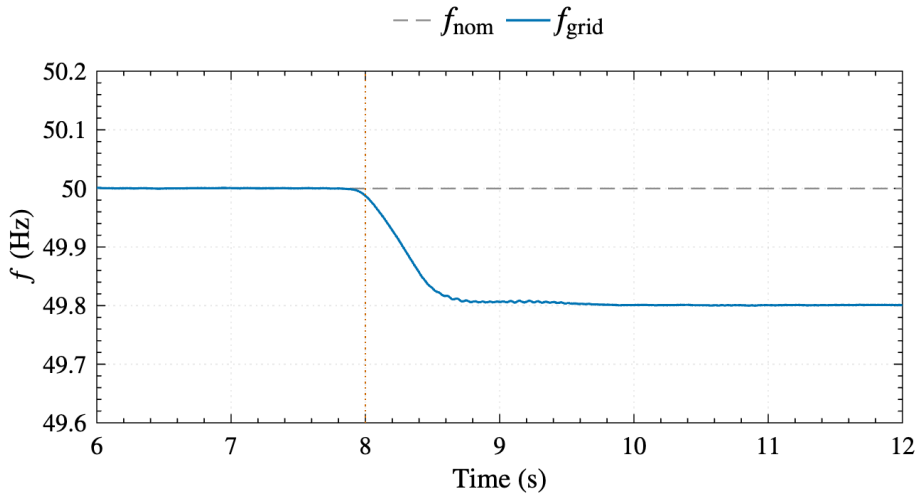


Figure 4.28: Frequency event simulated.

The steady-state active power response can be predicted analytically from the P–f droop law (Equation 3.9). Accounting for the sign convention adopted for plotting, the steady-state relationship reduces to

$$P_{meas,total} = P_{ref} + \frac{\Delta f^{pu}}{m_p}, \tag{4.3}$$

where $\Delta f^{pu} = (f_{grid} - f_{nom})/f_{nom}$. For this event ($\Delta f^{pu} = -0.2/50 = -0.004$, $m_p = 0.015$ pu), this predicts $P_{meas,total} \approx 0.233$ pu, compared to the measured steady-state value of $P_{meas,total} \approx 0.235$ pu (Figure 4.29), a difference of approximately 0.9%. This close agreement confirms the correct implementation of the P–f droop control.

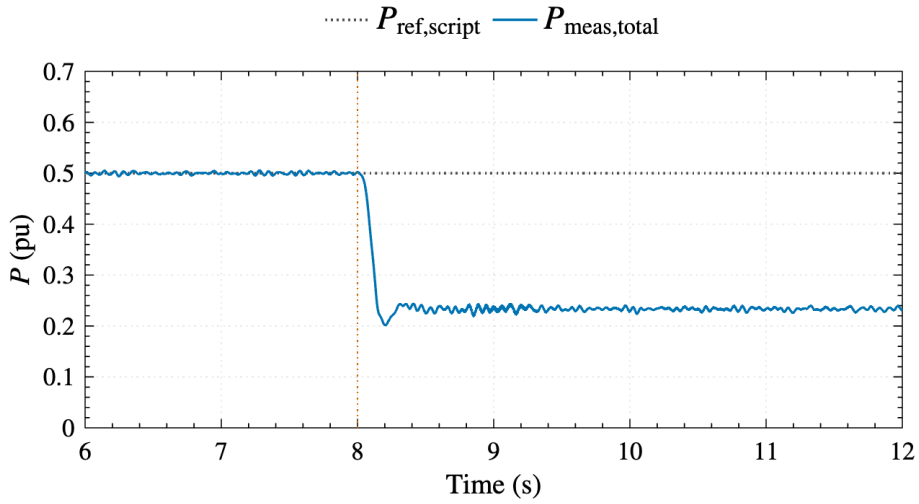
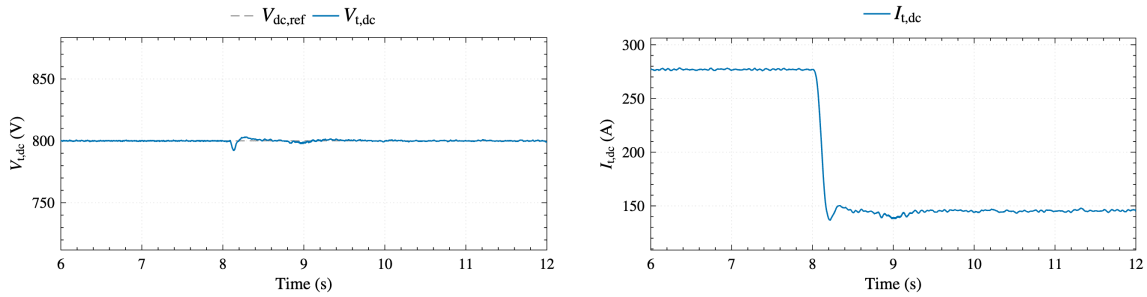


Figure 4.29: Measured value of total active power after the frequency event.

The corresponding DC-side response is presented in Figures 4.30–4.32, spanning the DC bus (V_t^{dc}, I_t^{dc}, P_t^{dc}) and the electrolyzer-equivalent load (V_h^{dc}, I_h^{dc}, P_h^{dc}). Figure 4.30 shows the DC bus voltage and current. At the instant of the frequency step ($t = 8$ s), both quantities exhibit a sharp transient, consistent with the abrupt reduction in AC-side active power shown in Figure 4.29. Following this transient, V_t^{dc} remains regulated at its 800 V reference, while I_t^{dc} settles at approximately 146 A, down from approximately 277 A pre-event, a reduction consistent with the lower active power now being delivered from the AC side.



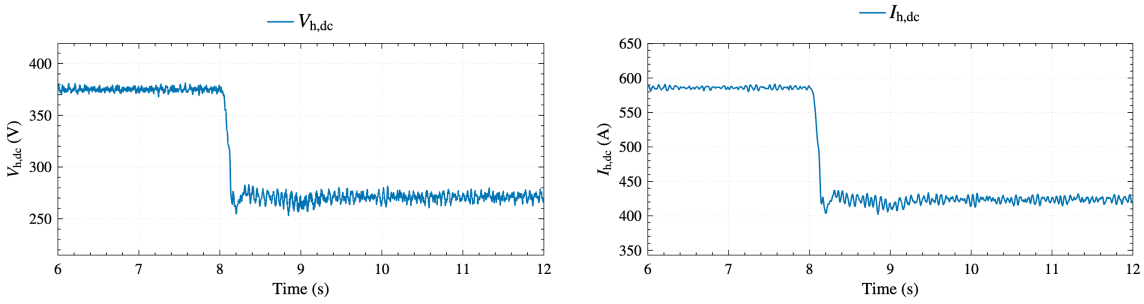
(a) V_t^{dc} (b) I_t^{dc}

Figure 4.30: (a) DC bus voltage, V_t^{dc}, against its reference $V_{dc,ref}$, and (b) DC bus current, I_t^{dc}, at the input of the Interleaved Buck Converter, under the simulated frequency event.

Figure 4.31 shows the corresponding voltage and current at the electrolyzer-equivalent load. Both quantities settle to new steady-state values following the same transient: V_h^{dc} near 271 V, down from approximately 375 V pre-event, and I_h^{dc} near 424 A, down from approximately 586 A. This new load operating point, at roughly half the power delivered under normal operation, provides a further independent check of the equivalent load resistance already established in Section 4.3.1: evaluating

$$R_{eq} = \frac{V_h^{dc}}{I_h^{dc}}, \tag{4.4}$$

gives approximately 0.640 Ω pre-event and 0.639 Ω post-event, a difference of under 0.15 % despite the delivered power differing by nearly a factor of two (≈ 220 kW versus ≈ 115 kW). This confirms that the electrolyzer-equivalent load behaves as a constant resistance across a wide range of operating points, not merely at the single power level examined under normal operation.



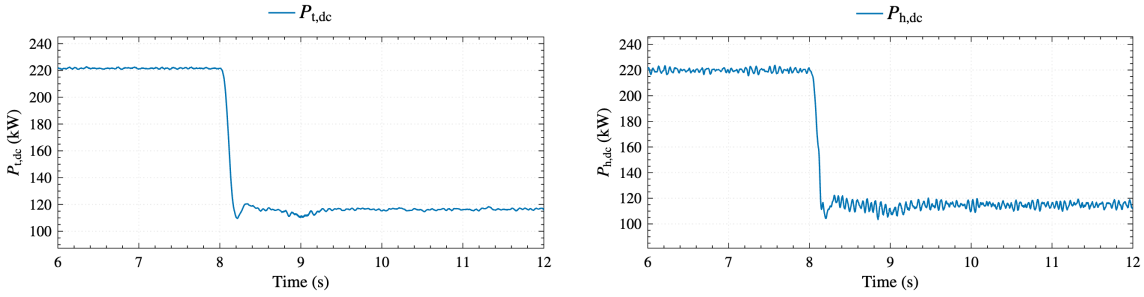
(a) V_h^{dc} (b) I_h^{dc}

Figure 4.31: (a) Voltage, V_h^{dc}, and (b) current, I_h^{dc}, at the terminals of the electrolyzer-equivalent load, under the simulated frequency event.

Finally, Figure 4.32 shows the power at the DC bus and at the electrolyzer-equivalent load, falling from approximately 221 kW and 220 kW, respectively, to approximately 117 kW and 115 kW after the event. The corresponding DC/DC conversion efficiency,

$$\eta_{DC/DC} = \frac{P_h^{dc}}{P_t^{dc}}, \tag{4.5}$$

evaluates to approximately 98.4 % post-event, closely consistent with the ≈ 99 % obtained under normal operation, with the same reservation regarding the efficiency values stated in Section 4.3.1.



(a) P_t^{dc} (DC bus) (b) P_h^{dc} (electrolyzer)

Figure 4.32: (a) Power at the DC bus, $P_t^{dc} = V_t^{dc} \cdot I_t^{dc}$, and (b) at the electrolyzer-equivalent load, $P_h^{dc} = V_h^{dc} \cdot I_h^{dc}$.

Taken together, Figures 4.30–4.32 show that the DC bus and electrolyzer-equivalent load respond to an AC-side frequency disturbance in a coordinated, stable manner: the DC bus voltage

control loop absorbs the transient without loss of regulation, and the resistive load characteristic remains consistent with the values established under normal operation.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

This dissertation set out to study, through simulation, the behavior of a grid-forming controlled electrolyzer capable of supporting the grid via droop-based active and reactive power control. The specific objectives defined in Section 1.4 are addressed as follows.

The review carried out in Chapter 2 established the technological choices on which the remainder of the work was built. PEM electrolysis was identified as the most suitable technology for grid-support applications, owing to its faster and more flexible dynamic response when compared with alkaline electrolysis. On the power electronics side, a two-stage conversion structure, composed of an AFE rectifier followed by an Interleaved Buck Converter, was adopted as a balanced compromise between controllability, power quality and modeling complexity. Among the grid-forming control strategies reviewed, filtered droop control was selected over the Virtual Synchronous Machine, since the low-pass filter on the power measurement reintroduces an inertia-like behavior while keeping a simpler structure with fewer parameters to tune. Virtual Impedance was chosen as the current-limiting method, favoring a smooth post-fault recovery over the harder clamping of current saturation algorithms.

Chapter 3 translated these choices into a complete simulation model. The grid feeds a three-winding Yd1 transformer whose Star and Delta secondaries supply two Grid-Forming AC/DC converters operating in a master–slave configuration: only the master executes the droop, Virtual Impedance and cascaded voltage–current control, while the slave follows the current reference generated by the master. The passive components of both converters were sized from established ripple and reactive power criteria, and the DC/DC stage, an Interleaved Buck Converter with three branches, was sized for the nominal operating point of the electrolyzer-equivalent load, with its control structured as an outer DC bus voltage loop, a power feedforward term and three inner current loops with phase-shifted carriers.

The results presented in Chapter 4 followed an incremental validation strategy. The four-quadrant test against an ideal DC source (Section 4.1.4) confirmed that the master–slave pair correctly tracks active and reactive power references across the converter's full operating envelope,

with the grid frequency kept within a narrow band around its nominal value. The isolated test of the DC/DC stage (Section 4.2.4) showed that the current loop of the Interleaved Buck Converter tracks its reference without steady-state error, maintains a balanced current sharing among the three branches, and rejects load disturbances within a few milliseconds. Finally, the complete system was evaluated under normal operation, a grid voltage fault and a grid frequency event (Section 4.3). In all three scenarios, the DC bus voltage remained regulated at its reference and the electrolyzer-equivalent load kept a consistent equivalent resistance across different power levels.

The droop-based controller was validated quantitatively, not only qualitatively. Under the voltage fault and the frequency event (Sections 4.3.2–4.3.3), analytical predictions derived directly from the Q–V and P–f droop laws (Equations 3.11 and 3.9) were compared against measured simulation results, with agreement within approximately 1% in both cases. This confirms the correct implementation of both droop loops, and not merely their qualitative presence.

Beyond these results, the development of this work exposed several practical complexities, which also constituted its main learning outcomes. The first concerned the per-unit representation of the two converters. Since the Star and Delta windings see different phase voltages, a single set of base values could not be used for both, and two distinct sets of peak per-unit bases had to be defined. Measurements were therefore converted to per unit separately for each converter, while the total active and reactive powers fed to the droop loops were summed in SI units and only then converted using the common base power. Identifying this requirement was essential to obtain a consistent operation of the two converters.

The second complexity was the master–slave coordination itself. Making two parallel converters behave as a single grid-forming unit required a single droop loop acting on the combined measured power, the sharing of the current references generated by the master, and a reference frame consistent between both converters. The phase shift introduced by the Yd1 transformer was compensated through a static angle offset, rather than a local Phase-Locked Loop at the slave, which ensured accurate current tracking without circulating currents between the transformer windings.

The third complexity was the integration of several subsystems that are individually stable into a complete system that remains stable as a whole. Each control loop, from the droop and Virtual Impedance stages to the AC voltage and current loops and the DC bus voltage and current loops of the Interleaved Buck Converter, interacts with the others through the shared DC bus and the coupling to the grid. This motivated the incremental validation strategy adopted in Chapter 4, in which each stage was validated in isolation before being assembled, as well as the separation of bandwidths between inner and outer loops. This process highlighted that the stability of the complete conversion chain cannot be inferred from the stability of its individual parts, and must be verified at each step of the integration.

Taken together, these results confirm the correct operation of the droop-based control of the AC/DC stage and of the current control of the Interleaved Buck Converter, each validated in isolation, under the electrolyzer-equivalent load representation adopted in this work. When both stages were integrated, the system remained stable and responded to grid disturbances in accordance with the droop laws, but a reactive power offset under zero reference and an inconsistency between the

AC-side active power and the power delivered to the DC bus under the voltage fault were also identified. Since the controllers of each stage were developed and tuned separately, these results show that the integration of the two conversion stages requires a deeper study, namely of a control system designed for the complete conversion chain. These limitations, along with other directions for further development, are addressed in Section 5.2.

5.2 Future Work

Although the objectives defined for this dissertation were fulfilled, several aspects of the proposed GFM electrolyzer could be further explored. Some directions are identified as particularly relevant continuations of the work developed in this dissertation:

- **Integrated control of the complete conversion chain.** The AC/DC and DC/DC controllers developed in this work were designed and tuned separately, and validated in isolation. When both stages were integrated, a reactive power offset under zero reference and an inconsistency between the AC-side active power and the power delivered to the DC bus under the voltage fault were observed (Section 4.3.2). A natural continuation of this work would be to identify the origin of these discrepancies, verifying whether the missing power is dissipated within the model or results from an inconsistency in the complete model, and to develop a control system designed for the complete conversion chain, accounting for the interaction between the AC/DC stage, the shared DC bus and the DC/DC stage.

- **Replacing the electrolyzer-equivalent load with the complete electrolyzer electrical model.** As discussed in Section 3.4.1, the electrolyzer was represented throughout this work by an equivalent resistive load, since the primary objective of the dissertation was to validate the proposed control strategy and the interaction between the electrical subsystems, rather than the electrochemical behavior of the stack itself. Replacing this simplified load with the dynamic EEC presented in Chapter 2, including the non-linear V–I characteristic and the double-layer capacitance effect, would allow the interaction between the DC/DC stage's cascaded control (namely its disturbance feedforward term) and the electrolyzer's own non-linear dynamics to be assessed. This is particularly relevant given that, as noted in Chapter 2, the electrolyzer does not behave as a purely resistive load during the fast power transients associated with grid-forming operation. This replacement would therefore provide a more realistic evaluation of the ripple delivered to the stack, of the DC/DC controller's disturbance-rejection performance under a genuinely non-linear load, and of the resulting implications for membrane degradation and stack lifetime.

- **Hardware-in-the-Loop (HIL) validation.** As stated in Section 1.4, this dissertation was intentionally limited to simulation, avoiding the cost, complexity, and safety constraints associated with experimental testing at this stage. A natural continuation of this work would be to validate the proposed control architecture through a Hardware-in-the-Loop setup, in

which the control algorithms are executed on dedicated real-time hardware while interacting with the simulated power system. This would allow the robustness and efficiency of the master–slave coordination to be assessed under realistic control execution and communication constraints, rather than the idealized, delay-free reference sharing assumed in the current model. In addition to the controller execution latency captured by running the control on real-time hardware, the same setup could be further extended to include physical sensors and analog-to-digital acquisition stages in the feedback path, exposing practical implementation aspects, such as sensor noise and analog-to-digital conversion effects, that a purely offline simulation cannot fully capture, thereby providing a more rigorous assessment of the control strategy's readiness for an eventual physical implementation.

- **LVRT validation against grid-code voltage-time curves and unbalanced faults.** The voltage fault examined in Chapter 4 was deliberately set at a moderate, 20% sag, analogous to the moderate frequency deviation used in the frequency event test, so that the underlying Q–V droop law could be validated cleanly, without the Virtual Impedance current-limiting mechanism (Section 3.3.3) or other saturation effects confounding the analytical comparison. A rigorous LVRT assessment, in the sense required by grid codes [16], [23], would instead require testing against the deeper, shorter-duration sags specified by the applicable voltage-time ride-through curve. Grid codes additionally require ride-through assessment under unbalanced fault conditions, such as single-phase-to-ground or line-to-line faults, which exercise the converter's negative-sequence current response separately from the symmetrical three-phase sag modeled in this work. Extending the model to represent such unbalanced grid conditions, and characterizing the Virtual Impedance mechanism's dynamic performance across both fault categories, is identified as a natural continuation of this work.

References

[1] M. M. Rahman, S. H. Dadon, M. He, M. Giesselmann, and M. M. Hasan, "An overview of power system flexibility: High renewable energy penetration scenarios," *Energies*, vol. 17, 24 2024, ISSN: 19961073. DOI: 10.3390/en17246393

[2] International Renewable Energy Agency, "Green hydrogen: A guide to policy making," IRENA, Abu Dhabi, Technical Report, 2020. [Online]. Available: https://www.irena.org/publications/2020/Nov/Green-hydrogen

[3] M. Carmo, D. L. Fritz, J. Mergel, and D. Stolten, "A comprehensive review on pem water electrolysis," *International Journal of Hydrogen Energy*, vol. 38, pp. 4901–4934, 12 2013, ISSN: 03603199. DOI: 10.1016/j.ijhydene.2013.01.151

[4] A. Buttler and H. Spliethoff, "Current status of water electrolysis for energy storage, grid balancing and sector coupling via power-to-gas and power-to-liquids: A review," *Renewable and Sustainable Energy Reviews*, vol. 82, pp. 2440–2454, 2018, ISSN: 18790690. DOI: 10.1016/j.rser.2017.09.003

[5] J. Rocabert, A. Luna, F. Blaabjerg, and P. Rodríguez, "Control of power converters in ac microgrids," *IEEE Transactions on Power Electronics*, vol. 27, pp. 4734–4749, 11 2012, ISSN: 08858993. DOI: 10.1109/TPEL.2012.2199334

[6] J. Matevosyan et al., "Grid-forming inverters: Are they the key for high renewable penetration?" *IEEE Power and Energy Magazine*, vol. 17, pp. 89–98, 6 2019, ISSN: 15584216. DOI: 10.1109/MPE.2019.2933072

[7] S. D'Arco, J. A. Suul, and O. B. Fosso, "A virtual synchronous machine implementation for distributed control of power converters in smartgrids," *Electric Power Systems Research*, vol. 122, pp. 180–197, 2015, ISSN: 03787796. DOI: 10.1016/j.epsr.2015.01.001

[8] O. Gomis-Bellmunt, S. D. Tavakoli, V. A. Lacerda, and E. Prieto-Araujo, "Grid-forming loads: Can the loads be in charge of forming the grid in modern power systems?" *IEEE Transactions on Smart Grid*, vol. 14, 2 2023, ISSN: 19493061. DOI: 10.1109/TSG.2022.3202646

[9] A. Olsson, "Green hydrogen from offshore wind in southern sweden: Case study on 500mw offshore wind farm," M.S. thesis, School of Electrical Engineering and Computer Science, KTH Royal Institute of Technology, Stockholm, Sweden, 2023.

[10] O. Schmidt, A. Gambhir, I. Staffell, A. Hawkes, J. Nelson, and S. Few, "Future cost and performance of water electrolysis: An expert elicitation study," *International Journal of Hydrogen Energy*, vol. 42, pp. 30 470–30 492, 52 2017, ISSN: 03603199. DOI: 10.1016/j.ijhydene.2017.10.045

[11] J Eichman, K Harrison, and M Peters, "Novel electrolyzer applications : Providing more than just hydrogen," *NREL Report*, September 2014.

[12] A. M. Abomazid, "Modeling and control of electrolysis based hydrogen production system," M.S. thesis, Graduate Program in Electrical Engineering and Computer Science, York University, Toronto, Ontario, Canada, 2021.

[13] S. D. Tavakoli et al., "Grid-forming services from hydrogen electrolyzers," *IEEE Transactions on Sustainable Energy*, vol. 14, 4 2023, ISSN: 19493037. DOI: 10.1109/TSTE.2023.3270295

[14] M. Canas and R. Esteves Araújo, "Power Electronics Systems for Green Hydrogen Production: An overview," en, *U.Porto Journal of Engineering*, vol. 12, no. 2, pp. 1–32, Jul. 2026, ISSN: 2183-6493. DOI: 10.24840/2183-6493_0012-002_003686 Accessed: Oct. 8, 2026. [Online]. Available: https://journalengineering.fe.up.pt/index.php/upjeng/article/view/2183-6493_0012-002_003686

[15] K. B. Tawfiq, H. Zeineldin, A. Al-Durra, and E. F. El-Saadany, "Emerging power electronic converters for hydrogen energy storage systems in smart cities: A comprehensive review," *IEEE Transactions on Industry Applications*, pp. 1–22, 2025. DOI: 10.1109/TIA.2025.3649445

[16] F. Perez, "Control of AC/DC Microgrids with Renewables in the Context of Smart Grids : Including Ancillary Services and Electric Mobility," Theses, Université Paris-Saclay ; Universidade federal de Itajuba. Brésil, Sep. 2020. [Online]. Available: https://theses.hal.science/tel-03050337

[17] V. Guida, D. Guilbert, and B. Douine, "Literature survey of interleaved dc-dc step-down converters for proton exchange membrane electrolyzer applications," *Transactions on Environment and Electrical Engineering*, vol. 3, 1 2019. DOI: 10.22149/teee.v3i1.129

[18] A. M. Elhawash, R. E. Araújo, and J. A. P. Lopes, "A New Adaptive Lead-Lag Control Scheme for High Current PEM Hydrogen Electrolyzers," en, pp. 1–6, Oct. 2023. DOI: 10.1109/VPPC60535.2023.10403130 Accessed: Sep. 12, 2026. [Online]. Available: https://ieeexplore.ieee.org/document/10403130/

[19] A. M. Elhawash, R. E. Araújo, and J. A. P. Lopes, "Frequency support from PEM hydrogen electrolysers using Power-Hardware-in-the-Loop validation," en, *International Journal of Hydrogen Energy*, vol. 175, p. 151 203, Oct. 2025, ISSN: 03603199. DOI: 10.1016/j.ijhydene.2025.151203 Accessed: May 28, 2026. [Online]. Available: https://linkinghub.elsevier.com/retrieve/pii/S0360319925042053

[20] A. Albalali, "Frequency stability of power electronic based power system with 100% renewable energy," M.S. thesis, School of Electrical Engineering and Computer Science, KTH Royal Institute of Technology, 2021.

[21] T. Qoria, "Grid-forming control to achieve a 100% power electronics interfaced power transmission systems," Ph.D. dissertation, École Nationale Supérieure d'Arts et Métiers (ENSAM), Lille, France, 2020.

[22] A. Camboni, "Parallel operation of grid-forming power inverters," M.S. thesis, School of Electrical Engineering and Computer Science, KTH Royal Institute of Technology, Stockholm, Sweden, 2023.

[23] F. Gonzalez-Longatt, J. L. Rueda, P. Palensky, H. R. Chamorro, and V. Sood, "Frequency support provided by inverted-based-generation using grid-forming controllers: A comparison during islanded operation," in *2021 IEEE Electrical Power and Energy Conference, EPEC 2021*, Institute of Electrical and Electronics Engineers Inc., 2021, pp. 113–118, ISBN: 9781665429283. DOI: 10.1109/EPEC52095.2021.9621418

[24] ENTSO-E, "High penetration of power electronic interfaced power sources (HPoPEIPS)," European Network of Transmission System Operators for Electricity (ENTSO-E), Implementation Guidance Document (IGD), 2017, Guidance document for national implementation for network codes on grid connection.

[25] MathWorks, *Design and analyze grid-forming converter*, https://www.mathworks.com/help/sps/ug/design-analyze-gridforming-converter.html, MATLAB & Simulink Documentation. Accessed: 27 July 2026.

[26] A. Hassan, O. Abdel-Rahim, M. Bajaj, and I. Zaitsev, "Power electronics for green hydrogen generation with focus on methods, topologies, and comparative analysis," en, *Scientific Reports*, vol. 14, no. 1, p. 24 767, Oct. 2024, ISSN: 2045-2322. DOI: 10.1038/s41598-024-76191-6 Accessed: Jul. 27, 2026. [Online]. Available: https://www.nature.com/articles/s41598-024-76191-6

[27] J. Fang, J. Liu, H. Wu, J. Chen, and F. Blaabjerg, "Chapter 2 - fundamentals of grid-forming converters," in *Grid-Forming Converters*, Academic Press, 2025, pp. 33–68, ISBN: 978-0-443-23735-5. DOI: https://doi.org/10.1016/B978-0-443-23735-5.00002-1 [Online]. Available: https://www.sciencedirect.com/science/article/pii/B9780443237355000021

[28] J. Fang, J. Liu, H. Wu, J. Chen, and F. Blaabjerg, "Chapter 5 - optimization of system design for grid-forming converters," in *Grid-Forming Converters*, Academic Press, 2025, pp. 191–239, ISBN: 978-0-443-23735-5. DOI: https://doi.org/10.1016/B978-0-443-23735-5.00005-7 [Online]. Available: https://www.sciencedirect.com/science/article/pii/B9780443237355000057

[29] J. Fang, J. Liu, H. Wu, J. Chen, and F. Blaabjerg, "Chapter 4 - control of grid-forming converters," in *Grid-Forming Converters*, Academic Press, 2025, pp. 131–190, ISBN: 978-0-443-23735-5. DOI: https://doi.org/10.1016/B978-0-443-23735-5.00004-5 [Online]. Available: https://www.sciencedirect.com/science/article/pii/B9780443237355000045

[30] K. Rahman, J. Hashimoto, and D. Orihara, "Virtual Impedance Control for Enhanced Current Limitation in Grid-Forming Inverters," en, in *2024 IEEE Third International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES)*, Delhi, India: IEEE, Apr. 2024, pp. 1078–1083, ISBN: 979-8-3503-8719-3. DOI: 10.1109/ICPEICES62430.2024.10719306 Accessed: Jun. 29, 2026. [Online]. Available: https://ieeexplore.ieee.org/document/10719306/

[31] T. Qoria, F. Gruson, F. Colas, G. Denis, T. Prevost, and X. Guillaud, "Critical Clearing Time Determination and Enhancement of Grid-Forming Converters Embedding Virtual Impedance as Current Limitation Algorithm," en, *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 2, pp. 1050–1061, Jun. 2020, ISSN: 2168-6777, 2168-6785. DOI: 10.1109/JESTPE.2019.2959085 Accessed: Jul. 2, 2026. [Online]. Available: https://ieeexplore.ieee.org/document/8931732/

[32] A. D. Paquette and D. M. Divan, "Virtual Impedance Current Limiting for Inverters in Microgrids With Synchronous Generators," en, *IEEE Trans. on Ind. Applicat.*, vol. 51, no. 2, pp. 1630–1638, Mar. 2015, ISSN: 0093-9994, 1939-9367. DOI: 10.1109/TIA.2014.2345877 Accessed: Jul. 3, 2026. [Online]. Available: https://ieeexplore.ieee.org/document/6872529

[33] I. Marcelo, "Conversor buck-boost com controle pi dedicado a um sistema autônomo de energia," M.S. thesis, Instituto Federal de Educação, Ciência e Tecnologia do Rio Grande do Sul, Porto Alegre, BR-RS, 2019.

[34] D. Govind, H. M. Suryawanshi, P. P. Nachankar, C. L. Narayana, and A. Singhal, "An enhanced master–slave control for accurate load sharing among parallel standalone AC microgrids," en, *International Journal of Circuit Theory and Applications*, vol. 51, no. 2, pp. 647–667, Feb. 2023, ISSN: 0098-9886, 1097-007X. DOI: 10.1002/cta.3445 Accessed: Jul. 27, 2026. [Online]. Available: https://onlinelibrary.wiley.com/doi/10.1002/cta.3445

[35] A. Mohd, E. Ortjohann, D. Morton, and O. Omari, "Review of control techniques for inverters parallel operation," en, *Electric Power Systems Research*, vol. 80, no. 12, pp. 1477–1487, Dec. 2010, ISSN: 03787796. DOI: 10.1016/j.epsr.2010.06.009 Accessed: Jul. 27, 2026. [Online]. Available: https://linkinghub.elsevier.com/retrieve/pii/S0378779610001392

[36] D. Guilbert, S. M. Collura, and A. Scipioni, "DC/DC converter topologies for electrolyzers: State-of-the-art and remaining key issues," *International Journal of Hydrogen Energy*, vol. 42, pp. 23 966–23 985, 37 2017, ISSN: 03603199. DOI: 10.1016/j.ijhydene.2017.07.174

[37] E. N. Mammeri, O. Lopez-Santos, A. E. Aroudi, J. Domajnko, N. Prosen, and L. Martinez-Salamero, "Modeling and control of a three-phase interleaved buck converter as a battery charger," *IEEE Access*, vol. 13, pp. 18 325–18 345, 2025. DOI: 10.1109/ACCESS.2025.3533032