FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO

Low Area Voltage Regulator for High-Speed Memory Interfaces

João Paulo Pinto Cunha



Mestrado em Engenharia Eletrotécnica e de Computadores

Supervisor: Prof. Vítor Tavares

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Approved in oral examination by the committee:

President: Prof. Manuel Cândido Duarte dos Santos
Referee: Prof. Luís Filipe Mesquita Nero Moreira Alves
Referee: Prof. Vítor Manuel Grade Tavares

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Resumo

Reguladores de tensão Low-dropout são amplamente utilizados em circuitos integrados modernos porque são capazes de fornecer tensões de alimentação estáveis e de baixo ruído para sistemas analógicos e digitais sensíveis.

Esta dissertação apresenta o projeto, avaliação e implementação de um LDO numa tecnologia CMOS de 55nm utilizando uma arquitetura de dispositivo de passagem NMOS. Para permitir o uso de um dispositivo de passagem NMOS mantendo uma tensão de dropout baixa, um *charge pump* é utilizado para gerar uma tensão de porta superior à tensão de alimentação nominal. O regulador inclui um amplificador de erro em cascode invertido para controlar a malha de realimentação e gerar uma tensão de saída precisa, independente das condições de alimentação e carga.

A metodologia de projeto adotada neste trabalho segue um fluxo de projeto de circuitos integrados analógicos hierárquico, no qual as especificações de nível de sistema são definidas e a arquitetura é selecionada, seguida pelo projeto de nível de transistor e implementação de layout. São analisados os compromissos entre corrente quiescente, desempenho transitório, estabilidade, razão de rejeição de ruído na alimentação, área de silício e eficiência energética. A implementação física segue técnicas de layout, como posicionamento simétrico de dispositivos e roteamento cuidadoso de redes importantes, a fim de aproximar os resultados o máximo possível dos obtidos nas simulações esquemáticas.

O LDO proposto é validado por meio de várias simulações, incluindo DC, AC, estabilidade, transitória e análises de Processo-Tensão-Temperatura. A verificação pós-layout é realizada para caracterizar o desempenho do LDO usando um modelo mais realista, com todas as não idealidades associadas.

Os resultados obtidos demonstram que o LDO proposto alcança uma operação estável em todas as faixas de operação, embora apresente degradação da margem de fase quando a corrente de carga é baixa. Alcança uma razão de rejeição de ruído na alimentação de aproximadamente -71dB para baixas frequências com 1mA de corrente de carga e um erro de saída de aproximadamente 2mV. Permanece robusto para simulações PVT, demonstrando a adequação do processo de projeto adotado.

Abstract

Low-dropout (LDO) voltage regulators are widely used in modern integrated circuits because they are capable of providing stable and low-noise supply voltages for sensitive analog and digital systems.

This dissertation presents the design, evaluation and implementation of an LDO in a 55nm CMOS technology using an NMOS pass device architecture. To enable the use of an NMOS pass device while keeping a low dropout voltage, a charge pump is used to generate a gate voltage higher than the nominal supply. The regulator includes a folded cascode error amplifier to control the feedback loop to generate an accurate output voltage independent of supply and load conditions.

The design methodology adopted in this work follows a hierarchical analog integrated circuit design flow, in which the system-level specifications are defined and the architecture is selected, followed by transistor level design, and layout implementation. Trade-offs between quiescent current, transient performance, stability, power supply rejection ratio, silicon area, and power efficiency are analyzed. The physical implementation follows layout techniques, such as symmetrical placement of devices, and cautious routing of important nets, in order to approximate the results as much as possible to the ones obtained in the schematic simulations.

The proposed LDO is validated through several simulations, including DC, AC, stability, transient, and Process-Voltage-Temperature (PVT) analyses. Post-layout verification is performed to check the performance of the LDO using a more realistic model, with all the non-idealities associated with the layout itself.

The obtained results demonstrate that the proposed LDO achieves a stable operation within all operating ranges, even though it has a phase margin degradation when the load current is low. It achieves a power supply rejection ratio of approximately -71dB for low frequencies for 1mA of load current with an output error of approximately 2mV. It remains robust for PVT simulations, demonstrating the suitability of the adopted design process.

UN Sustainable Development Goals

The United Nations Sustainable Development Goals (SDGs) provide a global framework to achieve a better and more sustainable future for all. It includes 17 goals[1] to address the world's most pressing challenges, including poverty, inequality, climate change, environmental degradation, peace, and justice.

The specific Sustainable Development Goals mentioned have the following names:

SDG 7 Ensure access to affordable, reliable, sustainable and modern energy for all

SDG 9 Build resilient infrastructure, promote inclusive and sustainable industrialization and foster innovation

SGD	Target	Contribution	Performance Indicators and Metrics
7	7.3	The proposed low-dropout voltage regulator improves power management efficiency in integrated electronic systems by reducing power losses and enabling low-power operation, contributing to more energy-efficient electronic devices.	Quiescent current, power efficiency, dropout voltage, power consumption.
	7.a	The design contributes to research and technological development in energy-efficient integrated circuits, supporting advances in power management solutions for modern electronic systems.	Successful design and verification of an integrated CMOS LDO; post-layout validation.
9	9.5	This work advances research in analog integrated circuit design through the development and physical implementation of a CMOS LDO regulator, contributing to innovation in semiconductor technology.	Complete IC design flow, layout implementation, DRC/LVS/PEX verification, simulation results.
	9.b	The proposed regulator demonstrates design methodologies and layout techniques that support the development of reliable and energy-efficient integrated circuits for future electronic applications.	Robust operation across PVT corners, stability analysis, transient response, PSRR and post-layout performance.

[1] https://sdgs.un.org/goals

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List of Acronyms

AI Artificial Intelligence
BIA Buffer Impedance Attenuation
BRI Body-Ripple Injector
CC-CG Cross-Coupled Common-Gate
CMOS Complementary Metal Oxide Semiconductor
CP Charge Pump
CPU Central Processing Unit
DC Direct Current
DIMM Dual Inline Memory Module
DNFL Dynamic Negative Feedback Loop
DNN Deep Neural Network
DRAM Dynamic Random-Access Memory
DRC Design Rule Check
EA Error Amplifier
FinFET Fin Field Effect Transistor
GBW Gain-Bandwidth product
HPC High-Performance Computing
IC Integrated Circuit
ICMR Input Common Mode Range
IoT Internet of Things
LDO Low Dropout Regulator
LVS Layout Versus Schematic
MOSFET Metal Oxide Semiconductor Field Effect Transistor
NMOS N-type Metal-Oxide-Semiconductor
OTA Operational Transconductance Amplifier
PCB Printed Circuit Board
PEX Parasitic Extraction
PI Pre-Emphasis Inverse
PMIC Power Management Integrated Circuit
PMOS P-type Metal-Oxide-Semiconductor

PVT Process, Voltage and Temperature

PSRR Power Supply Rejection Ratio

RCD Registered Clock Driver

SCE Short-Channel Effect

SR Slew Rate

SRC Supply-Ripple Cancellation

SSF Super Source Follower

UGF Unity Gain Frequency

WAG-NMC Wide-Range Adaptive-Gain Nested Miller Compensation

WPE Well-Proximity Effects

STI Shallow Trench Isolation

Chapter 1

Introduction

1.1 Context and Motivation

The emergence of services like Internet of Things (IoT), Cloud Computing, High-Performance Computing (HPC) and Artificial Intelligence (AI) has reinforced the need to store and process large quantities of data in the order of zettabytes [1]. Deep Neural Networks (DNNs) are essential components to perform the services mentioned above. However, as their parameters continue to increase, the number of operations and amounts of data required also increase [1]. This large number of operations leads to a great number of communications between the processor and off-chip memories due to a limit in memory bandwidth, as modeled by the Von Neumann architecture represented in Figure 1.1. This creates a bottleneck, decreasing the performance of the system, reinforcing the need for faster memory interfaces.

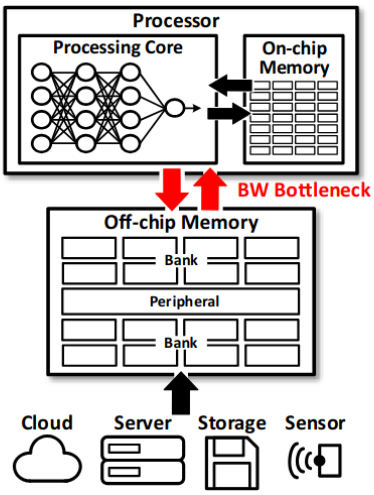


Figure 1.1: Von Neumann computing architecture. Reprinted from [1].

A Dynamic Random-Access Memory (DRAM) is composed by a certain number of cells and I/O components responsible for the communication with the outside of the chip [2]. A DRAM cell is a combination of two components: a capacitor that is used to store binary information as an

electrical charge and a transistor working as a switch that allows inserting/removing charge from the capacitor (representing a write/read from the memory). It is represented in Figure 1.2.

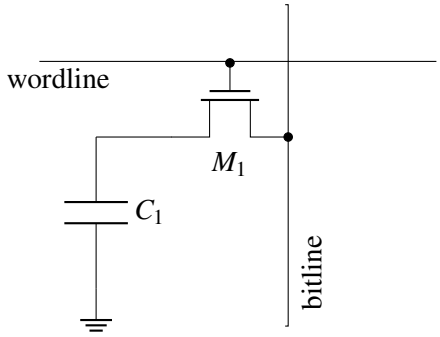


Figure 1.2: Basic DRAM cell [2].

A Dual Inline Memory Module (DIMM) consists on a Printed Circuit Board (PCB) with a great number of DRAMs. The design of this type of component is becoming increasingly harder due to the demand of large and fast memories [3]. Signal integrity on such conditions can be compromised due to the presence of non-ideal effects.

To allow maximum speed for DIMMs, a chip called Registered Clock Driver (RCD) is employed. The Central Processing Unit (CPU) memory controller sends the address, command, and clock signals to the RCD, and the latter is responsible for sending them to the DRAM chips [4]. This technique preserves signal integrity because the buffering of the RCD reduces substantially the load on the memory controller. The RCD does not buffer data signals, as they have a direct path between the memory controller and the DRAMs.

Usually, a system like the RCD is composed by several functional blocks and not all of them can be supplied with the same voltage as each one of them has specific power requirements [5]. A Power Management Integrated Circuit (PMIC) is used to deliver different supply voltages to different circuit blocks using voltage regulators. The voltage ratio $\frac{V_{out}}{V_{in}}$ can be either less or greater than 1, which means that they can function as step-up or step-down. By employing a voltage regulator, it is possible to generate a voltage ideally independent of supply conditions.

In memory systems, if a power supply falls below a certain value, data corruption can occur, and the reliability of the system can be compromised [6]. This is because noise and leakage currents will be more impactful on the system, creating bit errors and data loss. A well designed regulator is able to reject the noise present in the supply and reduce the risk of data corruption. The transient response is also an important parameter in the design of regulators as it evaluates its capability of maintaining a fixed voltage when sudden load changes happen.

1.2 Objectives

The main objective of this dissertaion is to design, implement and validate a voltage regulator using a 55nm Complementary Metal Oxide Semiconductor (CMOS) technology. To achieve this, the following goals were defined:

- Define the specifications of the system.
- Analyze several architectures and choose the most suitable one.
- Design the main building blocks
- Validate the performance through extensive simulations
- Develop the physical layout of the circuit
- Verify the physical implementation

The accomplishment of these objectives demonstrates a complete methodology for the design and physical implementation of a CMOS voltage regulator.

1.3 Dissertation organization

This document is organized into 5 chapters, each one presenting a different stage of the design and implementation of the proposed architecture.

Chapter 2 provides the fundamentals required to understand the design process. It reviews the operating principles of a basic regulator, including the most important parameters used to evaluate its performance. It also provides relevant literature review to serve as a reference to compare with the proposed design.

Chapter 3 presents the design methodology of the proposed circuit. Starting by the system-level specifications, the design requirements are defined. It presents the architecture selection process and shows the design insights of each funcional block. To conclude, the process of layout development is shown.

Chapter 4 evaluates the performance of the proposed design through extensive simulations. This chapter concludes with a summary of the characteristics of the circuit.

Chapter 5 summarizes the main achievements of the dissertation and presents possible future improvements that can be implemented in the proposed design.

Chapter 2

Background and State-of-the-Art

2.1 Fundamentals of Voltage Regulation

A voltage regulator is a circuit that has the capability to generate a constant output voltage independent of changes in the supply voltage and load variations. This family of circuits can be divided into two types: linear and switching regulators.

Linear voltage regulators employ a pass transistor (BJT or MOSFET) controlled by a high-gain Error Amplifier (EA) to maintain a steady output voltage in the presence of input voltage or load variations [7]. The output voltage (or some fraction of it) is compared with a reference voltage using an EA. The output voltage of the error amplifier will control the current in the pass device to keep the output voltage constant. An example for this type of circuit is shown in Figure 2.1. The zener diode defines the voltage at the non-inverting input. That voltage is then compared with V_{FB} to adjust the current in the transistor.

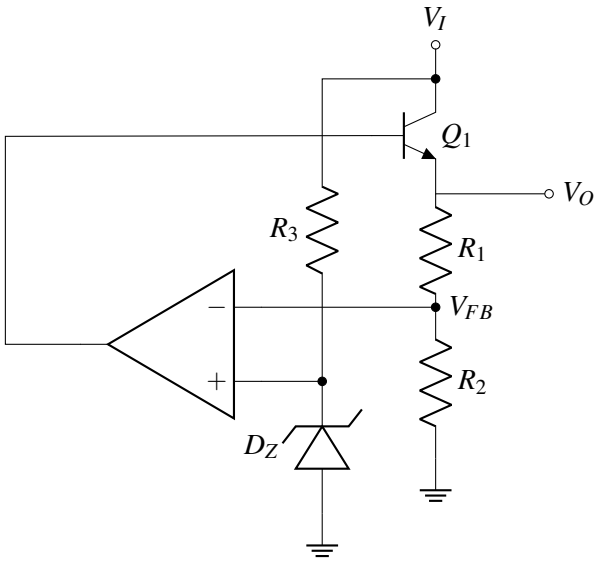


Figure 2.1: Schematic example of a linear regulator. Adapted from [8].

Contrary to linear regulators that use operational amplifiers to compare a reference voltage with a fraction of the output, switching regulators use another method to maintain a constant output. In this type of regulator, the transistor operates as a switch that acts as an open-circuit or short-circuit depending on the gate/base voltage [9]. That voltage is generated by another control circuit. In addition to the transistor, these circuits also use inductors, capacitors and diodes that can be arranged in multiple ways to achieve a desired functionality (step-up or step-down). Figure 2.2 shows the schematic of a Buck Converter, a classic example of switching regulator. The region of operation of M_1 is controlled by the v_{CTRL} voltage, which oscillates with a defined frequency.

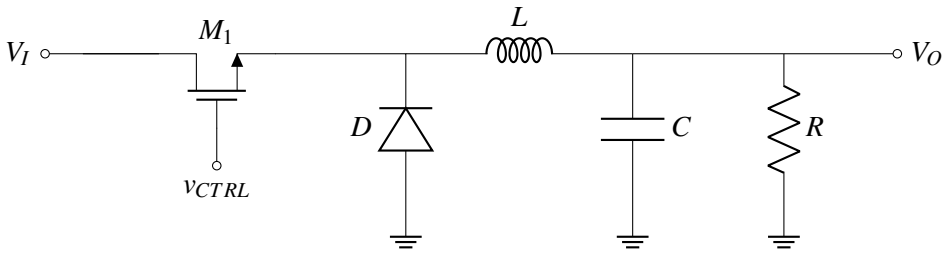


Figure 2.2: Standard Buck Converter topology.

In applications that demand a very clean and stable supply, linear regulators are generally preferred over switching converters because of their inherently lower output noise and ripple [7]. Switching regulators rely on high-frequency switching and energy storage elements, which introduce spectral components and ripple into sensitive blocks. To obtain a clean voltage whose value is close to the power supply, a specific type of linear regulator known as Low Dropout Regulator (LDO) is necessary. The traditional topology and fundamental knowledge about that type of circuit is presented in section 2.2.

2.2 Basics of LDO Regulators

The standard structure of an LDO is illustrated in Figure 2.3 [10]. In their fundamental configuration, they comprise a pass transistor, an error amplifier, a resistive feedback network, and a reference voltage. The circuit needs to be designed to function with a minimal dropout voltage.

In addition to the dropout voltage, the following metrics are also of interest in LDO design [10]:

- Power Supply Rejection Ratio (PSRR): this parameter refers to the capability of the output to stay constant despite variations in the input.
- Load Regulation: measures the ability of the output to remain constant when the load current changes.
- Output noise: the noise produced by the LDO that is reflected in the output even when the input is clean.

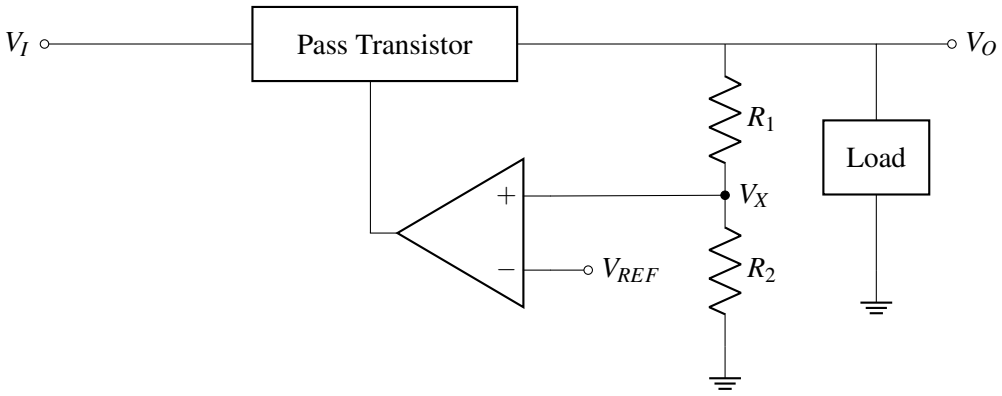


Figure 2.3: Standard LDO topology. Adapted from [10].

- Stability: a good phase margin is required to control the stability of the feedback loop.
- Power consumption and area: if a system uses many LDOs, these parameters need to be minimized.

Several parameters such as PSRR and stability are all significantly impacted by the pass transistor selection in an LDO. For this component both P-type Metal-Oxide-Semiconductor (PMOS) and N-type Metal-Oxide-Semiconductor (NMOS) can be used. If a PMOS is chosen, it will act as a controlled current source, while if an NMOS is employed, it will behave like a source follower [10].

The PMOS LDO is a typical choice because it has a lower dropout voltage compared with its NMOS counterpart. However, because of its low frequency pole at the output, this topology can be a concern in terms of stability [11].

The NMOS LDO has a better PSRR and because the output pole is placed at high frequency, the stability of the loop is easier to control [11]. The main drawback of this architecture is the fact that it has a greater dropout voltage [10]. To overcome this issue, the error amplifier needs to be supplied using a Charge Pump (CP) that will step-up the supply voltage of the circuit. This architecture is investigated in more detail in section 2.3.

2.3 Source Follower LDO

The standard architecture of the LDO with the pass transistor (NMOS) acting as a source follower is shown in Figure 2.4.

By looking at the schematic of the circuit, it is possible to conclude that, ideally, the output voltage v_o does not depend on v_i. The PSRR of the circuit is given by:

$$PSRR = \frac{\partial v_o}{\partial v_i} \rightarrow 0 \tag{2.1}$$

In this case, considering that the output resistance of M_1 (r_{o1}) and the gain A_1 are infinite the

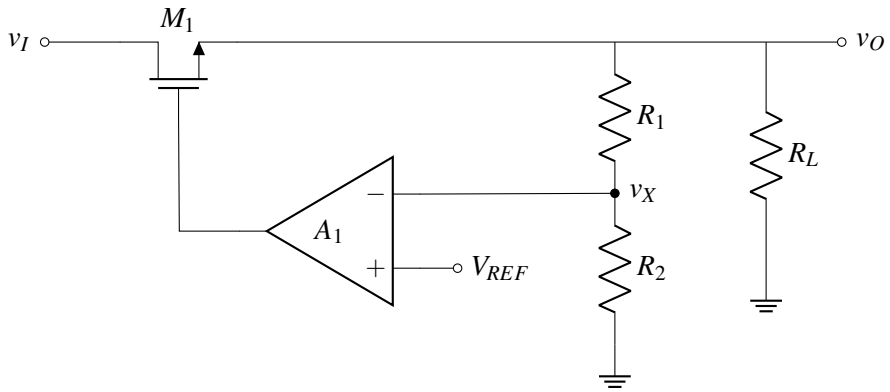


Figure 2.4: Schematic of the NMOS LDO. Adapted from [10].

PSRR tends to 0 for low frequencies.

The problem with the high dropout voltage arises from the fact that the maximum voltage at the error amplifier output is equal to the supply voltage and the minimum dropout required to keep the transistor in the saturation region is its threshold voltage [10]. A CP is required to increase the supply voltage and give it to the EA. By doing this, the gate voltage can be higher and it is possible to reduce the dropout.

To calculate the output impedance of the circuit, the model illustrated in Figure 2.5 is used. This value corresponds actually to the load regulation. It is given by the following expression:

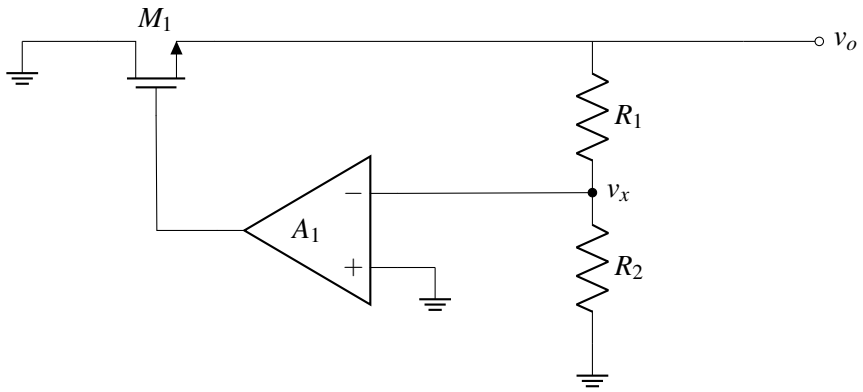


Figure 2.5: Model to calculate the LDO's output impedance. Adapted from [10].

$$R_o = \frac{v_o}{i_o} = \frac{1}{\frac{1}{R_1+R_2} + g_{m1}(1 + A_1 \frac{R_2}{R_1+R_2})} \tag{2.2}$$

Since $R_1 + R_2 \gg 1$ and $A_1 \frac{R_2}{R_1+R_2} \gg 1$,

$$R_o \approx (1 + \frac{R_1}{R_2}) \frac{1}{g_{m1} A_1} \tag{2.3}$$

where g_{m1} is the transconductance of M_1.

To calculate the PSRR considering the output resistance of the transistor (r_{o1}), the circuit can be seen as a voltage divider between r_{o1} and R_{out} [10].

$$PSRR = \frac{v_o}{v_i} = \frac{R_o}{R_o + r_{o1}} \approx (1 + \frac{R_1}{R_2}) \frac{1}{g_{m1} r_{o1} A_1} \tag{2.4}$$

Analyzing equations 2.3 and 2.4, one can conclude that both the PSRR and the load regulation lead to better results when the open loop gain (A_1) of the error amplifier is high.

It is important to note that the gain of the amplifier will be affected by its poles [10]:

$$A_1 = \frac{A_0}{1 + \frac{s}{\omega_0}} \tag{2.5}$$

Where ω_0 represents the dominant pole of the error amplifier. Naturally these poles will degrade both PSRR and load regulation.

$$PSRR = \frac{v_o}{v_i} = (1 + \frac{R_1}{R_2}) \frac{1}{A_0 g_{m1} r_{o1}} (1 + \frac{s}{\omega_0}) \tag{2.6}$$

$$R_o \approx (1 + \frac{R_1}{R_2}) \frac{1}{g_{m1} A_0} (1 + \frac{s}{\omega_0}) \tag{2.7}$$

Several techniques are presented in the literature to improve the performance of the circuit despite the presence of these poles.

2.4 Fundamentals of Analog IC Layout

The layout of an Integrated Circuit (IC) is a two-dimensional map composed by several geometric shapes used to define the masks that will be used in fabrication [12]. Those geometric shapes include:

- Active areas: where transistors are defined.
- Polysilicon: used to build transistor gates.
- Metal layers: used to make interconnections between the different nets of the circuit.
- Contacts: make connections between different layers.

Figure 2.6 shows a possible layout for a CMOS inverter. It is composed by an NMOS on the left and a PMOS on the right. The connections between the two devices are made using metal, represented by the blue rectangles. The black shapes are the contacts. Dashed yellow and green are the n^+ and p^+ implants, respectively. The n-well is represented in orange while the light green rectangles are made of polysilicon. These devices are sunken into the substrate.

The development of the layout is an important step in analog design. It is where the most realistic model of the circuit can be obtained taking into account the maximum number of non-idealities. Because of that, it has to be developed in a very cautious way, in order to keep the

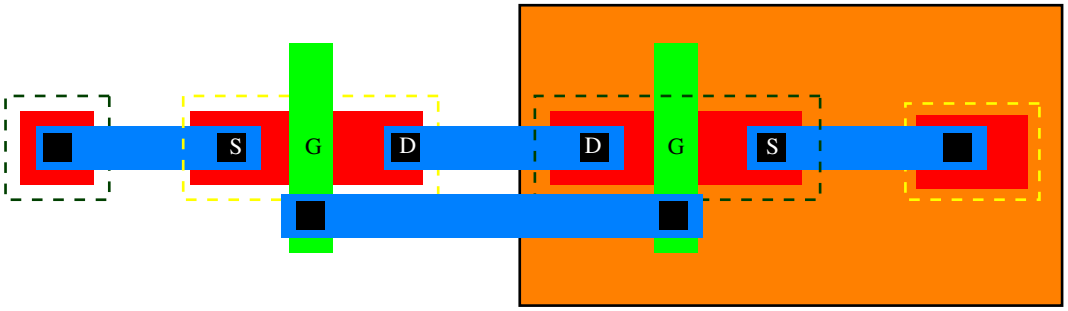


Figure 2.6: Layout of a CMOS inverter.

performance of the design as satisfactory as possible. Several techniques for analog layout are present in the literature to minimize the impact of parasitics and keep the robustness of the design.

2.4.1 Cross-Section of an IC

Figure 2.7 shows the cross-section of the CMOS inverter. The bulk of the PMOS transistor is represented by the n-well, which needs to be biased with a voltage higher than the substrate voltage (V_{SS}) to avoid the flow of current through the bulk. The substrate also corresponds to the bulk of the NMOS transistor, which means that in this process, the NMOS needs to have its bulk connected to V_{SS}. To connect the bulk of an NMOS to a voltage higher than V_{SS}, a p-well isolated by a deep n-well can be used, known as triple-well process. This approach comes with a higher cost of production and area.

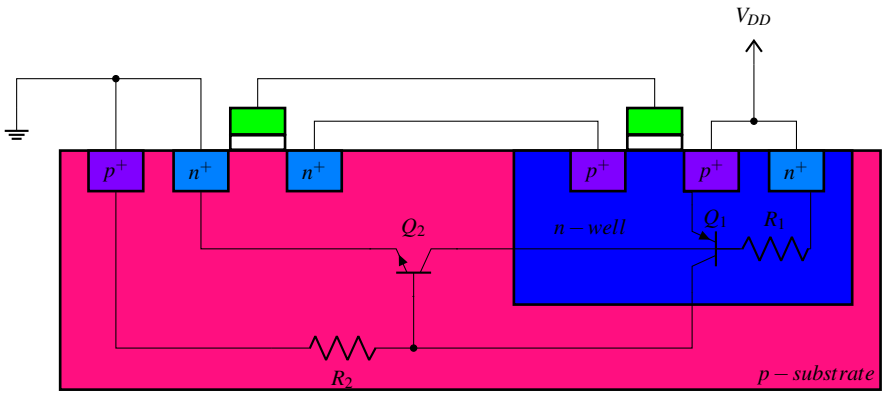


Figure 2.7: Cross-section of a CMOS inverter.

2.4.2 Latch-Up

Observing the cross-section of the CMOS inverter represented in Figure 2.7 it is possible to note the presence of a PNP bipolar transistor, Q_1, whose terminals are the p^+ implant, the n-well and the p substrate [12]. An NPN transistor is observable in similar conditions but in the NMOS device.

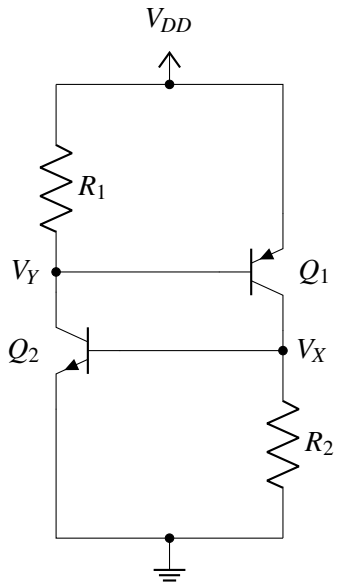


Figure 2.8: Model to represent latch-up

The parasitic circuit that represents the latch-up effect is represented in Figure 2.8. Analyzing the circuit, it is possible to observe the presence of a positive feedback loop. If a current starts flowing through R_2, the collector current of Q_2 will increase, decreasing the value of V_Y. This will cause the collector current of Q_1 to increase. Eventually the current from V_{DD} will be too high. To avoid that phenomenon, it is important to minimize the loop gain of this circuit [12]. This can be done by biasing the substrate and the n-well with guard-rings, that are composed by several contacts, reducing R_1 and R_2.

2.4.3 Impact of Parasitics

The layout of the IC introduces non-idealities that, most of the time, are not present after the schematic design. These non-idealities can come from the interconnects and transistors themselves. Although in the schematic phase it is possible to observe some parasitics, the layout gives a more realistic model.

An illustration of the parasitics can be seen in Figure 2.9. R_1 and R_2 represent resistances associated with the length of the metal layers. The capacitances C_{12} and C_{1sub} are the capacitances between the two metal layers and between the metal and the substrate, respectively.

The parasitic capacitances can be a concern regarding stability because they can change the position of the poles, affecting the frequency response of the circuit. The capacitances between metal traces that carry different signals can lead to issues such as crosstalk [12]. In the case of an LDO, which is a negative feedback system, the loop bandwidth and phase margin can become degraded if the layout is not designed carefully to handle the parasitics.

The parasitic resistances introduced by the length of the metal can lead to problems such as IR drop along the interconnection if the current in that specific branch is significantly high. Thermal noise can also be a concern in case long metal traces are used [12]. The parasitics can form an

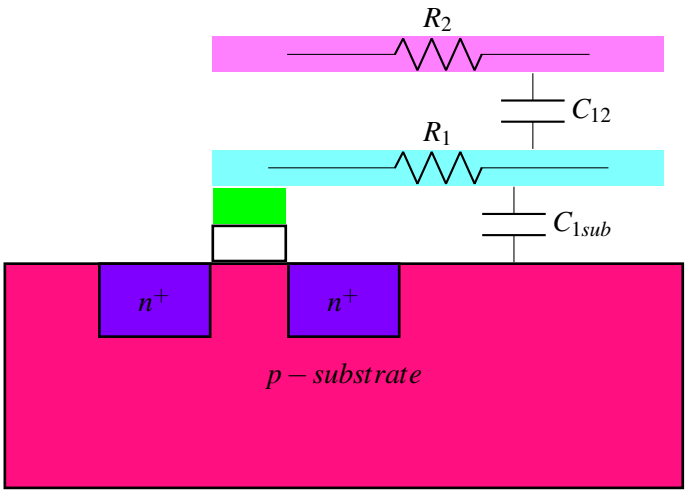


Figure 2.9: Layout of an NMOS transistor with interconnect parasitics.

RC network such as illustrated in Figure 2.9, increasing time constants of the circuit and slowing it down.

2.4.4 Well Proximity Effects and Dummy Devices

The n-well of a PMOS device is formed through a process of ion implantation where atoms are introduced in the substrate with focused beam [13]. The duration and intensity of the implantation are the most important factors that determine the dosage of the doping.

The main issue is that the implant is not placed at a 90° angle to the wafer [13], as it can be seen in Figure 2.10. This is a problem because the implant will reflect from the walls made by oxide and photoresist, causing the middle of the well to be doped with a different dosage from the areas in the border.

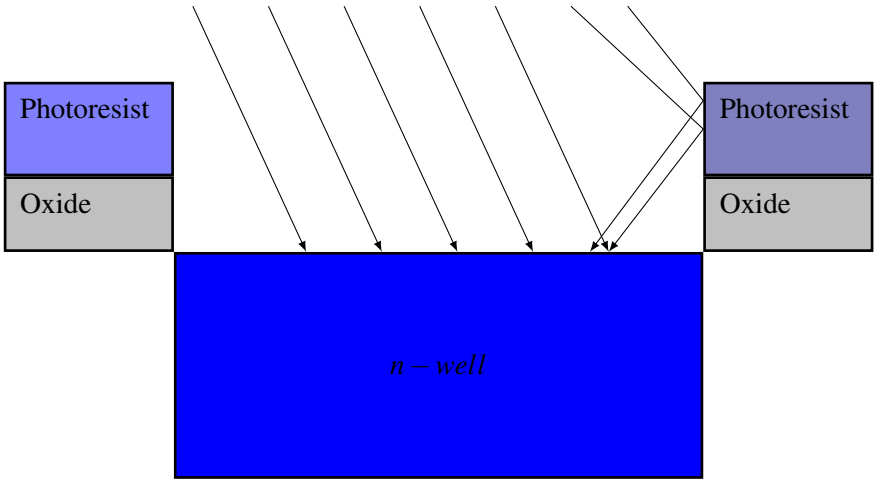


Figure 2.10: Representation of ion implantation [12].

That non-uniformity can cause differences between the parameters of the devices that are located in the border of the well and the ones located in the middle, causing a mismatch in V_{TH} for example. To avoid this issue, the active devices should be located as far as possible from the beginning and the ending of the well [13]. Another way to protect the active device is to put dummies surrounding an array of active devices. Those dummies are not active, which means they do not play a role in the design of the circuit but are important to protect the main devices. They can also be used to improve matching.

2.4.5 Shallow Trench Isolation

During fabrication, it is important to isolate adjacent transistors in the same silicon substrate. This is important to avoid the formation of a channel between them [12]. This is done using a technique called Shallow Trench Isolation (STI), in which an oxide layer surrounds the devices. Figure 2.11 shows a multifinger MOS device surrounded by a shallow trench, represented in light blue.

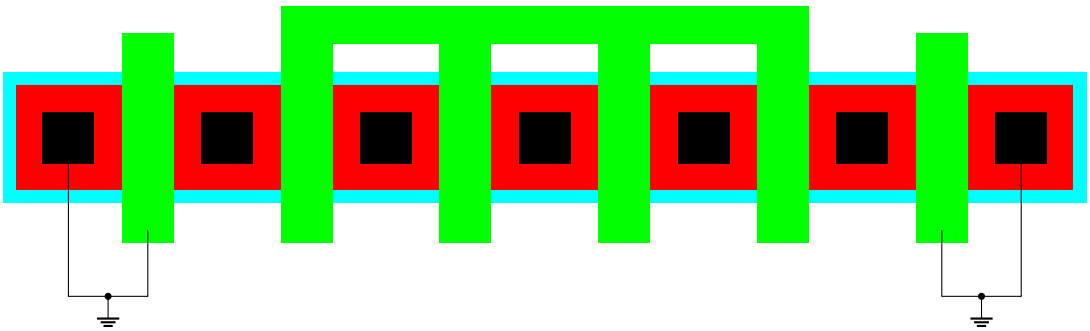


Figure 2.11: Device surrounded by shallow trench. Adapted from [12].

The oxide filling the trench can induce stress on the active device surrounded by it [12]. This stress can modify certain properties, such as V_{TH} and g_m. If two transistors that are supposed to be matched experience different environments, a mismatch can occur. The insertion of dummies, such as the ones presented in Figure 2.11 can minimize the effect caused by STI.

2.4.6 Matching Principles

Since the performance of analog circuits is strongly dependent on matching between the devices whether they are passive or active, it is important to assure that those boundaries remain as precise as possible. A deviation of the parameters of a certain device can decrease the performance of the system, introducing problems such as offset voltages.

One of the main concerns of analog layout is to minimize systematic mismatches by ensuring that the most important devices are fabricated in identical conditions. It is important that those devices remain close to each other, with identical orientations, and ensure that they share identical environments [12]. Figure 2.12 shows an example of matching of two devices. It is important to add dummy devices there to improve symmetry and ensure that both drain and source of M_1

and M_2 see the same environment. It is also relevant to observe that all the devices have the same orientation.

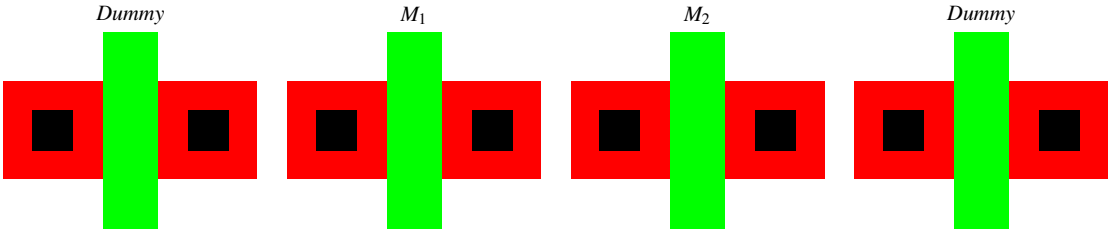


Figure 2.12: Active devices surrounded by dummies [12].

Several layout techniques have been developed to improve device matching. One of the most commonly used techniques is interdigitation. This approach requires that the devices are divided into several unit elements and are alternated in the layout. Figure 2.13 shows an example of interdigitation in which devices M_1 and M_2, by alternating one another, are exposed to similar process variations, making sure that the gradient affects both in the same way [14].

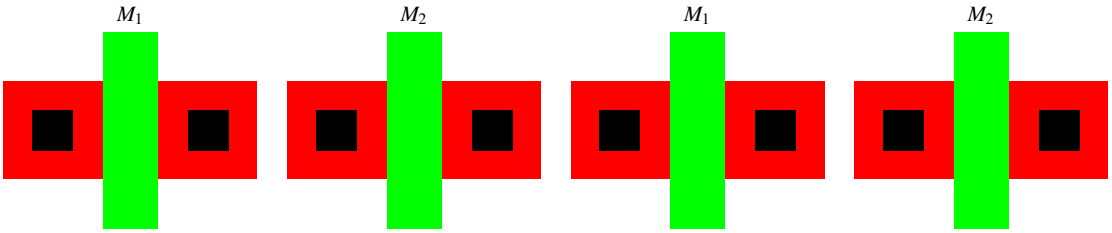


Figure 2.13: Interdigitated layout.

Another widely adopted technique is the common-centroid. In this case, the unit elements are placed in a way that they form a symmetry around a common centre. An example of this approach is shown in Figure 2.14. This configuration is capable of equalizing the effect of gradient along all the directions, maximizing device matching. Common-centroid layout is exceptionally effective for important structures such as differential pairs. The main drawback is that the routing in this type of configuration can be hard to develop [12].

2.4.7 Antenna Effect

Etching is used to create metal interconnects during fabrication. During this process, a layer of metal connected to the gate of a transistor can accumulate charge, acting as an antenna [12]. If the area of that metal is big enough, the charge present in it can increase the gate voltage above a level that it breaks down the gate oxide.

Usually, design rules for different technologies limit the area for the materials connected to the gate. More specifically, a maximum ratio between gate area and the area of the material connected to the gate is defined.

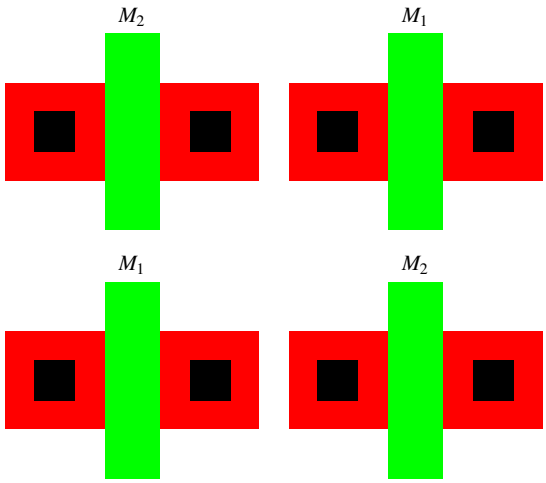


Figure 2.14: Common-centroid layout.

2.4.8 Electromigration

The atoms of a material can move due to the flow of current through it. This phenomenon is called electromigration [15]. If in a certain volume of metal, the number of atoms leaving and arriving is not equal, the material can be damaged. Two types of failures can occur [15]:

- Voids: result of a depletion of atoms and can lead to open circuits.
- Hillocks: result of a deposition of atoms and can lead to short-circuits.

The widths of the metal interconnects should be adjusted taking into consideration the value of the current that flows through them. An EM/IR analysis can be used to evaluate the effect of electromigration in the design.

2.4.9 Comparison Between Planar MOSFETs and FinFETs

The most recent technology nodes are not using the classical planar structure anymore. They use a type of three-dimensional device called Fin Field Effect Transistor (FinFET) [16]. This structure is more suitable for lengths below 20nm, giving a significant boost in performance.

Figure 2.15 shows the arrangement of a FinFET. It is composed of a silicon material called fin, represented in light grey, a dielectric surrounding it, and the gate above that dielectric [16].

In [17], a comparison between device parameters of FinFETs and planar Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) is performed. The main issue with the scaling of the devices in planar technologies is that the gate struggles to control the channel for lower nodes, leading to Short-Channel Effects (SCEs) and leakage currents. Since in the FinFET the gate surrounds the fin, it manages the channel in a more efficient way, preventing the issues stated before. The comparison between the two is done with a value of $V_{DD} = 1.2$V and an overdrive voltage of 200mV [17]. The first test that is done is the plot of g_m in function of the gate length, and it shows that the behaviour is similar for both planar and FinFET approaches. However the value of g_{ds}

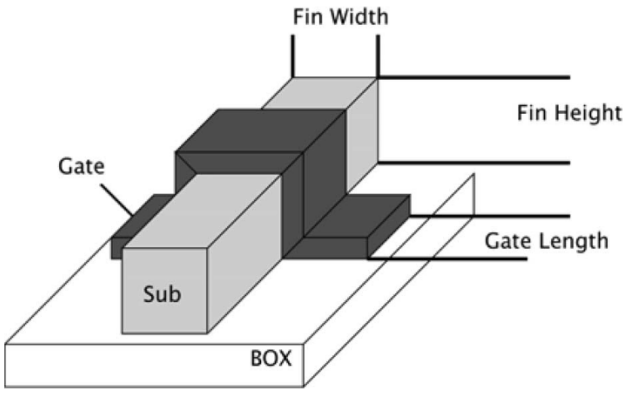


Figure 2.15: Structure of a FinFET. Reprinted from [17].

for a FinFET is significantly lower for the same length, providing a higher g_m/g_{ds} gain [17]. The cut-off frequency of the two structures is similar, since they have similar values of g_m and C_{gs}.

2.5 State-of-the-Art

Over the years, several LDO architectures have been proposed to satisfy different application requirements. Approaches such as adaptive biasing methods, capacitor-less topologies, and compensation techniques have been introduced to improve overall performance and reduce power consumption and silicon area.

In this section, contributions from the literature are presented, highlighting the architectures, design techniques, and performance metrics that each design intends to improve.

2.5.1 LDO with Buffer Impedance Attenuation

An LDO that improves transient response with low quiescent current is presented in [18]. It makes use of a technique called Buffer Impedance Attenuation (BIA), which consists of inserting a buffer stage with variable output impedance between the error amplifier and the PMOS pass device.

This work employs a large external output capacitor, in order to move the output pole to low frequencies. The output pole becomes, therefore, the dominant one. Stability in such conditions can be degraded due to the low frequency non-dominant pole in the gate of the PMOS pass device [18]. To solve this issue, a buffer can be used to drive the pass transistor, as shown in Figure 2.16.

Observing Figure 2.16, it is possible to identify three poles: the node V_O, the output of the error amplifier, and the output of the buffer [18]. To ensure stability, the input capacitance and the output resistance of the buffer should be as small as possible to push the non-dominant poles to high frequencies.

To implement the buffer, a source-follower can be considered. The output resistance of such a block is $1/g_m$. The value of g_m must be maximized to minimize the output resistance. To increase the value of g_m, the bias current of the device can be increased, which leads to an increase in

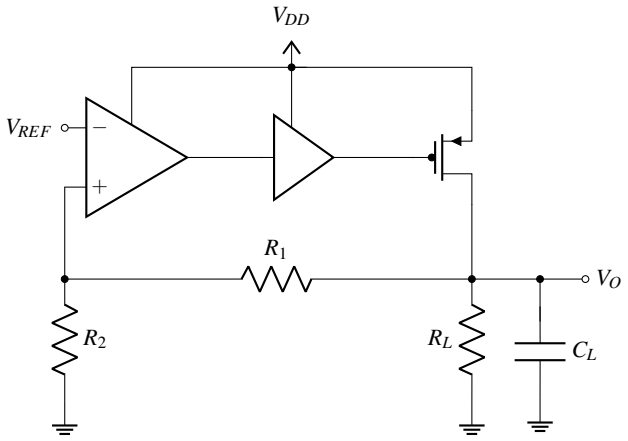


Figure 2.16: Representation of the driving of the pass device by a buffer in an LDO. Adapted from [18].

quiescent current. Another approach is to increase W/L of the transistor, which will increase the input capacitance of the buffer, leading to stability problems [18]. This means that a simple source-follower is not a suitable solution.

Figure 2.17 (a) presents the proposed buffer using a negative feedback technique. If there is an increase in the voltage at N_2, the drain current of M_{21} increases, increasing the base current of Q_{20}, and consequently its collector current [18]. The output resistance of the buffer will be given by

$$R_{o,buffer} = \frac{1}{g_{m21}(1+\beta)} \tag{2.8}$$

where β is the current gain of the NPN transistor.

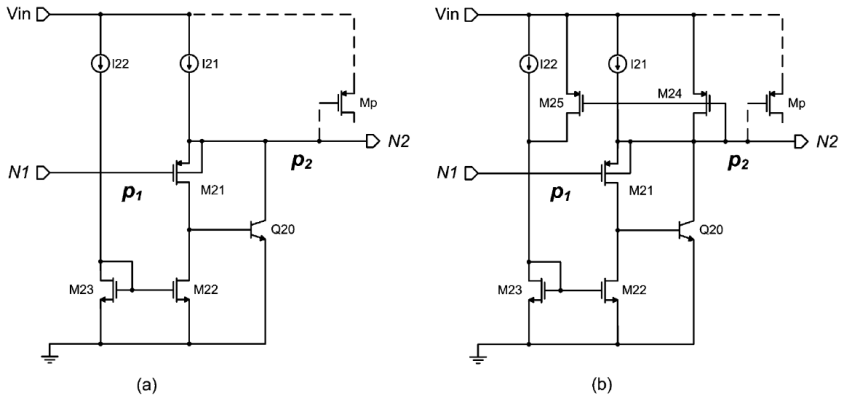


Figure 2.17: Source follower using shunt feedback technique. In (b), dynamic biasing is used. Reprinted from [18].

In Figure 2.17 (b), devices M_{24} and M_{25} are added to bias the buffer dynamically. When the load current rises from low to high, voltages at N_1 and N_2 decrease. Drain current of M_{24} and

$M25$ will step up, biasing the buffer with a higher current in that instant, increasing g_{m21} [18]. The resistance seen by the gate of the PMOS pass device will be

$$R_{o,buffer} = \frac{1}{g_{m21}(1+\beta)+g_{m24}} \tag{2.9}$$

2.5.2 Capacitorless LDO Architecture

Some LDO architectures require a very large output capacitor to ensure stability. It is impossible to integrate capacitors in the microfarad range. In [19], a capacitorless PMOS LDO is presented, with a smaller output capacitor in the picofarad range, allowing it to be placed on-chip. The topology is depicted in Figure 2.18.

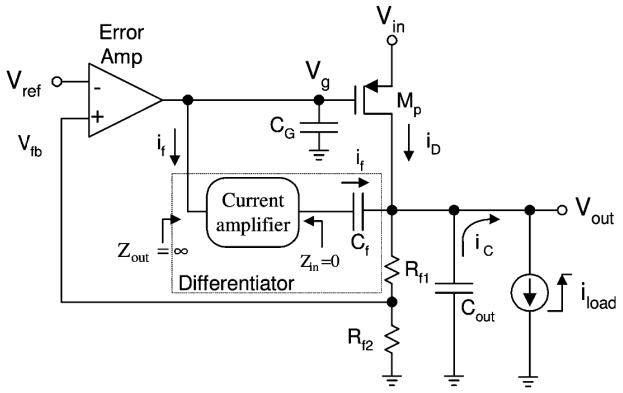


Figure 2.18: Schematic of the LDO employing a differentiator. Reprinted from [19].

Considering a typical PMOS LDO without a buffer between the error amplifier and the pass transistor, replacing the large output capacitor by a smaller one, will turn the gate of the pass transistor the dominant pole P_1 of the system. Since the pass device is large, P_1 is located at low frequency [19]. The second pole P_2 is located at the output and its frequency varies strongly with the load current, creating stability issues.

When the load current experiences a sudden change from low to high, the voltage at the gate of the PMOS pass device will take a certain amount of time to settle. That time delay is mainly associated with the delay of the pass transistor [19]. In Figure 2.18, the differentiator acts as a fast loop, speeding up the transient response.

The differentiator is useful to improve the transient response of the LDO and also serves as a compensation scheme [19]. When there is a sudden change in the output voltage, a current i_f flows through C_f and C_G, helping V_g to reach its final value faster. Once V_{out} and V_g settle, C_f acts as an open circuit once again. The differentiator also performs pole-splitting, improving the stability of the system.

2.5.3 C-Multiplier for Capacitorless LDO

In [20], a technique to improve the PSRR of an LDO is presented. The performance of supply-noise sensitive circuits can be improved when they are supplied by a high PSRR regulator.

Capacitorless LDOs usually have maximum load capacitance values below 100pF [20]. This is because, since the output pole is not dominant, having a large value of C_L can reduce the phase margin and affect the stability of the system. To overcome that limitation, the LDO proposed in [20] employs a capacitance multiplier in order for the dominant pole to be associated with V_{out}, as shown in Figure 2.19.

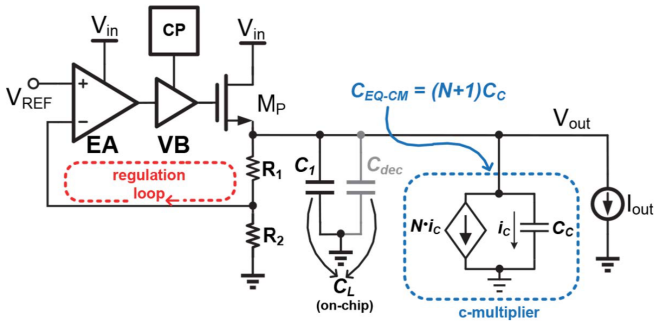


Figure 2.19: Schematic of the LDO employing a c-multiplier. Reprinted from [20].

Miller compensation is widely used in capacitorless regulators since it allows to compensate the circuit using a relatively small capacitance. This type of compensation involves moving the pole at the gate of the pass device to low frequencies. Because of that, the limited value of the bandwidth of the EA will degrade the loop-gain and the PSRR [20]. When a large C_L is used, defining the output node as the dominant pole, the output capacitor will be able to reject noisy frequencies below the first nondominant pole or the Unity Gain Frequency (UGF) of the LDO, depending on which one appears first [20].

The behaviour of the c-multiplier in Figure 2.19 is similar to a big output capacitor with a capacitance equal to C_{EQ_CM} [20]. This technique ensures that the pole at V_{out} is dominant regardless the value of the capacitance of the load.

2.5.4 Adaptively Biased Capacitor-less LDO

In [21], a fully integrated, output capacitor-less NMOS LDO that supports fast load steps without using bulky off-chip capacitors is presented. To obtain fast transient response without external capacitance, the regulator must achieve wide loop bandwidth and high slew rate at the pass device gate, while remaining stable over a broad load current range. The schematic of the circuit is presented in Figure 2.20.

The use of NMOS pass transistor M_N provides a larger Gain-Bandwidth product (GBW) and slew-rate compared to the PMOS, which translates to a decrease in the output transient response

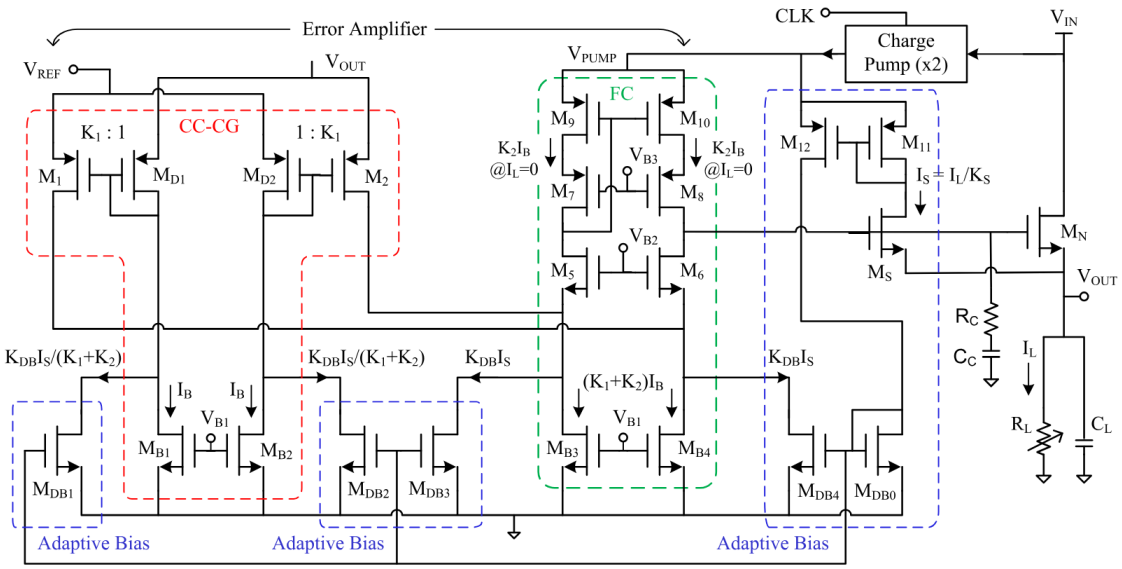


Figure 2.20: Schematic of the adaptively biased LDO. Reprinted from [21].

time [21]. The low output impedance of the source follower configuration is also a parameter to take advantage in this design.

Instead of a conventional structure, the LDO employs an error amplifier with a Cross-Coupled Common-Gate (CC-CG) input stage. This structure provides a low input impedance pushing the output pole to a higher frequency.

The Adaptive Biasing Circuit is central to the LDO's rapid transient response. The circuit functions by sensing the load current (I_L) flowing through the main regulation FET and dynamically increasing the error amplifier's bias current during load changes [21]. Transistor M_S is responsible for sensing the current through the pass transistor M_N. The current mirror M_{11}-M_{12} will be responsible to deliver the sensed current to M_{DB0} and M_{DB4} that will mirror the current to the error amplifier. This method enables a fast response from the LDO to transient load currents, enabling a fast transition to a stable final output value by improving the error amplifier slew-rate.

2.5.5 Adaptive Supply-Ripple Cancellation Technique

A common technique to remove peaking in the PSRR of an LDO is to add an external capacitor [10] that will act as a short-circuit from the output voltage to ground for high frequencies. This will make the LDO output independent of high frequency components that come from the supply or the load itself. To avoid the use of a large output capacitor, a Supply-Ripple Cancellation (SRC) technique can be implemented [22]. The SRC will amplify the ripples (v_r) in the supply voltage and inject them into the gate or body of the transistor [22]. The factor of amplification will vary accordingly to the necessary voltage to cancel the ripple effect. Figure 2.21 shows an example of an LDO with SRC injected into the gate terminal. The idea is to find the optimal value of v_{src} to eliminate the current created by the supply ripple, Δi.

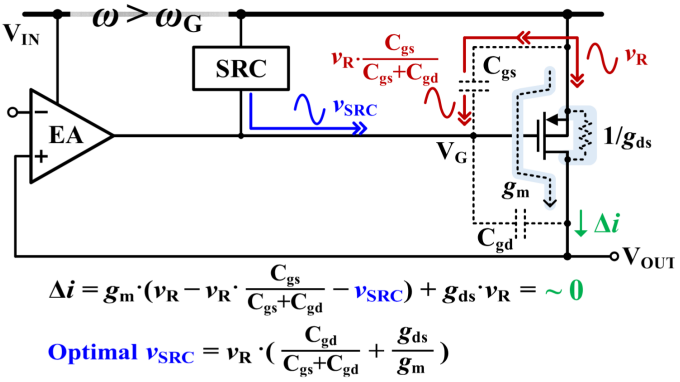


Figure 2.21: Example of an LDO employing SRC. Reprinted from [22].

Alternatively, v_{src} can be connected to the body gate of the pass transistor. This would avoid the addition of a summing circuit and would take advantage of the lower parasitic capacitance of the body gate [22] as shown in Figure 2.22.

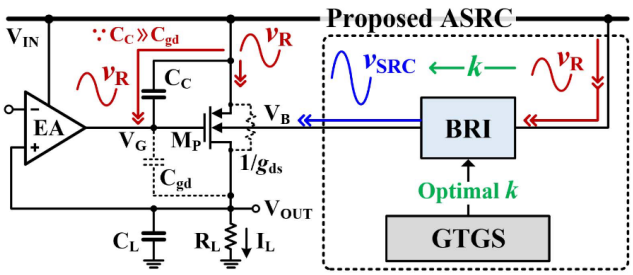


Figure 2.22: Block diagram of the proposed SRC LDO. Reprinted from [22].

The optimal value of v_{SRC} can be given by

$$v_{SRC} = v_R\left(\frac{g_m}{g_{mb}} \cdot \frac{C_{gd}}{C_C + C_{gd}} + \frac{g_{ds}}{g_{mb}} + 1\right) \tag{2.10}$$

Since $C_C \gg C_{gd}$ [22],

$$v_{SRC} \approx v_R\left(1 + \frac{g_{ds}}{g_{mb}}\right) \tag{2.11}$$

The LDO proposed in [22] makes use of a g_{ds}-to-g_{mb} sensor, represented in Figure 2.22 as GTGS, to find the ideal value of k, which corresponds to the amplification factor that will be applied to v_r in order to create v_{SRC}, as stated in equation 2.11. Additionally, it uses a Body-Ripple Injector (BRI), whose job is to amplify v_r by k and inject it into the bulk of the transistor.

2.5.6 LDO with Adaptive Compensation and Biasing

Dual loop LDO topologies can be used to obtain good results in terms of bandwidth or phase margin [23]. Such a structure is shown in Figure 2.23. The system is composed of three poles, being the third one located in high frequency. The loop NFL_M is responsible for establishing a

good DC loop gain while the loop NFL_S has a high bandwidth. The superposition of NFL_M and NFL_S forms NFL_G.

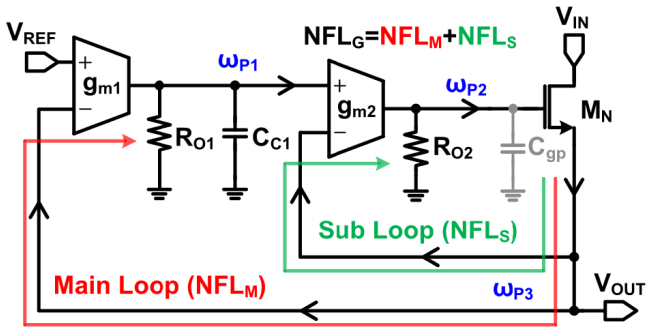


Figure 2.23: Dual-loop LDO topology. Reprinted from [23].

One issue with this topology is that C_{C1} must have a high value for ω_{p1} to become the dominant pole [23]. Another problem arises when I_{LOAD} has a small value, since ω_{p3} will move to the left and degrade the phase margin. Once again, the value of capacitors C_{C1} and C_{C2} must be large to compensate the system, reducing bandwidth and increasing area. In [23], a Wide-Range Adaptive-Gain Nested Miller Compensation (WAG-NMC) technique is used to compensate the system, as shown in Figure 2.24.

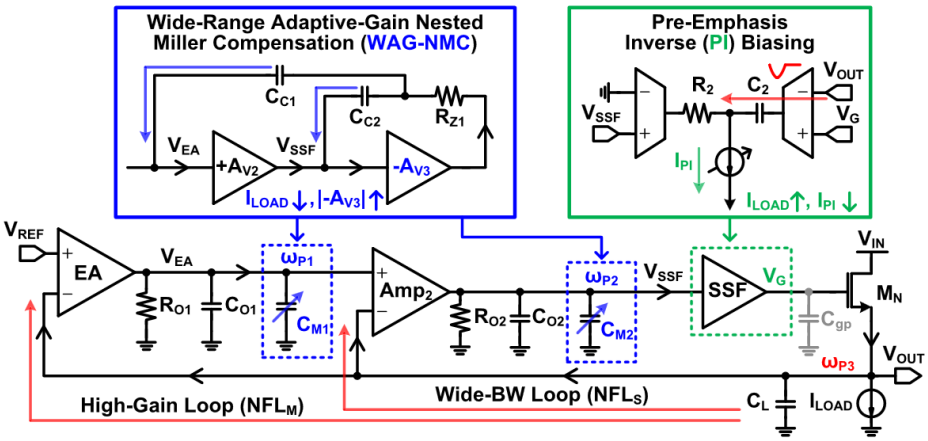


Figure 2.24: Proposed WAG-NMC LDO. Reprinted from [23].

The circuit uses a WAG-NMC [23]. Unlike conventional fixed compensation schemes, this topology dynamically adjusts the effective Miller capacitances through a variable-gain auxiliary amplifier whose gain depends on the sensed load current [23]. In this case, the values of C_{M1} and C_{M2} are adjusted based on load conditions using an amplifier A_{v3}, whose gain is inversely proportional to I_{LOAD}. This adjustment is done by applying that gain to C_{C1} and C_{C2}, taking advantage of miller effect. When I_{LOAD} decreases, A_{v3} will increase alongside C_{M1} and C_{M2}. This will cause the poles ω_{p1} and ω_{p2} to follow the movement of ω_{p3}, compensating the system effectively.

The research suggests applying a Pre-Emphasis Inverse (PI) biasing method to the Super Source Follower (SSF) that drives the NMOS pass transistor in order to further improve transient performance [23]. The inverse biasing provides higher bias current at light load and lower bias current at heavy load, which is advantageous for rapidly charging and discharging the large gate capacitance of the NMOS pass device. The pre-emphasis mechanism momentarily significantly increases the slew rate at the gate of the pass transistor.

2.5.7 LDO Suitable for Wide Current and Capacitance Ranges

Because the performance of electronic devices is constantly advancing, an increase in the values of load current is expected [24]. Because of that, efficient delivery of power to those loads is a very important prerequisite. With higher values of load current, LDOs are expected to have a higher gate capacitance in the pass device, which can slow down the transient response.

The load capacitances are also increasing, making the design of regulators a difficult challenge. The capacitorless and off-chip capacitor LDOs are two categories that are used in different environments with distinct characteristics, which means they are only suitable for specific ranges of output capacitances. In [24], an LDO suitable for a large current and wide range of output capacitance is presented and shown in Figure 2.25.

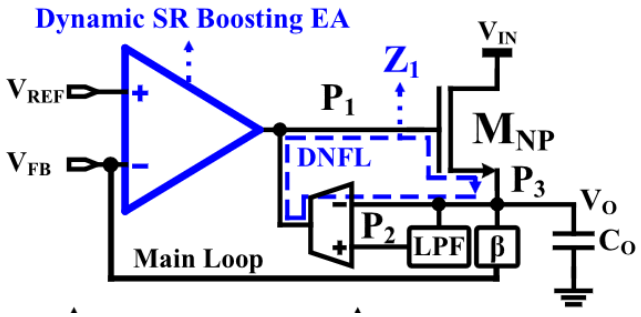


Figure 2.25: Architecture of the wide capacitance range LDO. Reprinted from [24].

It is composed by a Dynamic Negative Feedback Loop (DNFL), used to handle load transients. An additional zero is generated by the DNFL, contributing to frequency compensation. When a high frequency undershoot occurs in V_O, the low pass filter in the figure will block it, increasing the gate voltage of M_{NP}, speeding up the circuit. The dynamic Slew Rate (SR) boosting, changes the value of G_m of the EA based on load conditions, enhancing transient response.

2.5.8 Summary

It is evident from the literature covered in this chapter that there is an inherent trade-off between stability, transient responsiveness, power-supply rejection, and quiescent current when designing fully integrated, capacitor-less LDOs. Conventional architectures struggle to meet stringent specifications when the output capacitor is removed, particularly under wide load-current variations and fast load transients.

Several techniques have been proposed to mitigate these limitations. Adaptive biasing schemes improve transient response by increasing the slew rate of internal nodes during load steps, at the cost of potentially higher quiescent current. Supply-ripple cancellation techniques enhance PSRR over a wide frequency range but often require additional sensing and injection paths that increase the circuit complexity. Multi-feedback loop architectures provide an elegant way to improve bandwidth and transient response, although their analysis and compensation become increasingly complex as the number of loops increases. Table 2.1 shows a comparison between the parameters of the designs presented in this chapter.

Table 2.1: Performance Comparison of state-of-the-art LDO Regulators

	[18]	[19]	[20]	[21]	[22]	[23]	[24]
Pass transistor	PMOS	PMOS	NMOS	NMOS	PMOS	NMOS	NMOS
Technology [nm]	350	350	180	180	65	180	500
Input Voltage V_{IN} [V]	2.0–5.5	3	1.8	1.6–1.8	1.2	1.2	2.7–4.2
Output Voltage V_O [V]	1.8–3.15	2.8	1.2	1.4–1.6	1.0	1.0	2.4–4.0
Load Capacitance C_L [pF]	1×10^6	100	–	0–50	120	100	$0–10^6$
Active area [mm^2]	0.264	0.12	0.079	0.21	0.087	0.185	0.33
Quiescent Current I_Q [μA]	20	65	265	133	8–297.5	80–87	48
Current Range ΔI_L [mA]	200	0–50	0–10	31	25	299	0-2000
Undershoot ΔV_O [mV]	200	90	44	166	225	59	13–68
T_{settle} **[μs]**	–	15	0.3	0.019	1.5	0.48	1.2–1.65
T_{edge} **[ns]**	270	–	–	0.35	100	100	800
PSRR [dB] @Hz	-45@20k	-57@1k	-39@20M	–71@1k	–52@1M	–52@10k	-33@100k

Chapter 3

Proposed Architecture: Design and Implementation

3.1 System-Level Design

This section presents the high-level architecture of the system, as well as the specifications that should be met. Taking into account those specifications, the choice of each block of the circuit must be done carefully. The first design steps are also presented in this chapter.

To fulfil these specifications, it is necessary to evaluate the trade-offs between dropout voltage, power supply rejection, transient response, stability, power consumption and silicon area.

3.1.1 Design Specifications

The main parameters include the input and output voltages, PSRR, line and load regulation, and stability. In the design phase, it is also important to consider the temperature range and process variation.

The specifications presented in Table 3.1 are essential for all the design decisions. For example, maximum load current influences the sizing of the pass transistor, while the PSRR affects the design of both the error amplifier and the pass transistor.

Table 3.1: Target specifications of the proposed LDO regulator.

Specification	Design Objective
Input Voltage V_I	1.2V
Output Voltage V_O	950mV
Maximum Load Current I_L	1mA
Dropout Voltage	250mV
Operating Temperature	-40 to 125°C

3.1.2 Architecture Selection

The block diagram of the proposed LDO is represented in Figure 3.1. It consists of the following main blocks:

- Pass device
- Error amplifier
- Feedback network
- Charge pump

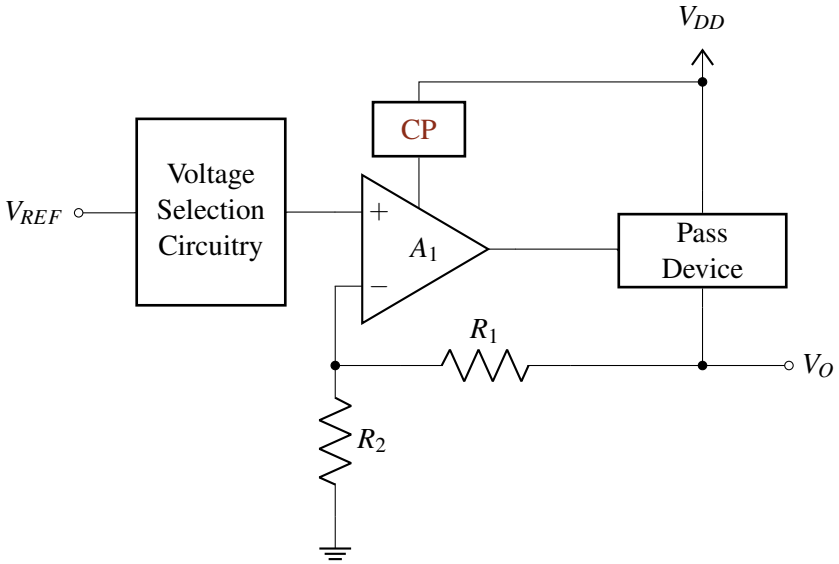


Figure 3.1: Proposed block diagram for the LDO.

The value V_{REF} consists of a reference voltage with little dependence on supply voltage or temperature. The EA (A_1) compares the reference voltage with the feedback voltage, which is a fraction of V_O. It amplifies the difference between those two signals to control the gate voltage of the pass device, thereby regulating the output voltage. The charge pump is used to allow the gate voltage of the pass device to be higher than V_{DD}. A voltage selection circuitry is used as a way to control the value of V_O using two bits, in case an output voltage lower than 0.95V is needed.

3.1.3 Pass Device Selection

The pass device can be seen as one of the most important components of the LDO because it has a direct influence on parameters like the regulator's dropout voltage, maximum load current, loop gain, stability and speed. The pass device can be implemented as an NMOS or a PMOS transistor. Each implementation has its advantages and disadvantages.

The main advantage of the PMOS implementation is that it does not need a gate voltage higher than the supply to achieve a low dropout, which decreases the complexity of the implementation, allowing a simpler control circuitry. However, the PMOS transistor would require a larger area [25] as the charge carrier mobility is lower. The gate capacitance due to the higher size can also limit the bandwidth of the system, slowing down the transient response.

On the other hand, the NMOS transistor takes advantage of the higher mobility of electrons, resulting in a lower ON resistance than a PMOS for the same size, increasing its capability to drive current. The main drawback of this topology is that the gate voltage must exceed the supply voltage for the NMOS to remain in saturation while keeping a low dropout. This can be achieved using a CP [25] as presented in Figure 3.1 with the cost of adding complexity to the circuit and, eventually, consuming more power. As the NMOS transistor acts as a source follower, the loop gain of the system will present a lower value than the one with the PMOS topology as the latter acts as a current source. Stability in this topology is easier to achieve, since the output pole is moved to higher frequencies [10].

Even though it requires the CP to boost its performance, the NMOS topology was selected for the proposed LDO as it allows a higher transconductance for a smaller device size. This property offers a better performance in terms of bandwidth and, consequently, transient response. It also shows a better PSRR value as the transconductance of the pass device in these conditions is independent of V_{DD}, reducing the noise propagation from the supply to the output. The comparison between the two topologies is summarized in Table 3.2.

Table 3.2: Comparison between PMOS and NMOS pass transistors in LDO regulators.

Characteristic	**PMOS Pass Transistor**	**NMOS Pass Transistor**
Silicon area	Larger device required	Smaller device required
Additional circuitry	Not required	Requires a charge pump for low dropout
Loop gain	Higher	Lower
Stability	Easier to achieve	Harder to achieve
Transient response	Generally slower	Generally faster
PSRR	Lower	Higher

3.1.4 Design Methodology

To design the LDO, a hierarchical methodology is used, starting by the development of each individual block before integrating it into the complete system. The analog design flow is presented in Figure 3.2. It is divided into several steps [26]:

- Design specifications: it is the first step as the specifications serve as the main reference for the rest of the design.
- Schematic design.

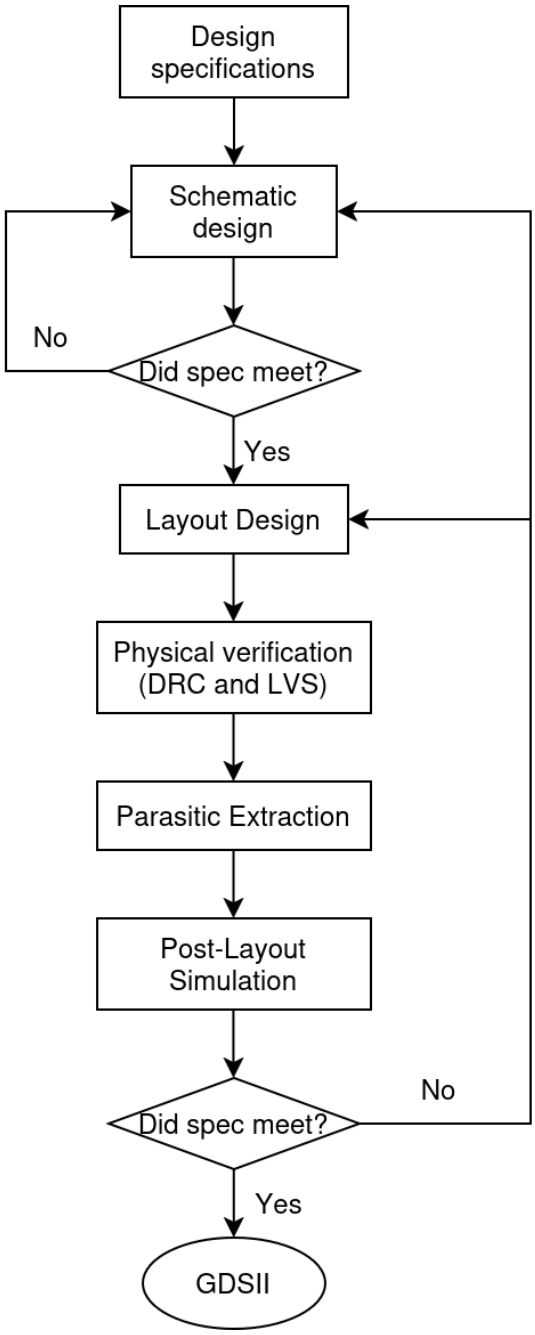


Figure 3.2: Analog IC Design Flow. Adapted from [26].

- Pre-layout simulation: used to verify the performance of the circuit before the layout phase.
- Layout design: it is the physical implementation of the schematic.
- Physical Verification: used to verify the Design Rule Check (DRC) and Layout Versus Schematic (LVS) rules.
- Parasitic Extraction: it returns the parasitic parameters of the components, giving a more realistic model of the circuit.

- Post-layout simulation: serves as the last check of the performance of the circuit with all the non idealities taken into account.

Before the schematic design phase, it is important to perform some analytical calculations to estimate some parameters of the system like the loop gain. These calculations are important as they serve as a basis for how each block inside the system should perform.

3.1.5 Initial Design Calculations

The calculations presented in this chapter serve as a reference before advancing to the design of the circuit itself. It is possible to use them to identify the expected values of certain parameters even though the implementation of the system is continuously refined through iterative simulations.

Analyzing Figure 3.1, it is possible to identify that the regulator consists on a negative feedback system. The block diagram of such a system is represented in Figure 3.3. From this, one can obtain:

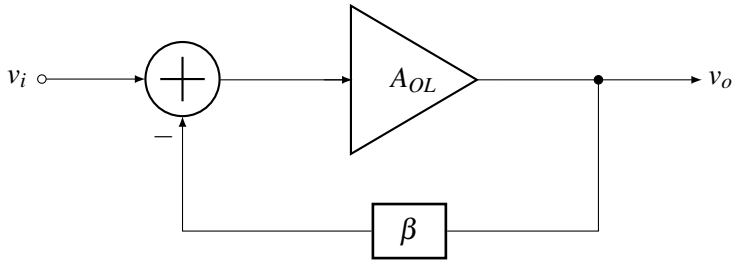


Figure 3.3: Representation of a feedback system. Adapted from [27].

$$A_{CL} = \frac{v_o}{v_i} = \frac{A_{OL}}{1 + \beta A_{OL}} \tag{3.1}$$

where the value of A_{OL} is called the open-loop gain and A_{CL} is the closed loop gain. This type of system is responsible for generating an error term comparing the input signal with a fraction of the output [27]. The main goal of this process is to minimize the error term, making the output of the β block equal to the input. By doing this, the output will become equal to the input scaled by a factor of $1/\beta$, where β is called the feedback factor. The ideal value for the closed-loop gain happens when $A_{OL} \to \infty$:

$$\frac{v_o}{v_i} \approx \frac{1}{\beta} \tag{3.2}$$

From the real and ideal values for the closed-loop gain of the system, it is possible to compute its error. The idea is to calculate the needed open-loop gain for a certain error value:

$$A_{CL}^{error} = \frac{A_{CL}^{ideal} - A_{CL}^{real}}{A_{CL}^{ideal}} \tag{3.3}$$

$$A_{CL}^{error} = \frac{\frac{1}{\beta} - \frac{A_{OL}}{1+\beta A_{OL}}}{\frac{1}{\beta}} \tag{3.4}$$

$$A_{CL}^{error} = \frac{1}{1+\beta A_{OL}} \tag{3.5}$$

From Figure 3.1, it is possible to observe that

$$\beta = \frac{R_2}{R_1 + R_2} \tag{3.6}$$

where $R_1 = R_2$, which means that $\beta = \frac{1}{2}$. Based on these expressions, to calculate the required loop gain for a given error:

$$A_{OL} = \frac{1 - A_{CL}^{error}}{\beta A_{CL}^{error}} \tag{3.7}$$

Which means that to have a error of 1% in the closed-loop gain, an open-loop gain of 198 is needed. The next step is to define the value of the feedback resistors. Having $R_1 = R_2 = 10\text{k}\Omega$ gives a good balance between area and power consumption. To calculate the values for V_O and the current through the feedback resistors I_{FB}:

$$V_O = V_{REF}(1 + \frac{R_1}{R_2}) \tag{3.8}$$

$$I_{FB} = \frac{V_O}{R_1 + R_2} \tag{3.9}$$

Knowing that $V_{REF} = 0.475\text{V}$, the value of V_O will be equal to 0.95V and I_{FB} wil be equal to $47.5\mu\text{A}$.

3.1.6 Stability Strategy

Because the regulator operates as a closed-loop system, the design of the feedback loop must be done carefully to ensure stability. The location of poles and zeros directly affects the frequency response, making stability analysis an important step during the design. Figure 3.4 shows the schematic of the proposed LDO alongside the location of its poles.

Regarding ω_{p1}, it is possible to observe that

$$\omega_{p1} = \frac{1}{C_{GPASS} R_{oEA}} \tag{3.10}$$

where C_{GPASS} is the capacitance seen from the gate of the NMOS pass transistor (and the output of the EA) to ground and R_{oA} is the output resistance of the error amplifier. Since this is the dominant pole, a compensation capacitor must be place in this node to reinforce the capacitance and move this pole to the left.

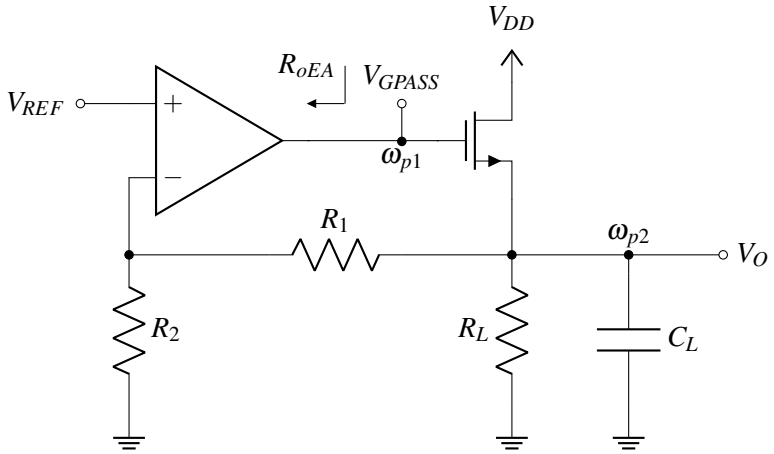


Figure 3.4: Schematic of the LDO with its poles.

As the pole ω_{p2} is located at the source of the NMOS transistor, its approximate equivalent resistance is $\frac{1}{g_{mpass}}$, so

$$\omega_{p2} \approx \frac{1}{\frac{1}{g_{mpass}} C_L} \tag{3.11}$$

The effect of these poles in the frequency response can be represented using a bode plot as shown in Figure 3.5.

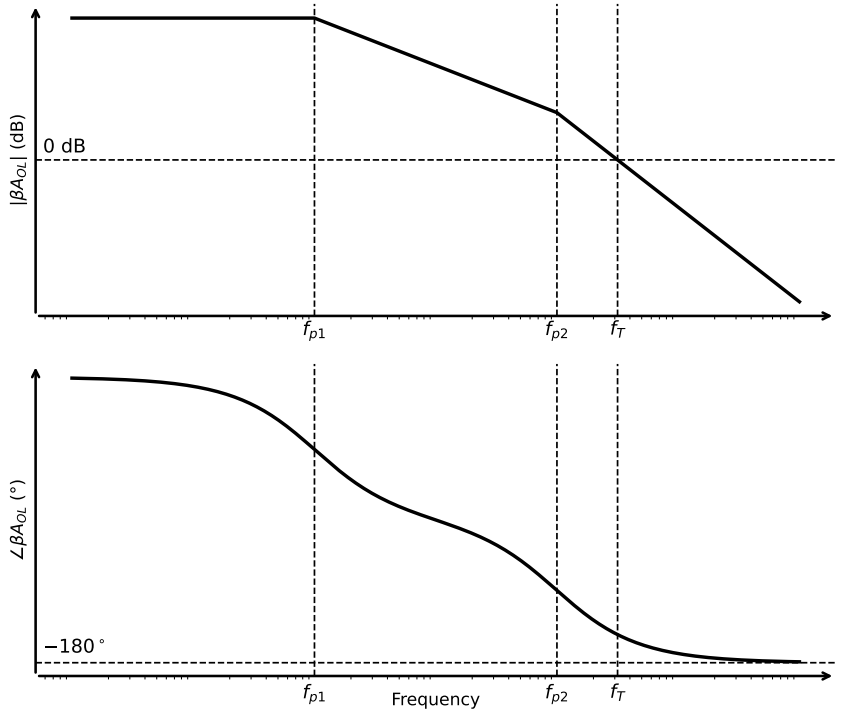


Figure 3.5: Loop gain of the system represented in a bode plot.

In Figure 3.5, it is shown the shape of the system's loop gain, which is given by βA_{OL}. Is is

possible to note that from equation 3.1 if $|\beta A_{OL}| = 1$ and $\angle \beta A_{OL} = 180°$, the value of the closed loop gain tends to infinity and the circuit starts oscillating [28]. The bode plot suggests that if the poles are close to each other, the phase margin of the system becomes degraded, which can lead to instability. Since the output pole ω_{p2} is defined by load conditions, the strategy to compensate the system consists in moving the pole ω_{p1} to the left, keeping a safe distance between the poles. It is important to note that the position of the output pole depends on the value of g_{mpass}, which depends on the value of the output current. A lighter load can cause stability problems since ω_{p2} will be closer to ω_{p1}. The EA also contains other internal poles and even though they also can lead to instability, ω_{p1} and ω_{p2} are the most important ones.

3.1.7 Design Trade-offs

To design an LDO, it is important to take into account the trade-offs between performance, power consumption and area. The trade-offs are summarized in Table 3.3.

The most evident trade-off appears when it is necessary to carry a large load current for a low dropout voltage. In order to achieve this, a pass transistor of great W/L is needed [10]. However, this will increase the gate capacitance of the device, which will penalize the bandwidth and transient response of the system.

As explained in the previous section, balancing bandwidth and stability is also a concern. To increase the system's phase margin, the dominant pole needs be moved to the left, decreasing the bandwitdth and slowing down the transient response.

There is also a trade-off between power consumption and bandwidth. As the quiescent current reduces, power consumption reduces as well. However, lower bias currents limit the loop bandwidth, degrading the regulator's response to sudden load variations.

Table 3.3: Main design trade-offs considered during the development of the proposed LDO regulator.

Design Objective	**Associated Trade-off**
Low dropout voltage	Larger pass transistor area, lower transient response
Low power consumption	Lower loop bandwidth, slower transient response
Fast transient response	Increased quiescent current and reduced phase margin
High loop stability	Reduced bandwidth and slower transient response

3.2 Circuit Design

This section presents the transistor-level implementation of the LDO. Each block is presented individually, including its principle and design considerations.

3.2.1 Pass Device

3.2.1.1 Operating Principle

The pass device represents the output stage of the regulator. For small-signal, it acts as a source follower and is controlled by the EA in order to keep the output voltage constant and independent of variations in the supply voltage. This stage is represented in Figure 3.6.

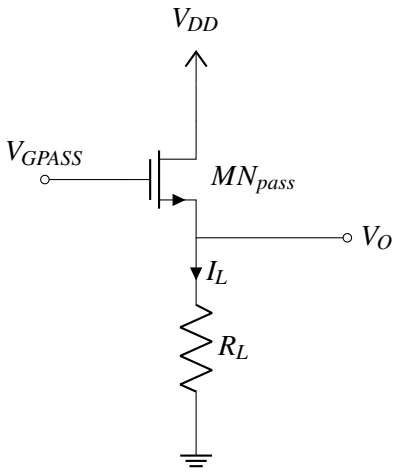


Figure 3.6: Representation of the LDO's output stage.

As discussed in chapter 3, the NMOS pass device topology was chosen due to the higher carrier mobility leading to a smaller device area and lower output impedance, which facilitates compensation without the use of a large external output capacitor.

It is interesting to study the effect of the output stage in the loop gain of the system. To compute the open-loop gain, the model presented in Figure 3.7 is applied:

$$A_{OL} = \frac{v_o}{v_i} = \frac{g_{mpass}(r_{opass} \parallel R_L \parallel (R_1 + R_2))}{1 + g_{mpass}(r_{opass} \parallel R_L \parallel (R_1 + R_2))} A_1 \tag{3.12}$$

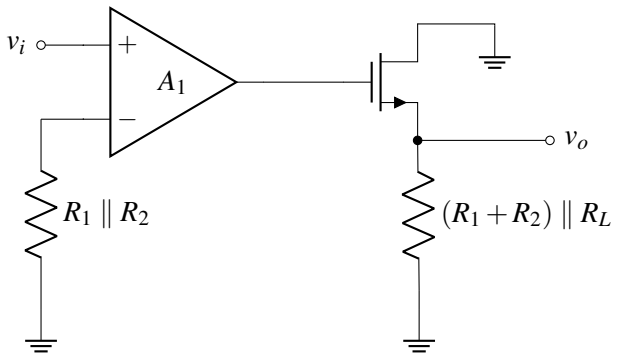


Figure 3.7: Model to compute the open-loop gain.

Equation 3.12 reveals that the loop gain is strongly related to both I_L and V_{DS}. When the supply voltage V_{DD} decreases, the transistor tends to leave the saturation region, causing a drop in

the values of g_{mpass} and r_{opass}, which will degrade the open-loop gain. The open-loop gain also drops by increasing I_L because even though the value of g_{mpass} increases, the product $g_{mpass}r_{opass}$ given by

$$g_{mpass}r_{opass} = \frac{\sqrt{2\mu_n C_{ox}\frac{W}{L}}}{\lambda}\frac{1}{\sqrt{I_L}} \tag{3.13}$$

decrases with I_L.

3.2.1.2 Design Considerations

It is clear from the previous section of this chapter that to design the pass transistor, several variables need to be taken into account. The transistor needs to be big enough to drive a large load current but its gate capacitance should not degrade the transient response of the system.

The device must satisfy the expression $V_{DS} \geq (V_{GS} - V_{THn})$ for the entire range of load current in order to remain in saturation. This suggests that a device with a big W/L ratio is needed to have a low dropout while minimizing the overdrive voltage. This means that the minimum achievable dropout is actually the device's overdrive voltage given by

$$V_{DO} \geq \sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L}}} \tag{3.14}$$

Another important second-order effect to be considered in this design is the body effect. That property shows a directly proportional relation between V_{SB} and V_{TH} given by [16]

$$V_{TH} = V_{TH0} + \gamma(\sqrt{2\Phi_F + V_{SB}} - \sqrt{|2\Phi_F|}) \tag{3.15}$$

where γ is the body-effect coefficient. This increase in the threshold voltage will degrade the gain of the EA A_1. This effect is mainly observed in some Process, Voltage and Temperature (PVT) simulations and will be explained later. The body effect will also cause a drop in the gain of the output stage, affecting the open-loop gain of the entire system because

$$A_{OL} = \frac{v_o}{v_i} = \frac{g_{mpass}(r_{opass} \parallel R_L \parallel (R_1 + R_2))}{1 + (g_{mpass} + g_{mbpass})(r_{opass} \parallel R_L \parallel (R_1 + R_2))}A_1 \tag{3.16}$$

where g_{mbpass} represents the dependance of the drain current in V_{BS}. Hence, instead of connecting the bulk of the transistor to ground, it is reasonable to connect it directly to the source. As this is an NMOS transistor, a triple-well design process is needed.

To avoid a large drop in the value of r_{opass}, a minimum-length device is not used in order to mitigate the effect of channel-length modulation.

The dimensions of the pass device were obtained through an iterative simulation in order to balance the trade-offs between current-driving capability, dropout voltage, gate capacitance and silicon area. It has a width of $600W_{min}$ and a length of $2L_{min}$.

3.2.2 Error Amplifier

3.2.2.1 Operating Principle

The error amplifier serves as the control element of the feedback loop by comparing the reference voltage V_{REF} with the feedback voltage V_{FB} that corresponds to the inverting input of the EA:

- If $V_{FB} < V_{REF}$, the value of V_{GPASS} will increase alongside with V_O.
- If $V_{FB} > V_{REF}$, the value of V_{GPASS} will decrease alongside with V_O.

The negative feedback will balance the two voltages making $V_{FB} \approx V_{REF}$.

The performance of this block is of extreme importance, as it affects several parameters:

- The gain A_1 of the device is strongly related with parameters like loop-gain and PSRR as well as the error of the closed-loop gain.
- Its BW is another important property because it affects transient response and the range of frequencies of supply rejection.
- It contains some internal poles which need to be taken into account while compensating the system.

Once again, it is important to find a trade-off between all of these parameters to achieve a satisfactory performance.

3.2.2.2 Topology Implementation

To maximize the performance of the circuit, the topology of the EA must be chosen carefully. To begin with, it seems intuitive to start with the simplest one, which is the one-stage Operational Transconductance Amplifier (OTA) shown in Figure 3.8.

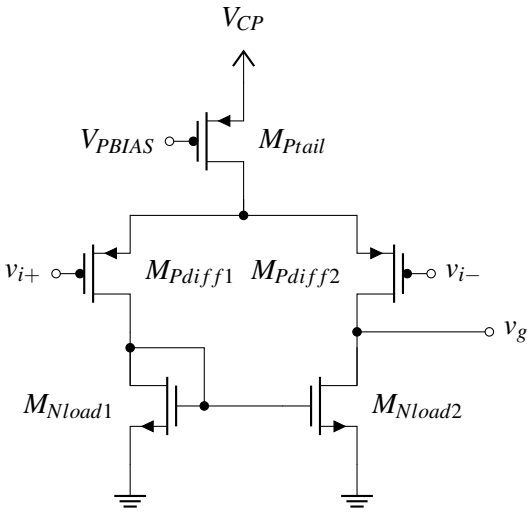


Figure 3.8: Schematic of the One-Stage OTA

The first choice to make consists on deciding between NMOS or PMOS input differetial pair. The main difference between the two is their Input Common Mode Range (ICMR). For the PMOS, as the common mode voltage at the input $V_{I,CM}$ incrases, device M_{Ptail} tends to leave the saturation region. However, if $V_{I,CM}$ deacreases, the differential pair transistors are at risk of going into triode region. The ICMR for the circuit in Figure 3.8 can be given by:

$$ICMR_{min} = V_{GSload} - |V_{THp}| \tag{3.17}$$

$$ICMR_{max} = V_{CP} - V_{SGtail} + |V_{THp}| - V_{SGdiff} \tag{3.18}$$

The value of $V_{I,CM}$, in practice, corresponds to the value of V_{REF}, which is closer to V_{SS} than to V_{CP} ($V_{REF} < 0.5$V). The $ICMR_{min}$ for an OTA with PMOS differential pair is significantly lower than its NMOS counterpart. That is the reason why the PMOS input pair topology is proposed for this work. This topology also performs better in terms of flicker noise.

Even though it is simple, the topology depicted in Figure 3.8 suffers from a great limitation. Its small-signal gain is approximately $g_{mdiff1,2}(r_{odiff1,2} \parallel r_{oload1,2})$, which in the majority of the cases is lower than 10 [29]. This amount of gain is far from sufficient to set the difference between V_{FB} and V_{REF} to 0.

To overcome that barrier, one or more gain stages can be added to boost the gain. However, that solution is not convenient because each gain stage comes with a cost of at least one additional pole [29], which would slow down the circuit (degrading the load transient response) and make the task of compensating the circuit even harder.

Instead of adding more gain stages, a better choice is to use a cascode topology. The first one to be considered is the telescopic cascode shown in Figure 3.9.

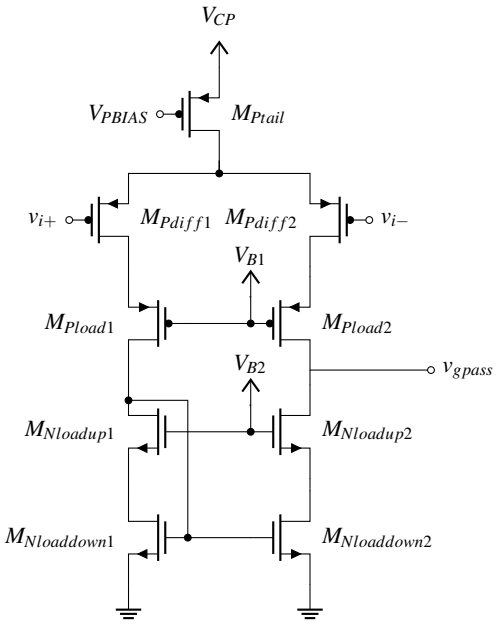


Figure 3.9: Schematic of the telescopic cascode.

Analyzing the circuit, it is possible to conclude that it has a small-signal gain of

$$A_v \approx g_{mPdiff1,2}[(g_{mPload1,2} r_{oPload1,2} r_{oPdiff1,2}) \parallel (g_{mNloadup1,2} r_{oNloadup1,2} r_{oNloaddown1,2})] \quad (3.19)$$

By increasing the output resistance (using cascode devices), the gain is boosted significantly as stated in equation 3.19. Unfortunately, the addition of the cascode devices introduces poles to the system and decreases the output swing [29].

In fact, the output swing is one of the main drawbacks of this topology due to the fact that it is hard to keep every transistor in saturation. The maximum value of V_O can be given by

$$V_{GPASS} \leq V_{CP} - |V_{ODPtail}| - |V_{ODPdiff1,2}| - |V_{ODPload1,2}| \quad (3.20)$$

This equation reveals that the maximum value for V_{GPASS} is severely limited, specially because it includes the overdrive voltage of the M_{Ptail} transistor. Because the input common mode voltage of the amplifier has a low value, the drain voltage of M_{Ptail} will also have a low magnitude because $V_{DPtail} = V_{ICM} + V_{SGPdiff1,2}$. This means that for M_{Ptail} to remain in saturation, the value of $V_{SGPdiff1,2}$ needs to be small, which means that $V_{SDPtail}$ will be relatively large, limiting the maximum value of V_{GPASS}. This limitation makes this topology inappropriate for this application, since V_{GPASS} needs to have a value greater than V_{DD}.

To solve the issue with the range of the output voltage, another cascode topology can be employed, which is the folded cascode shown in Figure 3.10.

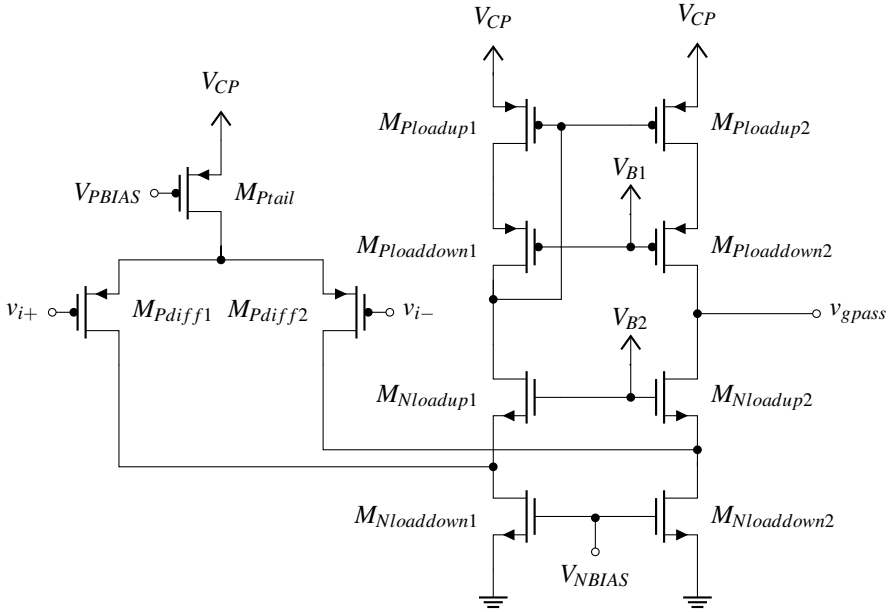


Figure 3.10: Schematic of the folded cascode amplifier.

In this architecture, the cascode devices are of the opposite type of the ones in the input. The approximate value for the gain of this topology is

$$A_v \approx g_{mPdiff1}\{[g_{mPdown1} r_{oPdown1} r_{oNup1}] \parallel [g_{mNup1} r_{oNup1} (r_{oNdown1} \parallel r_{oPdiff1})]\} \tag{3.21}$$

One disadvantage of this topology comparing to its telescopic counterpart is the lower output resistance because of the parallel between r_{odown1} and r_{odiff1} [29]. This will result in a lower small signal gain. The maximum output voltage of this topology can be given by

$$V_{GPASS} \leq V_{CP} - |V_{ODPloadup2}| - |V_{ODPloaddown2}| \tag{3.22}$$

Equation 3.22 reveals that the maximum voltage at the output is higher for the folded cascode relatively to the telescopic topology because it does not include the overdrive voltage of the tail current source. It is important to note that in a telescopic cascode, only one current source is needed to bias both the differential pair and the cascode devices. In the folded cascode, two current sources are needed: one for the differential pair and the other for the cascode and load transistors. This leads to a higher power consumption in the folded-cascode [29]. The poles at the sources of $M_{Nloadup1,2}$ are also more relevant than the ones in the sources of the cascode devices in the telescopic topology. This is because these nodes have a greater capacitance as they have more devices associated.

The folded-cascode topology seems to be the most suitable for this specific application as it is able to keep a reasonable gain and speed while having a good output swing.

3.2.2.3 Design Considerations

Starting with the differential pair $M_{Pdiff1,2}$, these devices will dictate GBW product of the amplifier. That value is given by

$$GBW = \frac{g_{mdiff1,2}}{2\pi C_{GPASS}} \tag{3.23}$$

where C_{GPASS} is the value of the capacitance between the gate of the pass transistor and ground. This expression points to the fact that to achieve a high GBW, a higher value of g_m is needed in the input pair devices, meaning that the bias current allocated to them should be relatively high. To increase the value of g_m even more, a good approach is to minimize the V_{OD} of the devices due to the fact that $g_m = \frac{2I_D}{V_{OD}}$. A drain current of 50μA was allocated for the input pair to balance the trade-off between speed and power consumption by the OTA, with a $\frac{g_m}{I_d}$ of approximately $15V^{-1}$. To minimize the V_{OD} of the devices, their size was increased accordingly. Due to the difficulties to have a high gain with minimum length, the length of the differential pair was set to $3L_{min}$.

The cascode devices $M_{Ploaddown1,2}$ and $M_{Nloadup1,2}$ are among the ones that contribute the most for the EA gain. The product $g_m r_o$ of a device can be given by

$$g_m r_o = \frac{2}{\lambda V_{OD}} \tag{3.24}$$

Equation 3.24 reveals that to maximize the product $g_m r_o$ of the device, V_{OD} must be minimized. Unfortunately, this solution comes with a trade-off. Since the minimization of V_{OD} implies larger devices, the bandwidth of the amplifier will be degraded due to a higher value of parasitic capacitances in that node. To achieve a balance between gain and bandwidth, the overdrive was minimized but minimum length was used for these devices. The same reasoning was applied to the devices $M_{Nloadup1,2}$. The minimization of $|V_{ODPloaddown2}|$ is also important to allow a higher maximum voltage, as stated in equation 3.22. A current of 10μA was allocated to that branch of the circuit.

The device $M_{Ploaddown2}$ can be severely affected by the performance of the pass transistor. The overdrive voltage of M_{Nout} needs to be minimized because its gate is connected directly to the drain of $M_{Ploaddown2}$. If V_{ODNout} is too high, $M_{Ploaddown2}$ is at risk of entering in triode region and degrade the gain of the EA. This is also the reason why the bulk of M_{Nout} is connected to a higher voltage than ground, reducing its V_{TH} due to the body effect.

For the devices $M_{Ploadup1,2}$, the overdrive voltages were also minimized in order to have a higher voltage at the pass transistor's gate. It is important to note that if the source voltages of $M_{Ploaddown1,2}$ need to be as high as possible to keep the devices on the top in saturation. This constitutes another reason why their V_{OD} must be minimized. In general, for this design, as the gate voltage of the pass transistor is above 1.2V and the charge pump supplies the OTA with 1.9V, the PMOS transistors have a lower margin to remain in saturation.

Devices $M_{Nloaddown1,2}$ are current mirrors. Their V_{OD} should be maximized in order to avoid mismatch in the threshold voltages and, consequently, in the current copied from other devices. To reduce the effect of channel-length modulation while minimizing those mismatches, these devices also have a length of $3L_{min}$. The sizes of the devices are presented in Table 3.4.

Table 3.4: Sizes of the EA devices.

Device	Width (W)	Length (L)	Type
M_{Ptail}	$80W_{min}$	$3L_{min}$	Thick-oxide
$M_{Pdiff1,2}$	$70W_{min}$	$3L_{min}$	Thin-oxide
$M_{Ploadup1,2}$	$48W_{min}$	$3L_{min}$	Thick-oxide
$M_{Ploaddown1,2}$	$44W_{min}$	L_{min}	Thick-oxide
$M_{Nloadup1,2}$	$10W_{min}$	L_{min}	Thick-oxide
$M_{Nloadown1,2}$	$12W_{min}$	$3L_{min}$	Thick-oxide

3.2.3 Biasing Circuits

The operating point of the folded cacscode OTA plays a very important role in its performance. Therefore, a well designed biasing network is essential to provide stable currents and gate voltages to the cascode devices of the OTA. This will ensure that all the transistors remain in saturation for the entire range of operation. The biasing circuitry is shown in Figure 3.11.

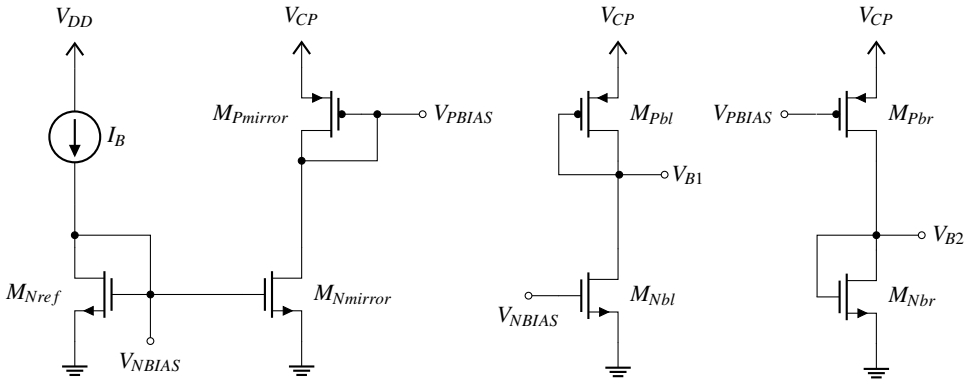


Figure 3.11: Biasing circuitry.

The circuit is composed by a "global" current mirror that generates the voltages at the nodes V_{NBIAS} and V_{PBIAS}. The refernce I_B serves as the master current for the error amplifier. This reference is replicated by current mirrors to bias the devices. The value chosen for I_B was 10μA.

The generation of V_{B1} is done by a device acting as a current source (M_{Nbl}) in series with a diode-connected transistor, whose drain is connected to the gate of the PMOS cascode devices. The value of V_{B1} must be adapted in order to keep both $M_{Ploaddown1,2}$ and $M_{Ploadup1,2}$ in saturation. The same reasoning is applied to V_{B2}, even though the design of this voltage must be even more carefull because of the risk of an eventual transition of the differential pair transistors to triode region. The sizes if the devices are shown in Table 3.5.

Table 3.5: Sizes of the devices of the bias network.

Device	Width (W)	Length (L)	Type
M_{Nref}	$2W_{min}$	$3L_{min}$	Thick-oxide
$M_{Nmirror}$	$2W_{min}$	$3L_{min}$	Thick-oxide
$M_{Pmirror}$	$8W_{min}$	$3L_{min}$	Thick-oxide
M_{Pbl}	$32W_{min}$	$3L_{min}$	Thick-oxide
M_{Nbl}	$2W_{min}$	$3L_{min}$	Thick-oxide
M_{Nbr}	$12W_{min}$	$3L_{min}$	Thick-oxide
M_{Pbr}	$48W_{min}$	$3L_{min}$	Thick-oxide

3.2.4 Output Voltage Selection

To provide flexibility in the regulated output voltage, a digitally controlled output voltage selection mechanism was implemented. This is interesting because in systems such as the RCD it is useful to use the same LDO topology to generate different voltages. The output voltage is selected through a two-bit digital control signal, denoted as $vout_{ctrl} < 1:0 >$. This allows four different control states and, consequently, four programmable output voltage levels. Based on the combination of these two bits, a set of signals SEL_n are generated using the architecture presented in Figure 3.12.

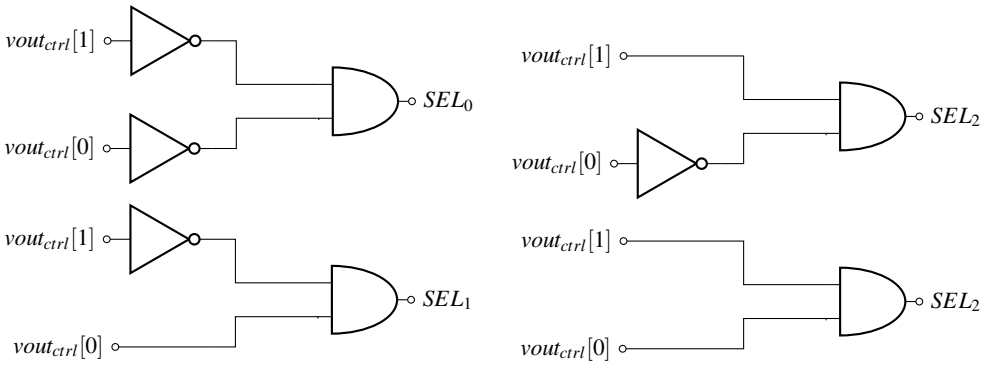


Figure 3.12: Generation of SEL_n signals.

The first approach consists on using the topology presented in Figure 3.13. The output voltage is determined by the feedback network of the LDO. By changing the feedback ratio according to the applied code $vout_{ctrl} < 1:0 >$, the output voltage can be modified. For instance, if $vout_{ctrl}[1] = 0$ and $vout_{ctrl}[0] = 0$, $SEL_0 = 1$ and $V_O = (1 + \frac{R_1}{R_{2S0}})V_{REF}$.

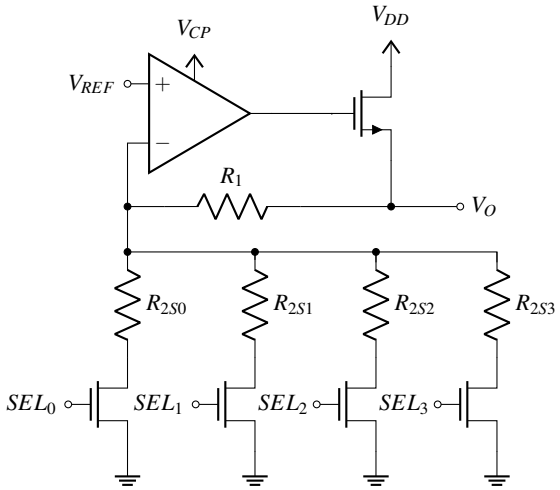


Figure 3.13: Output voltage selection implemented by modifying the feedback factor β.

The main drawback of this approach was the fact that the noise from the supply would be inserted directly into the feedback loop. Because of that, the value of PSRR for low frequency was dropping to approximately -44dB. The red line in Figure 3.14 represents the PSRR for this topology.

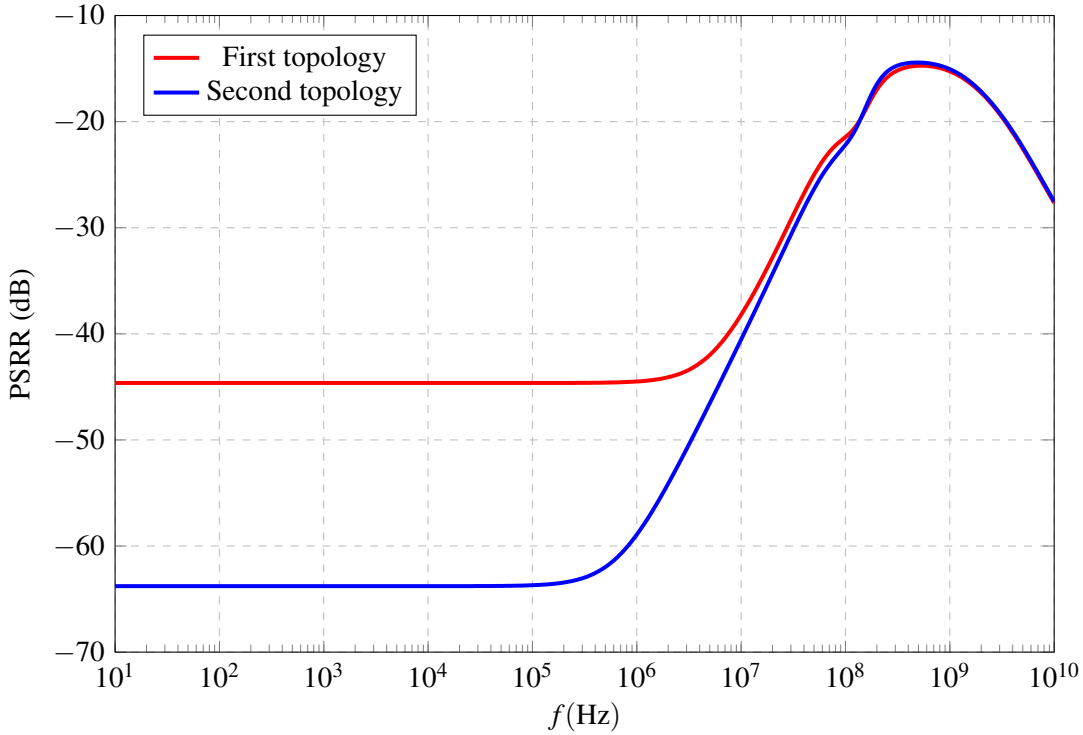


Figure 3.14: Comparison of the PSRR for the two architectures.

Figure 3.15 shows another topology that can solve the problem of PSRR degradation. Instead of varying the feedback factor β, a string of resistors creates a voltage divider of V_{REF}.

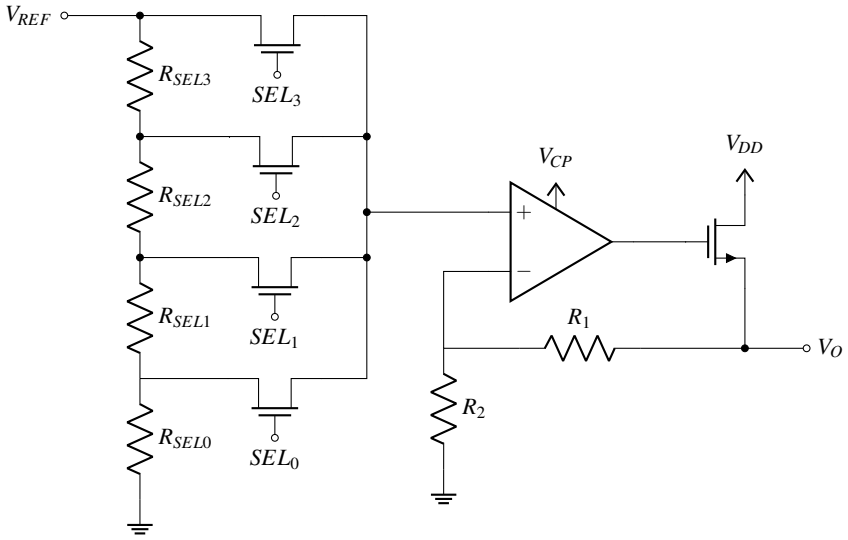


Figure 3.15: Output voltage selection using a resistive divider in V_{REF}.

This topology avoids the injection of noise directly into the feedback loop, enhancing the value of the low frequency PSRR significantly as the blue line in Figure 3.14 demonstrates. The size of the NMOS switches must be increased accordingly to keep them in deep triode region and

minimize their ON resistance. A current of $20\mu A$ was used in the resistor string to balance power consumption and area. The output voltage can be adjusted in steps of 500mV from 800mV to 950mV.

3.2.5 Charge Pump

The propoosed LDO uses an NMOS pass transistor to drive the load current, with this stage behaving as a source follower. Contrary to the case of a PMOS transistor, the NMOS requires its gate voltage to exceed the supply, in order to have a low dropout. To satisfy this requirement, the use of the charge pump is essential as it will generate a boosted voltage from V_{DD} to supply the error amplifier and allow a higher voltage at the gate of MN_{out}.

3.2.5.1 Operating Principle

A basic charge pump circuit is presented in Figure 3.16 [30]. This conceptual topology consists on a flying capacitor C_f, an output capacitor C_{CP} and four ideal switches controlled by two clock signals ϕ_1 and ϕ_2.

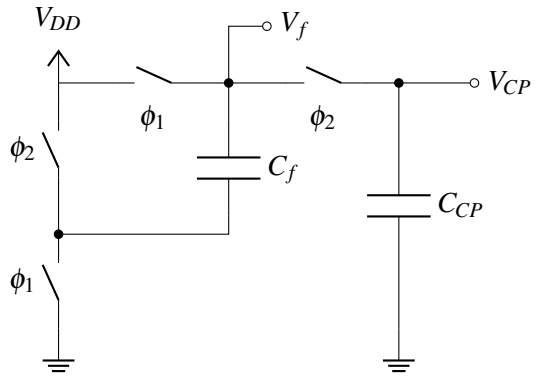


Figure 3.16: Voltage doubler charge pump [30].

When $\phi_1 = 1$ and $\phi_2 = 0$ capacitor C_f is charged with V_{DD}, making $V_f = V_{DD}$ and V_{CP} is disconnected from the circuit. This is called the refresh phase [30]. In the next clock phase, when $\phi_1 = 0$ and $\phi_2 = 1$, C_f, which is still charged with V_{DD} will be connected between the supply and V_{CP}, making $V_{CP} = 2V_{DD}$. This is called carge redistribution phase The output capacitor C_{CP} is responsible to maintain the value of V_{CP} even when the circuit returns to the refresh phase.

When the charge pump begins its operation at the instant $t = 0$, it takes a certain amount of time to reach its final value, mainly because in the beginning all the capacitors are discharged. Before the settling of V_{CP}, the waveform shows a step-wise ramp up, with the steps getting smaller as V_{CP} reaches the final value [30]. The value at the output in the n-th clock cycle can be given by

$$V_{CP,n} = \frac{2V_{DD}C_f + V_{Cf,n-1}C_{CP}}{C_f + C_{CP}} \tag{3.25}$$

A problem that can arise in the design of this type of circuit is that it cannot reach the final value of $2V_{DD}$ in the presence of load current. The charge in V_{CP} is equal to the charge consumed by the load [30]:

$$\Delta Q_{CP} = \Delta Q_{load} \tag{3.26}$$

This will cause that the final value of V_{CP} is equal to

$$V_{CP} = 2V_{DD} - \frac{I_{EA}}{f_{SW} C_f} \tag{3.27}$$

where I_{EA} is the current drawn by the error amplifier and f_{SW} is the frequency of the clock signals. Equation 3.27 suggests that to get a voltage as close as possible to $2V_{DD}$, the values of C_f and f_{SW} should be maximized.

Another important aspect that must be taken into account is the value of the ripple at the charge pump output. It is essential to analyze this issue because if the ripple has a high value it can be propagated to the output of the LDO, even though the error amplifier is able to filter the majority of it. The ripple at the charge pump output $V_{ripple,CP}$ can be given by [30]

$$V_{ripple,CP} = \frac{I_{EA}}{f_{SW} C_{CP}} \tag{3.28}$$

The equation suggests that the ripple for a certain amount of current can be minimized by maximizing f_{SW} and C_{CP}.

3.2.5.2 Topology Implementation

An implementation of the Dickson charge pump is presented in Figure 3.17. It works as follows: When $\phi_1 = 1$ (and $\overline{\phi_1} = 0$), transistors MP_1 and MN_1 are closed while MP_2 is open, charging the flying capacitor C_f with V_{DD}. Since MN_2 is a diode connected transistor, it will also be opened because, in steady-state, the value of V_{CP} is higher than V_{DD}, which is the value of the drain voltage of that device. When $\phi_1 = 0$, MP_2 will close, and C_f, which is already charged with V_{DD}, will have one of its terminals connected to the supply and the other connected to the drain of MN_2. Because of this, the voltage at the drain of MN_2 will be $2V_{DD}$, closing the transistor and making a connection to the output V_{CP}.

Even though it is simple and easy to understand, this topology has a strong drawback. When device MN_2 is closed, it has a minimum V_{DS} that is equal to its threshold voltage V_{TH}. This implies that the value of V_{CP} is way below $2V_{DD}$. Even though the charge pump only needs to supply 1.9V to the EA, this voltage drop is still to high, as it will be difficult to give enough margin for worst-case corners. This issue could be solved by cascading two or more pumping stages, but that solution would come with the cost of more power consumption and lower efficiency as well as a higher ripple.

A possible solution to this problem is to use a cross-coupled voltage doubler, shown in Figure 3.18 [31]. When $\phi_1 = 1$ and $\phi_2 = 0$, C_{f1} will be charged with V_{DD}, because M_{Nd1} will connect

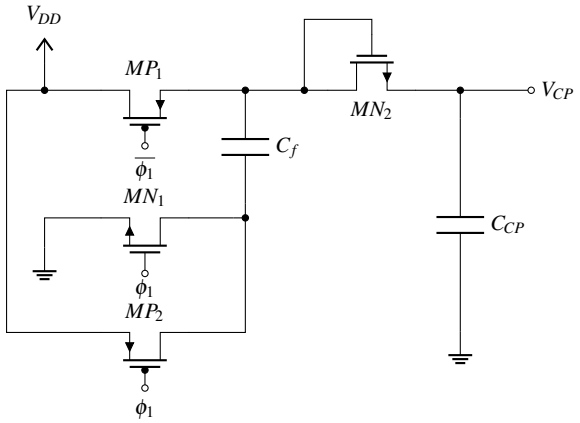


Figure 3.17: Possible implementation of a dickson charge pump.

the bottom plate of C_{f1} to ground and M_{Nu1} will connect the top plate to V_{DD}. Here it is assumed that both V_{f2} and V_{CP} are equal to $2V_{DD}$ from the previous phase, which means that M_{Pd1} is disconnected from V_{CP}. When $\phi_1 = 0$ and $\phi_2 = 1$, device M_{Pu1} will connect the bottom plate of C_{f1} to V_{DD} and M_{Pd1} will connect its top plate to V_{CP}, making $V_{CP} = 2V_{DD}$. The same reasoning can be applied to the other side of the circuit. This topology is useful to minimize the deviation of V_{CP} from $2V_{DD}$, as the voltage drop here is dependent only on the value of $C_{f1,2}$ and the ON and OFF resistances of the active devices.

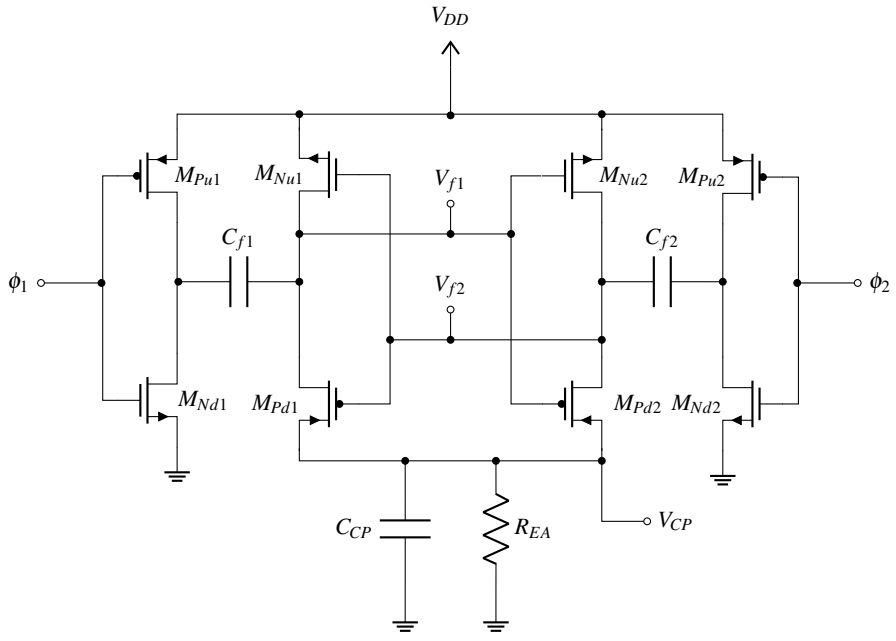


Figure 3.18: Cross-coupled voltage doubler.

3.2.5.3 Design Considerations

The design of the charge pump needs to take into consideration the balancing of a several trade-offs. Output voltage and ripple, power consumption, and silicon area are the main variables that should be balanced in order to achieve satisfactory results. The objective is to have a V_{CP} of approximately 1.9V, a value high enough to allow a relatively high voltage at the pass device's gate without moving the transistors of the EA out of saturation. The value of V_{CP} cannot be much higher to avoid increasing power consumption.

To have an output voltage V_{CP} as close as possible to $2V_{DD}$, the value of C_f must be as high as possible, as presented in equation 3.27. However, increasing the capacitance means increasing silicon area, so the capacitor must only be high enough to provide 1.9V. The size of the transistors also play an important role in this performance metric. Their size must be increased accordingly to minimize their ON resistance, avoiding voltage drops.

The output ripple can be minimized by maximizing the value of C_{CP}. For the same constraint on area stated before, its size must also be limited. Another issue that may arise with the increase of C_{CP}, is that the circuit takes more time to settle in its final value.

The clock frequency f_{SW} must be increased to increase V_{CP} and minimize $V_{ripple,CP}$. However, a large frequency value leads to a higher power consumption and reduces the regulator's efficiency.

The values for the different variables are summarized in Table 3.6. The NMOS devices have a width of $30W_{min}$ and the PMOS devices have a width of $80W_{min}$. All the transistors have a length equal to L_{min}.

Table 3.6: Parameters and values for the charge pump.

Parameter	Value
$C_{f1,2}$	350fF
C_{CP}	1pF
f_{SW}	1GHz

3.3 Layout

The layout of the proposed LDO was developed using a hierarchical design methodology, in which each block is implemented and verified before being integrated in the complete system. This approach is useful as it allows to evaluate every single block and, in case the performance drops, detect what is causing the failure in an earlier phase.

Several analog layout techniques, introduced in chapter 2, are used to improve matching and reduce sensitivity to fabrication variations. Dummy transistors are included around critical devices to minimize Well-Proximity Effects (WPE), and guard rings were used to bias the substrate and wells while eliminating the risk of latch-up. Dummies were also used to improve matching in some cases.

It was used a 55nm planar technology. To get better results in terms of area, a lower technology node could have been used. Due to timing constraints, the layout of the CP and the programming logic was not performed and the focus was directed to the analog blocks that required a precise matching between the devices.

3.3.1 Floorplan

The floorplanning stage defines the physical placement of the functional blocks that are part of the LDO. This stage is important because it will influence matching accuracy and parasitic coupling, as well as overall performance. It is also helpful to have a preliminary idea of the area of the circuit. Consequently, the placement of the blocks needs to be carefully done to avoid deviations from their intended functionality. The initial floorplan is shown in Figure 3.19.

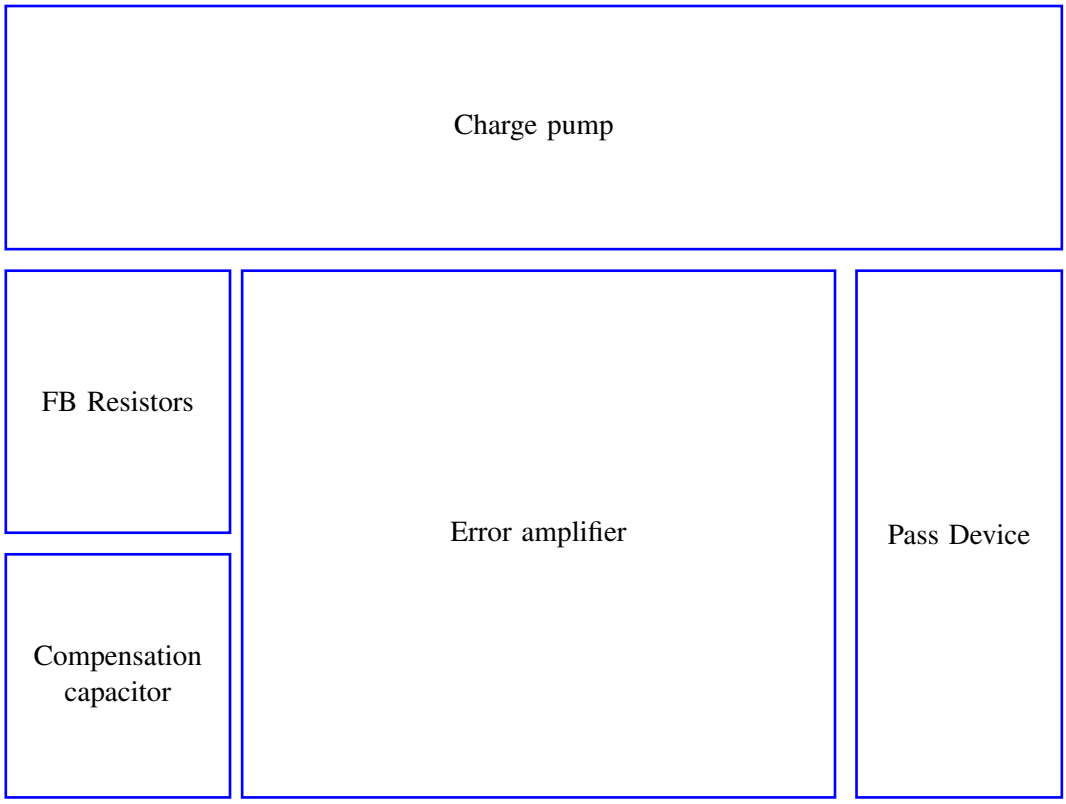


Figure 3.19: Initial floorplan of the layout.

The EA and the bias circuitry are positioned close to each other in order to minimize routing length and improve matching. The bias network incorporates important structures, such as current mirrors, used to set the operating point of the devices present in the EA. In fact, in Figure 3.19 only the EA is shown, because the error amplifier and the bias network are inside the same block. It is considered the biggest block of the circuit because it uses a several amount of thick-oxide devices to handle the high voltage of the CP.

The NMOS pass device, which is responsible to drive the load current needs to be placed next to the error amplifier. This is because it is a heavy device that carries a large amount of current,

which is not suitable to be matched with the internal devices of the EA. It is, therefore, treated as a single block. Another reason is that the output of the EA is connected to the gate of this device, and the closeness between the two allows to reduce the length of the routing.

Since the charge pump has a great amount of switching noise due to the operation of the clock signals, it was also allocated in a separate region relatively to the devices inside the EA. Due to timing constrains, the layout of the charge pump was not developed and the results presented in chapter 4 consider this block in the schematic implementation.

3.3.2 Error Amplifier and Bias Circuitry Layout

The EA is one of the most critical components of the LDO, as its performance directly influences the loop gain, bandwidth, and stability. Consequently, its layout needs to be done in a very cautious way to maintain the characteristics achieved after the schematic design.

This block was divided into five arrays of transistors:

- $M_{Pmirror}$; M_{Pbl}; M_{Pbr}; M_{Ptail}; $M_{Ploadup1}$; $M_{Ploadup2}$-these devices share a common terminal (V_{CP}), and they have the same length, which means that they can be in the same array.
- $M_{Ploaddown1}$; $M_{Ploaddown2}$-they have a different length from the previous ones, so they need to be placed in a separate array.
- M_{Pdiff1}; M_{Pdiff2}-these devices form the differencial pair. They need a very precise matching to achieve a strong symmetry. Contrary to the previous ones, they are low voltage devices, implying that they need a different guard ring.
- $M_{Nloadup1}$; $M_{Nloadup2}$-for the same reason as their PMOS counterparts.
- M_{Nref} $M_{Nmirror}$; M_{Nbl}; M_{Nbr}; $M_{Nloaddown1}$; $M_{Nloaddown2}$-for the same reason as their PMOS counterparts.

Figure 3.20 shows a portion of the array that includes the $M_{Pmirror}$ device. Since it includes a considerable amount of devices that act as current mirrors, a matching technique is required. Because there are many devices, an interdigitated layout is used due to the simplicity in the routing compared to common centroid. Dummy devices are used in the borders to ensure that all the devices share the same environment and to protect against WPE. The array continues downwards, following the same sequence and is flipped horizontally in each line to minimize gradient effects. Although it is not shown in the figure, there is also a line of dummies in the bottom of the array.

The array that includes $M_{Ploaddown1}$ is shown in Figure 3.21. In this case, a common centroid approach is used. Since the two devices do not share any terminal besides the gate, dummy devices in the middle are used to connect the two.

The array containing the differential pair transistor is depicted in Figure 3.22. It also follows a common centroid approach. In this case, some transistors that act as switches are used to improve matching and to protect against WPE. Since these switches are only receiving a static enable

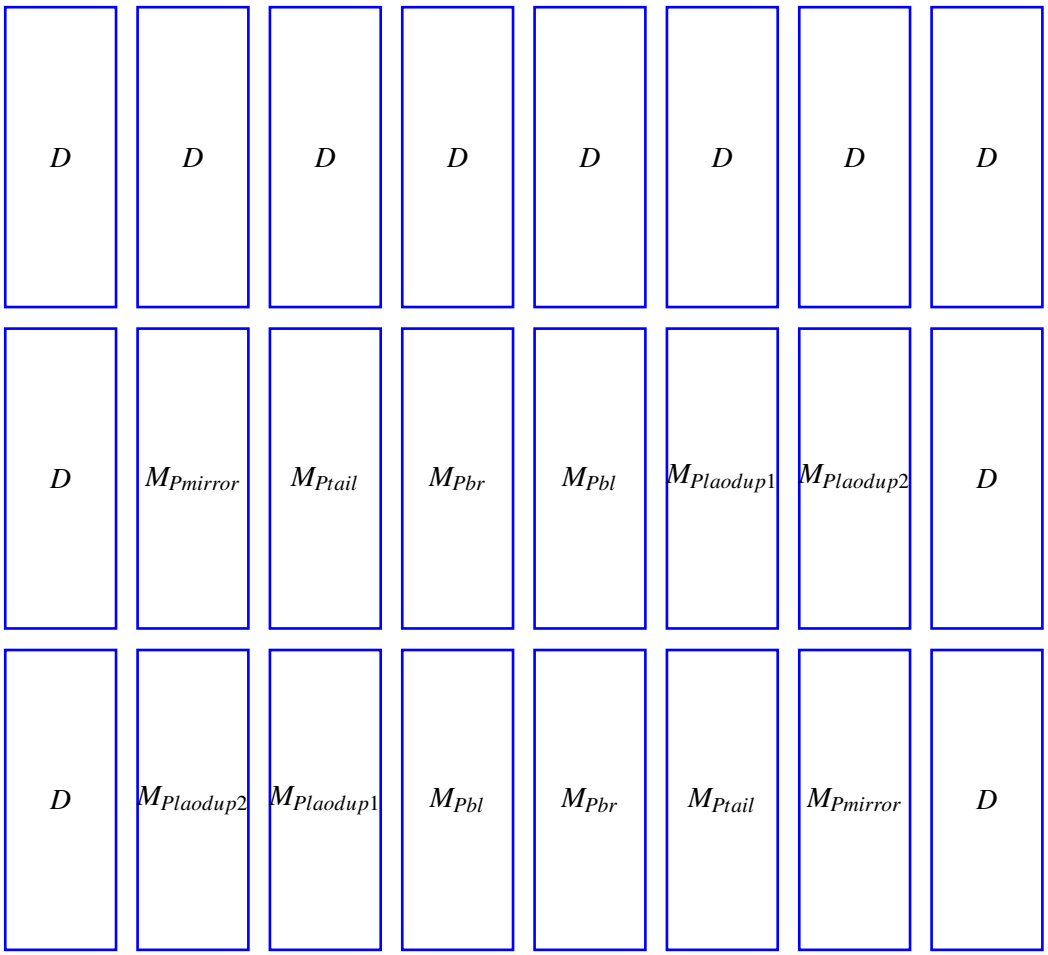


Figure 3.20: Matching of the top array.

signal, their only function is to allow or block the flow of current, meaning that they are always in triode or cut-off. Therefore, their matching is not of great importance.

The last two arrays were formed in a similar way to the first two, so their drafts are not shown here.

The routing needs also to be carefully considered. The width of the metal interconnects should be dimensioned taking into account two main factors: the amount of current that flows through them and their length. If a metal path needs to carry a higher current or has a very high length, its width should be increased accordingly to minimize IR drops. In addition the routing for differential input signals should be as symmetrical as possible, to avoid the introduction of offsets.

The connections to the power supply and ground were implemented using a grid that starts in the highest metal in the metal stack to the lowest one. It is important to use sufficiently wide metal traces to minimize IR drops. This is important for the guard rings to be biased in way that minimizes the substrate and n-well resistance, to avoid latch-up.

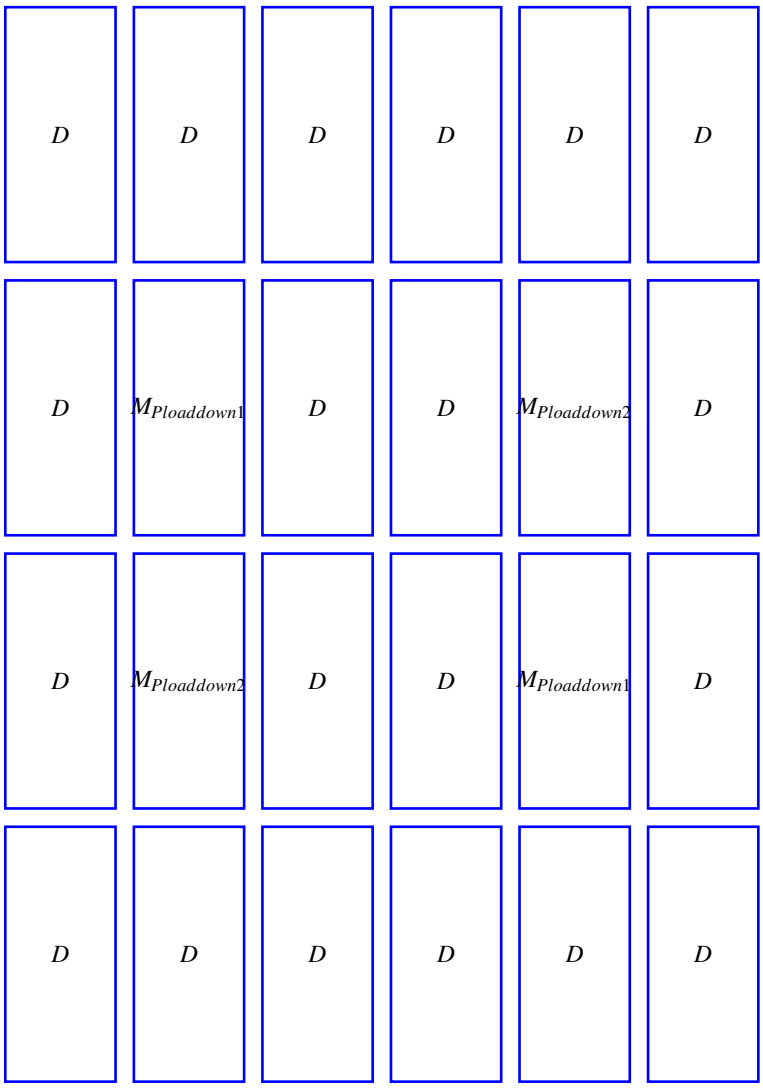


Figure 3.21: Matching of the array containing the PMOS cascode devices.



Figure 3.22: Matching of the array containing the differential pair.

3.3.3 Passive Components Layout

The placement of the passive components was carried out with the main goal of minimizing routing complexity and optimize silicon area utilization. These components must be placed carefully because they influence the output voltage accuracy and stability of the LDO.

The feedback resistors were positioned in unused regions inside the error amplifier boundary, improving area utilization and keep the interconnections as short as possible. The relatively large distance between R_1 and R_2 of the LDO, can lead to a small error in the ideal output voltage. Each resistor was divided in two series bars surrounded by dummies to improve matching.

The compensation capacitor was also placed inside the boundary of the error amplifier. The idea is that it must be located near the compensated node, which is the dominant pole of the system. It is important to minimize the length of the interconnect between the capacitor and this node, for the compensation network to behave similarly to the intended during the schematic design.

3.3.4 Pass Device layout

The pass transistor constitutes the largest active device of the LDO, because it needs to drive a large amount of current while keeping a small V_{DS}. Consequently, its physical implementation has a great impact on the performance of the system.

Due to its large size, it was treated as a single block rather than being placed in an array alongside other devices. Its location is close to the EA to avoid having a high interconnect distance between its gate and the output of the EA.

Because it needs to carry a high amount of current, its connection to V_{DD} needs to be as strong as possible. Since it carries approximately 1mA, an electromigration analysis is also needed. By using a wide trace of metal between V_{DD} and its drain, the risk of the formation of hillocks and voids due to electromigration is minimized.

3.3.5 Complete layout

The complete layout of the LDO with the exception of the CP and the programming logic is presented in Figure 3.23, illustrating the integration of the EA, pass device, bias circuitry, feedback network, and compensation capacitor. It is possible to observe the presence of the feedback resistors inside the boundary of the EA.

The layout occupies an area of $62\mu\text{m} \times 44\mu\text{m}$, corresponding to a total area of $2728\mu\text{m}^2$. This area includes all the implemented blocks alongside guard rings to bias the substrate and the n-well. To have a more realistic comparison in terms of area with other works, the layout of the charge pump should be also performed.

After the completion of the layout implementation, with DRC and LVS clean, a Parasitic Extraction (PEX) was performed. Post-layout simulations presented in the next chapter were carried out to evaluate the performance of the final system.

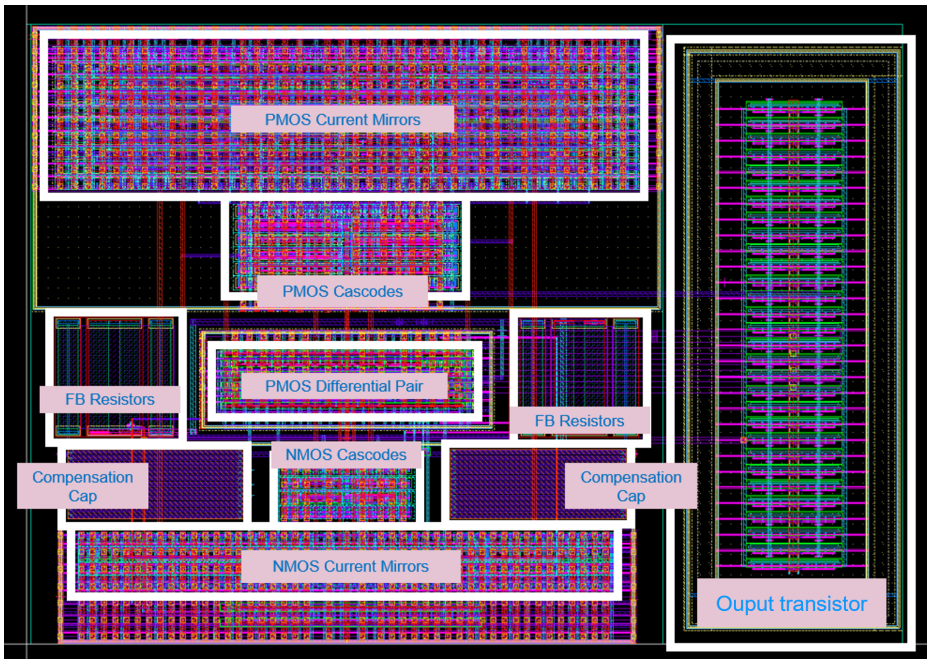


Figure 3.23: Layout of the LDO.

Chapter 4

Results

This chapter presents the simulation results of the proposed LDO. The main goal is to do an extensive verification of the implemented design and ensure that it satisfies the specifications established during the system-level design phase. It is important to verify both static and dynamic characteristics such as voltage regulation, stability, PSRR, transient response, power consumption, and efficiency. This section focuses on post-layout simulation results, but whenever necessary, pre-layout results are presented and compared to post-layout. Since the layout of the charge pump was not developed, the results presented in this chapter for that block are from schematic level simulations.

The performance of the LDO can be severely affected by manufacturing process, temperature variations, and supply fluctuations. Consequently, a PVT analysis is important to complement the simulations at typical conditions and ensure that the circuit remains robust under worst-case conditions. The corners used for these simulations are summarized in Table 4.1. It was used a load current of 1mA and load capacitance of 1pF, unless otherwise stated.

Table 4.1: Summary of the simulated PVT corners.

Corner	Process	Voltage	Temperature
corner_TT	TT	1.2V	25°C
corner_SS_TMIN_VMIN	SS	1.08V	−40°C
corner_FF_TMAX_VMAX	FF	1.32V	125°C
corner_SF_TMIN_VMIN	SF	1.08V	−40°C
corner_SF_TMAX_VMIN	SF	1.08V	125°C
corner_FS_TMIN_VMIN	FS	1.08V	−40°C
corner_FS_TMAX_VMIN	FS	1.32V	125°C

4.1 Charge Pump Metrics

The performance of the charge pump was evaluated to verify its ability of generating the boosted voltage to supply the EA. Its correct operation is fundamental to ensure a correct functionality of

the proposed LDO. Since the layout of the charge pump was not developed, the results presented in this section correspond to the schematic implementation. The clock signal was implemented as an ideal square wave with a period of 1ns and a rise and fall time of 10ps.

Figure 4.1 shows the startup behaviour of the charge pump. It is possible to observe that in the beginning, the output increases progressively in small steps before settling in its final value. For the typical corner (TT), the average value of V_{CP} is approximately 2.05V and has a settling time of about 17ns. The corner in which the waveform takes more time to settle is the SS_TMIN_VMIN, with a settling time of 27ns and a steady-state voltage of 1.83V. The higher error in this corner occurs due to the lower value of V_{DD} and because in the SS process, the ON resistances of the devices are larger. The generated voltage is enough to supply the EA, maintaining its functionality, as it will be possible to observe in the following sections.

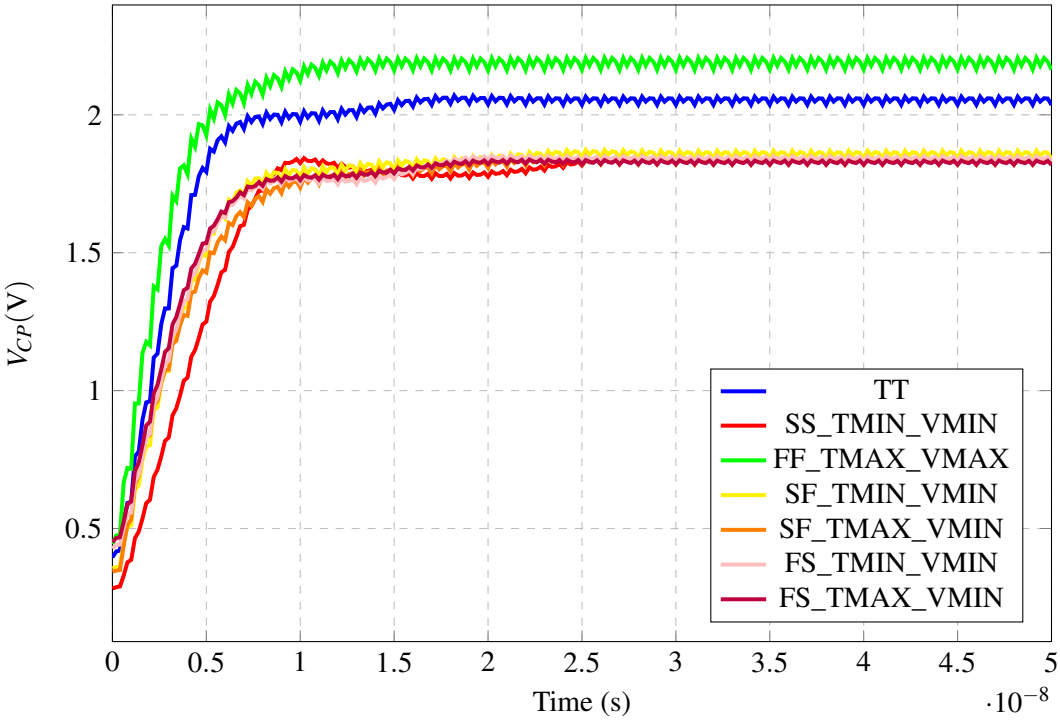


Figure 4.1: Startup simulation of the charge pump.

The switching nature of the charge pump inevitably produces a periodic ripple at V_{CP}. Figure 4.2 presents a detailed view of the steady-state waveform, in which the ripple can be observed. For the typical corner, it has a variation of approvimately 50mV. The worst case occurs in the FF_TMAX_VMAX, with a ripple of approximately 80mV.

The average input current of the charge pump is approximately 520μA for the typical corner, leading to an efficiency of

$$\eta_{CP} = \frac{210\mu \times 2.05}{520\mu \times 1.2} \approx 65.7\% \tag{4.1}$$

The value of 210μA corresponds to the current drawn by the EA which is, in this case, the output current of the CP. The corner FF_TMAX_VMAX is where the power consumption is higher, with

an input current of 580μA and an efficiency of $\approx$ 62.6%.

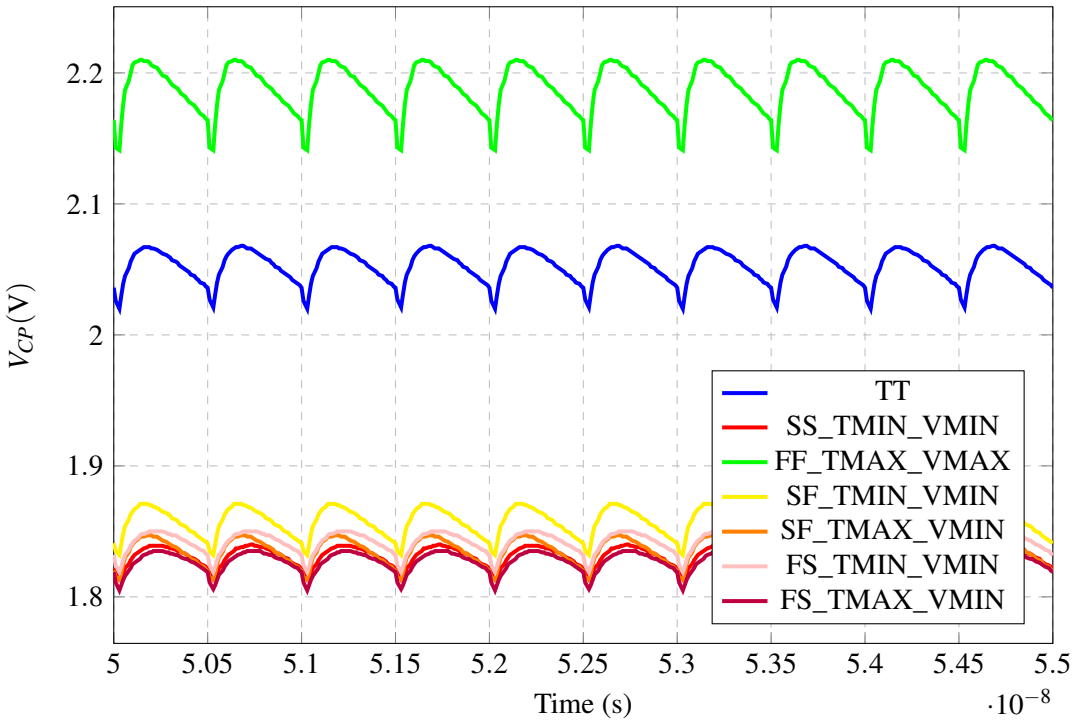


Figure 4.2: Ripple at the charge pump output.

4.2 DC Performance

To verify the ability of regulation of the LDO, a DC analysis was performed. It is important to see the behaviour of the output voltage V_O as a function of the supply voltage to evaluate the minimum dropout voltage. For this test, the CP was replaced by an ideal voltage of the same value as V_{CP}. Analysing Figure 4.3, it is possible to observe that the regulator is able to keep V_O at 950mV with a minimum supply voltage of approximately 1V, which is the point where the pass device enters the saturation region. The conclusion is that, for the typical corner, the minimum dropout voltage is about 50mV with 1mA of load current. Even in the region where the pass transistor is in saturation, a small variation of V_O with V_{DD} can be observed. The slope $\frac{\partial V_O}{\partial V_{DD}}$ corresponds to the line regulation, which is about 75μV/V.

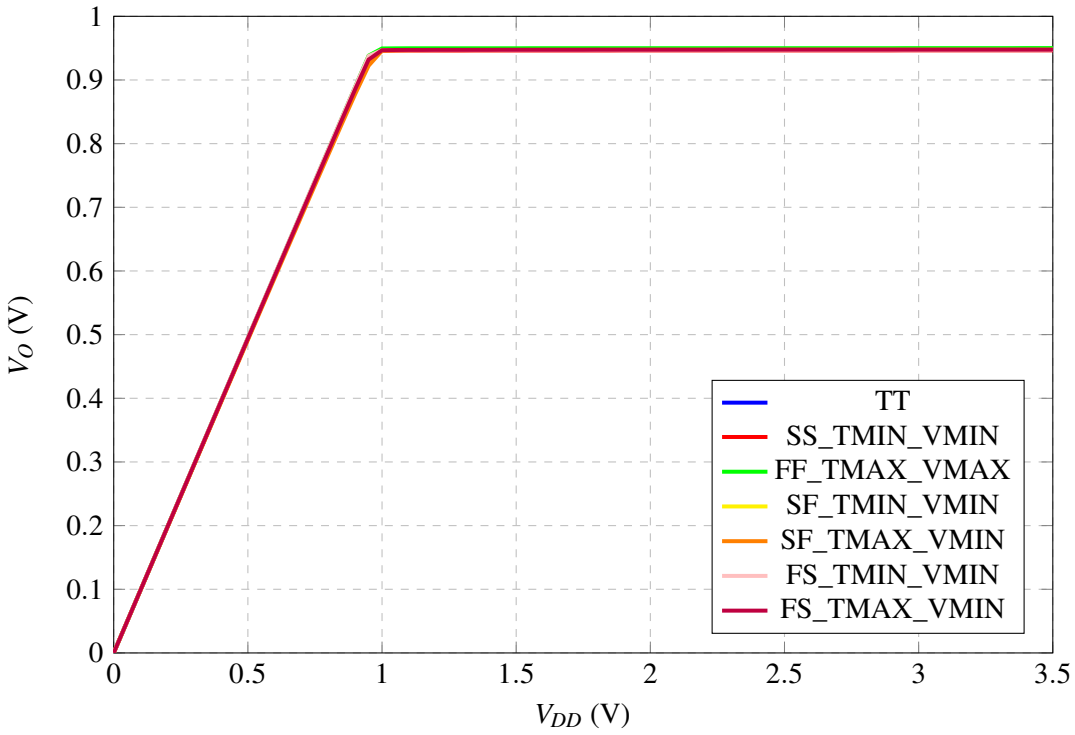


Figure 4.3: Plot of V_O vs V_{DD} for 1mA of load current.

Figure 4.4 shows V_O as a function of R_L. The plot shows that the regulator is capable of keeping the value of V_O at approximately 950mV for a load current of 1mA, which shows that the pass device is wide enough to drive that amount of current, for the typical corner. It is also possible to observe that the circuit is capable to regulate the voltage for a minimum value of R_L of 350Ω, translating to a maximum load current of approximately 2.5mA. This experiment was done using the nominal value of V_{DD}, which is 1.2V. The load regulation, which is the slope $\frac{\partial V_O}{\partial I_L}$ is about $2\text{mV}/\text{mA}$.

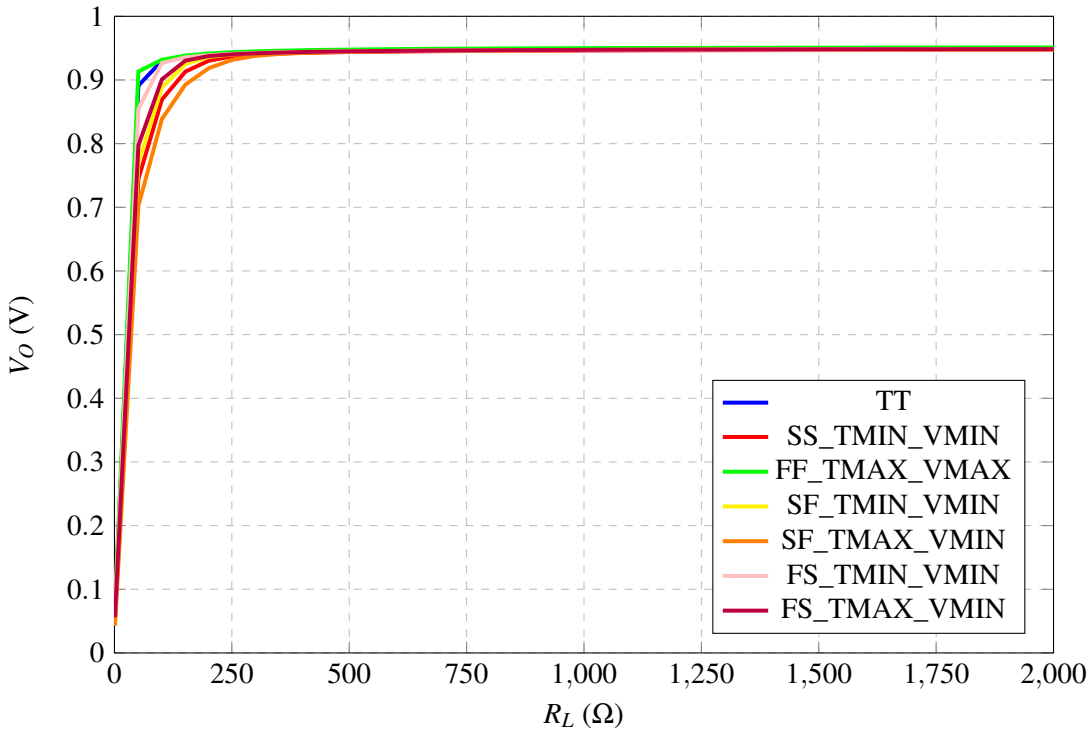


Figure 4.4: Plot of V_O vs R_L for 1.2V of supply voltage.

Table 4.2 presents the value of V_O for each corner. The corner SS_TMIN_VMIN presents the highest error in the output voltage. This is because, V_{TH} of M_{Nout} device will increase and $M_{Ploaddown2}$ will tend to leave the saturation region, decreasing A_1. In general, the difference between the ideal and real output voltages increased after parasitic extraction. As the pre and post-layout loop gain are similar, the conclusion is that this error is caused by mismatch in the feedback resistors, causing a deviation in the value of β.

Table 4.2: V_O for different PVT corners for $I_L = 1$mA.

Corner	V_O pre-layout	V_O post-layout
TT	949.35mV	947.84mV
SS_TMIN_VMIN	947.28mV	946.14mV
FF_TMAX_VMAX	951.34mV	949.83mV
SF_TMIN_VMIN	948.36mV	946.93mV
SF_TMAX_VMIN	948.16mV	946.94mV
FS_TMIN_VMIN	948.45mV	947.00mV
FS_TMAX_VMIN	948.41mV	947.16mV

4.3 Stability Analysis

The stability of the proposed LDO was evaluated through an AC simulation. The objective of this analysis is to evaluate the loop-gain and phase, over a wide range of frequencies, verifying the stability of the feedback loop. The parameters that require more attention are the loop-gain, gain crossover frequency and phase margin.

To evaluate the frequency response, the feedback loop was opened using a probe. This allows a precise measurement of the loop-gain without changing the DC operating point.

The movement of the poles is expected to happen after the physical implementation. It is, therefore, interesting to compare the the results of pre and post-layout simulations, as shown in Figure 4.5 for typical corner. As expected, due to the introduction of parasitic capacitances, the system's poles moved to the left, decreasing the UGF, which dropped from 110MHz to 85MHz. The magnitude of the loop-gain increased due to the resistances introduced by the metal lines.

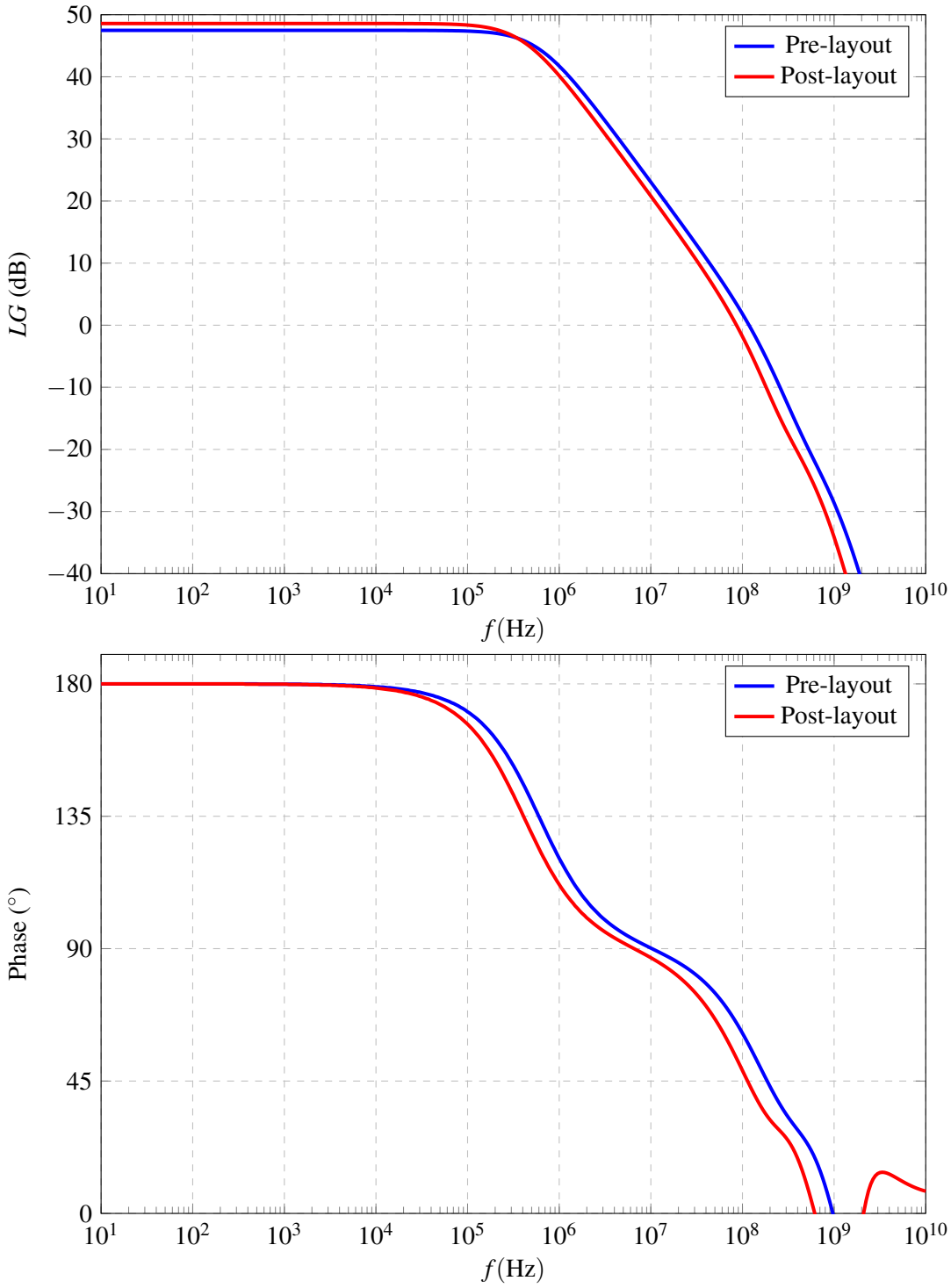


Figure 4.5: Comparison of pre and post-layout loop-gain magnitude and phase.

It is important to compare the performance when the regulator is operating with a light load and with a heavy load, as shown in Figures 4.6 and 4.7. For the low frequency gain, it is possible to observe that the two cases are similar. This is a sign that the pass device is wide enough to drive 1mA of current without decreasing the performance of the system. However, in terms of phase

margin, there is a significant difference in the behaviour of the loop for the two cases. For 1mA of load current, the phase margin is about 57° while for light load it drops to approximately 25°. This occurs because the output pole moves to the left as the load current decreases, decreasing the phase margin. This is explained by the fact that the frequency of that pole is inversely proportional to $1/g_{mpass}$. The gain crossover frequency also falls from 120MHz to 90MHz.

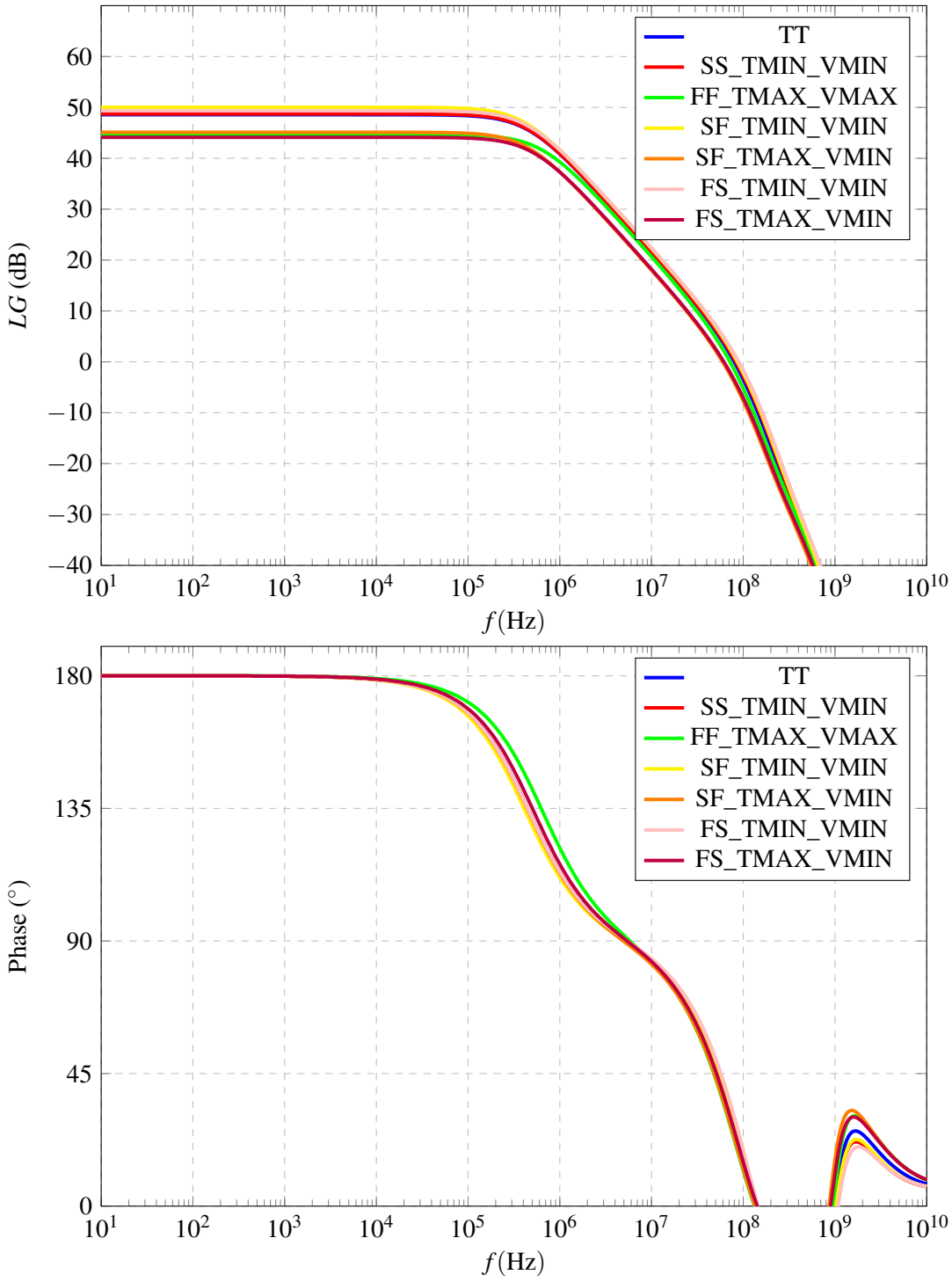


Figure 4.6: PVT simulations for the loop gain magnitude and phase when $I_L = 0mA$.

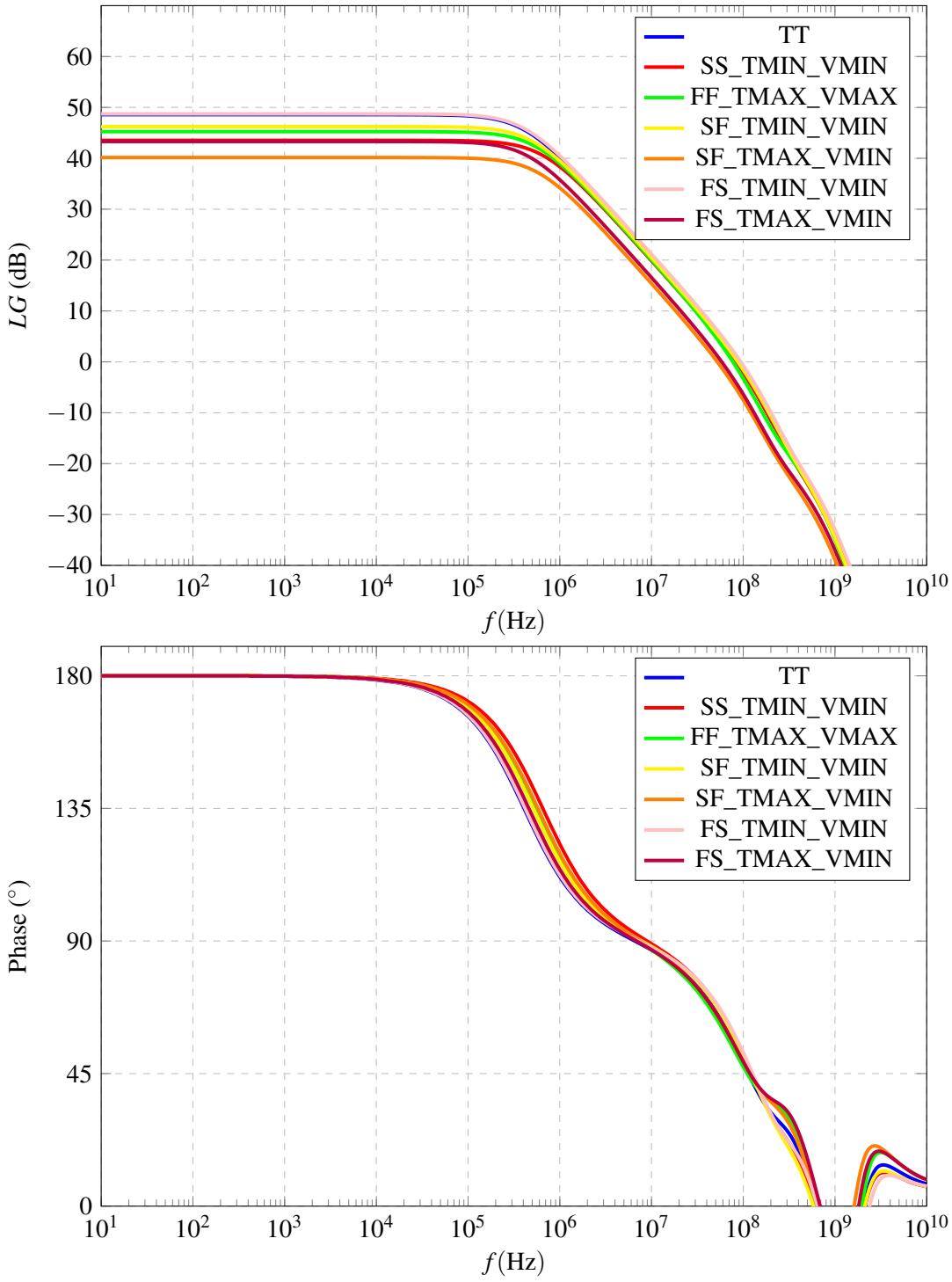


Figure 4.7: PVT simulations for the loop gain magnitude and phase when $I_L = 1mA$.

Table 4.3 presents the phase margin for every corner when the load current is in its lowest value and shows that SF_TMIN_VMIN is where the phase margin reaches its minimum value. This reveals the need for a monte carlo analysis for that corner in order to ensure that the system is stable in the presence of device mismatches.

Table 4.3: Phase margin for different corners

Corner	Phase margin ($I_L = 0$mA)
TT	25.24°
SS_TMIN_VMIN	25.75°
FF_TMAX_VMAX	27.51°
SF_TMIN_VMIN	23.17°
SF_TMAX_VMIN	36.40°
FS_TMIN_VMIN	24.76°
FS_TMAX_VMIN	37.35°

4.4 Power Supply Rejection Ratio

The PSRR represents the ability of the LDO to reject the variations in the supply voltage before they appear at the regulated output. A high PSRR ensures that these variations have little impact on the regulated voltage.

It was evaluated using an AC analysis that imposes small-signal variations on the supply voltage over a wide frequency range. The main goal is to observe the effect of these variations on the output voltage. The PSRR of the proposed LDO is plotted in Figures 4.8 and 4.9.

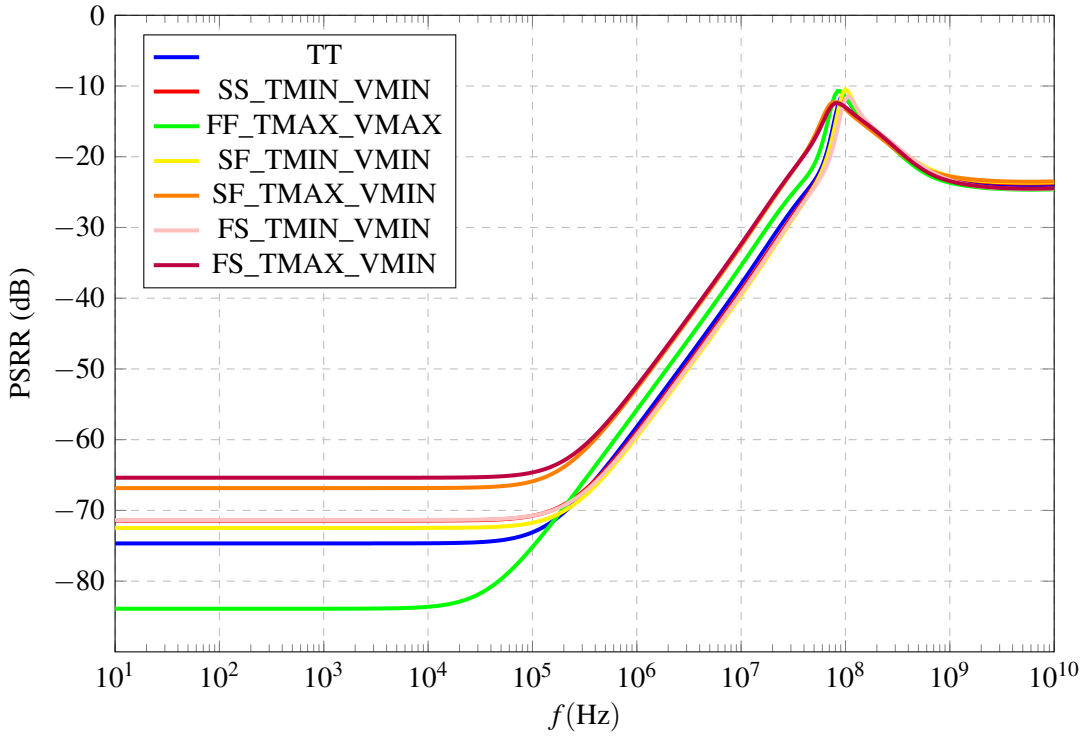


Figure 4.8: PVT simulations for PSRR with no load current.

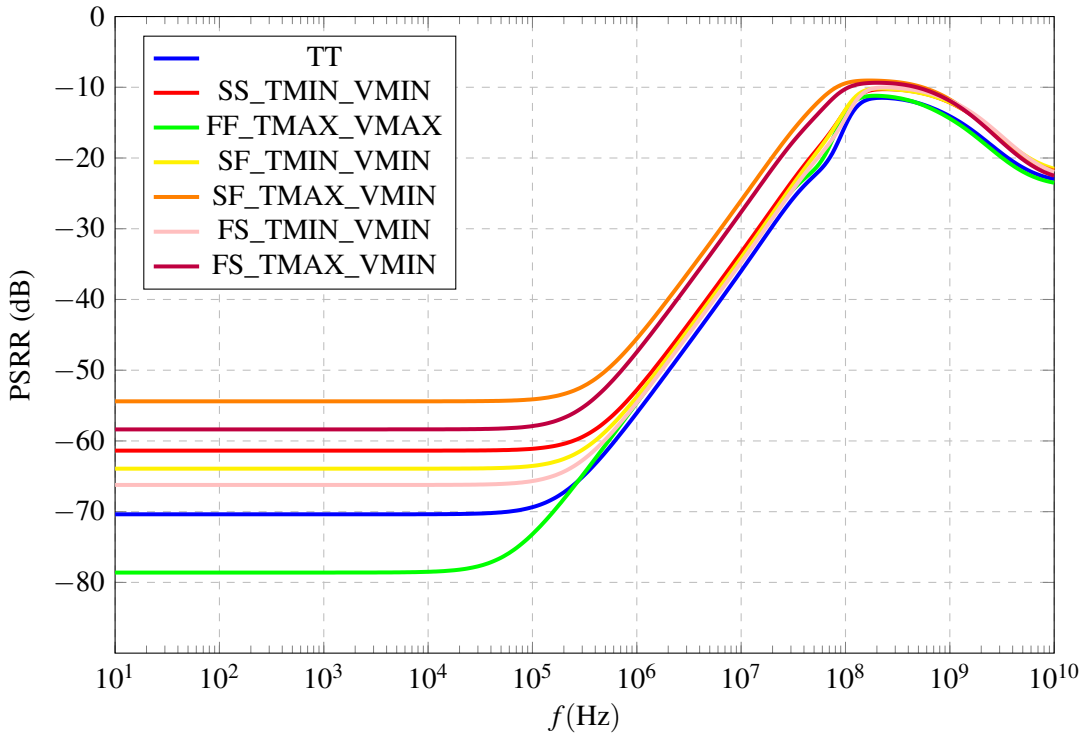


Figure 4.9: PVT simulations for PSRR with $I_L = 1\text{mA}$.

As expected, the PSRR is higher for light load, because both the product $g_{mpass}r_{opass}$ and A_1 decrease with the load current, which will decrease the rejection as stated in equation 2.4. For both cases, the LDO shows a high rejection for low frequencies. This happens because for that frequency region, the PSRR is primarly determined by the amplifier DC gain. As the frequency increases, the rejection becomes degraded due to the limitation on the bandwidth of the feedback loop. For high frequencies, the feedback loop presents almost no contribution to the PSRR.

A considerable variation across corners is seen for low frequencies because, for that range, the PSRR is highly dependent on the values of $g_{mpass}r_{opass}$ and A_1. The frequency in which it becomes to decrease also shows a significant variation because the banswidth of the loop varies considerably with the corners. However, it is possible to observe that the PSRR lies below -50dB for all corners.

4.5 Startup Analysis

Transient simulations were performed to evaluate the startup behaviour of the LDO from an unpowered state. This analysis is important to ensure that all the devices reach the intended operating point in a controlled way.

The startup simulation was performed through a step in the enable signal. The behaviour of V_O was analysed in both light and heavy load as shown in Figure 4.10. It is possible to observe that for no load condition, the waveform of V_O presents a considerable ringing, settling in approximately

35ns for typical corner. This ringing occurs because of the small phase margin in this current range. In its off state, the regulator consumes approximately 180nA of current.

The SS_TMIN_VMIN is the slowest corner to turn on, taking approximately 60ns to settle. When the regulator is in off state, for corners FF_TMAX_VMAX and FS_TMAX_VMIN, it is possible to observe that the value of V_O is slightly above 0V. This suggests the presence of some leakage current in those corners.

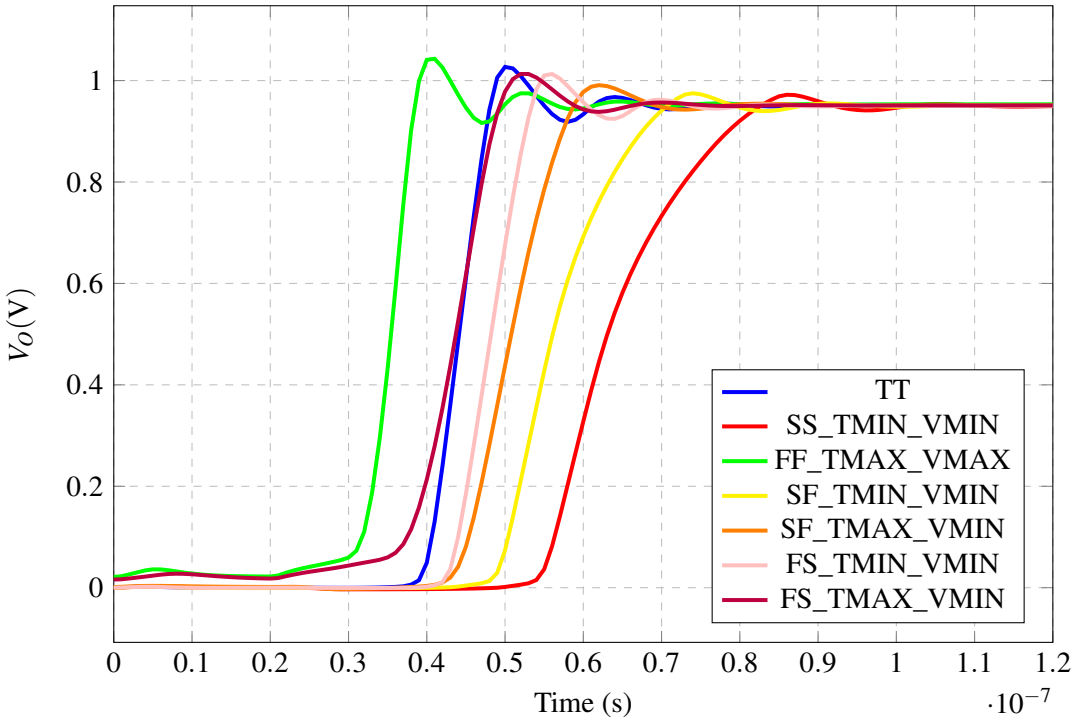


Figure 4.10: PVT simulations for startup.

4.6 Transient Response

The transient response of the LDO was analysed to evaluate its ability to keep a stable output voltage when sudden changes in operating conditions occur. For this test, abrupt variations in the load and in the supply were considered.

The line transient response was evaluated by applying a transient step equal to $\pm 10\%$ of V_{DD} with a rise time of 1ns. Figure 4.11 shows the behaviour of V_O for the input supply step. It is possible to observe that a small perturbation occurs in the output voltage with a maximum overshoot of approximately 25mV and maximum undershoot of 30mV, settling in approximately 13ns for the typical corner.

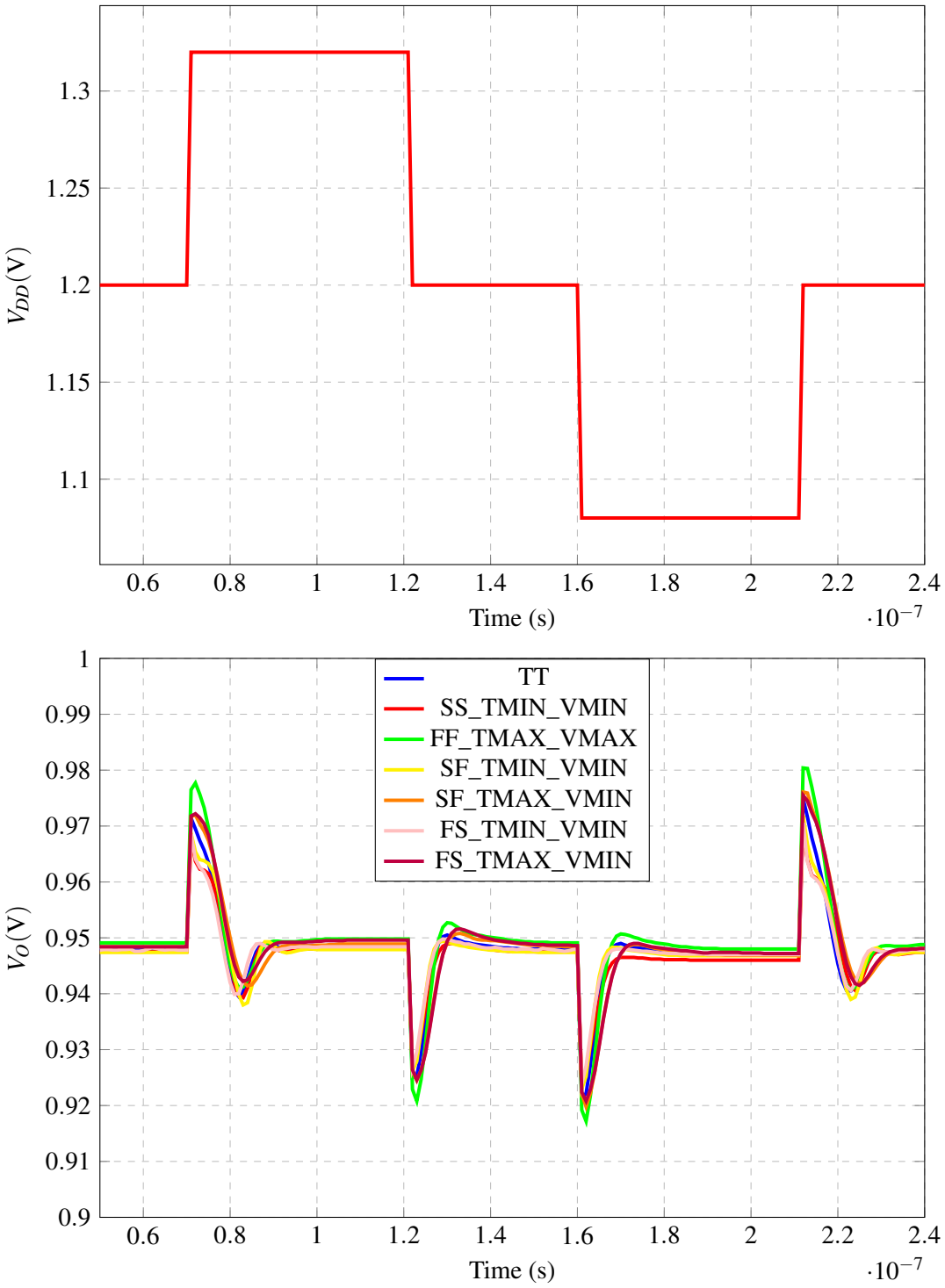


Figure 4.11: PVT simulations for line transient.

To evaluate the load transient response, a step of load current from 0mA to 1mA with a 1ns was applied. Figure 4.12 presents the waveform of V_O for the load current when the current steps from low to high and from high back to low. When there is a sudden increase in the load current, the feedback loop cannot respond instantaneously due to its finite bandwidth. This causes an

undershoot of 115mV and the loop corrects the value of V_O in 12ns in the typical corner. When the load current decreases, a significant amount of ringing in the waveform of V_O can be observed due to phase margin degradation and the settling time increases to about 30ns with an overshoot of 140mV for TT.

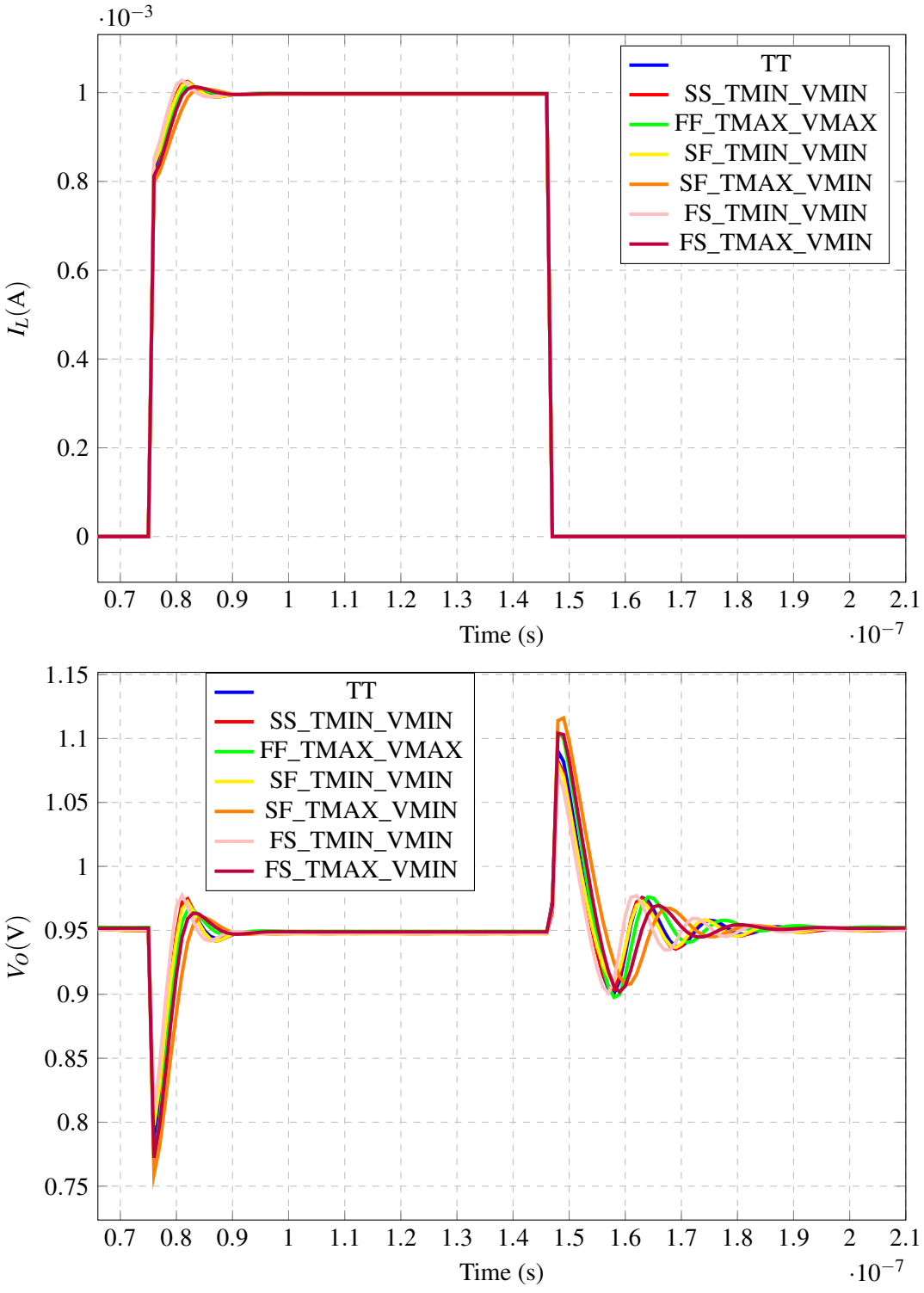


Figure 4.12: PVT simulation results for load transient.

4.7 Output Ripple

The output ripple of the proposed LDO was evaluated to assess the influence of the switching activity of the charge pump. The waveforms of V_O showing the ripple in more detail are presented in Figure 4.13.

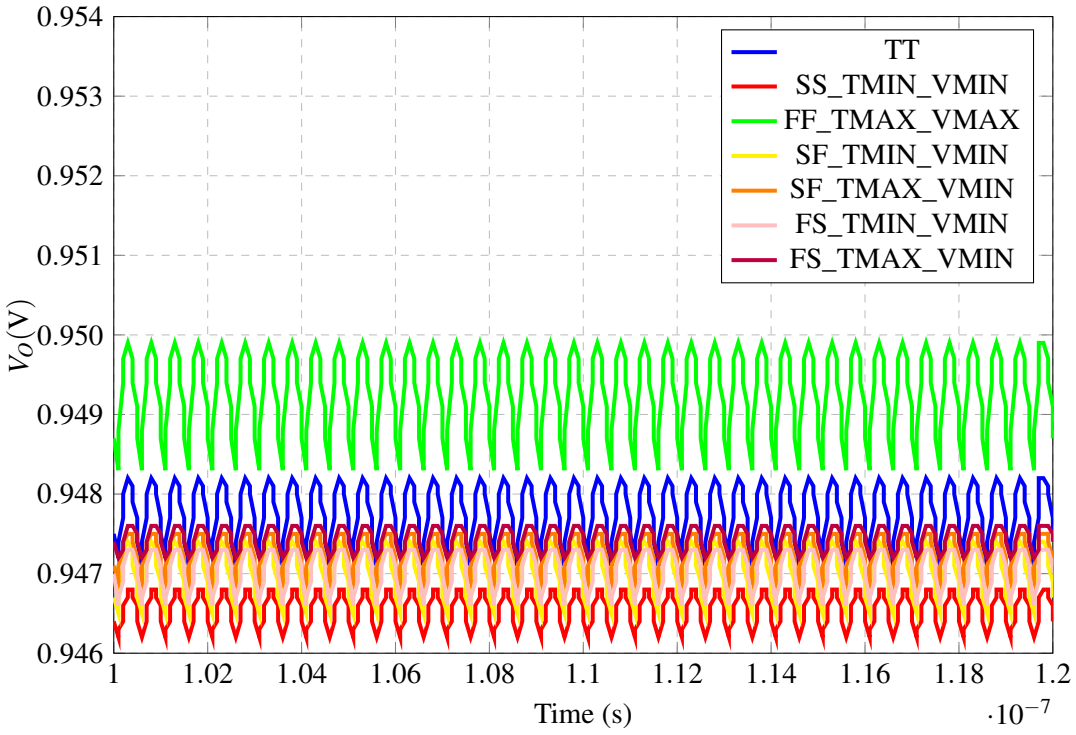


Figure 4.13: PVT simulations for the output ripple.

The peak-to-peak variation is approximately 1mV for typical corner and 1.8mV for the worst case, which is the corner FF_TMAX_VMAX. Despite this periodic variation, the operating point of the circuit is not significantly affected, meaning that the regulator still preserves performance.

The EA is capable of rejecting the majority of the fluctuations that come from V_{CP}. However, since the charge pump operates at a relatively high frequency, some capacitive coupling paths from V_{CP} to V_O will appear, creating a way for a fraction of the ripple to propagate to the output.

4.8 Power Consumption and Efficiency

The power consumption of the LDO was evaluated by measuring the load current and quiescent current. The quiescent current represents the internal current required to bias the different internal blocks such as the EA and the charge pump. Since this current is flowing continuously, it has a great impact in the efficiency of the circuit.

The quiescent current I_Q of the LDO is about 530μA. Since the error amplifier consumes approximately 200μA of this current, it is possible to conclude that the charge pump is responsible

to consume more than a half of the quiescent current of the LDO. This translates to an efficiency of

$$\eta = \frac{P_{OUT}}{P_{IN}} \times 100 \approx 51.7\% \tag{4.2}$$

for 1mA of load current.

4.9 Monte Carlo Simulations

Monte Carlo simulations were performed to evaluate the sensitivity of the LDO to statistical variations in the device parameters. While the PVT analysis evaluates the design under pre-defined conditions, Monte Carlo analysis provides a statistical evaluation of the circuit behaviour by introducing random variations in the device parameters. This analysis is particularly important to evaluate the impact of device mismatches in the performance of the circuit.

These simulations prove useful to evaluate the effect of mismatches in the components inside the circuit. Those mismatches represent variations between devices that were supposed to be identical but are different due to manufacturing imperfections.

4.9.1 Output Voltage Variation

The output voltage was selected as one of the most important metrics for the Monte Carlo analysis, as it can be severely affected by device variations. Mismatches in trasistor parameters can lead to the introduction of offsets, reinforcing the need for evaluation. Figure 4.14 presents the distribution of V_O for mismatch Monte Carlo simulations for corner TT.

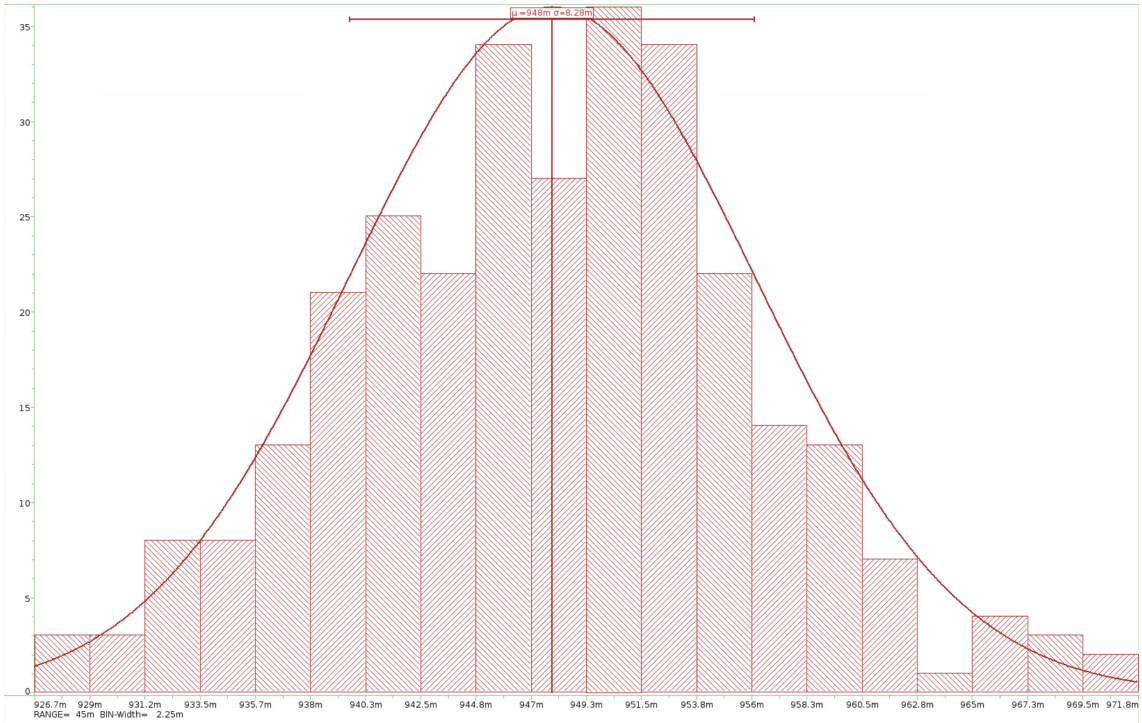


Figure 4.14: Monte Carlo simulations for the Direct Current (DC) value of V_O.

The results show that the output voltage is distributed around the mean value of 948mV with a standard deviation of approximately 8.28mV. The minimum and maximum simulated values are 926.7mV and 971.8mV, respectively.

Since the corner SS_TMIN_VMIN is the one whose measured value has the highest deviation to the ideal value, it is also important to run a Monte Carlo simulation for it. The results for this corner are presented in Figure 4.15 and show an average value of 947mV and a standard deviation of 8.38mV.

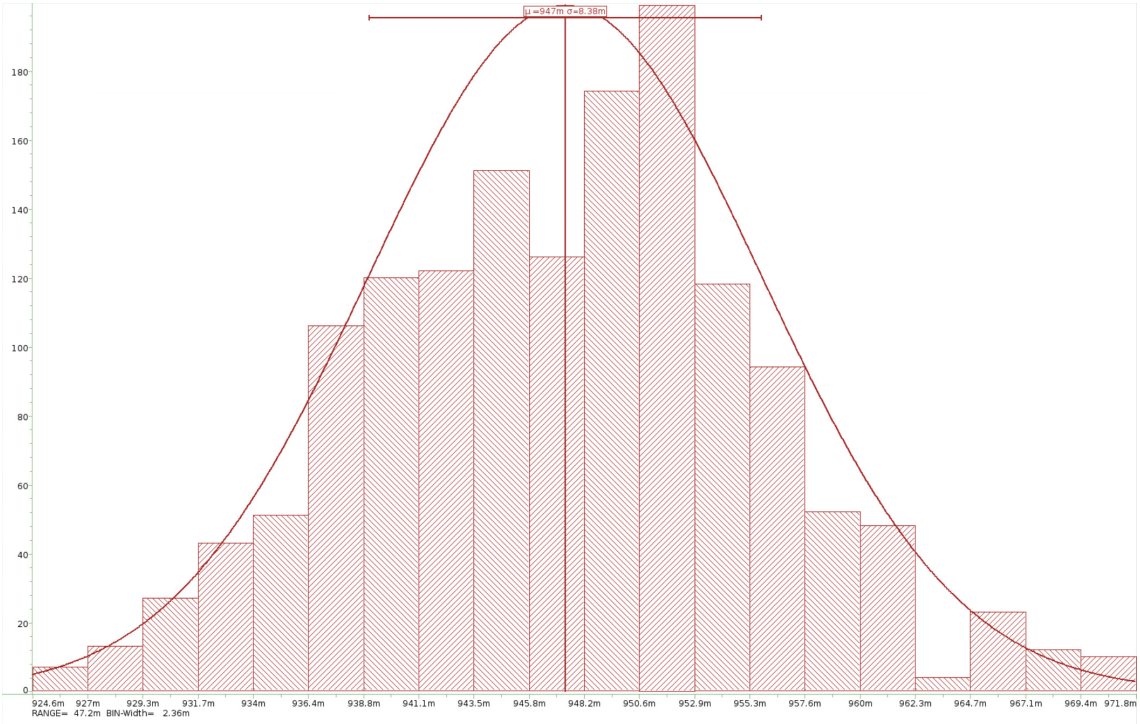


Figure 4.15: Monte Carlo simulations for the DC value of V_O in SS_TMIN_VMIN corner.

4.9.2 Loop Stability

Monte Carlo simulations were aditionally used to evaluate the robustness of the loop stability. Since variations in the parameters of the devices can modify the positions of poles and zeros of the system, simulations to observe the behaviour of the phase margin were performed. This analysis is particularly important for the case when $I_L = 0$mA.

For typical corner, it presents an average value of 25° with a standard deviation of 2.2°. The minimum phase margin obtained in the simulation runs was 22°, demonstrating that the LDO eventually stabilizes during transient response. However, this value of phase margin can lead to significant ringing in the circuit as it is very low.

Monte Carlo simulations for the phase margin were also performed in the worst-case corner, which is the SF_TMIN_VMIN, as presented in Table 4.3. The average value is 25° while the standard deviation is 5.18°. The minimum value is 18.9°.

4.10 Performance Summary

The main characterisitcs of the LDO are summarized in a datasheet shown in table 4.4. The values were obtained from the post-layout simulations presented in this chapter in nominal conditions.

Table 4.4: Summary of the proposed LDO performance for the typical corner.

Parameter	**Value**	**Unit**
Supply voltage (V_{IN})	1.2	V
Nominal output voltage (V_{OUT})	0.95	V
Maximum load current	1	mA
Dropout voltage	250	mV
Quiescent current (I_Q)	530	μA
Line regulation	75	μV/V
Load regulation	2	mV/mA
DC loop gain	48.5	dB
Unity-gain bandwidth	85	MHz
Phase margin	57	$^\circ$
PSRR @ 1 kHz	-70	dB
PSRR @ 100 kHz	-69.4	dB
Load transient undershoot	115	mV
Recovery time	12	ns
Startup time	35	ns
Operating temperature range	-40 to 125	°C
Total silicon area	2728	μm^2

Chapter 5

Conclusions and Future Work

5.1 Conclusions

This dissertation focused on the design, layout, and verification of a CMOS LDO regulator with an NMOS pass device. The design is composed by a folded cascode EA, a pass device, and a charge pump to achieve low-dropout. The layout of the charge pump was not developed and programming logic was not developed.

A wide number of simulations was performed to assess the regulator performance. DC, AC, stability, transient, and PVT analyses demonstrate that the design fulfills the specifications defined in the system-level for the specified range. Post-layout simulations confirm that the regulator is still functional after the inclusion of non-idealities introduced by the layout.

The circuit delivers a stable 0.95 V output with a line regulation of only 75μV/V and a load regulation of 2mV/mA of load current, which demonstrates its ability to keep an output voltage independent of supply and load conditions.

In terms of stability, the closed-loop bandwidth after layout is 85 MHz, and at a nominal load of 1 mA the phase margin is 57°, which guarantees a well-damped response. When the load is reduced to zero, the phase margin falls to approximately 25°, which explains the ringing observed when the load current falls to 0mA.

The LDO achieves a typical low frequency PSRR of approximately -71dB. It varies along the corners because of the variation in supply voltage and process parameters. The gradual degradation at higher frequencies follows the loop bandwidth limitation, which is expected for an LDO of this architecture.

With a 1mA of load current, the efficiency of the regulator is approximately 52%. This reveals that this architecture is more suitable for higher values of load current in terms of efficiency.

A tota area of 2728μ^2 was obtained in the layout, with the exception of the charge pump as stated before. In this case, the error amplifier is the biggest block in the circuit. However, in order for the circuit to carry a larger value of load current, the pass device would need to become dominant in terms of area.

Table 5.1 shows a comparison between the proposed LDO with previously reported designs. The quiscent current I_Q is the main the drawback of the design and for a 1mA LDO it limits severely its efficiency. The PSRR remains as one of the strongest points in the proposed design. The value of FoM_1 represents the amount of load current per unit of area and is given by

$$FoM_1 = \frac{I_{LMAX}}{Area} \tag{5.1}$$

The proposed LDO has a $0.367\text{A}/\text{m}^2$, although the layout of the CP and the programming logic would give a more accurate value.

Table 5.1: Comparison of the proposed LDO with other designs reported in the literature.

	[20]	[21]	[22]	[23]	[24]	This work
Pass transistor	NMOS	NMOS	PMOS	NMOS	NMOS	NMOS
Technology [nm]	180	180	65	180	500	55
Input Voltage V_{IN} [V]	1.8	1.6–1.8	1.2	1.2	2.7–4.2	1.2
Output Voltage V_O [V]	1.2	1.4–1.6	1.0	1.0	2.4–4.0	0.8–0.95
Load Capacitance C_L [pF]	–	0–50	120	100	$0–10^6$	1
Active area [mm^2]	0.079	0.21	0.087	0.185	0.33	0.002728
Quiescent Current I_Q [μA]	265	133	8–297.5	80–87	48	530
Current Range ΔI_L [mA]	0-10	31	25	299	0-2000	0-1
Undershoot ΔV_O [mV]	44	166	225	59	13–68	115
T_{settle} [μs]	0.3	0.019	1.5	0.48	1.2–1.65	0.012
PSRR [dB] @Hz	-39@20M	-71@1k	-52@1M	-52@10k	-33@100k	-71@10k -55@1M
FoM$_1$ [A/mm^2]	0.126	0.148	0.287	1.622	6.061	0.367

5.2 Future Work

Although the proposed LDO fulfills the design specifications, there are still several oportunities of future work for performance enhancement.

The first extension that can be applied to this work, is the development of the charge pump layout, followed by the post-layout verification of the complete regulator. This would allow a better comprehension of the influence of the parasitic effects introduced by this block and how they affect parameters, such as output ripple and startup time.

Another investigation that could be made is the development of a clock signal generator for the charge pump. This could be made using a ring oscillator with a mechanism of frequency control.

Compensation techniques to improve stability, specially at no load conditions to enhance transient performance would also be relevant to study. In addition, the implementation of an adaptive biasing technique or a fast loop could be interesting to reduce the quiescent current while keeping a good transient response under sudden changes in load conditions.

This work was done using a 55nm planar technology. To reduce the layout area, a smaller technology node could be used. A FinFET approach could be an interesting option to explore not only to reduce area, but to boost the performance of the regulator itself. As stated before, the

higher $\frac{g_m}{g_{ds}}$ of the FinFET can contribute to a higher loop gain and, consequently, a better supply rejection.

Finally, the final validation of the proposed LDO would consist of fabrication and experimental characterisation of the IC. This would allow comparing real world results with simulation, enabling the verification under practical operating conditions.

In summary, the proposed architecture may serve as a starting point for future developments targeting higher efficiency, improved transient response, and reduced silicon area.

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