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Control of Smart Reflectarray Antennas for Earth Observation and High Data-Rate Communications

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Resumo

Atualmente, um dos desafios de RF nos sistemas espaciais está relacionado com a otimização do tamanho e da massa do equipamento para o desempenho pretendido. Os sistemas espaciais atuais requerem antenas de alto ganho para atender aos requisitos de melhoria da resolução de imagem na observação da Terra e de comunicações com taxas de dados mais elevadas. Uma antena reflectarray modular, eletronicamente reconfigurável, é uma opção promissora para maximizar a razão entre a área efetiva da antena, quando desdobrada, e o volume, quando armazenada.

Esta tese de doutoramento apresenta o projeto, a implementação e a validação de uma arquitetura reflectarray sem fios, com orientação eletrónica do feixe (SATORI). A principal contribuição é um novo sistema de controlo que desacopla o *payload* em banda X de uma ligação de comando robusta a 433 MHz, eliminando, assim, a necessidade de cablagens de controlo complexas. Esta ligação é gerida por um “interpretador” híbrido microcontrolador-FPGA, de tamanho reduzido, em cada mosaico modular, que aciona díodos varactor de baixa potência para controlar a fase de reflexão de cada célula unitária.

Um protótipo de 0,5 m x 0,5 m, com 625 elementos, foi construído e validado na instalação CATR da ESA. O sistema demonstra com sucesso uma orientação eletrónica precisa do feixe até $\pm 30^\circ$, com uma precisão de apontamento de $\leq 0.2^\circ$. O plano de controlo sem fios revelou-se altamente fiável, tendo-se perdido apenas 42 pacotes ao longo de 13 horas de ensaios contínuos sobre a abertura, validando a premissa central da arquitetura.

O protótipo alcançou uma diretividade máxima de 22.8 dBi e um ganho máximo de ≈ 17 dBi. A eficiência total resultante de $\approx 25\%$ é um resultado previsto e quantificado do projeto, representando um compromisso de engenharia deliberado associado à utilização de varactores COTS de baixo custo para obter controlo contínuo da fase. Este orçamento de perdas de ≈ 6 dB é analisado em detalhe, sendo identificadas como principais contribuições as perdas por inserção dos varactores e a eficiência de iluminação do alimentador. Este trabalho valida com sucesso uma arquitetura escalável e resiliente para antenas reconfiguráveis, demonstrando a sua eficácia na obtenção de uma solução robusta e adaptável. Além disso, fornece um roteiro claro para trabalho futuro no sentido de aumentar a eficiência de abertura através da integração de elementos de sintonia com Q mais elevado.

A reflectarray proposta, com orientação eletrónica do feixe e controlo sem fios, oferece uma abordagem modular, com uma interface mais simples entre a antena e a plataforma do satélite, bem como um volume de armazenamento promissora reduzido para uma antena de grande área desdobrável. Os resultados obtidos neste trabalho mostram que esta tecnologia reflectarray é competitiva quando comparada com outras soluções para antenas de grande abertura.

Abstract

Nowadays, one of the RF challenges in space systems relates to equipment size and mass optimisation for the desired performance. Current space systems require high-gain antennas to meet the demanding requirements for improved Earth Observation image resolutions and higher data-rate communications. A modular, electronically reconfigurable reflectarray antenna is a promising choice to maximise the ratio between the antenna's effective deployed area and stowed volume.

This PhD thesis presents the design, implementation, and validation of a wireless, beam-steerable reflectarray architecture (SATORI). The core contribution is a novel control system that decouples the X-band payload from a robust 433 MHz command link, thereby eliminating the need for complex control harnesses. This link is managed by a low-footprint, hybrid microcontroller-FPGA "interpreter" on each modular tile, which actuates low-power varactor diodes to control the reflection phase of each unit cell.

A 0.5m x 0.5m, 625-element prototype was built and validated at the ESA CATR facility. The system successfully demonstrates precise electronic beam steering to $\pm 30^\circ$ with a pointing accuracy of $\leq 0.2^\circ$. The wireless control plane proved highly reliable, where only 42 packets were lost over 13 hours of on-aperture continuous testing, validating the architecture's core premise.

The prototype achieved a peak directivity of 22.8 dBi and a peak gain of ≈ 17 dBi. The resulting $\approx 25\%$ total efficiency is a predicted and quantified design outcome, representing a deliberate engineering trade-off for using low-cost, COTS varactors to achieve continuous phase control. This ≈ 6 dB loss budget is analysed in detail, with varactor insertion loss and feed illumination efficiency identified as the primary contributors. This work successfully validates a scalable and resilient architecture for reconfigurable antennas, demonstrating its effectiveness in achieving a robust and adaptable solution. It provides a clear roadmap for future work on enhancing aperture efficiency by integrating higher-Q tuning elements.

The proposed wireless beam-steerable reflectarray offers a modular approach, featuring a more straightforward interface between the antenna and the satellite platform, as well as a promisingly small stowed volume for a high deployable area antenna. The results obtained in this work show that this reflectarray technology is competitive when compared with other solutions for large aperture antennas.

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Abbreviations

AIT	Assembly, Integration and Testing
AP-S	IEEE Antennas and Propagation Society
AUT	Antenna Under Test
AWGN	Additive White Gaussian Noise
BCH	Bose-Chaudhuri-Hocquenghem
BER	Bit Error Rate
BPSK	Binary Phase Shift Keying
CATR	Compact Antenna Test Range
CRC	Cyclic Redundancy Check
CSV	Comma-Separated Values
DC	Direct Current
EIRP	Equivalent Isotropically Radiated Power
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESA	European Space Agency
ESTEC	European Space Research and Technology Centre
EUCAP	European Conference on Antennas and Propagation
FEC	Forward Error Correction
FEUP	Faculty of Engineering of the University of Porto
FPGA	Field-Programmable Gate Array
GUI	Graphical User Interface
HFSS	High Frequency Structure Simulator
I2C	Inter-Integrated Circuit
IGARSS	IEEE International Geoscience and Remote Sensing Symposium
ISM	Industrial, Scientific and Medical
JPL	Jet Propulsion Laboratory
LEO	Low Earth Orbit
LHCP	Left-Hand Circularly Polarised
LNA	Low-Noise Amplifier
MarCO	Mars Cube One
MEMS	Micro-Electromechanical Systems
OMERA	One-Meter Reflectarray Antenna
OOK	On-Off Keying
OTA	Over-the-Air

PCB	Printed Circuit Board
PER	Packet-Error Rate
PLL	Phase-Locked Loop
PWM	Pulse-Width Modulation
RADAR	Radio Detection And Ranging
RF	Radio Frequency
RHCP	Right-Hand Circularly Polarised
RMS	Root-Mean-Square
RX	Receiver
SAR	Synthetic Aperture Radar
SEE	Single Event Effect
SLL	Sidelobe Level
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface
TID	Total Ionising Dose
TMR	Triple Modular Redundancy
TRL	Technology Readiness Level
TX	Transmitter
UART	Universal Asynchronous Receiver-Transmitter
UHF	Ultra High Frequency
URSI	International Union of Radio Science
USNC/URSI	U.S. National Committee of URSI
XPD	Cross-Polarisation Discrimination

Chapter 1

Introduction

This chapter provides a motivation and context, followed by the objectives of this thesis. Lastly, it presents the contributions and publications generated by this work, concluding with the thesis document structure.

1.1 Context and Motivation

An antenna enables energy exchange between guided currents and free-space waves, allowing information to be transmitted and received efficiently across vast distances. As radio systems scale in capability and ubiquity, there is persistent pressure to deliver higher gain, faster agility, and lower size, weight, and power (SWaP), especially in space platforms where volume and mass are at a premium.

A reflectarray is a planar reflecting aperture illuminated by a feed, whose surface is discretised into engineered elements that impose prescribed reflection phases to synthesise a desired far-field wavefront [1, 2]. Compared with parabolic reflectors, reflectarrays are thinner and mechanically simpler; compared with active phased arrays, they avoid bulky RF beamforming networks and distributed RF amplification while preserving high directivity through spatial feeding [3]. These properties make reflectarrays particularly attractive for small satellites, where deployable apertures must pack into tight stowage volumes without sacrificing electromagnetic performance [4].

Beyond fixed-beam operation, there is strong momentum toward *electronically reconfigurable* reflectarrays that steer and shape beams without moving parts. Reconfigurable surfaces promise rapid scanning/tracking, resilience to small deployment imperfections, and on-orbit adaptability for communications, remote sensing, and Synthetic Aperture Radar (SAR) [5, 3]. Reconfigurability is typically achieved by embedding tunable components in each unit cell. Such components may be varactor diodes that are robust and enable continuous control [6], RF MEMS for low-loss switched states [7], PIN-diode architectures for robust 1 to 2 bit control [8], or liquid-crystal technology for high-frequency, wide-aperture beam steering [9].

A practical system-level trade-off is the phase quantisation used at the element level: lower-bit designs simplify bias/control but can degrade gain and raise sidelobes; conversely, higher resolution improves pattern quality at the expense of hardware complexity. Recent analyses and demonstrations quantify these effects and provide valid targets (e.g., 2-bit often balancing performance vs. complexity) [10, 11]. These insights disclose the architecture of scalable, flight-ready reconfigurable reflectarrays.

However, a key bottleneck remains the control and power distribution to thousands of elements. Conventional designs route extensive harnesses from the platform to the aperture, increasing mass, integration risk, EMI susceptibility, and assembly/test effort. These disadvantages motivate a modular reflectarray with wireless configuration control to eliminate most control cabling while retaining per-cell phase programmability, which is an approach aligned with the thesis goal of delivering a high-gain, beam-steerable reflectarray with simplified integration for small platforms [4, 9, 12].

1.2 Thesis Objectives

This thesis assesses whether a reflectarray can become technologically competitive compared with phased arrays and parabolic reflectors regarding high-gain antennas. This PhD work proposes a new design of a modular X-Band reflectarray for Earth Observation and communications space applications, where its beam is wirelessly controllable. The proposed configuration enables finer beam steering tuning by dividing the reflectarray into similar, modular parts. In addition, the total wiring and integration complexity will drastically decrease by wirelessly controlling the beam, allowing for an easy assembly on a satellite platform. During this thesis, the development of different hardware prototypes tested the hypothesis proposed by simulations, resulting in a 0.5-by-0.5 meter reflectarray with individual unit cell control.

1.3 Author Contributions

There is ongoing work at the Faculty of Engineering of the University of Porto on SAR technologies for various platforms, with a primary focus on satellites. The thesis idea began by exploring ways to reduce the satellite's mass and volume while maintaining its RF performance. The proposal was submitted to the European Space Agency (ESA) through the Open Space Innovation Platform (OSIP) and was continuously iterated on with two mentors, from a preliminary idea through two evaluation phases. Throughout the process, TEKEVER and TICRA joined the team, as the thesis development and results could impact development roadmaps for both entities. The evaluation round ranked this thesis idea among the top 5 and selected it for implementation. The main contributions and novelties of this PhD are summarised below:

- A dedicated, out-of-band *wireless* control plane at 433 MHz (On-Off Keying (OOK), 9.6 kbps) that eliminates most control harnessing while preserving per-cell programmability.

- A tile-level, hybrid microcontroller–FPGA interpreter enabling low-latency, highly parallel actuation with configuration feedback.
- An end-to-end validation under payload illumination that quantifies reliability (Packet-Error Ratio (PER), Electromagnetic Compatibility (EMC) coexistence) and timing (command-to-bias latency) at the system level.
- Simulation, development and testing of all parts of a wireless reconfigurable reflectarray.
- Demonstration of the above bullets in a full 0.5×0.5 m, 25-tile, 625-cell aperture with 21 non-uniform phase states.
- A fully modular and scalable reflectarray architecture using identical, wirelessly-addressed tiles for simplified manufacturing, integration, and scaling of large antenna apertures.

Table 1.1 shows a comparative analysis between the proposed reflectarray architecture and design choices and the existing approaches available on literature.

Table 1.2 shows a comparative analysis between the contributions of this thesis and the state-of-the-art.

Compared to wired control approaches, SATORI removes the harnessing and still meets the reliability and latency objectives, validated at the antenna level.

The following conference papers have already been published and presented:

- B. Correia and S. Cunha, "Newspace SAR Constellation for Low Latency Applications," 2021 IEEE International Geoscience and Remote Sensing Symposium IGARSS, 2021, pp. 8091-8094, doi: 10.1109/IGARSS47720.2021.9554516.
- B. Correia, S. Cunha, M. Zhou, V. Cristina, B. Byrne and P. M. Iglesias, "Wirelessly Controllable Reflectarray Antenna," 2023 17th European Conference on Antennas and Propagation (EuCAP), Florence, Italy, 2023, pp. 1-5, doi: 10.23919/EuCAP57121.2023.10133056.
- B. Correia, S. Cunha, M. Zhou, V. Cristina, B. Byrne and P. M. Iglesias, "Enhancing Data Downlink Performance With Beam Steerable Reflectarray Antennas," 2023 IEEE International Geoscience and Remote Sensing Symposium IGARSS, 2023.
- B. Correia, S. Cunha, "Metamaterial Antennas for RADAR and SAR," 2023 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (AP-S/URSI)
- B. Correia, M. Santos, S. Cunha, W. Yatman, V. Cristina, B. Byrne and P. M. Iglesias, "SATORI - Smart reflectArray anTennas fOr eaRth observation," 2024 8th Workshop on Advanced RF Sensors and Remote Sensing Instruments, ESA-ESTEC, The Netherlands.
- M. Santos, B. Correia, S. Cunha, "Adaptive autofocus for precision tuning of array-type antennas using/during on-board SAR data processing," 2024 8th Workshop on Advanced RF Sensors and Remote Sensing Instruments, ESA-ESTEC, The Netherlands.

Table 1.1: This thesis vs. representative reconfigurable reflectarray approaches.

Dimension	Representative prior approaches	This work (SATORI)
Control method	Wired bias/control harnesses (row/-column buses, SPI/I ² C); per-element or per-panel cabling. System-level reliability/latency often limited in reporting. ¹	<i>Wireless</i> out-of-band control at 433 MHz (OOK, 9.6 kbps) with broadcast/unicast and 6-bit <code>TileID</code> ; strong frequency separation from X-band payload for EMC.
Addressing granularity	Centralised addressing; scalability constrained by harnessing. ¹	Per-tile addressing with broadcast refresh; graceful degradation by tile.
Reliability under illumination	Rarely quantified at aperture scale; EMC typically assumed or tested separately. ¹	Over-the-air on-aperture campaign: PER 0.168% (25,000 updates; 95% CI [0.124, 0.227] %); no observed control-payload interference.
End-to-end update latency	Rarely stated end-to-end (cmd→bias).	≈ 58 ms (RF airtime + MCU parse/SPI + FPGA update + RC settling), meeting ≤ 100 ms objective.
Aperture realisation	Reconfigurable unit cells across technologies (varactor, PIN, RF-MEMS, liquid crystal), generally with wired distribution. ²	0.5×0.5 m aperture; 25 tiles × 25 cells; varactor-loaded cell with 21 non-uniform phase steps; interpreter per tile with configuration feedback.
Beam-steering & polarisation	Numerous demos; reporting varies by element tech. ²	Electronic steering to ±30° with $\epsilon_\theta \leq 0.2^\circ$ across tested states; boresight XPD > 25 dB.
Efficiency (boresight)	Wide range depending on feed/element/quantisation. ²	$D_{pk} \approx 22.8$ dBi, $G_{pk} \approx 17$ dB (~ 25% total efficiency) with quantified loss budget.
Scaling	Often discussed conceptually; wiring becomes dominant. ¹	Tile replication with broadcast refresh; prepared for 64-tile addressing.

Notes:¹ Foundational reviews and books on reflectarrays, design and scanning: [13, 14, 5, 3].² Examples across element technologies and reconfigurable demonstrations: varactor- and tuning-based cells [15, 6], RF-MEMS-based reconfiguration [16, 17], PIN-diode switching [18, 8], liquid-crystal scanning at mm-wave [9], and large-scale optical control [19].

Table 1.2: Quantitative Benchmarking of SATORI Against State-of-the-Art Reconfigurable and Deployable Reflectarray Systems

Parameter	SATORI (This Work)	MarCO [4]	OMERA [20]	ISARA [21]	Kamoda [18]	Venneri [6]	Yang [11]
RF Performance & Geometry							
Aperture Size (m ²)	0.25 (0.5×0.5)	~0.35 (0.5×0.7)	1.0 (1×1)	~0.27 (3-panel)	0.014 (0.12×0.12)	0.09 (0.3×0.3)	0.04 (0.2×0.2)
Frequency (GHz)	9.6	8.425	35.75	26	60	11.95	10
Peak Gain (dBi)	17.0 [†]	29.2	~37*	33.5	~20	~24	~18
Aperture Efficiency (%)	25 [†]	~65	TBD	~55	~30	~40	~28
Peak Directivity (dBi)	22.8	–	–	–	–	–	–
Reconfiguration & Control Architecture							
Control Method	Wireless (433 MHz OOK)	Passive (Fixed)	Passive (Fixed)	Passive (Fixed)	Wired (MEMS bias)	Wired (Varactor bias)	Wired (PIN bias)
Active Device	Varactor (COTS)	None	None	None	RF-MEMS (Custom)	Varactor (COTS)	PIN diode (COTS)
Phase States	21 (continuous)	Fixed	Fixed	Fixed	2 (1-bit)	Continuous	2 (1-bit)
Beam Steering	±30°	Fixed beam	Fixed beam	Fixed beam	±30°	±40°	±30°
Pointing Accuracy (°)	≤0.2	N/A	N/A	N/A	TBD	TBD	~1
End-to-End Latency (ms)	58 [‡]	N/A	N/A	N/A	~10 [§]	TBD	<1 [§]
Control Harness	Zero	N/A	N/A	N/A	Full array	Full array	Full array
System Reliability & Validation							
Packet Error Rate (%)	<0.17 (95% CI)	N/A	N/A	N/A	N/A	N/A	N/A
On-Aperture Test	25,000 pkts (payload ON)	N/A	N/A	N/A	N/A	N/A	N/A
EMC Co-Existence	Validated (X vs 433 MHz)	N/A	N/A	N/A	Assumed	Assumed	Assumed
TRL	4 (Prototype)	9 (Flight)	5–6 (Breadboard)	9 (Flight)	3–4 (Lab demo)	3–4 (Lab demo)	3–4 (Lab demo)
Deployment & Scalability							
Deployment Type	Modular tiles	Folded panels	Origami hinges	3-panel fold	Rigid (lab)	Rigid (lab)	Rigid (lab)
Total Mass (kg)	TBD	~1.0	TBD	<1.5	TBD	TBD	TBD
Scalability	Tile replication (6-bit addr.)	Panel addition (mech. complex)	Panel addition (mech. complex)	Panel addition (mech. complex)	<i>Harness-limited</i> (complexity ∝ N ²)	<i>Harness-limited</i> (complexity ∝ N ²)	<i>Harness-limited</i> (complexity ∝ N ²)
Key Innovation & Contribution							
Unique Feature	Out-of-band wireless control, zero harness	CubeSat Mars relay, flight-proven	Origami-inspired, high packing efficiency (8:1)	Integrated solar cells, Ka-band CubeSat flight	Low-loss MEMS (<0.25 dB loss), high isolation	Single varactor, continuous phase control	Optimized 1-bit, quantization study (phase error)

Notes:

[†] *Quantified design outcome:* 25% efficiency represents a deliberate trade-off using low-cost COTS varactors to achieve continuous phase control and wireless operation. Detailed loss budget: varactor insertion loss (~3 dB), feed illumination efficiency (~2 dB), spillover (~1 dB). Comparable to other varactor-based systems (Venneri: 40%, Yang: 28% for quantised control).

[‡] *End-to-end latency:* RF airtime (433 MHz OOK @ 9.6 kbps) + MCU decode + SPI transfer + FPGA PWM update + RC filter settling ($\tau = 10$ ms). Meets <100 ms objective for SAR stripmap mode reconfiguration between passes.

[§] *MEMS/PIN switching time only;* does not include command routing, decoding, or settling. SATORI latency is system-level (includes full control stack).

* Theoretical gain assuming ideal $\lambda/2$ spacing and perfect phase. OMERa measured performance pending full deployment validation.

- B. Correia, S. Cunha, W. Yatman, V. Cristina, B. Byrne and P. M. Iglesias, "RF analysis of a wireless controlled reconfigurable reflectarray antenna," 2024 42nd ESA Antenna Workshop, ESA-ESTEC, The Netherlands.

The following journal paper was submitted:

- B. Correia, S. Cunha, W. Yatman, B. Byrne and P. M. Iglesias, "Wirelessly Controllable Modular Reflectarray for Satellite High-Gain Earth Observation and Communication Antennas," in IEEE Aerospace and Electronic Systems Magazine - accepted.

The "Metamaterial Antennas for RADAR and SAR" paper consisted of a preliminary study for antenna systems miniaturisation for SAR applications, and the authors decided to publish it to justify the importance of the proposed thesis.

1.4 Report Objectives and Document Structure

This PhD thesis report includes eight chapters. The structure is as follows:

- Chapter 1 presents the motivation, contributions, and document structure of this work.
- Chapter 2 provides the fundamentals of the reflectarray needed to comprehend this thesis, positioning the technology, comparing it to phased arrays and parabolic reflectors.
- Chapter 3 shows the proposed reflectarray architecture, starting from the active unit cell and continuing to the preliminary budgets that justify the design options for the following stages.
- Chapter 4 presents the hardware development, focusing on unit cell and reflectarray simulations. It shows the optimisation process for different steering angles, including uncertainty quantification due to the non-linear behaviour of the chosen active devices, as well as the control PCB that will control the reflectarray.
- Chapter 5 explains the RF protocol used to control each unit cell of the reflectarray individually.
- Chapter 6 describes the written software for the microcontroller and application that controls the reflectarray and the FPGA firmware.
- Chapter 7 exposes the manufacturing, ground support equipment and the results obtained through measurements at FEUP and ESA facilities.
- Chapter 8 presents this thesis's conclusions and future work.

Chapter 2

Reflectarray State of the Art and Fundamentals

This chapter provides the reader with an introduction to reflectarray principles and the state of the art, presenting different unit cell configurations to achieve various radiation properties, such as multi-frequency operation or dual-polarisation. This chapter also explains how active devices can contribute to the reconfigurability of reflectarrays and the impact of the mechanical design on space applications. Finally, it shows the latest trends in reflectarray applications.

Before going into the principles of reflectarray antennas, this chapter presents the two major conventional architectures historically employed for high-gain applications: the phased array and the parabolic reflector. For decades, these technologies have been the baseline of satellite communications, radar systems, and Earth observation missions. A critical analysis of their respective operational advantages and technological limitations to highlight the technology this thesis proposes and specific design trade-offs offered by the wireless-controlled reflectarray topology, which is the central focus of this thesis.

2.1 Phased Array Antennas

In many applications, single-element antennas cannot provide highly directive radiation patterns, much less reconfigurable steerable patterns. When designing antennas for space applications, it is sometimes desirable that the radiation is stronger in specific directions and pattern nulls exist in others. This can reinforce signal strength from/to the desired devices and significantly reduce the reception/transmission to other devices capable of receiving the same signal. Figure 2.1 shows the geometry of an $M \times N$ planar antenna array with isotropic antenna elements lying in the x - y plane.

Phased arrays synthesise directive patterns by controlling the complex excitations of many radiating elements, where the radiated field factorises into an element pattern and an array factor; a progressive phase across the aperture steers the main beam without moving parts [23, 24]. True-time-delay beamforming techniques mitigate beam squint relative to phase-only steering for

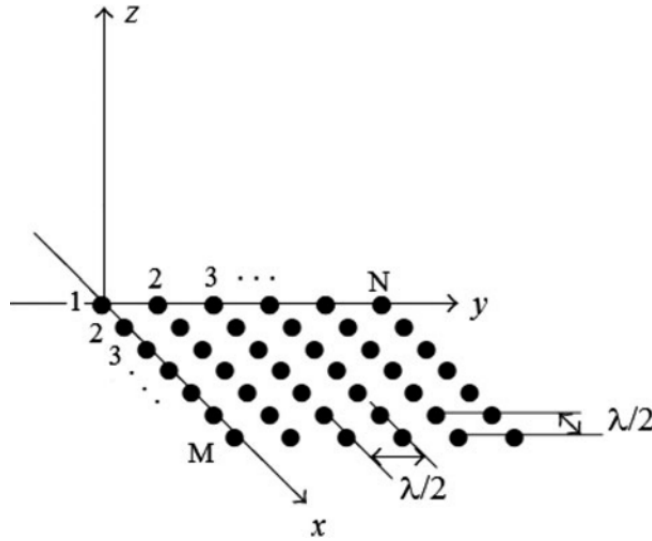


Figure 2.1: Geometry of a planar antenna array with isotropic radiators. [22].

wide bandwidths. Classic array behaviour links beamwidth to λ/D (wavelength λ divided by aperture size or array diameter D) and sidelobes to illumination taper, while element spacing controls grating-lobe. The mutual coupling and feed/distribution networks perturb the idealised array factor and must be accounted for in modelling and calibration [23, 25, 18].

The most significant advantage of phased array technology is the capability for rapid electronic beam steering. Beams can be repositioned in microseconds, enabling advanced functionalities such as beam shaping to enable different SAR modes and instantaneous hopping between different ground stations, all infeasible with mechanically steered systems. Active electronically scanned arrays (AESAs) provide a high degree of reliability, as the failure of a small number of individual transmit/receive (T/R) modules does not lead to a catastrophic failure of the entire antenna but rather a gradual and predictable "graceful degradation" of its performance.

However, this functional flexibility significantly increases the system complexity and power consumption, as each radiating element in the array requires a signal, necessitating highly complex and often lossy beamforming networks, demanding more RF power to compensate. Active phased arrays, in particular, consume substantial DC power, and the resulting waste heat from thousands of T/R modules requires thermal management systems. Finally, the high number of components, such as radiating elements, phase shifters, amplifiers, and control circuits, makes phased arrays considerably more complex and expensive to manufacture, integrate, and test when compared to reflector antennas of an equivalent aperture size. The reflectarray architecture directly addresses these critical drawbacks by ingeniously combining the structural simplicity of a reflector, using a single space-fed source to eliminate the complex feed network, with the electronic beam agility of a phased array, achieved by electronically manipulating the phase of each re-radiating element on its surface [26, 5, 27, 28].

In summary, compared with reflectarrays, AESAs excel in rapid, wide-angle scanning and bandwidth. Contrarily, reflectarrays concentrate RF power at a single feed and avoid distributed

RF beamforming networks, lowering insertion loss and simplifying thermal management [1, 2]. In the proposed wireless-controlled reflectarray architecture, complex RF generation is centralised and only low-power control reaches the tiles, allowing for preserving electronic agility at the surface while easing harness and thermal budgets relative to a conventional AESA [8, 16].

2.2 Parabolic Reflector Antennas

The parabolic reflector is a high-gain antenna technology and has been a subject of extensive study and refinement since its beginning, widely used for space applications [29, 30]. Its operation principle is based on a shaped parabolic conducting surface reflecting incident electromagnetic waves from a single feed antenna, positioned at the reflector's focal point. This geometric arrangement transforms the original spherical wavefront from the feed into a planar wavefront, forming a high-gain beam. Figure 2.2 shows different possible geometries for reflector antennas.

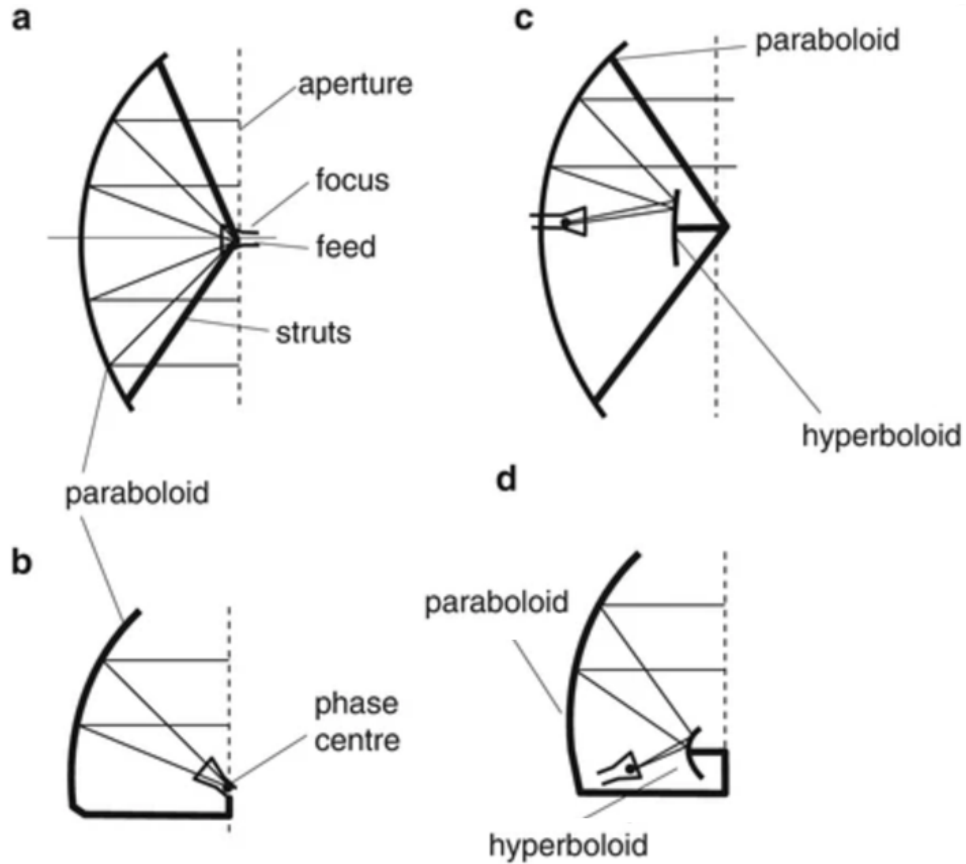


Figure 2.2: Reflector geometries; (a) symmetrical paraboloid; (b) offset parabolic reflector; (c) symmetrical Cassegrain; and (d) offset Cassegrain. [31]

One of the advantages of this architecture is its potential for high aperture efficiency, which can exceed 65% in well-designed systems with no significant system constraints [32], making parabolic reflectors effective at converting an antenna's physical aperture area into realised gain.

Furthermore, because the reflecting surface is a non-resonant structure, its performance is primarily limited by the operational bandwidth of the feed antenna. This effect allows a single reflector to achieve broad bandwidths, frequently spanning entire frequency bands such as the Ku-band for satellite communications. Due to its passive nature and physical separation from the active feed electronics, parabolic reflectors can withstand high power levels, a critical requirement for high-power satellite downlinks and radar applications [33].

Despite these significant advantages, the parabolic reflector has drawbacks, many of which have become more pronounced with the beginning of smaller satellite platforms. From a generic point of view, prime-focus paraboloids are efficient but suffer feed blockage; offset reflectors remove blockage at the expense of mechanical asymmetry. Dual-reflector Cassegrain/Gregorian systems place the feed near the structure while shaping aperture phase and amplitude; shaped-surface designs tailor patterns without severe feed taper penalties [34, 35, 36]. For the specific case of space applications, the most important limitation is its inherently three-dimensional, non-planar geometry. This results in a bulky and volumetric structure that is challenging to stow within the constrained fairings of a launch vehicle and difficult to integrate onto the satellite bus. Consequently, beam steering is almost exclusively achieved through mechanical means, such as actuating the entire dish assembly or the feed structure. These mechanical gimbal systems are not only heavy and slow, but also power-intensive. Still, they are also power-intensive and represent a significant single point of mission failure due to the risks of mechanical wear, lubricant degradation in the vacuum of space, and pointing errors. As expected, the deployment challenge is higher for larger apertures, necessitating complex and high-risk mechanisms that involve unfurlable mesh surfaces, hinges, and booms, which add considerable mass, cost, and complexity to a satellite mission [37, 38, 39, 4, 40].

Reflectarrays appeared as an innovative solution, aiming to replicate the high-gain performance of a parabolic dish but within a planar, low-profile, and electronically steerable form factor, as a solution to these mechanical and volumetric challenges.

A reflectarray bridges phased array and reflector technologies as it is a quasi-planar, discretised aperture illuminated by a single feed, where each cell imparts a designed reflection phase. This yields planar manufacturability, compact stowage, and, with active cells, allows electronic steering without gimbals, in exchange for managing dispersion and bandwidth [1, 2]. As it will be shown in the following subsections, there are designs demonstrating dual-polarisation, broadband behaviour suitable for telecom satellites [41]; electronically controlled cells using PIN diodes or MEMS provide beam switching and reconfiguration [8, 16]. In summary, phased arrays maximise agility and bandwidth at higher power/thermal complexity; classic reflectors maximise aperture efficiency with mechanical steering; reflectarrays offer a pragmatic middle ground with high gain-per-kilogram, small stowed volume for high deployed area ratio, and electronically steerable beams when dispersion and polarisation are carefully engineered [41, 8].

2.3 Fundamentals of Reflectarray Antennas

As previously mentioned, active reflectarray antennas combine the phased arrays' beam-steering capabilities with reflectors' structural simplicity and low-profile nature. By removing complex feed networks and bulky mechanical steering systems with a flat or slightly curved surface of engineered elements, reflectarrays offer a compact and cost-effective solution for directional radiation. They usually consist of a flat array of passive or active elements illuminated by a feed antenna, typically a horn, placed at an optimised location that acts as the focal point of a parabolic reflector. Each array element imposes an appropriate phase shift on the incident wavefront, enabling the reradiated fields to interfere constructively with the desired far-field direction.

The primary reflectarray design objective is compensating for the spatial phase delay caused by the varying path lengths from the feed to each element. By adjusting the local reflection phase, the reflectarray forms a beam with desired characteristics - such as directionality, shape, or polarisation - without mechanical steering. Figure 2.3 illustrates this mechanism.

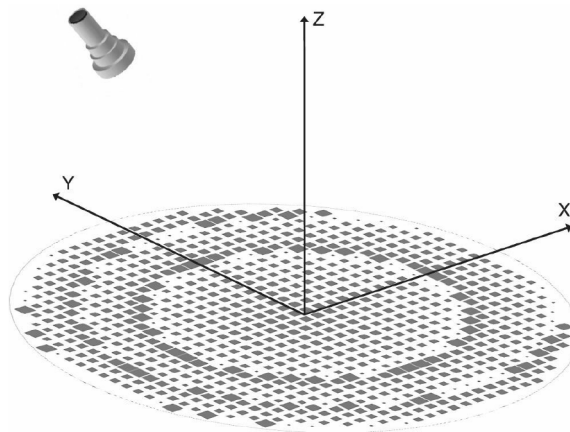


Figure 2.3: Typical geometry of a planar reflectarray antenna. [14]

Historically, the reflectarray concept was introduced by Berry *et al.* [42], who used short-circuited waveguides of different lengths to control the reflection phase of each cell. Later, the first printed reflectarray was proposed in [43], utilising microstrip technology to reduce manufacturing complexity and cost. Since then, printed reflectarrays have become the most widely adopted configuration due to their planar nature, integration capabilities, and compatibility with standard PCB processes.

Traditional phased arrays rely on electronic phase shifters, while reflectarrays achieve similar functionality by adjusting the geometry or loading of each passive element to obtain the required phase delay. The feed does not necessarily need to be centred (as shown in Figure 2.3), and array elements are typically assumed to lie in the far-field of the feed, enabling spherical-wave approximation for local excitation [14]. This effect creates a spatially varying incident phase that requires precise compensation to produce a planar (collimated) wavefront in the desired direction.

The required reflection phase ϕ_i at each element position is governed by:

$$\phi_i + \phi_0 - k_0 (r_i + \bar{r}_i \cdot \hat{r}_0) + \Delta\phi_{\text{coupling}} = 2\pi N, \quad (2.1)$$

Where r_i is the distance from the feed to the i th element, ϕ_0 is an arbitrary reference phase, $\bar{r}_i$ is the vector from array centre to i th element, $\hat{r}_0$ is the unit vector in beam direction, k_0 is the free-space wavenumber, $\Delta\phi_{\text{coupling}}$ compensates for mutual coupling between adjacent elements, which can distort the intended phase distribution if not accurately modelled or calibrated, and N is an integer accounting for phase periodicity.

Unlike continuous parabolic surfaces, reflectarrays approximate the required phase distribution using discrete elements on a Cartesian grid. This results in pixelated approximations of ideal profiles [14]. Figure 2.4 (a) illustrates how spatial delay and progressive phase are accounted for to obtain the desired aperture phase distribution when the feed phase centre is placed along the z-axis at a distance of 170 mm from the aperture. The array is designed to have a beam in the broadside direction, hence no progressive phase is required, as shown in (b). The reflectarray discretised apertures and continuous phase distributions are shown in (c) and (d). The phase moves outwards from the array's centre, completing almost three complete phase cycles (0 to 2π).

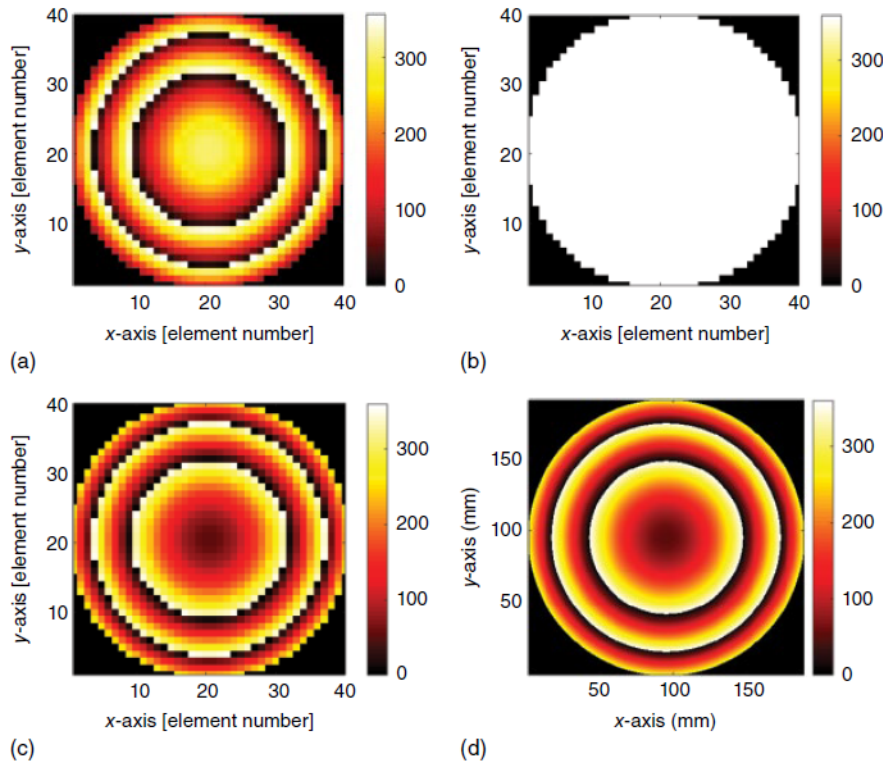


Figure 2.4: Phases on aperture with centred feed and broadside beam: (a) spatial delay; (b) progressive phase; (c) discretised phase distribution; (d) continuous aperture phase. [14]

As previously mentioned, reflectarrays offer several advantages: they eliminate complex feed networks required in phased arrays, provide planar construction, and allow large apertures with

lower mass. However, they present challenges in achieving large bandwidths, polarisation control, and accurate phase control under varying environmental conditions.

Recent advances include:

- Bandwidth enhancement techniques such as multi-resonant elements [44].
- Metasurface-based designs offering broader operational ranges [45].
- Machine learning-aided optimisation for unit cell design [46].
- Space-qualified designs for satellite applications [21].

These developments aim to overcome limitations and extend reflectarrays' capabilities into new application domains like 5G/6G communications and terahertz systems.

2.4 Reflectarray Unit Cells

A reflectarray is a quasi-periodic structure where each unit cell induces a controlled variable phase shift to an incoming wavefront to form and point it to obtain the desired radiation pattern. These unit cells can be printed or volumetric structures, like microstrip patches, dipoles, dielectric resonators, or loop-based geometries [47]. Printed structures offer low-cost manufacturing, a planar profile, and compatibility with standard PCB processes, making them widely adopted.

To accurately model reflectarrays, it is necessary to account for inter-element mutual coupling and realistic boundary conditions. Additionally, implementing microstrip solutions requires proper impedance matching between the line and the radiating patch to avoid undesired reflection modes that degrade the beam quality.

A fundamental design challenge is to achieve a full 360° phase tuning range with minimal insertion loss and good reflection efficiency. At the same time, the unit cell topology selection depends on application requirements such as bandwidth, polarisation, scanning capability, and operating frequency. This section explores some examples of unit cell architectures, from classical delay lines to modern multiband and dual-polarised configurations.

2.4.1 Phase/Time Delay Line Unit Cell

This type of unit cell converts the incident wave into a guided wave that propagates along a transmission line terminated in a short or open circuit, inducing a reflection. The corresponding phase shift is approximately proportional to twice the line length:

$$\phi_{\text{delay line}} = 2kl \quad (2.2)$$

Here, l is the physical length of the delay line, and k is the propagation constant of guided waves. A differential phase distribution is achieved by varying l throughout the array. Although this configuration is simple and intuitive, practical challenges include radiation loss in bends,

impedance mismatches caused by stub resonances and ground plane reflections. Figure 2.5 shows an example of a unit cell with a physical length delay line.

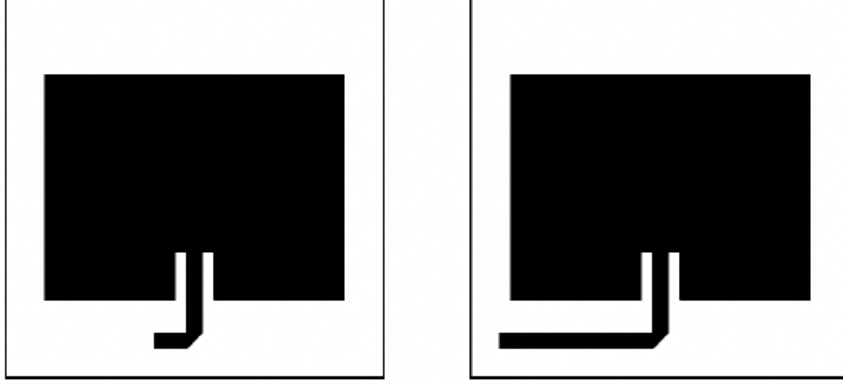


Figure 2.5: Schematic models of reflectarray patch elements with attached phase/time-delay lines of two different lengths. [14]

2.4.2 Variable Size Unit Cell

This method adjusts the element's physical dimensions of each unit cell to control its resonance frequency, modulating the reflected phase. It is possible to obtain a near-linear phase variation by scaling a resonant structure's width, length, or diameter. This concept was initially applied to printed dipoles [48] and later extended to rectangular microstrip patches [49]. Figure 2.6 presents a possible unit cell design where the reflection phase variation is achieved through changing its size.

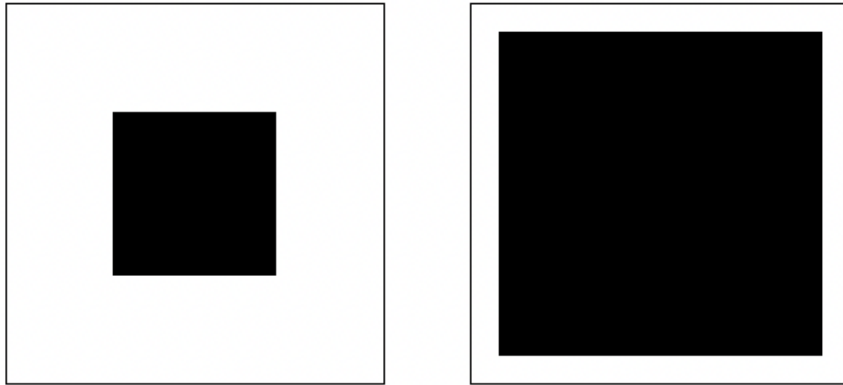


Figure 2.6: Schematic models of variable size reflectarray square patch elements of two different sizes. [14]

Although a complete 360° phase coverage is theoretically achievable at resonance, there are practical limitations such as mutual coupling, dielectric losses, and inter-element spacing that reduce the usable range. Additionally, the resonator's quality factor (Q) determines the steepness

of the phase slope, where high- Q elements result in sharper phase transitions. Compared to a delay-line-based approach, changing the size of a square patch offers compact implementation but may require precise fabrication to maintain uniformity across the array. Figure 2.7 represents the S-curve of a reflectarray patch unit cell. It gives the reflection phase as a function of the patch size for a specific incident angle for both V- and H-polarisations.

Recent developments include elliptical, polygonal, or compound geometries to enhance polarisation capabilities or broaden the tuning range [50].

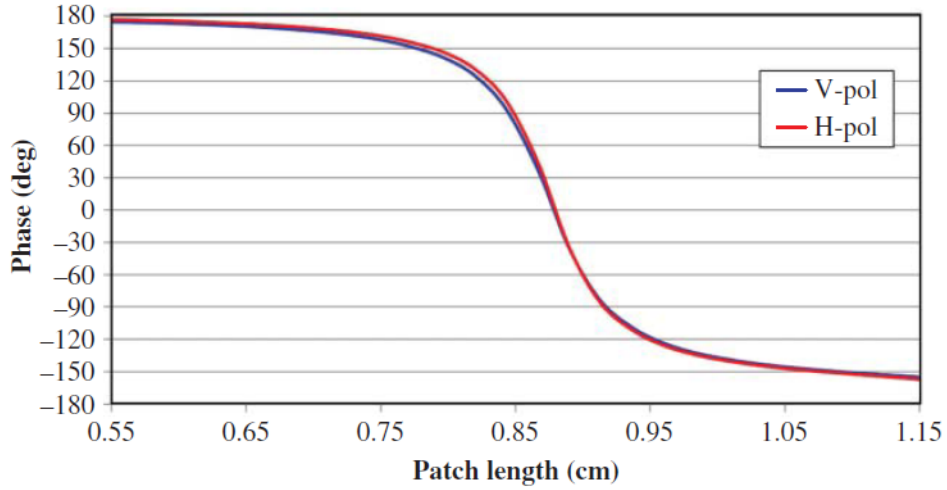


Figure 2.7: Simulated S-curve of the reflectarray patch unit cell showing reflection phase as a function of patch size for V- and H-polarisations, illustrating dual-polarisation sensitivity. [4]

2.4.3 Variable Rotation Angle Unit Cell

This technique, applicable to circularly polarised designs, controls the reflected phase by physically rotating the resonant element. Considering a right-hand circularly polarised (RHCP) incident wave,

$$\vec{E}_i = E_0 (\hat{x} + j\hat{y}) e^{jk_0 z} e^{j\omega t}, \quad (2.3)$$

the reflected wave has the opposite circular polarisation and acquires an additional geometric phase that depends on the rotation angle ψ of the element:

$$\vec{E}_r(\psi) = \Gamma E_0 (\hat{x} - j\hat{y}) e^{-jk_0 z} e^{j\omega t} e^{j2\psi}, \quad (2.4)$$

where Γ represents the reflection coefficient of the unit cell. Therefore, a physical rotation of the resonant element by an angle ψ introduces a geometric phase shift in the reflected field given by

$$\Delta\phi = 2\psi. \quad (2.5)$$

This principle relies on the geometric phase [51] and is represented in Figure 2.8. Its simplicity and potentially low-loss implementation make it attractive for reflectarray designs. However, the technique is inherently associated with circularly polarised operation and requires accurate fabrication and orientation of anisotropic resonant elements.

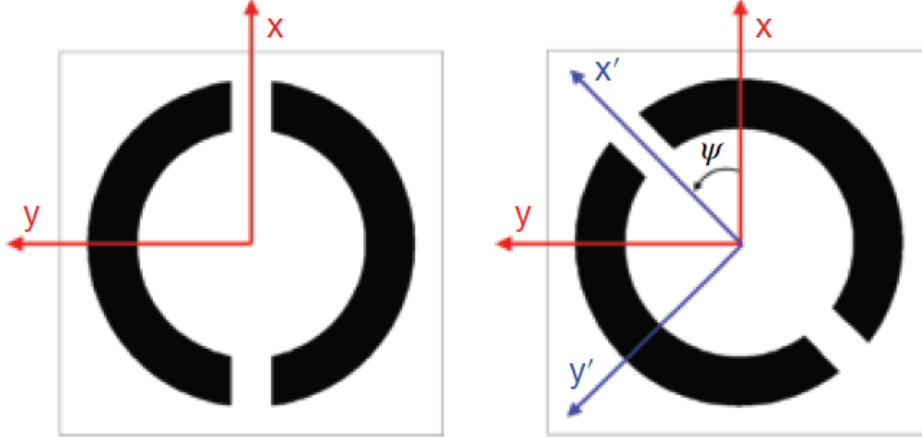


Figure 2.8: Schematic model of a circularly polarised unit cell. Left: reference element with 0° phase shift. Right: rotated element inducing a 2ψ phase shift. [14]

2.4.4 Dual-Polarization Unit Cell

In remote sensing and communication systems, dual-polarisation capability enhances link reliability and enables techniques such as polarimetric SAR imaging. Dual-polarised unit cells support independent phase control in orthogonal polarisations while minimising cross-coupling.

Two main design strategies exist:

- Orthogonal dipole pairs or crossed patches, as presented in [41]. The proposed cell comprises four dielectric layers (A, B, C, and D) with printed dipoles. The phase-shift for Y-polarisation is controlled at different frequencies by adjusting the lengths of the three dipoles printed on top of layer B and the one on top of layer C, as shown in Figure 2.9. Similarly, the phase for X-polarisation is controlled by the lengths of the four dipoles printed in the X-direction. The novelty of this element is that it combines lateral and stacked coupled dipoles to increase the phase range and number of resonances, while keeping an independent phase control for each polarisation.
- Multi-layered structures with polarisation-sensitive elements [52]. The authors propose an antenna configuration that is an elliptical reflectarray panel with 1110mm x 1090mm axes. The dimensions of the reflectarray cell are 10mm x 12mm, and the reflectarray elements are placed in a grid of 110 x 90 for X-polarisation and 109 x 89 for Y-polarisation. Figure 2.10 shows the reflectarray cells, based on four dipoles for each polarisation in two layers.

Some advanced designs offer multiple tuning degrees of freedom for each polarisation, enabling frequency agility and polarisation diversity. The unit cell optimisation involves full-wave simulation and parametric tuning to minimise inter-port isolation and maximise reflection phase coverage.

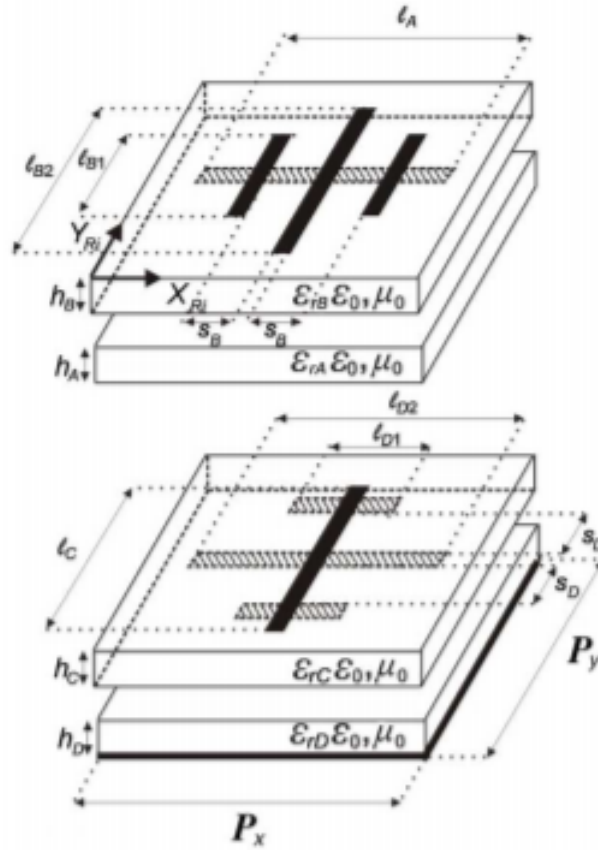


Figure 2.9: Dual-polarisation reflectarray element composed of four coplanar dipoles per polarisation layer. Geometry supports low cross-polarisation levels and is optimised for transmit/receive Ku-band operation. [41]

2.4.5 Multi-Frequency Unit Cell

Reflectarrays are intrinsically narrowband due to the resonant nature of their elements. Researchers have developed unit cells capable of operation at two or more frequency bands to overcome this by:

- Stacking multiple resonant structures (multi-layer)
- Embedding nested or concentric resonators on the same layer (coplanar)

Key examples include:

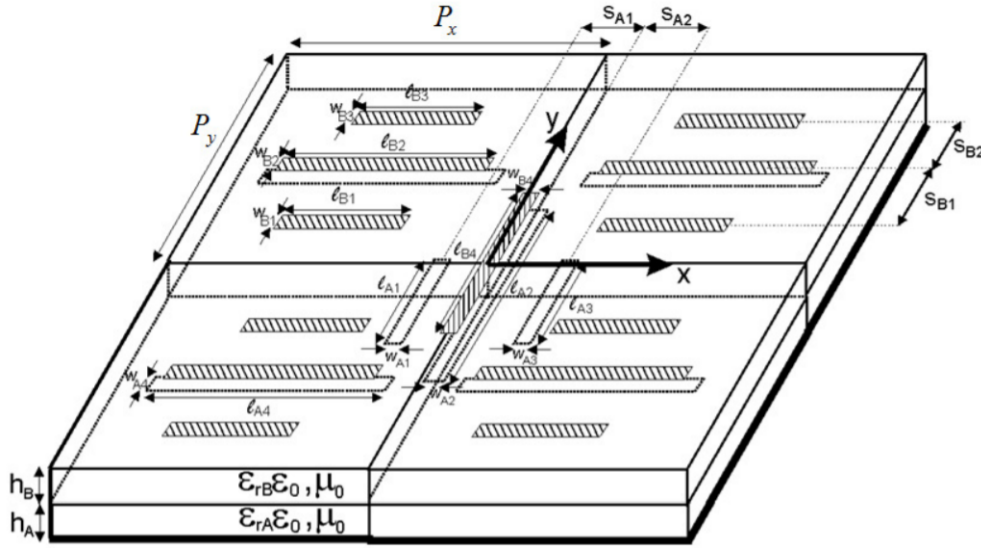


Figure 2.10: Alternative dual-polarisation reflectarray element using four dipoles per polarisation across two metallization layers, optimised for beam shaping. [52]

- Phoenix elements with scalable geometries for 10/20 GHz dual-band use [53]. As depicted in 2.11(a), the proposed Phoenix element comprises two square loops and a square patch. The sizes of the outermost loop and innermost patch are fixed. When the middle loop changes its size, the element repeats itself after a complete cycle, as illustrated in Figure 2.11(b), thus achieving the rebirth capability with a full 360° phase coverage. Although the Phoenix element has a similar geometrical shape to the triple square loop element, its operation mechanism is entirely different, as it adjusts different geometrical parameters.
- Mixed-element patches for Ka-band up/downlinks [54]. The authors presented the results of numerical simulation of the proposed unit-cell shown in Figure 2.12. The dimensions of the proposed unit-cell were optimised for low loss and enough phase variations versus $L1$ and $L2$ for TE and TM-polarised incident angles of up to 30° .
- Triple-resonant loop-patch combinations for enhanced bandwidth [55]. Figure 2.13 depicts the configuration of the triple-resonance phasing element. The element has five independent geometrical parameters, namely, $W1, W2, W3, d1$ and $d2$. The authors found that $W1$ and a parametric sweep between 0.5 and 0.8 with 0.01 intervals are the representative parameters, which not only represent the element configuration, but also provide sufficient phase responses for reflectarray design.
- Polarisation-frequency combined designs using split-ring resonators [56]. As shown in Figure 2.14, the unit cell consists of a cross dipole (for the lower band) and a split rectangular ring (for the upper band) printed on a single-layer substrate with permittivity 2.2 and thickness 0.787 mm. In the unit cell, the splits in the rectangular element allow for avoiding overlapping as each element's size changes to compensate for the phase of the incoming wave.

These designs exploit resonance multiplicity to achieve broader phase coverage and better impedance matching across bands. For example, stacked resonators enable independent tuning at distinct frequencies by varying their inductive and capacitive loading:

$$f_n = \frac{1}{2\pi\sqrt{L_n C_n}}$$

Where f_n is the resonance frequency of the n -th resonator, L_n is its inductance, and C_n is its capacitance.

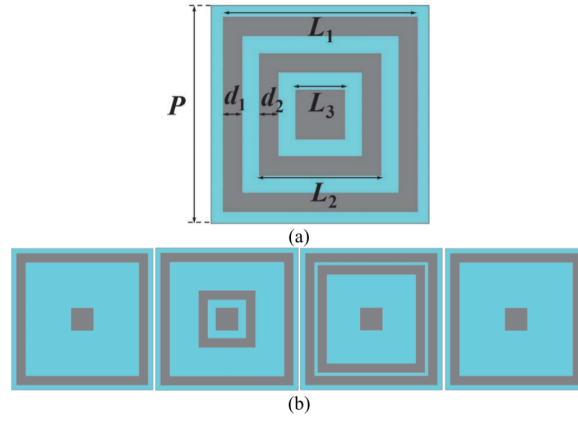


Figure 2.11: Phoenix element for dual-band reflectarrays: (a) layout and parameters; (b) element size adjustment mechanism to tune reflection phase at both bands. [53]

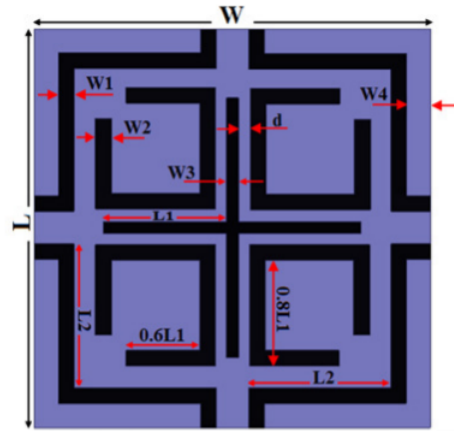


Figure 2.12: Ka-band dual-polarisation unit cell composed of crossed dipoles and rectangular/truncated ring resonators for phase tuning at 20 and 30 GHz. [54]

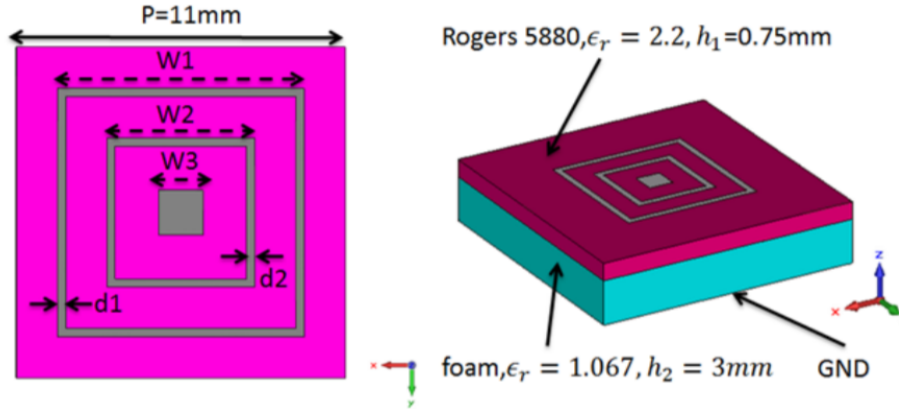


Figure 2.13: Triple-resonant unit cell using square loops and an internal patch to enable broadband dual-frequency operation with dual linear polarisation. [55]

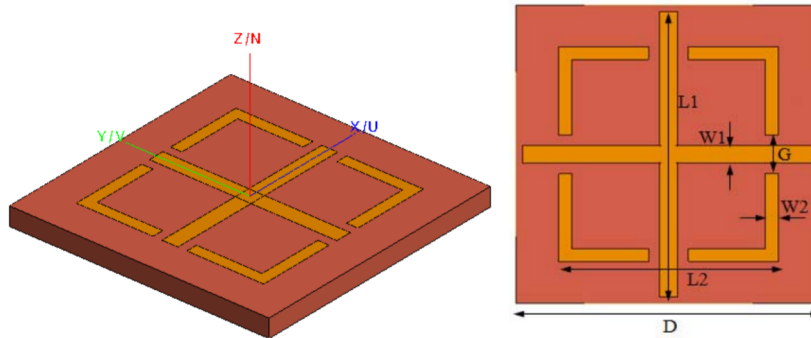


Figure 2.14: Dual-band, dual-polarised reflectarray unit cell using cross-dipole and split-ring elements for operation near 12 and 14 GHz. [56]

These designs exploit resonance multiplicity to achieve broader phase coverage and better impedance matching across bands. Design trade-offs include fabrication complexity, increased thickness, and mutual interference between resonances.

Tightly coupled dipole arrays [57], multi-resonant apertures [58], and metamaterial unit cells are some recent trends exploring broadband techniques.

Independently of the chosen unit cell, material choices and fabrication tolerances play an essential role in high-frequency implementations. Substrate selection must consider dielectric losses, thermal expansion, and mechanical robustness, particularly for space-borne or millimetre wave applications.

2.5 Techniques for Reflectarray Electronic Beam Steering

The demand for agile, electronically reconfigurable reflectarrays has grown significantly in recent years, driven by advances in satellite communications, terrestrial mmWave networks, remote

sensing, and radar systems [59]. These systems benefit from rapid beam steering, area coverage flexibility, and robustness against interference - making them ideal for dynamic environments where mechanical steering is impractical.

Electronic reconfiguration of reflectarrays typically relies on solid-state devices such as PIN and varactor diodes, field-effect transistors (FETs), and Micro-Electromechanical Systems (MEMS). These tuning mechanisms change the reflection phase of each unit cell by modifying either the geometry or the impedance loading in real time. This section reviews key enabling technologies for implementing beam-steerable reflectarrays.

2.5.1 PIN Diodes

PIN diodes operate as RF switches controlled by a DC bias voltage, effectively presenting either a low (ON) or high (OFF) impedance state. This enables binary or quantised control of the reflection phase.

In [60], a 60-GHz reconfigurable reflectarray employed microstrip patches with integrated stubs loaded with single PIN diodes. The ON/OFF states induced a 180° phase shift, functioning as single-bit phase shifters. This configuration offers a balance between cost, switching speed, and integration simplicity, making it particularly suitable for low-bit (1- to 2-bit) phase quantisation reflectarrays where fine resolution is not critical.

In a more advanced implementation [8], an X-band beam-switching reflectarray was constructed with 244 elements on a circular aperture. Each sub-array utilised pairs of aperture-coupled patches and delay lines, enabling a reduction in the number of electronic components. Beam switching occurred by biasing different subsets of diodes, allowing the main beam to scan across a 180° in the azimuthal plane. A third neutral state was implemented with all diodes reverse-biased, yielding a broadside beam.

Other solutions allow for more than 180° reconfigurability at the cost of having more than one PIN diode connected at each unit cell. Although PIN diodes can have low RF losses, their power consumption is at least an order of magnitude higher compared to varactor diodes, which may be an issue for large aperture reflectarrays.

2.5.2 Varactor Diodes

Varactor diodes offer tunable capacitance controlled by reverse-bias voltage, enabling continuous phase modulation. When integrated into a resonant element, the varactor modifies the effective electrical length and, thus, the reflection phase.

Reference [61] presents a C-shaped microstrip patch loaded with a single varactor diode. A DC bias from 0 to 20 V varied the junction capacitance from 3 pF to 0.14 pF, providing a broad phase tuning range. Compared to PIN diodes, varactors provide continuous tuning but at the cost of increased sensitivity to temperature variations, voltage drift, and increased insertion loss due to nonlinearity.

Varactor-loaded reflectarrays are attractive for continuously steerable systems, particularly when fine angular resolution is required.

2.5.3 MEMS Devices

MEMS (Micro-Electromechanical Systems) switches or capacitors are promising due to their low loss, low power consumption, high isolation, and miniaturisation potential. However, their slower switching speeds (typically microseconds), limited power handling, and packaging complexity remain barriers to widespread adoption.

Reference [16] presents a digitally tunable reflectarray with a double-cross loop element loaded with five MEMS capacitors. This configuration allowed 32 discrete reflection phase states, achieving fine resolution across the full 360° range. The system also leveraged phase redundancy to suppress frequency dispersion.

MEMS-based reflectarrays are particularly advantageous for millimetre-wave applications due to their high Q-factor, low loss, and fine phase resolution. However, reliability under thermal cycling, switching latency and long-term mechanical fatigue remain open research challenges.

Table 2.1 presents a summary of the key characteristics of each device.

Table 2.1: Comparison of key characteristics for electronic tuning technologies used in reconfigurable reflectarrays, including phase resolution, power consumption, switching speed, and integration complexity [62].

Parameter	RF MEMS	PIN Diode	Varactor Diode
Costs	Medium	Low	Medium/High
Loss	Very Low	Low	High
Power Consumption	Negligible	High	Negligible
Speed	Microseconds	Nanoseconds	Nanoseconds
Technology Readiness	Foundry required	Market available (COTS)	Market available (COTS)
Mounting Complexity	Low	Low	Low
Biasing Complexity	High voltage (60V)	Low voltage (1V)	Medium voltage (0–30V)

2.5.4 Emerging Reconfiguration Technologies

Eliminating complex and failure-prone wiring harnesses is a primary driver for innovation in large-aperture reconfigurable antennas. While the preceding sections focused on electronically controlled elements requiring direct bias lines, the literature explores several alternative control paradigms. These methods deliver control signals and/or energy to the unit cells without a physical electrical connection, enhancing scalability and deployment reliability for space applications. Also, in addition to the conventional diodes and MEMS, new materials and control strategies are pushing the limits of reconfigurable reflectarrays:

- **Liquid Crystals:** Enable continuous, low-voltage tuning, but have slow response times. Best suited for quasi-static beam shaping [63].
- **Optical Control:** Some research has focused on using optical signals to achieve wireless control of reflectarray elements. The fundamental principle relies on the photoconductive effect, where illuminating a semiconductor material with light of an appropriate wavelength generates charge carriers, drastically changing its conductivity. In a typical implementation, a laser or other light source illuminates a gap in a microwave transmission line or a switching element like a PIN diode. This illumination effectively closes the switch, altering the element's resonant properties and, thus, its reflection phase [19, 64]. Optical control offers several advantages, including high isolation between the control signal (light) and the RF signal and immunity to electromagnetic interference. Researchers have demonstrated optically activated phase shifters and reconfigurable antennas using this principle. The control can be delivered by a scanning laser beam or by illuminating the entire array with a patterned light source, removing the need for a complex wire-routing network on the array surface. However, this paradigm presents its challenges for space applications, including the potential degradation of photosensitive materials due to radiation, the need for a precise and reliable optical distribution and pointing system, and potential interference from direct solar illumination [65].
- **Phase Change Materials (PCMs):** Emerging material science offers another path to wireless reconfiguration through the use of phase-change materials (PCMs) like Vanadium Dioxide (VO_2) or Germanium-Antimony-Tellurium (GST). These materials exhibit a significant change in their electrical properties when an external source alters their material phase, such as heat or an optical pulse. For example, VO_2 undergoes a metal-insulator transition when heated above a critical temperature, drastically changing its resistivity [66, 67]. Integrating PCMs into the reflectarray unit cell allows the reflection phase to be switched by thermally or optically addressing the cell. This provides for bistable, non-volatile phase states, meaning the array can maintain its configuration without continuous power application. The main challenges for this technology include the energy required to induce the phase transition, the speed of the transition, and ensuring uniform and repeatable thermal control across a large array in a space environment with extreme temperature variations [68].
- **Mechanical Reconfiguration:** Another approach to reconfigurability avoids complex on-array electronics by employing mechanical actuation to alter the unit cells' geometry physically. Micro-motors or piezoelectric actuators can change the physical height of a reflecting patch relative to its ground plane, thereby tuning its reflection phase through mechanical adjustment. Recent innovations include electro-mechanical systems with cam-shaped actuators beneath each unit cell to provide continuous phase modification [69, 70]. Mechanically reconfigured arrays offer the potential for low-loss phase shifting and high-power handling, as the RF path does not contain lossy semiconductor devices. However, they typically suffer from slower switching speeds due to mechanical inertia, higher power consumption for the

actuators, and concerns about long-term reliability in the harsh space environment, including issues like stiction and lubricant degradation [71].

- Other wireless control architectures that eliminate the need for bulky DC bias lines using RF power harvesting or optical control, such as [72].

By reviewing these alternative wireless paradigms, it becomes clear that the choice of a control architecture involves a complex trade-off between performance, complexity, power consumption, and environmental robustness. The RF-based wireless control link proposed in this work is positioned as a pragmatic and robust solution specifically for space applications, aiming to circumvent the primary drawbacks of these alternatives, such as the radiation and solar sensitivity of optical systems, the mechanical reliability concerns of actuated systems, and the thermal management challenges of PCMs.

2.5.5 Phase Quantisation and Performance Trade-offs

Many practical reflectarrays use quantised phase states (e.g., 1-bit to 3-bit resolution) to simplify control electronics. While fewer states reduce system complexity, they can introduce phase errors leading to gain degradation and increased sidelobe levels.

Studies [11] show that 2-bit (four-state) designs offer a good trade-off between performance and complexity. Higher resolution enables sharper beams and reduced grating lobes but increases hardware overhead. Therefore, the optimal quantisation depends on the application's angular resolution, power constraints, and integration density.

Overall, electronically beam-steered reflectarrays present a promising alternative to gimbaled reflectors and phased arrays, balancing performance, cost, and mechanical simplicity.

2.5.6 Wireless Control Architectures for Reflectarray Antennas

The majority of electronically reconfigurable reflectarrays demonstrated in the literature rely on direct electrical connections between a centralised controller and the individual tuning elements distributed across the aperture. These wired control architectures typically employ one of three topologies: matrix addressing schemes where row and column buses distribute bias voltages to elements at their intersections. These serial peripheral interface buses daisy-chain commands to groups of elements through integrated circuits embedded on the aperture, or parallel direct wiring where individual control lines route from a central unit to each active element [18, 16, 6]. While these approaches have demonstrated functional success in laboratory environments, they constrain the scalability, deployability, and system-level simplicity of large reconfigurable apertures for space applications.

The architectural limitations of wired control become increasingly severe as aperture dimensions grow and element counts scale into the thousands. A reflectarray with N individually controllable elements requires at minimum $\log_2(N)$ address lines and separate data and power distribution networks when using multiplexed architectures, or N individual control lines when using

direct wiring. For a 1000-element aperture, this translates to hundreds of conductors that must be routed across the antenna surface, through deployment hinges if the structure is foldable, and back to the spacecraft bus. The resulting cable harness contributes significant mass that scales with aperture size, introduces mechanical complexity that increases integration time and cost, creates additional points of failure through connectors and solder joints, and generates potential electromagnetic interference pathways where control signals can couple into the sensitive RF aperture or where high-power payload signals can disrupt low-voltage control electronics [5, 3].

From a spacecraft integration perspective, the dense harness required by wired control architectures complicates the mechanical design of deployable structures. Each hinge line in a folding reflectarray must accommodate the control cabling, which can represent single points of failure for large numbers of elements. The routing constraints often drive panel dimensions and hinge locations, subordinating electromagnetic optimisation to mechanical necessity.

The research literature contains remarkably few attempts to eliminate or significantly reduce this control harness through wireless or alternative command distribution methods. A comprehensive survey of reconfigurable reflectarray publications from the past two decades reveals that wireless control remains essentially unexplored [13, 73]. The optical control methods discussed previously represent the closest analogue to the proposed approach in this work, where laser illumination replaces electrical connections to activate photoconductive switches integrated into microwave elements. Pioneering work by Miao and Lin demonstrated large-scale optically addressed reflectarrays where a scanning laser beam individually illuminates silicon photoconductors integrated into each unit cell, changing their microwave impedance and thereby controlling the reflection phase [19, 74]. This method eliminates the electrical control wiring and demonstrates the principle of wireless element addressing, but introduces other significant challenges for space applications. The photoconductors are sensitive to solar illumination, requiring careful spacecraft attitude control or physical shielding to prevent the Sun from inadvertently commanding the aperture [64]. The optical distribution system itself adds mass and complexity due to the required laser sources, beam steering mechanisms, and optical paths that must maintain alignment during launch vibration and on-orbit thermal cycling. In addition, the photoconductor integration requires specialised semiconductor processing that cannot use commercial off-the-shelf components, substantially increasing cost and limiting the technology to research demonstrations [63].

The absence of true wireless control architectures in the reflectarray literature creates a significant gap between the demonstrated capabilities of these antennas and their potential for scalable space deployment. For next-generation missions requiring apertures of several meters or more, the harness problem can become a constraint that can change the architectural viability of reconfigurable surfaces.

This thesis addresses the wireless control gap directly by proposing and demonstrating a dedicated out-of-band RF command link that operates orthogonally to the aperture's primary electromagnetic function. The architecture treats configuration control as a separate communication system with its own frequency allocation, link budget, and reliability requirements rather than as a parasitic function forced to coexist with the payload RF. By establishing a wireless control

plane at 433 MHz that is spectrally isolated from the X-band aperture by more than an octave in frequency, the design avoids the interference coupling and solar sensitivity issues that constrain optical approaches while eliminating the harness mass and integration complexity that burden wired architectures. The tile-level intelligence paradigm, where each modular subassembly contains its own receiver and interpreter electronics, enables true scalability through replication of identical building blocks rather than increasingly complex centralised control. The broadcast and addressed command protocol supports both rapid whole-aperture updates and targeted corrections to individual tiles or cells, providing operational flexibility that would require substantial wiring resources in conventional architectures.

The novelty and significance of this contribution must be understood within the broader context of reflectarray research. While the field has successfully advanced unit cell designs, achieving excellent electromagnetic performances, it has not addressed the current control architectures that constrains practical implementation at scale [10]. The wireless architecture presented in this thesis represents an enabling technology that fundamentally changes the scaling characteristics of reconfigurable apertures. The wireless control results establish a new architectural baseline for future reconfigurable aperture development, opening pathways toward electronically steerable antennas that are practical to build, test, integrate, and operate in demanding space environments.

2.6 Stowing and Fabrication Techniques for Satellite Applications

One of the most critical engineering challenges in designing reflectarray antennas for space applications is ensuring compact stowage during launch and precise deployment in orbit. Reflectarrays must fit within the constrained volume of a launch vehicle and subsequently deploy into a nearly planar configuration to preserve their radiation pattern fidelity. Even slight deviations from the intended surface flatness can lead to gain degradation, beam distortion, and pointing inaccuracies.

The deployment mechanism, particularly the hinge system, is pivotal in maintaining structural repeatability and minimising surface deformation. Errors introduced during deployment—such as hinge misalignments, thermal-induced warping, or adhesive failures—can cause significant out-of-plane displacement. These deviations become more pronounced in large apertures and high-frequency systems.

A technique to enhance structural rigidity over the satellite's operational thermal range is symmetric PCB stack-ups on both sides of the reflectarray. This symmetry mitigates thermally induced curvature by balancing thermal expansion forces [75].

The deployment hinges are categorised into root and wing hinges, each influencing different aspects of the array geometry. While root hinges primarily impact overall beam pointing, wing hinges can degrade both gain and point due to localised warping. The hinge height, stacking configuration, and bonding process are key determinants of stowed volume and deployment reliability.

JPL demonstrated significant advancements in the Mars Cube One (MarCO) CubeSat mission [4]. Their design employed torsion spring-actuated butt hinges and U-shaped channels around the PCB edges to minimise stowed thickness. The bonding process involves injecting adhesive into

gaps between the panel and hinge channels, using a tooling jig for alignment. However, thermal cycling caused the bond material to decompress, producing fixed deployment errors. Reinforcement with metal wires mitigated these effects.

The OMERA (One-Meter Reflectarray Antenna) program [20] provided further validation by quantifying surface flatness after deployment. Figure 2.15 shows the measured out-of-plane deviation.

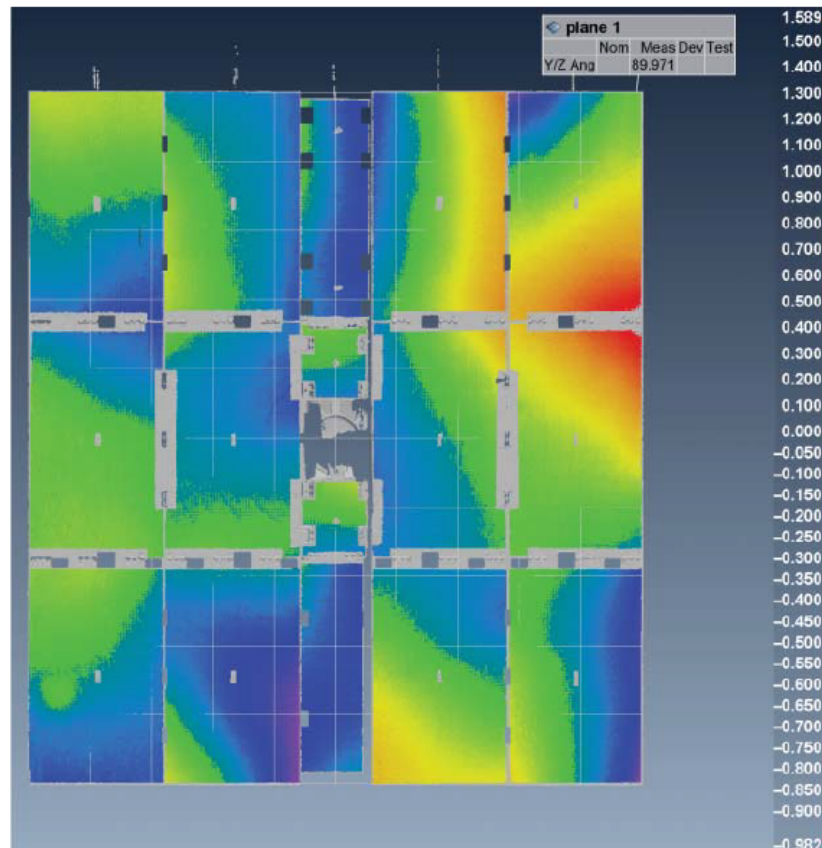


Figure 2.15: Final adjusted surface profile of a deployed reflectarray panel from the OMERA project. Colour bar units represent millimetres. Left side deviation: 0.98 mm; right side: 1.59 mm. [20]

Despite being under 2 mm, the localised panel inaccuracies resulted in a measured gain degradation of 0.3 dB [76]. These findings underscore the importance of hinge quality, bonding uniformity, and thermal design in maintaining high-performance reflectarray deployments.

Several innovative deployment mechanisms have emerged to replace or enhance traditional hinges:

- **Origami-Inspired Structures:** Use folded patterns to achieve compact stowage and reliable unfolding kinematics [77].
- **Tensegrity Frameworks:** Employ tensioned cables and compressive rods to maintain structural integrity while minimising mass.

- Inflatable Reflectarrays: Utilise pressurised membranes to deploy large surfaces with minimal launch volume.

Material selection must accommodate extreme orbital conditions: temperature cycling, vacuum-induced outgassing, and radiation exposure. Ideal materials exhibit low dielectric loss, high radiation tolerance, and minimal coefficient of thermal expansion (CTE) mismatch. Ensuring CTE compatibility between substrates, adhesives, and support structures helps preserve reflectarray shape across temperature swings [78].

The integration of reflectarrays with other spacecraft components presents further opportunities and constraints. Notably, recent concepts involve dual-purpose surfaces where reflectarray elements are transparent to visible light, enabling co-integration with solar cells. This multifunctionality is particularly valuable in CubeSats and other small satellite platforms with stringent area constraints [78].

In summary, deployable reflectarrays' mechanical and thermal design is inseparable from their RF performance. Future innovations must address mechanical tolerances, hinge mechanics, and material engineering to support larger apertures and higher frequency bands in compact satellite platforms.

Chapter 3

Proposed Reconfigurable Reflectarray Architecture and Feasibility Study

This chapter provides the proposed modular reflectarray architecture. It demonstrates how to achieve modularity without compromising control. It also displays the baseline for each primary design block, encompassing hardware, software, and firmware. In addition, this chapter presents preliminary feasibility studies to determine that there are no preliminary restrictions to the proposed design.

This thesis covers two distinct parts: the reflectarray design and the wireless control, which also includes the development of hardware and radio control signals. This chapter presents the overall system-level architecture proposed in this thesis, explaining the rationale behind design decisions and comparative trade-offs where necessary. It also included feasibility studies to assess the viability of the proposed solution in actual use cases.

The proposed reflectarray consists of a two-dimensional array of identical tiles, each equipped with wireless control for individual cells. With this approach, obtaining the desired size and format for the entire reflectarray is possible by simply adding the desired number of tiles in a specific direction. Figure 3.1 presents the concept for the proposed reflectarray antenna.

For this thesis, the reflectarray size is 0.5-by-0.5 meters. The reason for this choice of reflectarray size is that it offers significantly better gain and beam control performance compared to a smaller one. The larger aperture enables more effective beam steering and can support more advanced functionalities, such as beam shaping or null steering, which is critical for the reflectarray tests. However, the increased size introduces several challenges. Fabricating a larger array is more expensive and complex due to the higher number of elements and the increased PCB area, and it increases the complexity of the thesis because the design must address scalability issues from an early stage.

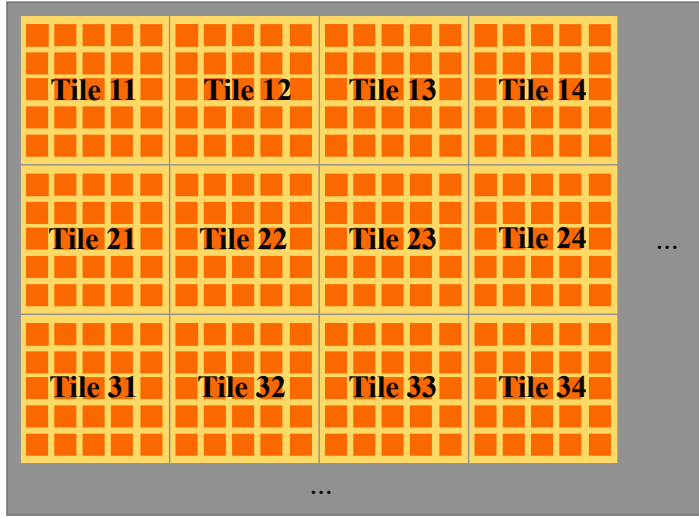


Figure 3.1: Reflectarray architecture.

3.1 Tile Architecture

Figure 3.2 shows the tile architecture, which is possible to verify that it will be composed of an array of unit cells. For this work, each unit cell will consist of a PCB element with an embedded active device capable of changing its reflection coefficient phase. At this initial phase, a 5×5 array, resulting in 25 unit cells, is considered a reasonable controllable number in each tile. For X-Band applications, each unit cell will have about $20 \times 20 \text{ mm}$ and each tile, consequently, $100 \times 100 \text{ mm}$. As previously presented, there are several examples of printed cells in the literature, and depending on the chosen format, it is possible to obtain various characteristics for the reflectarray, such as bandwidth and gain.

The reflectarray beam will be wirelessly controllable by an independent feed on the platform, with a different operating RF frequency, exclusively used to send specific configuration signals to mitigate implementation problems and RF interference. An RX antenna in each tile will receive these radio control signals and then be interpreted and decoded by a specific low-footprint circuit, designated as *interpreter*, embedded on the back of each tile, acting on the varactor diodes by regulating their reverse bias voltage.

In the following subsections, the different components of the tile architecture are introduced and presented in more detail.

3.1.1 Interpreter

The interpreter PCB is responsible for processing the radio control signal received via a 433 MHz antenna and generating the appropriate control voltages for the varactor diodes of a tile or reflectarray. A 433 MHz UHF control link provides a robust, low-SWaP command plane decoupled from the 9.6 GHz SAR payload baseline. At 433 MHz, free-space and material losses are lower, making

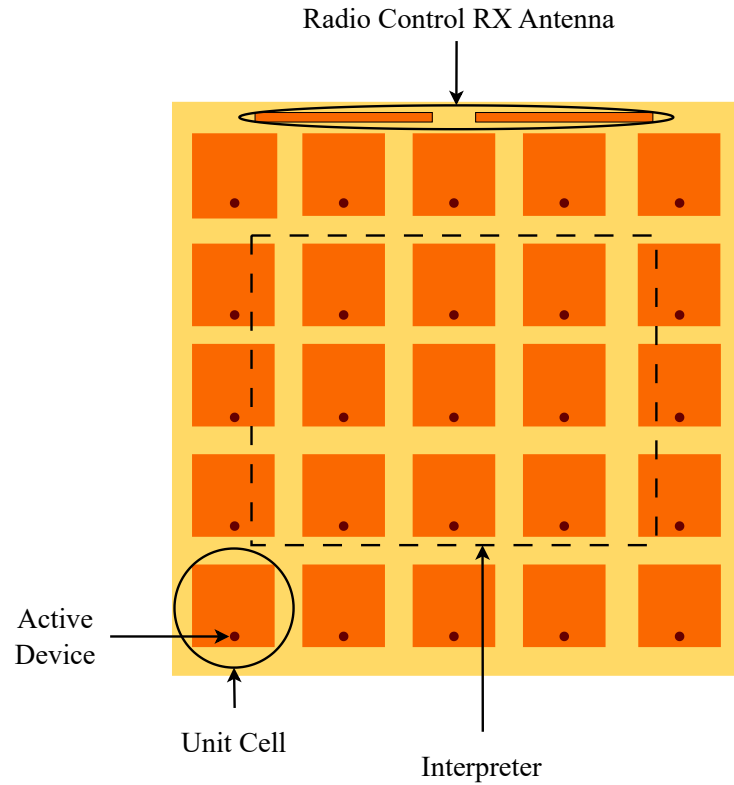


Figure 3.2: Tile architecture.

it an ISM frequency suitable for proximity operations, which reduces the likelihood of interference from another payload on the satellite. So, a narrowband OOK receiver with high sensitivity can cover the full aperture with modest EIRP while keeping the protocol simple, microcontroller-friendly and with a wide low-power electronics availability. An OOK modulation allows for a reduction in processing capability requirements, contributing to lower power consumption. In addition, by showcasing such capabilities through simple modulation, it demonstrates that the proposed system can be applied to a broader range of applications in noisier environments. Equally important, the significant frequency separation from X-band maximises EMC margins: the X-band feed and RF stack inherently reject UHF energy. At the same time, the limiter and dedicated 433 MHz filtering on the RF RX front-end provide strong out-of-band attenuation, protecting the interpreter from saturation by the X-band illumination. Conversely, the control signal RF emissions sit far outside the reflectarray operating band. They are further suppressed by the X-band front-end and aperture response, minimising self-interference, spurious re-radiation, and RF-to-bias coupling into the varactor network.

The signal flow begins with the reception of the signal on each tile's radio control signal antenna, passing the resulting signal through a u.FI cable to the interpreter PCB. Then, the radio control signal is limited and filtered to ensure that high-power signals do not damage the board's components. The RF power limiter protects the board from high input power, ensuring safe opera-

tion by limiting the output leakage, and the filtering stage ensures minimal signal loss and provides a 25 dB minimum out-of-band attenuation, making it an effective solution for handling the 433 MHz signals.

The receiver circuit then converts the RF signal into serial data. It offers a reliable wireless serial data transfer in the 433 MHz band, with a sensitivity of -112 dBm and a data rate capacity of up to 10,000 bps.

The microcontroller decodes this data, determining the tile configuration and forwarding this information to the FPGA using the SPI protocol. The microcontroller also manages the addressing of each tile through pull-up or pull-down resistors, ensuring each tile only decodes the relevant data. The FPGA generates the required pulse-width modulation (PWM) signals, which are subsequently translated into the appropriate voltage range to control the varactor diodes. RC low-pass filters are employed to convert the PWM signals into steady-state voltages. Combining a microcontroller for signal decoding and an FPGA for PWM generation ensures efficient processing and control, leveraging the unique strengths of each device's architecture and capabilities. The FPGA generates PWM signals in the 0 V to 3.3 V range, which are then translated to the 0 V to 5 V range required by the varactor diodes to achieve the necessary phase variation. An RC filter is applied immediately after the voltage translators to convert the PWM signals into stable analogue voltages, ensuring precise control of the varactors. This interpreter design enables precise and scalable control of the tiles while maintaining low power consumption and ensuring robust operation through reliable signal handling and processing. Figure 3.3 shows the interpreter architecture.

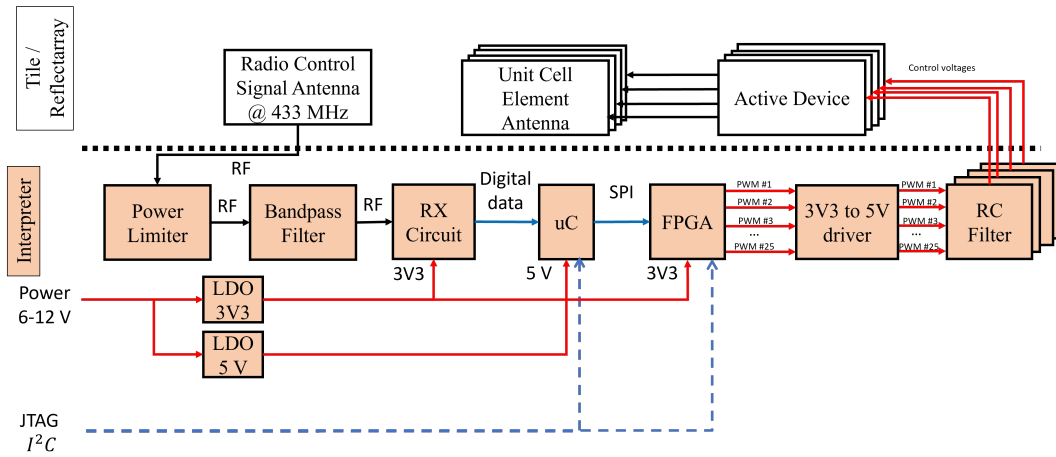


Figure 3.3: Interpreter hardware architecture.

3.1.2 Unit Cell and Active Device

As previously mentioned, several possible devices can be used to adjust the phase of the reflectarray, considering both RF and DC performance. PIN diodes present an impractical solution for the proposed design since their use primarily enables binary control. Hence, no continuous control of the reflected phase between 0° and 360° is possible. A more relevant aspect is that they

have high power consumption, given the large number of unit cells on the reflectarray. Although varactor diodes have higher losses compared to MEMS, they enable continuous phase variation control within a lower voltage range. Regarding MEMS, despite having lower power consumption and insertion loss, while presenting high linearity and isolation [16], they still incur a high cost, which would increase the total reflectarray cost. Manufacturing and testing reflectarrays with liquid crystals and similar solutions require special facilities, making these approaches impractical until technology advances. Additionally, they are highly sensitive to temperature variations, which makes them challenging to use in space applications. Considering this tradeoff, the varactor diode is chosen for use in this work.

Although it is the best device for the proposed application, selecting varactor diodes necessitates acknowledging their inherent trade-offs to the end goal. The literature highlights varactors exhibit higher insertion loss than alternatives like MEMS and suffer from a nonlinear capacitance-voltage (C-V) relationship [79, 80]. Having a high insertion loss directly degrades antenna gain and overall efficiency. The nonlinear C-V curve presents a control challenge, as any instability or noise in the bias voltage will translate nonlinearly into phase errors, which can degrade beam quality and pointing accuracy. This thesis confronts these challenges through careful system design. The impact of insertion loss is accepted as a trade-off for achieving continuous, low-cost tuning, low-power, and easy integration when scaling the reflectarray, not requiring specific facilities or manufacturing requirements. It is also important to emphasise that this thesis aims not to develop hardware to achieve the best performance, but to evaluate the feasibility of the proposed concept. The control system mitigates the nonlinear effects with a highly stable and distributed power supply. It employs high-resolution Pulse-Width Modulation (PWM) to generate the bias voltages, allowing for a fine-grained digital approximation of the inverse C-V curve to linearise the phase response.

As such, it is necessary to assess several parameters to choose the right varactor diode for the proposed digitally steerable X-Band reflectarray. For this thesis, the varactor diode shall be compliant with the following requirements:

- **Linearity:** The varactor diode shall have constant and predictable behaviour to ensure precise control for the different beam steering angles.
- **Voltage Control Range:** The voltage tuning range of the varactor diode shall be between 0 V and 5 V to enable the usage of low-power electronics.
- **Capacitance Range:** The varactor diode's capacitance range shall cover the required values for the reflectarray beam steering - more details in the following section.
- **Package and Mounting:** The varactor diode physical package shall be compatible with the simulation and integration needs.

For space applications, the varactor diode selection must consider other specifications, such as temperature stability and radiation tolerance, but these trade-offs were not part of this thesis work

plan. In addition to the overall electrical, mechanical and performance requirements, the analysis must consider the varactor diode's cost, as a large reflectarray might require several thousand diodes.

3.1.3 Radio Control Antenna

As previously mentioned, the control link is allocated in a band spectrally separated from the reflectarray operating band to minimise coupling with the phase-tuning elements and preserve the unit-cell scattering properties. Also, as each tile operates autonomously, there must be a specific antenna to receive the radio control signal from the feed antenna on the platform. This antenna cannot impact the reflectarray design, so its design must be minimal. The selected type is a planar dipole inserted on the top part of the reflectarray. On the bottom layer, the balun realises a $100 - to - 50 \Omega$ transformation (differential dipole to single-ended line), where its output presents a broadband 50Ω interface to the u.FL connector. The signal filtering is done at the interpreter PCB level to reduce the number of components and the RF path to minimise interference as much as possible. RF traces are routed along unit-cell and tile gaps and referenced to a continuous ground with dense via stitching to contain return currents. The overall link budget will show that the antenna does not need the best possible performance, making it possible to design in such a small area for the given operating frequency.

3.2 Radio Control Signal

There are several suitable modulation schemes to send the control signals. However, due to its simplicity in implementation, On-Off Keying (OOK) was selected as the principal option. The Bit Error Rate (BER) on an OOK channel is stated by (3.1) and gives the probability of a bit error occurring along the channel.

$$P_{b,OOK} = Q\left(\sqrt{\frac{E_b}{N_0}}\right), \quad (3.1)$$

Where E_b/N_0 is the energy-per-bit to noise power spectral density ratio, and the Gaussian Q -function is defined as:

$$Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^\infty \exp\left(-\frac{t^2}{2}\right) dt. \quad (3.2)$$

The transmitted data can contain errors as data transmission systems are subject to noise. To mitigate the effects of these errors, error detection and correction techniques will be employed. Coding techniques are called Forward Error Correction (FEC) and Cyclic Redundancy Check (CRC). The goal is to achieve robust detection while minimising the detection of false messages.

For implementation simplification purposes, the messages to all tiles will be the same (broadcast), and each interpreter will be capable of controlling the unit cells accordingly. Two types of suitable signal architectures can then serve this purpose:

- To send the exact phase configuration for each active phase cell device at any given instant of time;
- To send the coefficients of a 2-D phase function (e.g., a polynomial) with the correct phase configuration for the initial time and a trend for the following samples to reduce the number of commands over time.

The first approach is to send shorter signals more often, while the second option leads to longer signals sent less frequently.

The dedicated feed in the platform will transmit the radio control signals, providing a specific power density distribution along with the aperture.

3.3 Software and Firmware

As previously mentioned, each interpreter PCB has a microcontroller and an FPGA to decode the RF protocol and actuate in each unit cell. Figure 3.4 describes the high-level SATORI Software and Firmware architecture.

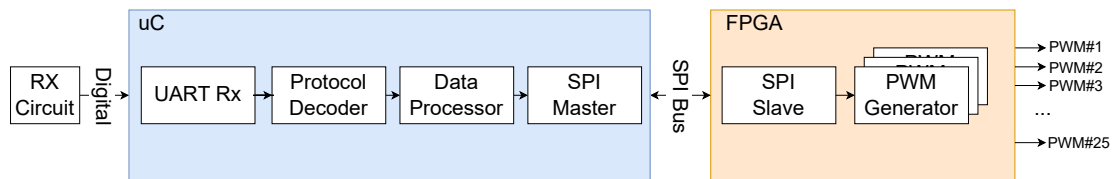


Figure 3.4: SATORI Software and Firmware interaction.

The software has four main blocks:

- UART RX - decodes the UART protocol on top of the OOK modulation;
- Protocol Decoder - interprets the different fields of the protocol and creates a structure for further decoding;
- Data Processor - understands each field of the protocol and computes the required values for each PWM;
- SPI Master - communicates the required FPGA routing, meaning what PWM value shall have each output.

In addition, there is a standard code to configure all the interpreter board devices, including FPGA memory programming and digital communication protocols.

The Firmware has two main blocks:

- SPI Slave - decodes the SPI generated by the microcontroller;
- PWM Generator - generates the different PWM values and routes them according to the microcontroller computation;

3.4 Preliminary Feasibility Budgets

The analysis elaborated on preliminary power and data budgets as an initial feasibility study. Also, the evaluation assessed the ability of the reflectarray and corresponding active devices to withstand high RF power transmitted through the antenna feed.

3.4.1 Power Budget

Some considerations were made to estimate the power budget of the reflectarray. This analysis refers to the reflectarray architecture present in fig. 3.3, being, therefore, a worst-case scenario once it includes the LNA:

- Each varactor diode has leakage currents in the order of magnitude of 100 nA , operating at 5 V . Such results in $0.5\text{ }\mu\text{W}$ for each unit cell. As previously mentioned, each tile will have 25 controllable unit cells and, therefore, the total average power for the varactors is $12.5\text{ }\mu\text{W}$;
- As mentioned before, the FPGA will operate using a low-frequency clock, allowing lower power devices to be selected. There are suitable FPGAs for the required operation consuming about 0.2 W .

Each tile has a total power consumption for beam shaping of 0.3 W . Since each tile will have $0.150 \times 0.150\text{ m}$, a 3.5 m^2 antenna will consume less than 45 W . This value still needs to be multiplied by the duty cycle factor of the reflectarray use in orbit. Considering the total power consumption of a typical SAR instrument while operating, or even a telemetry transponder, the total power consumption of the proposed wireless control system is negligible, making it a suitable candidate for new instruments.

3.4.2 Reflectarray Wireless Control Data Budget

A spotlight SAR mission is used as a reference to predict the required beam steering rate. A maximum of 1 degree per second rate is considered a good estimation for the satellite beam steering rate. Calibration messages can be sent, at a lower rate, to verify that the beam is correctly pointed.

At this stage, a message rate between 1 to 10 Hz is enough to satisfy the requirement for the beam steering capability. At this rate, using messages up to 100 bytes with FEC / CRC overhead of 1:2 is compatible with a 19200 baud rate, which fits 20 kHz bandwidth with an E_b/N_0 of about 10 dB. For such a small bandwidth, 1 mW of transmission power is enough to close the link budget over the maximum distance between the feed and any tile. Also, it allows for low carrier frequency and even lower power levels for this wireless communication. As previously stated, using a lower carrier frequency allows for a more independent interpreter circuit approach.

3.4.3 Reflectarray Power Handling

This section assesses if the RF power transmitted to the reflectarray can damage the active devices. Considering the SAR X-Band mission as a reference and assuming that:

- The RF peak power is 1000 W (60 dBm);
- The reflectarray antenna feed gain is 6 dBi - this value is just for link budget purposes, as a feed with this gain at 2-meter distance would create high spillover losses;
- The minimum distance between the feed and the closest tile of the reflectarray is 2 meters, resulting in 58.1 dB of free-space losses at a transmission frequency of 9.6 GHz.

Using a patch antenna as the printed element of the unit cell, and assuming that its efficiency will be lower than expected given the tunable varactor diode existence, the predicted gain compared to an isotropic antenna will be around 4 dBi.

The total power received by each reflectarray unit cell is then $60 + 6 - 58.1 = 7.9$ dBm, and the total power reaching the varactor diode is $7.9 + 4 = 11.9$ dBm, which corresponds to approximately 15.4 mW.

From (3.3) is possible to compute the voltage increment, V , at the varactor diode terminals during the transmission of an RF Power, P , of 1000 W at the reflectarray feed antenna:

$$P = \frac{V^2}{R} \Leftrightarrow V = \sqrt{P \times R}, \quad (3.3)$$

where R corresponds to the unit cell impedance, 50 Ω , assuming antenna matching. The average voltage increment is then 0.88 V. By multiplying the obtained voltage value by $\sqrt{2}$, it is possible to get the peak voltage value, 1.25 V (2.5 V peak-to-peak voltage). A varactor diode can cope with such value without disruption using a control voltage between 0 and 5 V.

Another critical aspect of the reflectarray power handling budget is ensuring the immunity of the 433 MHz wireless control link from the high-power X-band payload signal, which operates at 9.6 GHz with a peak power that can exceed 2000 W. To achieve this, the design incorporates an RF isolation strategy, leveraging bandpass filters centred at 433 MHz with a 20 MHz bandwidth and a minimum rejection of 60 dB at X-band frequencies, validated by the manufacturer S-Parameters. Additionally, the interpreter's RF front-end includes a high-power limiter to attenuate any residual X-band leakage, with a threshold set at -10 dBm to protect the low-noise amplifier and the following components.

3.4.4 Wireless Control Link Reliability

The reliability of the 433 MHz wireless control link is mission-critical; its failure would render the entire antenna system inoperable. Therefore, the analysis must go beyond the link budget, requiring an assessment of the electromagnetic and regulatory environment. The control link must be robust against two primary sources of interference, ensuring it complies with Electromagnetic Interference and Compatibility (EMI/EMC) requirements:

- **External Interference:** The 433 MHz band belongs to the Industrial, Scientific, and Medical (ISM) spectrum and is shared with various low-power devices. The 433 MHz band also has a secondary allocation for licensed amateur radio operators, who can transmit at significantly higher power levels. When in orbit, the satellite is not entirely immune to uplink interference from these ground-based sources, as it passes overhead. Still, the probability of being interfered with is very low.
- **Intra-Satellite Interference:** This is a more critical hazard. A satellite bus is an intensely noisy RF environment, containing high-power transmitters (such as the reflectarray's own X-band feed), switching power supplies, and high-speed digital processors. The receiver has a sensitivity of -112 dBm, making it highly susceptible to saturation by the noise generated by the satellite's components. The RF front-end features filtering and RF power limiting to prevent system malfunctions caused by interference. Additionally, the protocol is robust and can support FEC mechanisms, ensuring the system has a resilient communication link. If necessary, additional techniques can be employed, such as RF shielding of the interpreter module.

Regarding the regulatory framework, the use of any radio frequency in space is governed by an international treaty, principally the ITU Radio Regulations. The selection of an ISM band, typically subject to local acceptance and intended for terrestrial use, for a mission-critical control function in space requires strong justification. While this architecture is for a proof-of-concept, a flight-ready model would require a regulatory review to ensure compliance and prevent harmful interference to other space services. Regarding the possible interferences, they need to be individually studied, as they are dependent on both the platform and the payload. In any case, the current architecture already supports generic high-isolation filtering that enables standard platform operations.

Chapter 4

Hardware Development

This section presents the hardware developed for this thesis. It includes the simulation results of a vertical polarisation unit cell performance, considering the equivalent model of the varactor diode. It shows that a full range of control over the unit cell is possible, serving as a baseline for a wireless reconfigurable reflectarray. It also presents a mechanism that allows the emulation of active devices in QUPES software, thereby enabling highly reliable and fast simulations when scaling a unit cell to a complete reflectarray. This chapter includes the radio control RX antenna simulation and the reflectarray simulation. Additionally, it displays the interpreter architecture choices and layout details.

4.1 Unit Cell Design

The 9.6 GHz square unit cell is a rectangular patch antenna with a varactor diode, as presented in Fig. 4.1. It consists of a rectangular patch of width, $patch_W$, of 12.32 mm, length, $patch_L$, of 7.32 mm, and uniform inter-element spacing, Sub_L and Sub_W , of 20 mm. The array is printed onto a 0.812 mm-thick Rogers RO4003C.

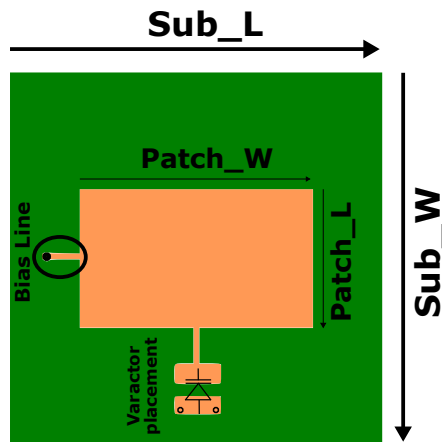


Figure 4.1: Unit cell model.

A single cell in an infinite array environment allows the behaviour of the proposed reflectarray configuration to be studied. This approach is well-suited for reflectarrays with active devices, which are usually large and made up of similar elements. In addition, the single-cell model permits the differentiation of the simulation of the circuit's passive and active circuit parts. The simulation took advantage of the Ansys cosimulation capabilities. The rectangular patch analysis uses the commercial full-wave software, Ansys HFSS, that simulates the antenna geometry, including bias circuitry, and supports the Floquet harmonics necessary to enforce periodic boundary conditions. At the same time, Ansys Circuit allows adding the equivalent circuit of the varactor to the simulation, allowing for the estimation of the impact of adding it. The simulation setup, shown in figure 4.2, includes two ports: one that supports Floquet modes, which models the incident plane wave and a lumped port located at the same area as the diode. Phase-shift walls, implemented using master-slave couples and configured to represent different angles of incidence, enforce periodic boundary conditions. To better account for the current-crowding effect caused by the presence of the varactor on the patch surface, the width of this lumped port has to be equal to the diameter of the diode.

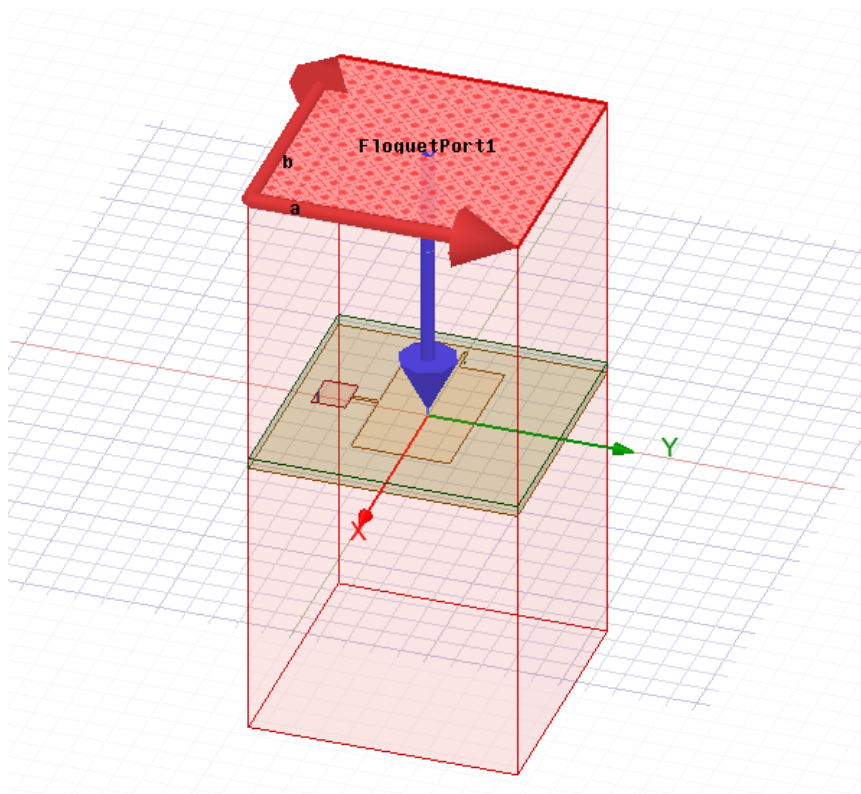


Figure 4.2: Ansys simulation unit cell model

The bias line is where the DC power is applied. By inserting it in the middle of the patch of the non-radiating edge, where the patch currents are virtually zero, it is possible to provide isolation between the RF currents on the patch and the bias circuitry [15]. With this approach, there is no need to insert RF chokes in the design, avoiding the use of extra components. Figure 4.3 shows

that the simulated surface electric field is near zero for the different phases.

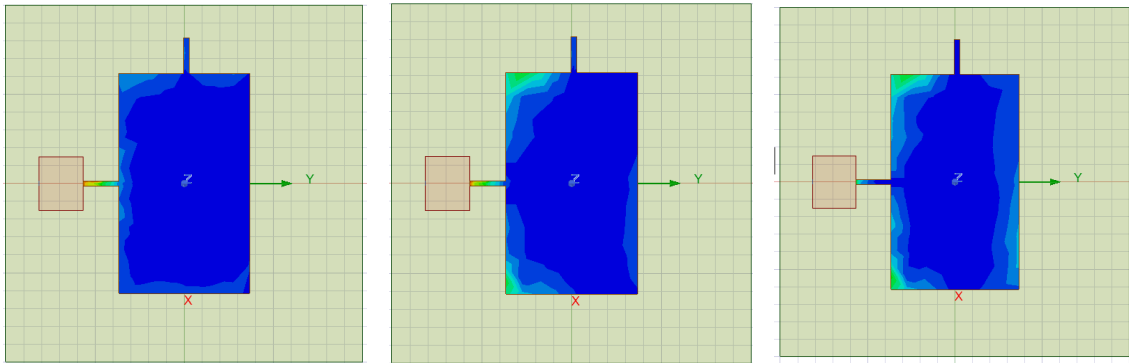


Figure 4.3: Electric field magnitude for a phase of 0 deg, 45 deg and 90 deg, respectively.

The varactor is inserted on the unit cell's top layer, as the simulation setup's lumped port represents it. Then, the Ansys Circuit tool allowed studying the effect of the varactor diode effect by running a parametric simulation where the diode capacitance changes to understand the reflection magnitude and phase change for a given frequency. Figure 4.4 presents the equivalent circuit of the patch antenna with the varactor equivalent circuit as used in the simulation, as well as the final placement of the varactor in the patch.

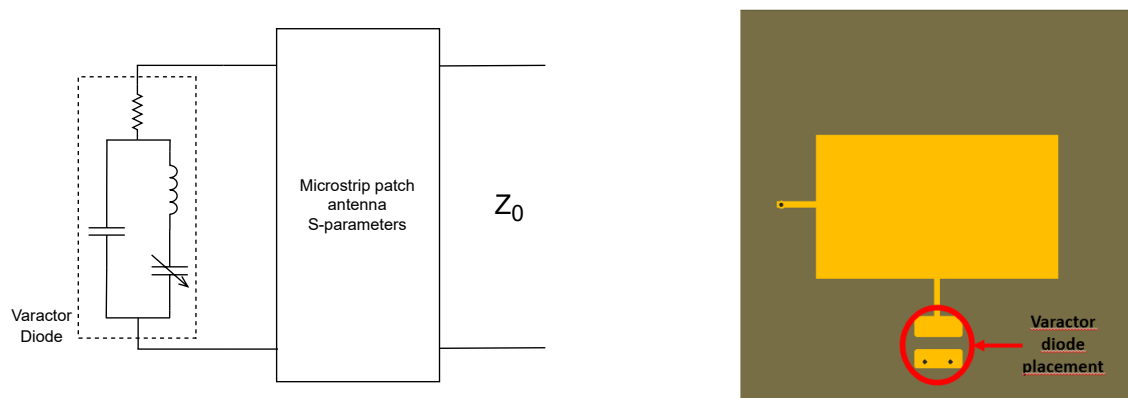


Figure 4.4: Unit cell model, equivalent model, and unit cell model and varactor placement

Figure 4.5 presents the losses and the phase variation for a capacitance variation. As expected, the loss is higher when the phase variation is more accentuated, but its magnitude is lower than 3 dB. This loss is due to the intrinsic varactor series resistance. It is also possible to observe that the significant phase variance occurs between 1 pF and 3.5 pF. Skyworks SMV1275 varactor diode is a suitable device for this design since it allows the required capacitance variation within a voltage range of 0 V and 5 V. This varactor diode does not have the highest Q-factor. Still, it presents a good trade-off between price and electrical characteristics, allowing for scalability when manufacturing the reflectarray.

QUPES is a TICRA Tools software framework product that allows the design of quasi-periodic surfaces such as reflectarrays. The software cannot yet add active devices to the unit cells and then

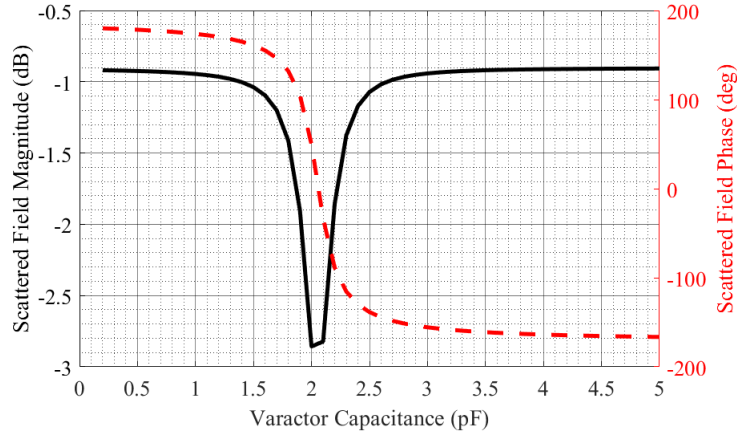


Figure 4.5: Simulated reflected magnitude and phase field

scale for the entire array [81]. Nevertheless, it is possible to replicate the behaviour of the varactor diode by varying the patch length and increasing the substrate loss tangent. Varying the patch size allows the replication of the capacitance variance, while the increased loss tangent emulates the parasitic resistance of the varactor. As such, this method required a fine-tuning of the parameters to match the results obtained with the actual varactor diode.

Afterwards, since both tools use different EM-solving methods, the HFSS simulation was repeated with the same conditions as in QUPES to evaluate the results. The simulation consisted of having the same unit cell design with equal electrical substrate properties and then only changing the patch length. Fig. 4.6 presents the results. The comparison reveals a strong correlation between the two solvers. The emulated phase response in QUPES deviates from the high-fidelity Ansys co-simulation by a maximum of 5.2 degrees. It exhibits a root-mean-square (RMS) error of 2.8 degrees across the whole tuning range. Similarly, the emulated insertion loss differs by a maximum of 0.3 dB at the operational frequency. This quantitative agreement provides the confidence to use QUPES as the primary simulation tool for the entire reflectarray, taking advantage of its precise and fast optimisation capabilities.

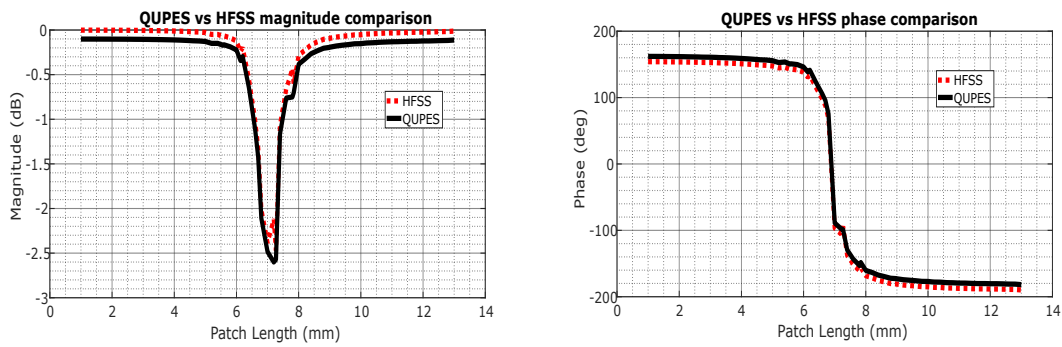


Figure 4.6: Magnitude and phase comparison between Ansys HFSS and TICRA QUPES solvers.

4.2 Tile Design

As previously stated, each tile has an associated individual control to allow for modularity while keeping control of individual unit cells easy when scaling the reflectarray. As such, each tile needs the capability of receiving a 433 MHz radio signal from the platform. Besides a radio control antenna, the tile has a layer for analogue routing, resulting in two connectors connecting directly to the interpreter's PCB. The standalone tile design also has one power and one digital connector for programming, testing and debugging single interpreter boards. In addition, the board has tabs to make it easier to hold the structure during testing.

4.2.1 433 MHz Radio Control RX Antenna

Before designing the antenna, it was necessary to understand the requirements. The following list presents the necessary link budget considerations, concluding that the minimum directivity for the radio control signal RX antenna is:

- The receiver has a sensitivity of -112 dBm;
- The reflectarray and the radio control TX antenna will be spaced around 3 meters, resulting in a free space loss of 34.71 dB at 433 MHz operating frequency;
- The TX module has an output of 0 dBm;
- Considering that the TX antenna has 0 dBi of gain, and the TX and RX circuits have a loss of 10 dB, the minimum RX antenna directivity needs to be -77 dBi.

Given the size of the tile and the available space, a planar dipole is the best candidate for the radio control signal antenna. A chip antenna would add an increased PCB height, making it unfeasible, as the antenna splits into different foldable panels for a satellite.

A new simulation environment focused on this antenna with the previous substrate specification - Rogers 4003C with a total height of 0.812 mm - but with no further size constraints. The objective of this simulation was to create a valid model before being adjusted to the final tile configuration. Again, the simulation used the finite element method (FEM) in HFSS in the frequency domain. Figure 4.7 shows the final tuned planar dipole with the following design parameters:

- Substrate length (x-axis) of 380 mm;
- Substrate width (y-axis) of 520 mm;
- Dipole length of 258.5 mm;
- Dipole width of 6.5 mm;
- Port gap width of 6.5 mm.

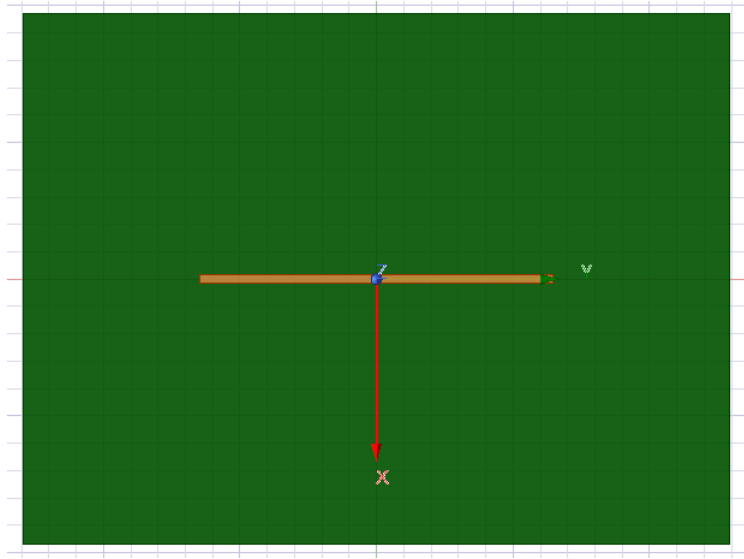


Figure 4.7: Simulation model of the planar dipole.

The simulation used a 50Ω lumped port on the port gap width. Due to the nature of a dipole, there was no ground plane in the simulation. Figures 4.8 and 4.9 present the planar dipole reflection coefficient and radiation pattern, respectively.

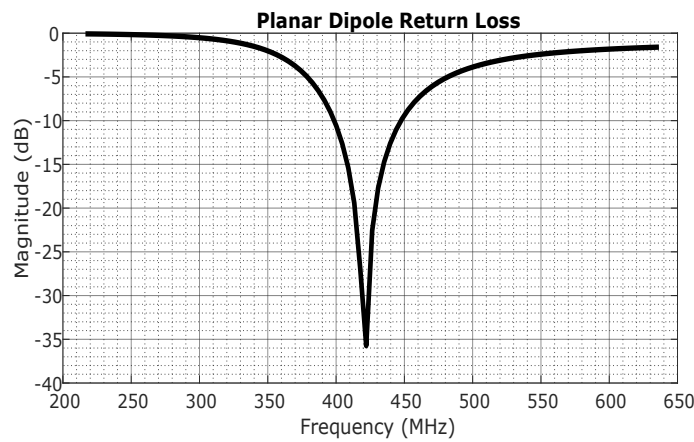


Figure 4.8: Initial planar dipole simulated reflection coefficient.

As it is possible to observe, the antenna is matched for the desired frequency, presenting a gain of 2 dB.

Although achieving a good RF performance, the final planar dipole has several design constraints. Since each tile has a 100 mm width and length, the maximum dipole length must be smaller to avoid touching the following antenna of the adjacent tile. Also, the reflectarray requires a uniform ground plane to re-radiate the electromagnetic wave. In addition, the presence of the X-Band unit cells close to the dipole will affect its performance. Such constraints are typical in electrically small antennas, where the radiating elements are usually a small fraction of the operating wavelength. Then, the VHF antenna must be resimulated and optimised with the proper

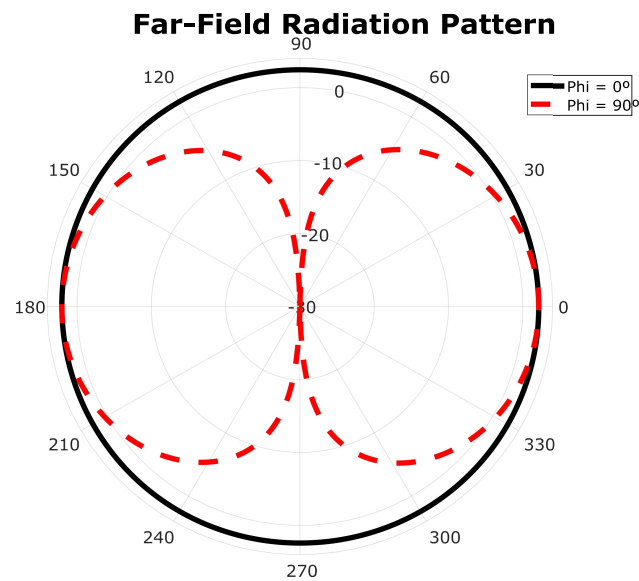


Figure 4.9: Initial planar dipole simulated far field gain.

specifications. The result is a planar dipole antenna that contains a matching inductor and a balun. The inductor will contribute to creating an artificial length to help match the antenna, since its size is smaller than required due to the available space. The antenna has no restricted efficiency requirement, as the link budget proves. Figure 4.10 shows the simulation model created to simulate the radio control signal RX antenna. It has the full tile size and has metallic patches representing the ones that will compose the reflectarray. The orange part represents the dipole, the brown part provides the spacing, and the red part indicates the inductor placement.

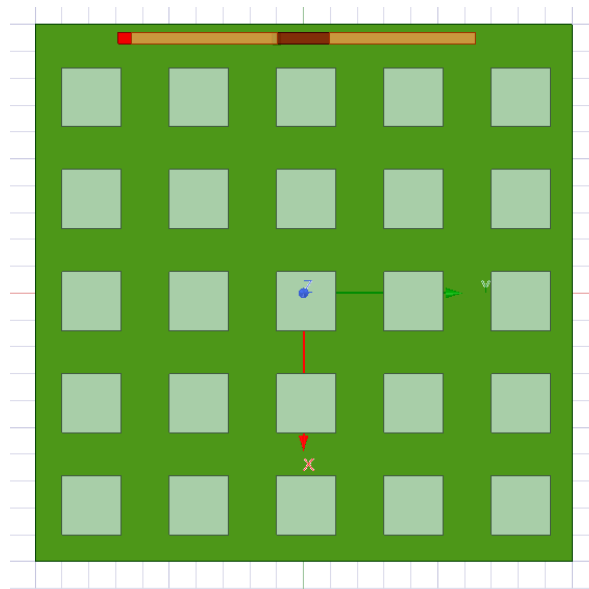


Figure 4.10: Simulation model of the 433 MHz antenna.

Figure 4.11 shows the reflection coefficient, while figure 4.12 presents the simulation results

of the radio control signal antenna. Observing an estimated gain of approximately -31 dBi is possible, and the antenna does not achieve the -10 dB reflection coefficient. As previously stated, the dipole behaviour is equivalent to an electrically small antenna due to its reduced size. As such, its input impedance and radiation efficiency degradation occur due to the losses.

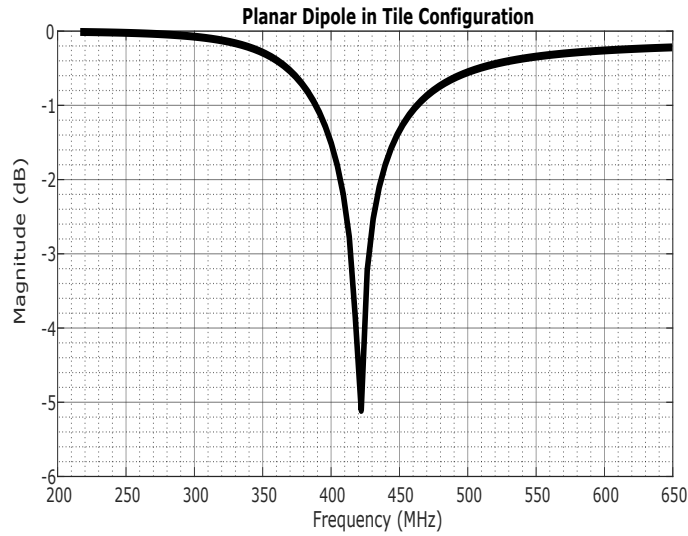


Figure 4.11: Reflection coefficient simulation result of the 433 MHz antenna.

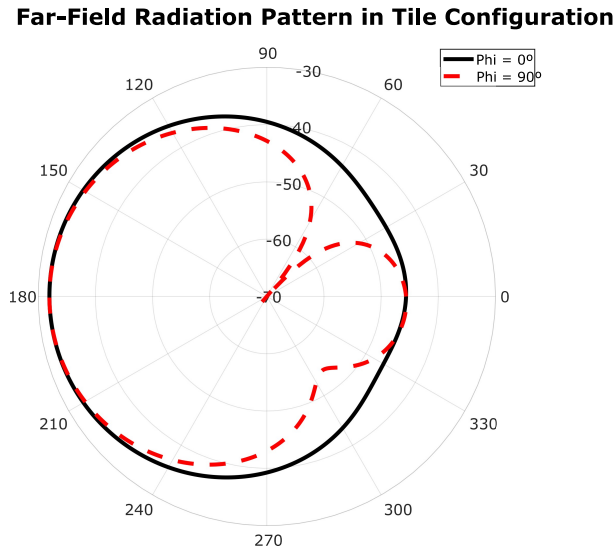


Figure 4.12: Far field gain simulation result of the 433 MHz antenna.

4.2.2 Tile Layout

It is necessary to route individual power signals, as each varactor requires a particular voltage. In addition, the development and debugging process requires digital signals to interact with the interpreter circuits. So the tile design is composed of the antenna and routing parts. Only with a

multi-layer PCB design could such a need be accommodated. Figure 4.13 shows the final PCB stackup for both the tile and the reflectarray.

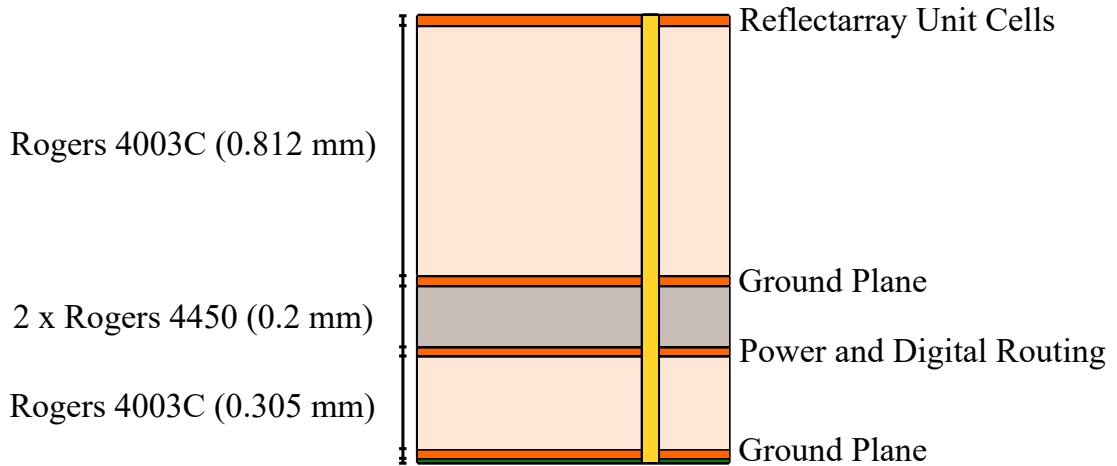


Figure 4.13: Tile and reflectarray stackup.

The first substrate core is exclusive to the antenna part, the second is the prepreg between the two core substrates, and the third is another core substrate with less dielectric height. The selection of an asymmetric substrate relates to minimising the PCB height. The top layer has the reflectarray unit cells, the radio control RX antenna and the corresponding space for the varactors and matching inductors. The first intermediate layer is the reflectarray ground plane. The second intern layer is for power and digital routing, while the bottom layer is another ground plane with minor routing to avoid electromagnetic interference when integrating it for tests. The design includes through-hole vias to pass the signal between all layers. There are no buried or blind vias to minimise the PCB manufacturing risk and keep the design simpler to manufacture and, therefore, cheaper.

Figure 4.14 shows the top, bottom and the intermediate layer used for routing. As previously mentioned, the second layer only has the reflectarray ground plane, so it is unnecessary to present it.

Tile manufacturing consisted of two phases. The first version only had the antenna part (top layer and respective ground plane), while the second one had the full stackup. This approach allowed isolating the antenna's behaviour from the control part, so the tests could focus only on the RF side before scaling it to a more complex system. As the first version had no power routing, each unit cell had a wire soldered to the feeding via on the back of the tile to allow voltage variation to control each unit cell individually. The first version also allowed testing the RF performance before scaling it for the entire reflectarray.

4.3 Interpreter

The interpreter receives the radio control signal from its 433 MHz antenna tile through a u.FL connector, decodes the signal and generates the necessary voltages to control the varactor diodes of the corresponding tile. The information flow is as follows:

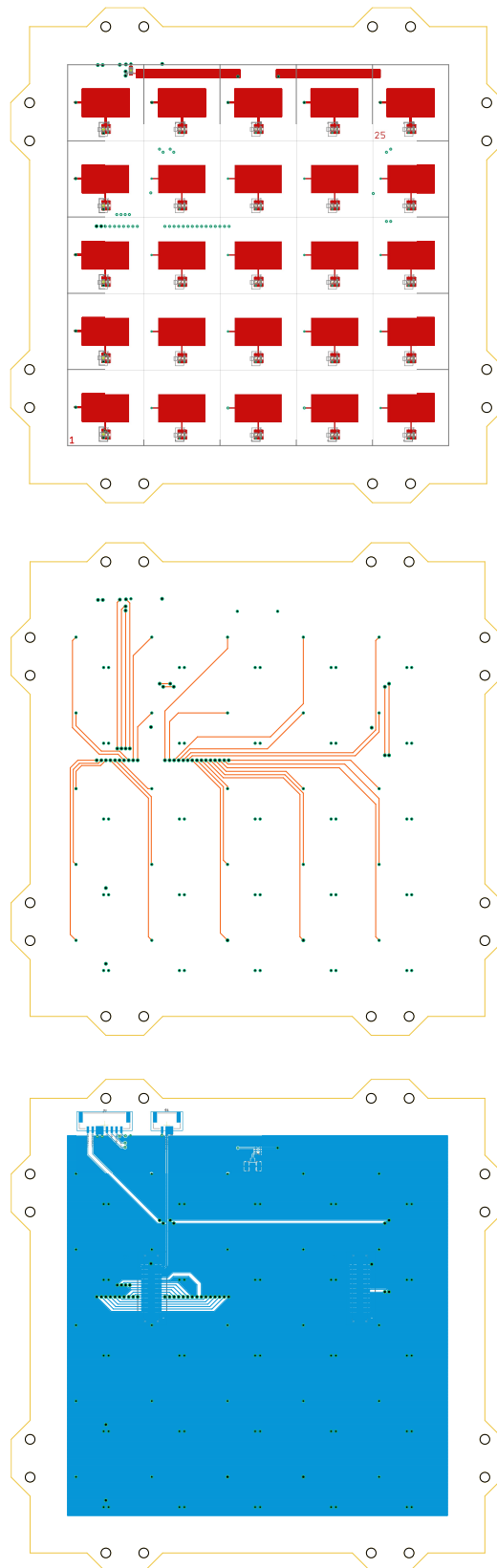


Figure 4.14: Tile top, intermediate and bottom layers, respectively.

- The radio control signal is limited and filtered - this step ensures the powerful signal from X-Band does not damage the devices on the board;
- The RX circuit, RXM-433-LR device, receives the RF signal and transforms it into serial data;
- The microcontroller receives and decodes the data, understanding what shall be its tile configuration matrix and communicates this information to the FPGA through an SPI protocol;
- The FPGA receives the commands and generates and outputs the proper Pulse-Width Modulated (PWM) values for each varactor;
- The driver will translate the PWM signal from 0V and 3.3 V to 0 V and 5 V, as the varactors are controlled within this voltage range;
- Each output has an RC low-pass filter to transform each PWM into a steady-state voltage.

4.3.1 RF Power Limiter and Filtering

The power limiter device is a very reliable limiting component. It exhibits 7 dBm typical output leakage powers at a maximum of 32 dBm input power in the 433 MHz frequency range. It also presents a delta output power versus the delta input power of 0.3 dB, typical within its input power limiting range of 12 to 32 dBm. It also shows a low insertion loss, making this a suitable solution for the required application.

The filter has low loss and does not require a matching network for operation at 50 Ω . The minimum out-of-band attenuation is 25 dB, making this filter a good solution.

4.3.2 RX Circuit

The RXM-433-LR receiver was the selected device for the wireless reception of serial data in the 433 MHz band, as it can achieve a typical sensitivity of -112 dBm. It can establish a reliable wireless link capable of transferring serial data rates of up to 10000 bps. The standalone device tests showed link reliability and excellent noise immunity. Besides the performance specifications, the device has an SMD package that does not require external RF components besides an antenna, allowing for easy integration at the PCB level. It has a very low power consumption, less than 20mW.

4.3.3 Microcontroller

The ATMEGA2560-16U presents the overall required specifications to accommodate the protocol data rates. Also, it has some features that make it suitable for the SATORI application:

- 5 V powered;
- low-power consumption;

- Up to 56 I/Os that can help give an address to the different tiles, enabling scalability;
- JTAG programmable, allowing multiple interpreter boards to be programmed simultaneously;
- In-built UART, SPI, and I2C pins allow communication between the devices and enable individual configuration if needed.

The microcontroller will be the *brain* of the tile, as it will decode, interpret and generate commands to control its tile. Each microcontroller will have a specific address generated by pull-ups or pull-downs, allowing each tile to understand if the packets need to be discarded or decoded, depending on the address configuration.

4.3.4 FPGA

Throughout the architecture and design phase, it was necessary to perform a trade-off between using:

- a single microcontroller to decode the RF protocol and actuate on the varactor diodes;
- a microcontroller to decode the RF protocol and a different one to actuate on the varactor diodes;
- a microcontroller to decode the RF protocol and an FPGA to actuate on the varactor diodes.

The most suitable option was to select two different devices. This selection relates to the fact that each device must take advantage of its intrinsic properties: the microcontroller has higher processing capabilities with a more straightforward code implementation compared with an FPGA, while the FPGA can have several processes running in parallel while having an elevated number of available pins to use as PWM outputs.

This discrete hybrid architecture was chosen over a fully integrated System-on-a-Chip (SoC) that combines a processor and FPGA fabric on a single die. While an SoC could benefit board space and power consumption, the discrete approach provides several key advantages for this specific application. First, it allows for the "right-sizing" of components, selecting a microcontroller and an FPGA that are perfectly sized for their respective tasks without the overhead of an underutilised, power-consuming processor core that might be present in an off-the-shelf SoC. Second, development complexity and cost can be lower, as it leverages separate, well-established toolchains for each device. Finally, a discrete design offers greater flexibility in component selection, which is critical for sourcing space-qualified or radiation-tolerant parts that may not be available in an integrated SoC package when upscreening the system for a space application. This approach paves the way for a very compact future design and makes the chosen architecture adaptable for this research and development context.

The selected FPGA belongs to the Spartan-6 family, which provides integration capabilities with the lowest total cost for high-volume applications. It has 102 available I/Os, and it can switch

off unused FPGA memory banks, allowing it to reduce overall power consumption. The interpreter PCB has an auxiliary memory since the FPGA does not have internal flash memory. Every time the interpreter is DC-powered, the microcontroller loads the FPGA program into memory, enabling the FPGA to program itself by reading that memory.

4.3.5 Driver and Filters

The microcontroller works at 5 V, while the FPGA operates at 3.3 V. This voltage difference requires a voltage translation to ensure both devices interpret the signal correctly. In addition, the FPGA outputs PWMs between 0 V and 3.3 V, but the varactor diodes need a voltage variation between 0 V and 5 V to achieve the required phase variation of 360 degrees. There is a connection between the same voltage translator model and the FPGA outputs to provide the proper variation to feed the varactor diodes.

In addition, since the varactors need a steady-state voltage instead of a voltage variation, an RC filter immediately after the voltage translators allows the conversion of the PWM into an analogue signal.

4.3.6 Interpreter Layout

As in the case of the tile/reflectarray, the interpreter PCB required a multi-layer PCB, but in this case, the objective was to have enough space for wire routing and not to isolate the antenna part from digital/power routing. Figure 4.15 illustrates the chosen stackup for the interpreter PCB.

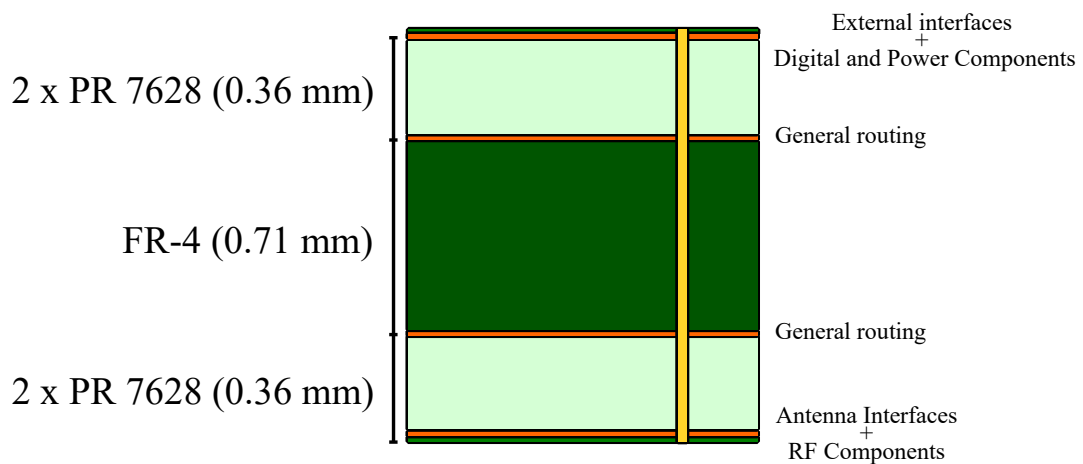


Figure 4.15: Interpreter stackup.

On the top layer, there are four interfaces: UART for debugging purposes, JTAG for the microcontroller programming, JTAG for the FPGA programming and power. Regarding the power, there is a jumper that allows selecting which connector the power will come from - the power connector or the bottom connector that connects to the corresponding tile. The interpreter board accepts up to 12 V, so right after the power connector, there is power filtering and conversion for the 5 V, 3.3 V and 1.2 V required to feed the different components. Accessing a non-populated

pin header from the top and bottom layers is also possible. Those pins have FPGA inputs/outputs and SPI signals from the microcontroller-FPGA digital interface for debugging. On the bottom layer, there are three interfaces: u.FL connector to pass the 433 MHz signal from the tile to the interpreter PCB, and two 40-pin connectors to pass power and digital signals between both boards. The 40-pin connectors have a high detent to attach the interpreter PCB to the corresponding tile mechanically. Each tile has six resistors for addressing the tile. Each resistor can be pulled up or down to set a digital 1 or 0, respectively. Those pull-ups/downs are connected to the microcontroller input pins that then read their value, allowing it to know the address of the corresponding tile. Each tile has a different configuration, so there is a single address per tile. By having six resistors, it is possible to have up to 64 tiles, allowing scalability of this solution. Figure 4.16 shows the interpreter layout for each of the four layers.

4.4 Reflectarray Design

As previously mentioned, it was possible to emulate an active cell in QUPES, optimising this structure with accurate and fast results. The reflectarray is 0.5-by-0.5 meters, which can be very time-consuming to simulate in general-purpose software. Figure 4.17 shows the QUPES simulation model. The resulting radiation patterns presented alongside this subsection refer to the reference system presented in the figure.

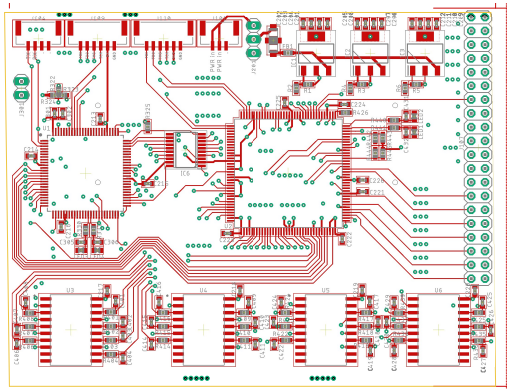
In addition to the proposed tile matrix for this antenna, the reflectarray features internal connections between tiles, requiring only a single pair of wires between the platform and the antenna for operation. In summary, the following list presents the overall SATORI reflectarray architecture:

- 5-by-5 tile, where each one has 5-by-5 unit cells and the radio control signal antenna;
- Internal power routing of 6 V to 12V to feed the reflectarray;
- Internal digital routing for programming and debugging purposes;
- Tabs and holes to create a mechanical structure to attach the reflectarray during tests.

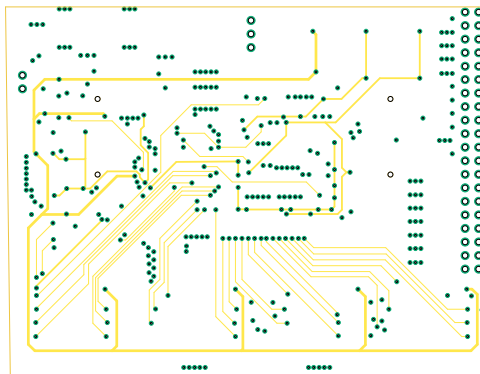
4.4.1 Reflectarray Feed

The far-field radiation characteristics of a reflectarray antenna entirely depend on correctly describing the feed characteristics. The reflectarray aperture illumination depends on the feed antenna's radiation pattern and position, as an optimum illumination of the aperture increases the efficiency of the reflectarray antenna [82]. The reflectarray aperture efficiency depends on the feed horn positions, which are directly related to the aperture illumination. The selected feed horn was a broadband dual-polarised horn antenna available at the University for the required frequency range.

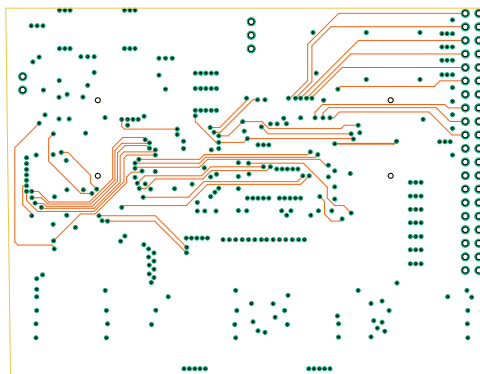
To have the most accurate possible simulation model, the reflectarray feed horn was characterised in the FEUP anechoic chamber, in terms of realised gain, phase centre, and two-cut radiation pattern.



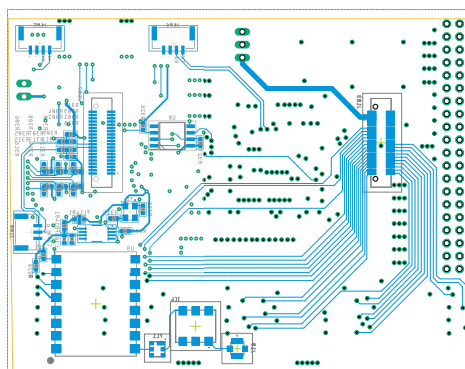
(a) Interpreter top layer.



(b) Interpreter layer 2.



(c) Interpreter layer 3.



(d) Interpreter bottom layer.

Figure 4.16: Interpreter layers layout.

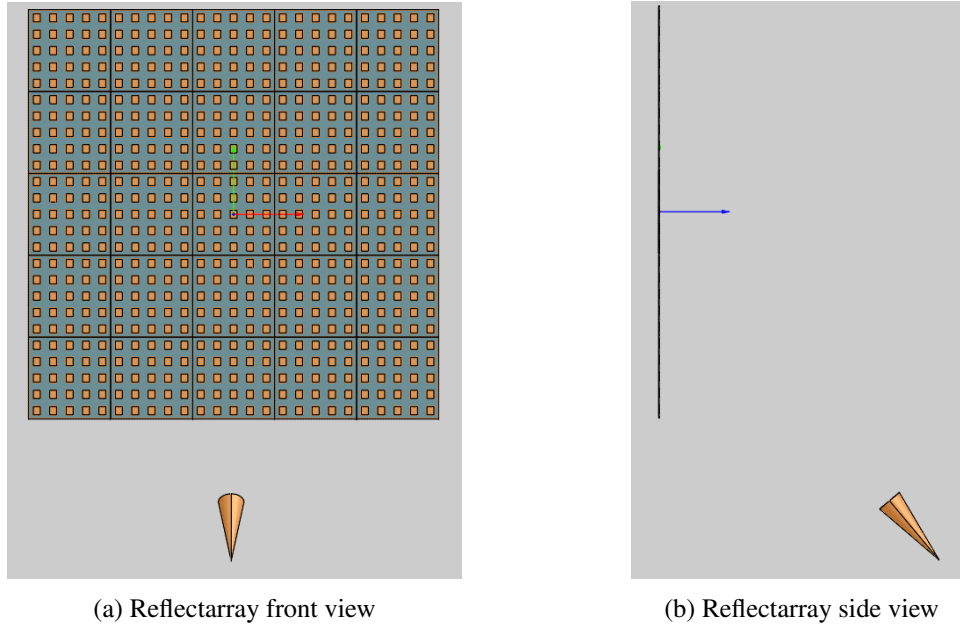


Figure 4.17: Reflectarray view with radiation pattern reference system visualisation.

As the reference antenna has an unknown performance, it is also considered an Antenna Under Test (AUT). This way, the realised gain calculation should use the 3-Antenna Method. The 3-Antenna Method involves measuring S_{21} with three different antennas, resulting in three equations with three unknown variables: the gain of each antenna. Free Space Losses (FSL) can be determined using the formula:

$$FSL(dB) = 10 \times \log_{10} \left(\frac{\lambda}{4\pi d} \right)^2 \quad (4.1)$$

Where d represents the distance between two antennas and λ the wavelength of the transmitted frequency, 9.6 GHz. The following system of equations allows the computation of the gain of the three antennas with three different measurement combinations between antennas A, B, and C:

$$\begin{cases} S_{21}^{ab} = FSL + G_a + G_b : \text{Measurement with antennas A and B} \\ S_{21}^{ac} = FSL + G_a + G_c : \text{Measurement with antennas A and C} \\ S_{21}^{bc} = FSL + G_b + G_c : \text{Measurement with antennas B and C} \end{cases} \quad (4.2)$$

For simplification purposes, the analysis assumes that the antennas point correctly in the direction of the most significant gain.

The gain of antenna A, for example, is then derived by solving for each antenna gain by interchanging equations.

After knowing the gain of antenna A, the remaining gains are trivial to determine. Applying this logic with the reference antenna as Antenna C, for example, makes it possible to compute the reference gain at boresight. This information is valuable for proceeding with the radiation pattern calculation. The analysis also assumes that the AUT phase centre coincides with the rotation

centre for simplification purposes.

To retrieve the radiation pattern, it is necessary to rotate the AUT on the rotor while taking S_{21} measurements for each angle step. With this information, one can easily determine the absolute radiation pattern values by comparing with the gain at boresight of the reference antenna and the FSL:

$$G_{AUT}(\theta) = S_{21}(\theta) - G_{REF}(boresight) - FSL \quad (4.3)$$

This measurement covered the whole azimuth angle $[-180, +180]^\circ$ in steps of 2° to achieve good measurement resolution without compromising the measurement time. Figure 4.18 shows the feeding horn radiation pattern for both ports. It is possible to verify that both ports have the same gain when pointing to boresight; however, the horizontal scan provides a broader beam. Further tests also showed a cross-polarisation isolation of around 20 dB for the frequency range of interest, and port isolation of 30 dB, which allows concluding that both ports can be used. However, it is necessary to rotate the antenna accordingly, as the reflectarray has V-Pol.

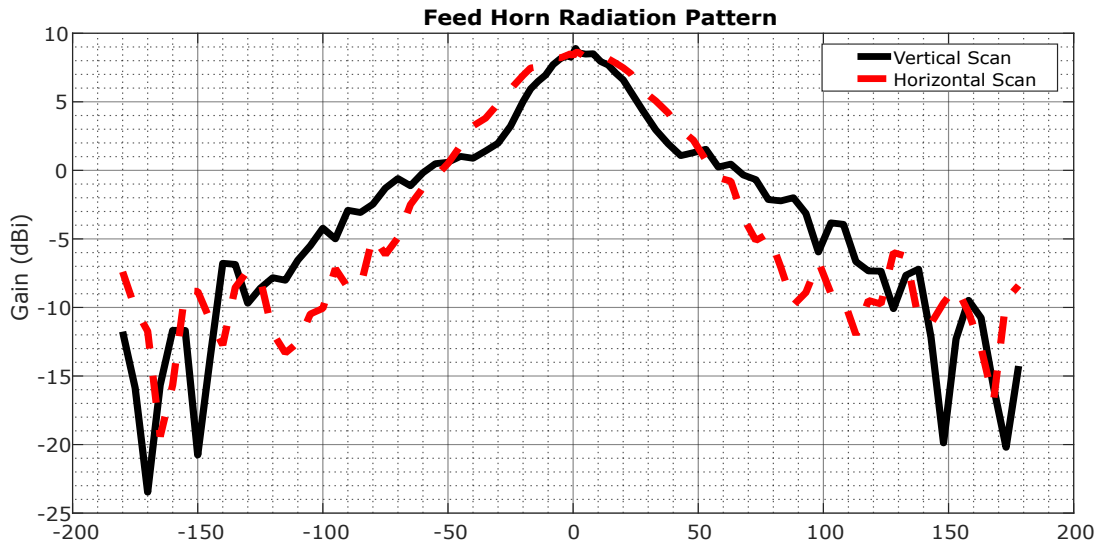


Figure 4.18: Reflectarray feeding horn radiation pattern.

The definition of the phase centre refers to the centre of curvature at the intersection between a far-field phase surface and a plane containing the horn axis. For this use case, it is essential to obtain the phase centre of the feeding horn to model its position relative to the accurately reflectarray on QUPES. Such misalignments can result in significant changes in the far-field radiation phase, potentially affecting the symmetry of the radiation pattern around its main-beam direction and the overall antenna efficiency.

A method involving iterative antenna placement allows for determining the phase centre until the S_{21} phase exhibits minimal variation. Through this iterative process, the observed phase centre is identified and placed on the axis of rotation. Knowing that point B, depicted in Figure 4.19, is the centre of rotation of the rotor. Sliding the antenna support along the x-axis allowed it to iterate

to the optimal point where S_{21} phase variation was minimal. Figure 4.20 shows the results for different iterations, allowing the finding of the feeding horn phase centre.

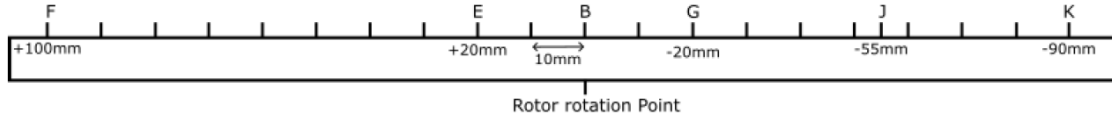


Figure 4.19: Reference system to iterate antenna phase centre.

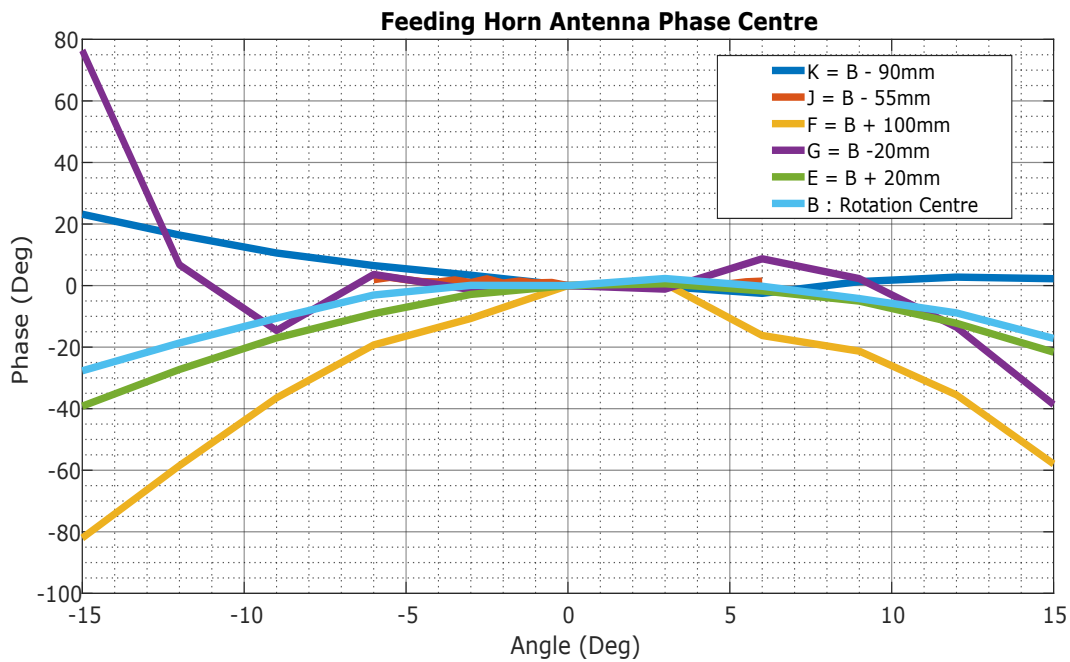


Figure 4.20: Phase centre measurement.

The initial approach to characterise the feeding horn consisted of importing its measured radiation pattern into QUPES through a .cut file, thereby providing the simulation with a realistic representation of the feed. However, an accurate description of the antenna radiation pattern requires a sufficient number of angular samples and pattern cuts, which depends on both the electrical size of the feed and the spatial variation of its radiation pattern. QUPES, as well as other TICRA Tools, can represent a tabulated feed by computing a spherical wave expansion from the supplied radiation-pattern data. Once the corresponding spherical-wave coefficients have been determined, the field can be reconstructed at the angular sampling required by the subsequent electromagnetic analysis. Consequently, supplying only a limited number of cuts does not necessarily restrict the reconstructed pattern to those cuts. Nevertheless, the accuracy of the resulting feed model remains dependent on whether the input data contain sufficient information to correctly determine the spherical-wave content of the antenna. For a rigorous spherical-wave representation, the angular sampling of the input radiation pattern must satisfy the spherical-wave expansion sampling

criterion. In the polar direction, the maximum angular spacing is given by

$$\Delta\theta \leq \frac{180^\circ}{N}, \quad (4.4)$$

where N represents the maximum polar-mode order retained in the spherical wave expansion. The required value of N is primarily determined by the electrical size of the antenna and the desired accuracy of the expansion. A commonly used estimate for the required number of polar modes is

$$N \approx kr_0 + 10, \quad (4.5)$$

where

$$k = \frac{2\pi f}{c} \quad (4.6)$$

is the free-space wavenumber, f is the operating frequency, c is the speed of light, and r_0 is the radius of the minimum sphere that completely encloses the radiating feed. Therefore, electrically larger antennas require a larger number of spherical modes and, consequently, a finer angular sampling of the measured radiation pattern. The required sampling in the azimuthal direction, ϕ , is similarly determined by the azimuthal modal content of the radiation pattern. For feeds exhibiting a simple and highly symmetric azimuthal dependence, the amount of input data can be significantly reduced. For example, when the feed is rotationally symmetric, and its field exhibits the expected sine/cosine dependence in ϕ , two orthogonal principal-plane cuts may provide sufficient information to reconstruct the radiation pattern. In the present case, however, the available measured cuts revealed noticeable differences between the two principal planes, indicating that the feed could not be accurately represented by assuming rotational symmetry. Consequently, using only two orthogonal cuts as input to QUPES could result in a reconstructed radiation pattern that differs from that of the actual feed. A complete experimental characterisation of the feed would therefore require measurements with sufficient angular resolution in both θ and ϕ to satisfy the spherical-wave sampling requirements. Such a characterisation was not available from the FEUP anechoic chamber, since it would require a properly calibrated spherical near-field measurement setup. For this reason, the available feed-pattern data were used as an initial approximation and subsequently adjusted through an iterative comparison between the simulated and measured radiation performance of the complete reflectarray.

4.4.2 Reflectarray Simulation Model

The simulation followed some considerations:

- Each unit cell has the same behaviour as the one simulated with the varactor diode, regarding losses and phase variation.
- The reflectarray has 25 independent tiles, built in the same panel but independently manipulable.

- The setup uses the exact distance and relative position between the feeding horn and the reflectarray as in the anechoic chamber measurement.
- The simulation has an equivalent feed to the one used.
- The patches could have 21 different sizes, meaning there will be 21 different PWM voltages to feed the varactor diodes - this is achievable with an FPGA generating them.
- The optimisation goal was to achieve the maximum gain towards $\theta = 0$ degrees.
- The simulation runs for a maximum of 300 iterations but stops earlier if the optimisation, based on a minimax algorithm, reaches the desired accuracy.

Typically, each simulation takes two iterations. The first one optimises towards the desired goal. However, QUPES uses a cubic interpolation between the discrete sample points of a database, so it considers a continuous patch size *vs* reflected phase curve. So, the second iteration uses the values from the first simulation and discretises them according to those used on the reflectarray. The subsection 4.4.5 details the values and the rationale behind them. The results presented in this and the following subsections already consider the discretisation.

Figure 4.21 shows the radiation pattern simulation result when optimising the reflectarray towards $\theta = 0$ degrees.

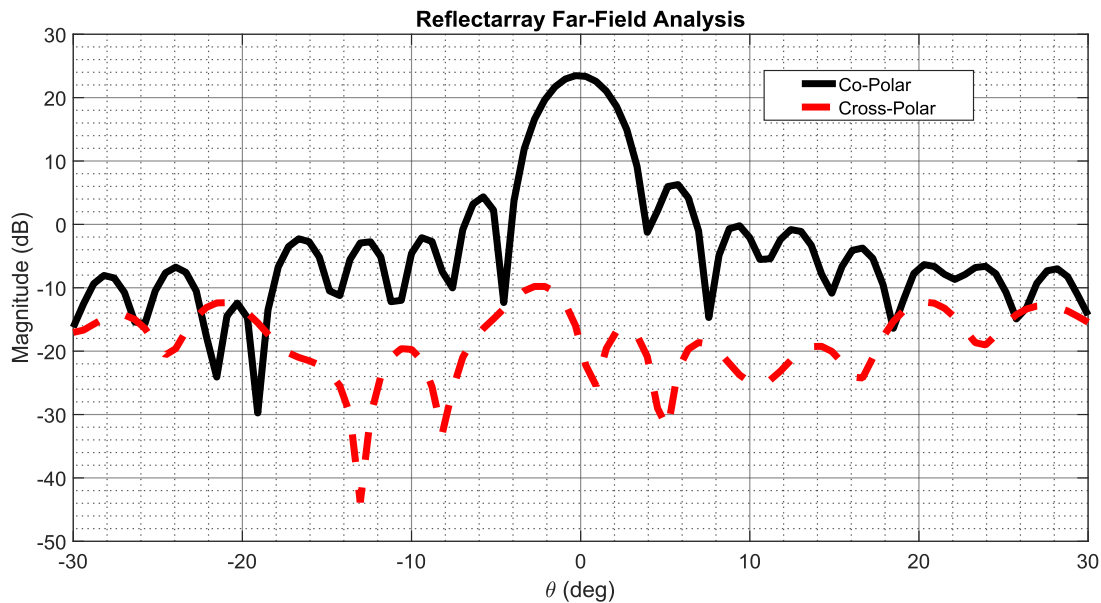


Figure 4.21: Reflectarray QUPES optimisation.

It is possible to verify that the maximum directivity points in the correct direction, with a value of approximately 23 dB. The Sidelobe Level (SLL) is more than -17 dB and symmetric along the entire pattern. The gain does not reach its maximum potential based on the reflectarray area. This result happens due to different factors, like the varactor diode losses, but mainly due to the use of the feeding horn. The inability to fully characterise the horn added uncertainties to determining

its optimal position relative to the reflectarray. If the performance of the reflectarray were the core of the thesis and not the wireless control, then the best would be to use a fully characterised corrugated conical horn antenna. A corrugated conical horn is ideal for reflectarrays because it:

- Provides symmetric, low-cross-polarisation beams.
- Offers a stable phase centre and beamwidth.
- Efficiently illuminates the array with minimal losses.
- Supports moderate to wide bandwidths.

These features and proper radiation pattern and phase centre knowledge are used on QUPES to help maximise gain, beam control, and polarisation purity - all essential for high-performance reflectarray antennas.

After the optimisation, the Uncertainty Quantification (UQ) tool from TICRA allowed the estimation of a more precise radiation pattern for the SATORI reflectarray [83]. A few details about the simulation implementation are in the Ticra Tools user manual and are listed here:

- Mean performance: What is the expected (mean) system performance?
- Variation in performance: What is the variation in the system performance?
- Deviation from nominal: How does the expected performance deviate from the nominal performance?
- Confidence intervals: With α – percent certainty, how will the system perform?
- Partial variance: How much of the variation in performance is caused by a specific variable?

After testing different varactor diodes, it was possible to verify that they could present ± 0.5 V for the same applied FPGA voltage, indicating differences in the internal resistance between the different parts. The simulation considered a uniform distribution between $[-1; 1]$ mm on top of the optimised patch size value to emulate the feeding voltage imprecision of each varactor diode. Manufacturing tolerances are likely much smaller, but this exaggerated value is a worst-case scenario to model the varactor diode variation.

Figure 4.22 presents the simulation result of the uncertainty quantification. The black line shows the most expected value, while the grey area shows, with a confidence interval of 95%, the values that the radiation pattern can have. As expected, the maximum gain drops to about 19 dB since the beamwidth increases, while the sidelobes can increase. It is also noticeable that the sidelobe level will be about -13 dB.

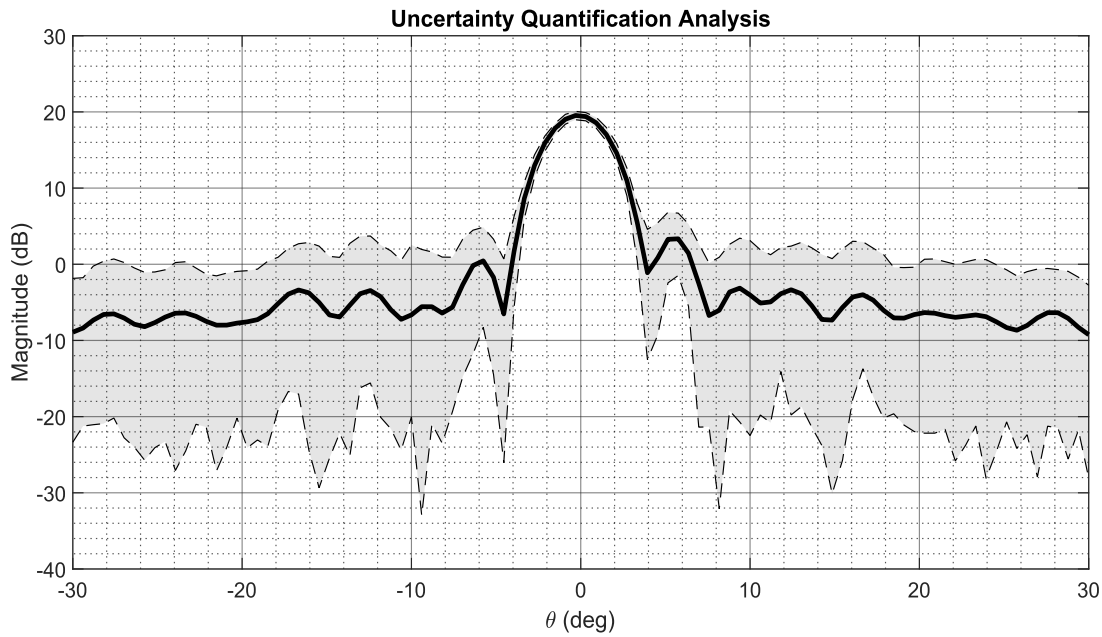


Figure 4.22: Uncertainty quantification of the reflectarray simulation.

4.4.3 Beam Steering Capabilities

As previously said, beam steering is critical for modern space-based antenna systems, particularly for SAR and satellite communications applications. This ability to adjust the main beam direction allows an increased coverage area, improved signal quality, and higher system flexibility. For SAR and communications applications, a variation between $\pm 30^\circ$ in the antenna θ axes covers the application's needs.

The reflectarray design incorporates beam steering capabilities within a $\pm 30^\circ$ range in the antenna's θ axis. The following considerations determine the range selection:

- It provides sufficient coverage for typical LEO satellite orbits;
- It balances the trade-off between steering range and antenna gain degradation;
- It accommodates the requirements for both SAR imaging and communications applications.

Beam steering occurs through individual phase control of each unit cell in the reflectarray. Applying a progressive phase shift across the array of elements steers the main beam to the desired direction. The validation of the beam steering capabilities used the previous QUPES setup, but the optimisation goal was towards $\theta \pm 30^\circ$.

- Optimisation goals for steering the beam to various angles within the $\pm 30^\circ$ range;
- Maintaining the previous antenna configuration and feed position;
- Start using the minimax algorithm for optimisation, with a maximum of 300 iterations. If the algorithm did not converge, then the simulation was repeated with a higher number of iterations.

Fig. 4.23 presents the simulated far-field radiation patterns for steering angles of $\theta = \pm 30^\circ$.

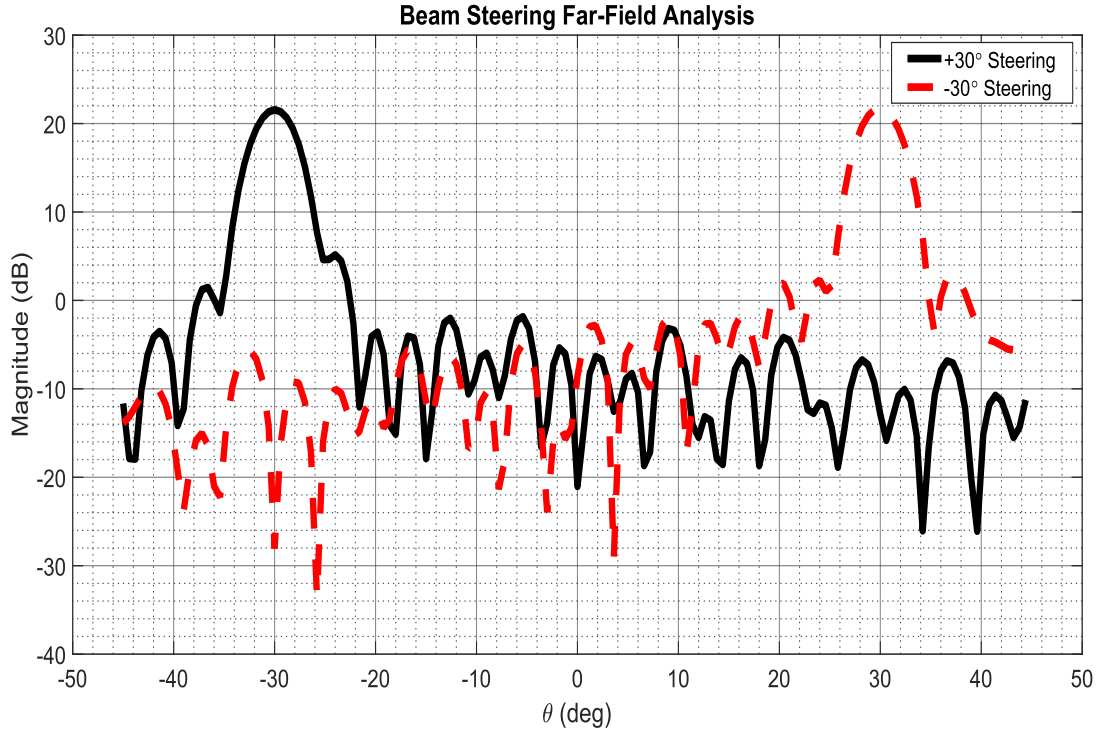


Figure 4.23: Reflectarray simulation for $\theta = \pm 30^\circ$.

Regarding the steered beams, the 3-dB beamwidth for both steered beams is approximately 10° . The slight broadening of the steered beams is consistent with the expected behaviour due to the reduced effective aperture in the steering plane. The peak gain for both steered beams is approximately 21.5 dB, representing a slight reduction (about 1.5 dB) compared to the broadside gain. This minor decrease is typical in beam steering systems and results from the smaller effective aperture at larger steering angles.

The steered beams' first sidelobes occur at approximately $\pm 20^\circ$ from the main beam, with levels of about -15 dB relative to the central beam peak. The consistency in sidelobe levels across steering angles suggests a robust design that maintains sidelobe performance even when steered. No significant grating lobes are visible within the whole angular range shown, indicating that the element spacing of the reflectarray is sufficiently small to avoid grating lobe formation for these steering angles.

The simulation results demonstrate that the reflectarray design can effectively steer the beam within the specified $\pm 30^\circ$ range while maintaining acceptable gain and sidelobe levels. This capability ensures that the antenna can meet the diverse requirements of both SAR and communication applications in a space environment.

4.4.4 Graceful Degradation

One of the strong points of this modular approach is that it allows for compensation for any possible tile lost. In that case, the entire reflectarray can be reconfigured to achieve a better radiation pattern. Unlike monolithic antenna designs, which can have a destructive single point of failure, this distributed system can tolerate the loss of one or more tiles and reconfigure the remaining active elements to mitigate the performance impact, allowing the system to operate continuously. This subsection studies the effects of losing a tile in different positions of the reflectarray, and then the result after reflectarray reconfiguration, evaluating the impact on SLL and beam pointing accuracy, which are critical to the target applications. This damage can happen, for example, if one interpreter cannot be powered anymore or has a damaged device that compromises the individual control of each unit cell. The simulation flow on QUPES consists of:

- Simulation of the entire reflectarray with no malfunctions, optimising the beam direction towards boresight to establish a performance baseline;
- Re-simulation with one tile forced into a non-responsive state (all its patches set to the same size), emulating a failure of its interpreter control circuit;
- Re-optimisation of the phase settings for all remaining functional tiles to compensate for the failed tile and recover performance.

This methodology allows for a quantitative performance analysis before and after compensation. The study considers two worst-case scenarios: the failure of a tile at the border and the failure of a tile in the centre of the reflectarray. The analysis is for a beam pointing to boresight for simplification purposes. A quick analysis showed the results are even better when tested for different steering angles.

4.4.4.1 Analysis of a Border Tile Failure

The failure of a tile at the edge of the array, Figure 4.24, represents an asymmetric fault. The immediate and reconfigured performance is analysed below.

The three plots refer to the optimal condition, the effect of losing one tile, and the result after compensation. As shown in Figure 4.25, the immediate loss of a border tile disrupts the aperture field, causing the peak gain to drop by approximately 1.2 dB. This result is a significant but not mission-ending degradation. After reconfiguring the remaining 24 tiles, the phase distribution is re-optimised to compensate for the inactive area. This active compensation successfully recovers most of the lost performance, resulting in a final gain loss of only 0.4 dB relative to the nominal state. This demonstrates the powerful capability of the active reconfiguration to maintain the primary communication link margin. High sidelobes can mask weaker targets or create image artefacts, degrading data quality for SAR imaging. Contrarily, low sidelobes are essential for high-data-rate communications to prevent interference with adjacent satellites, and precise beam

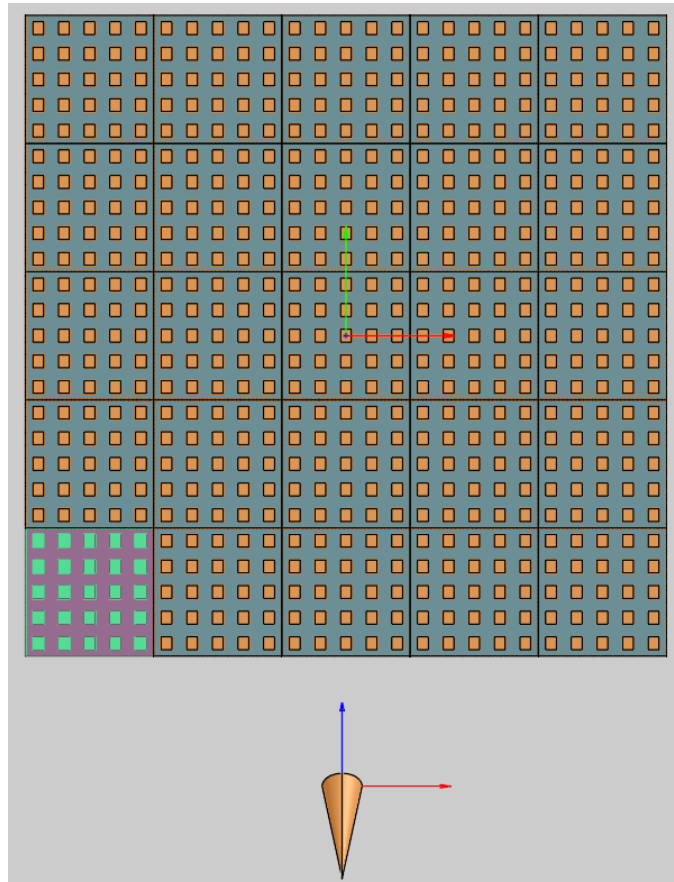


Figure 4.24: Reflectarray with malfunction simulation in the highlighted tile - border position.

pointing is critical to maintain the link. The asymmetric failure of a border tile perturbs the carefully tapered amplitude and phase distribution across the aperture. This reduces gain and raises sidelobe levels and can introduce a pointing error. Analysing the simulation results, the failure causes the first sidelobe to increase and introduces a small but significant pointing error. The re-configuration algorithm, primarily optimised for gain recovery, also attempts to restore the pattern shape. The simulation shows that reconfiguration significantly improves the gain, approximates the SLL to its nominal level, and improves the pointing error. Quantifying these trade-offs is crucial for assessing the true post-failure operational capability.

4.4.4.2 Analysis of a Central Tile Failure

The failure of a central tile, Figure 4.26, represents a symmetric but high-impact fault, as this region receives the highest illumination from the feed horn.

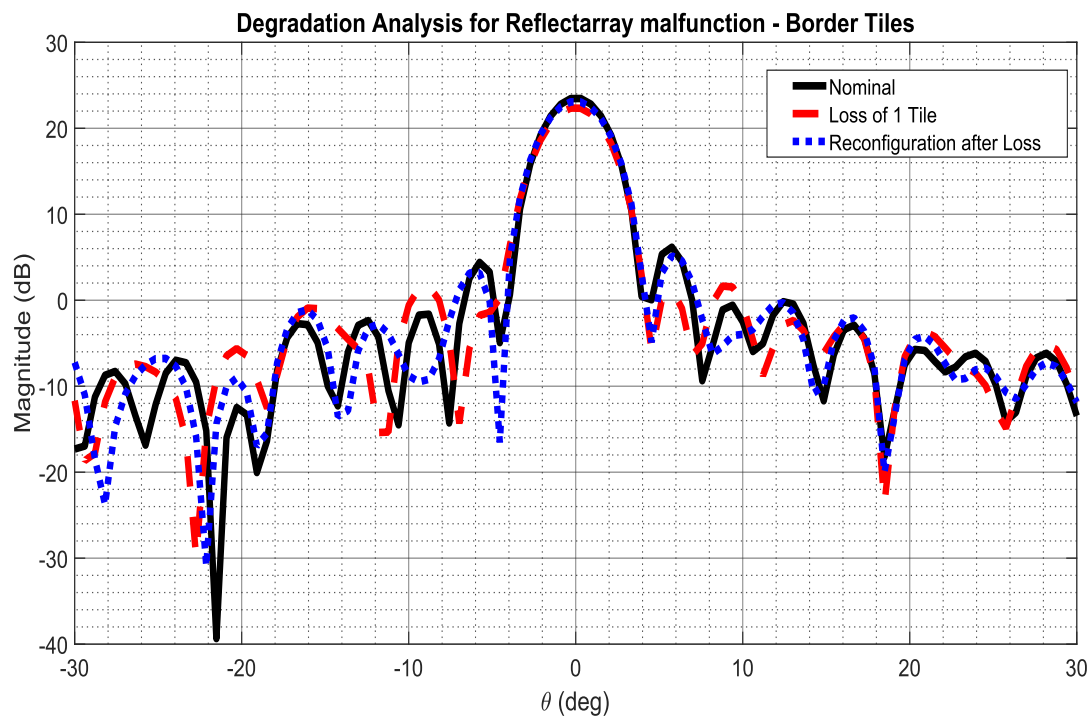


Figure 4.25: Impact of losing one border tile and reconfiguring the reflectarray to compensate.

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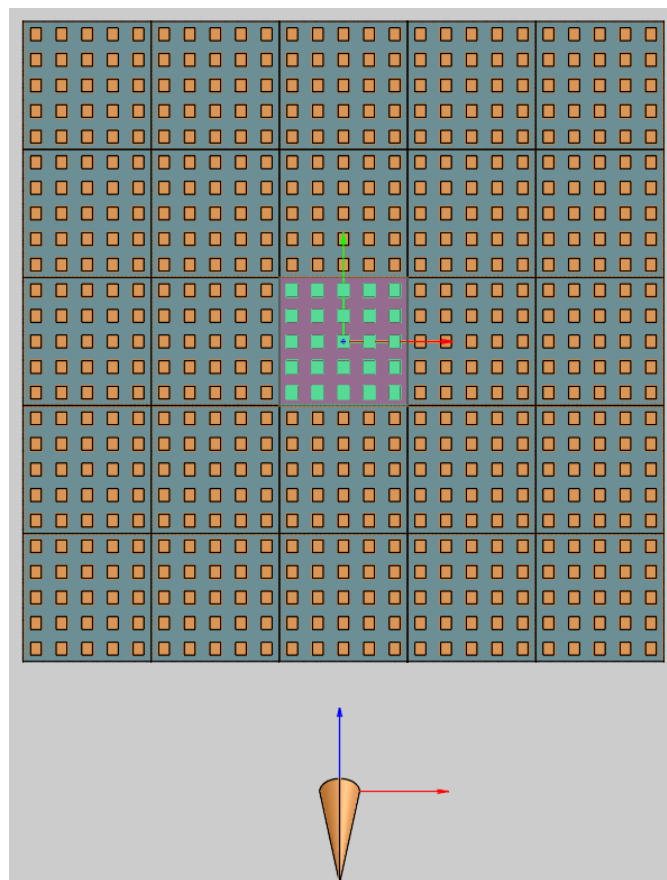


Figure 4.26: Reflectarray with malfunction simulation in the highlighted tile - central position.

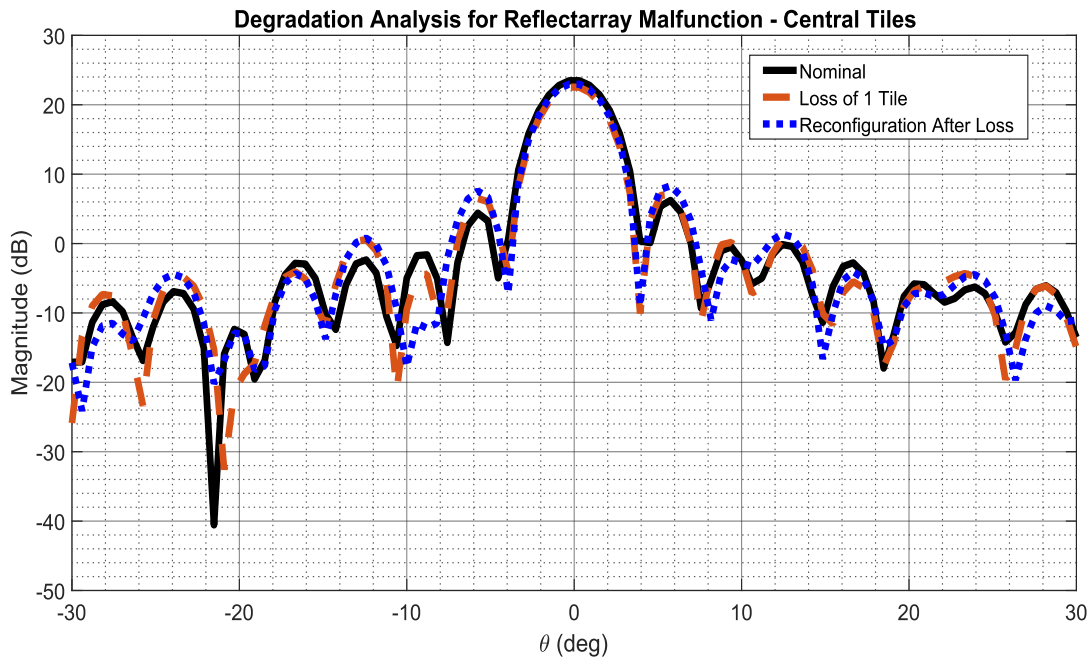


Figure 4.27: Impact of losing one central tile and reconfiguring the reflectarray to compensate.

The loss of a central tile has a slightly smaller initial impact on gain, causing a drop of approximately 1.1 dB, as shown in Figure 4.27. However, the ability to compensate is more limited. After reconfiguration, the final gain loss is 0.8 dB. This reduced recovery capability is because the central region has the most significant phase variation and contributes most to the focused beam; the surrounding tiles have less authority to compensate for this loss than a failure at the periphery.

A central failure, being more symmetric, is less likely to cause a significant beam squint. However, it creates a large "hole" in the most critical part of the aperture illumination, which can severely disrupt the sidelobe structure. As it is possible to observe, this leads to a more substantial increase in the sidelobe levels across the pattern. The reconfiguration algorithm works to reshape the beam, but the large central void makes it difficult to suppress the resulting sidelobes entirely. The analysis indicates that while pointing accuracy is largely maintained, the SLL performance after reconfiguration remains notably worse than in the border-failure case.

4.4.4.3 Summary of Graceful Degradation Performance

Table 4.1 quantitatively compares the reflectarray's performance under different failure scenarios.

Table 4.1: Summary of Graceful Degradation Simulation Results

Performance Metric	Nominal Behaviour	Border Tile Failure (Degraded)	Border Tile Failure (Reconfigured)	Central Tile Failure (Degraded)	Central Tile Failure (Reconfigured)
Peak Gain (dBi)	23.0	21.8	22.6	21.9	22.2
Peak SLL (dB)	-17.0	-17.7	-17.0	-12.0	-11.5
Pointing Error (deg)	0.0	0.53	0.17	0.04	0.02

The analysis confirms that the proposed modular and reconfigurable architecture improves performance against tile malfunctions. The system can recover a significant part of the lost gain, readjust the SLL closer to nominal levels and recover the pointing accuracy. This analysis validates the resilience of the architecture while also providing essential data for developing more advanced reconfiguration algorithms in future work that could co-optimize for gain, SLL, and pointing accuracy.

4.4.5 Reflectarray Reflected Phases Discretisation

The previous simulations considered a continuous phase control of each unit cell. Since the PWM generator is an FPGA, creating many different control voltages is easy. However, for power consumption optimisation, it is essential to understand the number of reflected phases that do not compromise the reflectarray's overall performance, while minimising the total number of different PWMs. It is then necessary to study the impact of having a discrete number of voltages to control the reflectarray unit cells.

Although simulating the unit cell with a finite number of points, 81, while running the optimisation, QUPES uses cubic interpolation between the discrete sample points of a database - meaning it considers a continuous phase curve. Before applying the reflectarray control voltages discretisation, it is good to understand where the higher cell concentrations are, instead of going straight to an equidistant distribution of points along the patch size span. Fig. 4.28 shows the results of the reflection phase for each patch size. It also includes the number of times each set of patch sizes repeats in the previous optimisation - it is important to note that in this simulation, the patch length will correspond to a voltage value. This histogram contains the patch sizes for the $\theta = 0^\circ$ and $\theta = \pm 30^\circ$ simulations, so it is representative of the entire values the reflectarray reflected phases might take. This analysis allows a practical study of where the higher PWM value density must be.

As it is possible to verify, there is a significant accumulation of values in the area of the most accentuated phase variation instead of the less variant border extremes. This is an expected result as several wavelength cycles exist in the reflectarray phase distribution for the three configurations. Analysing the result, it is possible to conclude that the area of higher phase variation shall have higher control granularity, instead of the $+180^\circ$ and -180° extremes. Translating the patch length to voltage, 6 mm corresponds to 0 V, while 12 mm corresponds to 5 V. There are 21 different PWM values. From the 21 values, 3 are between 0 V and 1 V, and 3 are between 4 V and 5 V. The remaining 15 values are equally distributed between 1 V and 4 V, focusing on the area with higher value density.

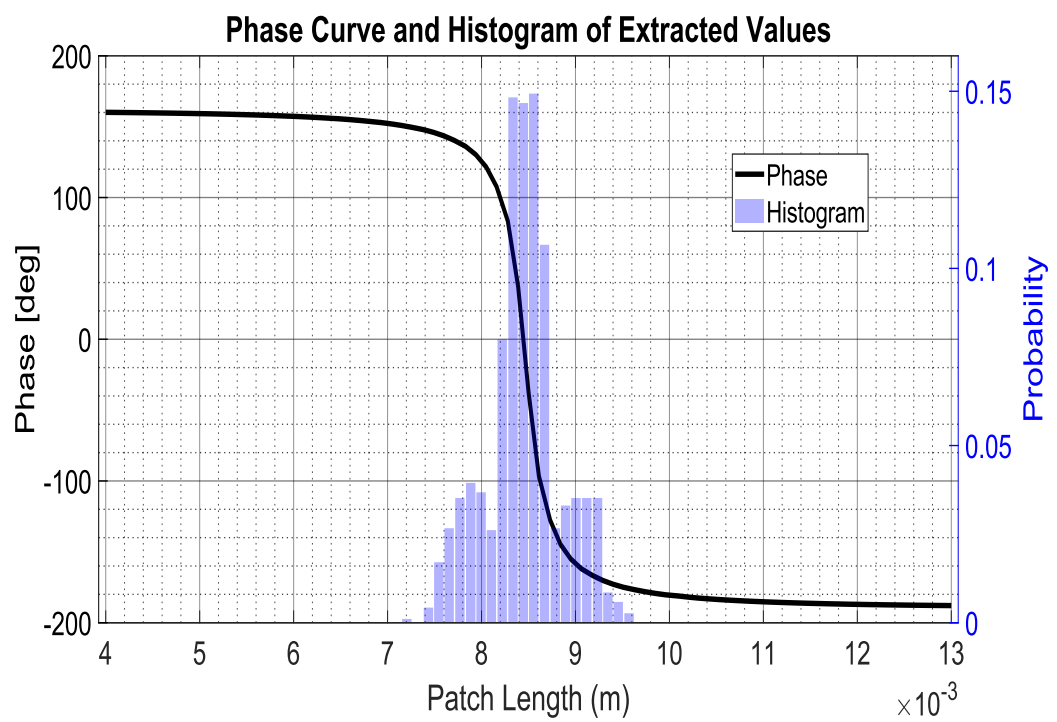


Figure 4.28: Phase curve and histogram of patch lengths distribution.

Chapter 5

RF Protocol Architecture

This chapter focuses on the developed RF protocol design, presenting requirements and design choices regarding error correction techniques. It also includes an analysis of the protocol reliability.

5.1 Protocol Design

The protocol has the following requirements:

- The protocol shall be able to transmit messages at 100 Hz (100 messages/second).
- The baud rate shall be 9600 bps.
- The control protocol must be lightweight to minimise decoding requirements on low-power microcontrollers.
- It must be suitable for power-constrained platforms, using minimal transmission and reception energy.
- The protocol can have a low data rate: antenna beam control does not require high-speed data; 1-10 Hz update rates are sufficient.
- It must allow broadcast and individual addressing: the system must enable sending commands to all tiles or specific ones.
- The protocol shall be robust to noise and interference: ensures reliable operation in non-ideal RF environments.
- The protocol must be scalable to accommodate different RF frontend configurations.

The first requirement comes from making a ratio of the message length to accommodate all the necessary fields and commands to trigger the reflectarray; the second requirement is imposed by the limitation of the TX and RX devices - a maximum data rate of 10000 bps. These requirements

impose limits on the FEC selection (message redundancy). The message size vs FEC selection allows studying which type of FEC to consider for an SNR value if needed. The protocol permitted the design of messages in two kinds of versions. Both versions have the same size and allow different antenna controls, as shown in figures 5.1 and 5.2.

	0								1								2								3							
Version 1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	Preamble 24 bits																							Version 4 bits				Polarization 2 bits		Tile Id 2 MSBits		
1	Tile ID 8 Bits								Tile ID 3 LSBits			Unit Cell ID 5 bits			Command 16 bits																	
2	CRC 8 bits																															

Figure 5.1: Version 1 of the RF protocol.

	0								1								2								3							
Version 2	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	Preamble 24 bits																							Version 4 bits				Polarization 2 bits		Polynomial 2 MSBits		
1	Polynomial 32 LSBits																															
2	CRC 8 bits																															

Figure 5.2: Version 2 of the RF protocol.

Since this is an asynchronous communication link, the preamble allows the start of packet transmission detection and also contributes to the receiver synchronisation. The preamble design must be long enough to ensure synchronisation between both ends with 1 byte of margin. The version field detects the message type, allowing up to 16 protocol implementations. Reflectarrays with double polarisation can use the polarisation field to define which components shall actuate.

In version 1 of the protocol:

- The Tile ID field defines which tile the message is for.
- The Unit Cell ID identifies the unit cell.
- The Command field specifies the desired PWM to set the varactor voltage.

In version 2 of the protocol:

- The polynomial field determines a polynomial equation that allows the interpreter to compute the PWM for each unit cell and possible drift on the pointing. This protocol version allows for sending fewer messages when controlling the reflectarray, allowing an even faster beam change. This calculation and the polynomial equation fall outside the current scope and remain reserved for future work.

Both versions of the RF protocol have a CRC-8 check applied at the end of each packet to detect corruption. In the event of CRC failure, the packet is discarded and will not change any unit cell state.

The protocol design has the option of using FEC algorithms or not. For this thesis use cases, since the RX device has high sensitivity and there is a short-distance communication link, it is not necessary to use FEC. All fields (payload) are encoded/decoded except the preamble, as its purpose is for link synchronisation only. Consequently, the flow is the following:

- The transmitter creates the message by encoding the payload and then adds the preamble.
- The receiver detects the preamble and records the number of bits equivalent to the payload message size. Decodes the received bits using the selected FEC algorithm, if applicable, and evaluates the protocol by analysing the version field.

The modulation used for RF communication is On-Off keying on a 433 MHz carrier frequency, as several devices receive baseband data and transform it into an RF signal. Operating at 868/915 MHz ISM frequencies would also be possible, reducing the required size of the RX antenna, but the availability of TX/RX devices decreases, not allowing for a good trade-off between power, cost and size. Tests done with the TXM-433-LR and RXM-433-LR devices showed compliance with the above requirements, making them the most suitable candidates for the VHF communication link.

There could be other modulation techniques and/or adding a layer to the developed code before proper FEC encoding/decoding algorithms. Still, they would not add specific advantages in this case, as the processing demand and power consumption would increase.

Although a preliminary analysis showed that FEC would not be needed, there were two algorithm implementations: Hamming (a linear code) and BCH (a cyclic code). The selection of these algorithms reflects their simplicity, ease of implementation, and suitability for decoding on a microcontroller platform. Since the distance between the transmitter and receiver is in the order of magnitude of meters rather than kilometres, more advanced and robust codes, such as those used in satellite communications (e.g., turbo codes or low-density parity-check codes), are deemed excessive for the current application involving a reflectarray antenna control from its satellite platform.

The design uses an ATMEGA2560 microcontroller and employs one of its commercially available evaluation boards during the protocol development, implementation, and debugging phases. All the developed code was in C++.

The following section presents the feasibility and performance tests for the TX/RX devices and the developed RF protocol.

5.2 RF Protocol Simulation and Test

5.2.1 Matlab FEC simulation

This simulation aims to estimate the Bit Error Rate (BER) curve using theoretical curves and simulated results. The performed simulations cover the SATORI system, which only uses On-Off Keying (OOK) modulation, and Forward Error Correction (FEC) is applied to observe its impact on BER. The selected FEC schemes are Hamming (7,4) and BCH (31,16).

The simulation consisted of creating scripts to simulate OOK encoding and decoding. On top of that, the built-in Matlab functions allowed the application of the FEC encoding/decoding algorithms.

OOK Modulation

- **No FEC:** Simulated BER for OOK modulation without FEC.
- **Hamming (7,4):** Simulated BER for OOK modulation with Hamming (7,4) FEC.
- **BCH (31,16):** Simulated BER for OOK modulation with BCH (31,16) FEC.

The simulation plots the results as BER curves against E_b/N_0 (in dB). The analysis compares theoretical BER curves with simulated results for each modulation scheme and FEC configuration.

As a further study, the analysis repeated the OOK simulation using BPSK modulation to understand their main differences. As expected, BPSK modulation shows better performance. However, the increasing coding/decoding complexity and the required electronic components do not justify its implementation.

Figure 5.3 presents simulated and theoretical curves for both modulations with different FEC configurations.

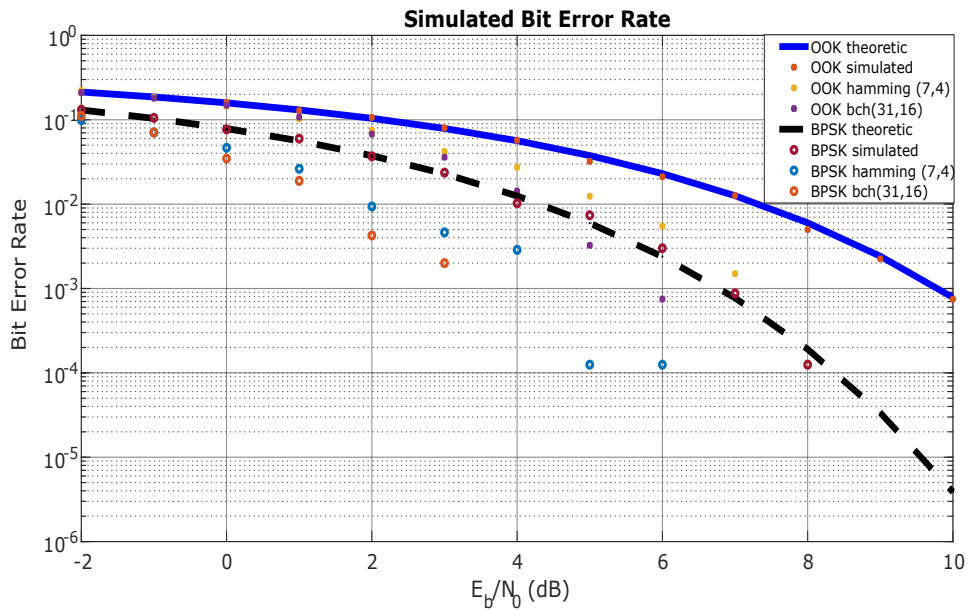


Figure 5.3: FEC simulation for different SNR using OOK modulation

As expected, the simulated results show that FEC schemes such as Hamming (7,4) and BCH (31,16) significantly enhance the BER performance for an OOK modulation. The selection of modulation and FEC schemes should align with the specific requirements of the communication system, considering factors like bandwidth, power efficiency, error correction capability and data rate. The more robust the FEC algorithm, the more resilient the communication protocol becomes.

Although OOK using BCH has the best performance, it will increase the total overhead, reduce the number of messages to send each second and increase the reflectarray configuration time. If the distance between the radio control signal transmitter on the satellite platform and the reflectarray increased, OOK using BCH would be better in the SATORI protocol.

For simplification purposes, it is important to note that this simulation assumes an Additive White Gaussian Noise (AWGN) channel that does not fully represent the expected reality of an intra-satellite EMI environment. As previously mentioned, the dominant noise sources on a satellite are more likely to be impulsive, structured, and periodic, originating from switching power supplies, high-speed digital clocks, and RF payload transmitters. This noise can cause burst errors, where multiple consecutive bits are corrupted. The current protocol, with a simple CRC-8 error detection and 0x707077 preamble, is robust enough to handle such burst errors reliably. If the environment is even noisier, while a detailed analysis is beyond the current scope, future work should consider more powerful error detection codes (e.g., CRC-16 or CRC-32) and more resilient synchronisation sequences (e.g., Barker or Gold codes) to enhance protocol robustness in an operational environment.

5.2.1.1 Protocol Reliability and Error Detection Analysis

The forward error correction and cyclic redundancy check mechanisms embedded in the SATORI RF protocol provide a quantifiable trade-off between transmission overhead and error detection capability. To assess the protocol's reliability, it is essential to characterise two complementary failure modes: the probability that a corrupted message passes undetected through the error-checking mechanism, and the probability that the system rejects a valid message due to false-positive detection. These probabilities directly inform the system-level reliability and validate the architectural choice of dedicating a separate control channel rather than attempting to multiplex configuration commands with the payload RF.

The probability of undetected error, denoted P_{ue} , represents the most critical failure mode because it results in the aperture applying an incorrect configuration that the system believes to be correct. For the CRC-8 error detection code employed in the SATORI protocol, this probability depends fundamentally on the structure of the error pattern and the generator polynomial. The CRC-8 polynomial with hexadecimal representation 0x07 generates a cyclic code with Hamming distance properties that guarantee detection of all single-bit errors, all double-bit errors, any odd number of errors, and all burst errors of length eight or fewer bits. For random error patterns that exceed these guaranteed detection cases, the probability of an undetected error approaches the theoretical limit of $P_{ue} = 2^{-r}$ where r is the number of CRC bits. For the eight-bit CRC employed in this design, this yields:

$$P_{ue} \approx 2^{-8} = \frac{1}{256} \approx 0.0039 = 0.39\% \quad (5.1)$$

This theoretical bound applies to random error patterns uniformly distributed across the message. In practice, the channel characteristics of the 433 MHz on-off keying link exhibit both

random noise-induced errors and potential burst errors from impulsive interference sources on the spacecraft bus. The CRC-8 code provides stronger protection against burst errors within its eight-bit span, meaning that the effective undetected error probability may be lower than the theoretical bound for realistic interference scenarios. However, for system-level reliability analysis, the conservative estimate of approximately 0.39% represents an appropriate design margin.

When SATORI uses FEC in addition to CRC error detection, the analysis becomes more refined because the FEC decoder can introduce its own errors when attempting to correct heavily corrupted messages. For the Hamming(7,4) code with single-error correction capability, the decoder will always produce an output even when the received word contains more than one error. If the error pattern causes the syndrome calculation to point to an incorrect bit position, the decoder flips the wrong bit. It produces an erroneous output that subsequently passes or fails the CRC check depending on the resulting bit pattern. The probability of decoder-induced error that passes CRC undetected combines the probability of uncorrectable error patterns with the CRC false negative rate:

$$P_{ue,FEC} = P(e > t) \cdot P_{ue} + P(\text{miscorrection} \rightarrow \text{valid CRC}) \quad (5.2)$$

Where t is the error correction capability of the code and $P(e > t)$ is the probability that the number of errors e exceeds the correction threshold. For Hamming(7,4) with $t = 1$, any received block with two or more errors may result in miscorrection. At the operating signal-to-noise ratio observed during testing (high SNR with PER below 0.17 percent), multi-bit errors within a single seven-bit codeword occur with very low probability, making the FEC decoder highly reliable. The BCH(31,16) code with three-error correction capability provides even stronger protection, reducing the probability of miscorrection to negligible levels at the measured channel quality.

The complementary failure mode, false positive rejection, occurs when the system discards a correctly received message due to erroneous CRC validation. This failure probability depends on the bit error rate in the CRC field itself and the probability that random bit flips in the payload produce a CRC remainder that exactly matches a corrupted checksum. For a properly designed CRC implementation where the checksum computation uses the entire payload and the generator polynomial is primitive, the false positive rate equals the probability that exactly those bit errors occur which preserve the checksum relationship:

$$P_{fp} = \prod_{i=1}^r P(\text{bit error in CRC position } i) \approx (BER)^r \quad (5.3)$$

At the measured bit error rate of less than 0.2 percent, corresponding to the observed packet error rate with No-FEC configuration, this yields a false positive probability of approximately $(0.002)^8 \approx 2.56 \times 10^{-22}$, which is small and can be neglected in system-level analysis. This result confirms that the CRC-8 mechanism will not introduce spurious packet rejections that would require retransmission overhead.

The practical implication of this analysis for the SATORI architecture is that the dominant reliability concern is the undetected error probability of approximately 0.4 percent when operating

without FEC. This probability must be compared with the system-level fault tolerance. Since each configuration command is absolute rather than incremental, a single corrupted packet affects only the targeted unit cell or tile rather than propagating errors throughout the aperture.

The measured performance validates the protocol design decision to prioritise simplicity and low latency over maximal error protection. The no-FEC configuration achieves the target message rate of 100 Hz with 72-bit packets while maintaining reliability sufficient for closed-loop beam steering. The FEC options remain available for degraded channel conditions or missions requiring higher assurance levels, demonstrating the architectural flexibility to trade transmission efficiency against error resilience based on application-specific requirements. This analysis quantifies the reliability characteristics that underpin the successful over-the-air validation campaign and establishes confidence bounds for the wireless control subsystem's contribution to overall antenna performance.

5.2.2 RF Protocol Hardware and Software Preliminary Tests

After designing, integrating, and validating all the software, system-level tests validated real use-case scenarios with the actual hardware. Figure 5.4 shows the experiment setup for the three different FEC protocol selections: No FEC, Hamming(7,4), and BCH(31,16)

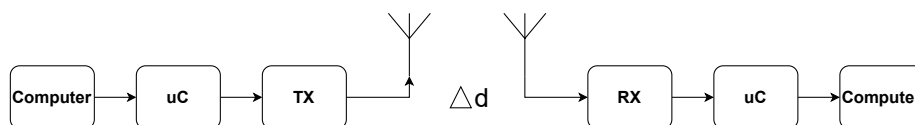


Figure 5.4: Experiment setup.

Each scenario consisted of a transmission of a total of 100 messages. All the experiments had fixed transmitted power and variable distance. All the remaining parameters were the same. For this experiment, the setup used evaluation boards of each device to reduce debug time during hardware development and troubleshooting.

Increasing the distance while keeping the remaining parameters unchanged influences the system's SNR. The idea is to find the system limits of each version, testing what could be needed depending on the distance between the reflectarray and the radio control signal TX antenna.

The receiver software listens to the RX device via UART and transmits any received packet to the computer. The transmitter firmware monitors the UART connection with the computer, transmitting the packets via the TX device.

This simple yet reliable and representative setup helped verify that the devices worked as expected. Data was successfully transmitted from computer A to computer B without FEC. After this stage, the tests evolved to validate the performance of the different protocols at different distances. Additionally, there was a monitor pin to measure the firmware packet decoding time.

Since the SATORI RF protocol is asynchronous, the devices used to transmit and receive data over the air need to *lock*. After that, they can decode the data correctly. One of the critical and first

tasks was to ensure that the selected preamble value indeed *locked* the devices before meaningful data (*payload*) is recorded by the microcontroller.

The first value selected for the preamble was 0xFFAA77. The objective is that the third byte of the preamble, 0x77, is correctly decoded by the RX device. With the support of a logic analyser, it was possible to see that this did not occur.

After carefully analysing the transacted data, it was possible to conclude that the devices needed more transitions (from high to low and vice-versa) to effectively *lock* and start to decode the received data correctly. The final value selected for the preamble was 0x707077, as seen in figure 5.5. It is possible to see that the initial bytes are not well decoded, as expected, but then the device recovers, and the bytes are well received. The red plot is the transmitted data, while the blue is the received data. The results indicate that the system failed to decode the first byte correctly while it successfully received the remaining data.

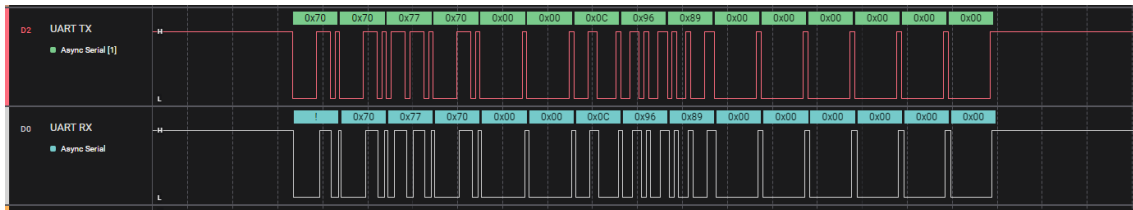


Figure 5.5: New preamble with correct data being transmitted and received

To test the protocol robustness and validate FEC influence, a test with three distances was used: 3.65 meters, 10.2 meters, and 15 meters. All the encoding algorithms were tested for the first distance, while the other two only used No FEC and BCH. This subsection focuses on the 3.65-meter distance with No FEC since it is the most realistic SATORI application. Table 5.1 presents the results of six runs without FEC.

Table 5.1: Obtained error ratio for each experiment run

Run	Error Rate
1	0%
2	3%
3	1%
4	0%
5	0%
6	2%

As it is possible to see, the error is small, even with a simple setup that had no tuned antennas. Also, considering the message length, the No FEC solution has the best overall performance, capable of transmitting 133 messages each second, which is more than the requirement of 100 messages per second.

Chapter 6

Software and Firmware Development

The software has different building blocks: transmission, reception, and debugging. This chapter explains each part individually. The transmission side generates the protocol-compliant packet from a standard CSV file, allowing it to be sent through RF. The receiver decodes the protocol and generates a packet enabling the FPGA to interpret it and control each cell individually. The debug part allows the user to communicate with the reflectarray through I^2C to command or retrieve values from the reflectarray. This part permitted direct access to the applied configuration during RF protocol development, since the RF protocol is unidirectional. Figure 6.1 shows the typical test setup and how they interact.

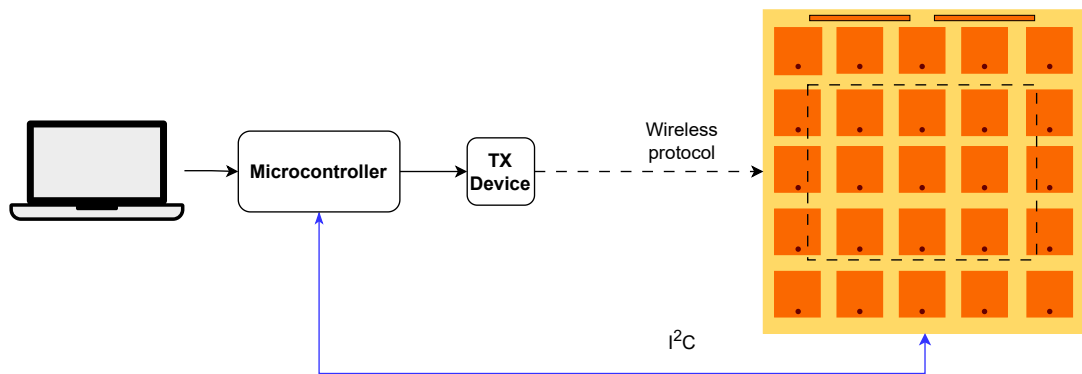


Figure 6.1: Test setup showing the software interactions.

Figure 6.2 shows the composing modules of the encoder, decoder and communications main blocks. They are responsible for creating and decoding the proper protocol packet and transmitting it, considering all the timings and flow control.

6.1 RF Protocol Packet Generation

Any embedded protocol implementation requires an error-free manipulation of bit fields within a communication packet.

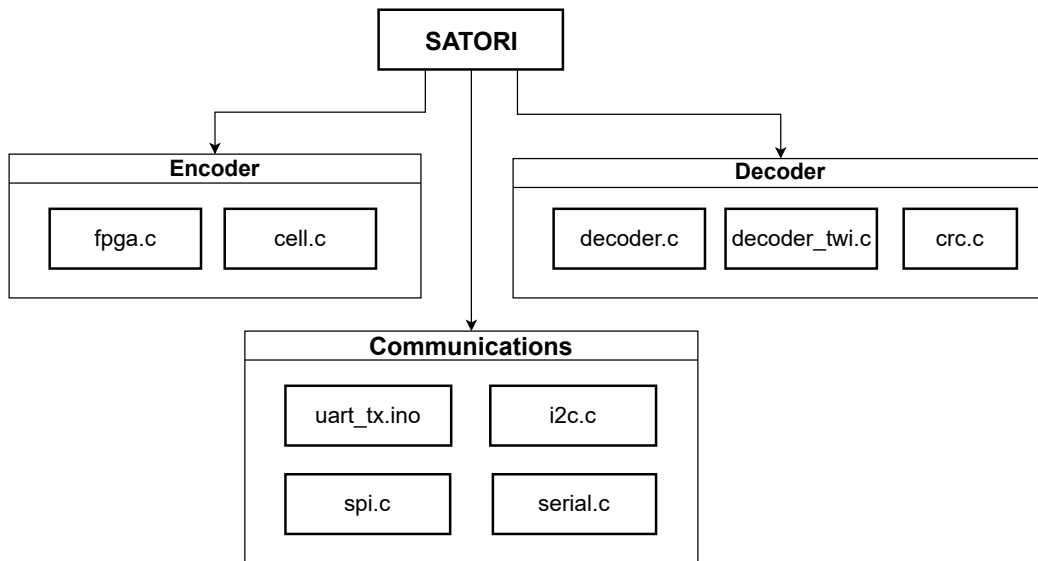


Figure 6.2: Software main blocks and modules.

In the firmware, the `decoder.c` module handles the manipulation of bit fields, and the constants and data structures in the `helper.h` header restricts the operations of this module. The `protocol_t` and `addr_t` C structures formally codify the protocol's data unit structure. This approach provides a typed, structured representation of the packet, instead of constant offsets along the code, enhancing code readability and maintainability. The `parseRxPacket` function encapsulates the core of the field manipulation logic. This function translates a raw 9-byte buffer, representing a received packet frame, into a fully populated `protocol_t` struct. This translation does not use computationally expensive loops or high-level string manipulation libraries, allowing less intensive tasks and lowering power consumption. Instead, the implementation uses direct low-level bitwise operations to achieve this. This technique translates directly to a minimal number of highly efficient machine code instructions on the target AVR architecture, guaranteeing maximum performance and a minimal memory footprint.

The extraction process for each field, as implemented in `parseRxPacket` follows the following approach:

- **Preamble and Command Fields:** The 24-bit preamble and the 16-bit command field are assembled from multiple bytes. For the command field, this involves shifting the most significant byte left by 8 bits and then combining it with the least significant byte using a bitwise OR operation. This canonical method reconstructs a 16-bit integer from two 8-bit bytes in an embedded context.
- **Single-Byte Field Extraction:** Simpler fields contained within a single byte, such as the 4-bit version and 2-bit polarisation, are isolated from the fourth byte of the buffer. This split is accomplished by shifting the byte to the right to align the desired bits to the least significant position and then applying a bitwise AND with a pre-defined mask. This mask, a binary

value with ones only in the positions of the desired bits, effectively clears all other bits in the byte, isolating the field of interest.

- **Cross-Byte Field Reconstruction:** The 13-bit `tile_id` field reconstruction is the most complex operation, handling data fields that are not byte-aligned. This field spans three separate bytes of the protocol. The firmware reconstructs the full 13-bit identifier by:
 1. Extracting the most significant bits from `p_rx_buffer[3]`, masking them with `TILE_MASK_H`, and shifting them left by `TILE_POSITION_H` to place them in their correct final position.
 2. Taking the entirety of `p_rx_buffer[4]` and shifting it left by `TILE_POSITION_M`.
 3. Extracting the least significant bits from `p_rx_buffer[5]`, masking them, and shifting them right by `TILE_POSITION_L`.
 4. Combining these three intermediate results using bitwise OR operations.

This register-level data manipulation ensures that the computationally intensive task of parsing incoming packets imposes a minimal and deterministic processing load on the microcontroller. This determinism guarantees the system meets its real-time processing deadlines, even at the maximum specified message rate. Although the microcontroller does not have more computational needs for this specific case, some protocol evolutions might. For example, as previously mentioned, version 2 of the protocol requires a polynomial computation of the current pointing position and the necessary drift to ensure a fast steering of the antenna. This use case is one example where computation efficiency is critical.

6.2 Transmitter Component

The transmitter specification offers a flexible approach to channel coding that allows for a strategic trade-off between data throughput and communication robustness. As stated in the previous chapter, the system supports three distinct transmission modes:

- **Mode 1: No Forward Error Correction (FEC):** In environments with high signal quality and low noise (high SNR), the payload data can be transmitted directly without an error-correcting code. This mode maximises the effective data rate by eliminating all redundant parity bits, which is the baseline for this thesis.
- **Mode 2: Hamming(7,4) FEC:** The system can employ a Hamming(7,4) code for channels susceptible to occasional, random bit errors. This classic, low-complexity block code can correct any single-bit error within each 4-bit data block, offering a significant improvement in reliability with modest data overhead.
- **Mode 3: BCH(31,16) FEC:** In highly challenging or mission-critical communication environments where multiple bit errors are likely, the system can utilise the BCH code. The

selected BCH(31,16) code can correct up to three bit errors within each 16-bit data block, providing a very high degree of channel resilience at the cost of a higher redundancy overhead.

The payload generation is the first step performed by the *Protocol* class, assigning the intended value to each field. If no FEC algorithm is selected, the system inserts the preamble after creating the packet payload. This procedure allows the creation of payload data for protocol versions 1 and 2.

This section analyses the encoding algorithms specified for the transmitter at the microcontroller level.

6.2.1 Block Encoding

When implementing block encoding and decoding, handling data sizes that do not naturally fit into the fixed block sizes requires an encoding algorithm. The zero padding technique solves the issue. Zero padding involves adding extra zeros to the end of the data to ensure that it becomes a multiple of the block size. This approach simplifies the encoding and decoding processes but introduces some overhead.

In this work, the method used for block coding was to limit each byte to 7 bits (in the case of Hamming) or limit each 4 bytes to 31 bits (in the case of BCH). Although this is not optimal, it ensured a seamless development.

Figure 6.3, which shows the Matlab message size computation, already considers the zero padding technique to calculate the necessary bits to transmit the data:

- **No FEC:** 72 bits
- **Hamming(7,4):** 108 bits
- **BCH(31,16):** 117 bits
- **BCH(31,11):** 179 bits

In the case of the C++ implementation, the following message length has double the size. Either for Hamming and BCH, the total message size is 15 bytes (120 bits), which corresponds to an overhead (compared to zero padding) of:

- **No FEC:** 0 bits
- **Hamming(7,4):** 12 bits
- **BCH(31,16):** 3 bits

The impact of this message size on the system is substantial since the size of the message does not satisfy the requirement of 100 messages per second. Reducing the number of messages

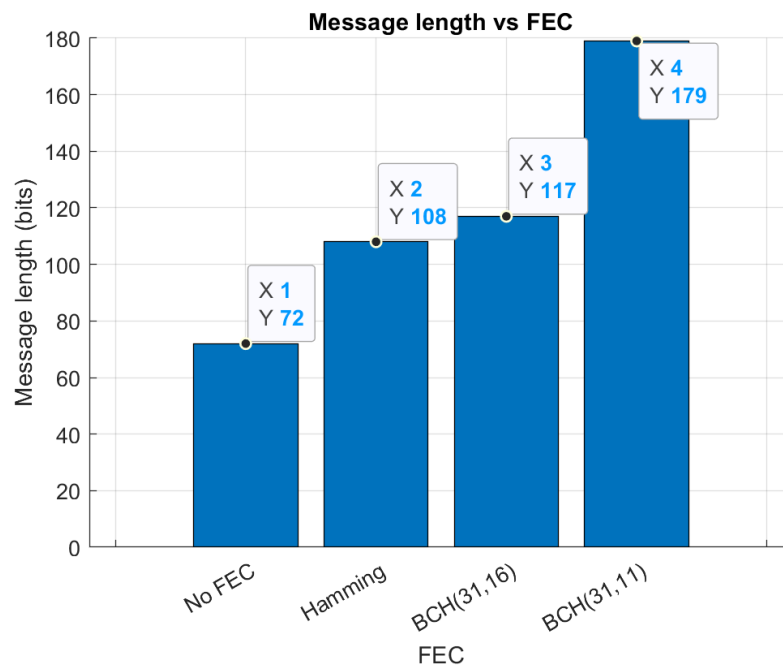


Figure 6.3: Messages length per coding algorithm

per second could be necessary for a noisier environment to obtain higher reliability in a different application.

The `Encoder` class is responsible for encoding data into an array by calling the `Hamming` or `BCH` class. The `encode` method takes four parameters:

- `data`: The input data to be encoded.
- `data_length`: The length of the input data.
- `encoded_data`: The buffer to store the encoded data.
- `encoded_data_length`: The length of the encoded data buffer.

The algorithm is as follows:

- The method first checks if the provided data and encoded data pointers are not null.
- Depending on the selected encoder, it either uses the Hamming (7,4) or BCH (31,16) encoding algorithm.
- For the Hamming (7,4) encoder, each data byte is divided into two bytes, and each part is encoded separately using the Hamming algorithm.
- For the BCH (31,16) encoder, each pair of input bytes is encoded into four bytes using the BCH algorithm.
- If encoding is successful, the method returns `SUCCESS`; otherwise, it returns an error code.

6.2.2 Hamming(7,4) Encoding

The *hamming* class encodes the data using Hamming(7,4). The code word size is 7 bits: 4 bits are the message bits, and 3 are parity bits. Hamming uses parity bits to detect bit errors if the total number of bit errors is 1. Hamming(7,4) can correct the bit error by flipping the bit in the error position.

The computation of the 3 parity bits involves a linear combination of the 4 message bits. The operation uses modulo 2. The Generator Matrix format also summarises the encoded procedure. The selected linear combination is:

Let d_0, d_1, d_2 , and d_3 represent the original data bits.

1. Parity bit $P1$ is computed as the XOR of bits 1, 2, and 3 of the original data:

$$P1 = d_1 \oplus d_2 \oplus d_3$$

2. Parity bit $P2$ is computed as the XOR of bits 0, 2, and 3 of the original data:

$$P2 = d_0 \oplus d_2 \oplus d_3$$

3. Parity bit $P3$ is computed as the XOR of bits 0, 1, and 3 of the original data:

$$P3 = d_0 \oplus d_1 \oplus d_3$$

These equations represent the linear combinations used to compute the parity bits in the Hamming code (7,4). The following code is the Hamming(7,4) encoding procedure. The function calculates the parity bits using linear combinations of specific data bits. The macros `P1`, `P2`, and `P3` define the positions of the parity bits in the encoded data:

- `P1`: Position 4
- `P2`: Position 5
- `P3`: Position 6

Compute the parity bits as follows:

- `P1` is calculated as the XOR of the original data bits 1, 2, and 3;
- `P2` is calculated as the XOR of the original data bits 0, 2, and 3;
- `P3` is calculated as the XOR of the original data bits 0, 1, and 3.

After computing the parity bits, the function fills the encoded data with the original data bits. The original data bits occupy positions 0 to 3 in the encoded data.

6.2.3 BCH(31,16) Encoding

BCH codes are more robust and can correct more errors than Hamming(7,4). The BCH(31,16) is selected since it can correct up to 3 bits in a message with a small overhead. BCH codes are cyclic, and their encoding procedure relies on modulo-2 division. The parity bits computation uses a modulo-2 division between the original message and the selected polynomial. The remainder of this operation is the parity bits of the code word. The modulo-2 division implementation is simple by using polynomial division that resorts to XOR operations.

A function `get_data_with_code_word` generates a code word from an original message using polynomial division.

A `get_top_bit` function extracts the top bit of a 32-bit data value. This function determines whether to perform polynomial division during code word generation.

A `get_data_with_code_word` function performs the following steps to generate a code word:

1. Extract Message: It extracts the 16-bit message from the original 32-bit data;
2. Polynomial Division: It performs polynomial division using the BCH (31,16) polynomial;
3. Shift and Combine: It shifts the message to the left by $n - k$ bits and combines it with the remainder obtained from polynomial division to form the generated code word.

Algorithm 1 shows the encoder pseudocode. This procedure is a high-level controller that selects one of two distinct error-correcting schemes already presented.

6.3 Receiver Component

This subsection presents the architecture breakdown of the software architecture developed for the reflectarray, integrating RF decoding, protocol parsing, and communication with the FPGA layer. The system is implemented in the C programming language, optimised for embedded environments, and validated through unit tests and hardware testing. The hardware testing consisted of preliminary software development on the microcontroller evaluation board level, toggling specific pins, oscilloscope and logic analyser signals evaluation. The design followed a modular approach to allow for easier development and troubleshooting. The global system behaviour is produced by the `main.c` module, which functions as the high-level application controller. Each C file, named after its module, contains that module's functionality. There are the hardware-related modules and the protocol ones. Hardware modules deal with low-level peripheral control and actuation/state on the device: they configure on-chip interfaces (UART, SPI, I^2C) at the register level, handle chip-selects and byte transfers, frame and send words to the FPGA to set PWM values, and maintain the current cell configuration in memory. Protocol modules deal with message structure and integrity: they parse received frames into fields (preamble, addressing with version, polarisation, tile_id, unit_cell_id, command, CRC), decode I^2C dump packets, and compute/verify an 8-bit CRC over payloads. The protocol logic modules are:

Algorithm 1 ENCODER: encode function**Require:** Input data array D , data length L_D , and selected encoder E **Ensure:** Output encoded data array D_{enc} and status code S

```

1:  $S \leftarrow \text{PARAM\_ERROR}$ 
2: if  $D$  is NULL or  $D_{enc}$  is NULL then
3:   return  $S$ 
4: end if
5: if  $E = \text{hamming\_7\_4}$  then
6:   if output buffer length is at least  $2 \times L_D$  then
7:      $i \leftarrow 0$ 
8:     while  $i < L_D$  do
9:        $\text{lower\_nibble} \leftarrow D[i] \text{ AND } 0x0F$  ▷ Process lower 4 bits of a byte
10:       $D_{enc}[2i] \leftarrow \text{HammingEncode}(\text{lower\_nibble})$ 
11:       $\text{upper\_nibble} \leftarrow (D[i] \text{ AND } 0xF0) \gg 4$  ▷ Process upper 4 bits
12:       $D_{enc}[2i+1] \leftarrow \text{HammingEncode}(\text{upper\_nibble})$ 
13:       $i \leftarrow i + 1$ 
14:    end while
15:     $S \leftarrow \text{SUCCESS}$ 
16:  end if
17: else if  $E = \text{bch\_31\_16}$  then
18:   if output buffer length is at least  $2 \times L_D$  then
19:      $i \leftarrow 0$  ▷ Input index
20:      $j \leftarrow 0$  ▷ Output block index
21:     while  $i < L_D$  do
22:        $\text{message} \leftarrow (D[i] \ll 8) \text{ OR } D[i+1]$  ▷ Combine 2 bytes into a 16-bit message
23:        $\text{codeword} \leftarrow \text{BCH\_Encode}(\text{message})$  ▷ Encode 16 bits into a 32-bit codeword
24:       Split 32-bit  $\text{codeword}$  into 4 bytes
25:       Store the 4 bytes in  $D_{enc}$  starting at index  $4 \times j$ 
26:        $i \leftarrow i + 2$ 
27:        $j \leftarrow j + 1$ 
28:     end while
29:      $S \leftarrow \text{SUCCESS}$ 
30:   end if
31: end if
32: return  $S$ 

```

- `decoder.c`: Provides the logic for parsing raw byte arrays received from the communication channel into the formally defined protocol data structure, extracting fields such as preamble, addressing (version, polarisation, tile ID, unit cell ID), command, and CRC.
- `decoder_twi.c`: Specialised decoder for Two-Wire Interface “dump” packets, parsing command sequences and validating them via CRC to ensure integrity before further processing.
- `crc.c`: Implements a table-driven Cyclic Redundancy Check (CRC-8, polynomial 0x07) calculation, serving as the primary mechanism for detecting transmission errors in serial communications.

The hardware abstraction and driver modules are:

- `spi.c`: Low-level Serial Peripheral Interface (SPI) master driver for the microcontroller, encapsulating register-level control of clock polarity/phase, bit order, chip-select signalling, and byte-level data transfers.
- `fpga.c`: Abstraction layer built on top of `spi.c` to communicate with the FPGA. It packs per-cell configuration data (pin state and PWM value) into the required 16-bit frame format and transmits it according to the FPGA’s specific serial protocol.
- `serial.c`: Manages initialisation and configuration of the Universal Asynchronous Receiver - Transmitter (UART) peripheral, forming the physical link to the RF receiver module and enabling both transmission and reception (with interrupt support). In addition to its operational role, it provides a debug output function used during development and troubleshooting to extract diagnostic information from the microcontroller to a host computer.
- `i2c.c`: Low-level driver for the microcontroller I^2C hardware in slave mode, handling address recognition, ACK/NACK signalling, and bit-rate configuration.
- `cell.c`: Provides functions to update individual unit cell configurations, interfacing with `fpga.c` to commit changes over SPI and staging outgoing data for transmission over I^2C .
- `config_status.c`: Maintains an in-memory representation of the current cell configuration (e.g., PWM values).

A central header file, `helper.h` provides a single source for system-wide definitions. It contains the formal definitions of the protocol data structures, custom type aliases, and the bit-level constants (masks and positions) that control the protocol. This centralisation is critical for preventing inconsistencies and ensuring all modules operate on a shared, unambiguous understanding of the data structures they manipulate.

Figure 6.4 shows the microcontroller flow diagram. It shows what the microcontroller does for each state and the packet parsing and integrity check when there is a received packet.

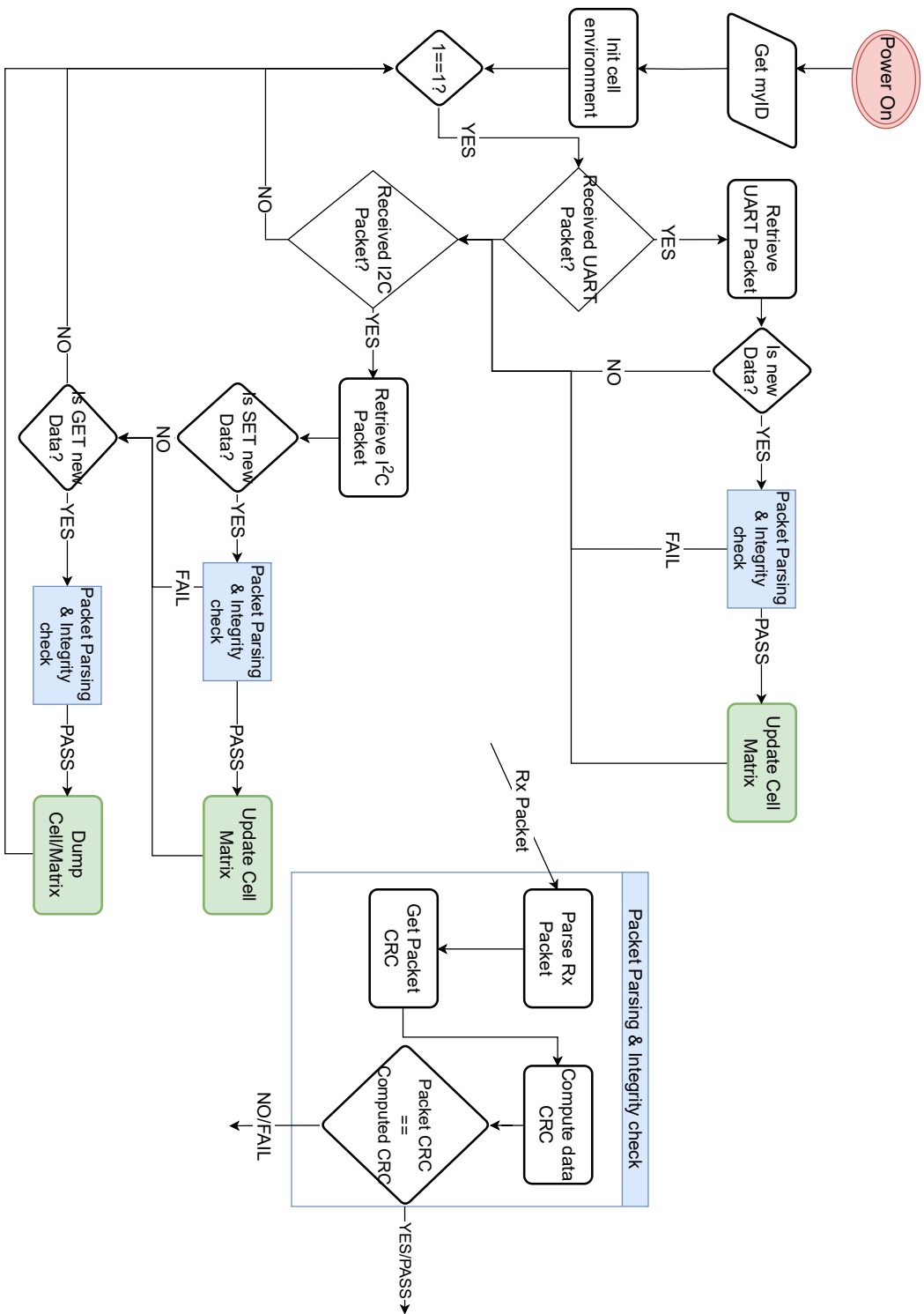


Figure 6.4: Microcontroller program flow.

The packet parsing is performed by detecting the received bytes and deciding based on whether there is a packet to process or not. The parser function extracts the transmitted payload after the packet and protocol version are detected. Two functions implementation allow to detect and parse information: *detect_packet* and *parse_packet*.

The function ‘detect_packet’ operates similarly to a state machine with two idle and ‘packet_detected’ states.

- **idle:** In this state, the function is waiting for the start of a packet. It shifts the current preamble by 8 bits and appends the new byte. If the last 8 bits of the preamble match the desired value, the state changes to ‘packet_detected’, and the byte counter resets to 3. If there is no match, the detector resets.
- **packet_detected:** In this state, the function stores the incoming byte in the ‘encoded_data’ array and increments the counter. If the byte counter reaches the ‘TOTAL_RAW_SIZE’, it indicates that a complete packet is available, resets the detector, and returns the flag ‘PACKET_AVAILABLE’. Otherwise, it returns ‘PACKET_DETECTED’.
- **default:** This state handles all undefined states by resetting the detector and returning 0.

The function *parse_packet* returns an `int8_t` value indicating the success or failure of the packet parsing process.

- `-1`: Failure to decode the data.
- `>0`: Successful CRC check and data extraction, returning the packet version.

The function initially attempts to decode the received data. If the system uses Forward Error Correction (FEC), it decodes the data using the FEC decoder. Otherwise, it copies the encoded data directly. If the decoding process is successful, the system sets the return value to `SUCCESS`. The function checks the CRC of the decoded data. If the CRC check passes, it extracts the protocol version from the data and other relevant information based on the protocol version.

- **Protocol version 1:**

1. Extracts polarisation, tile ID, unit cell address, and command from the data.
2. Updates the corresponding variables with the extracted values.
3. Sets the return value to `PROTOCOL_V1`.

- **Protocol version 2:**

1. Extracts polarisation and polynomial commands from the data.
2. Updates the `polynomial_command` variable with the extracted value.
3. Sets the return value to `PROTOCOL_V2`.

- **Default:**

1. Sets the return value to `-2` indicating an invalid protocol.

6.3.1 Block Decoding

The *Decoder* class is responsible for decoding data into an array by calling the *Hamming* or *BCH* class. The `decode` method takes four parameters:

- `encoded_data`: The encoded data to be decoded.
- `encoded_data_length`: The length of the encoded data.
- `data`: The buffer to store the decoded data.
- `data_length`: The length of the decoded data buffer.

The algorithm is as follows:

- The method first checks if the provided data and encoded data pointers are not null.
- Depending on the selected encoder, it either uses the Hamming (7,4) or BCH (31,16) decoding algorithm.
- For the Hamming (7,4) decoder, each pair of encoded bytes represents one byte of data. The method decodes each pair of bytes and stores the result in the data buffer.
- For the BCH (31,16) decoder, each group of four encoded bytes represents two bytes of data. The method decodes each group of four bytes using the BCH algorithm and stores the result in the data buffer.
- If decoding is successful, the method returns `SUCCESS`; otherwise, it returns an error code.

6.3.2 Hamming(7,4) Decoding

The decoding algorithm consists of computing the parity bit values. If they are zero, then the message received is error-free. Otherwise, there is an error. The syndrome is calculated based on the parity bit values in the error scenario. If the syndrome is different from zero, there is an error. When the syndrome belongs to the Syndrome table, the error can be corrected by flipping the bit of the error position given by the Syndrome table. The decoding algorithm uses the same linear combination used in the Hamming(7,4) encoding to calculate the parity bits. The algorithm computes 3 parity bits as a linear combination of the 4 message bits. The operation uses modulo 2.

The functions `get_data` and `decode` are responsible for extracting the original data from received data and detecting/correcting errors using Hamming (7,4) code.

The `get_data` function retrieves the original data from the received encoded data. It extracts the original 4 bits of data from the received 7-bit encoded data.

The `decode` function performs the following steps:

1. **Compute Parity Bits:** The function calculates parity bits $P1$, $P2$, and $P3$ using linear combinations of specific received data bits.

2. Compute Syndrome: It computes the syndrome using the calculated parity bits.
3. Error Detection and Correction: If a non-zero syndrome is detected, the function checks if the error can be corrected using a pre-defined syndrome table. If the error can be corrected, it corrects the received data. Otherwise, it indicates that the error cannot be corrected.
4. Extract Original Data: After error correction (when applicable), the function calls the `get_data` function to extract the original data from the corrected received data.

Considering an example where the received data is 1011101 (binary). The function performs the following steps:

1. Compute Parity Bits:

- $P1 = 1 \oplus 0 \oplus 1 \oplus 1 = 1$
- $P2 = 1 \oplus 1 \oplus 1 \oplus 1 = 0$
- $P3 = 1 \oplus 0 \oplus 1 \oplus 1 = 1$

2. Compute Syndrome: $\text{syndrome} = (1 \times 2^2) + (0 \times 2^1) + (1 \times 2^0) = 5$
3. Error Detection and Correction: Since the syndrome is non-zero, the function checks if the error can be corrected using the syndrome table. If the error can be corrected, it corrects the received data.
4. Extract Original Data: After error correction, the function calls the `get_data` function to extract the original data from the corrected received data.

6.3.3 BCH(31,16) Decoding

The implementation of the BCH(31,16) decoding algorithm used was the one from Robert Morelos-Zaragoza available at [84]. Only the decoding algorithm was extracted from Robert Morelos-Zaragoza's work, reducing the variable size to a maximum of 32 to save on allocated memory. This decoding algorithm validates the implemented BCH(31,16) encoder algorithm.

Since the algorithm from Robert Morelos-Zaragoza works with arrays and not bits, a conversion at the beginning of the decoding is necessary to convert a received 32-bit variable into a 32-byte array. The inverse is done at the end of the decoding to recover the 16-bit message.

Initially, the TX and RX programs were installed on two independent evaluation boards to mitigate the protocol software implementation at the microcontroller level. In addition, a laptop interface allowed control of the TX side and analysis of the reception side. Sections 6.4 and 6.5 show the laptop and microcontroller developments, respectively.

Algorithm 2 shows the decoder pseudocode. As explained previously, this procedure reverses the encoding process by translating an array of encoded bytes into the original data.

Algorithm 2 DECODER: decode function

```

1: procedure DECODE(encodedData, encodedDataLength, data, dataLength)
Require: encodedData  $\neq$  NULL, data  $\neq$  NULL
Ensure: Decoded data is stored in the data buffer and a status code is returned.
2:   status  $\leftarrow$  PARAM_ERROR
3:   if data  $\neq$  NULL and encodedData  $\neq$  NULL then
4:     switch (encoder_selected)
5:     case hamming_7_4:
6:       if encodedDataLength  $\geq 2 \times$  dataLength then
7:         dataIndex  $\leftarrow$  0
8:         for i  $\leftarrow$  0 to encodedDataLength  $- 1$  step 2 do
9:           status, lowNibble  $\leftarrow$  HAMMING.decode(encodedData[i])
10:          data[dataIndex]  $\leftarrow$  lowNibble
11:          status, highNibble  $\leftarrow$  HAMMING.decode(encodedData[i + 1])
12:          data[dataIndex]  $\leftarrow$  data[dataIndex]  $\vee$  (highNibble  $\ll$  4)
13:          dataIndex  $\leftarrow$  dataIndex + 1
14:        end for
15:        if status  $\geq$  0 then
16:          status  $\leftarrow$  SUCCESS
17:        end if
18:      end if
19:      case bch_31_16:
20:        if encodedDataLength  $\geq 2 \times$  dataLength then
21:          dataIndex  $\leftarrow$  0
22:          for i  $\leftarrow$  0 to encodedDataLength  $- 1$  step 4 do
23:            receivedWord  $\leftarrow$  (encodedData[i]  $\ll$  24)  $\vee$  (encodedData[i + 1]  $\ll$  16)  $\vee$ 
(encodedData[i + 2]  $\ll$  8)  $\vee$  encodedData[i + 3]
24:            status, decodedWord  $\leftarrow$  BCH.decode(receivedWord)
25:            data[dataIndex]  $\leftarrow$  (decodedWord  $\wedge$  0xFF00)  $\gg$  8       $\triangleright$  Extract high byte
26:            data[dataIndex + 1]  $\leftarrow$  decodedWord  $\wedge$  0x00FF       $\triangleright$  Extract low byte
27:            dataIndex  $\leftarrow$  dataIndex + 2
28:          end for
29:          if status  $\geq$  0 then
30:            status  $\leftarrow$  SUCCESS
31:          else
32:            status  $\leftarrow$  ERROR_DETECT_NOT_CORRECTED
33:          end if
34:        end if
35:      default:
36:        break
37:      end switch
38:    end if
39:    return status
40: end procedure

```

6.4 The Server Program

The server program is the program that connects the computer to the microcontroller evaluation board. This program reads a file with the intended messages to be transmitted and forwards them to the evaluation board. The server program uses the previously developed libraries. The user can define the transmitter packets by creating a *.txt* file with the following structure:

```
[fec] [version] [polarisation] [tile_id] [unit_cell_id] [command]
[fec] [version] [polarisation] [polynomial]
```

Where the field *fec* represents the selected FEC algorithm:

- 0: no FEC
- 1: Hamming(7,4)
- 2: BCH(31,16)

The server program reads the data received from the evaluation board and parses it according to the protocol version and selected FEC. Between 2 consecutive transmissions from the computer, there is a 1 ms delay.

A `log` class is intended to record the number of transmitted and received packets.

Code Overview The code consists of several key components:

- `PROTOCOL`: Manages packet construction, encoding, and decoding.
- `LOG`: Handles logging of transmitted and received data.
- `USB`: Manages USB communication.
- `TILE`: Represents the tile structure used in the protocol.

The main functionality of the code is to read data from a USB port, process it using the selected protocol, and log the data. The code also supports sending commands read from a file over the USB connection.

6.5 The TX/RX Microcontroller Program

The program uploaded to the evaluation board is similar to the server program in encoding/decoding messages. The `Protocol` class is used, and the difference from the *server program* is that now the data arrives via UART.

The microcontroller can have two different roles:

- Transmitter: transmit the data received from the computer to the TXM-433-LR through UART or through I^2C directly to the antenna (for debug purposes only);

- Receiver: receive the data from the antenna via I^2C to have feedback on the actual configuration.

The receiver part helps during the debug process, as the other means to test the antenna configuration is to measure the voltage of each unit cell.

The function `main.cpp` contains the main code. Below is a brief overview of its purpose and structure:

- The code manages data transmission and reception between the microcontroller board and antenna unit cells;
- The code includes several libraries and header files necessary for communication, protocol handling, and other functionalities;
- Different definitions configure the board selection, mode selection (transmitter or receiver), and FEC methods (such as Hamming or BCH);
- The code defines tasks for reading data from the USB port, transmitting and receiving data over RF, and resetting the watchdog timer;
- Set up UART, I^2C , SPI, and other peripherals' initialisation functions.

The code has several sections based on the selected mode (transmitter or receiver) and protocol configuration. Key points include:

- The code can operate in transmitter, receiver, or both, depending on the defined flags.
- Depending on the selected FEC method, the appropriate protocol is instantiated, such as Hamming or BCH.
- Separate tasks are defined for reading data from the USB port connected to the microcontroller and transmitting and receiving data. The main loop executes these tasks.
- UART initialisation functions are provided for setting up communication with the USB port and other devices.

Figure 6.5 presents the flowchart of the microcontroller that commands and receives feedback from the reflectarray.

6.6 FPGA Firmware Design and Implementation

The successful operation of the reflectarray relies on the precise and independent control of its 25 varactor-based phase-shifting elements of each tile. A dedicated firmware architecture for a Field-Programmable Gate Array (FPGA) meets this requirement. As previously mentioned, the FPGA is a specialised co-processor, offloading the computationally intensive task of multi-channel signal

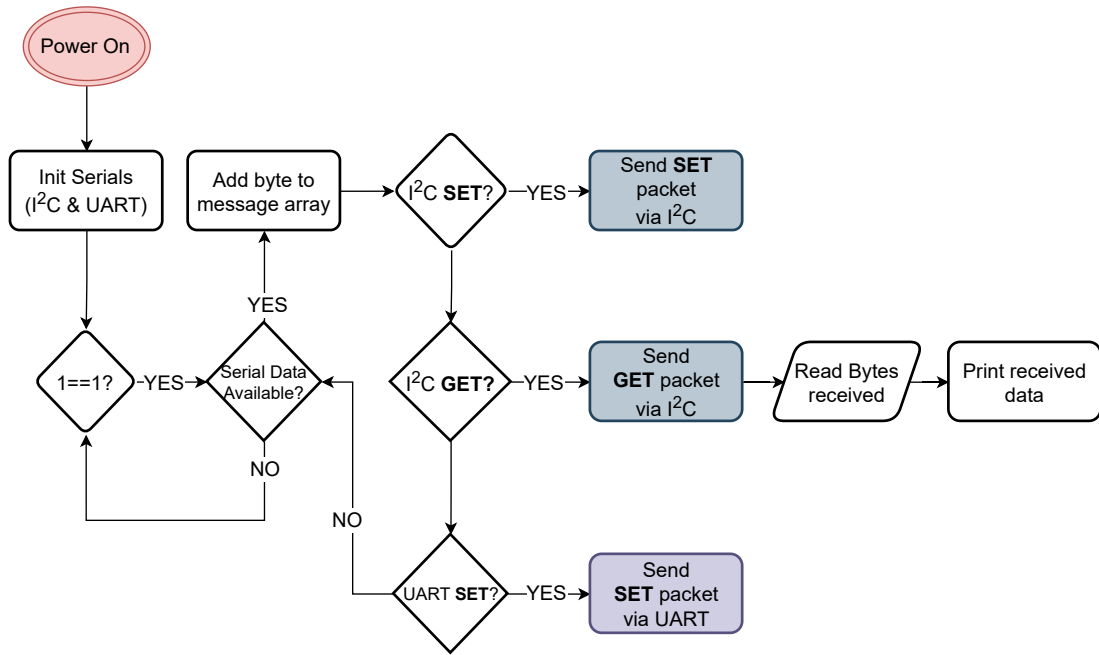


Figure 6.5: TX/RX microcontroller flow.

generation from the microcontroller. Its primary function is to receive high-level commands from a host microcontroller and, in response, generate 25 independent, high-resolution PWM signals. As mentioned in the hardware development section, when passed through a low-pass filter, these PWM signals provide the stable analogue bias voltages necessary for tuning each varactor.

This section details the FPGA firmware’s architectural design, modular implementation, and verification strategy. The design prioritises modularity for scalability, robustness in asynchronous signal handling, and clock-cycle-level precision in signal generation, all of which are critical for the scientific and operational objectives of the thesis. The design implements the entire firmware in Verilog HDL. Figure 6.6 shows the high-level hierarchical architecture.

6.6.1 Firmware Architecture and Data Flow

The firmware is architected hierarchically, comprising four principal subsystems operating in concert: the Clocking and Synchronisation Subsystem, the SPI Slave Communication Interface, the Control and Demultiplexing Logic, and the Multi-Channel PWM Actuator. This modular design is evident in the `top.v` and `sub_top.v` source files, ensuring that each functional block is self-contained, simplifying development and verification. The operational data flow is as follows:

1. A command packet is transmitted from the host microcontroller to the FPGA via a Serial Peripheral Interface (SPI) bus.
2. The SPI Slave Communication Interface receives the 16-bit serial data packet and converts it into a parallel format. Upon receiving a complete packet, it asserts a `done` signal.

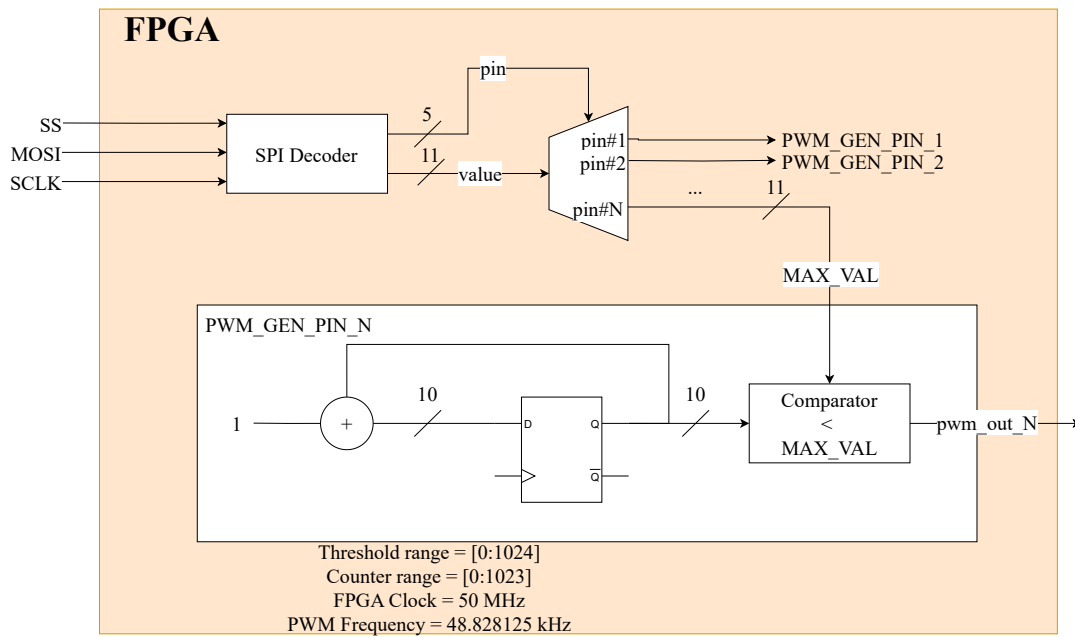


Figure 6.6: SATORI FPGA firmware high-level diagram.

3. The `done` signal triggers the Control and Demultiplexing Logic, which latches the 16-bit data. The system decodes this data into a 5-bit channel address (`pwm_id`) and an 11-bit duty cycle value (`counter_val`).
4. The demultiplexer updates the target PWM channel's duty cycle register with the new `counter_val`, leaving all other channels unaffected.
5. The Multi-Channel PWM Actuator, a bank of 25 independent PWM generators, continuously generates output signals based on their respective, most recently updated duty cycle values.

Digital logic requires a stable clock source and robust handling of asynchronous inputs throughout the development of the FPGA part:

- **Clock Generation:** A Phase-Locked Loop (PLL) generates a high-frequency and low-jitter internal system clock of 50 MHz from a more common external crystal oscillator. Monitoring the PLL's locked signal ensures the system operates only after the clock stabilises.
- **Asynchronous Signal Synchronisation:** The SPI bus signals and the external reset are asynchronous to the FPGA's internal system clock. All asynchronous inputs pass through a two-stage synchroniser, implemented in a specific module to prevent metastability. This prevention uses a two-flip-flop synchroniser that protects against setup and hold time violations, ensuring reliable data capture across different clock domains.

6.6.2 SPI Slave Communication Interface

A custom-designed SPI *slave* module manages communication with the host. This module receives a 16-bit data packet that encodes the target channel and its desired value. The 16-bit packet protocol is structured as follows:

- Bits [15:5] (11 bits): Represent the PWM duty cycle value.
- Bits [4:0] (5 bits): Represent the address of the PWM channel to be updated, allowing for the selection of one of $2^5 = 32$ possible channels (each tile only uses 25 afterwards).

Regarding the module implementation, it first detects the start of a transaction when the slave select line is asserted. It then uses a positive-edge detector on the synchronised SPI clock to generate a single-cycle enable pulse. One bit is sampled from the synchronised MOSI line on each pulse and shifted into a 16-bit shift register. After receiving 16 bits, a flag is asserted for a single clock cycle, signalling to the downstream logic that valid data is available for processing.

6.6.3 Control and Demultiplexing Logic

The `map.v` module acts as the core system of the design, responsible for interpreting the commands received from the SPI interface and routing the PWM values accordingly.

Its primary role is to act as a 1-to-25 demultiplexer. When a packet is received successfully, identified by a specific flag, the module captures the 5-bit `pwm_id` and the 11-bit `counter_val` from the SPI data bus. Based on the PWM ID, the system routes the `counter_val` to one of the 25 threshold outputs (e.g., `threshold_0`, `threshold_1`, etc.). A critical feature of this implementation is that for any given packet, the firmware updates only the addressed threshold register; all other 24 registers explicitly hold their previous state. This mechanism prevents unintended channel changes and ensures precise, targeted control. If an invalid `pwm_id` is received, a default case ensures no registers are written, preserving system state.

6.6.4 Multi-Channel PWM Actuator

The final stage of the firmware is the generation of the analogue control voltages, achieved through 25 instances of a digital PWM generator. The `actuator.v` module is a structural wrapper, instantiating 25 copies of the `pwm_gen.v` module. This one-to-one mapping provides a clean and scalable architecture where each PWM channel operates independently. The core of the signal generation lies within the same module and consists of a free-running 10-bit counter and a magnitude comparator:

- The counter increments on every rising edge of the 50 MHz `clk_sys`, cycling through values from 0 to 1023. This process creates a fixed-period digital ramp.
- The comparator continuously compares the instantaneous value of the counter against the programmable 11-bit threshold value.

- The PWM output is asserted high (1) if counter < threshold and low (0) otherwise.

This implementation results in a PWM signal with the following precise characteristics:

- Resolution: The 10-bit counter provides $2^{10} = 1024$ discrete steps, controlling the duty cycle with a resolution of $1/1024 \approx 0.0977\%$. The 11-bit threshold input allows for values from 0 to 1024, enabling duty cycles from 0
- Frequency: The clock frequency and the counter's range determine the period of each PWM cycle: $T_{PWM} = 1024 \times T_{clk} = 1024 \times (1/50 \text{ MHz}) = 20.48 \mu s$. This yields a stable PWM frequency of $f_{PWM} = 1/20.48 \mu s = 48.828125 \text{ kHz}$, which is well above the operating frequency of the varactor control circuitry, allowing for effective low-pass filtering.

6.6.5 Design Verification

The verification process used extensive tests to ensure the firmware's functional correctness and robustness. These tests moved from unit-level testing to complete system integration, using test benches to automate the validation process.

Table 6.1: FPGA Module-level test benches.

Test Bench	Module	Description
tb_spi.v	spi.v	Simulates bit-wise SPI communication and validates correct extraction of pin/value fields.
tb_pwm_gen.sv	pwm_gen.v	Applies a range of duty cycle values and checks output timing using assertions.
tb_actuator.sv	actuator.v	Verifies routing behaviour for each pin selection and confirms encoding correctness.
tb_sync.v	sync.v	Simulates metastability conditions and verifies signal stabilisation across clock domains.
tb_pos_edge_det.sv	pos_edge_det.v	Tests correct edge flag generation under varied toggling rates and transition sequences.
tb_map.v	map.v	Validates pin mapping logic using exhaustive and randomised input patterns.
tb_subtop.v	sub_top.v	Performs end-to-end simulation: SPI command reception through PWM signal output on selected pins.

All test benches share common verification features:

- Time-based stimulus using `#delay` mechanisms to simulate real-time behavior.
- Self-checking assertions to enable automated pass/fail verification without manual intervention.

- Waveform inspection for manual analysis and timing validation.
- Corner case coverage including:
 - SPI back and forth signal exchange without delays.
 - Edge conditions such as `value = 0` (0% duty cycle) and `value = 1023` (100% duty cycle).

The simulation results confirmed the correctness of signal transitions, timing alignment across modules, routing consistency, and robust operation under reset and asynchronous conditions. The test benches give confidence in the reliability and scalability of the final design. In addition to the performed tests, several pins were routed to available pin headers in the interpreter PCB to support debugging with the support of oscilloscopes and logic analysers.

6.7 System-Level Timing and Latency Analysis

It is necessary to estimate the latency since the command is issued to the physical response to understand if the system meets the message rate requirements. The requirement of a 1-10 Hz update rate implies a total latency budget of 100-1000 milliseconds for the entire control chain to execute a command. This total latency, T_{total} , results from the sum of several sequential delays:

$$T_{total} = T_{RF} + T_{\mu C} + T_{SPI} + T_{FPGA} + T_{filter} \quad (6.1)$$

Where:

- T_{RF} , RF transmission time: The time to transmit the command packet. For a 72-bit packet (No FEC) at 9600 bps, this is $72/9600 \approx 7.5 \text{ ms}$.
- $T_{\mu C}$, microcontroller processing time: The time for the ATMEGA2560 to receive the bytes via UART, detect the packet, decode the protocol, check the CRC, and formulate the SPI command. Given the 16 MHz clock speed and efficient bitwise implementation, this is estimated to be under 1 ms.
- T_{SPI} , SPI transfer time: The time to transfer the 16-bit command to the FPGA. At a typical SPI clock of 1 MHz, this is $16/1000000 = 16 \mu s$.
- T_{FPGA} , FPGA processing time: The time for the FPGA to demultiplex the command and update the PWM duty cycle register. This command occurs within a few clock cycles of the 50 MHz system clock, making it negligible ($< 1 \mu s$).
- T_{filter} , RC filter settling time: The time for the RC low-pass filter to convert the new PWM signal into a stable DC voltage. The settling time to within 1% of the final value is approximately 5 times the time constant ($5\tau = 5 \times R \times C$). For the chosen component values of $R = 10 \text{ k}\Omega$, $C = 1 \mu F$, then $\tau = 10 \text{ ms}$, the settling time would be approximately 50 ms.

Summing these components gives an estimated total latency of approximately $7.5 + 1 + 0.016 + 0.001 + 50 = 58.5 \text{ ms}$. This value is within the 100 ms lower bound of the required performance budget, confirming that the system meets its real-time control objectives.

The analysed latency refers to the worst-case scenario where the control applies to each unit cell. By having tile-to-tile control or even control of the entire reflectarray at once with broadcast messages, the latency and, therefore, the control rate decrease further.

Chapter 7

Manufacturing Prototype and Experimental Results

This chapter presents the obtained results for both antenna performance and wireless control. It states the method, the results together with its justification, and a brief conclusion.

The experimental campaign validates that the proposed wirelessly controlled, modular reflectarray achieves electronic beam steering of $\pm 30^\circ$ with the developed low-latency RF wireless control protocol.

As previously mentioned, the antenna is a $[0.5\text{ m} \times 0.5\text{ m}]$ modular reflectarray composed of 25 tiles with 25 unit cells per tile, where each cell uses a varactor-loaded resonant element with PWM-to-bias conversion providing 21 non-uniform phase steps. Figure 7.1 shows the manufactured full-scale reflectarray in Rogers RO4003C substrate.

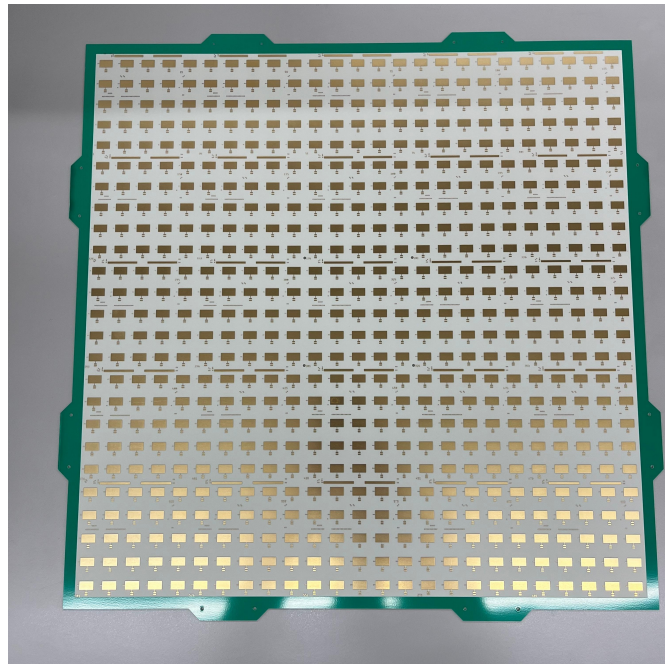


Figure 7.1: Manufactured reflectarray.

The reflectarray required two independent tests:

1. Over-the-air tests of the wireless link to test the actual control use case. The metrics are packet error rate, meaning the number of wrong or discarded packets in the complete reflectarray configuration.
2. Far-field pattern measurements at ESTEC using Compact Antenna Test Range (CATR). The gain computation method uses an antenna substitution against a calibrated standard-gain horn. The authors report peak gain, 3-dB beamwidth, SLL, Cross-Polarisation Discrimination (XPD), and pointing error.

7.1 Ground Support Equipment

A stable setup that ensures repeatability without constant calibrations is required to control the reflectarray. This subsection presents the test support hardware and software developed to guarantee an easy way of testing the reflectarray, allowing its control and to receive configuration feedback.

7.1.1 Hardware

A transmitter must exist on the platform to send the wireless command and configure the reflectarray. As mentioned, the TXM-433-LR is the selected device to support this need. As such, the device was mounted on a simple PCB to allow easy access to all its interfaces. Also, to enable a wider voltage input range, a low-power regulator at the power input ensures an input voltage from 5 V to 12 V that regulates its output to the required 3V3. On the RF side, an SMA allows for an antenna connection. Lastly, a digital interface connecting to a microcontroller that sends the modulated protocol to the TXM-433-LR. After receiving the analogue signal, this device acts as an upconverter and RF power amplifier, translating a baseband signal to an RF one. Although this is a simple setup, this PCB enables an easy setup installed in a different laboratory or an anechoic chamber.

7.1.2 Reflectarray Control App

An app was developed to facilitate the reflectarray control and improve the user experience. It allows a transparent configuration of the reflectarray by computing the voltage to phase configuration, the wireless transmission, and the interpreter electronics. It provides:

- Configuration of the reflectarray from a pre-defined comma-separated values (CSV) file listing `tile_id`, `unit_cell_id` and `voltage`;
- Configuration of the reflectarray with the theoretical values obtained with [2.1](#), by providing the feed (x, y, z) coordinates and the desired (ϕ , θ) pointing;
- Retrieval of configuration feedback from the aperture to validate what was effectively applied;

- Computation and visualisation of a theoretical per-cell voltage matrix for a target beam configuration, which can then be exported or transmitted directly;
- Numerical and graphical comparison between the reflectarray QUPES optimisation and theoretical configuration.

Figure 6.1 already illustrates software-hardware interactions at a high level and Figure 7.2 shows the application structure. The app runs on a laptop and communicates with a microcontroller board via USB.

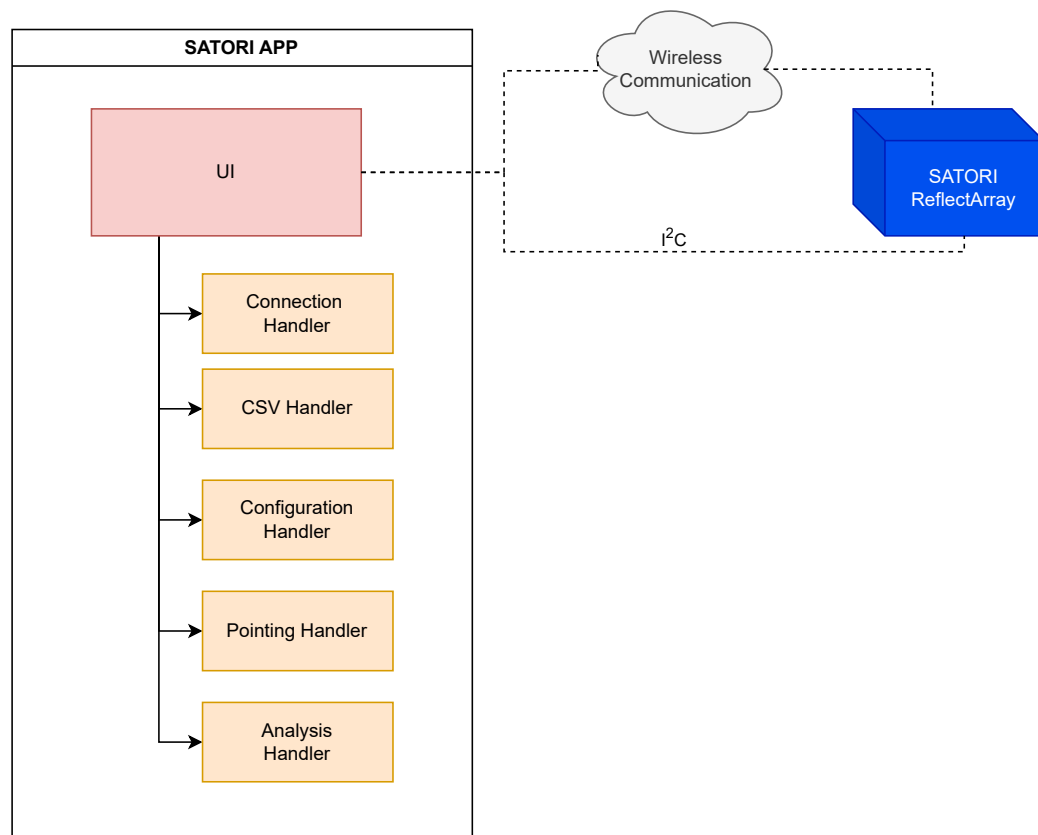


Figure 7.2: Control application structure.

From the app's perspective, a configuration cycle follows four steps:

1. Read the user-provided CSV describing per-cell settings - the encoder/packet generator supports CSV sources and builds protocol-compliant frames; or generate the configuration matrix by having the feed position and the pointing direction.
2. Convert each per-cell command into protocol frames (preamble, version, polarisation, addressing, command, CRC) and stream them over UART to the TX path. The microcontroller forwards the stream to the UHF transmitter module.

3. On each tile, the interpreter decodes the frame, updates the addressed PWM channel via SPI to the FPGA, and the RC network converts the PWM duty cycle into the varactor bias voltage.
4. Upon user request, the app queries the array over the debug I^2C link to obtain the applied PWM/voltage map per tile for verification. This mechanism allows for comparing the actual reflectarray configuration to the one sent, identifying possible deviations.
5. In addition, it is also possible to individually configure a specific reflectarray unit cell, tile or set of tiles at once.

The app accepts either a flat list or a matrix representation.

- For the first, it reads one row per cell with `tile_id`, `unit_cell_id`, `voltage_V` fields. The voltage is given in volts, referring to the 0–5 V bias range used by the varactor network. Example:

```
tile_id,unit_cell_id,voltage_V
7,11,4.7
7,12,1.99
7,13,0.5
...
```

- Regarding the matrix CSV, it reads a dense $N_{\text{tiles}} \times N_{\text{cellsPerTile}}$ matrix (row-major) of voltages. The app reshapes and emits the corresponding flat list internally.

Figure 7.3 shows the flowchart of the control application for a typical application where a pre-configured CSV file is loaded to configure the reflectarray.

Figures 7.4 and 7.5 show the Graphical User Interface (GUI) of the reflectarray control application. As it is possible to verify, it allows per-cell configurations to be directly inserted by the user, as well as pre-defined CSV configurations. It also allows feedback from the entire reflectarray configuration or individual tiles to be received. To open the control menu for a specific tile, as shown in Figure 7.5, the users only need to press the tile they want to control on the main menu.

During transmission, voltages are mapped to the FPGA threshold register domain using the calibrated 0 - 5 V to 0 - 1024 duty-cycle relation (11-bit threshold, 10-bit counter). This method preserves the practical 21 non-uniform phase steps selected for this prototype while remaining compatible with finer PWM resolution for future variants.

The app reuses the encoder libraries developed in Chapter 6 to assemble frames with optional FEC (none, Hamming(7,4), or BCH(31,16)) and CRC-8 over the payload. Packets are streamed at 9600 bps to the TXM-433-LR modem through the microcontroller. The design meets the message-rate and latency targets: with No-FEC frames (72 bits), the end-to-end delay per update is dominated by the RC settling time and remains below the 100 ms requirement.

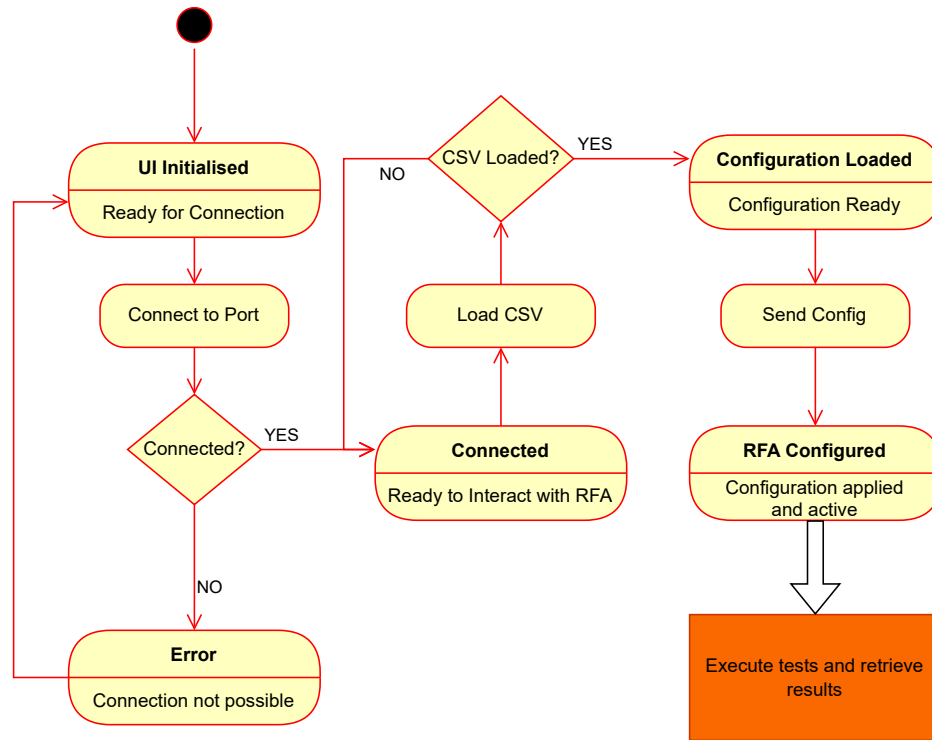


Figure 7.3: Control application flowchart.

The app can retrieve a dump over the I^2C debug bus for configuration validation. Each tile returns its current per-cell thresholds/PWM codes, which the app parses and compares against the commanded set. The interface provides:

- per-cell match/mismatch highlighting and absolute/relative error in volts and duty cycle;
- tile-level summaries and a global configuration accuracy metric;
- exportable logs (CSV) for traceability across campaign runs.

As the following section will explain, this was the mechanism used in the experimental campaign to verify end-to-end integrity (commanded vs. applied), and it achieved a perfect match across the 6250 checked unit-cell states in the dedicated validation runs.

As previously explained, theoretically estimating the required phase for each unit cell is possible. The estimator computes the aperture's target reflection phase distribution for a desired steering direction (boresight and $\pm\theta$ along principal planes for this demonstrator), then maps phase to bias voltage using the unit-cell phase–voltage characteristic and the project's discretisation strategy. The workflow is:

1. Given the array geometry and feed placement, compute the required reflection phase per cell to point the main beam at the requested (θ, ϕ) .

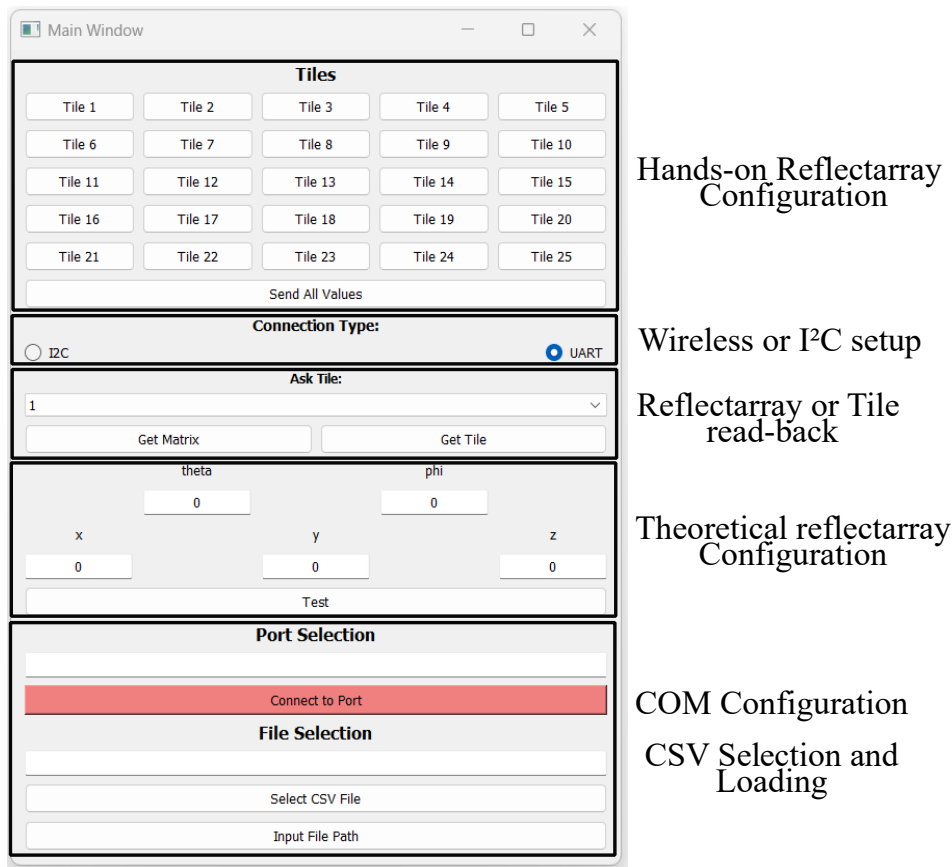


Figure 7.4: Control Application Graphical User Interface.

2. Project each target phase onto the 21-step, non-uniform set selected from the EM simulation to minimise pattern degradation while saving power and command bandwidth.
3. Apply the calibrated inverse phase–voltage look-up to obtain the per-cell bias values in 0–5 V, then convert to PWM thresholds for transmission.

The estimator can output the result as a CSV compatible with the app’s ingest stage or transmit it directly. The app stores the steering target, quantisation mode, LUT version, and the exact CSV used for TX alongside each run for repeatability and saves it into the CSV filename.

The GUI exposes four primary actions: Load CSV / estimate for a given feed position and pointing direction, send command, receive feedback through I^2C and compare with the sent configuration. It also provides additional plots with the configuration sent to allow quick diagnosis and comparison between QUPES and theoretical configurations. Figure 7.6 presents a possible output extracted with the control app. The comparison considers both the phase distribution and the control voltage level. As can be seen, the graphic stain between QUPES and the theoretical outcomes is similar. This result allows to conclude that configuring the reflectarray with the theoretical configuration would already provide a significant result. Nevertheless, as expected, there are differences since QUPES offers an optimised configuration that considers several factors, such

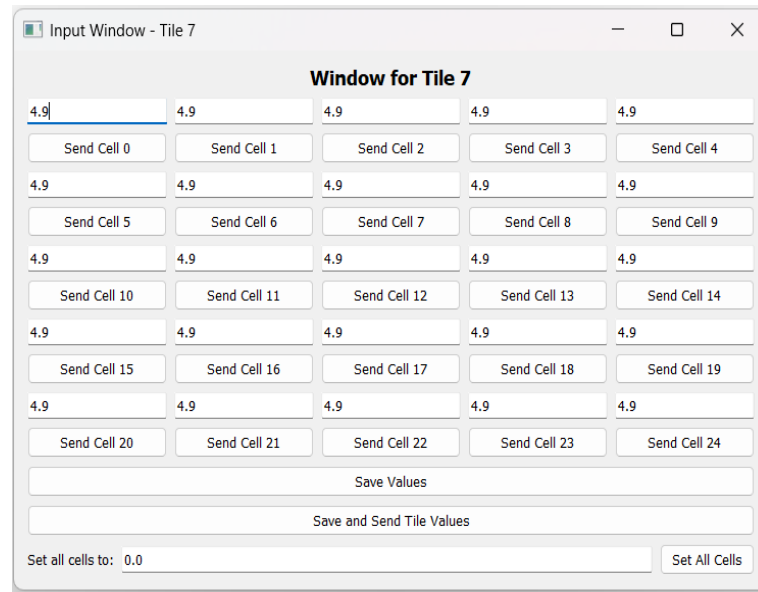


Figure 7.5: Control Application Graphical User Interface for unit cell configuration.

as the inter-element crosstalk, minimising the number of cells in the most lossy area. In addition, the phase reference, ϕ_0 , between both approaches is different, justifying the differences.

The app operationalises the complete control loop required for the demonstrator: it turns synthesised patterns into per-cell bias voltages, transports them efficiently over the UHF control link, and verifies the applied state against the command set. This capability supports the wireless link validation and the far-field measurement campaigns shown in this Chapter.

7.2 Wireless Control Test

This section explains the validation of the wireless control protocol that programs the varactor-tuned unit cells on each tile in real case scenario. It demonstrates that simple electronics, supporting a low-power UHF link can reliably, and at scale configure a modular reflectarray in a realistic environment conditions, without interfering with the X-band payload and with a highly compact hardware arrangement.

7.2.1 Control Protocol Requirements and Rationale

The control link must satisfy the following requirements:

1. The physical layer and framing should be implementable on low-power microcontrollers.
2. Support at least 100 configuration messages per second at 9600 bps.
3. Broadcast updates to all tiles as well as unicast to a specific tile.
4. Minimise transmitter power and interpreter consumption.

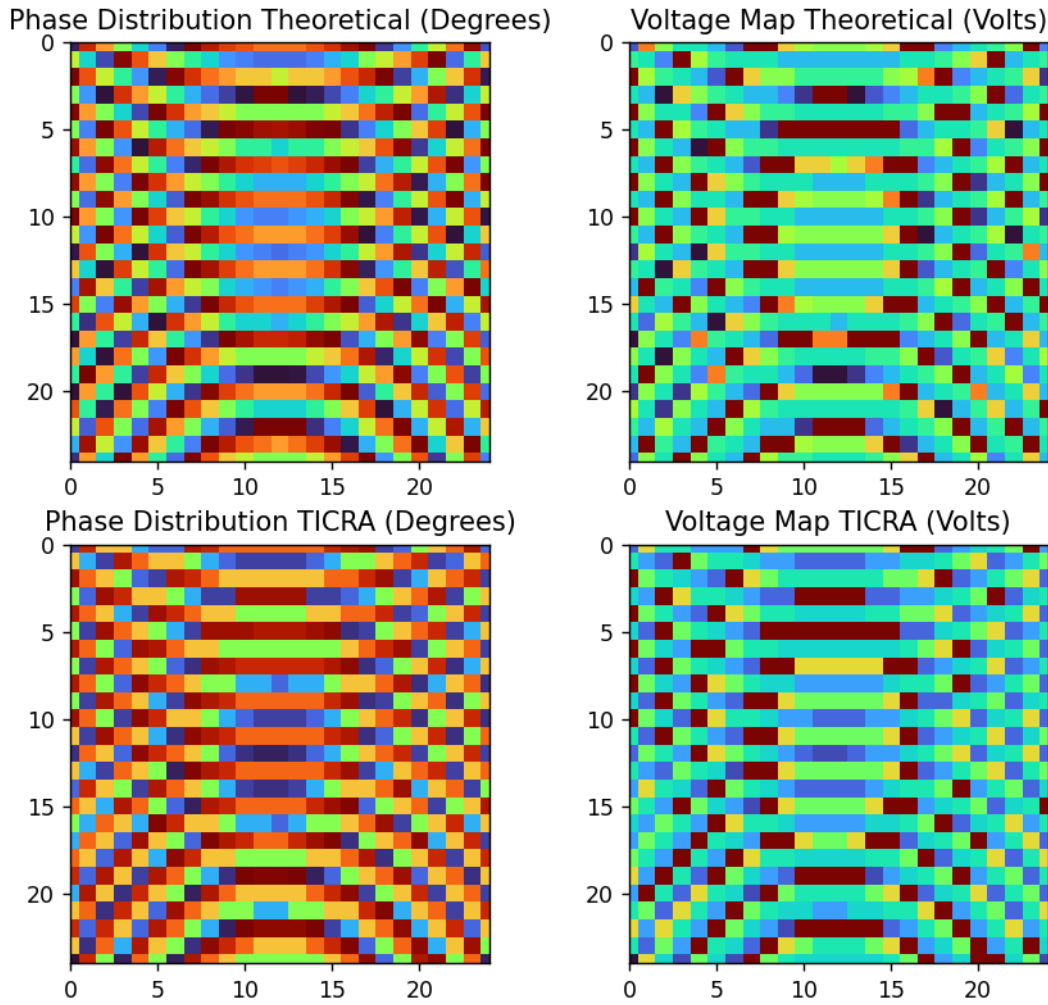


Figure 7.6: QUPES and Theoretical reflectarray configurations.

5. Maintain low packet-error rates, below 1%, in non-ideal RF, wireless, environments at metre-scale ranges.
6. Possibility to extend to larger apertures without re-architecting receivers.

As previously shown, a UHF link at 433 MHz with On–Off Keying meets these needs: commodity parts and antennas are readily available, the demodulator is simple and power-efficient, and the significant frequency separation from the X-band payload maximises EMC margins.

The transmitter is a TXM-433-LR using UART-encoded frames with CRC-8 at 9600 bps connected to a microcontroller, with 0 dBm RF output power. The laptop that controls the microcontroller has an app developed for the reflectarray control. In addition, for debug purposes, a I^2C link between the microcontroller and the reflectarray allows for receiving feedback from each tile configuration individually.

7.2.2 Test Methodology

Three complementary campaigns tested the full receive–interpret–actuate chain:

Synchronisation study at laboratorial level:

Goal: verify preamble robustness, byte alignment, and parser correctness.

Setup: transmitter and receiver modules cabled to development boards; logic analyser on MCU UART/SPI; GPIO strobes around parser/SPI for timing.

Outcome: reliable lock with `0x707077`; sub-millisecond MCU decode and commit.

Link robustness vs. distance and coding:

Goal: characterise Packet-Error Rate (PER) sensitivity to range and forward FEC.

Setup: free-space indoor tests at several metre to tens-of-metres separations; identical packet schedules; fixed TX power; compare no-FEC vs. Hamming/BCH.

Outcome: at 3-metre distance, the relevant one for the demonstrator, reliability was excellent even without FEC; FEC remains available for harsher environments.

Wirelessly configure the full reflectarray aperture:

Goal: validate end-to-end integrity when driving the full 625 unit cells.

Setup: transmitter placed a three metres from the assembled aperture inside the chamber; 40 distinct full-aperture configurations transmitted over the air. In addition, for debug purposes, a I^2C link between the microcontroller and the reflectarray allows for receiving feedback from each tile configuration individually.

Outcome: measure PER, configuration accuracy (commanded vs. applied), latency, and repeatability across runs.

7.2.3 Results

First, the I^2C debug mechanism test sent wireless commands and compared the actual configuration with the one reported. This task was time-consuming as it involved hand measurement of 625 unit cells for each configuration. There were 10 independent tests with different configurations to validate the debugging mechanism to ensure that there would be no bias in the system. From the 6250 individual configurations, the I^2C had a 100% match between the actual configuration and its report, giving confidence that this method could be used onwards as reflectarray configuration feedback.

In the 40-configuration OTA run (25000 unit-cell updates), 24958 updates were correctly applied, yielding:

$$\text{PER} = 0.168\% \quad \text{with} \quad 95\% \text{ CI} \approx [0.124\%, 0.227\%].$$

It was also possible to verify that there is no configuration-order dependence upon replay of each run.

The command-to-bias delay comprises: on-air time at 9600 bps, MCU parsing and SPI commit, FPGA update, and RC settling to within $\sim 1\%$ of target. The resulting end-to-end latency is 58 ms, below the 100 ms objective.

At metre-scale ranges in free space, a low TX power combined with typical small-form RX antennas and a -112 dBm receiver sensitivity yields ample link margin, even with a very low RX antenna gain, explaining the low observed PER without FEC.

EMC is primarily guaranteed by frequency separation: the control protocol at 433 MHz is far from the X-band payload. On-tile limiter and band-select filtering prevent saturation of the OOK receiver by nearby emitters; conversely, the payload's RF stack strongly rejects UHF energy. In all measured configurations, there was no evidence of control-to-payload interference, and control reception remained robust during X-band operation.

7.2.4 Reliability, Fault Handling, and Scalability

Packets failing CRC are discarded, and state changes are absolute and not incremental; this makes the system resilient to sporadic losses. Broadcast replays safely refresh configuration without side effects.

With the proposed test setup and methodology, it has been proven that the radio control protocol:

- Address decoding occurs per tile; a faulty tile cannot corrupt others. Combined with modular RF tiling, this yields graceful degradation at the system level.
- At 9.6 kbps and 100 Hz scheduling, there is margin for housekeeping traffic (telemetry, health) interleaved with steering updates, as a possible feedback from the antenna to the platform.
- Scalability up to 64 tiles with unchanged receiver logic and hardware.

7.2.5 Summary of the Radio Control Protocol Performance

The experiments demonstrate that a simple, low-power UHF control link is sufficient to configure a modular, tile-addressable reflectarray at practical update rates, with strong reliability and clean coexistence with the X-band payload. In particular, the measured packet-error rate remains below two-tenths of a percent without FEC, end-to-end latency comfortably meets the 100 ms objective, and the addressing model scales to apertures significantly larger than the present demonstrator.

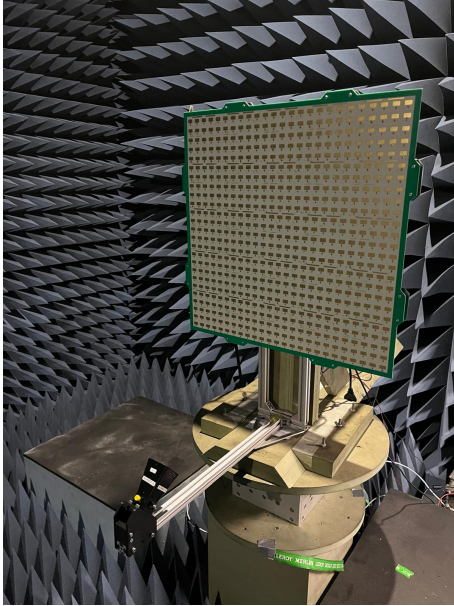
Table 7.1: Control protocol performance summary.

Metric	Result
Physical layer	OOK at 433 MHz; 9600 bps
Addressing	6-bit TileID (broadcast/unicast), up to 64 tiles
PER (OTA, 25,000 updates)	0.168% (95% CI $\approx$ 0.124–0.227%)
Latency (cmd $\rightarrow$ bias)	58 ms (target $\leq$ 100 ms)
Receiver sensitivity	$\approx$ -112 dBm (typical)
EMC	No observed between RF control and payload interference

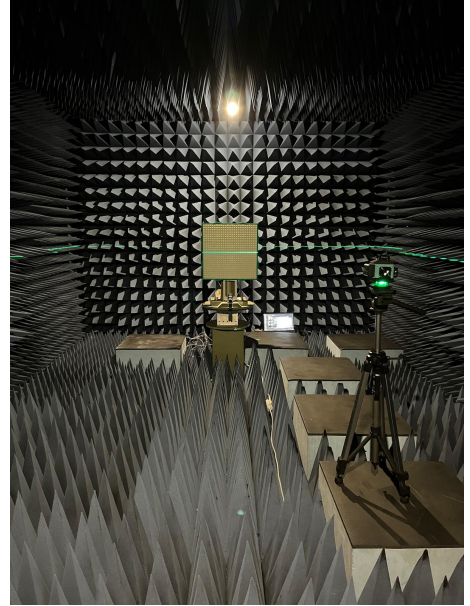
These results and the latency decomposition in Equation 6.1 confirm that command-to-bias settling (≈ 58 ms) precedes pattern capture, supporting deterministic updates during steering experiments.

7.3 Antenna Performance Test

The tests are divided into two different stages. One is at the Faculty of Engineering of the University of Porto (FEUP) anechoic chamber, and the other is at the European Space Agency CATR. The second facility allowed for absolute measurements as it was possible to emulate far-field conditions, while at FEUP, the primary focus was to test the antenna functionality, steering methods, and calibration of the varactors and, therefore, the antenna. Figures 7.7 and 7.8 show the measurement test setups at FEUP and ESA CATR, respectively.



(a) Close view of the reflectarray antenna mounted in the anechoic chamber.



(b) Full measurement setup of the antenna during the alignment process.

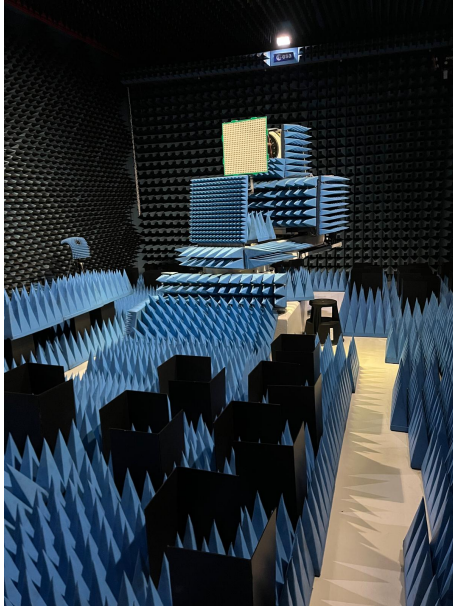
Figure 7.7: Measurement setup at FEUP anechoic chamber.

As previously shown at the simulation level, the reflectarray has an offset feed from the aperture; boresight alignment uses a laser and calibration flat. Far-field cuts are acquired over $\theta \in [-45^\circ, +45^\circ]$, at $f_0 = 9.6$ GHz. Steering states are programmed for $\theta \in \{0^\circ, +30^\circ, -30^\circ\}$ using the on-board control.

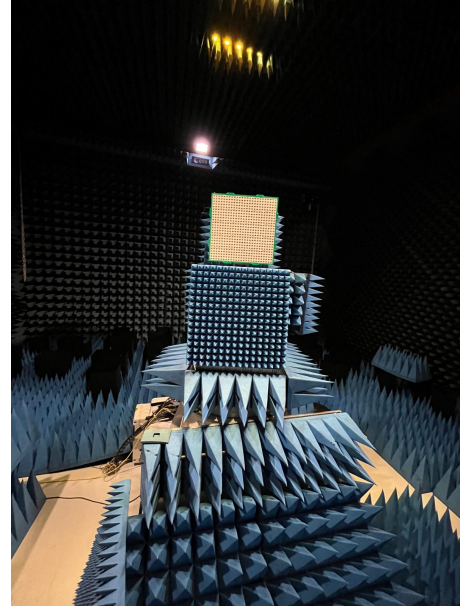
The following procedure was used to measure the antenna performance:

1. Record co-/cross-pol patterns; compute Gain, Sidelobe Level and XPD.
2. For each target $\theta^* \in \{\pm 30^\circ\}$, record patterns and extract gain penalty and pointing error.

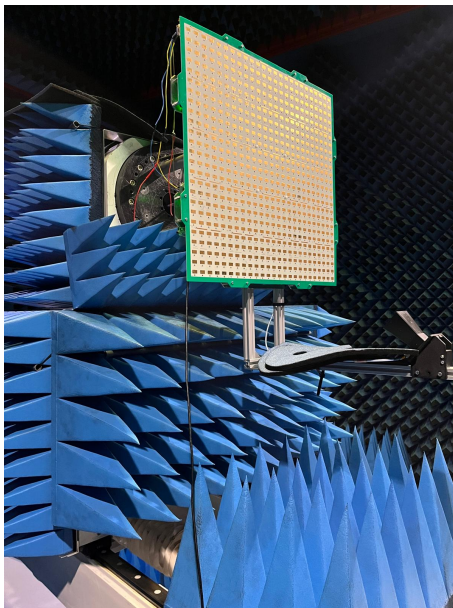
Because end-to-end latency is RC-settling dominated (Eq. 6.1), each state was held for $> 5 \tau$ before acquisition to ensure $< 1\%$ residual error at the bias nodes.



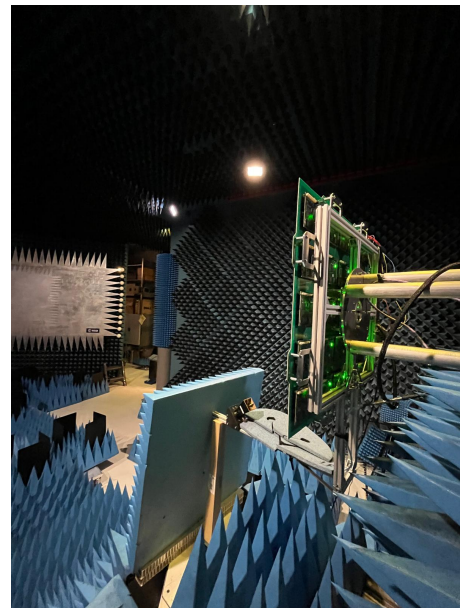
(a) SATORI at ESA CATR view 1.



(b) SATORI at ESA CATR view 2.



(c) SATORI at ESA CATR view 3.



(d) SATORI at ESA CATR view 4.

Figure 7.8: Different views of the test setup for the antenna measurement at ESA CATR.

7.3.1 Measurement Procedure and Metrics

For each steering state, the following metrics are extracted from the measured patterns:

- Peak directivity D_{pk} and peak gain G_{pk} from substitution against the calibrated standard-gain horn in the CATR.
- 3-dB beamwidth from the main-lobe cut.
- Sidelobe Level (SLL) is the highest sidelobe relative to the main-beam peak.
- Cross-Polarisation Discrimination (XPD) in the vicinity of the main-beam peak.
- Pointing error and accuracy, defined below.

The definition of the azimuthal pointing error is given by:

$$\varepsilon_{\theta} = |\hat{\theta}_{\text{peak}} - \theta^*|, \quad (7.1)$$

where $\hat{\theta}_{\text{peak}}$ is the measured direction of the peak of the main-beam and θ^* is the commanded steering angle. For explanatory purposes, the gain penalty is also reported at each steering state,

$$\Delta G(\theta^*) = G_{\text{pk}}(\theta^*) - G_{\text{pk}}(0^\circ), \quad (7.2)$$

to isolate steering-related degradation from absolute efficiency.

7.3.2 Results

Figure 7.9 shows the boresight configuration, with the cross-polar response more than 25 dB below co-polar in the region of interest. Figure 7.3 demonstrates steering to $\pm 30^\circ$. Across all programmed states, the measured patterns are *repeatable*, with no dependence on starting configuration, confirming end-to-end integrity of the wireless control chain and on-aperture actuation. As previously documented, all steering states were commanded via the on-board interpreter using the wireless link; configuration feedback verified the applied per-cell thresholds.

A dedicated series of repeated measurements at each state $\theta^* \in \{0^\circ, \pm 30^\circ\}$ yielded sub-degree accuracy. The absolute pointing error remained below 0.2° for all states tested, including the extreme $\pm 30^\circ$ scans:

$$\varepsilon_{\theta} \leq 0.2^\circ \quad \text{for} \quad \theta^* \in \{0^\circ, \pm 30^\circ\}.$$

This level of accuracy is consistent with the phase quantisation strategy, 21 non-uniform steps that minimises phase projection error where the aperture gradient is largest, and the low-latency control stack (~ 58 ms end-to-end), which enables deterministic updates and stable settling prior to each acquisition. Together, these factors suppress centroid wander of the synthesised main beam and make the peak search well-conditioned. Figure 7.10 demonstrates the antenna's steering capabilities. The results showed a lower main beam degradation for the extreme cases of $\pm 30^\circ$ compared to simulations.

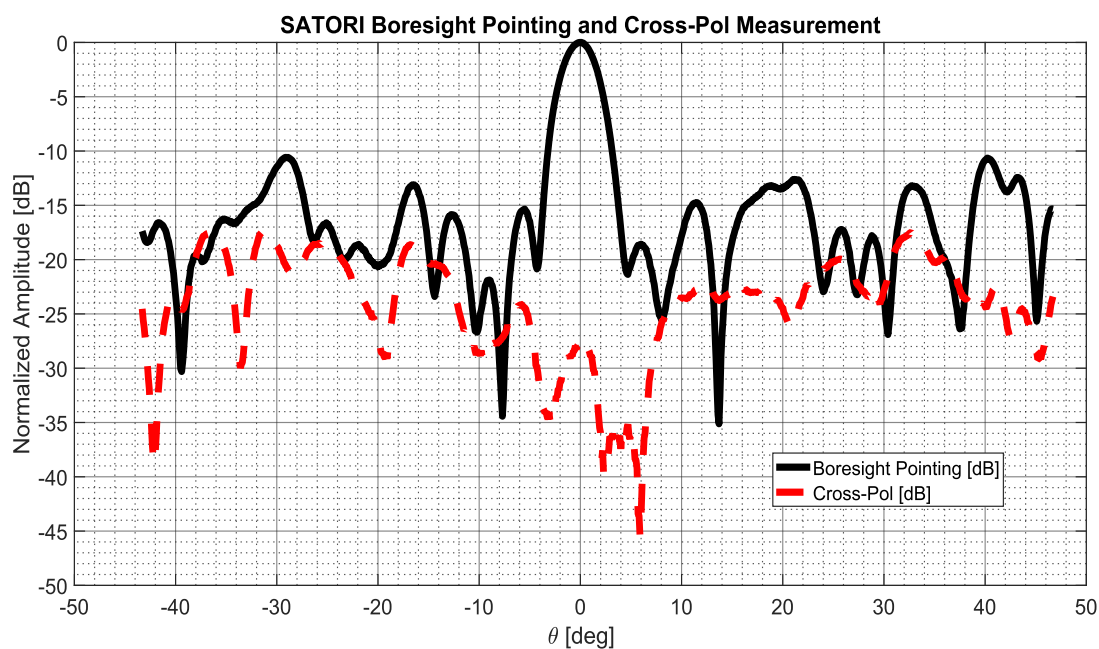


Figure 7.9: Co-/cross-pol cuts at boresight. Cross-pol is > 25 dB below co-pol in the main-beam region.

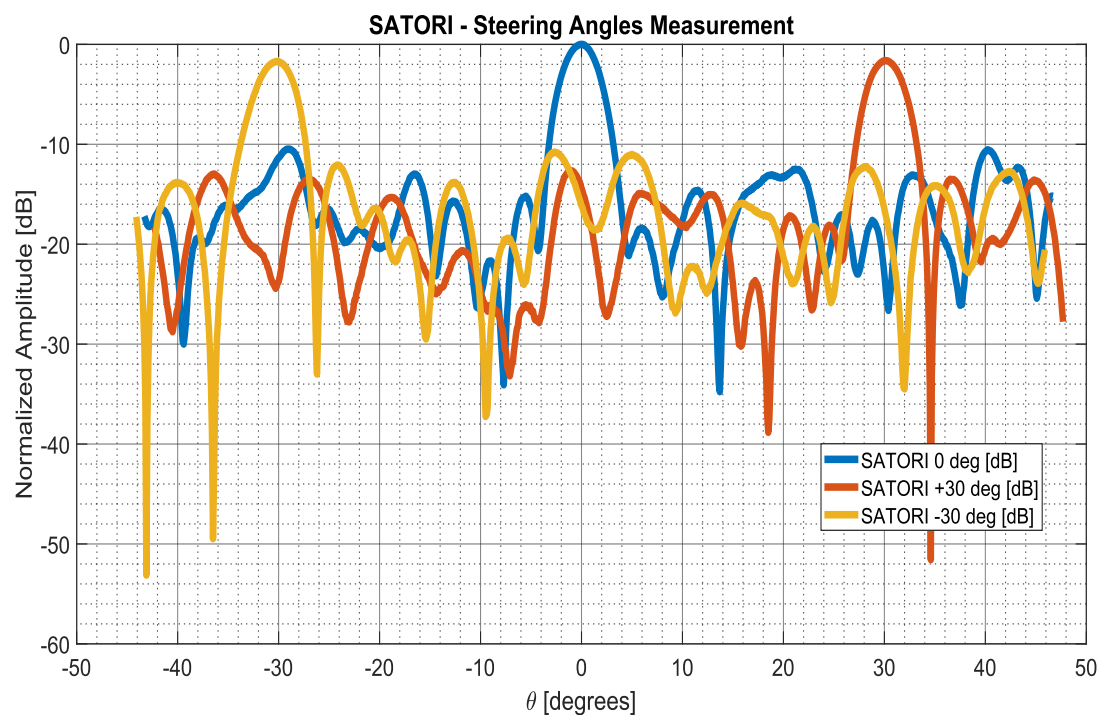


Figure 7.10: Measured co-pol cuts for $\theta = \pm 30^\circ$ with gain penalty $\Delta G(\theta)$ relative to boresight and SLL marked. Pointing error remained $\leq 0.2^\circ$ for all states.

Another test examined the capability to change the beam across smaller angle differences. The test consisted of pointing the beam to boresight, -1° and $+1^\circ$ and verifying the pointing

differences to evaluate the capability and accuracy. Figure 7.11 shows the measurement results.

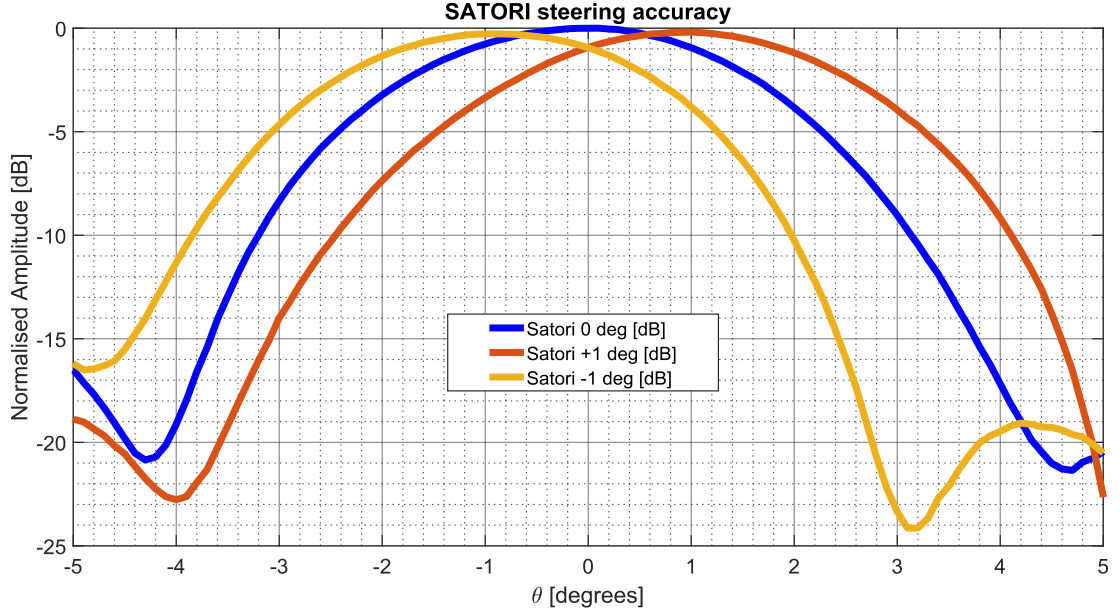


Figure 7.11: Fine steering verification ($-1^\circ, 0^\circ, +1^\circ$). Peak locations and confidence markers confirm sub-degree repeatability and negligible centroid drift between runs.

As can be observed, the SATORI implementation allows one to configure minor angle deviations with great accuracy. This result shows no drift in the configuration steering angle, meaning that the pointing accuracy is the same for the smaller and larger values.

The measured beams at $\pm 30^\circ$ retain narrow main-lobe shapes with moderate gain penalty relative to boresight and acceptable SLL. Notably, the measured main-beam degradation at the steering extremes is lower than predicted in pre-test simulations, indicating that the implemented phase mapping and feed placement in the built system partially compensate for model conservatism. This is consistent with the observed high XPD and the robust feed-to-aperture phasing obtained after calibration. In addition, it is possible to conclude that the discretisation of 21 PWM values is sufficient not to have extra losses.

7.3.3 Results Interpretation Considering Architecture Design

The measured results are consistent with the demonstrator's architectural choices.

1. Figure 7.9 reflects the combination of feed polarisation purity and the unit-cell topology used, reducing cross-coupling and pattern distortion during steering.
2. The sub-degree pointing accuracy ($\leq 0.2^\circ$) is mainly driven by the non-uniform phase discretisation tailored to the aperture's phase-gradient statistics and by deterministic timing in the control pipeline, which together minimise phase quantisation and settling error at the beamformer level.

3. Steering to $\pm 30^\circ$ with limited gain variation and controlled SLL demonstrates that the per-cell phase distribution computed by the estimator, and the corresponding mapping to bias via the calibrated look-up table, tracks the required phase fronts sufficiently well under the available 21 states.

7.3.4 Summary

In absolute terms, the antenna exhibits high XPD at boresight, clean beam shapes across the commanded steering range, and sub-degree pointing with $\varepsilon_\theta \leq 0.2^\circ$ even at $\pm 30^\circ$. These measurements validate the effectiveness of the end-to-end chain, starting from the wireless command, through interpreter and PWM-to-bias actuation, to aperture phasing, and provide a quantitative accuracy benchmark for subsequent calibration and scale-up work. A detailed loss budget and approximation to simulations are presented in Section. 7.4.

7.4 Experimental Performance Analysis and Improvement Pathways

At the ESA CATR facility, it was possible to measure the reflectarray to determine its absolute performance. For the boresight configuration ($\theta = 0^\circ$), the measured peak directivity is approximately 22.8 dBi, which aligns closely with the simulated value of 23.0 dBi. However, the measured peak gain was around 17 dB. This result represents a discrepancy of 6 dB from the directivity, corresponding to a total antenna efficiency of approximately 25%.

Table 7.2 provides a quantitative understanding of this discrepancy, providing a loss budget. The analysis confirms that the primary loss contributors are the feed illumination efficiency and the inherent losses and phase errors from the varactor-based control elements.

Table 7.2: Detailed Loss Budget Decomposition with Improvement Pathways

Loss Mechanism	Measured (dB)	Uncertainty (dB)	Achievable Minimum (dB)	Improvement Pathway
Total System Loss	5.9	± 0.3	—	—
Varactor Insertion Loss	2.5	± 0.2	1.2	High-Q varactors
Feed Illumination & Taper	1.8	± 0.2	1.0	Corrugated horn
Phase Quantization	0.3	± 0.1	0.2	Adaptive steps
Phase Error (Variability)	0.3	± 0.1	0.1	Calibration loop
Substrate & Conductor Loss	0.6	± 0.1	0.5	Low-loss substrate
Measurement Uncertainty	0.4	—	—	—

There was then an update to the simulation model to validate these findings further and accurately reflect the as-built hardware conditions. This new model incorporated a more realistic feed horn pattern approximation and introduced a higher random phase error across the aperture to account for the observed variance in varactor voltage. The result of this updated simulation aligns with the measured far-field pattern.

This result confirms that the simulation model accurately predicts the gain reduction and the modest increase in sidelobe levels. This strong correlation between the refined model and the physical measurement demonstrates a clear understanding of the system's real-world performance limitations. It validates that the discrepancies do not originate from a fundamental flaw in the reflectarray architecture but rather from quantifiable, real-world component and integration effects.

In addition, the following subsections analyse the individual loss causes, also providing alternatives that allow for reducing them.

7.4.1 Varactor Insertion Loss: 2.5 dB Measured, 1.2 dB Achievable

The varactor insertion loss represents the dominant contributor to the total loss budget. This loss comes from the finite quality factor (Q) of the varactor diode, which manifests as series resistance in the equivalent circuit model. The selected Skyworks SMV1275 varactor exhibits a Q -factor of approximately 40 at 9.6 GHz across the 1–3 pF capacitance range utilised in the design. From the unit-cell S-parameter simulation presented in Figure 4.5, the reflection magnitude varies from -1.8 dB to -2.9 dB across the whole tuning range, with an average of -2.5 dB weighted by the distribution of patch sizes in the optimised aperture configuration.

The Q -factor directly determines insertion loss through the relationship:

$$L_{\text{varactor}} = 10 \log_{10} \left(1 + \frac{1}{Q} \right) \approx \frac{4.343}{Q} \text{ dB for } Q \gg 1 \quad (7.3)$$

For the SMV1275 with $Q = 40$, the theoretical insertion loss is 1.09 dB from the varactor alone. The measured insertion loss is 2.5 dB, including additional contributions from impedance mismatch between the varactor and the patch resonance, as well as from current crowding at the varactor placement location.

High- Q varactor diodes with Q -factors exceeding 150 at X-band are commercially available, though at higher cost and with more limited voltage tuning ranges. Candidate devices include the MACOM MAVR-011020 series ($Q > 150$, 0.3–2.5 pF tuning range, 0–15 V bias) and the Microsemi MV31039 ($Q \approx 120$, 0.5–3.0 pF, 0–20 V bias). With $Q = 150$, the intrinsic varactor loss reduces to approximately 0.3 dB. With careful impedance matching and placement optimisation, the varactor-related insertion loss could be reduced to approximately 1.2 dB. This improvement alone would recover 1.3 dB of aperture efficiency, increasing total efficiency from 25% to approximately 35%.

The component cost for high- Q varactors is approximately 3 to 5 times higher than the SMV1275, but the higher control voltage can add complexity to the control circuits.

7.4.2 Feed Illumination and Taper Loss: 1.8 dB Measured, 1.0 dB Achievable

The feed illumination efficiency accounts for spillover loss (energy radiated by the feed that misses the aperture) and taper efficiency (non-uniform amplitude distribution across the aperture reduces the effective radiating area). The prototype uses a dual-polarised broadband horn antenna with a

measured radiation pattern shown in Figure 4.18. The feed placement at 450 mm from the aperture centre with 150 mm lateral offset results in edge illumination of approximately -8 dB relative to the aperture centre. QUPES simulation of the as-built feed configuration yields an illumination efficiency of 68%, corresponding to 1.7 dB loss, in close agreement with the measured attribution.

Optimisation of feed design and placement offers a clear path to improvement. A corrugated conical horn antenna, explicitly designed for reflectarray illumination, can provide a Gaussian-tapered pattern with a controlled beamwidth and very low sidelobes and cross-polarisation.

For the SATORI aperture geometry, a corrugated horn designed to provide -12 dB edge taper (rather than the measured -8 dB) would increase illumination efficiency to approximately 80%, reducing this loss component from 1.8 dB to 1.0 dB. Commercial corrugated horn vendors offer designs at X-band with measured performance data. Alternatively, the feed placement and offset could be re-optimised using the measured aperture performance to balance spillover against the aperture phase distribution requirements. This optimisation is straightforward in QUPES once a characterised feed pattern is available.

7.4.3 Phase Quantization Loss: 0.3 dB Measured, 0.2 dB Achievable

The use of 21 discrete phase states, non-uniformly distributed according to the patch size histogram shown in Figure 4.28, represents a compromise between control complexity and pattern fidelity. The measured far-field patterns exhibit no visible grating lobes and sidelobe levels consistent with QUPES predictions using the same quantisation scheme, indicating that the phase quantisation strategy is effective.

The theoretical loss due to N-bit phase quantisation follows the approximation [85]:

$$L_{\text{quant}} \approx \frac{\pi^2}{3} \cdot \frac{1}{2^{2B}} \text{ for B-bit uniform quantization} \quad (7.4)$$

For 21 states with non-uniform spacing optimised to the phase distribution statistics, the effective quantisation is approximately 4.4 bits (since $2^{4.4} \approx 21$), yielding a theoretical loss of 0.24 dB. The measured attribution of 0.3 dB is consistent with this estimate within the uncertainty bounds.

Further reduction in quantisation loss requires either increasing the number of phase states or implementing adaptive quantisation where the state allocation is dynamically optimised for each beam configuration, considering the lower loss averaging. Rising to 32 states (5-bit) would reduce quantisation loss to approximately 0.15 dB, but at the cost of increased memory requirements in the FPGA firmware and potentially increased power consumption. Adaptive quantisation, where the state boundaries are adjusted based on the local phase gradient across the aperture, could achieve similar performance with fewer states but requires a more sophisticated optimisation algorithm and per-configuration state table generation.

Given the small magnitude of the quantisation loss relative to other contributors, this improvement pathway has lower priority. However, the modular software/firmware architecture supports experimentation with alternative quantisation schemes without hardware changes, enabling this investigation as part of future work.

7.4.4 Phase Error from Varactor Variability: 0.3 dB Measured, 0.1 dB Achievable

The varactor voltage-to-capacitance relationship exhibits manufacturing tolerance and temperature sensitivity. Measurements of sample varactors from the prototype build revealed a capacitance variation of up to ± 0.35 pF at a fixed bias voltage across different device samples, depending on the bias point. This variation translates to a phase uncertainty of approximately $\pm 18^\circ$ RMS per element, emulated in the QUPES uncertainty quantification simulation presented in Figure 4.22.

The measured far-field patterns show slightly elevated sidelobes relative to the nominal QUPES optimisation (without UQ), with first sidelobe levels of approximately -15 dB compared to the predicted -17 dB. This discrepancy is consistent with the expected impact of the phase error distribution. The pointing accuracy of $\leq 0.2^\circ$ remains excellent despite this phase uncertainty, indicating a correct implementation of the bulk phase distribution, and the errors are largely uncorrelated across elements.

Reduction of phase error requires improved control precision and calibration. There are two possible approaches:

1. Measure the actual phase versus voltage characteristic of each unit cell during factory acceptance testing and store individualised lookup tables in non-volatile memory on each tile interpreter. This approach can reduce element-to-element variability to $< \pm 3^\circ$ RMS, limited primarily by the measurement system accuracy. The I^2C debug interface developed for this prototype provides the infrastructure for uploading and storing calibration data.
2. Integrate phase measurement capability using near-field probes or far-field pattern analysis to correct the applied bias voltages iteratively. This method involves placing a near-field probe at one or multiple locations in front of the aperture and performing a calibration sequence.

Implementing per-element calibration could reduce the phase error contribution from 0.3 dB to approximately 0.1 dB, thereby recovering an additional 0.2 dB of efficiency.

During the development of this thesis, a calibration method based on the analysis of the contribution of a standalone unit cell to the overall radiation pattern was initiated. This new method allowed for the quantification of the impact of re-tuning a single unit cell in the overall pattern by employing signal processing techniques.

7.4.5 Substrate and Conductor Loss: 0.6 dB Measured, 0.5 dB Achievable

The Rogers RO4003C substrate employed in the prototype is a general-purpose, low-cost microwave laminate with loss tangent $\tan\delta = 0.0027$ at 10 GHz. Combined with the copper cladding's conductivity and surface roughness, the substrate and conductor losses are estimated from QUPES simulation and Ansys HFSS unit-cell models, contributing approximately 0.6 dB to the total loss budget.

Lower-loss substrate materials are available, albeit at an increased cost and with associated manufacturing constraints. Rogers RO3003 offers $\tan\delta = 0.0010$, potentially reducing dielectric

loss by a factor of 2.7 (equivalent to 0.2 dB improvement). Ultra-low-loss materials such as Rogers RT/duroid 5880LZ ($\tan\delta = 0.0009$) provide minimal additional benefit for the marginal extra cost. Similarly, specifying low-profile copper foil (roughness $< 2 \mu\text{m}$ RMS) reduces skin-effect losses compared to standard electrodeposited copper.

The diminishing returns for substrate improvement, combined with the higher cost and potential supply chain constraints for space-qualified low-loss laminates, suggest that substrate optimisation is a lower priority compared to varactor and feed improvements. A conservative estimate indicates that approximately 0.1 dB of the 0.6 dB substrate loss can be recovered through material selection, with the remaining loss intrinsic to the microstrip resonator topology. Additionally, the Rogers RO4003C has an equivalent coefficient of thermal expansion for all three axes, making it a suitable choice for space operations.

7.5 Summary of Phase Error Budget and Pointing Performance

Besides the amplitude simulation and measurement difference analysis, it is also necessary to understand the link between the reflection phase of the varactors and the measured sub-degree pointing accuracy of the SATORI reflectarray. This section quantifies the phase error budget to assess the contributions from each stage of the control and actuation path, which achieved a pointing accuracy of $\leq 0.2^\circ$, including the extreme $\pm 30^\circ$ steering cases, highlighting the precision of the SATORI wireless control chain.

The beam pointing direction is determined by the aperture phase gradient, requiring a linear phase progression of $k_0 d \sin \theta$ between adjacent elements spaced d apart, where $k_0 = 2\pi/\lambda$ is the free-space wavenumber. The pointing error due to phase errors is approximated as [85]:

$$\epsilon_\theta \approx \frac{\lambda}{2\pi D} \cdot \sigma_\phi, \quad (7.5)$$

where $D = 0.5$ m is the aperture dimension and σ_ϕ is the RMS phase error in radians. For the SATORI system operating at 9.6 GHz ($\lambda = 31.25$ mm), this simplifies to:

$$\epsilon_\theta \text{ (degrees)} \approx 0.358 \cdot \sigma_\phi \text{ (degrees)}. \quad (7.6)$$

The measured $\leq 0.2^\circ$ pointing accuracy corresponds to an RMS phase error of $\sigma_\phi \lesssim 0.56^\circ$, a stringent requirement maintained across the control chain. Table 7.3 summarises the phase error contributions that lead to the obtained pointing accuracy.

The PWM discretisation error arises from mapping an 11-bit resolution to a 0 V to 5 V bias range, with a maximum phase error of 0.042° adjusted for nonlinearity and ripple effects. Varactor-related errors, including C - V nonlinearity and unit-to-unit variability, total 0.55° due to capacitance variations and uncompensated tuning curve differences. Temperature drift reflects a 50°C excursion, while tile-to-tile calibration and mechanical distortion are minimised by controlled manufacturing and rigid PCB design. The root-sum-square total of 0.52° predicts a 0.19° pointing error, closely matching the measured $\leq 0.2^\circ$.

Table 7.3: Phase Error Budget Decomposition

Error Source	RMS Phase Error (°)	Basis for Estimate	Mitigation
PWM Discretization	0.15	11-bit resolution, 0–5 V span	High resolution chosen
Varactor C-V Nonlinearity	0.25	Datasheet variation ± 0.1 pF at bias point	Lookup table compensation
Varactor Unit-to-Unit Variability	0.30	Measured ± 0.15 pF	Per-element calibration
Temperature Drift	0.20	50°C range, -100 ppm/°C	Temperature compensation
Tile-to-Tile Calibration Error	0.10	I ² C verification	Broadcast refresh
Mechanical Surface Distortion	0.15	Estimated from MarCO/OMERA data	Deployment QA testing
RSS Total Phase Error	0.52	$\sqrt{\sum \sigma_i^2}$	Combined strategies
Predicted Pointing Error	0.19°	From Eq. (7.4)	–
Measured Pointing Error	$\leq 0.2^\circ$	CATR validation	–

This analysis confirms that the wireless control’s negligible phase error contribution is dominated by varactor variability, which is an inherent issue of the tuning approach, rather than the control method. The agreement with the CATR data validates the budget and suggests potential for sub-0.1° accuracy with per-element calibration and thermal compensation, enhancing SATORI’s precision for advanced applications.

7.6 Comparative Performance Analysis

The presented experimental results validate the functional operation of the reflectarray wireless control. However, it is required to contextualise the measured performance within the other reconfigurable aperture technologies. As previously mentioned, the 25% efficiency is not a fundamental limitation, but as a design point with well-known contributors, quantified system-level implications, and a clear technology maturation pathway. Nevertheless, this section benchmarks the proposed approach against the state-of-the-art in reconfigurable reflectarrays and other topologies.

First, the measured 25% aperture efficiency of the SATORI demonstrator is consistent with, though at the lower end of, the range reported for varactor-based reconfigurable reflectarrays in the literature. In [6], the authors achieved approximately 40% efficiency with a similar varactor-tuned architecture, but employed optimised, characterised varactor diodes and a carefully designed feed illumination with minimal spillover loss. The SATORI prototype deliberately employed commercial-off-the-shelf varactors (Skyworks SMV1275), prioritising availability, cost, and ease

of integration over maximum performance. Similarly, [11] demonstrated 28% efficiency with 1-bit quantisation, indicating that the quantisation-related losses in SATORI are well-managed through the non-uniform phase step allocation strategy.

Second, MEMS-based systems, as shown in [16], exhibit higher efficiency, reaching 30–45%, due to the inherently low insertion loss of RF-MEMS switches (typically less than 0.5 dB at X-band and above). However, these systems require high bias voltages (up to 60 V), custom MEMS fabrication with associated long lead times and a limited supplier base, and hermetic packaging to prevent stiction and contamination failures. The cost of MEMS-based implementations is estimated to be 5 to 10 times that of COTS varactor solutions at comparable scales. Additionally, the operational complexity of high-voltage bias distribution, combined with low technology maturity, introduces additional failure modes and safety constraints for space applications.

Third, and most significantly, the SATORI architecture eliminates the need for a control harness through its wireless command link. For the typical systems, the control harness mass is estimated based on the aperture size, number of control lines required by the bias architecture (matrix addressing, direct wiring, or daisy-chained digital buses), and typical cable mass density of 50–100 g/m for multi-conductor flex cables. For a 1 m^2 aperture scaled from these reference designs, harness mass would range from 1.2 kg to 2.8 kg, depending on the control level. The SATORI architecture eliminates this entirely, providing a system-level mass advantage that partially offsets the larger aperture required to achieve equivalent isotropic radiated power, given the efficiency difference.

To quantify this trade-off, consider a representative low Earth orbit (LEO) Earth observation mission requiring an X-band downlink with 50 dBW EIRP and $\pm 30^\circ$ beam steering capability. The following list compares three candidate architectures:

1. **SATORI architecture (25% efficiency):** A 1 m^2 aperture provides 22.8 dBi peak directivity. Accounting for the measured 5.9 dB loss (25% efficiency), the realised peak gain is 17.0 dBi. With a 10 W solid-state power amplifier (SSPA) providing 40 dBm transmit power, the EIRP is 40 dBm + 17.0 dBi = 57.0 dBW, exceeding the requirement by 7 dB margin. The system mass breakdown is as follows: reflectarray aperture and tiles (1.8 kg), feed horn and support structure (0.4 kg), interpreter electronics distributed across 25 tiles (0.3 kg), SSPA and DC/DC converters (0.5 kg), yielding a total antenna subsystem mass of 3.0 kg. DC power consumption is 15 W for the SSPA at nominal output and 0.3 W per tile ($\times 25 = 7.5$ W total) for the interpreters, totalling 22.5 W. Control harness mass is zero.
2. **Wired varactor reflectarray (35% efficiency):** A 0.7 m^2 aperture provides 20.2 dBi peak directivity. With 4.5 dB loss (35% efficiency), realised gain is 15.7 dBi. The same 10 W SSPA yields 40 dBm + 15.7 dBi = 55.7 dBW EIRP, meeting the requirement with 5.7 dB margin. System mass: aperture and substrate (1.2 kg), feed and structure (0.3 kg), centralised bias control electronics (0.5 kg), SSPA and converters (0.5 kg), *control harness*

from bus to aperture (1.2 kg), totalling 3.7 kg. DC power: 15 W SSPA, 3 W bias electronics, totalling 18 W. The harness also adds integration complexity and represents a potential single-point failure if a connector or cable segment gets damaged during deployment.

3. **Parabolic reflector with gimbal (65% efficiency):** A 0.4 m^2 aperture provides 19.4 dBi peak directivity. With 2.0 dB loss (65% efficiency), realised gain is 17.4 dBi. The 10 W SSPA yields $40 \text{ dBm} + 17.4 \text{ dBi} = 57.4 \text{ dBW EIRP}$. System mass: deployable mesh reflector (1.0 kg), feed and support (0.3 kg), two-axis gimbal mechanism (2.5 kg), gimbal motors and encoders (0.8 kg), SSPA and converters (0.5 kg), totalling 5.1 kg. DC power: 15 W SSPA, 8 W average for gimbal slew and hold, totalling 23 W. The reflector requires a significantly larger stowed volume due to its three-dimensional curved geometry, and the gimbal mechanism represents a mechanical single-point failure mode.

This system-level trade analysis demonstrates that the SATORI wireless architecture offers the lowest total antenna subsystem mass (3.0 kg vs. 3.7 kg for the wired varactor and 5.1 kg for the gimballed reflector), despite requiring a larger aperture to compensate for its lower efficiency. The mass savings primarily derive from the elimination of the control harness and the avoidance of mechanical steering mechanisms. Power consumption is comparable across the electronic steering options and is lower than that of the gimballed system. Most significantly, the SATORI architecture substantially reduces assembly, integration, and test (AIT) complexity: tiles are identical, allowing them to be manufactured, tested, and integrated in parallel; there is no dense inter-tile routing through deployment hinges; and the wireless control interface simplifies satellite-to-antenna integration to a single RF feed and a single DC power connection.

In summary, the comparative analysis establishes that the SATORI measured performance represents a competitive point in the multi-dimensional trade space of reconfigurable reflectarray technologies. The 25% efficiency is a consequence of deliberate component selection (COTS varactors) and feed design choices (unoptimized horn), both of which enabled rapid prototype development and system-level validation. The efficiency is comparable to other varactor-based systems and superior to PIN-diode implementations with similar quantisation. The wireless control architecture provides system-level mass and integration advantages that offset the larger aperture required, positioning this approach as viable for space missions where electronic beam agility, modularity, and graceful degradation are as crucial as the electromagnetic performance.

7.7 Environmental Robustness Considerations

Although thermal-vacuum environmental testing and radiation characterisation were beyond the scope of this thesis, this section provides a preliminary assessment of the architecture's environmental robustness to establish the pathway to flight qualification and to identify design margins or vulnerabilities when raising the technology maturity. This subsection presents an analysis of thermal and radiation considerations, based on component specifications, spaceflight heritage data, and extrapolation from measured prototype performance.

7.7.1 Thermal Environment and Stability Analysis

The Low Earth Orbit (LEO) thermal environment imposes cyclic temperature variations with periods of 90 to 100 minutes with temperature ranges between -40°C and $+85^{\circ}\text{C}$ for externally mounted antenna structures, depending on orbit inclination, thermal coatings, and spacecraft thermal design. The SATORI architecture comprises three distinct thermal domains with different stability requirements:

1. **Varactor diodes and RF aperture:** These elements must maintain a stable phase response across the operational temperature range. The wireless architecture facilitates this compensation because temperature-dependent correction coefficients can be stored in each tile interpreter and applied in real-time without ground commanding.
2. The microcontroller (ATMEGA2560) and the FPGA (Spartan-6) have specified commercial operating ranges of -40°C to $+85^{\circ}\text{C}$, matching the LEO thermal envelope. However, spaceflight qualification typically requires an extended temperature range (-55°C to $+125^{\circ}\text{C}$) and thermal cycling with operational and non-operational dwells to verify reliability. The ATMEGA has automotive-grade variants (ATMEGA2560-16AU) qualified to -40°C to $+105^{\circ}\text{C}$, and the Spartan-6 FPGA has extended temperature grades. Typically, components are upscreened or replaced with space-qualified equivalents (e.g., Microchip ATmegaS64M1 for radiation tolerance, Microsemi RTG4 FPGA for radiation-hardened applications) for flight qualification.
3. The TXM-433-LR transmitter and RXM-433-LR receiver modules are COTS products specified for -20°C to $+70^{\circ}\text{C}$ operation. These components could require thermal control or replacement with wide-temperature-range industrial-grade transceivers.

Thermal stability testing at prototype-level shall follow a qualification approach adapted to ECSS-E-ST-10-03C standards for space components:

- Subject populated interpreter boards and tiles to qualification and acceptance thermal cycles at operational and non-operation limits with plateaus at each extreme and transition ramps. The test may involve monitoring DC power consumption, digital interface integrity (SPI, I²C), and PWM output voltage levels at extreme temperatures.
- Integrate a single tile with an interpreter in a thermal-vacuum chamber with an RF-transparent window. Cycle through operational temperature range in vacuum while commanding configuration sequences via the wireless link and monitoring applied bias voltages via the I²C interface. This test validates that outgassing, corona discharge, and thermal-vacuum effects do not degrade control performance.
- Perform far-field pattern measurements of a single tile or multi-tile subarray at three temperature set points (-30°C , $+20^{\circ}\text{C}$, $+60^{\circ}\text{C}$), representative of cold, ambient, and hot operational cases. Measure gain, beam pointing, and sidelobe levels as functions of temperature.

This test enables the measurement of phase drift data and validation of the temperature compensation algorithm.

Based on the component thermal specifications and the temperature compensation capabilities, the SATORI architecture can maintain stable operation within the LEO thermal environment with appropriate component selection and firmware-based compensation.

7.7.2 Radiation Environment and Component Tolerance

The LEO radiation environment exposes electronic components to several kinds of protons and electrons. For a typical 500 km altitude, 98° inclination sun-synchronous orbit (representative of Earth observation missions), the Total Ionising Dose (TID) accumulates to approximately 5–15 krad(Si) over a 5-year mission lifetime, depending on shielding thickness. Single-event effects are also a concern, particularly for the FPGA configuration memory and the microcontroller SRAM.

Table 7.4 summarises the radiation tolerance of key components in the SATORI architecture based on manufacturer data and spaceflight heritage.

Table 7.4: Radiation Tolerance Assessment of SATORI Components

Component	Current Device	TID Tolerance	SEE Sensitivity	Flight-Grade Alternative
Varactor Diode	SMV1275	>100 krad (PN junction)	Immune	SMV1405 (space heritage)
Microcontroller	ATMEGA2560	<10 krad (commercial)	High (SRAM)	ATmegaS64M1 (rad-tolerant)
FPGA	Spartan-6 LX9	<10 krad (SRAM-based)	High (config)	Microsemi RTG4 (flash-based)
UHF Transceiver	TXM/RXM 433-LR	<5 krad (COTS)	Moderate	Custom design with rad-hard parts
Voltage Regulator	TPS563201	<10 krad (commercial)	Low	RHFL4913 (rad-hard)
Passive Components	COTS (R, C, L)	>100 krad (bulk effects)	Immune	Same, with lot screening

The analysis reveals that the varactor diodes and passive components are inherently radiation-hard due to their simple physics (PN junctions, bulk resistors, ceramic capacitors), requiring no special design consideration beyond lot screening and pre-flight testing to eliminate infant mortality failures. On the other hand, the digital control components are the limiting elements that might require replacement with space-qualified or rad-tolerant variants for flight.

Mitigation strategies for TID: Component upsampling through destructive physical analysis (DPA) and TID testing of procurement lots can extend the commercial parts' effective TID tolerance to 15–30 krad, sufficient for many LEO missions with modest shielding (2–3 mm aluminium equivalent). Table 7.4 identifies candidate replacements for critical components. By following a

modular tile architecture, the interpreter PCB can be redesigned for rad-hard components without changing the tile's mechanical or RF interface.

Mitigation strategies for SEE: Single-event upsets in the microcontroller SRAM and FPGA configuration memory pose a risk of transient failures (incorrect PWM values applied to varactors) or persistent failures (FPGA configuration corruption). Possible solutions include implementing TMR at the FPGA level and using a watchdog on the microcontroller.

Chapter 8

Conclusions and Future Work

This chapter synthesises the thesis’s main findings and distils the architectural and experimental conclusions drawn from the wireless-controlled X-band reflectarray demonstrator. It highlights the contributions, measured performance, limitations, and implications for spaceborne applications. Then it outlines targeted future work from efficiency improvements, calibration and robustness, scale-up to mission-class apertures, and environmental qualification, to raise the TRL of this equipment, allowing for a possible in-orbit demonstration in the future.

8.1 Conclusions

This thesis introduced SATORI, a wirelessly controllable, modular X-band reflectarray architecture that separates the high-frequency aperture from a low-frequency control plane. The central premise was that a sparse command-and-control link at 433 MHz, carried over a simple on-tile receiver and interpreter, can reliably set thousands of tunable phase elements while the payload operates at X-band. The resulting system dispenses with dense data harnesses, simplifies assembly, integration, and test, and scales by tiling identical subassemblies. The work combined unit-cell electromagnetic design, tile-level electronics, software and firmware, and aperture-level system integration, followed by measurements and over-the-air control validation.

The architecture decouples three concerns typically related in future electronically steerable apertures:

1. Electromagnetic performance at the operating band,
2. Distribution of configuration data,
3. Power delivery and health monitoring.

By establishing a dedicated 433 MHz control link, the design enforces frequency orthogonality with the X-band payload. Also, the interpreter RF frontend protects the hardware by out-of-band filtering and limiting. This separation reduces electromagnetic compatibility risks and eliminates subtle RF-to-bias couplings when control signalling shares the operating band or its harmonics.

In parallel, tile-level intelligence, given by a compact interpreter composed of microcontroller logic for protocol handling and a parallel PWM fabric for bias synthesis, localises complexity and enables independent, low-latency updates. The net effect is a software-defined antenna in which high-level commands map deterministically to per-cell voltages without a centralised high-speed architecture.

Performing antenna measurements at FEUP and ESA facilities confirmed the capability of electronically steering the beams across a practical scan range with mainlobe directivity and side-lobe levels consistent with full-wave simulation, including realistic feed illumination, quantisation, and varactor loss models. Broadside results matched predictions to within small margins once residual calibration errors were accounted for, indicating the contributors that govern the observed efficiency: illumination/taper loss, varactor series resistance and bias-dependent Q, dielectric and conductor loss in the stack-up, and phase non-idealities from discretised control states.

The experimental campaign in Chapter 7 directly validates the architectural statements in the initial comparative analysis (Table 1.1). The prototype successfully demonstrated the wireless control paradigm, achieving a Packet Error Rate (PER) of just 0.168% during on-aperture testing, confirming the link's reliability under illumination. The system's responsiveness was confirmed with a measured end-to-end latency of ≈ 58 ms, comfortably meeting the ≤ 100 ms objective. Furthermore, the 0.5×0.5 m, 625-cell aperture successfully achieved its target electronic steering range of $\pm 30^\circ$ with a high pointing accuracy of $\epsilon_\theta \leq 0.2^\circ$. The measured gain of ≈ 17 dBi ($D_{pk} \approx 22.8$ dBi) quantifies the $\approx 25\%$ efficiency trade-off, aligning with the analysis. The previous chapter outlined the loss budget of the system, presenting a way forward for direct improvement and demonstrating that this thesis architecture imposes no performance limitation. All the presented results showed excellent pointing accuracy, not as a standalone result, but as a repeatable one. These results collectively validate that the SATORI approach successfully implements the proposed modular, wirelessly-controlled architecture. In addition, the proposed validated architecture's versatility allows for scalability not only for similar reflectarrays but also for other topologies.

Using varactor-tuned unit cells is a deliberate compromise between continuous phase agility and insertion loss. Varactors allow simple biasing, fine phase resolution, and COTS availability, but their Q-factor and C–V nonlinearity impose penalties on aperture efficiency and calibration stability over temperature and bias. These penalties were mitigated by:

1. Shaping the voltage-to-phase lookup to concentrate resolution where the unit-cell slope is steep,
2. Filtering the PWM-derived bias to reduce ripple and phase noise,
3. Allocating margin in the loss budget.

Regarding scalability and resilience, the tiling enables graceful scale-out and fault containment. Because each tile interprets broadcast and addressed messages, the same air interface serves global reconfigurations and targeted corrections. Fault injection at the tile level showed that the

aperture can often be re-optimised in software to recover most of the gain and constrain sidelobe growth, especially when faults are peripheral. This property favours spaceborne deployments, where partial degradation might occur over mission life. From a manufacturing perspective, identical tiles allow parallel testing, while a single DC feed per tile simplifies power harnessing compared with high-speed digital backplanes.

The demonstrated results establish a credible path to large, steerable apertures that are modular in hardware and software-defined in control. For Earth observation (e.g., SAR) and space communications, the approach allows a lower AIT complexity, improved serviceability, and competitive SWaP. The broader contribution is methodological: treat configuration transport as a separate RF system with its link budget, protections, and interfaces, rather than a side-effect of the payload RF design.

8.2 Future Work

The results motivate a focused roadmap to raise Technology Readiness Level (TRL), improve efficiency, and validate mission utility.

Scaling to larger apertures and higher tile counts is the most direct path to mission-class performance. A larger panel accentuates illumination management, mechanical flatness, and phase uniformity. Future prototypes should:

1. Design a specific feed for the antenna aperture,
2. Refine feed placement and pattern shaping to reduce spillover and taper loss,
3. Change for a higher-Q varactor diode to improve efficiency,
4. Quantify scan loss, cross-polarisation discrimination, and sidelobe behaviour at the edges of the steering envelope,
5. Explore sparse or non-uniform tilings that balance structural constraints with electromagnetic performance.

As already mentioned, although it was not the focus of this thesis, the proposed reflectarray already showed an efficiency in line with typical electronic reflectarrays. In any case, possible efficiency improvements are available mainly at the unit-cell level. On the unit-cell side, higher-Q tunable elements (improved varactors, stacked or resonantly enhanced topologies) can be down-selected through side-by-side tiles to quantify gains against complexity. Temperature sensors, per-tile voltage/current telemetry, and an on-aperture beacon (or near-field probes during AIT) would support automated phase metrology and recalibration in situ. Tightening the voltage-to-phase model over temperature and ageing can reduce mainlobe degradation and sidelobe growth at large scan angles.

To close the gap to flight, the interpreter PCB components should migrate to radiation-tolerant parts or upscreened COTS with characterised total ionising dose and single-event resilience. The

Software chain must include CRC updates, with watchdogs supervising protocol parsing, PWM generation and general functioning of the microcontroller. Power distribution must be hardened against conducted and radiated EMI, with per-tile telemetry exposing margins and enabling fault isolation. At the firmware level, there should be a modular approach with Triple Modular Redundancy (TMR), a fault tolerance technique that uses three identical logic blocks to protect against single-event upsets.

A complete environmental test campaign must occur as part of the TRL increase. Thermal-vacuum cycling, random vibration, and shock will validate mechanical integrity and interconnect robustness at tile seams. EMC testing must specifically target coexistence: measure the radio control signal sensitivity and packet error versus incident X-band EIRP, and measure payload spurious and noise figures.

One of the key aspects of future development is productisation. Design-for-manufacture and design-for-test dominate the schedule and cost at larger scales. Standardised fixtures, automated per-cell bias verification, and access to the interpreter interfaces reduce AIT time and variability. Clear addressing schemes and documented procedures for manufacturing, assembly, programming, and substituting tiles are required to support apertures with dozens to hundreds of tiles.

By completing the previous steps, there would be a technology maturation capable of increasing from TRL4 to TRL8. The ultimate step is to perform an in-orbit demonstration mission to finalise the whole cycle and achieve TRL9.

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