

**FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO**

# **Design and Implementation of a 600V to 24V DC/DC Converter for the Formula Student Prototype**

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# Resumo

Este trabalho apresenta o projeto e a implementação de um conversor DC/DC isolado capaz de reduzir uma tensão de 600 V proveniente do acumulador de alta tensão para 24 V, destinada ao sistema de baixa tensão de um veículo elétrico da Formula Student. O conversor foi projetado para fornecer uma potência de 1 kW, cumprindo os requisitos de isolamento galvânico definidos pelas regras da Formula Student Germany (FSG).

Foi realizada uma revisão do estado da arte para avaliar e comparar as topologias mais adequadas a esta gama de tensão e potência, com foco nas topologias Phase-Shifted Full-Bridge (PSFB) e LLC ressonante. A análise justificou a escolha da topologia LLC de meia ponte, devido à sua elevada eficiência, operação em comutação suave (soft-switching) e design magnético compacto.

O projeto engloba a modelação analítica através da aproximação do primeiro harmónico (FHA), o dimensionamento de parâmetros, a análise em pequena-sinal e o desenvolvimento do controlo. Foi projetado e ajustado um controlador PI de modo a garantir a regulação estável da tensão de saída e uma resposta transitória robusta. Os resultados de simulação em PLECS validaram os modelos teóricos, confirmando o comportamento dinâmico correto e a capacidade de regulação sob diferentes condições de entrada e carga.

O conversor desenvolvido estabelece uma etapa de alimentação de baixa tensão fiável, eficiente e segura para o veículo da Formula Student.

**Palavras-chave:** Conversor DC/DC; Conversor Ressonante LLC; Phase-Shifted Full-Bridge (PSFB); Dual Active Bridge (DAB); Formula Student; Isolamento de Alta Tensão; Conversão 600 V para 24 V; Controlo PI; PLECS; Eletrónica de Potência.

# Abstract

This work presents the design and implementation of an isolated DC/DC converter capable of stepping down 600 V from the high-voltage accumulator to 24 V for the low-voltage system of a Formula Student electric vehicle. The converter was designed to meet a 1 kW power target while complying with galvanic isolation requirements defined by Formula Student Germany (FSG) rules. A state-of-the-art review was conducted to evaluate and compare suitable topologies for this voltage and power range, focusing on the Phase-Shifted Full-Bridge (PSFB) and the LLC resonant converter. The analysis justified the selection of the half-bridge LLC topology due to its high efficiency, soft-switching operation, and compact magnetic design. The project encompasses analytical modeling through the first harmonic approximation (FHA), parameter design, small-signal analysis, and control development. A PI controller was designed and tuned to ensure stable output voltage regulation and robust transient response. Simulation results using PLECS validated the theoretical models, confirming the correct dynamic behavior and regulation capability across varying input and load conditions. The developed converter design establishes a reliable, efficient, and safe low-voltage supply stage for the Formula Student vehicle.

**Keywords:** DC/DC Converter; LLC Resonant Converter; Phase-Shifted Full-Bridge (PSFB); Dual Active Bridge (DAB); Formula Student; High-Voltage Isolation; 600 V to 24 V Conversion; PI Control; PLECS; Power Electronics.

# UN Sustainable Development Goals

The United Nations Sustainable Development Goals (SDGs) provide a global framework to guide actions towards a fair, sustainable, and resilient future. Comprising 17 interconnected objectives, this agenda addresses key challenges such as climate change, inequality, access to clean energy, and environmental sustainability.

This dissertation, focused on the design and implementation of an isolated DC/DC converter for a Formula Student electric prototype, directly contributes to SDG 7 (Affordable and Clean Energy) and SDG 8 (Decent Work and Economic Growth) through innovation in efficient energy conversion and the promotion of engineering education and collaboration.

The specific Sustainable Development Goals mentioned have the following names:

**SDG 7** Ensure access to affordable, reliable, sustainable and modern energy for all

**SDG 8** Promote sustained, inclusive and sustainable economic growth, full and productive employment and decent work for all

The connection between this research and specific SDG targets is summarized below:

| SDG | Target | Contribution                                                                                                                                                                 | Performance Indicators and Metrics                                                                                                                  |
|-----|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | 7.1    | Development of a custom isolated DC/DC converter for the FSFEUP vehicle improves conversion efficiency, reliability, and sustainability of the low-voltage auxiliary system. | Regulated 24 V from 600 V input; verified via PLECS simulations and prototype validation on the Vasco da Gama CoLAB platform.                       |
|     | 7.a    | Collaboration among FEUP, FSFEUP, and Vasco da Gama CoLAB promotes applied research and innovation in clean, efficient vehicle power electronics.                            | Partnerships formalized; joint supervision and development milestones; modular design and documentation shared for future Formula Student projects. |
| 8   | 8.2    | In-house design and implementation strengthen local engineering capability and reduce dependence on commercial converter modules.                                            | Converter fully designed and assembled internally, with cost reduction versus comparable commercial units.                                          |
|     | 8.6    | Project enhances student training and hands-on experience in sustainable mobility power electronics.                                                                         | Student-led design, simulation, and testing; FSFEUP prototype integrated into the team's vehicle; knowledge transfer to subsequent cohorts.         |

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Guilherme Pereira

*“Ai, meu patrão, troveja, relampeja, chove que mete medo, zás, na cama!”*

Maria Alzira da Silva Pereira

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# List of Acronyms

|          |                                                                                 |
|----------|---------------------------------------------------------------------------------|
| AC       | Alternating Current                                                             |
| APM      | Auxiliary Power Module                                                          |
| APS      | Auxiliary Power Supplies                                                        |
| BMS      | Battery Management System                                                       |
| $C_r$    | Series Capacitance                                                              |
| CSI      | Common Source Inductance                                                        |
| DAB      | Dual Active Bridge                                                              |
| DC       | Direct Current                                                                  |
| DF       | Dissipation Factor                                                              |
| ECU      | Electric Control Unit                                                           |
| EMI      | Electromagnetic Interference                                                    |
| ESR      | Equivalent Series Resistance                                                    |
| EV       | Electric Vehicle                                                                |
| FEUP     | Faculty of Engineering of the University of Porto                               |
| FET      | Field-Effect Transistor                                                         |
| FHA      | First Harmonic Approximation                                                    |
| FS       | Formula Student                                                                 |
| FSG      | Formula Student Germany                                                         |
| FSFEUP   | Formula Student team from the Faculty of Engineering of the University of Porto |
| $F_p$    | Parallel Resonant Frequency                                                     |
| $F_r$    | Resonant Frequency                                                              |
| $F_s$    | Switching Frequency                                                             |
| $F_x$    | Normalized Switching Frequency                                                  |
| $G_{dc}$ | DC Voltage Gain                                                                 |
| $GaN$    | Gallium Nitride                                                                 |
| HV       | High Voltage                                                                    |
| $L_m$    | Magnetizing Inductance                                                          |
| $L_s$    | Leakage Inductance                                                              |
| LV       | Low Voltage                                                                     |
| LVS      | Low Voltage system                                                              |
| m        | Ratio of Total Primary Inductance to Resonant Inductance                        |
| MLCC     | Multilayer Ceramic Capacitors                                                   |
| MOSFET   | Metal-Oxide-Semiconductor Field-Effect Transistor                               |
| n        | Transformer Turn Ratio                                                          |
| $N_p$    | Number of Primary Turns                                                         |
| $N_s$    | Number of Secondary Turns                                                       |
| PCB      | Printed Circuit Board                                                           |

|              |                                                |
|--------------|------------------------------------------------|
| PI           | Proportional Integral                          |
| PLECS        | Piecewise Linear Electrical Circuit Simulation |
| PSFB         | Phase Shift Full Bridge                        |
| PWM          | Pulse-Width Modulation                         |
| Q            | Quality Factor                                 |
| $R_{ac}$     | Reflected Load Resistance                      |
| RMS          | Root Mean Square                               |
| $S_iC$       | Silicon Carbide                                |
| SOA          | Safe Operating Area                            |
| TS           | Tractive System                                |
| ZCS          | Zero Current Switching                         |
| ZVS          | Zero Voltage Switching                         |
| $Z_{series}$ | Series Impedance                               |

# Chapter 1

## Introduction

In today's competitive field of electric vehicle engineering, the Formula Student (FS) competition stands out as a unique platform where university teams from around the world compete to design, build, and race high-performance electric vehicles, [17]. FS is not only a test of speed but a test of innovation, challenging detail engineer, and teamwork. I am a current member of the Electronics & Software Department within a Formula Student team, based in Porto, Portugal, Figure 1.1. A team established four years ago and supported by a dedicated group of engineer student, striving to build the best possible electric race car.



Figure 1.1: Formula Student Porto Team, [17].

Our team's mission is simple yet challenging: to push the limits of what an electric racing car can achieve within the constraints of FS competition rules [18]. Each subsystem of the vehicle must be meticulously designed, refined, and tested to maximize both performance and reliability. The project's emphasis on power conversion efficiency and weight reduction directly aligns with these goals. One of the most impactful upgrades to improve overall vehicle performance and efficiency is a DC/DC converter, which interfaces the vehicle's high-voltage battery system with its low-voltage electronics. Replacing the low-voltage battery traditionally used in the car with a high-performance DC/DC converter not only saves weight but also allows for optimized power distribution throughout the vehicle.

This ambitious endeavor is made possible through the invaluable support of Vasco da Gama [52] who plays a pivotal role in advancing engineering excellence, particularly in the challenging

and innovative field of Formula Student. As a partner of FS FEUP, Vasco da Gama CoLAB has consistently demonstrated its commitment to fostering engineering talent and supporting groundbreaking projects. Their expertise, resources, and guidance provide an unparalleled opportunity for growth and development, making them an invaluable ally in the pursuit of engineering excellence.

Having the opportunity to carry out my master's dissertation with the support of Vasco da Gama CoLAB is not only a privilege but also a source of immense motivation. Their trust in my abilities and their dedication to this project create an environment where I can push my limits, learn from industry professionals, and grow into a more competent and confident engineer. This collaboration allows me to bridge academic knowledge with real-world applications, sharpening my technical skills while broadening my understanding of practical engineering challenges.

Through this partnership, I am able to contribute to a project that holds significant potential to elevate the performance and engineering capabilities of the FS FEUP vehicle. The development of a 600V to 24V DC/DC converter, tailored to the specific requirements of Formula Student. It will enhance the vehicle's efficiency, reliability, and competitiveness, marking a vital step forward in its evolution.

## **1.1 Aim of the Thesis**

The aim of this thesis is to explore and analyze galvanically isolated DC/DC converter topologies to identify and develop the most suitable solution for application in a Formula Student electric vehicle prototype. The focus is on designing a DC/DC converter that meets the specific requirements of the FS FEUP team while adhering to the strict technical and safety standards outlined by the Formula Student competition rules.

This involves not only selecting and optimizing the appropriate topology but also ensuring the converter aligns with the team's design objectives, such as high efficiency, weight reduction, and reliable performance. The details of these requirements, along with the governing competition rules, will be discussed in subsequent sections to provide a comprehensive understanding of the challenges and constraints that shaped this development process.

## **1.2 Formula Student Rules and Requirements**

The Formula Student competition challenges university teams to design, build, and race electric vehicle prototypes while adhering to stringent regulations. These regulations shape the technical specifications of all systems, including the electrical powertrain, ensuring safety, reliability, and performance.

In the scope of the auxiliary power supply, a 600 V to 24 V unidirectional DC/DC converter, to replace the necessary for an additional battery, several rules need to be followed as requirements set by the competition. To be more precise, the standard and the rules that this design will follow will be the rules of the most privileged competition in the world, which is the German competition.

The Formula Student Germany (FSG) rules impose strict requirements on electric vehicle designs to ensure safety and fair competition. These rules directly influence the design of auxiliary DC/DC converters:

### ***EVI.1 Tractive System***

***EVI.1.1*** *Tractive System (TS) – every part that is electrically connected to the motors and TS accumulators. The LVS may be supplied by the TS if a galvanic isolation between both systems is ensured.*

### ***EVI.2 Electrical***

***EVI.2.1*** *Galvanic Isolation – two electric circuits are defined as galvanically isolated if all of the following conditions are true:*

- *The resistance between both circuits is more or equal to 500 Ohm/V, related to the maximum TS voltage of the vehicle, at a test voltage of maximum TS voltage or 250 V, whichever is higher.*
- *The isolation test voltage RMS, AC for 1 min, between both circuits is higher than three times the maximum TS voltage or 750 V, whichever is higher.*
- *The working voltage of the isolation barrier, if specified in the datasheet, is higher than the maximum TS voltage.*

*Capacitors that bridge galvanic isolation must be class-Y capacitors.*

These regulations emphasize the necessity of galvanic isolation, robust electrical insulation, and compliance testing during vehicle inspection. They shape the foundational design of any DC/DC converter for Formula Student applications.

## **1.3 DC/DC Converter Design Requirements**

The design of a DC/DC converter for a Formula Student prototype must address several key considerations:

**High Efficiency:** Maximizing energy transfer minimizes power losses, reducing heat generation and extending the vehicle's operating range during races.

**Thermal Management:** Efficient heat dissipation is critical to maintaining performance and reliability under the intense conditions of Formula Student competitions.

**Compactness and Power Density:** Space and weight constraints in Formula Student vehicles demand compact, lightweight converters with high power density to optimize vehicle dynamics and performance.

**Electromagnetic Compatibility (EMC):** Suppressing electromagnetic interference (EMI) is essential to avoid disruptions to sensitive LV systems like control electronics and sensors.

**Light Load Efficiency:** Many LV systems operate intermittently during a race, requiring the converter to maintain high efficiency even under partial loads.

**Load Variation Response:** The DC/DC converter must handle rapid load changes without compromising stability or efficiency, ensuring consistent performance under dynamic racing conditions.

By addressing these considerations, the DC/DC converter can meet the demanding performance, safety, and reliability requirements of Formula Student vehicles.

## Chapter 2

# State-of-the-Art

### 2.1 Overview of Isolated DC/DC Converters

Isolated DC/DC converters are indispensable components in electric vehicle (EV) architectures, facilitating efficient energy transfer and ensuring the safety and reliability of power systems. These converters are particularly critical in modern EVs, where they bridge the high-voltage (HV) traction battery and low-voltage (LV) auxiliary systems [8, 10, 33]. Their role is foundational to the seamless operation of EV powertrains, making them a cornerstone of ongoing advancements in power electronics.

#### 2.1.1 Role of Isolated DC/DC Converters in EV Architectures

The electrification of transportation, a defining technological shift of the 21st century, has imposed stringent requirements on EV powertrain systems. As illustrated in Figure 2.1, the HV traction battery powers the propulsion system and provides energy to LV auxiliary loads, such as electronic control units (ECUs), lighting, and infotainment systems [10].

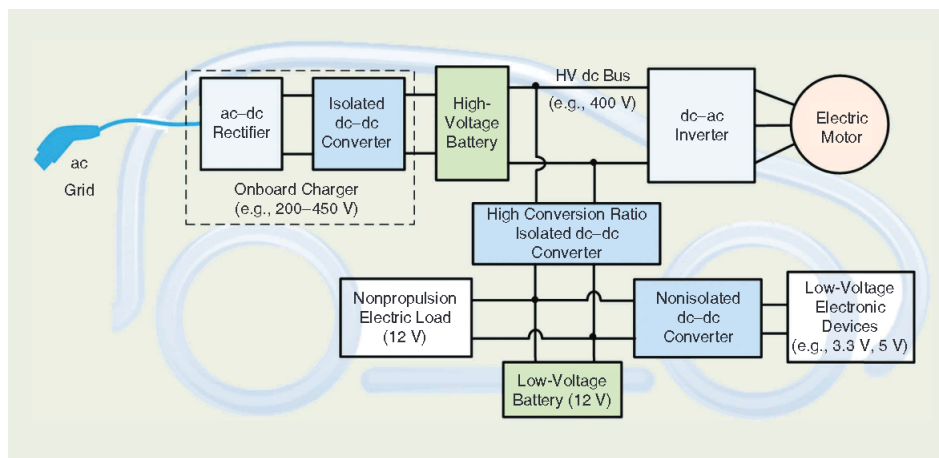


Figure 2.1: Architecture of a typical battery-powered EV, [10].

In this architecture:

- The high-voltage DC bus connects the traction battery to the inverter, which drives the electric motor. The onboard charger integrates an AC-DC rectifier and an isolated DC/DC converter to charge the HV battery from the grid.
- A high-conversion-ratio isolated DC/DC converter links the HV bus to the LV system. This converter efficiently steps down the voltage to 12V or 24V for powering auxiliary systems like sensors, control units, and communication modules, while maintaining galvanic isolation for safety.

Figure 2.1 encapsulates the comprehensive integration of these components within an EV powertrain, showcasing the isolated DC/DC converter as a pivotal element in connecting and isolating the high-voltage and low-voltage systems.

## 2.2 Topology Analysis

### 2.2.1 Overview of Isolated DC/DC Converter Topologies

Isolated DC/DC converters are critical components in electric vehicles (EVs), enabling efficient energy transfer between high-voltage (HV) and low-voltage (LV) domains. A classification of DC/DC converters based on their isolation is shown in Figure 2.2.

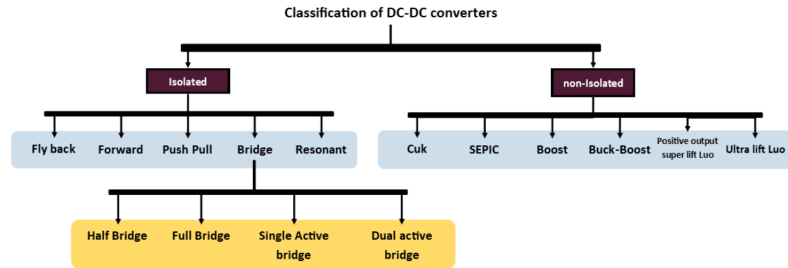


Figure 2.2: Classification of DC/DC Converters, [40].

Various topologies have been developed, each offering unique advantages and limitations:

#### 2.2.1.1 Flyback Converter

The flyback converter is widely used for low-power applications due to its simplicity and low cost. However, for high-power applications such as the Formula Student prototype's 1kW requirement, the flyback converter suffers from limitations like high voltage stress on components, low efficiency, and difficulty managing electromagnetic interference (EMI) [4, 5].

#### 2.2.1.2 Forward Converter

The forward converter improves upon the flyback design by introducing a tertiary winding to reset the transformer's core, which reduces voltage stress and improves efficiency. Despite these

improvements, its power-handling capability is limited, making it unsuitable for high-power, high-voltage applications [6].

#### **2.2.1.3 Push-Pull Converter**

The push-pull converter uses two switches on the primary side of the transformer, offering improved power handling compared to the flyback and forward converters. However, it suffers from high voltage stress on switches and poor efficiency at higher power levels, which disqualifies it for the Formula Student requirements [5].

#### **2.2.1.4 Half-Bridge Converter**

The half-bridge converter provides moderate efficiency and power handling. However, its design complexity and the potential for voltage imbalance across the capacitors limit its scalability to higher power levels [39].

#### **2.2.1.5 Full-Bridge Converter (Without Phase Shift)**

The standard full-bridge converter can handle higher power levels but lacks soft-switching capabilities (e.g., ZVS), which limits its efficiency at high frequencies. This limitation makes it unsuitable for applications requiring high efficiency and compact thermal management [5].

#### **2.2.1.6 Resonant Converters**

Resonant converters, such as the LLC Resonant topology, utilize a resonant tank comprising inductors and capacitors to achieve soft switching and high efficiency. The LLC topology is particularly suited for high-voltage, high-power applications, as it minimizes switching losses and provides excellent thermal management [4, 5].

#### **2.2.1.7 Dual Active Bridge (DAB) Converter**

The DAB converter features two full bridges on the primary and secondary sides of the transformer, enabling bidirectional power flow. Its symmetrical design and advanced modulation schemes allow efficient energy transfer across a wide range of operating conditions. The DAB topology is increasingly popular in EV applications due to its scalability and high efficiency [4, 39].

### **2.2.2 Justification for Focusing on LLC Resonant, PSFB, and DAB Topologies**

The selection of LLC Resonant, PSFB, and DAB converters as the most suitable topologies for the Formula Student application is based on the specific design requirements: a high step-down ratio from 600V to 24V, 1kW output power, and the need for galvanic isolation. Other isolated topologies were excluded for the following reasons:

- **Flyback Converter:** Limited power-handling capability, high voltage stress, and low efficiency at high power levels [4, 5].
- **Forward Converter:** Power-handling capability is insufficient for a 1kW system [6].
- **Push-Pull Converter:** High voltage stress and limited efficiency at higher power levels [5].
- **Half-Bridge Converter:** Design complexity and voltage imbalance issues [39].
- **Full-Bridge Converter (Without Phase Shift):** Lack of soft-switching capabilities reduces efficiency at high frequencies [5].

The LLC Resonant, PSFB, and DAB converters meet the key requirements of Formula Student vehicles, providing the optimal balance between efficiency, power density, and control complexity required for a compact and high-performance system. The detailed analysis supporting the selection of the most suitable topology for this application is presented in Section 2.4.

## 2.3 MOSFET Operation

MOSFETs are fundamental components in DC/DC converter designs, especially with the advent of SiC and GaN technology. Their efficient switching capabilities and low conduction losses make them ideal for high-frequency and high-power applications. Understanding the nature of losses in MOSFETs is crucial for optimizing converter performance.

### 2.3.1 Conduction and Switching Losses

MOSFET power losses are primarily categorized into conduction losses and switching losses.

#### 2.3.1.1 Conduction Losses

Conduction losses occur when the MOSFET is in the 'on' state, allowing current to flow through its channel. The resistance offered by the channel in this state is denoted as  $R_{DS(on)}$ . The power dissipated due to this resistance is given by:

$$P_{cond} = I_D^2 \times R_{DS(on)} \quad (2.1)$$

where  $I_D$  is the drain current. Minimizing  $R_{DS(on)}$  is essential to reduce conduction losses, which is a significant advantage of SiC MOSFETs due to their inherently lower  $R_{DS(on)}$  compared to traditional silicon MOSFETs.

#### 2.3.1.2 Switching Losses

Switching losses occur during the transitions between the 'on' and 'off' states of the MOSFET. These losses are attributed to the simultaneous presence of voltage across the MOSFET and current through it during switching events. The total switching loss per cycle can be approximated by:

$$P_{sw} = \frac{1}{2} V_{DS} I_D (t_{rise} + t_{fall}) f_{sw} \quad (2.2)$$

where:

- $V_{DS}$  = Drain-to-source voltage
- $t_{rise}$  = Rise time during turn-on
- $t_{fall}$  = Fall time during turn-off
- $f_{sw}$  = Switching frequency

It's important to note that this equation provides an estimate and may not account for all parasitic elements present in practical circuits.

### 2.3.2 Soft Switching

Soft-switching techniques are employed to reduce commutation losses by minimizing the voltage or current present during switching transitions. The two main approaches are ZVS and ZCS. Although these methods ideally achieve lossless transitions, in practice, they significantly reduce, but do not entirely eliminate, switching losses due to non-ideal device characteristics and parasitic elements. Figure 2.3 illustrates the characteristic current and voltage waveforms for a PSFB converter operating under hard-switching and soft-switching conditions, respectively.

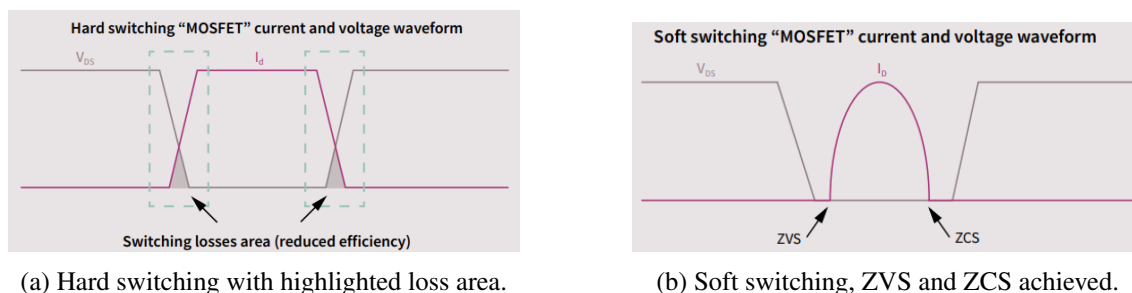


Figure 2.3: PSFB converter key current and voltage waveforms illustrating hard-switching and soft-switching operation, [2].

#### 2.3.2.1 Zero Voltage Switching (ZVS)

In ZVS, the MOSFET is turned on when the voltage across it is zero. This is typically achieved by using resonant circuits or adding auxiliary components that create conditions where the drain-source voltage  $V_{DS}$  drops to zero before the MOSFET turns on. By ensuring  $V_{DS} = 0$  at the moment of switching, the overlap between voltage and current is minimized, thereby reducing switching losses.

#### 2.3.2.2 Zero Current Switching (ZCS)

ZCS involves turning the MOSFET on or off when the current through it is zero. This approach is common in applications where inductive components are present. By timing the switching event to occur when the current naturally crosses zero, the energy dissipated during the transition is minimized, leading to lower switching losses.

Implementing soft switching techniques like ZVS and ZCS is essential in high-frequency DC/DC converters to enhance efficiency and reduce thermal stress on the components.

## 2.4 Focus on LLC, DAB and PSFB

### 2.4.1 Phase-Shift Full-Bridge (PSFB) Converter

The PSFB converter, Figure 2.4, is a highly versatile and efficient isolated DC/DC converter topology widely used in medium- to high-power applications. Its design is based on a full-bridge configuration, incorporating four active switches on the high-voltage side and a rectification stage on the low-voltage side. This topology is particularly suitable for electric vehicle (EV) systems, such as auxiliary power supplies (APS), where high voltage step-down ratios, galvanic isolation, and high power density are required [32].

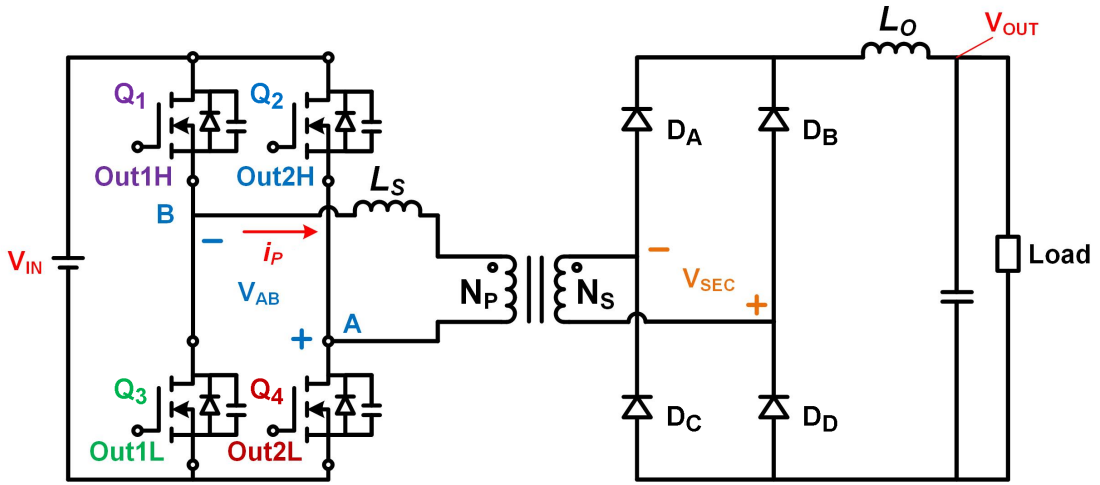


Figure 2.4: PSFB with a full-bridge rectifier, [32].

The shim inductor is implemented to extend the ZVS range. To guarantee ZVS operation even at the lowest achievable primary current, the shim inductor must satisfy the following conditions, [37]:

$$L_S \geq (2 \cdot C_{OSS,avg}) \cdot \frac{V_{in,max}^2}{\left(\frac{i_{p2}^2}{2} \frac{\Delta L}{2n}\right)^2} - L_{leak} \quad (2.3)$$

where  $L_{leak}$  represents the transformer's leakage inductance and the average output capacitance of the switch is given by, [37]:

$$C_{OSS,avg} = \sqrt{\frac{V_{ds,test}}{V_{in,max}}} C_{OSS} \quad (2.4)$$

Here,  $C_{OSS}$  denotes the normalized output capacitance of the switch.

The output inductor is crucial in controlling the output current ripple and minimizing stress on secondary-side components. Its value can be determined using the following expression, [37]:

$$L_O = \frac{V_O(1 - D_{typ})}{2\Delta I_L f_s} \quad (2.5)$$

Where  $D_{\text{typ}}$  is the nominal duty cycle.

As shown in Figure 2.5, the full-bridge converter waveforms under phase-shifted control exhibit a negative drain-to-source current before the MOSFET turn-on transitions, enabling soft switching.

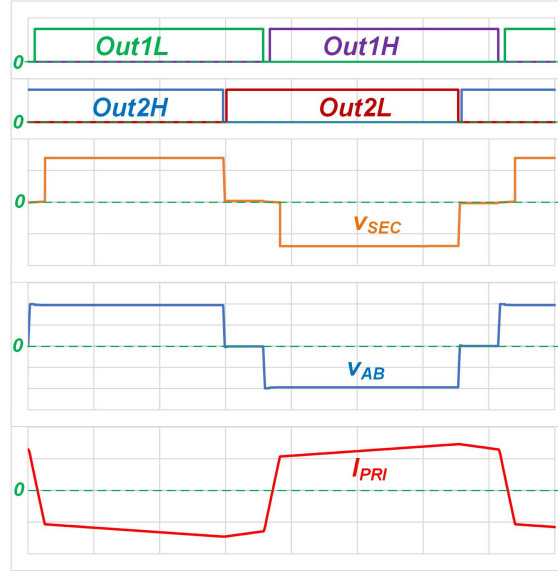


Figure 2.5: PSFB waveforms, [32].

As illustrated in Figure 2.5, the PSFB converter operates by introducing a phase difference between the gate driving signals of the two primary legs of the full-bridge circuit. Specifically, leg 1 MOSFET driving signals (Out1L and Out1H) are phase-shifted relative to leg 2 MOSFET driving signals (Out2L and Out2H), while the duty cycle of all four driving signals remains constant. This phase shift determines the duration of the voltage pulse ( $V_{AB}$ ), which directly impacts energy transfer between the primary and secondary sides of the transformer [32].

During operation, when a diagonal pair of MOSFETs (e.g.,  $Q_1$  and  $Q_4$  or  $Q_2$  and  $Q_3$ ) is turned on, either the input voltage ( $+V_{\text{IN}}$ ) or its inverse ( $-V_{\text{IN}}$ ) is applied across the transformer's primary winding ( $V_{AB}$ ). The series inductor ( $L_S$ ) is energized during this interval, enabling energy transfer from the primary side to the secondary side through the transformer. The phase difference between the two legs dictates the non-zero voltage duration of  $V_{AB}$ , which directly controls the energy transfer.

On the secondary side of the transformer, the voltage waveform ( $V_{\text{SEC}}$ ) is a bipolar square wave that mirrors  $V_{AB}$ . This waveform is then rectified by the output rectification stage to produce a unipolar square wave. The output inductor subsequently performs a "buck" operation to regulate the output voltage, with the pulse width of  $V_{\text{SEC}}$  controlling the output voltage level. This method of operation allows the PSFB converter to achieve efficient voltage regulation while maintaining soft-switching capabilities [32].

### 2.4.1.1 Modes of Operation and Working Stages

The Phase-Shift Full-Bridge (PSFB) converter operates by regulating the phase difference between the two bridge legs on the primary side. Its operation is divided into distinct stages, each characterized by specific current and voltage waveforms. In fact, the PSFB topology can be referred to as six staging modes, due to its cyclic symmetry. Figure 2.26, represents the variables waveforms present in a cycle of operation.

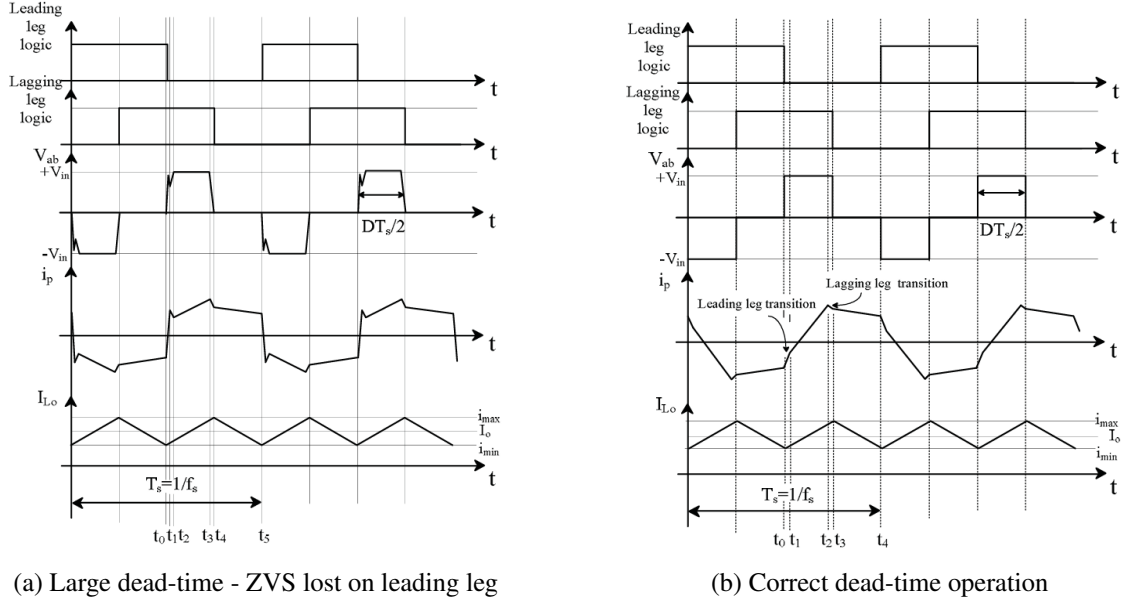


Figure 2.6: PSFB converter key waveforms, [37]

Before time  $t_1$ , the active components in the circuit include diodes  $D_1$ ,  $D_A$ ,  $D_B$ ,  $D_C$ , and  $D_D$ . At this moment, the voltage at both the primary and secondary windings of the transformer ( $V_{T_{in}}$  and  $V_{T_{out}}$ ) is zero. Additionally, the current flowing through the primary winding of the transformer is negative, represented as  $-I_p$ .

The PSFB converter's operation can be broken into the following key stages within a switching cycle [22, 37, 45, 46]:

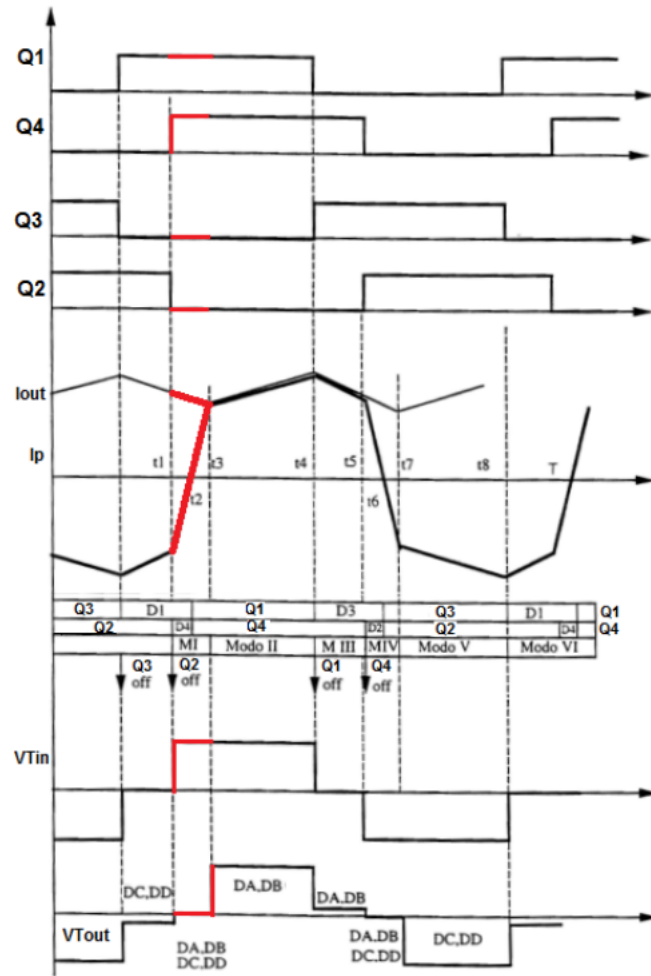
**Mode I - duty cycle loss**

Figure 2.7: Mode I, [45].

The mode *I* lasts from  $t_1$  to  $t_3$ , as shown in Figure 2.7. At the initial moment, transistor  $Q_2$  is turned off by removing the gate drive signal, while transistor  $Q_1$  remains on. Then,  $Q_4$  is switched on. However, due to the negative current in the transformer primary winding ( $I_p$ ) at that moment,  $Q_4$  does not conduct.

The inductor  $L_s$ , located in the transformer primary winding, is responsible for storing sufficient energy to enable ZVS. During this stage,  $L_s$  accumulates energy due to the interaction between the parasitic capacitors of  $Q_2$  and  $Q_4$ , where  $Q_2$  is charging while  $Q_4$  is discharging. On the transformer's secondary side, all four rectifier diodes are conducting, effectively short-circuiting the secondary winding.

The transformer secondary voltage  $V_{sec}$  remains at zero until the primary current  $I_p$  reverses to the positive direction and rises to reach the reflected output inductor current  $I_{Lo}$  at mode  $t_3$ .

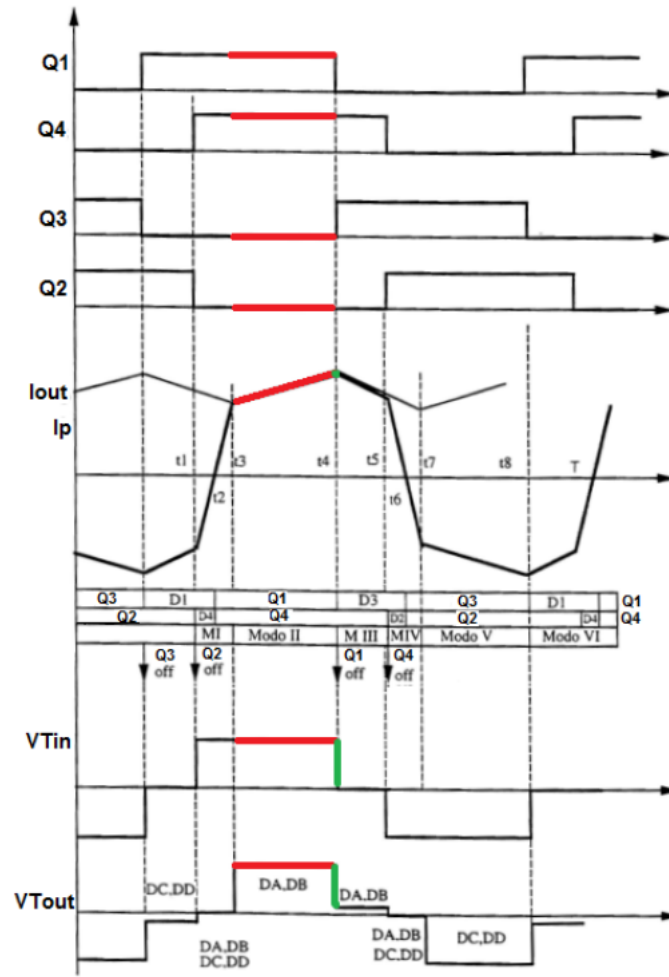
**Mode II - power delivery mode**

Figure 2.8: Mode II, [45].

At  $t_4$  this mode ends with a transition on  $Q_1$  to off.

In this mode, highlighted in Figure 2.8, energy is transferred to the load. At time  $t_3$ , the transformer secondary voltage  $V_{\text{sec}}$  equals  $nV_{\text{in}}$ , and the rectifier diodes  $D_A$  and  $D_D$  are forward biased and conducting. As a result, the converter operates as a full bridge with PWM, since transistors  $Q_1$  and  $Q_4$  are both active, completing the circuit.

The effective phase-shift duty cycle begins in the interval from  $t_3$  to  $t_4$ . During this period, the current through the output filter starts to increase, and the primary winding current  $I_p$  reaches the reflected output inductor current  $nI_{L_o}$ .

At  $t_4$ , this mode ends with the transition of  $Q_1$  to the off state.

**Mode III -  $Q_3$  ZVS**

In this mode, which corresponds to time  $t_4$ , transistor  $Q_1$  turns off.

Transistor  $Q_4$  remains active and conducts the primary current to capacitors  $C_1$  and  $C_3$ , charging  $C_1$  and discharging  $C_3$  from  $nV_{in}$  to zero. When  $C_3$  is fully discharged, the body diode  $D_3$  starts to conduct, enabling ZVS for  $Q_3$ .

In this mode, the transformer secondary voltage becomes zero, and the rectifier diodes  $D_A$  and  $D_D$  carry current.

#### Mode IV - freewheeling mode

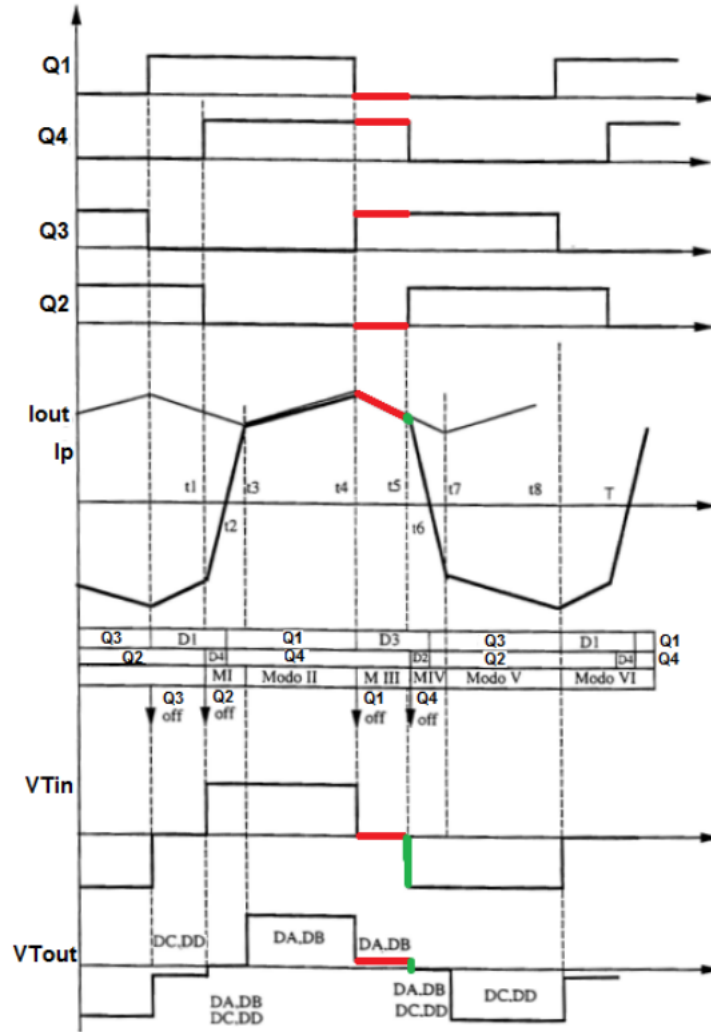


Figure 2.9: Mode IV, [45].

At mode IV, Figure 2.9, at time  $t_4$ , transistor  $Q_3$  is turned on, and the primary current  $I_p$  freewheels through  $Q_3$  and  $Q_4$ .

During the interval from  $t_4$  to  $t_5$ , the voltage  $nV_{in}$  is zero, and the current  $I_p$  decreases due to the short circuit of the power transformer's primary winding through  $Q_3$  and  $Q_4$ . Additionally, the output inductor voltage is discharged by the load.

**Mode V -  $Q_2$  ZVS**

At time  $t_5$ , transistor  $Q_4$  is turned off, and the transformer's primary current charges the capacitor  $C_4$  of transistor  $Q_4$  while discharging the capacitance  $C_2$  of transistor  $Q_2$ . When capacitance  $C_2$  is fully discharged from  $nV_{in}$  to zero, the body diode  $D_2$  starts to conduct, enabling ZVS for transistor  $Q_2$ .

As a result, the circuit transitions into the symmetrical mode I.

**2.4.1.2 Zero Voltage Switching (ZVS) and Efficiency Benefits**

The ZVS operation is directly influenced by the load current and the dead-time interval. At higher loads, sufficient energy stored in the leakage inductance ensures complete discharge of the MOSFET output capacitance, achieving ZVS. However, at lighter loads, the reduced energy in the resonant circuit makes it challenging to sustain ZVS, leading to increased switching losses due to hard-switching events. While auxiliary circuits or advanced control strategies can restore ZVS under low-load conditions, they often come at the cost of increased circuit complexity. Consequently, a trade-off between efficiency, cost, and design simplicity is necessary when optimizing phase-shift full-bridge converters for varying load conditions [32, 53].

**2.4.1.3 Analysis of Current Stress and Rectifier Losses**

Circulating currents during the non-power transfer phase increase the current stress on primary-side MOSFETs, contributing to conduction losses. This circulating current, while essential for enabling ZVS, requires careful optimization of the transformer leakage inductance to balance the trade-off between ZVS achievement and conduction losses [32].

The rectification stage on the secondary side experiences significant conduction losses, especially in high-power, low-voltage applications. Synchronous rectification can reduce these losses by minimizing the forward voltage drop compared to traditional diodes. However, such designs may introduce additional control complexity and increased costs. [53].

**2.4.1.4 Efficiency Implications**

Combined losses from primary-side current stress and secondary-side rectifier inefficiencies can significantly affect the converter's overall performance. Advanced control strategies, such as variable dead-time adjustments, dynamically optimize ZVS and minimize losses across varying load conditions, improving efficiency over a wide operational range [32, 53].

### 2.4.2 Dual Active Bridge (DAB) Converter

The DAB converter, shown in Figure 2.10, is a highly versatile and efficient isolated DC/DC topology widely used in medium- to high-power applications. It consists of two full-bridge converters—one on the primary side and another on the secondary side of a transformer—connected by a leakage inductance. This structure supports bidirectional power transfer and provides excellent control capabilities, making it suitable for applications such as EV chargers, renewable energy systems, and energy storage [42], [7].

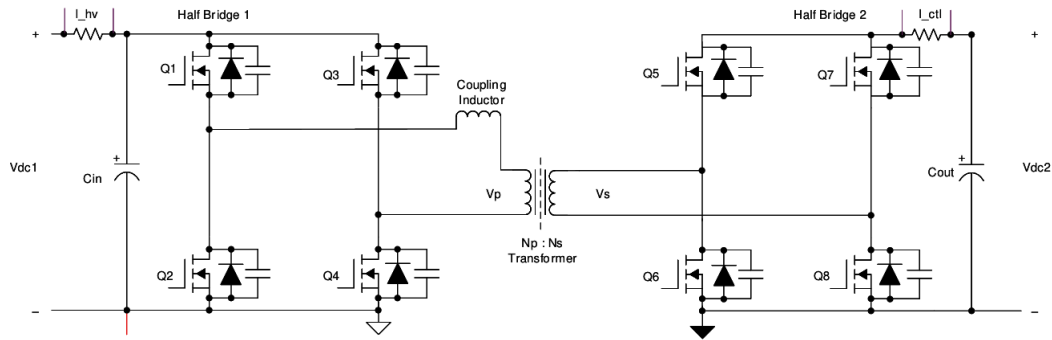


Figure 2.10: DAB Converter, [25].

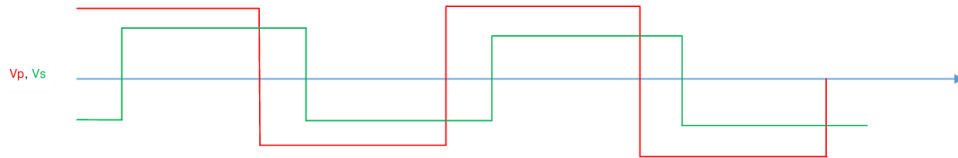


Figure 2.11: DAB waveforms, [25].

In a DAB converter, power transfer occurs through the generation of high-frequency square waves on both the primary and secondary sides of the transformer, facilitated by the switching action of MOSFETs, illustrated in Figure 2.11. These square waves are phase-shifted relative to each other, enabling power transfer from the leading bridge to the lagging bridge. The direction of power flow can be reversed simply by altering the phase shift between the two bridges.

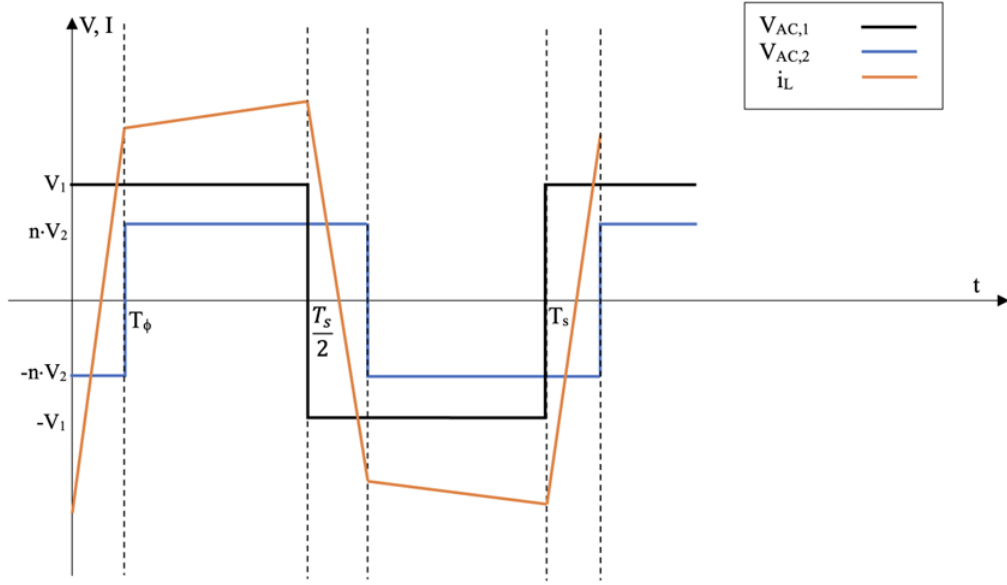


Figure 2.12: Square wave voltages with phase shift  $\phi$  and current profile in one period, [9].

Phase-shift modulation, shown in Figure 2.12, operates with a duty cycle fixed at  $D_1 = D_2 = 0.5$  while maintaining a constant switching frequency  $f_s$  for both square waves. The only varying parameter is the relative phase shift between the two waves, which will be denoted by a phase shift duty ratio, which is defined as follows:

$$D_\phi = \frac{T_\phi}{\frac{T_s}{2}} \quad (2.6)$$

Where the phase shift represented in seconds is given by  $T_\phi$  and  $T_s$  being the switching period, with  $\frac{T_s}{2}$  representing the duration of a half-cycle of the period.

By knowing that the power transfer function of the DAB converter is written as:

$$P_1 = \frac{nV_1V_2\phi(\pi - \phi)}{2\pi^2 f_s L_S} \quad (2.7)$$

The expression shows the dependence of the average power transfer on the phase shift  $\phi$ , which can be seen in Figure 2.13.

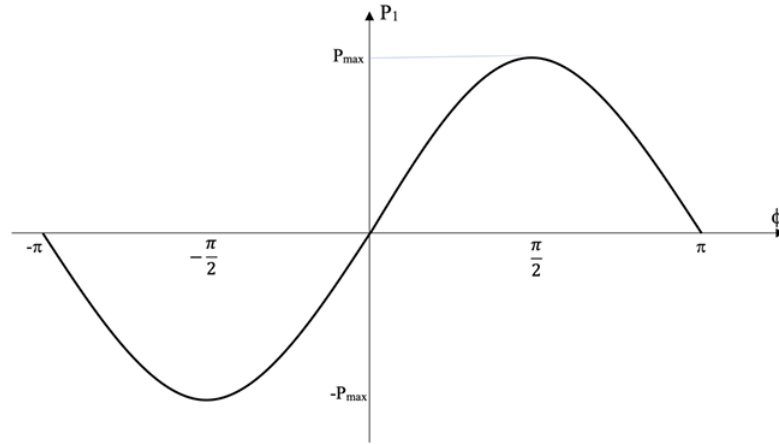


Figure 2.13: Power vs phase shift  $\phi$ , [9].

The maximum power is located when the phase shift has the absolute value of  $\frac{\pi}{2}$ , with a maximum power value given by:

$$|P_{1,\max}| = \frac{nV_1V_2}{8f_sL_S} \quad (2.8)$$

This inherent feature, shown in 2.10, allows the DAB to achieve seamless bidirectional power transfer, as illustrated in Figure 2.13.

#### 2.4.2.1 Modes of Operation of the DAB Converter

The diagonal switches are switched on and off simultaneously, generating a square wave output from each bridge. The switching operation of the converter is detailed in this section, [7, 9, 25, 34, 50].

The switching sequence is divided into four intervals, defined by the inductor current waveform and the phase shift between the voltages on the primary and secondary sides of the transformer. Figure 2.14 presents the corresponding voltage and current waveforms of the DAB converter.

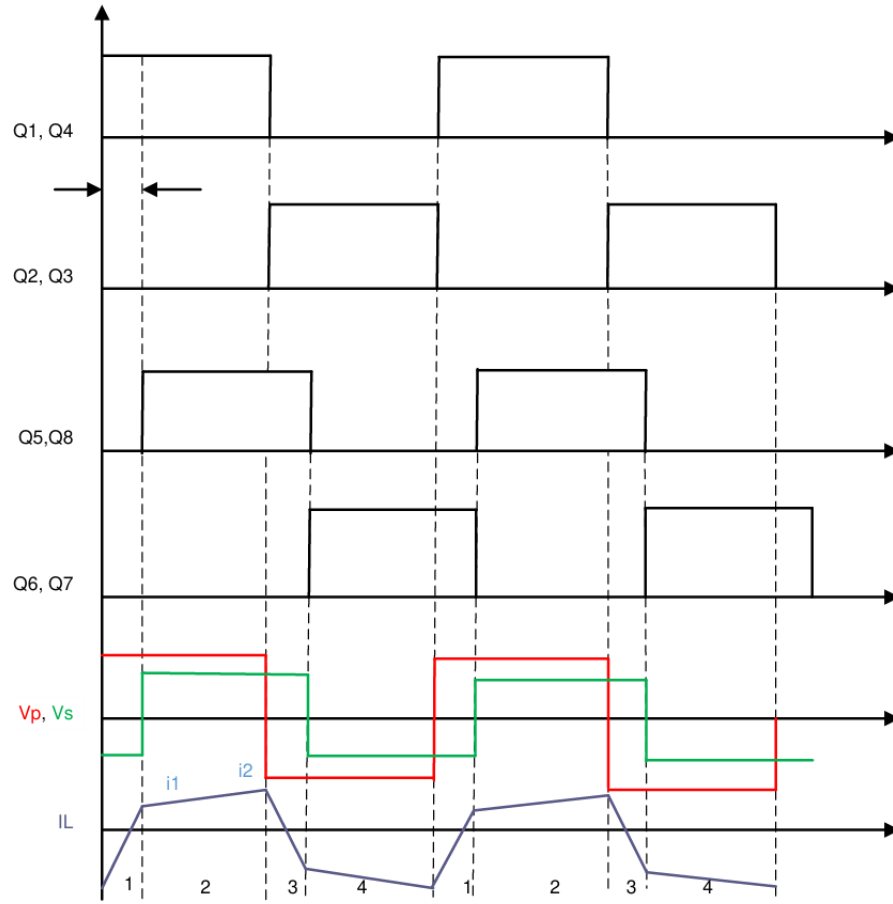


Figure 2.14: Gate Signals, Transformer Pri. and Sec. Voltages, Inductor Current, [25].

### Mode I

**Time interval:**  $0 < t < T_\phi$ , where:

$$T_\phi = \frac{\phi}{2\pi \cdot f_s} = T_s \cdot \frac{\phi}{2\pi} \quad (2.9)$$

In this interval, the inductor current alternates between positive and negative phases, following the commutation pattern illustrated in Figures 2.15 and 2.16. During this phase, switches  $Q_1$  and  $Q_4$  on the primary side, as well as switches  $Q_6$  and  $Q_7$  on the secondary side, conduct current.

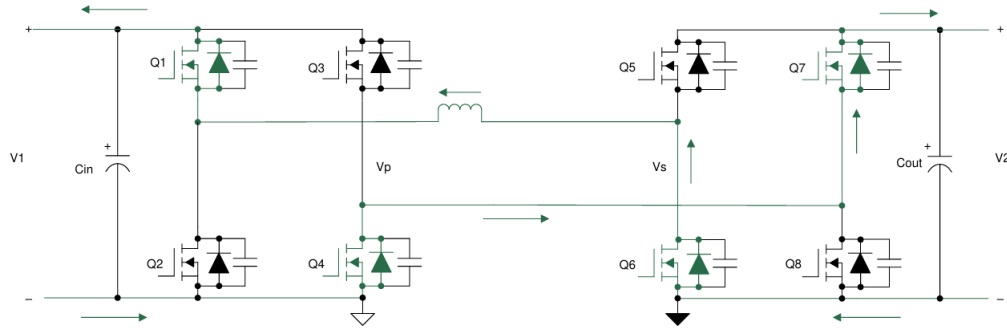


Figure 2.15: Interval 1: Negative Inductor Current, [25].

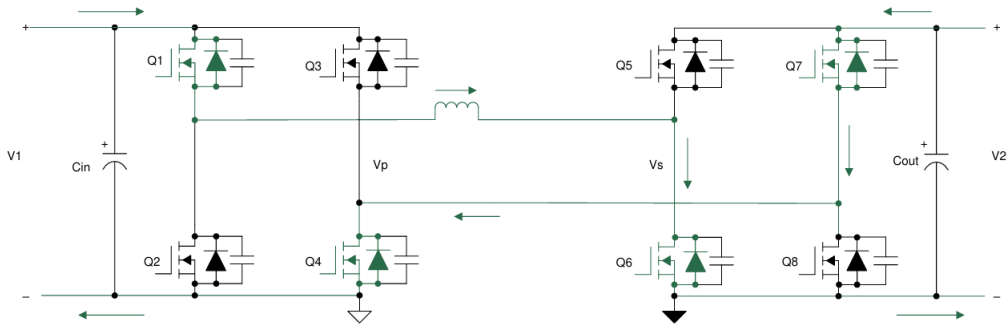


Figure 2.16: Interval 1: Positive Inductor Current, [25].

Throughout this interval, the voltage across the primary winding, represented as  $V_p$ , is equal to  $V_1$ , while the voltage across the secondary winding,  $v_s$ , corresponds to  $nV_2$ . The difference between these voltages is applied across the leakage inductance, influencing the current slope, which can be approximated by:

$$\frac{di_L}{dt} = \frac{V_1 + nV_2}{L_S} \quad (2.10)$$

## Mode II

**Time interval:**  $T_\phi < t < \frac{T_s}{2}$

During the second interval, the inductor current remains positive. The voltage applied to the transformer's primary winding is  $V_1$ , while the secondary winding voltage is  $V_2$ , both maintaining a positive polarity. As a result, the difference between these voltages is imposed across the leakage inductor, influencing the current slope, which can be expressed as:

$$\frac{di_L}{dt} = \frac{V_1 - nV_2}{L_S} \quad (2.11)$$

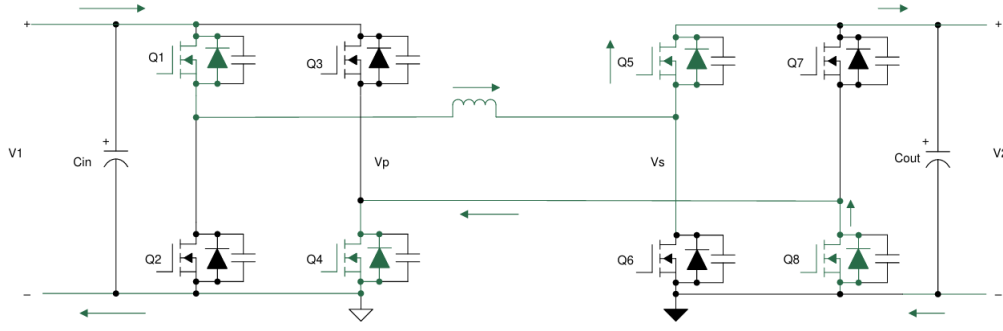


Figure 2.17: Interval 2, [25].

The commutation sequence for this interval is depicted in Figure 2.17.

In this phase, switches  $Q_1$  and  $Q_4$  remain turned on. However, since the secondary voltage reaches  $V_2$  while the inductor current remains positive, switches  $Q_5$  and  $Q_8$  are activated to conduct current. A brief dead-time occurs between the turn-off of  $Q_6$  and  $Q_7$  and the activation of  $Q_5$  and  $Q_6$  and  $Q_7$  and  $Q_8$ . Is during this dead time, that ZVS takes place.

### Mode III

**Time interval:**  $\frac{T_s}{2} < t < \frac{T_s}{2} + T_\phi$

In the third interval, the inductor current begins to decrease from its positive peak towards a negative value, as illustrated in Figure 2.14. In this phase, the voltage across the transformer's primary winding is  $-V_1$ , while the voltage across the secondary remains  $V_2$ . As a result, the difference between these voltages,  $(-V_1 - V_2)$ , is applied across the inductor, causing the current to decrease with a negative slope, which can be expressed as:

$$\frac{di_L}{dt} = -\frac{V_1 + nV_2}{L_S} \quad (2.12)$$

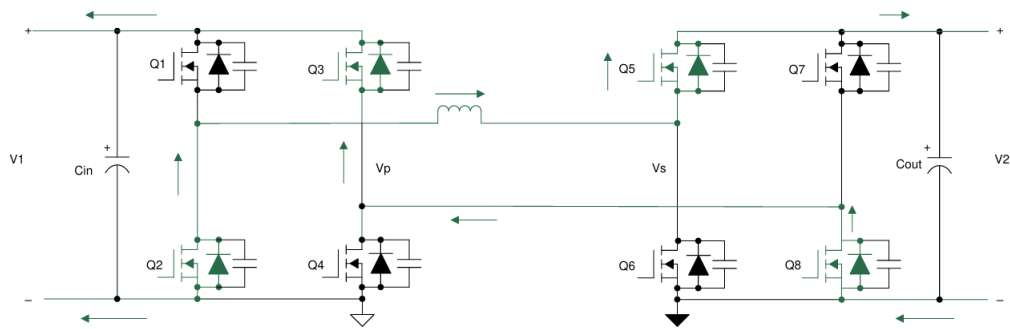


Figure 2.18: Interval 3: Positive Inductor Current, [25].

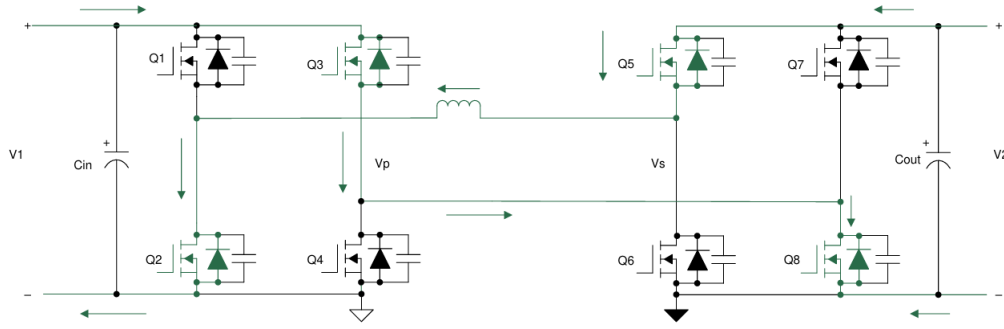


Figure 2.19: Interval 3: Negative Inductor Current, [25].

Throughout this interval, switches  $Q_5$  and  $Q_8$  remain turned on. However, as the primary voltage transitions to  $-V_1$ , switches  $Q_2$  and  $Q_3$  begin conducting current. The conduction behavior for both positive ( $I_L > 0$ ) and negative ( $I_L < 0$ ) inductor currents is illustrated in Figures 2.18 and 2.19.

#### Mode IV

**Time interval:**  $\frac{T_s}{2} + T_\phi < t < T_s$

During the fourth interval, the inductor current continues to decrease in the negative direction. Throughout this phase, the primary voltage remains at  $-V_1$ , while the secondary voltage is  $-V_2$ . The difference between these voltages, given by  $(-V_1 + V_2)$ , is applied across the inductor, resulting in a negative current slope, which can be expressed as:

$$\frac{di_L}{dt} = -\frac{V_1 - V_2}{L_s} \quad (2.13)$$

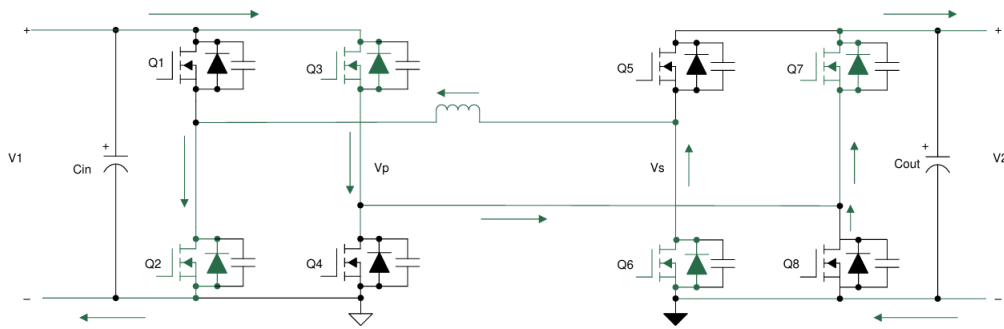


Figure 2.20: Interval 4, [25].

During this interval, switches  $Q_2$  and  $Q_3$  remain in conduction. However, as the secondary voltage transitions to  $-V_2$ , switches  $Q_6$  and  $Q_7$  turn on to facilitate current flow, as depicted in Figure 2.20.

### 2.4.2.2 Zero Voltage Switching (ZVS) and Efficiency Benefits

The DAB converter is a soft-switched topology that enables ZVS under specific conditions. The converter operates by phase-shifting the bridge voltages, allowing energy transfer through the inductor. Above a certain power level, all switching devices can achieve ZVS, particularly when the transformer turns ratio matches the input-to-output voltage ratio. Under these conditions, the resulting current remains mostly in phase with the applied voltages, and the energy transfer inductor maintains zero voltage across it for most of the switching cycle, minimizing conduction losses.

However, at low power levels, ZVS operation becomes challenging due to reduced inductor current, which may not be sufficient to fully discharge device output capacitances before switching transitions. This loss of ZVS at light loads increases switching losses and reduces efficiency. Additional components such as snubber circuits or resonant elements can be introduced to maintain ZVS, but these increase circuit complexity and costs. Switching frequency selection is also crucial—higher frequencies shrink magnetics but may increase light-load switching losses.

### 2.4.2.3 Analysis of Current Stress and Losses

The DAB converter experiences high current stress due to its bidirectional operation and the reliance on energy transfer through an inductor. The current stress depends on the modulation scheme, transformer turns ratio, and power transfer direction. The symmetric circuit structure of the DAB ensures that efficiency is independent of the power flow direction, but certain drawbacks exist.

High RMS currents, particularly on the LV side of the transformer, increase conduction losses. For example, the maximum RMS transformer current on the LV side can reach high values. These high currents contribute to thermal stress, requiring careful thermal management and component sizing.

Additionally, DC-blocking capacitors are introduced in the power stage to prevent transformer core saturation due to unbalanced currents. Such imbalances can arise from mismatched PWM signals, propagation delays in gate drivers, or system asymmetries, particularly during startup and load transients. These capacitors must handle significant RMS currents while providing sufficient capacitance to avoid distorting switch node voltage waveforms.

The use of wide-bandgap semiconductor devices, such as SiC or GaN MOSFETs, allows for higher switching frequencies, reducing magnetic component size and improving thermal conditions. However, excessive output capacitance ( $C_{out}$ ) can lead to increased switching losses at light loads, negatively impacting efficiency.

### 2.4.2.4 Efficiency Implications

The efficiency of the DAB converter is highly dependent on operating conditions, including input voltage variations, load levels, and modulation strategy. Under nominal conditions where the input-to-output voltage ratio matches the transformer turns ratio, conduction losses are minimized,

and the converter operates efficiently. The phase-shift control ensures that the current is mostly in phase with the applied voltages, maximizing power transfer as mentioned before.

However, when the DAB operates over a wide voltage and power range, its efficiency can degrade significantly. If the transformer turns ratio does not match the voltage conversion ratio, the inductor experiences a non-zero voltage across it throughout the switching cycle, leading to continuous current changes and higher RMS current values. This increases conduction losses and may cause one of the bridges to lose ZVS, further increasing power dissipation.

At reduced loads, efficiency drops due to the loss of ZVS and the relatively constant transformer core losses. As the phase shift is reduced to lower power transfer, the available inductor current at switching transitions decreases, preventing lossless voltage transitions. The core loss remains unchanged at a given voltage conversion ratio, contributing to higher relative losses at lower power levels.

To optimize efficiency, the modulation strategy, transformer design, and switching frequency must be carefully selected. The trade-off between heat sink design, transformer size, and efficiency target plays a crucial role in determining the best operating point for the converter. The integration of advanced control techniques and additional resonant components can further enhance performance but introduces added complexity.

### 2.4.3 LLC Resonant Converter

The LLC resonant converter, shown in Figure 2.21, is an advanced isolated DC/DC converter topology that leverages a resonant tank circuit to achieve efficient power conversion. The resonant tank consists of a series inductor ( $L_r$ ), a resonant capacitor ( $C_r$ ), and a magnetizing inductor ( $L_m$ ) in the transformer. The oscillating current in the resonant tank drives energy transfer from the primary side to the secondary side through the transformer. The magnetizing inductor ( $L_m$ ) supports soft-switching by storing energy during each cycle and releasing it to assist in ZVS. This resonance-based energy transfer minimizes losses and enhances efficiency across a wide load range.

This configuration not only enables soft-switching operation but also contributes to high efficiency and reduced stress on components, due to its resonant characteristics, making it well-suited for high-frequency and high-power applications demanding optimized performance, [1, 15, 36, 50].

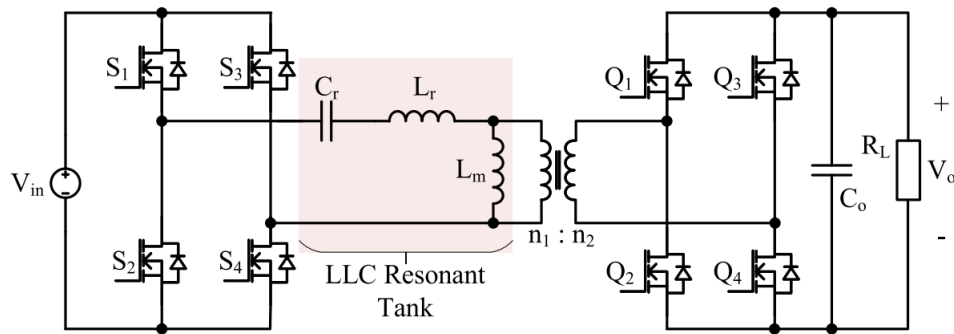


Figure 2.21: LLC Full Bridge Converter, [1].

#### 2.4.3.1 Resonant Tank Analysis

The resonant tank is made up of a resonant capacitor and two inductors: the resonant inductor  $L_r$ , in series with the capacitor and transformer, and the magnetizing inductor  $L_m$ , in parallel, [49]. The tank's role is to filter out the square wave's harmonics, outputting a sine wave of the fundamental switching frequency to the input of the transformer.

The resonant tank gain is derived by analyzing the equivalent resonant circuit depicted in Figure 2.22.

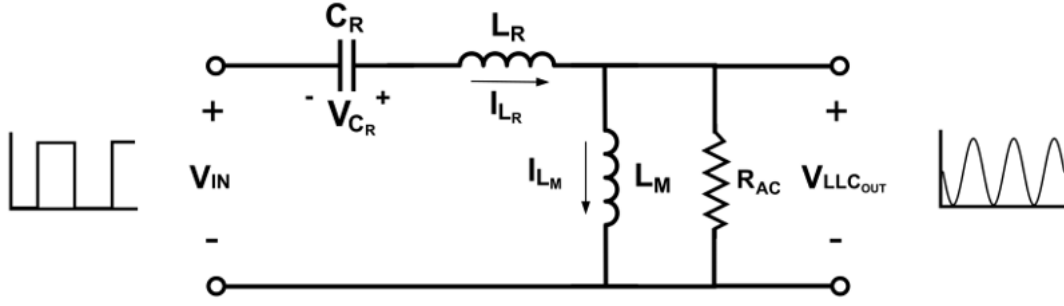


Figure 2.22: Schematic of an LLC Resonant Tank, [41].

The circuit shown in Figure 2.22 can be effectively analyzed and modeled using the FHA method. This approach begins by simplifying the input and output square-wave voltages and currents to their fundamental frequency components, deliberately ignoring all higher-order harmonics.

Additionally, the influence of the output capacitor and the transformer's secondary-side leakage inductance is disregarded to streamline the analysis. The secondary-side voltages and currents are then referred to the primary side, allowing the creation of a unified model. The bipolar square-wave voltage and its associated current on the secondary side are also represented only by their fundamental components. By following these steps, the nonlinear and non-sinusoidal behavior of the original LLC resonant half-bridge converter circuit, as shown in Figure 2.22, is approximated by a linear, sinusoidal model shown in Figure 2.23.

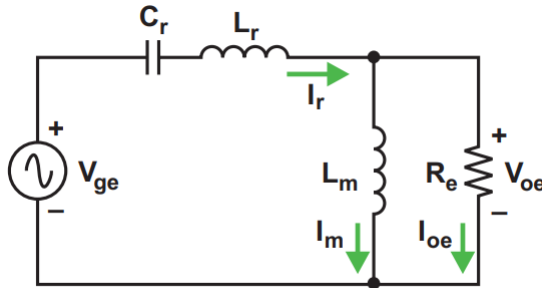


Figure 2.23: Linear Sinusoidal Circuit, [21].

In this linear model, both the input voltage ( $V_{ge}$ ) and output voltage ( $V_{oe}$ ) are sinusoidal and share the same frequency, derived from the fundamental component of the original switching waveform. This FHA-based circuit model provides a simplified yet accurate foundation for deriving the voltage-transfer function and serves as a critical tool in the design and analysis of resonant converters.

### 2.4.4 Relationship of Electrical Variables

On the input side, the fundamental voltage of the square-wave voltage ( $V_{sq}$ ) is;

$$v_{ge}(t) = \frac{2}{\pi} \times V_{DC} \times \sin(2\pi f_{sw}t) \quad (2.14)$$

And its RMS value is,

$$V_{ge} = \frac{\sqrt{2}}{\pi} \times V_{DC} \quad (2.15)$$

On the output side, since  $V_{so}$  is approximated as a square wave, the fundamental voltage is:

$$v_{oe}(t) = \frac{4}{\pi} \times n \times V_o \times \sin(2\pi f_{sw}t - \phi_V) \quad (2.16)$$

where  $\phi_V$  is the phase angle between  $V_{oe}$  and  $V_{ge}$ , and the RMS output voltage is:

$$V_{oe} = \frac{2\sqrt{2}}{\pi} \times n \times V_o \quad (2.17)$$

The fundamental component of current corresponding to  $V_{oe}$  and  $I_{oe}$  is:

$$i_{oe}(t) = \frac{\pi}{2} \times \frac{1}{n} I_o \times \sin(2\pi f_{sw}t - \phi_i) \quad (2.18)$$

where  $\phi_i$  is the phase angle between  $i_{oe}$  and  $V_{oe}$ , and the RMS output current is:

$$I_{oe} = \frac{\pi}{2\sqrt{2}} \times \frac{1}{n} \times I_o \quad (2.19)$$

Then the AC equivalent load resistance,  $R_e$ , can be calculated as:

$$R_e = \frac{V_{oe}}{I_{oe}} = \frac{8n^2}{\pi^2} \times \frac{V_o}{I_o} = \frac{8n^2}{\pi^2} \times R_L \quad (2.20)$$

The input-output transfer ratio of the FHA-based circuit  $T_{FHA}$  can be expressed as

$$T_{FHA} = \frac{V_{op}}{V_f} = \frac{2nV_o}{\eta V_{in}} \quad (2.21)$$

and  $T_{FHA}(s)$  can be derived by the Laplace transformation in the  $s$ -domain as

$$T_{FHA}(s) = \left| \frac{sL_m \parallel R_{ac}}{sL_r + (sC_r)^{-1} + sL_m \parallel R_{ac}} \right| \quad (2.22)$$

by expanding the parallel/series terms, the FHA gain becomes:

$$T_{FHA}(s) = \frac{C_r L_m R_{ac} s^2}{C_r L_r L_m s^3 + C_r R_{ac} (L_r + L_m) s^2 + L_m s + R_{ac}}. \quad (2.23)$$

This reveals a third-order plant with two zeros at the origin and three poles governed by  $L_r$ ,  $L_m$ ,  $C_r$ , and the AC load  $R_{ac}$ . Physically:

- The complex pole pair creates the resonant hump.
- The real pole ( $\approx$  high-frequency roll-off) limits crossover.
- Lower  $R_{ac}$  (heavier load  $\Rightarrow$  higher  $Q_e$ ) reduces damping, sharpening the hump; higher  $R_{ac}$  damps it.

Since the circuit in Figure 2.23 is a single-frequency, sinusoidal AC circuit, the calculations can be made in the same way as for all sinusoidal circuits. The angular frequency is:

$$\omega = \omega_{sw} = 2\pi f_{sw} \quad (2.24)$$

The capacitive and inductive reactances of  $C_r$ ,  $L_r$ , and  $L_m$ , respectively, are:

$$X_{C_r} = \frac{1}{\omega C_r}, \quad X_{L_r} = \omega L_r, \quad X_{L_m} = \omega L_m \quad (2.25)$$

Where,

$$\omega_m = (L_m C_r)^{-1/2}, \quad \omega_{r1} = 2\pi f_{r1}, \quad \omega_{r2} = 2\pi f_{r2} \quad (2.26)$$

now, the Equation 2.22 can be transposed to the frequency domain by the equivalent  $s = j\omega$  as

$$T_{FHA}(\omega) = \left| \frac{-\frac{\omega^2}{\omega_m^2} R_{ac}}{\left(1 - \frac{\omega^2}{\omega_{r2}^2}\right) R_{ac} - \frac{\omega^2}{\omega_m^2} R_{ac} + j\omega \left(1 - \frac{\omega^2}{\omega_{r1}^2}\right) L_m} \right| \quad (2.27)$$

Higher gain of  $T_{FHA}$  is obtained as the quality factor decreases, which means that the load decreases. Therefore, the turn ratio of the transformer should be determined under the full load condition.

At the no-load condition,  $R_{ac} \rightarrow \infty$ , the input-output ratio simplifies to a simple impedance divider as

$$\frac{V_o}{V_{in}} = \frac{\eta}{2n} \cdot \frac{L_m}{L_m + L_r - (\omega^2 C_r)^{-1}} = \frac{\eta}{2n} \cdot \frac{L_m}{L_m + L_r}. \quad (2.28)$$

The primary-side RMS load current  $I_{oe}$ :

$$I_{oe} = \frac{\pi}{2\sqrt{2}} \cdot \frac{I_o}{n} \quad (2.29)$$

The RMS magnetizing current is:

$$I_m = \frac{V_{oe}}{\omega L_m} = \frac{2\sqrt{2}}{\pi} \cdot \frac{n \cdot V_o}{\omega L_m} \quad (2.30)$$

The circulating current in the series resonant circuit is:

$$I_r = \sqrt{I_m^2 + I_{oe}^2} \quad (2.31)$$

The secondary-side RMS load current  $I_{oe\_s}$ , that is the current referred from the primary-side  $I_{oe}$  to the secondary side:

$$I_{oe\_s} = n \cdot I_{oe} \quad (2.32)$$

Due to the center-tapped configuration of the transformer's secondary side, the output current is evenly divided between the two secondary windings. As a result, the current through each winding can be calculated individually as:

$$I_{sw} = \frac{\sqrt{2} \cdot I_{oe\_s}}{2} \quad (2.33)$$

The corresponding half-wave average current for each winding is:

$$I_{sav} = \frac{\sqrt{2} \cdot I_{oe\_s}}{\pi} \quad (2.34)$$

#### 2.4.4.1 Voltage Gain Characteristics

Using the Fundamental Element Simplification (FES) method, it's possible to get the dc voltage gain  $G_{dc}$ , [20], of the LLC resonant converter as shown in Equations (2.35), (2.36) below:

$$G_{dc} = \frac{1}{2} \cdot K(Q, m, F_x) \cdot \frac{N_s}{N_p} = \frac{1}{2n} \cdot K(Q, m, F_x). \quad (2.35)$$

$$K(Q, m, F_x) = \left| \frac{V_{o\_ac}(s)}{V_{in\_ac}(s)} \right| = \frac{F_x^2(m-1)}{\sqrt{(m \cdot F_x^2 - 1)^2 + F_x^2 \cdot (F_x^2 - 1)^2 \cdot (m-1)^2 \cdot Q^2}} \quad (2.36)$$

Where,

$$Q_e = \frac{\sqrt{L_r/C_r}}{R_{ac}} \quad (2.37)$$

$$C_r = \frac{1}{2\pi \cdot Q_e \cdot f_r \cdot R_e} \quad (2.38)$$

$$L_r = \frac{1}{(2\pi f_r)^2 C_r} \quad (2.39)$$

$$L_m = L_n \cdot L_r \quad (2.40)$$

$$R_{ac} = \frac{8}{\pi^2} \cdot \frac{N_p^2}{N_s^2} \cdot R_o \quad (2.41)$$

$$F_x = \frac{f_s}{f_r} \quad (2.42)$$

$$f_r = \frac{1}{2\pi\sqrt{L_r \cdot C_r}} \quad (2.43)$$

$$f_p = \frac{1}{2\pi} \sqrt{\frac{L_r + L_m}{L_r L_m C_r}} \quad (2.44)$$

$$m = L_n = \frac{L_m}{L_r} \quad (2.45)$$

The gain of the resonant tank, denoted as  $K$ , can be plotted against the normalized switching frequency for varying values of the quality factor  $Q$ , while keeping a fixed value for the ratio  $m$ . An example of such a plot, with  $m = 6$ , is shown in Figure 2.24. The specific choice of  $m$  will be addressed in a later section of this document.

As illustrated in Figure 2.24, the lower  $Q$  curves correspond to light load conditions, whereas higher  $Q$  curves indicate heavier load operations. Notably, all  $Q$  curves, representing different load scenarios, intersect at the resonant frequency ( $F_x = 1$ , or  $f_s = f_r$ ), where the gain equals unity.

Additionally, Figure 2.24 reveals that each gain curve exhibits a peak, which demarcates the transition between inductive and capacitive impedance regions of the resonant tank. These regions can be clearly identified in the plot, with the inductive and capacitive operation areas shaded for clarity. This distinction is critical, as the design aims to ensure inductive operation across the full range of input voltages and load currents, avoiding operation within the capacitive region entirely, since in this region the converter's gain behavior becomes much sharper and more difficult to control, with the gain–frequency curves exhibiting a steeper gradient that makes regulation across the frequency spectrum considerably more challenging.

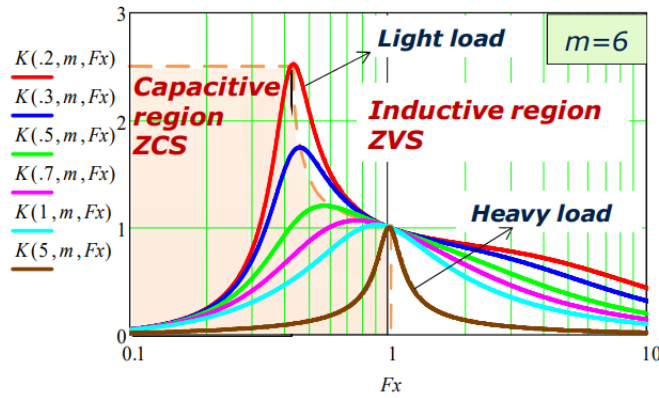


Figure 2.24: Voltage Gain within Frequency Spectrum, [49].

In Figure 2.24, the modes of operation of the LLC converter in the range of frequency, which represents two operation modes that depend on the load and frequency of operation.

In the capacitive region, the current is lagging the voltage. On the primary side, the current on the transit diode FET will have a hard commutation.

In the inductive region, the current is leading the voltage, and that is the fact that causes ZVS operation before turning on the FET gate.

#### 2.4.4.2 Modes of Operation

As the LLC network gain is modulated by frequency, the converter operates in three distinct modes based on input voltage and load current conditions [48], as illustrated in Figure 2.25.

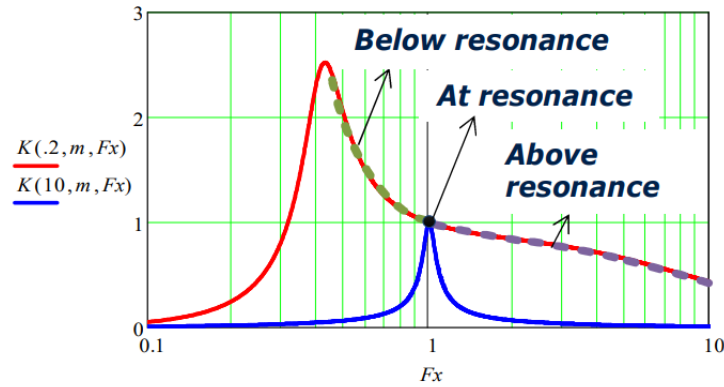


Figure 2.25: Operation within Frequency Spectrum, [48].

#### Key waveforms

The following information describes the behavior of the converter in each operating mode and shows its key waveforms.

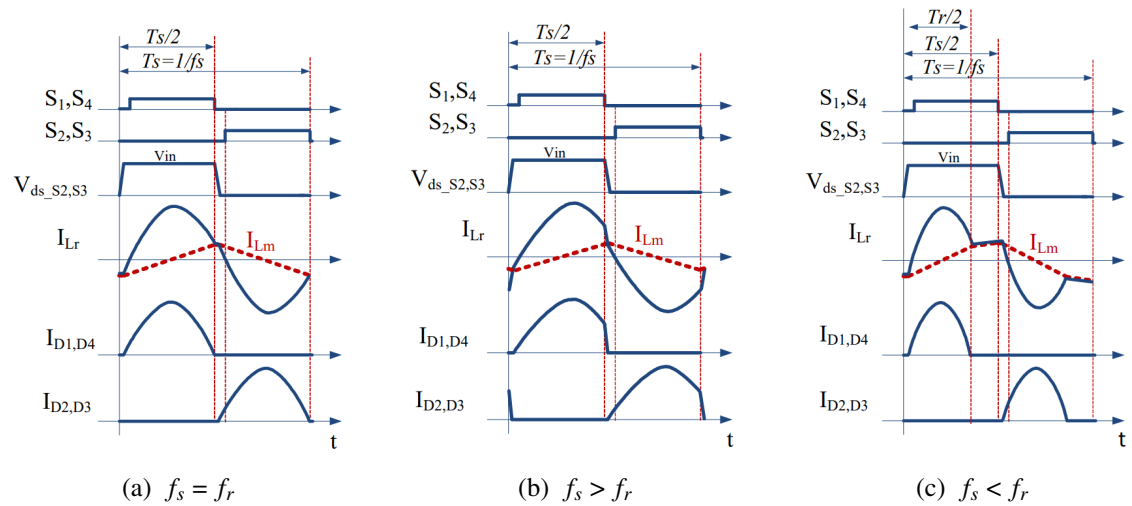


Figure 2.26: LLC converter key waveforms, [49]

### Operation at Resonant Frequency ( $f_s = f_r$ )

At the resonant frequency, Figure 2.26a, each half of the switching cycle completes a full power delivery operation. The resonant half-cycle aligns perfectly within the switching period, ensuring optimal energy transfer.

- At the end of each switching half-cycle, the resonant inductor current  $I_{L_r}$  reaches the magnetizing current  $I_{L_m}$ , leading to zero current at the rectifier.
- The resonant tank operates with unity gain, meaning the voltage gain remains approximately 1.
- This mode provides optimal efficiency and performance, making it the preferred operating condition when the input and output voltages are nominal.

### Operation Above Resonant Frequency ( $f_s > f_r$ )

When the switching frequency exceeds the resonant frequency, Figure 2.26b, the power delivery operation is interrupted before completion due to the earlier activation of the opposite switching pair.

- The resonant half-cycle is not fully completed, leading to increased turn-off losses in the primary-side MOSFETs.
- The secondary-side rectifier diodes experience hard commutation, increasing stress and losses.
- This mode typically occurs at higher input voltages, where the converter behaves as a buck converter to step down voltage.

### Operation Below Resonant Frequency ( $f_s < f_r$ )

At switching frequencies lower than the resonant frequency, Figure 2.26c, freewheeling operation occurs after the power delivery phase.

- When the resonant half-cycle completes,  $I_{L_r}$  reaches the magnetizing current  $I_{L_m}$ , triggering freewheeling at the end of the switching half-cycle.
- During freewheeling, circulating energy increases conduction losses on the primary side.
- This mode is used at lower input voltages, where the converter operates as a boost converter to step up voltage.

Despite the three operating modes discussed, the converter undergoes only two fundamental operations within each switching cycle. Each of the previously mentioned modes may incorporate one or both of these operations.

### Power Delivery Operation

Power delivery occurs twice per switching cycle. In the first half of the cycle, the resonant tank is excited by a positive voltage, causing the current to resonate in the positive direction. The equivalent circuit for this state is depicted in Figure 2.27a. In the second half of the cycle, the resonant tank is excited by a negative voltage, resulting in current resonance in the negative direction, as illustrated in Figure 2.27b.

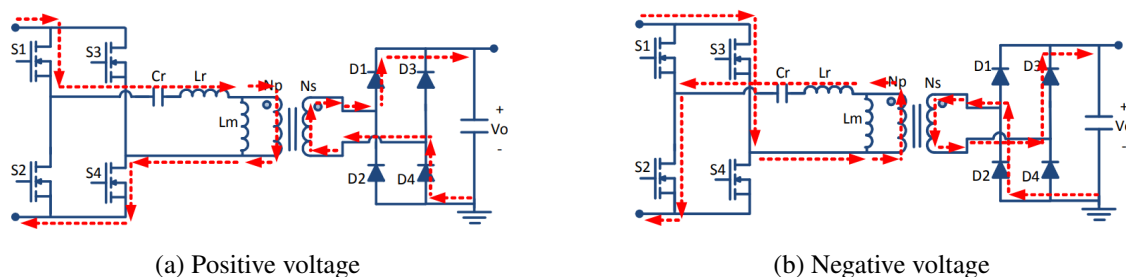


Figure 2.27: Power delivery equivalent circuits, [49]

During these power delivery phases, the magnetizing inductor voltage corresponds to the positive or negative reflected output voltage, while the magnetizing current alternates between charging and discharging. The difference between the resonant current and the magnetizing current flows through the transformer and rectifier to the secondary side, facilitating power transfer to the load.

### Freewheeling Operation

The freewheeling operation occurs after the power delivery phase, but only if the resonant current reaches the transformer magnetizing current. This condition is met when the switching frequency  $f_s$  is lower than the resonant frequency  $f_r$ , causing the transformer secondary current to drop to zero and disconnect the secondary-side rectifier. As a result, the magnetizing inductor enters resonance with the resonant inductor and capacitor.

The frequency of this secondary resonance is lower than the original resonant frequency  $f_r$ , particularly when the magnetizing inductance  $L_m$  is significantly larger than the resonant inductance  $L_r$ . Under these conditions, the primary current during freewheeling undergoes minimal variation and can be approximated as constant for simplicity.

The equivalent circuits for the freewheeling operation in both halves of the switching cycle are illustrated in Figure 2.28a and Figure 2.28b.

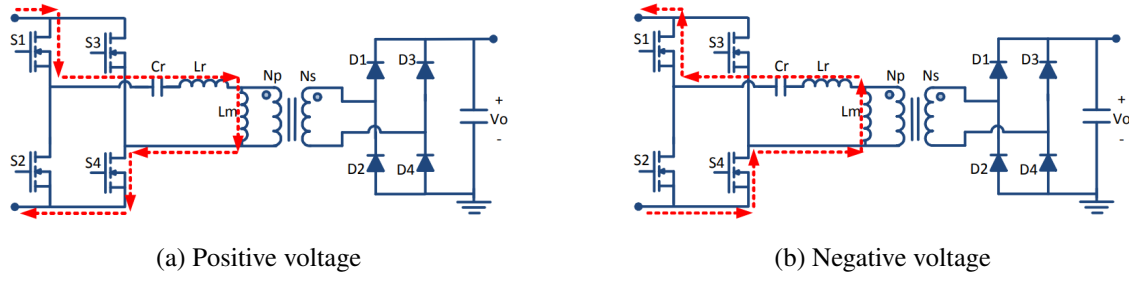
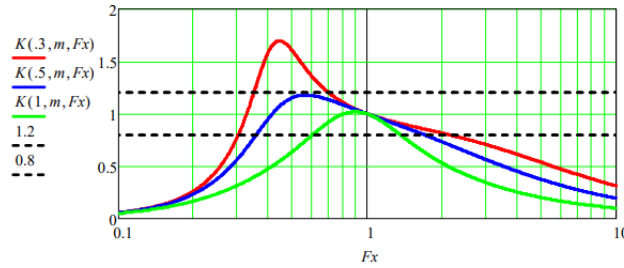


Figure 2.28: Freewheeling equivalent circuits, [49]

#### 2.4.4.3 Quality Factor (Q) Analysis

The quality factor depends on the load current. Heavy load conditions operate at high  $Q$  values, while lighter loads have lower  $Q$  values. It is important to set a value for the  $Q_{\max}$  associated with the maximum load point.

To illustrate the effect of the  $Q$  value on voltage regulation, Figure 2.29 shows an example voltage gain plot for different  $Q$  values. Let's assume that the resonant tank gain is required to range from 0.8 to 1.2 for example. A plot of different curves where it will vary the quality factor and maintain constant the ratio value.

Figure 2.29: Constant  $m$  value, varying  $k$ , [49].

The low  $Q$  value curve ( $Q = 0.3$ ) achieves a higher boost gain but is less sensitive to frequency modulation in the "above resonance" region ( $f_s > f_r$ ). As a result, the switching frequency must increase significantly to reach the minimum voltage gain ( $K = 0.8$ ), leading to additional switching losses. In contrast, the higher  $Q$  value curve ( $Q = 1$ ) can achieve the minimum gain ( $K = 0.8$ ) with a smaller increase in switching frequency but is unable to reach the maximum gain ( $K = 1.2$ ).

Thus, a moderate  $Q$  value of approximately 0.5 appears to satisfy the voltage gain requirements in this particular case.

In conclusion, while adjusting the  $Q$  value can help achieve a higher maximum gain, it also increases the frequency modulation range.

#### 2.4.4.4 Ratio Value (m) Analysis

The parameter  $m$  is static and must be optimized at the beginning of the design process, [26]. Therefore, it is essential to understand the impact of the  $m$  ratio on converter operation. To illus-

trate this effect, Figure 2.30 shows resonant tank gain plots for different  $m$  values ( $m = 3, 6$ , and  $12$ ).

It is evident that lower values of  $m$  can achieve higher boost gain and a narrower frequency modulation range. This narrower range allows for more flexible control and regulation, which is especially advantageous in applications requiring a wide input voltage range. However, lower  $m$  values for the same quality factor  $Q$  and resonant frequency  $f_r$  result in a smaller magnetizing inductance ( $L_m$ ), leading to higher peak-to-peak magnetizing current ripple. This increased ripple contributes to greater circulating energy and conduction losses.

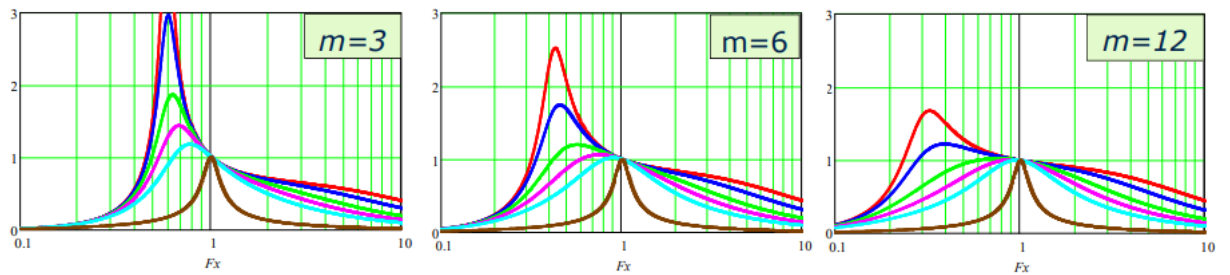


Figure 2.30: Constant  $k$  value, varying  $m$ , [49].

#### Low $m$ value

- Higher boost gain
- Narrower frequency range
- More flexible regulation

#### High $m$ value

- Higher magnetizing inductance
- Lower magnetizing circulating current
- Higher efficiency

#### 2.4.4.5 Frequency Range

The operating frequency range is chosen based on the desired gain and efficiency trade-offs, ensuring sufficient margin for ZVS and stable operation.

When studying the resonant converter, it is convenient to reduce the architecture to a passive element arrangement such as presented in Figure 2.31 and 2.32. The high-voltage square signal is replaced by its fundamental content thanks to the first harmonic approximation (the so-called FHA in the literature): because we operate a tuned LC filter, all harmonics can be considered rejected and only the fundamental passes through. Of course, this statement holds as long the controller drives the resonating work in the vicinity of its resonant frequency. Figure 2 offers such

a simplified representation of the resonant cell, actually pointing out a series impedance ( $L_s$  and  $C_s$ ) with a parallel impedance ( $L_m$  and the reflected load).

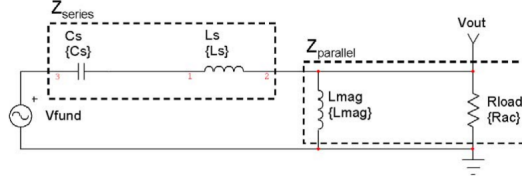


Figure 2.31:  $Z_{series}$  and  $Z_{parallel}$  Representation, [43].

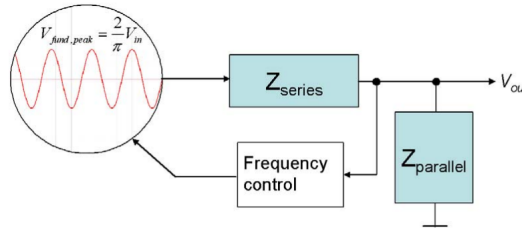


Figure 2.32: Impedance Representation, [43].

Another point of analysis is the frequency that depends on the load condition.

Depending on the loading, the network resonant frequency varies between two different values:

- $R_L = 0$ , short-circuit,  $L_m$  disappears and  $Z_{series}$  becomes a short. The series resonant point for  $Z_{series}$  is thus:

$$f_{\max} = f_r = \frac{1}{2\pi\sqrt{L_r \cdot C_r}} \quad (2.46)$$

At  $F_{sw} = F_s$ ,  $Z_{series}$  becomes short and the ac transfer function drops to 1 or 0 dB.

- $R_L = \text{infinite}$ , light or no load condition,  $L_m$  appears in series with  $L_s$  and the whole network resonates to:

$$f_{\min} = \frac{1}{2\pi\sqrt{L_r + L_m} \cdot C_r} \quad (2.47)$$

- $0 < R_L < \text{infinite}$ , the resonance which combines  $L_m$  and  $L_s$ , shifts depending on the total quality coefficient.

Since the LLC converter is designed to operate in the inductive region, it is necessary to define its frequency range across the entire spectrum of operating conditions. Figure 2.33 below illustrates this region, highlighting the converter's operating frequency range, including its minimum and maximum limits.

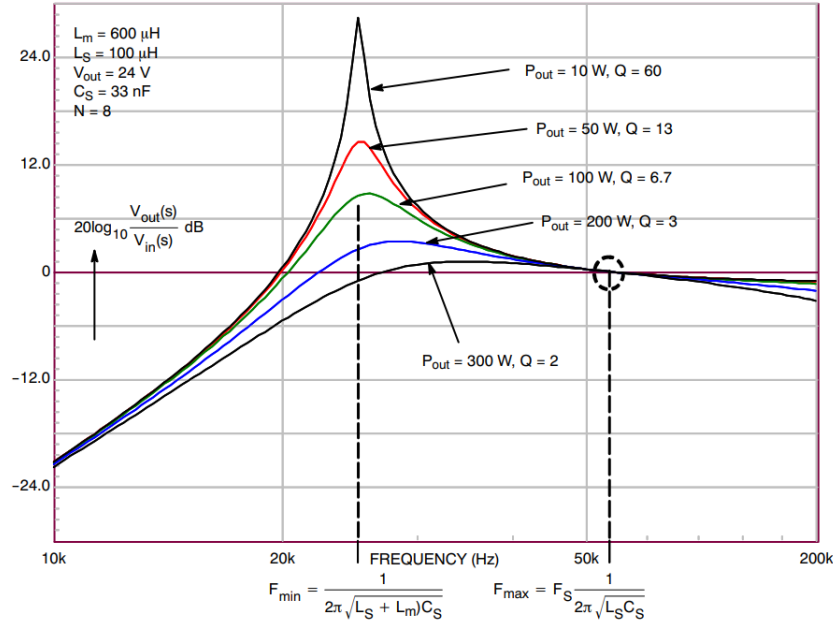


Figure 2.33: The AC Response of Figure 2.32 Circuit with Various Load Conditions, [43].

The example above, as expected, shows that by having the goal of operation well defined, it can establish the maximum and minimum frequency.

#### 2.4.4.6 Analysis of Current Stress and Losses

The LLC resonant converter is known for its high efficiency across varying load conditions, attributed to its resonance-based operation and soft-switching capability. Assuming that the LLC is designed to work at a resonant frequency on its full load capability:

**Full-Load Efficiency:** At full load, the converter operates near the unit gain, at the resonant frequency, where circulating currents are minimal. This reduces conduction losses in both the primary and secondary circuits. ZVS on the primary side and ZCS on the secondary side ensure efficient operation, reducing component stress and heat dissipation.

Synchronous rectification on the secondary side further improves efficiency by lowering conduction losses compared to diode-based rectification.

**Light-Load Efficiency:** Under light loads, the converter operates at a higher switching frequency to maintain voltage regulation. While ZVS is still achievable, the magnetizing current and circulating currents become more significant, leading to increased conduction losses. Techniques like burst mode or adaptive control strategies are often employed to minimize light-load inefficiencies by limiting magnetizing current and reducing switching frequency. These methods ensure optimized performance without sacrificing control stability.

#### **2.4.4.7 Efficiency Implications**

The LLC resonant converter achieves high efficiency through soft-switching techniques like ZVS on the primary side and ZCS on the secondary side, minimizing switching losses and heat generation. At full load, the converter operates near its resonant frequency, reducing circulating currents and conduction losses. However, under light-load conditions, increased magnetizing and circulating currents can degrade efficiency. Advanced control strategies, such as burst mode operation and adaptive switching frequency modulation, are essential to mitigate light-load losses and maintain high efficiency across a wide operating range.

## 2.5 Comparative Analysis

### 2.5.1 Efficiency Across Operating Ranges

The efficiency of LLC, PSFB, and DAB converters varies depending on load conditions, soft-switching capabilities, and energy transfer mechanisms.

At full load, the LLC converter achieves the highest efficiency due to resonance-based energy transfer and soft-switching, minimizing conduction and switching losses. The PSFB converter also maintains high efficiency by utilizing ZVS to reduce switching losses, but its dependence on leakage inductance energy limits performance at extreme operating points. The DAB converter is highly efficient at medium-to-heavy loads, leveraging phase-shift modulation to minimize conduction losses.

At light loads, however, efficiency trends diverge. The LLC converter's efficiency drops due to increased magnetizing currents from higher switching frequencies. The PSFB converter struggles to maintain ZVS on the lagging leg, leading to increased switching losses. Similarly, the DAB converter suffers from circulating currents, which elevate conduction losses and degrade efficiency.

### 2.5.2 Power Density and Thermal Management

Power density and thermal performance are critical factors in high-efficiency applications, especially where size and thermal dissipation constraints exist.

The LLC converter excels in power density, as its resonance-based operation reduces the size of passive components like transformers and inductors. Soft-switching also minimizes heat dissipation, making thermal management easier. The PSFB converter, in contrast, requires larger magnetic components, such as shim inductors, to maintain ZVS, reducing its power density. Its thermal management also becomes challenging due to circulating currents at light loads, increasing conduction losses.

The DAB converter, with its symmetrical structure and high-frequency operation, allows for a compact layout with minimal parasitic inductance, achieving high power density. However, circulating currents in non-power transfer phases generate additional thermal stress, requiring more complex thermal management strategies.

### 2.5.3 Control Complexity and Implementation Difficulty

Control complexity varies significantly among LLC, PSFB, and DAB converters due to differences in modulation strategies and control requirements.

The LLC converter requires variable-frequency control, making it more complex to regulate, as the controller must continuously adjust the frequency to maintain operation in the inductive region for ZVS. This requires a sophisticated controller and careful design of the resonant tank ( $C_r, L_r, L_m$ ).

The PSFB converter is simpler in terms of control, as it uses a fixed switching frequency with phase-shift modulation to regulate output voltage, which simplifies synchronization and control implementation.

The DAB converter, however, is the most complex in terms of control. Since bidirectional power flow is achieved through precise phase-shift modulation, the timing and synchronization between primary and secondary bridges must be carefully managed. Additionally, optimization for different load conditions further increases control difficulty.

## 2.6 Suitability for Formula Student-Specific Constraints

Formula Student electric vehicles demand compact, efficient, and reliable DC/DC converters that operate under strict weight, space, thermal, and dynamic performance constraints. This section compares the suitability of LLC, PSFB, and DAB converters in these aspects.

### 2.6.1 Weight, Space, and Power Density

Compactness and lightweight design are critical for Formula Student prototypes.

- The LLC converter achieves high power density due to resonance-based energy transfer, allowing for smaller magnetic components and lighter designs [35, 37].
- The PSFB converter requires a shim inductor and a larger transformer, making it bulkier and heavier than LLC [35].
- Although the DAB converter features a symmetrical architecture, in terms of compactness and lightweight design, it tends to be less advantageous, as it requires a large number of semiconductor devices and corresponding cooling components for each, resulting in a bulkier overall implementation, [54].

### 2.6.2 Efficiency for Varying Loads

Formula Student endurance events demand high efficiency across different loads.

At full load, all three converters perform well:

- LLC achieves the highest efficiency, leveraging soft-switching (ZVS and ZCS) [37].
- PSFB follows closely, benefiting from ZVS on the primary side [11].
- DAB operates efficiently with optimized phase-shift modulation [35].

At light loads, efficiency trends diverge:

- LLC efficiency drops due to higher magnetizing current, but can be mitigated using more sophisticated control techniques.
- PSFB efficiency declines, as ZVS on the lagging leg is lost, increasing switching losses.

- DAB efficiency is impacted by circulating currents, leading to higher conduction losses [11, 35].

### 2.6.3 Thermal Management and Cooling Requirements

Thermal management is critical due to space constraints and limited cooling capacity in Formula Student vehicles.

- The LLC converter has minimal thermal stress due to soft-switching, simplifying cooling system design.
- The PSFB converter suffers from heat build-up at light loads, requiring dead-time optimization to mitigate losses.
- The DAB converter, while efficient at high loads, has higher conduction losses at light loads, which may necessitate additional cooling solutions.

### 2.6.4 Robustness and Reliability

Although the LLC converter offers high efficiency, it is sensitive to variations in component values and demands accurate tuning to maintain stable operation.

The PSFB converter, with its fixed switching frequency, demonstrates greater robustness against load fluctuations and maintains reliable performance even under demanding conditions.

The DAB converter provides excellent adaptability, but its inherently complex control strategy can present stability challenges, particularly in dynamically changing environments.

### 2.6.5 Control Complexity and Implementation

The LLC converter depends heavily on precise frequency tuning and careful optimization of the resonant tank, both of which add to the design and control complexity. In contrast, the PSFB converter is simpler to implement, as it uses fixed-frequency phase-shift modulation and benefits from the availability of mature, off-the-shelf controller ICs. The DAB converter, renowned for its bidirectional power flow capability, requires a more sophisticated control scheme that involves precise phase-shift synchronization. While this offers high adaptability to dynamic load conditions, such complexity is unnecessary for the FS DC/DC converter application, where only unidirectional operation, stepping down voltage, and delivering power to the load are required. In this context, implementing an advanced bidirectional control system would introduce avoidable complexity without practical benefit.

2.7 Summary

The table 2.1 presents a comprehensive comparison of the LLC, PSFB, and DAB topologies based on key metrics such as efficiency, power density, thermal management, and suitability for Formula Student constraints. Each criterion highlights the strengths and limitations of the respective converters, providing a detailed evaluation to assist in identifying the most suitable topology for the given application.

Table 2.1: Comparison of LLC, PSFB, and DAB Converters Across Key Metrics.

| Metric                      | LLC                                                                   | PSFB                                                                        | DAB                                                                   |
|-----------------------------|-----------------------------------------------------------------------|-----------------------------------------------------------------------------|-----------------------------------------------------------------------|
| Efficiency                  | High (~96–97%) at full load; drops (~90–92%) at light load            | Consistent at medium-to-high loads (~94–96%); drops (~85–88%) at light load | High (~95–97%) at medium-to-high loads; drops (~88–90%) at light load |
|                             | Light-load drops due to magnetizing/circulating currents or ZVS loss. |                                                                             |                                                                       |
| Power Density               | High; compact resonant tank                                           | Moderate; larger components                                                 | High; symmetrical design                                              |
| Thermal Management          | Simplified at full load; light-load stress                            | Requires advanced cooling for losses                                        | Simplified at high loads; cooling for light-load losses               |
| Control Complexity          | High; variable-frequency tuning                                       | Moderate; dead-time tuning                                                  | High; phase-shift modulation                                          |
| Implementation              | Iterative resonant tank design                                        | Standard controllers; transformer design                                    | Complex bidirectional design                                          |
|                             | Compact/Modular designs vary by topology.                             |                                                                             |                                                                       |
| Cost                        | Moderate; precise components                                          | Low; simpler components                                                     | High; advanced control                                                |
| Formula Student Suitability | Compact, efficient; robust control needed                             | Reliable; larger size challenging                                           | Compact; complex control requires expertise                           |

2.7.1 Final Outcome

The LLC resonant converter was selected as the optimal topology for the Formula Student electric vehicle application due to its ability to meet the project’s stringent requirements for high efficiency, compact design, and reliable performance. Its resonance-based energy transfer minimizes switching losses, enabling high efficiency across a wide range of operating conditions. At full load, the LLC converter achieves efficiencies exceeding 96%, making it particularly well-suited for the 1 kW power demand of the low-voltage system. Moreover, its ability to maintain ZVS on

the primary side and ZCS on the secondary side significantly reduces switching losses and heat generation, thereby simplifying the overall thermal management.

Among the variations of the LLC topology, the configuration adopted for this project was the half-bridge LLC resonant converter with a center-tapped secondary, Figure 2.34.

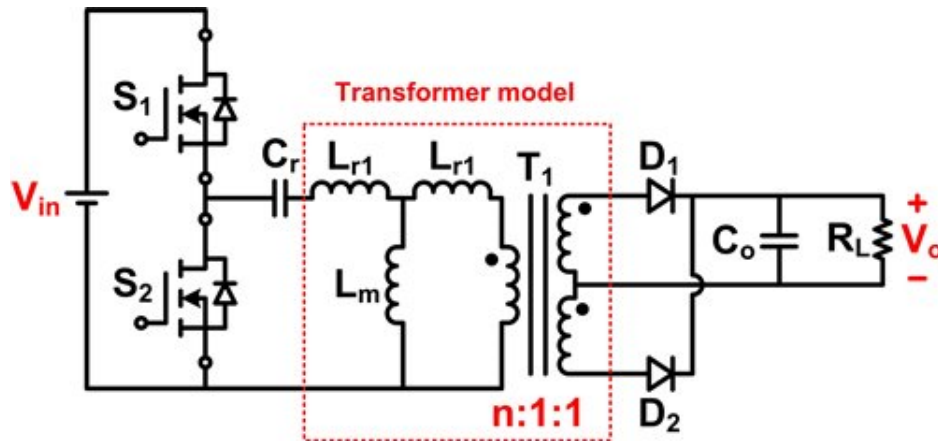


Figure 2.34: LLC Resonant Half-bridge Center-tap Configuration, [30].

This choice was primarily driven by the cost and complexity trade-offs. While a full-bridge configuration could offer higher power-handling capability, it would require twice the number of semiconductor devices and corresponding gate drivers with the respective control, leading to increased cost, size, complexity, and cooling requirements. Given the design constraints of the Formula Student application, specifically a 400 V to 600 V input bus and a 1 kW power level, the half-bridge configuration provides a more efficient and cost-effective solution, fully capable of meeting the required performance without unnecessary component overhead.

Operating at relatively high switching frequencies, the LLC converter enables the use of smaller transformers and passive components, contributing to a compact and lightweight design that aligns well with the limited space available in Formula Student vehicles.

In summary, the half-bridge center-tap LLC resonant converter represents a well-balanced compromise between performance, efficiency, cost, and compactness. While its design demands careful tuning of the resonant tank and a robust control strategy, these challenges are outweighed by its ability to deliver stable, efficient, and compact power conversion suitable for the high-voltage to low-voltage conversion required in this project.

## Chapter 3

# Design Methodology and Parameter Optimization

The parameter design of the LLC resonant converter is essential to achieve high efficiency, soft switching, and reliable operation. This chapter presents the complete design process of the LLC resonant converter developed for this project. The objective is to detail the reasoning, methodology, and equations used to determine the key parameters and component selections that ensure the converter meets the electrical and functional requirements established for the Formula Student application.

The chapter begins with the parameter design of the LLC converter, where the transformer turns ratio, converter gain characteristics, and resonant tank parameters, such as  $L_r$ ,  $L_m$ , and  $C_r$  are defined. The relationships between these parameters are analyzed to achieve the desired voltage conversion ratio, efficiency, and soft-switching operation.

Next, the resonant circuit design verification is performed, validating the chosen component values against the expected operating points. The transformer and semiconductor device selections are then discussed in detail, focusing on the electrical, thermal, and switching performance requirements of both MOSFETs and diodes.

Finally, the design considerations for ZVS, rectifier stage, and output filter are presented, ensuring that the converter delivers a stable 24 V output with minimal ripple and high overall efficiency.

### 3.1 Parameter Design of LLC Converter

The converter characteristics for its design are listed below:

- Input voltage: 400 to 600 VDC
- Rated output power: 1 kW
- Output voltage: 24 VDC

- Rated output current: 42 A
- Maximum peak-to-peak output voltage ripple: 240 mV

By defining the parameters listed above, the process of sizing and dimensioning the parameters of the LLC converter can begin according to the flow chart in Figure 3.1.

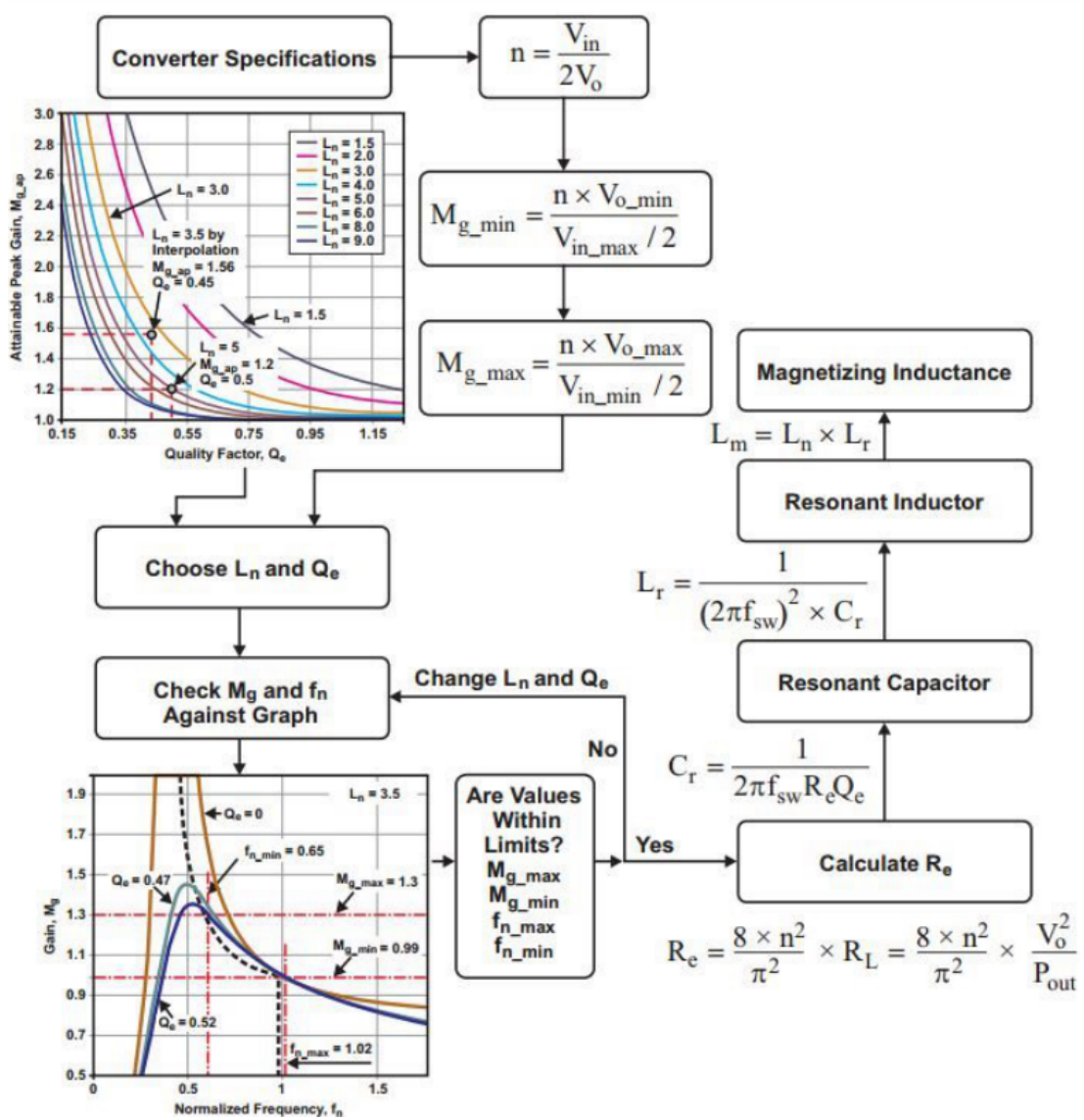


Figure 3.1: LLC Resonant Half-bridge Converter Design Flow Chart, [30].

The design flow for the LLC resonant converter begins with defining the converter specifications, including the input voltage range, output voltage, and required power level. Using these parameters, the turns ratio  $n = \frac{V_{in}}{2V_o}$  is determined. With the turns ratio established, the minimum and maximum voltage gains ( $M_{g\_min}$  and  $M_{g\_max}$ ) are calculated based on the operating input and output voltage limits.

Next, suitable values for the normalized magnetizing inductance ( $L_n$ ) and the quality factor ( $Q_e$ ) are selected using the gain–frequency characteristic curves. These parameters directly influence the shape of the gain curve and define the operating region of the converter. The gain and normalized frequency are then verified against the design graphs to ensure the converter operates within the desired limits over the entire voltage and load range. If the gain boundaries are not satisfied,  $L_n$  and  $Q_e$  are iteratively adjusted until proper operating points are achieved.

Once valid parameters are obtained, the equivalent resistance  $R_e$  is calculated, followed by the determination of the resonant components: the resonant capacitor  $C_r$ , resonant inductor  $L_r$ , and magnetizing inductance  $L_m$ .

This process ensures that the converter achieves high efficiency, maintains ZVS under various operating conditions, and provides stable operation over the full range of input and load variations.

### 3.1.1 Transformer Turns Ratio (n)

Determining the transformer's turns ratio is a crucial first step, as it directly influences several other key parameters in the system. This ratio not only defines the voltage gain but also impacts the design and behavior of the entire resonant tank. Many of the subsequent calculations, such as resonant frequency, impedance matching, and component sizing, depend on the selected turns ratio.

Moreover, the transformer often represents the most constrained and challenging component to source, due to limitations in its specifications. Because it frequently becomes the limiting factor in the overall converter design, it must be considered at the very beginning of the design process. Starting with the transformer ensures that the rest of the circuit can be accurately and efficiently tailored to match its characteristics.

The transformer turns ratio is given by:

$$n = \frac{V_{in\_nom}/2}{V_{o\_nom}} = 12.5 \quad (3.1)$$

### 3.1.2 Converter Gain Boundaries

The converter gain,  $M_g$ , is primarily influenced by three factors: the input voltage seen by the converter (i.e., the battery voltage), the load or equivalent impedance ( $R_{ac}$ ), and the operating frequency of the converter. As expressed in Equation 2.41, variations in the load impedance directly affect the equivalent resistance and consequently the quality factor ( $Q_e$ ), Equation 2.37, altering the shape of the gain curve. To ensure operation within the Safe Operating Area (SOA), it is essential to account for the voltage limits imposed by the Battery Management System (BMS). In the FSFEUP vehicle, the BMS constrains the accumulator voltage to a maximum of 600 V and a minimum of 480 V, preventing the cells from reaching their cutoff energy and minimum voltage limit of 2.5 V. The worst-case condition occurs when the converter operates at the minimum input voltage during maximum discharge current (175 A). Considering the internal resistance of each

cell (15 mΩ) and the 144s5p configuration, the total pack resistance is approximately:

$$R_{bat} = \frac{144 \times 0.015}{5} = 432 \text{ m}\Omega \quad (3.2)$$

Under these conditions, the minimum voltage seen at the converter input can be estimated as:

$$V_{in,min} = 480 \text{ V} - (175 \text{ A} \times 0.432 \text{ }\Omega) \approx 404.4 \text{ V}. \quad (3.3)$$

Therefore, by defining a minimum converter input voltage limit of 480 V, the design ensures that the converter gain remains within the required boundaries, maintaining stable operation and compliance with the SOA across all expected operating conditions.

Having established the voltage operating limits and their impact on the converter's gain behavior, it becomes necessary to define the corresponding gain boundaries that guarantee proper line regulation. These boundaries are determined by the minimum and maximum gain values,  $M_{g\_min}$  and  $M_{g\_max}$ , which the converter must achieve to maintain regulation throughout the normalized frequency range and across varying input and load conditions. According to Equations 3.4 and 3.5, the gain curve must encompass both  $M_{g\_min}$  and  $M_{g\_max}$  within the frequency limits, ensuring reliable operation under all scenarios.

When the output current is zero ( $I_o = 0$ ), the set of all  $M_g$  values greater than the minimum gain at no-load must contain both  $M_{g\_min}$  and  $M_{g\_max}$ :

$$\{M_g \mid M_g > M_{g\_-\infty}\} \supseteq \{M_{g\_min}, M_{g\_max}\} \quad (3.4)$$

When the output current is greater than zero ( $I_o > 0$ ), the set of all possible gain values must still include both  $M_{g\_min}$  and  $M_{g\_max}$ :

$$\{M_g \mid M_g \geq 0\} \supseteq \{M_{g\_min}, M_{g\_max}\} \quad (3.5)$$

The minimum and maximum gain value,  $M_{g\_min}$  and  $M_{g\_max}$ , are given by:

$$M_{g\_min} = \frac{n \times (V_{o\_min} + V_F)}{V_{in\_max}/2} \quad (3.6)$$

$$M_{g\_max} = \frac{n \cdot (V_{o\_max} + V_F + V_{loss})}{V_{in\_min}/2} \quad (3.7)$$

To account for power losses in the converter, a forward voltage drop of  $V_F = 0.7 \text{ V}$  is assumed for the secondary-side diode. Additionally, a total voltage drop due to conduction and power losses is estimated as  $V_{loss} = 2.05 \text{ V}$ . Assuming a converter efficiency of 92%, the remaining 8% represents power losses. Referring these losses to the output voltage at full load (42 A), the output voltage drop can be calculated as:

$$\frac{1000 \text{ W} \cdot 0.08}{0.92 \cdot 42 \text{ A}} = 2.05 \text{ V} \quad (3.8)$$

This voltage drop is added to the maximum gain calculation,  $M_{g\_max}$ , in order to ensure proper voltage-load regulation under full-load conditions.

### 3.1.3 $L_n$ and $Q_e$

To ensure stable and reliable line regulation in the converter's operation, it is essential that the design accounts for both the minimum and maximum gain values. Under no-load conditions ( $I_o = 0$ ), the quality factor becomes zero, which simplifies the gain characteristics such that they depend solely on the normalized inductance  $L_n$ . In this scenario, choosing the correct value for  $L_n$  becomes critical, since it is chosen so that the resulting gain curve intersects both  $M_{g\_min}$  and  $M_{g\_max}$  within the desired operating frequency range. Using the equations 3.6 and 3.7, respectively, the gain limits are given by:

- $M_{g\_min} = 1.029$
- $M_{g\_max} = 1.672$

This ensures that the converter operates efficiently across varying line conditions, as illustrated by the crossover points in Figure 3.2. When a load is applied ( $I_o > 0$ ),  $Q_e$  must also be considered, since the quality factor varies inversely with the load resistance, as shown in Equations 2.37 and 2.41. This variation modifies the shape of the gain curve, but the fundamental requirement remains: the gain must stay within the defined boundaries.

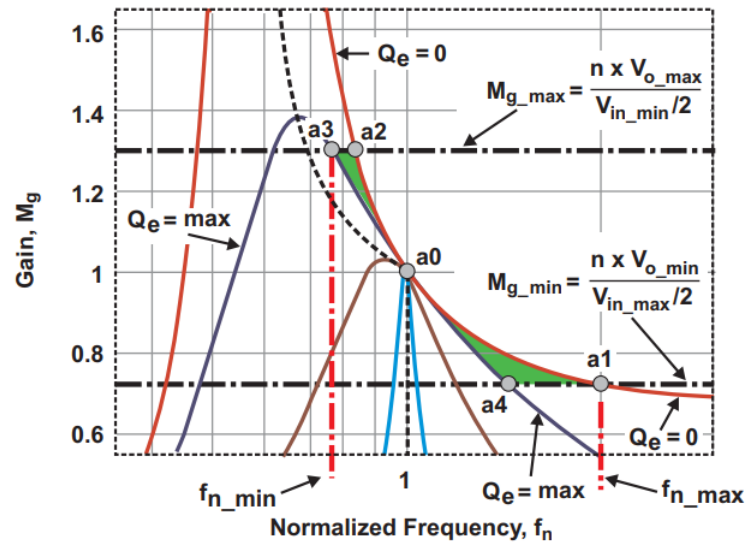


Figure 3.2: Recommended design region and operating boundaries.

In addition to meeting gain limits, it is crucial to ensure that the converter operates within the appropriate region of the gain spectrum, specifically the inductive region. This is the safe and stable area of operation for LLC resonant converters, as illustrated in Figure 3.2, and must be respected to avoid instability. The gain curves define the operating zones, and careful selection

is required to prevent the converter from entering the capacitive region, which could result in undesirable behavior. One key reference point is  $a_3$ , which corresponds to the maximum quality factor  $Q_{e\_max}$ , determined by the highest expected load. Since the gain depends on both  $L_n$  and  $Q_e$ , multiple gain curves must be evaluated to ensure that the chosen operating point stays within the desired inductive region while still satisfying the necessary gain requirements.

To efficiently explore the design space and identify suitable values for  $L_n$  and  $Q_e$ , a series of MATLAB scripts was developed. The first script iteratively sweeps through different values of normalized inductance  $L_n$ , maintaining the quality factor,  $Q_e$ , constant, [A.2](#).

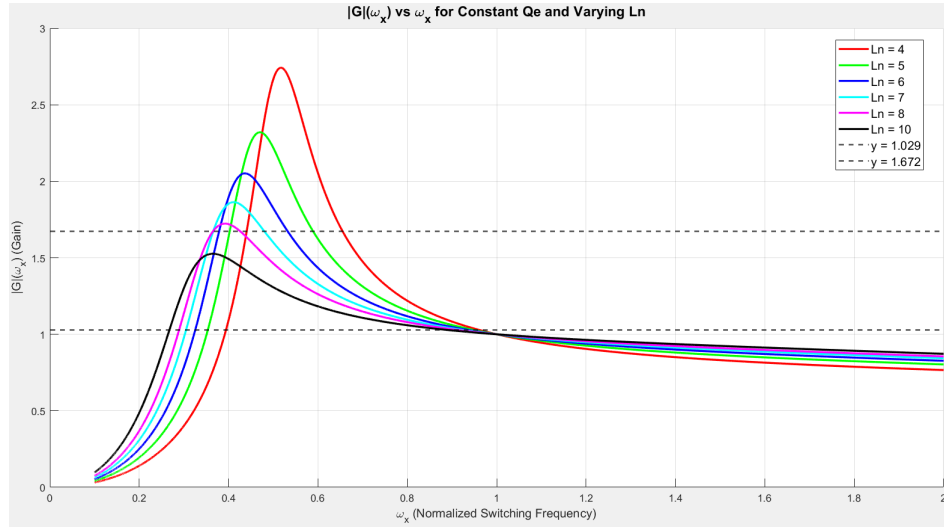


Figure 3.3: Gain Curves with  $Q_e = 0.25$  varying  $L_n$ .

The second focuses on varying the  $Q_e$ , with  $L_n$  constant, taking into account different load conditions, [A.3](#).

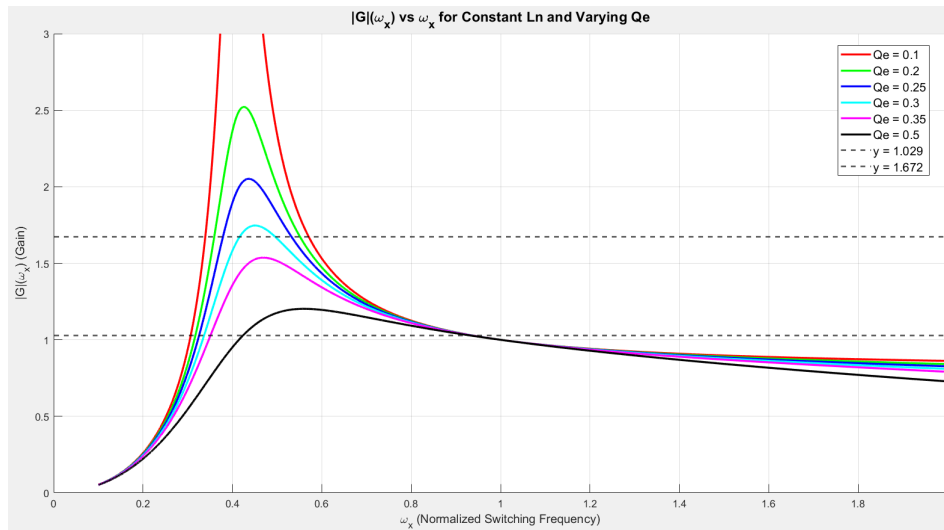


Figure 3.4: Gain Curves with  $L_n = 6$  varying  $Q_e$ .

After analyzing the behavior of the gain curves for various parameter combinations, a final script was created, A.4, which consolidates the results and generates the complete gain profile of the converter under maximum load conditions. This final output clearly shows, Figure 3.5, the gain limits  $M_{g\_min}$  and  $M_{g\_max}$ , as well as the frequency range in which the converter can operate safely within the inductive region.

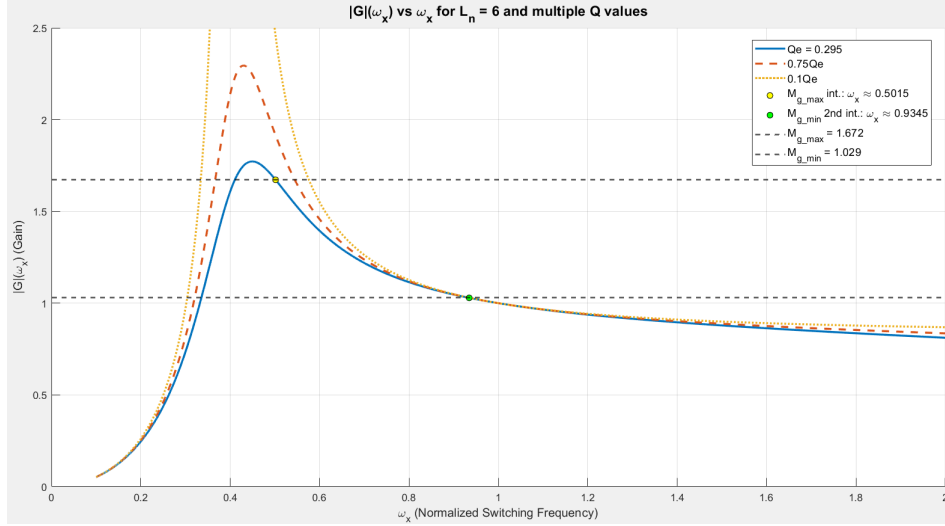


Figure 3.5: Gain Curve with established  $L_n = 7$  and  $Q_e = 0.295$  values.

As shown in Figure 3.5, the resulting gain curve for  $L_n = 7$  and  $Q_e = 0.295$  intersects the maximum gain limit at a normalized switching frequency of approximately  $\omega_x = 0.5015$ , and the second intersection with the minimum gain limit occurs at  $\omega_x = 0.9345$ . This defines a usable frequency range from 50 to 94 kHz in normalized terms.

With these operating conditions established and the resonant tank now fully characterized, the design is ready for final calculations. Using the MATLAB script A.1, developed for this purpose, the values of the resonant components can now be precisely determined.

- Equivalent Load Resistance,  $R_e$ : 67.23 Ohm
- Resonant Capacitor,  $C_r$ : 79.84 nF
- Resonant Inductor,  $L_r$ : 31.72 uH
- Magnetizing Inductor,  $L_m$ : 222.07 uH

### 3.1.4 Resonant Inductor Selection

The selected resonant inductor  $L_r$  must be rated to handle:

- Resonant Inductor,  $L_r$ : 31.72 uH
- Rated Current,  $I_{L_r}$ : 5.829 A

- Terminal AC voltage,  $V_{L_r}$ : 56.2 V

$$V_{L_r} = \omega L_r \cdot I_r \quad (3.9)$$

### 3.1.5 Resonant Capacitor Selection

The resonant capacitor  $C_r$  plays a critical role, operating under high-frequency and high-magnitude current conditions. For this reason, it is essential that the selected capacitor has a low dissipation factor (DF) to minimize power losses and thermal stress. Capacitor types such as electrolytic and multilayer X7R ceramic typically exhibit high DF values and are therefore not well suited for resonant applications. While NP0 ceramic capacitors offer low DF and can be considered, their limited capacitance range can pose design constraints. A common and effective choice for LLC converters is metalized polypropylene film capacitors, which provide both a very low DF and the capability to handle high-frequency AC currents reliably. When selecting a resonant capacitor, its voltage rating must also be derated depending on the switching frequency. Therefore, the final choice of  $C_r$  must account for both the electrical stress and the frequency-dependent derating behavior. In addition to meeting the required capacitance and voltage criteria, the selected capacitor must also be rated to handle:

- Resonant Capacitor,  $C_r$ : 79.84 nF
- Rated Current,  $I_{C_r}$ : 5.829 A
- AC voltage,  $V_{C_r}$ : 246.3 V

$$V_{C_r} = X_{C_r} \cdot I_r = \frac{I_r}{\omega C_r} \quad (3.10)$$

- RMS voltage,  $V_{C_r\_RMS}$ : 388.2 V

$$V_{C_r\_RMS} = \sqrt{\left(\frac{V_{in\_max}}{2}\right)^2 + V_{C_r}^2} \quad (3.11)$$

- Peak voltage,  $V_{C_r\_peak}$ : 648.4 V

$$V_{C_r\_peak} = \frac{V_{in\_max}}{2} + \sqrt{2} \cdot V_{C_r} \quad (3.12)$$

Given the electrical requirements of the resonant capacitor and the choice of polypropylene film capacitors due to their low dissipation factor and suitability for high-frequency operation, special consideration must be given to voltage and current ratings. Polypropylene film capacitors, while ideal for handling high-frequency AC currents, exhibit frequency-dependent voltage derating characteristics. For example, technical documentation often shows that a capacitor rated for a given RMS voltage at low frequencies may only withstand half of that voltage at higher switching frequencies. As a result, a common and effective design strategy is to divide the required capacitance across multiple capacitors in parallel. This method takes advantage of the fact that

lower-capacitance film capacitors typically support higher AC voltage ratings within the high-frequency spectrum, though they come with lower individual current ratings. By connecting them in parallel, the overall current demand is distributed among the units, ensuring that both voltage and current specifications are met safely.

### 3.1.6 Resonant Circuit Design Verification

With the resonant tank components now defined, the next step is to carry out a complete design verification of the LLC resonant converter. This involves reapplying the analytical calculations to confirm the final performance characteristics of the system based on the selected values. The resonant tank is composed of the following components:

- Resonant Capacitor,  $C_r$ : 81 nF
- Resonant Inductor,  $L_r$ : 33  $\mu$ H
- Magnetizing Inductor,  $L_m$ : 220  $\mu$ H

Based on these finalized component values, the script yields the detailed final specifications for the converter as follows:

- Switching Frequency:  $f_{min}$  46.5 kHz to  $f_{max}$  97.5 kHz
- RMS Primary-Side Load Current,  $I_{oe}$ : 4.242 A
- RMS Magnetizing Current,  $I_m$ : 3.997 A
- Total Resonant Tank Current,  $I_r$ : 5.829 A
- Total Secondary-Side RMS Load Current:,  $I_{oe\_s}$ : 50.908 A
- Transformer (center-tapped) current per winding,  $I_{sw}$ : 35.997 A

### 3.1.7 Transformer Selection

The theoretical value of the transformer turns ratio, as derived in Equation 3.1, serves as a fundamental starting point in the design of the LLC resonant converter. This ratio not only determines the voltage gain but also impacts several other parameters throughout the design process. However, beyond the voltage ratio, it is also critical to ensure that the selected transformer can handle the required current levels in both its primary and secondary windings.

To accurately determine the necessary current ratings, a detailed analysis was performed using a script, A.1. This script implements Equations 2.29 through 2.34, to evaluate the current flowing through each winding under various operating conditions. These values were essential for specifying a transformer capable of meeting the converter's electrical demands and ensuring reliable operation across its intended load and frequency range.

So the transformer specifications were:

- Turns ratio ( $n$ ): 12.5
- Primary terminal voltage: 500 VAC
- Primary winding's rated current,  $I_r$ : 5.8 A
- Secondary terminal voltage: 32 VDC
- Secondary winding's rated current,  $I_{sw}$ : 51 A
- Frequency at no load: 93 kHz
- Frequency at full load: 47 kHz
- Insulation between primary and secondary sides: Galvanic Isolation

### 3.1.8 Primary-Side MOSFETs Selection

In the process of selecting power semiconductors for the LLC resonant converter, both Gallium Nitride (GaN) and Silicon Carbide (SiC) MOSFETs were evaluated. GaN and SiC devices each offer significant performance advantages over traditional silicon MOSFETs, particularly in high-efficiency and high-frequency power conversion. SiC MOSFETs are well known for their high voltage blocking capability and thermal performance, making them suitable for applications involving high power and harsh environments. On the other hand, GaN FETs excel in high-frequency switching due to their extremely low gate charge, low output capacitance, and fast switching speeds, which contribute to reduced switching losses and improved overall efficiency.

Given the frequency range of operation in this converter, GaN technology was selected as the most suitable option. The choice was further supported by the desire to explore and apply a newer, cutting-edge semiconductor technology to the design, with the aim of both innovating and expanding practical knowledge. Additionally, GaN FETs align well with one of the core requirements of this project, compactness. Since the converter is intended to be physically small, the use of GaN devices, particularly those with integrated gate drivers, offers a clear advantage in minimizing the overall footprint. This integration not only simplifies the PCB layout but also contributes to reducing parasitics and improving system reliability, making GaN the ideal choice for this application.

Each MOSFET must be rated to withstand the full input voltage, which represents the maximum voltage stress during operation:

$$V_{Q1\_peak} = V_{Q2\_peak} = 1.2 * V_{in\_max} = 720V \quad (3.13)$$

Under steady-state conditions, once the resonant capacitor voltage is established, each MOSFET conducts approximately half of the resonant current. However, during startup and transient events, the current through each device can momentarily reach the peak resonant current:

$$I_{Q1\_RMS} = I_{Q2\_RMS} = I_r = 5.829A \quad (3.14)$$

Due to the ZVS operation of the converter, switching losses in the MOSFETs are significantly reduced. As a result, conduction losses become a more dominant factor in efficiency, emphasizing the importance of selecting devices with low on-resistance  $R_{DS_{on}}$ . Nevertheless, the choice must consider the typical trade-off between  $R_{DS_{on}}$  and the drain-to-source capacitance  $C_{DS}$ , as lower resistance often comes at the cost of higher output capacitance.

The selection of the GaN FET for this converter was based on a set of specific design and performance requirements to ensure efficiency, protection, and compact integration. In addition to electrical performance, ease of layout and thermal management were also considered critical. The requirements were:

- Integrated gate driver
- Voltage rating > 720 VDC
- Continuous current rating > 6 A
- Integrated over-current protection
- Integrated over-temperature protection
- Top-side cooled package

Based on the outlined requirements, the selected GaN FET for this design is the *Texas Instruments, LMG3522R030-Q1*, [27].

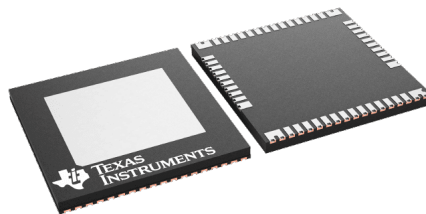


Figure 3.6: LMG3522R030-Q1 GaN FET, [27].

Table 3.1: Main features of the LMG3522R030-Q1 GaN FET, [27]

| Parameter                                       | Value                                                        |
|-------------------------------------------------|--------------------------------------------------------------|
| Manufacturer                                    | Texas Instruments                                            |
| Device type                                     | Automotive-qualified GaN power FET                           |
| Voltage rating, $V_{DS} FET_{ON}$               | 650 V                                                        |
| Voltage rating, $V_{DS(SURGE)} FET_{switching}$ | 720 V                                                        |
| Transient Ringing Peak Voltage, $V_{DS(tr)}$    | 800 V                                                        |
| Continuous drain current, $I_D$                 | 74 A (at 25°C)                                               |
| RDS(on)                                         | 30 mΩ                                                        |
| Gate charge, $Q_g$                              | 7.5 nC                                                       |
| Output charge, $Q_{OSS}$                        | 55 nC                                                        |
| Package                                         | QFN, 8 × 8 mm                                                |
| Operating junction temperature                  | −40°C to 150°C                                               |
| Automotive qualification                        | AEC-Q101, Q100                                               |
| Key features                                    | Integrated driver, low switching loss, zero reverse recovery |

### 3.1.9 ZVS Design

One of the key advantages of the LLC resonant converter topology is its ability to significantly reduce switching losses, primarily through the use of ZVS on the primary side. However, as previously discussed, achieving ZVS imposes constraints on the operating region of the converter, limiting the recommended design area to the right-hand side of the resonant gain curves shown in Figure 3.2.

To achieve ZVS, a MOSFET is turned on only after its drain-to-source voltage ( $V_{DS}$ ) has been externally reduced to zero. A typical method to enable this is to reverse the current flow through the body diode of the MOSFET just as a gate-drive signal is applied. As illustrated in Figure 3.7, when Q1 turns off at time  $t_1$ , there is a deliberate delay before Q2 is turned on at  $t_2$ . This interval, known as the dead time ( $t_{dead}$ ), allows the resonant current  $I_r$  to transition from Q1 to Q2. During this time,  $I_r$  first discharges the drain-to-source capacitance  $C_{DS}$  of Q2, reducing its  $V_{DS}$  to zero, and then begins to forward-bias Q2's body diode. When the gate-drive signal is applied at  $t_2$ , Q2 is already conducting through its body diode, ensuring that  $V_{DS\_Q2} \approx 0$ , aside from the small forward voltage drop of the diode. A similar process must occur for Q1 during its turn-on cycle. Achieving this condition requires that a non-zero current continue to flow in the same direction immediately after the switch turns off. This current is typically sustained by the inductive elements of the circuit, which naturally cause current to lag behind voltage.

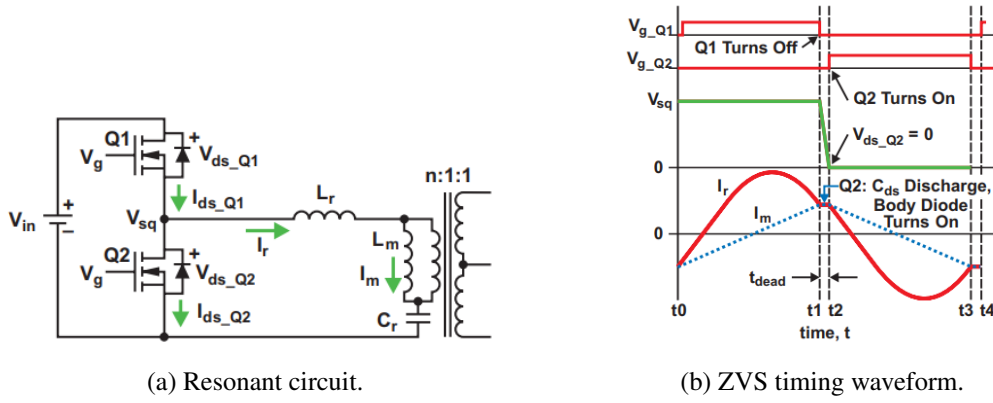


Figure 3.7: ZVS operation.

To guarantee ZVS, the converter's input impedance  $Z_{in}$  must be inductive, and it can be expressed in its polar form:

$$Z_{in} = |Z_{in}| e^{j\phi_z}, \quad (3.15)$$

The phase angle  $\phi_z$ , between  $I_r$  and  $V_{ge}$  varies in relation to  $-\pi/2 \leq \phi_z \leq \pi/2$ . The impedance characteristics are determined as follows:

- $\phi_z > 0$ : Inductive impedance
- $\phi_z < 0$ : Capacitive impedance
- $\phi_z = 0$ : Purely resistive impedance

Since the phase angle  $\phi_z$  is a function of switching frequency, the resonant peak locus where  $\phi_z = 0$  serves as the boundary between the inductive and capacitive regions, Figure 2.24. Therefore, ZVS is achievable only when the input phase angle is greater than zero:

$$\phi_z > 0 \quad (3.16)$$

Moreover, sufficient inductive energy must be available to ensure the ZVS condition is met. During  $t_{dead}$ , the resonant current  $I_r$  is approximately equal to the magnetizing current  $I_m$ , which is inherently sinusoidal. In this interval,  $I_m$  circulates through the output capacitances  $C_{DS}$  of Q1 and Q2. The magnetic energy stored in  $I_m$  is converted into electric energy to charge and discharge the respective  $C_{DS}$  capacitors. This energy transition must occur before the body diode of Q2 starts conducting. Given that the resonant capacitor  $C_r$  is significantly larger than  $2 \times C_{DS}$ , its influence during  $t_{dead}$  can be neglected.

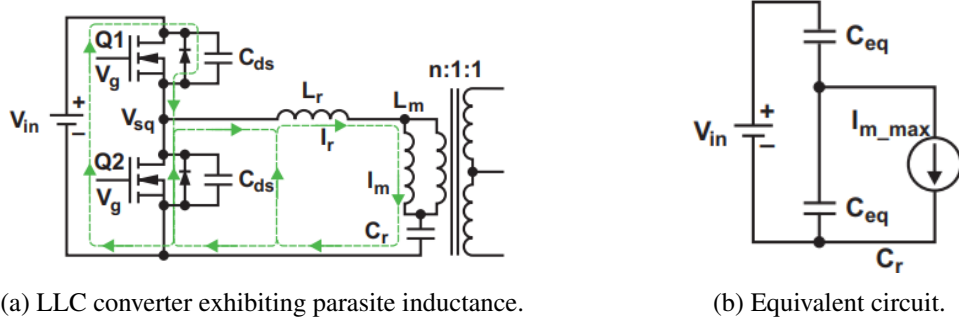


Figure 3.8: Securing sufficient inductive energy for ZVS.

An equivalent circuit for this interval is shown in Figure 3.8, where an effective capacitance  $C_{eq}$  models both the intrinsic and parasitic capacitances. For Q2's body diode to conduct before  $t_{dead}$  ends, the following conditions must be satisfied:

$$\frac{1}{2}(L_m + L_r)I_{m\_peak}^2 \geq \frac{1}{2}(2C_{eq})V_{in}^2 \quad (3.17)$$

$$t_{dead} \geq 16 \cdot C_{eq} \cdot f_{sw} \cdot L_m \quad (3.18)$$

These conditions ensure that enough energy is available within the magnetizing current to fully charge and discharge the capacitances, thereby enabling reliable ZVS operation.

The worst-case minimum magnetizing current  $I_{m\_min}$  is determined as:

$$I_{m\_min} = \frac{2\sqrt{2}}{\pi} \cdot \frac{n \cdot V_o}{2\pi f_{sw} L_m} \quad \text{with } f_{sw} = 97.4 \text{ kHz} \quad (3.19)$$

Based on the selected MOSFET characteristics,  $C_{eq} = 250\text{nF}$ , and the required energy for zero-voltage switching, the minimum dead time is calculated to be approximately  $64.25 \text{ ns}$ . Therefore, implementing a dead time of  $100 \text{ ns}$  ensures compliance with the ZVS condition under worst-case scenarios.

### 3.1.10 Rectifier Diodes Selection

The voltage rating of the secondary-side rectifier diodes is established as follows:

$$V_{DB} = \frac{V_{in\_max}/2}{n} \cdot 2 \quad (3.20)$$

The current rating of the diodes is established as follows:

$$I_{sav} = \frac{\sqrt{2} \cdot I_{oe\_s}}{\pi} \quad (3.21)$$

For the output rectification stage, the required diode specifications were  $V_{DB} = 50\text{VDC}$  and  $I_{sav} = 22.92\text{A}$ . Based on these requirements, the *Vishay General Semiconductor, V60D60C-M3/I* rectifier

diode was selected. This device meets the necessary electrical ratings and is well-suited for high-current, low-voltage rectification in high-frequency power converter applications.

### 3.1.11 Output Filter

The full-wave output current of the rectifier can be expressed as:

$$I_{rect} = I_{sw} = \frac{\pi}{2\sqrt{2}} \cdot I_o \quad (3.22)$$

With an operating frequency of approximately 100 kHz, the RMS current rating for the output capacitor for the load current  $I_o$  can be calculated as:

$$I_{C_o} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} \cdot I_o\right)^2 - I_o^2} = \sqrt{\frac{\pi^2}{8} - 1} \cdot I_o \quad (3.23)$$

Typically, a single capacitor is not sufficient to handle the high RMS current required at these frequencies. To address this limitation, multiple capacitors are often connected in parallel. Capacitors with high RMS current ratings and low equivalent series resistance (ESR) are especially suitable for this application. The ripple voltage across the output is primarily influenced by the AC current flowing into and out of the output capacitors during each switching cycle. This current, multiplied by the ESR of the capacitors, gives a close estimation of the ripple voltage. Since both the AC ripple and the DC load current contribute to the total current through the capacitors, this method provides a conservative and reliable design criterion. To meet a ripple voltage specification of 240 mV, the maximum allowable ESR can be derived accordingly.

$$ESR_{max} = \frac{V_{o\_pk-pk}}{I_{rect\_peak}} = \frac{V_{o\_pk-pk}}{\left(\frac{\pi}{4} \cdot I_o\right) \cdot 2} \quad (3.24)$$

To determine the ceramic capacitance needed to keep the ripple voltage within acceptable limits, the minimum required value to limit the ripple to 240 mV<sub>pp</sub> is calculated as:

$$dc = \left( \frac{V_{out\_nom}}{V_{in\_min} \cdot \eta} \right) \quad (3.25)$$

$$C_{min} = \frac{I_{out} \cdot dc \cdot (1 - dc) \cdot 1000}{f_{sw\_min} \cdot V_{pp}} \quad (3.26)$$

Ultimately, the combination of capacitors has to satisfy the following critical requirements:

- Voltage rating: 32 V
- Ripple current rating: 20.14 A
- ESR: < 3.67 mΩ
- Minimum ceramic capacitance: 232.3 nF

For the output filter design, a two-stage capacitor strategy was adopted to optimize ripple suppression across a wide frequency range. This approach combines two different types of capacitors, each selected for its specific performance characteristics. Multilayer ceramic capacitors (MLCCs) were used for high-frequency ripple filtering due to their low inductance and excellent high-frequency response. In parallel, polymer capacitors, chosen for their low equivalent series resistance (ESR), were employed to manage ripple at lower frequencies and to contribute to bulk energy storage.

The result of this combination is a filter design where ceramic capacitors dominate the high-frequency response, effectively suppressing fast-switching noise, while polymer capacitors dominate the ESR behavior and provide stability through their ability to handle higher ripple currents and support steady-state output. This hybrid approach allows the filter to meet both transient and steady-state performance requirements more efficiently than using a single capacitor type alone.

## 3.2 Dynamic Modeling and Control Design

### 3.2.1 Plant seen by the controller

Before designing the controller, it is important to understand the dynamic behavior of the converter as seen from the control point of view. Around the nominal operating point, the plant can be represented by the FHA transfer function, expressed in polynomial form as:

$$T_{FHA}(s) = \frac{C_r L_m R_{ac} s^2}{C_r L_r L_m s^3 + C_r R_{ac} (L_r + L_m) s^2 + L_m s + R_{ac}}. \quad (3.27)$$

This third-order transfer function exhibits two zeros at the origin and three poles, one real and one complex-conjugate pair. The complex poles are associated with the resonant tank ( $L_r, L_m, C_r$ ) and generate the typical gain peak around the resonant frequency. The real pole introduces an additional attenuation at higher frequencies, limiting the open-loop bandwidth.

From the controller's perspective, this means the system behaves as a band-pass network whose resonance produces a phase lag near  $f_s - f_p$ . To ensure stability and adequate dynamic response, the loop crossover frequency must be placed well below the resonant peak, where the phase shift is still moderate.

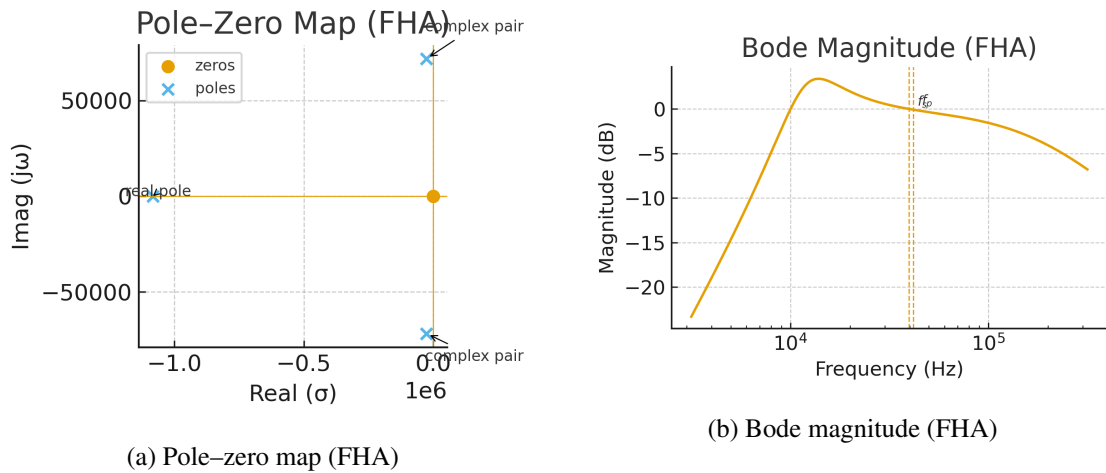


Figure 3.9: LLC FHA deconstruction: the complex pole pair produces the resonant hump; the real pole flattens high-frequency gain.

The dynamic characteristics observed in Figure 3.9 indicate that the converter presents a smooth, single resonant hump followed by a stable roll-off. Therefore, a proportional–integral (PI) controller is suitable for this type of plant. The script used to create these plots is provided in Appendix A.7.

The PI provides an integrator to remove steady-state error and a zero to compensate the phase lag introduced by the resonant tank. By properly tuning the crossover frequency below the resonant region, the PI controller can ensure adequate phase margin, fast transient response, and robustness against parameter variations without requiring more complex control strategies.

### 3.2.2 Proportional Integral (PI)

For the control methodology of the LLC resonant converter, a PI controller was selected, [29]. Given the extensive effort required for the design, tuning, and implementation of more advanced control strategies, it was deemed practical to begin with a simpler and well-established solution during the prototype phase. PI control is among the most commonly used approaches in industrial power electronics due to its simplicity, reliability, and effectiveness in regulating steady-state errors.

The PI controller can be designed to meet performance specifications defined either in the time domain or in the frequency domain. Regardless, the implementation reduces to determining two real-valued gains: one for the proportional path and one for the integral path.

The PI control configuration implemented was the parallel, as can be seen below, Figure 3.10.

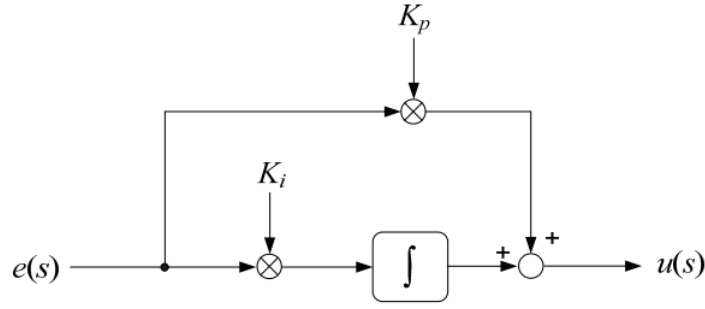


Figure 3.10: PI - Parallel configuration.

In this control structure, the proportional and integral components operate in parallel, each contributing to the overall response. Conceptually, the process of tuning the controller for transient response can be relatively straightforward: one adjusts each gain in turn, blending together different amounts of proportional and integral control action, until the desired specifications are met.

The parallel PI controller transfer function is:

$$F(s) = K_p + \frac{K_i}{s} = \frac{K_p s + K_i}{s} \quad (3.28)$$

The transfer function of the parallel PI controller implemented in this project takes the standard form of an integrator combined with a single real zero, commonly referred to as the zero-plus integrator configuration. This can be expressed generically as:

$$F(s) = \frac{b_1 s + b_0}{s} \quad (3.29)$$

This structure is widely used in power supply loop compensation, where  $b_1$  typically represents the proportional gain component and  $b_0$  defines the zero frequency. In the conventional case,  $b_1 = 1$  and  $b_0$  directly sets the location of the controller zero.

### Discrete Transformation

Several techniques exist for converting a continuous-time transfer function into an equivalent discrete-time representation. One of the most widely used approaches is the bilinear transform, also known as the *Tustin* method. This method substitutes each occurrence of the Laplace variable  $s$  in the continuous-time domain with an expression involving the discrete-time variable  $z$  and the sampling period  $T$ , thereby enabling implementation in digital control systems.

The transformed equation will be:

$$F(z) = A \cdot \frac{c_1 z + c_0}{z - 1} \quad (3.30)$$

where the numerator coefficients are:

$$c_1 = b_1 + \frac{T}{2}b_0 \quad c_0 = -b_1 + \frac{T}{2}b_0 \quad A = \frac{b_0}{c_1 + c_0} \quad (3.31)$$

With the discrete-time transfer function of the PI controller now established, the corresponding time-domain difference equation can be derived by algebraic manipulation and applying the shifting property of the Z-transform.

$$u(k) = u(k-1) + Ac_1e(k) + Ac_0e(k-1) \quad (3.32)$$

### Parallel Controller Gains

To ensure that the discrete-time implementation of the PI controller closely replicates the behavior of its continuous-time counterpart, it is necessary to properly determine the equivalent proportional and integral gains.

The structure of the discrete-time PI controller in parallel form is presented below. To clearly distinguish the gains used in the discrete-time domain from those in the original continuous-time controller, the discrete-time proportional and integral gains are denoted as  $V_p$  and  $V_i$ , respectively.

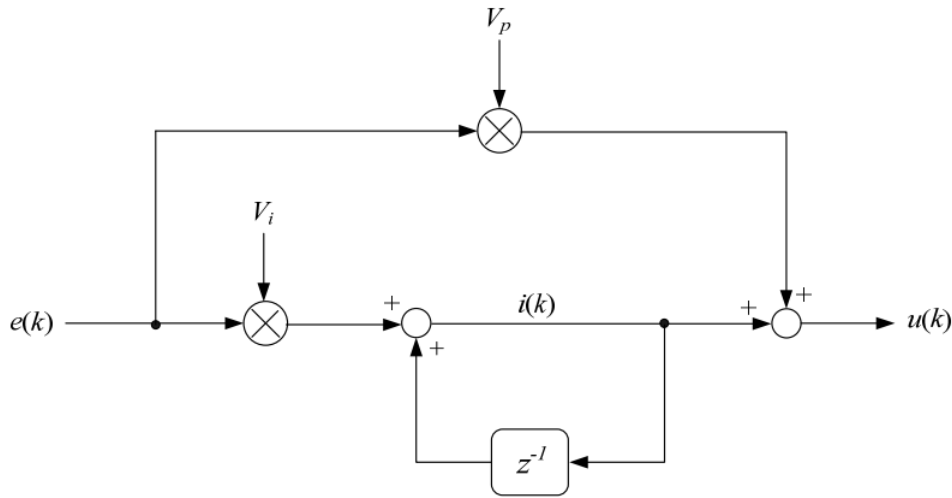


Figure 3.11: Discrete time parallel PI structure.

The corresponding difference equation can then be derived:

$$u(k) = u(k-1) + (V_p + V_i)e(k) - V_p e(k-1) \quad (3.33)$$

The gain values for the discrete-time controller are expressed as follows:

$$V_p = A \left( K_p - \frac{T}{2} K_i \right) \quad (3.34)$$

$$V_i = ATK_i \quad (3.35)$$

## Chapter 4

# Converter Implementation and Simulation Analysis

This chapter describes the practical implementation and simulation analysis of the designed LLC resonant converter. Following the design stage presented in Chapter 3, the focus now shifts toward the hardware realization, control implementation, and verification of the converter's operating behavior through simulation.

The first part of the chapter provides a detailed overview of the hardware implementation, including the converter's main building blocks, filtering stages, rectifier configuration, and sensing and control signal architecture. These aspects ensure proper integration between the power and control stages, enabling stable and safe operation.

Subsequently, the converter's performance is evaluated through a series of simulation studies. These include frequency sweep open-loop analysis, closed-loop validation, soft-start behavior, and dynamic response under load variations. An efficiency evaluation considering semiconductor losses is also conducted to assess the converter's overall performance under realistic operating conditions.

### 4.1 Hardware Implementation and Design Details

Moving towards the practical implementation and the development of a final prototype, it is necessary to select components with the appropriate specifications to meet the project requirements. The first component chosen was the transformer of the converter, as it forms the basis for designing the resonant tank and determining the converter currents.

An analysis of available off-the-shelf transformers was carried out, and the selected component was a planar transformer from *PREMO DCDC2400-001* [19]. The DCDC series includes high-performance LLC transformers and chokes specifically designed for automotive on-board DC/DC converters. This component is optimized for power conversion up to 2 kW and features a low-profile design, making it well-suited for integration into compact automotive systems. The use

of litz wire and copper frames ensures high efficiency and robustness across a wide temperature range, while compliance with AEC-Q200 standards guarantees automotive-grade reliability.

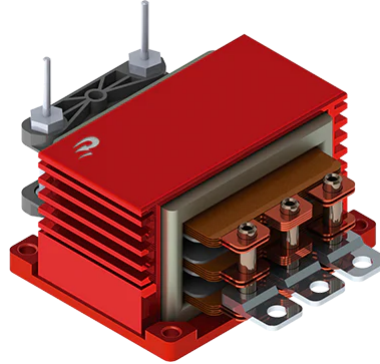
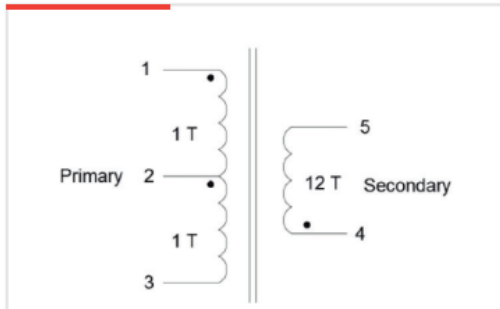


Figure 4.1: Planar Transformer, [19].

#### ELECTRICAL DIAGRAM



(a) Electrical Diagram

#### ELECTRICAL SPECIFICATIONS

| INDUCTANCE at 25°C                      |                       |
|-----------------------------------------|-----------------------|
| L1-3 = Lp<br>(100kHz/1Vac)              | 18,5μH ±20%           |
| DC RESISTANCE at 25°C                   |                       |
| R1-3                                    | 0,30mΩ MAX            |
| R4-5                                    | 25mΩ MAX              |
| TURN-RATIO                              |                       |
| Np:Ns                                   | 1+1:12                |
| LEAKAGE INDUCTANCE                      |                       |
| Llk4-5<br>(100kHz/1Vac, 1-3<br>shorted) | 1,80μH MAX            |
| DIELECTRIC STRENGTH                     |                       |
| {Np}/{CORE}                             | 500Vac/50Hz/5mA/1min* |
| {Np}/{Ns+CORE}                          | 3kVac/50Hz/5mA/1min*  |

(\*) 1min in qualification / 2sec in mass production

(b) Electrical Specifications

Figure 4.2: *PREMO DCDC2400-001* datasheet details, [19].

The magnetizing inductance provided in the datasheet is measured on the primary winding (pins 1–3), with a value of

$$L_{m,pri} = 18.5 \mu H \quad (4.1)$$

To refer this inductance to the secondary side, the quadratic relation of the turns ratio must be applied:

$$L_{m,sec} = L_{m,pri} \cdot \left( \frac{N_s}{N_p} \right)^2 \quad (4.2)$$

where  $N_p = 2$  corresponds to the two primary turns (1+1) and  $N_s = 12$  to the number of secondary turns.

Thus, we obtain

$$L_{m,sec} = 18.5 \mu H \cdot \left(\frac{12}{2}\right)^2 = 18.5 \mu H \cdot 36 \approx 666 \mu H \quad (4.3)$$

Therefore, the magnetizing inductance referred to the secondary side is approximately  $666 \mu H$ .

The leakage inductance provided in the datasheet is measured on the secondary winding, with a value of

$$L_{lk,sec} = 1.8 \mu H \quad (4.4)$$

Using the same calculation approach as applied for the magnetizing inductance, this value, referred to the primary side, corresponds to approximately

$$L_{lk,pri} \approx 0.05 \mu H \quad (4.5)$$

This value is minimal when compared to the required resonant inductance and will therefore be considered negligible for the resonant tank design. It is also important to note that in the present converter implementation, the transformer windings are used inversely, meaning that the datasheet primary corresponds to the secondary in the converter, and vice versa.

The magnetizing inductance of the transformer is significantly higher than the value initially considered in the section *Resonant Circuit Design Verification*. As a result, the resonant tank of the converter must be adapted to this higher magnetizing inductance in order to ensure that the converter operates within the required gain range.

To achieve this, the resonant tank had to be recalculated. Specifically, the resonant inductance and capacitance values were redesigned using a MATLAB script (see Appendix A.5). This script recalculates the resonant tank based on the updated magnetizing inductance of the transformer and generates the corresponding gain–frequency curves for different load conditions. The process was carried out iteratively, since both the inductance ratio  $L_n$  and the resonant frequency strongly influence the converter's behaviour at various load factors. Through these iterations, new values for the resonant tank parameters were obtained, ensuring that the converter is able to operate over the entire required range for this project.

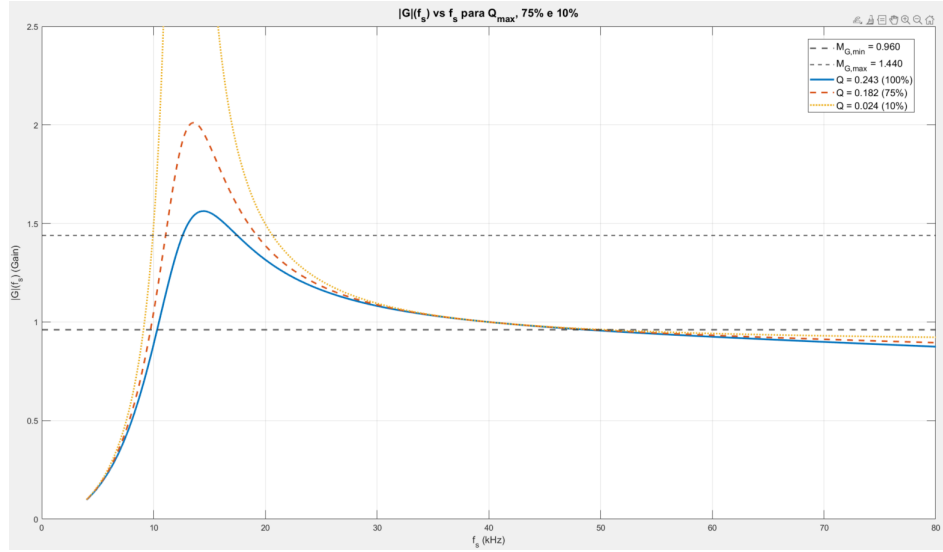


Figure 4.3: Converter Characteristics Curves.

As a consequence of this adjustment, and as illustrated in the Figure 4.3, the resonant frequency of the tank decreased while the ratio between the magnetizing inductance and the resonant inductance increased, reaching approximately 40 kHz and  $L_n = 10$ , respectively.

Finally, the results obtained from the MATLAB script can be summarized as follows:

- Quality factor:  $Q_e = 0.243$
- Equivalent load resistance:  $R_{eq} = 67.23 \, \Omega$
- Resonant capacitor:  $C_r = 243.56 \, \text{nF}$
- Resonant inductor:  $L_r = 65.00 \, \mu\text{H}$
- Resonant frequency:  $f_{res} = 40.0 \, \text{kHz}$

With the new values of the resonant capacitor and resonant inductor determined, it was necessary to select commercially available components that meet these requirements. The following components were chosen:

- Resonant capacitor: three capacitors of 82 nF connected in parallel, resulting in a total of 246 nF, model *KEMET R76QI28205050J* [14].
- Resonant inductor: 65  $\mu\text{H}$ , model *Würth Elektronik 7443783533650* [16].

With the updated resonant capacitor and inductor values, the MATLAB script (Appendix A.1) was executed once again to perform the complete design of the LLC converter. This script automates the full dimensioning process, including the resonant tank design, transformer and rectifier specification, input and output filter sizing, semiconductor selection, and verification of ZVS conditions. It therefore provides a comprehensive computational framework that integrates all key design stages of the converter. The obtained results are summarized below.

### Resonant-Circuit Verification

- Resonant capacitor:  $C_r = 246.0$  nF
- Resonant inductor:  $L_r = 65.0$   $\mu$ H
- Magnetizing inductor:  $L_m = 660.0$   $\mu$ H
- Quality factor at full load:  $Q_e = 0.242$
- Switching frequency range:  $f_{sw,min} = 19.0$  kHz,  $f_{sw,max} = 39.8$  kHz
- RMS primary-side load current:  $I_{pri} = 4.24$  A
- RMS magnetizing current:  $I_m = [1.62, 3.38]$  A
- Resonant tank current (total):  $I_{tank} = [4.54, 5.43]$  A
- Secondary-side RMS load current (total):  $I_{sec} = 50.91$  A
- Transformer (center-tapped), current per winding:  $I_{winding} = 36.0$  A

### Resonant Inductor Selection

- Series resonant inductance:  $L_r = 65.0$   $\mu$ H
- Rated current:  $I_{L_r} = 5.4$  A
- Terminal AC voltage:  $V_{L_r} = [73.8, 42.1]$  V

### Resonant Capacitor Selection

- Series resonant capacitance:  $C_r = 246.0$  nF
- Rated current:  $I_{C_r} = [4.5, 5.4]$  A
- AC voltage:  $V_{C_r} = [73.8, 184.7]$  V
- RMS voltage:  $V_{C_r,RMS} = [308.9, 352.3]$  V
- Peak voltage:  $V_{C_r,peak} = [404.4, 561.2]$  V

### ZVS Design Considerations

- MOSFET rating: 720.0 V/5.97 A
- Equivalent capacitance of MOSFET: 250.0 pF
- Worst-case minimum magnetizing current:  $I_{m,min} = 1.57$  A
- Required dead time:  $t_d > 78.81$  ns

### Rectifier Diodes

- Output diode voltage rating: 50.0 V
- Output diode current rating: 22.92 A

### Output Filter

- Output capacitor ripple current: 20.14 A
- ESR: 3.67 m $\Omega$
- Minimum ceramic capacitance to achieve ripple voltage of 0.24 mV<sub>pp</sub>: 568.3  $\mu$ F

Table 4.1: Summary of recalculated LLC converter design parameters.

| Parameter                                   | Value               |
|---------------------------------------------|---------------------|
| Resonant capacitor, $C_r$                   | 246.0 nF            |
| Resonant inductor, $L_r$                    | 65.0 $\mu$ H        |
| Magnetizing inductor, $L_m$                 | 660.0 $\mu$ H       |
| Quality factor (full load), $Q_e$           | 0.242               |
| Switching frequency range, $f_{sw}$         | 19.0 kHz – 39.8 kHz |
| RMS primary-side load current, $I_{pri}$    | 4.24 A              |
| RMS magnetizing current, $I_m$              | 1.62 – 3.38 A       |
| Resonant tank current, $I_{tank}$           | 4.54 – 5.43 A       |
| RMS secondary-side load current, $I_{sec}$  | 50.91 A             |
| Transformer winding current (center-tapped) | 36.0 A              |
| MOSFET rating                               | 720.0 V / 5.97 A    |
| Rectifier diode ratings                     | 50.0 V / 22.92 A    |
| Output capacitor ripple current             | 20.14 A             |
| Minimum ceramic capacitance                 | 568.3 $\mu$ F       |

#### 4.1.1 Converter Block Diagram

With the electrical and magnetic parameters of the LLC stage established, the work transitions from system modelling to hardware definition. Figure 4.4 consolidates these decisions into a block diagram that serves as the baseline for the PCB design. The diagram highlights the GaN half-bridge, the resonant tank and transformer, the center-tap rectifier, and the galvanic-isolation boundary separating the high-voltage and control domains. From this baseline, the main hardware choices for filtering and sensing are presented next.

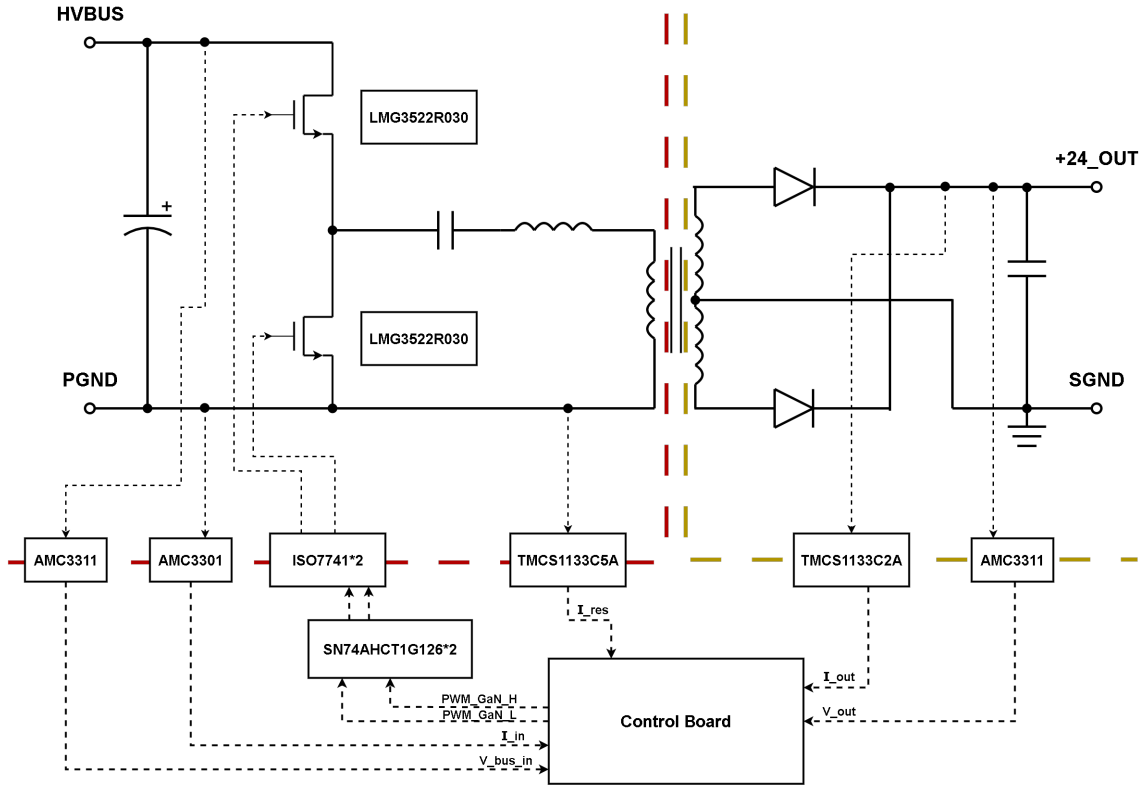


Figure 4.4: Block diagram of Proposed Converter Circuit.

#### 4.1.2 Input Filter Design

In order to ensure stable operation of the half-bridge resonant converter and to suppress undesired high-frequency disturbances, an input filter was implemented at the DC link. The input filter is composed of a combination of a film capacitor and ceramic capacitors, each chosen to fulfill a specific role in stabilizing the converter and minimizing switching-related transients.

The bulk energy storage is provided by a film capacitor (C4AQCBU5100A11J, 650 V, 10  $\mu$ F), [13]. Film capacitors are well-suited for this purpose due to their high voltage rating, low ESR, and excellent long-term stability. This capacitor acts primarily as the main DC bus decoupling element, maintaining a low-impedance energy reservoir to support the half-bridge stage during high-frequency switching transitions.

To further suppress high-frequency oscillations and dampen parasitic ringing at the input stage of the two GaN transistors, three multilayer ceramic capacitors (GRM43DR72J104KW01L, 0.1  $\mu$ F, 630 V), [38]. They were placed in parallel with the film capacitor. Ceramic capacitors, with their inherently low parasitic inductance and ESR, are highly effective at providing local high-frequency decoupling. Their placement close to the power switches ensures that high  $di/dt$  switching currents are locally bypassed, preventing voltage overshoot and minimizing electromagnetic interference (EMI).

### 4.1.3 Output Filter Design

The output stage of the half-bridge resonant converter requires careful filtering in order to attenuate voltage ripple and to guarantee a stable DC voltage at the load. For this purpose, a mixed capacitor network was implemented, combining multilayer ceramic capacitors (MLCCs) with aluminum hybrid polymer capacitors. This configuration provides both high-frequency decoupling and strong bulk energy storage, while minimizing equivalent series resistance (ESR).

A total of 24 ceramic capacitors (UMK325AB7106MM-T, 10  $\mu\text{F}$ , 50 V), [47], were connected in parallel. These capacitors provide a large cumulative capacitance with low parasitic inductance, effectively suppressing high-frequency switching ripple. Their placement close to the rectifier output minimizes loop impedance, ensuring that high  $di/dt$  current components are locally bypassed.

In addition, six aluminum hybrid polymer capacitors (EEH-ZS1V471UP, 470  $\mu\text{F}$ , 35 V, ESR = 14 m $\Omega$ ), [12], were employed to provide bulk energy storage. Due to their inherently low ESR and high ripple current capability, these capacitors are particularly effective at reducing low-frequency ripple and maintaining output voltage stability under dynamic load conditions. With six devices in parallel, the total capacitance increases to 2820  $\mu\text{F}$ , and the effective ESR is reduced to approximately 2.33 m $\Omega$ , significantly improving transient response and ripple suppression.

### 4.1.4 Rectifier Stage

For the rectification stage of the half-bridge LLC converter, the device V60D60C-M3/I, [44], was selected. This component is a Schottky rectifier diode consisting of two elements in a common-cathode configuration, rated for 30 A per diode and a repetitive reverse voltage of 60 V.

The primary requirement for the rectifier in this design is to withstand the secondary-side RMS current of approximately 50 A (as calculated in the design) while maintaining low conduction losses and minimizing reverse-recovery effects. The V60D60C-M3/I meets these requirements for the following reasons:

- **Current rating:** Each diode is capable of carrying 30 A average forward current, with surge capability well above the expected peaks. In the center-tapped configuration, the effective current per diode is within this limit.
- **Voltage rating:** The device is rated for 60 V reverse repetitive voltage ( $V_{RRM}$ ), which provides sufficient margin over the reflected secondary voltage of the converter. This is adequate given the design constraints, provided that proper snubbing is implemented to limit ringing.
- **Schottky technology:** The Schottky construction results in negligible reverse-recovery charge, which is advantageous in high-frequency resonant converters.
- **Low forward voltage drop:** With a forward voltage in the range of 0.5–0.6 V at the operating current, conduction losses are kept low.

- Thermal performance: The device offers low junction-to-case thermal resistance, making it suitable for operation in compact designs when mounted on an adequate PCB copper area or heatsink.

#### 4.1.5 Sensing and Control Signals

In the design of the resonant converter PCB, several key signals were acquired in order to enable feedback control and monitoring of the converter's operation. A voltage mode control strategy was adopted, where the output voltage is continuously monitored and used to adjust the switching frequency of the converter. In this way, the converter maintains a regulated output of 24 V, independent of variations in load or input voltage.

Although this approach represents the minimum requirement for basic regulation, it is not the most optimal control strategy for fine-tuned operation of an LLC resonant converter. Therefore, the sensing circuitry was designed not only to provide the necessary output voltage feedback but also to establish the basis for future improvements in the control algorithm, as seen in Figure 4.4. By monitoring additional signals, it will be possible to redesign the control in later iterations to improve efficiency and performance.

For this purpose, the following quantities were measured:

- Input voltage
- Input current
- Resonant tank current
- Output current
- Output voltage

To ensure safety and signal integrity, all measurements were taken using galvanically isolated sensors, thereby maintaining a clear separation between the high-voltage and low-voltage domains of the converter.

Two types of isolation sensors from Texas Instruments were employed:

- Voltage sensing: AMC3311, [24]
- Current sensing: AMC3301, [23], (for input current) and TMCS1133, [31], (for output current and resonant tank current)

The AMC series sensors provide isolated analog outputs, which were further processed to improve signal quality. An operational amplifier (OPA320), [28], was used to amplify and filter the output of the sensors. In addition, a reference common-mode voltage of 1.65 V was generated, also with the OPA320, in order to properly bias the amplified signals for the analog-to-digital conversion stage, as can be seen in Figure 4.5.

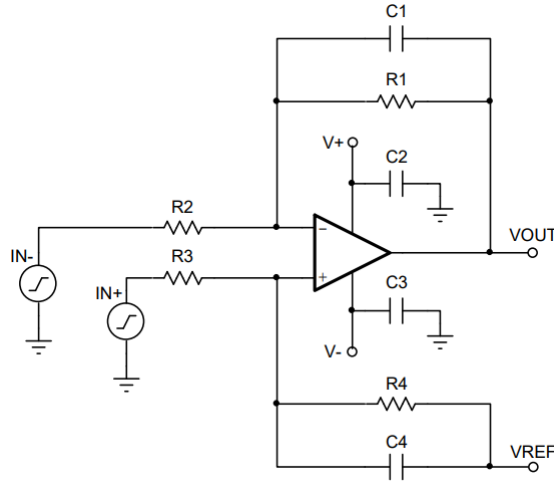


Figure 4.5: Difference amplifier schematic, [51].

Equation 4.6 below displays the transfer function of the difference amplifier circuit configuration.

$$V_{out} = \left( \frac{R_4}{R_3 + R_4} \right) \times \left( 1 + \frac{R_1}{R_2} \right) \times IN_+ + \left( \frac{R_3}{R_3 + R_4} \right) \times \left( 1 + \frac{R_1}{R_2} \right) \times V_{ref} - \frac{R_1}{R_2} \times IN_- \quad (4.6)$$

By setting  $R_1 = R_4$  and  $R_2 = R_3$ , the expression in Equation 4.6 simplifies to Equation 4.7.

$$V_{out} = \frac{R_1}{R_2} \times (IN_+ - IN_-) + V_{ref} \quad (4.7)$$

This sensing architecture enables accurate feedback for the present voltage mode control while simultaneously creating the necessary foundation for advanced control strategies in future work, which could further optimize efficiency and dynamic performance of the converter.

## 4.2 Simulation

The simulation stage plays a crucial role in validating the theoretical design and control strategy of the LLC resonant converter before practical implementation. Through a series of structured analyses, different operating conditions and control scenarios are evaluated to verify performance, stability, and efficiency across the converter's full operating range. The models are implemented using *PLECS*, allowing precise representation of the resonant tank behavior, switching dynamics, and control loops.

The simulation process is organized into several key steps. First, an open-loop frequency sweep analysis is performed to characterize the resonant network, evaluate the gain-frequency relationship, and determine the optimal operating region. Next, a closed-loop analysis validates the converter's voltage regulation performance under feedback control, confirming system stability and dynamic response. The soft-start mechanism is then investigated to ensure smooth startup

behavior without excessive inrush currents or voltage overshoot. Following this, the converter's dynamic performance is tested under a step change in load current, assessing transient response and control robustness. Finally, an efficiency evaluation is conducted, including semiconductor switching and conduction losses, under a realistic resistive load variation to determine the converter's real-world performance.

This systematic approach ensures a comprehensive understanding of the converter's steady-state and transient operation, confirming the effectiveness of the chosen design parameters and control strategies prior to experimental validation.

#### 4.2.1 Frequency sweep open-loop analysis

To evaluate the frequency response of the converter under realistic conditions, a dedicated simulation script was developed.

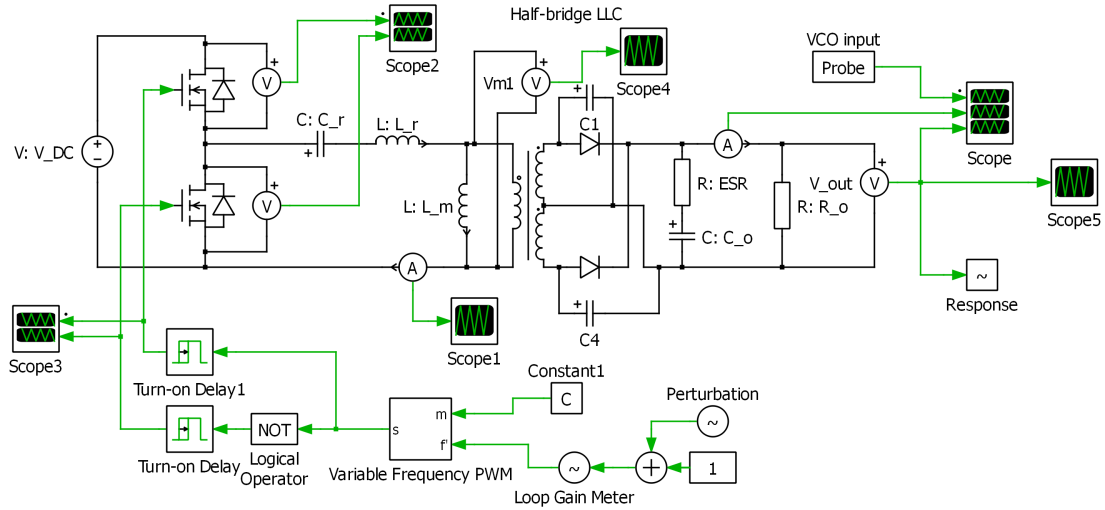


Figure 4.6: Simulation schematic used in the frequency sweep analysis.

The corresponding schematic is shown in Figure 4.6, while the script was employed to automate the frequency sweep across the full operating range of the LLC converter under constant full-load operation at 1 kW, Appendix A.6. This analysis was performed for multiple input voltages (450 V, 500 V, 550 V, and 600 V), allowing a direct comparison of the output voltage behavior under varying supply conditions.

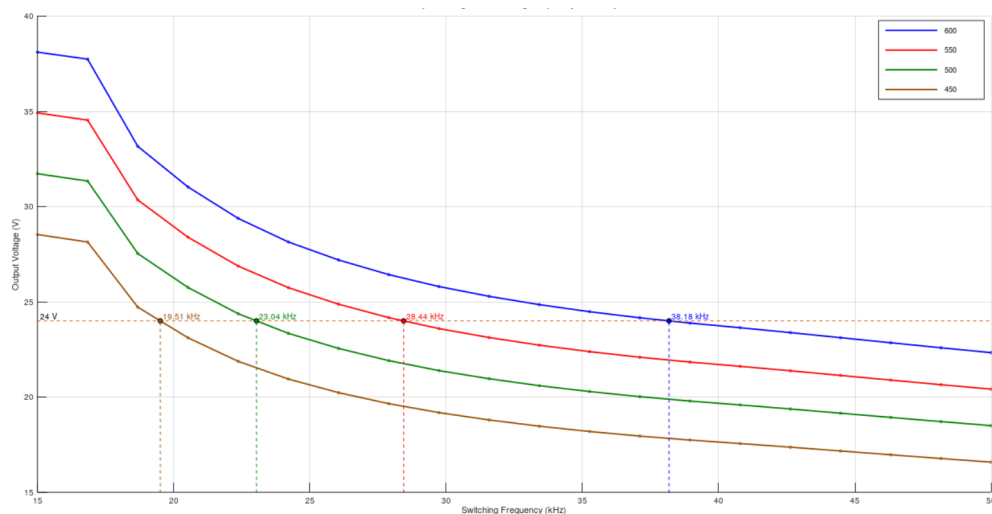


Figure 4.7: LLC output voltage vs. switching frequency for different input voltages at 1 kW load.

The resulting plot, shown in Figure 4.7, presents four distinct curves corresponding to each input voltage level. For each curve, the intersection with the 24 V reference line indicates the switching frequency required to achieve regulated output operation. These results provide valuable insight into the converter's sensitivity to input voltage variations and the corresponding adjustment range necessary for the control system.

#### 4.2.2 Close-loop analysis

In this approach, the converter's output voltage is continuously monitored and used as the feedback input to a PI controller. Based on the voltage error, the PI controller dynamically adjusts the switching frequency of the converter to regulate and stabilize the output voltage. This method ensures a reliable and steady output across the entire operating range of input voltages and output power levels. The complete schematic of the LLC converter used in the simulation is shown below, in Figure 4.8.

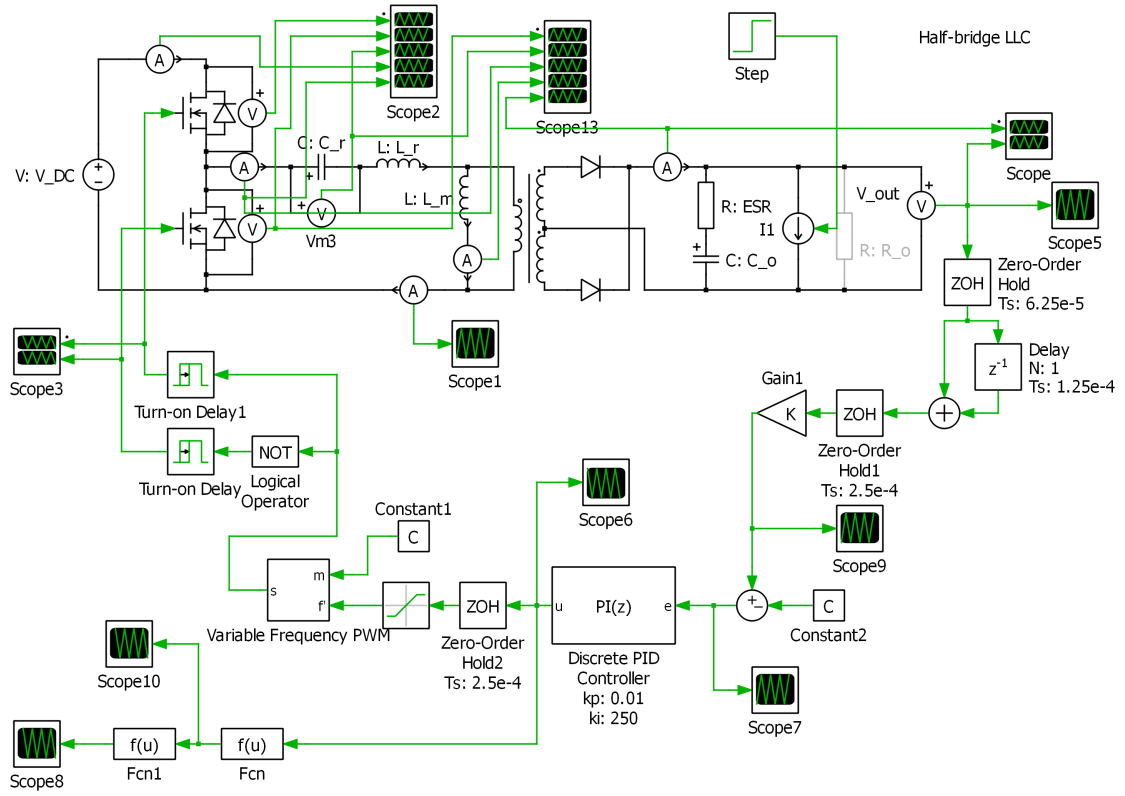


Figure 4.8: Simulation schematic used in closed-loop analysis.

To ensure that the simulation environment closely represents the real implementation, particular attention was given to the sampling process of the data acquisition system and the control loop frequency. This consideration is important, as in practical applications, the performance and stability of the control loop strongly depend on the relationship between the sampling rate, the control update rate, and the switching frequency of the power converter.

In this simulation, the data acquisition was performed at a sampling frequency of 16 kHz, which corresponds to four times the control loop frequency. To comply with the Nyquist theorem and mitigate the influence of high-frequency noise, the sampled values were processed through a simple averaging mechanism. Specifically, two consecutive samples were acquired, summed, and then divided by two, resulting in the mean value of the two readings. This averaging buffer can be mathematically expressed as:

$$i_{\text{mean}}[k] = \frac{i[k] + i[k-1]}{2} \quad (4.8)$$

This filtered value was then used as the effective feedback input for the control loop.

The control loop frequency was established at 4 kHz, which was chosen according to common guidelines in power electronics. Typically, the control loop frequency is set to at least one-tenth of the maximum switching frequency of the converter to balance response speed and stability. Since the resonant LLC converter under study operates within a variable switching frequency range up to 40 kHz, the 4 kHz control loop frequency satisfies this design criterion. From this control

frequency, all other sampling rates in the simulation were derived, ensuring coherence between the digital control implementation and the physical constraints of the converter operation.

The tuning process for the PI controller consisted of starting with default values, which typically apply a unity gain to the proportional path while the integral action is initially disabled. To start the tuning process, the integral gain is set to zero, and the proportional gain is set to one. From this baseline, the proportional gain is gradually adjusted while monitoring the system's step response. This tuning seeks to achieve a desirable trade-off between rise time and overshoot. Once a satisfactory dynamic response is obtained through proportional control, the integral gain can be introduced to correct any steady-state error and ensure the output settles to its nominal value. However, since the integral term significantly affects system stability, it was increased cautiously from a very low initial value. As integral gain tends to increase overshoot and induce oscillations, it may be necessary to fine-tune  $K_p$  again to reach a balanced and stable response.

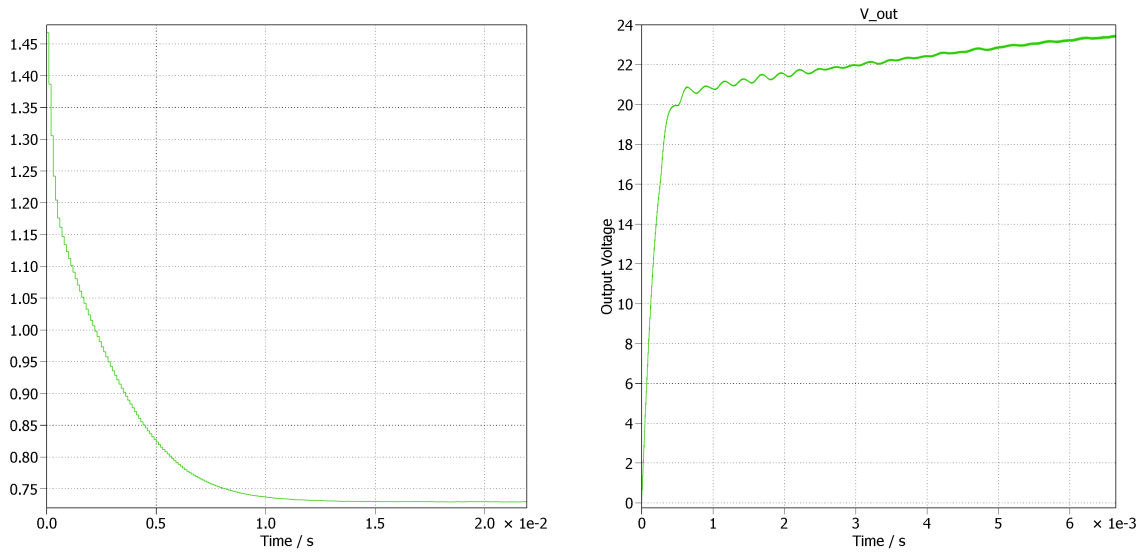
After performing an iterative process of fine-tuning the PI controller to balance transient response and steady-state accuracy, the final gain values were determined. The proportional gain was set to  $K_p = 0.01$ , providing adequate response without introducing excessive overshoot, while the integral gain was chosen as  $K_i = 250$ , ensuring effective correction of steady-state error.

After tuning the PI controller, the simulation results confirmed that the converter operates correctly across a wide range of conditions. The system was tested under various input voltages, from the maximum to the minimum of the specified range, as well as under different load conditions, including load transients and step changes. In all cases, the PI controller demonstrated effective regulation, with the control loop consistently converging to zero error. As a result, the output voltage reliably stabilized at the desired value of 24 V.

The figures presented below illustrate the main operating signals of the resonant converter, including the resonant tank voltage, resonant inductor current, resonant capacitor voltage, magnetizing current, and the output voltage before the rectifier stage. Additional figures show the converter output voltage converging to 24 V during the startup phase while operating initially at half load. Subsequently, a step change in the output current was introduced in the simulation to increase the load to full capacity (1 kW), demonstrating the controller's ability to maintain stable operation and accurate voltage regulation under dynamic load variations.

### 4.2.3 Soft-Start control and startup behavior

The soft-start function is implemented to ensure a controlled startup sequence, preventing large inrush currents and overstressing of the power components during initialization. In this control strategy, the converter starts operating at a switching frequency 1.5 times higher than the resonant frequency, Figure 4.9a, corresponding to a region where the voltage gain is very low. From this point, the switching frequency is gradually decreased, allowing the converter to transition smoothly along the gain curve until it reaches the required operating region. This progressive reduction in frequency enables the output voltage to rise steadily and converge to its steady-state value without overshoot, as can be seen in Figure 4.9b.



(a) Normalized switching-frequency multiplier over time. The converter starts at  $1.5\times$  the resonant frequency and gradually decreases to the steady-state point.

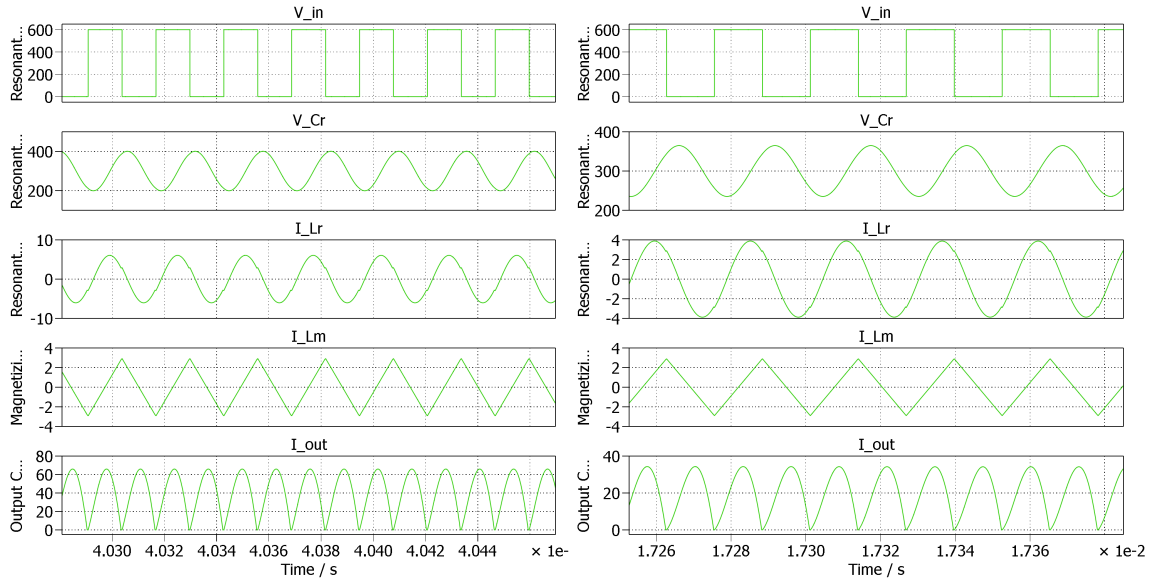
(b) Output voltage during startup.

Figure 4.9: Soft-start simulation of the LLC resonant converter.

#### 4.2.4 Dynamic performance under current step load variation

This simulation highlights the dynamic behavior of the LLC resonant converter when subjected to a sharp step variation in load, from 500 W to 1 kW. The results illustrate the transient response of the main resonant tank variables, as well as the output voltage and current of the converter. As shown in the figures below, the converter maintains stable operation and quickly settles to the new steady-state condition, demonstrating effective regulation and robustness under sudden load changes.

**Simulation:**  $600 V_{bus,max}$  - [500 to 1000] W



(a) The steady-state waveforms at full load (1 kW). (b) The steady-state waveforms at half load (500 W).

Figure 4.10: Simulation results of the LLC resonant converter operating at an input voltage of  $V_{bus} = 600$  V. The figure presents the main resonant tank waveforms, including the tank voltage ( $V_{in}$ ), the resonant capacitor voltage ( $V_{Cr}$ ), the resonant inductor current ( $I_{Lr}$ ), the magnetizing current of the transformer ( $I_{Lm}$ ), and the output current ( $I_{out}$ ). The converter is subjected to a load step, imposed by a change in the output current, from 500 W to 1 kW.

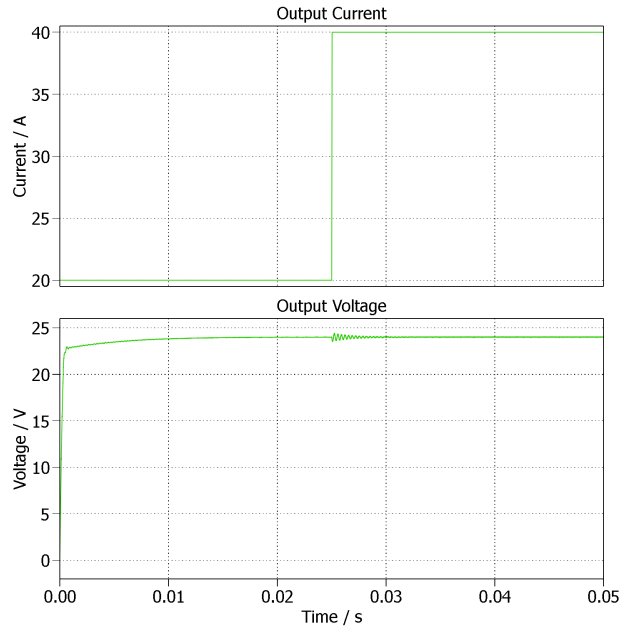
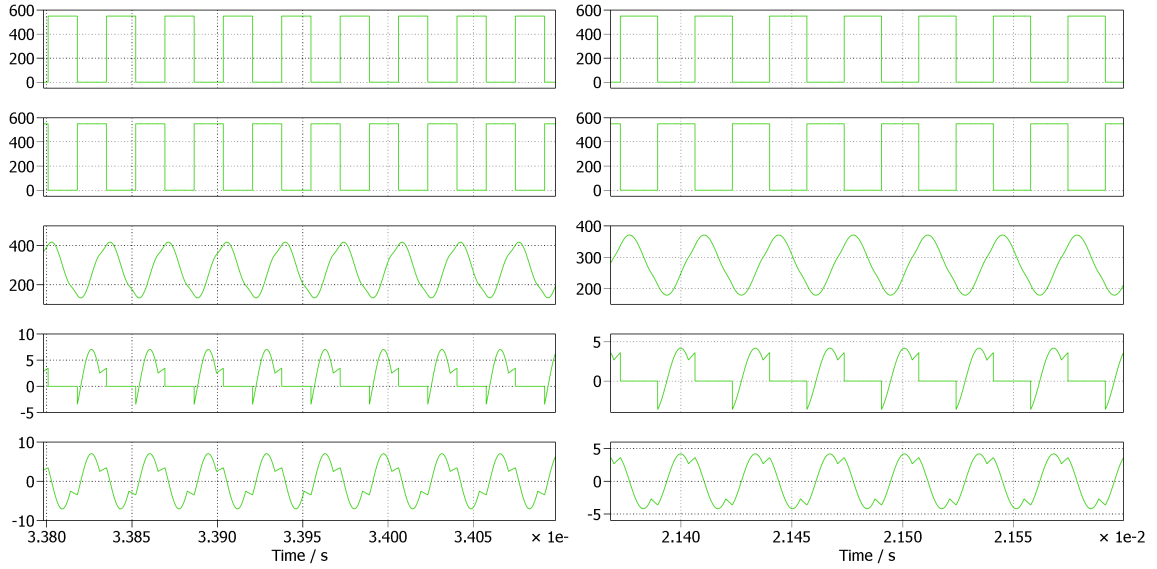


Figure 4.11: Simulation results corresponding to the operating condition of  $V_{bus} = 600$  V.

**Simulation:**  $550 V_{bus,nom}$  - [500 to 1000] W



(a) The steady-state waveforms at full load (1 kW). (b) The steady-state waveforms at half load (500 W).

Figure 4.12: Simulation results of the LLC resonant converter operating at an input voltage of  $V_{bus} = 550$  V. The figure presents the main resonant tank waveforms, including the tank voltage ( $V_{in}$ ), the resonant capacitor voltage ( $V_{Cr}$ ), the resonant inductor current ( $I_{Lr}$ ), the magnetizing current of the transformer ( $I_{Lm}$ ), and the output current ( $I_{out}$ ). The converter is subjected to a load step, imposed by a change in the output current, from 500 W to 1 kW.

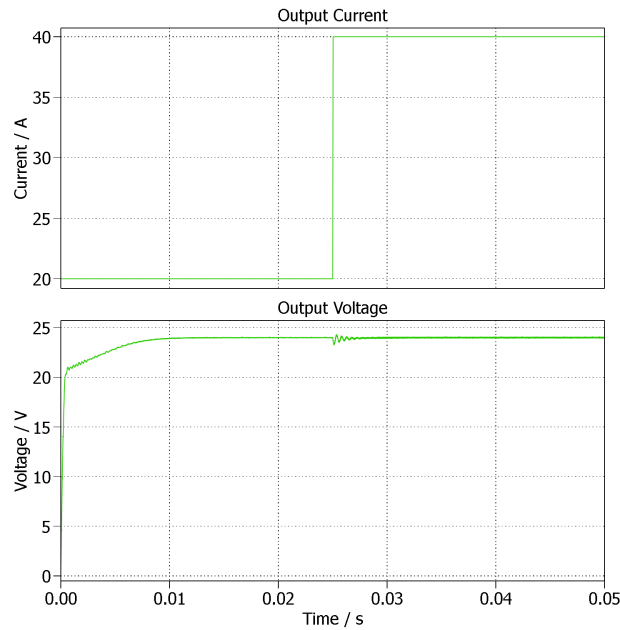
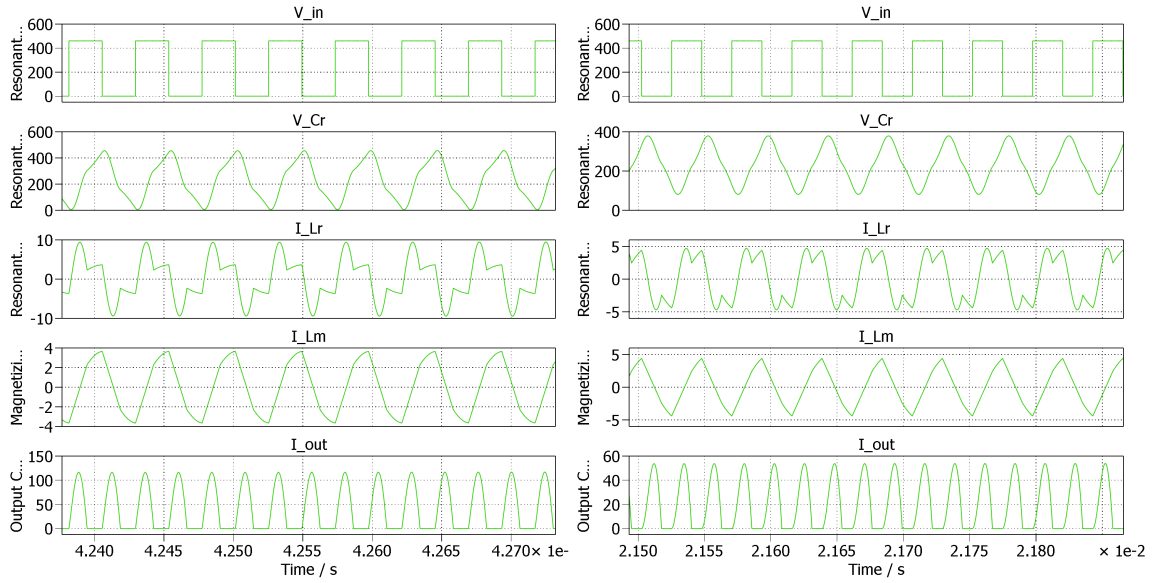


Figure 4.13: Simulation results corresponding to the operating condition of  $V_{bus} = 550$  V.

**Simulation:** 400  $V_{bus,min}$  - [500 to 1000] W



(a) The steady-state waveforms at full load (1 kW). (b) The steady-state waveforms at half load (500 W).

Figure 4.14: Simulation results of the LLC resonant converter operating at an input voltage of  $V_{bus} = 400$  V. The figure presents the main resonant tank waveforms, including the tank voltage ( $V_{in}$ ), the resonant capacitor voltage ( $V_{Cr}$ ), the resonant inductor current ( $I_{Lr}$ ), the magnetizing current of the transformer ( $I_{Lm}$ ), and the output current ( $I_{out}$ ). The converter is subjected to a load step, imposed by a change in the output current, from 500 W to 1 kW.

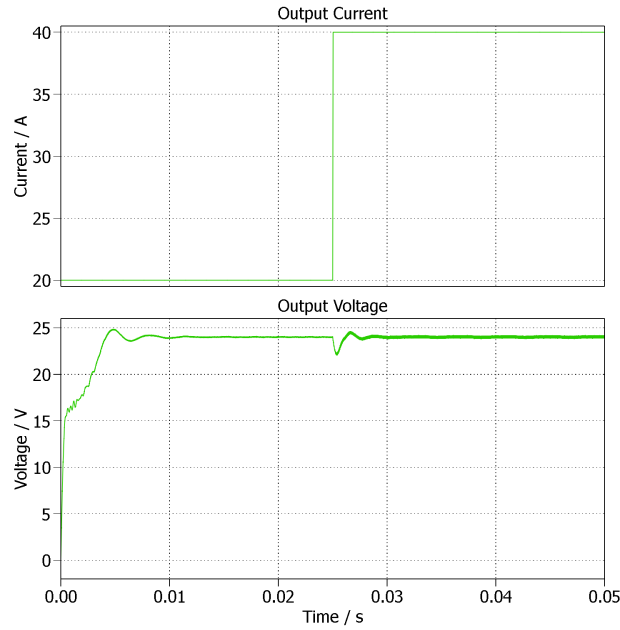


Figure 4.15: Simulation results corresponding to the operating condition of  $V_{bus} = 400$  V.

#### 4.2.5 Efficiency evaluation considering semiconductor losses under resistive load variation

In this simulation, both the dynamic behavior and efficiency of the LLC resonant converter are evaluated under realistic operating conditions. To achieve a more accurate representation of the converter's performance, semiconductor losses from both the MOSFETs and rectifier diodes are included in the model, accounting for conduction and switching effects, Figure 4.16.

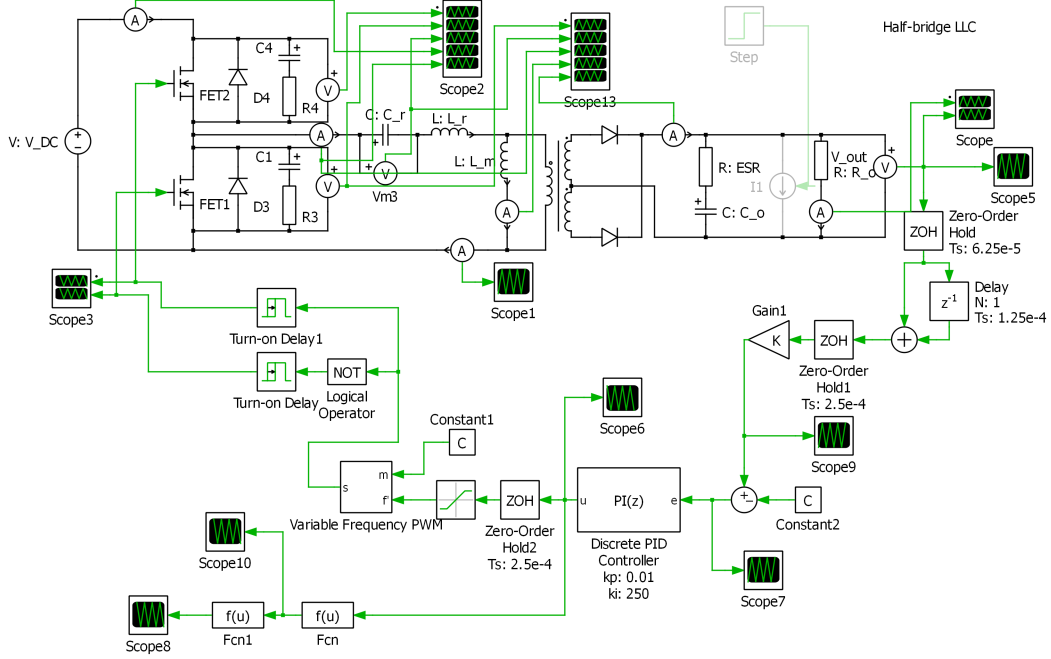


Figure 4.16: Simulation results corresponding to the operating condition of  $V_{bus} = 400$  V.

A continuously varying resistive load is applied to emulate gradual load transitions, allowing the observation of the converter's response to smooth power variations rather than abrupt step changes. This approach provides a more realistic evaluation of the converter's voltage regulation and dynamic stability across its entire operating range.

The results presented in the figures below show the output voltage and current waveforms for the converter operating at *minimum*, *nominal*, and *maximum* input voltages, all corresponding to a 1 kW output load. The quantitative values and performance indicators discussed in the following subsections are derived from these simulation results.

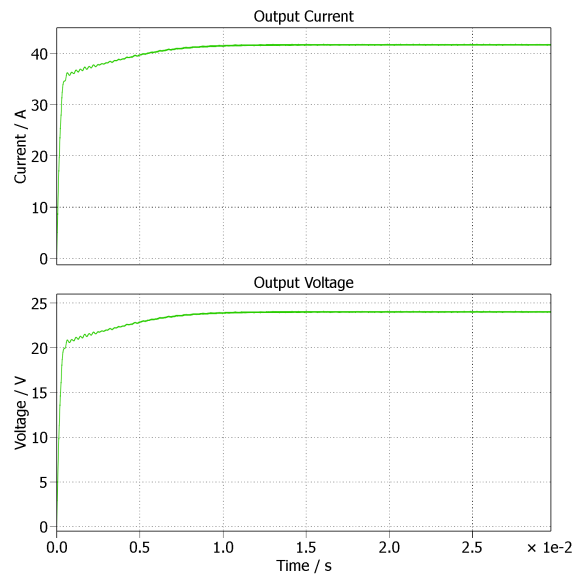


Figure 4.17: Output waveforms (including semiconductor losses) at  $V_{bus} = 600$  V under a 1 kW resistive load. Fast settling with low ripple.

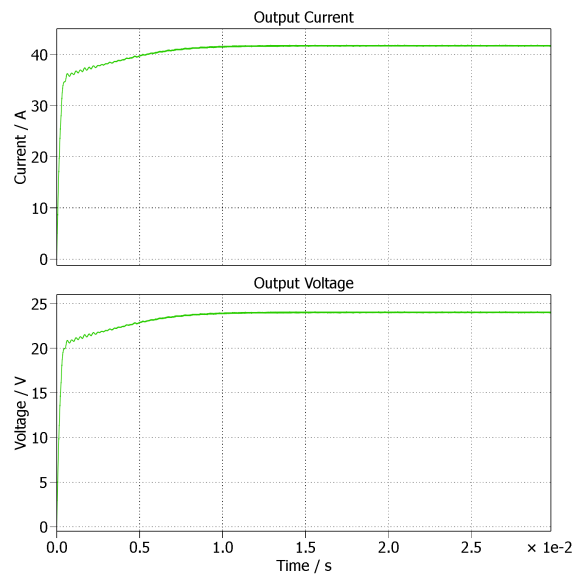


Figure 4.18: Output waveforms (including semiconductor losses) at  $V_{bus} = 550$  V (nominal) under a 1 kW resistive load. Slower rise with stable steady-state regulation.

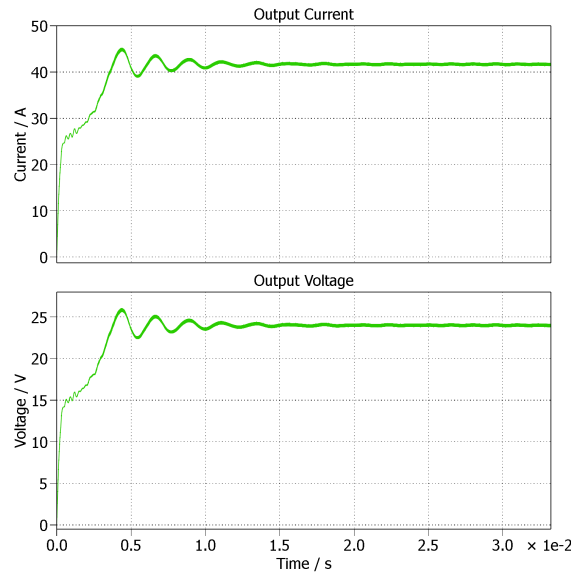


Figure 4.19: Output waveforms (including semiconductor losses) at  $V_{bus} = 400$  V (minimum) under a 1 kW resistive load. Transient overshoot with damped oscillations before settling.

#### 4.2.5.1 Output voltage ripple analysis

The output voltage ripple is analyzed for each operating point to identify the worst-case condition, corresponding to the highest stress on the rectifier stage. This analysis highlights the converter's ability to maintain proper voltage regulation across the full input voltage range, even under the most demanding load scenarios.

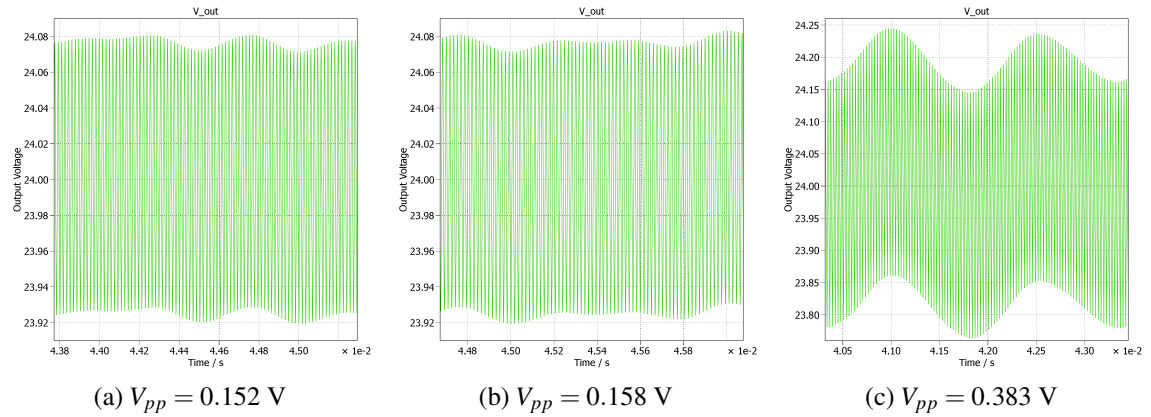


Figure 4.20: Output voltage ripple  $V_{out}$  under a 1 kW resistive load for three input voltages: (a) 600 V (maximum), (b) 550 V (nominal), and (c) 400 V (minimum). Each subfigure shows the zoomed  $V_{out}$  waveform used to evaluate the peak-to-peak voltage ripple.

The results show increased ripple at lower input voltage due to higher current stress and resonant tank deviation from optimal operating conditions.

#### 4.2.5.2 Efficiency results and discussion

The converter efficiency is then calculated considering the semiconductor losses introduced into the model. As shown in Table 4.2, the LLC resonant converter maintains an efficiency above 94% across the entire input voltage range, demonstrating stable and predictable performance under all operating conditions.

Table 4.2: Efficiency analysis of the LLC resonant converter under different input voltages at 1 kW output.

| $V_{bus}$ [V] | $I_{in}$ [A] | $P_{in}$ [W] | $V_{out}$ [V] | $I_{out}$ [A] | $P_{out}$ [W] | Losses [W] | $\eta$ [%] |
|---------------|--------------|--------------|---------------|---------------|---------------|------------|------------|
| 600           | 1.7559       | 1053.54      | 24.0009       | 41.6683       | 1000.08       | 53.46      | 94.93      |
| 550           | 1.9155       | 1053.53      | 24.0006       | 41.6715       | 1000.12       | 53.41      | 94.93      |
| 400           | 2.6551       | 1062.02      | 24.0138       | 41.6907       | 1001.15       | 60.87      | 94.27      |

The slight reduction in efficiency observed at lower input voltages is mainly attributed to increased conduction losses, as the input current rises to maintain the same output power level.

Additionally, part of the total losses is associated with the incomplete achievement of ZVS across the full operating range. While ZVS is successfully achieved in most conditions, certain operating regions—particularly at light load or at the lower input voltage boundary exhibit partial or absent ZVS operation.

These effects could be mitigated through a more optimized control strategy or adaptive frequency modulation approach, ensuring that ZVS conditions are maintained throughout the full load range.

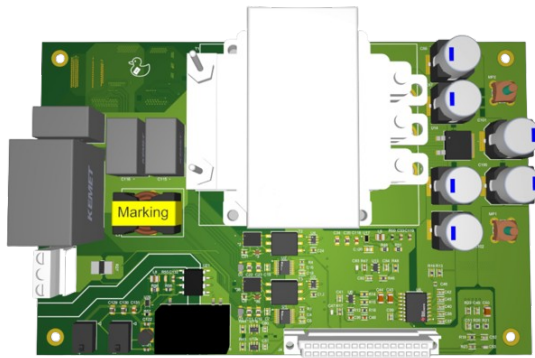
Nevertheless, the converter's efficiency values remain within the expected range for this topology and power level. The results confirm that the designed LLC resonant converter achieves high efficiency, stable voltage regulation, and reliable operation under realistic conditions, validating the effectiveness of both the selected topology and control implementation.

## Chapter 5

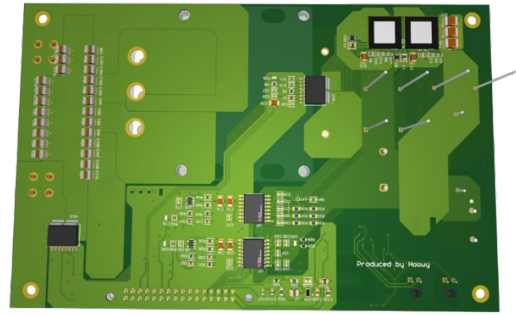
# Experimental Validation and Hardware Testing

### 5.1 PCB overview and layout considerations

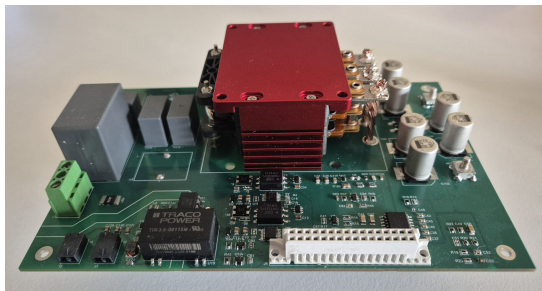
This section summarizes the PCB-level decisions that enable the validated performance of the 600 V, 1 kW half-bridge LLC converter. Rather than detailing every footprint, I focus on the constraints that drove the layout, the implementation tactics used, and the measured outcomes that verify those choices. Full schematics, layer plots, and the manufacturing package are provided in Appendix [A.8](#).



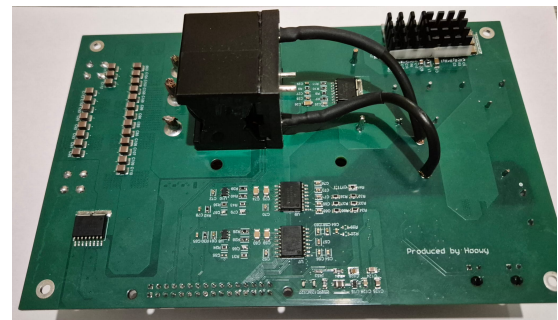
Front (component) side.



Back side.



PCB prototype front side.



PCB prototype back side.

Figure 5.1: Assembled PCB, front and back views, illustrating the four-layer implementation and the separation between low-voltage/control and high-voltage power regions.

The printed-circuit board was deliberately kept simple and designed following standard high-frequency power-layout practices. It uses a four-layer stack-up. While the stack is consistent across the board, the layer functions vary by region. On the high-voltage input side, Layers 1 and 4 carry power, as external layers can handle higher currents for equal track widths. In contrast, Layers 2 and 3 serve as ground/signal planes, ensuring that high  $di/dt$  paths always reference an adjacent ground. On the high-voltage output side, the layers are arranged symmetrically to share the rectifier current among the top, inner, and bottom power planes. Creepage, clearance, and minimum polygon spacing comply with IPC-2221 standards.

Galvanic isolation is maintained throughout: sensing, communication, and bias domains are isolated from the vehicle ground, and the low-voltage ground is kept separate from the two power grounds (high-side and low-side) of the power stage. Logic buffers were added on the PWM signal paths to the GaN gate driver stages to ensure clean and well-defined switching edges. Although the selected GaN devices have limited voltage margins, careful PCB layout practices were implemented to minimize parasitic inductance and ringing in the half-bridge stage. The positive switching node is on the top layer and the corresponding return plane is directly beneath it. This minimized the loop area and inductance, thereby reducing overshoot, ground bounce, and other signal integrity issues during high-speed switching transitions.

## 5.2 PCB Bench Testing and Validation

Before proceeding to the practical validation of the converter, several preparatory steps were carried out to ensure safe and reliable testing conditions. The main objectives of these initial tests were to validate the functionality of the low-voltage supply, confirm the correct operation of the sensing circuits, and verify the converter behavior both with and without the PWM control signals applied. Additionally, load tests were planned to assess the converter's response under different operating conditions.

For control and monitoring, an *Infineon XMC4500 Relax Kit* microcontroller board was used, [3], programmed to generate the required PWM signals and execute the control algorithm. The system was integrated with the *Micrium* real-time operating environment, which allowed live interaction with the control variables and real-time observation of the system behavior during testing.

This setup enabled step-by-step verification of the converter's critical functionalities prior to full-power operation, ensuring that each subsystem supply, sensing, control, and power stage performed as expected and provided a stable foundation for subsequent experimental validation.

### 5.2.1 Test Preparation and Experimental Setup

Before performing the practical validation of the converter, a set of preparatory steps was carried out to ensure safe and reliable testing conditions. The main objectives of these initial tests were to:

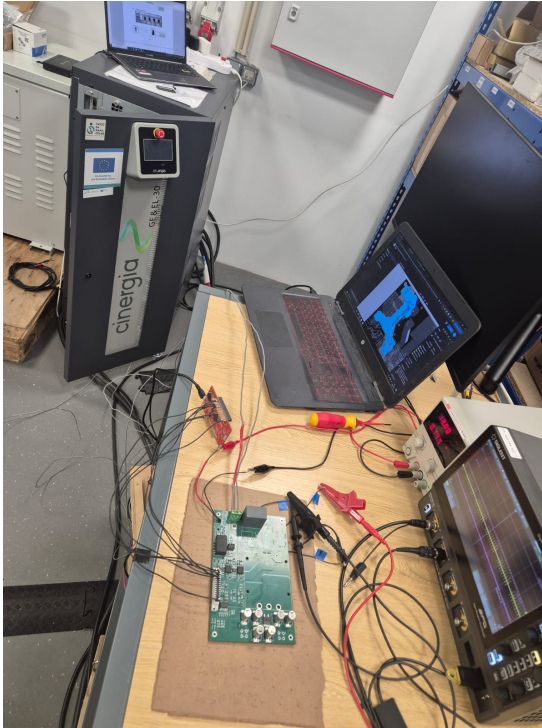
- Validate the correct operation of the low-voltage (LV) auxiliary supply;
- Verify the integrity and accuracy of the sensing circuits;
- Check the converter's electrical behavior both with and without the PWM control signals applied;
- Prepare load tests to evaluate the converter's response under different operating conditions.

For control and monitoring, an *Infineon XMC4500 Relax Kit* microcontroller board, [3], was used to generate the required PWM signals and execute the implemented control algorithm. The firmware was developed and tested using the *Micrium* real-time operating environment, which enabled live observation of control variables and direct interaction with the system during testing. This allowed parameter tuning and verification of control behavior in real time, facilitating rapid debugging and validation.

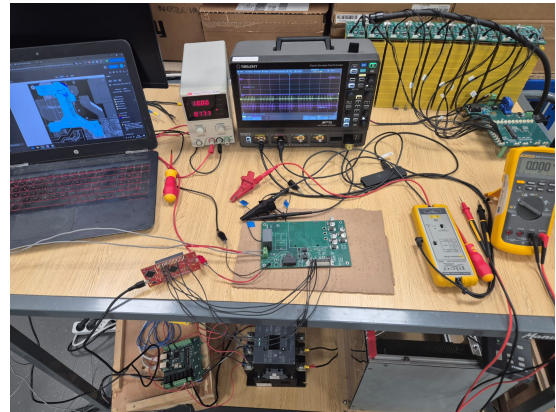
The experimental setup, shown in Figure 5.2, was arranged on an isolated test bench to ensure operator safety and signal integrity. The setup included:

- A programmable power source to emulate the high-voltage (HV) DC bus;
- A precision digital oscilloscope for waveform monitoring;
- A laboratory DC supply to power the control and sensing circuitry;

- The *XMC4500* controller board connected to the converter PCB.



(a) Side view of the laboratory setup showing the power source and control instrumentation.



(b) Front view of the test bench with the converter PCB, oscilloscope, LV supply, and *XMC4500* control board.

Figure 5.2: Experimental bench setup used for low-voltage validation and converter functional testing.

### 5.2.2 Low-Voltage Validation and Functional Verification

After assembling the prototype, the converter underwent several low-voltage bench tests to validate its electrical and control functionalities prior to high-voltage operation. The main focus of these tests was to ensure proper startup sequencing, confirm correct gate-drive timing and PWM signal integrity, and validate that all measurement channels responded accurately. Tests were initially conducted without activating the PWM signals to verify static behavior and circuit safety, followed by active switching tests to confirm signal synchronization and control loop behavior.

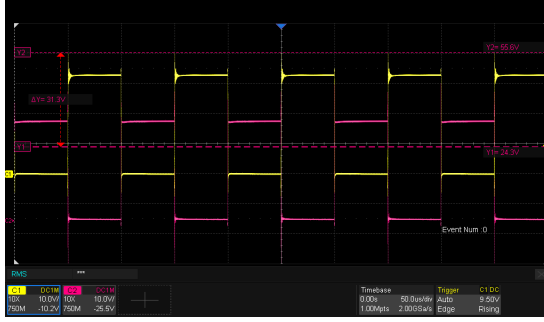
Throughout the tests, the control variables were monitored through the *Micrium* interface, allowing real-time inspection of the converter's performance.

## 5.3 Experimental Results

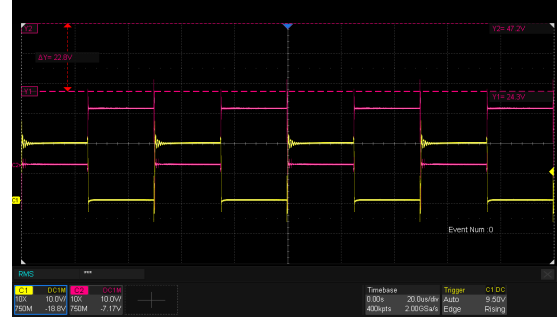
### 5.3.1 No-Load Test

After validating the low-voltage and sensing stages, the converter was subjected to a series of progressive electrical tests. Initially, the input voltage was applied without activating the switching

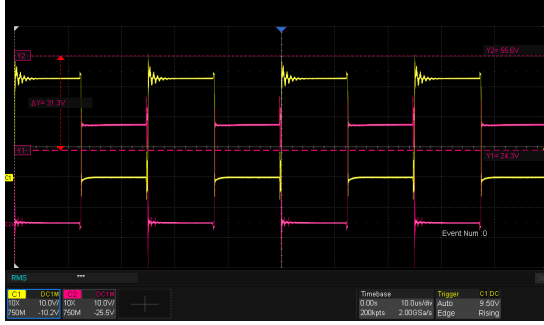
stage to confirm the correct operation of the power supply, sensing feedback, and protection circuitry. Once these checks were successfully completed, the converter was tested under switching conditions with the *GaN* transistors operating at no-load to evaluate gate-drive behavior, signal synchronization, and switching waveform integrity. The results of these switching tests are presented in the figures below.



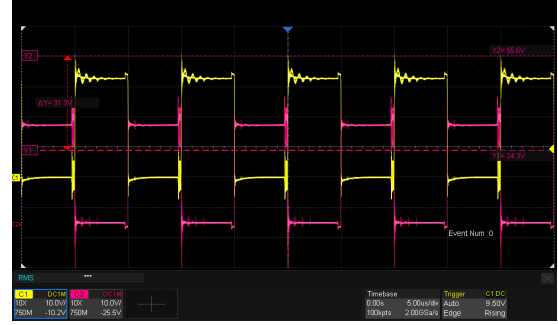
(a) Zoom on switching edges at 50  $\mu\text{s}/\text{div}$ ;  $\sim 31\text{ V}_{pp}$  gate swing indicated.



(b) Complementary GaN gate signals (CH1/CH2). Overview at 20  $\mu\text{s}/\text{div}$ .



(c) Closer view at 10  $\mu\text{s}/\text{div}$  highlighting edge ringing and dead-time region.



(d) Fine zoom at 5  $\mu\text{s}/\text{div}$  showing damped oscillations after transitions.

Figure 5.3: Oscilloscope captures of the complementary PWM/gate signals driving the GaN half-bridge. The yellow trace corresponds to the *upper (high-side)* GaN gate signal, and the magenta trace corresponds to the *lower (low-side)* GaN gate signal. Subfigures use different time bases to illustrate the overall period, switching edges, ringing, and dead-time behavior.

All validation steps confirmed the correct functionality of the sensing, control, and power circuits, providing confidence for the transition to start power testing.

### 5.3.2 Initial Load Testing and Transformer Behavior

During the load testing phase, the converter was operated under nominal load conditions to evaluate its performance. However, abnormal behavior was observed, leading to a failure caused by transformer core saturation.

The issue was traced to the operating frequency range of the converter, set between 20 kHz and 40 kHz (Table 4.1), which was significantly lower than the transformer's nominal design frequency of 100 kHz as specified in the manufacturer's datasheet.

Operating at such reduced switching frequencies resulted in longer magnetization intervals during each switching cycle. Consequently, the magnetic flux in the core accumulated without sufficient time to reset, progressively driving the transformer into magnetic saturation. This condition led to a sharp increase in the magnetizing current, imposing excessive electrical and thermal stress on the converter components.

To prevent potential hardware damage, the test was immediately stopped, and the cause was confirmed to be directly related to the mismatch between the actual operating frequency and the transformer's intended design frequency.

### 5.3.3 Steady-State Operation and Performance Evaluation

Following this observation, it was concluded that the resonant tank design of the converter would not perform as originally intended, since the transformer could not operate effectively within the designed frequency range. The core characteristics and construction limited its ability to sustain flux variations at frequencies significantly below its nominal specification.

Considering this constraint, a new test was conducted with the converter operating at a fixed switching frequency of 100 kHz, corresponding to the transformer's nominal design point. The purpose of this test was to validate the overall operation of the converter and verify its functional behavior under realistic switching conditions, even though this frequency does not correspond to the ideal resonant operating region of the LLC topology.

The test was conducted under the following conditions:

- Input voltage,  $V_{\text{BUS}} = 100 \text{ V}$
- Load resistance,  $R_{\text{load}} = 1 \Omega$
- Switching frequency,  $f_{\text{sw}} = 100 \text{ kHz}$
- Output voltage,  $V_{\text{out}} = 3.2 \text{ V}$  (expected)

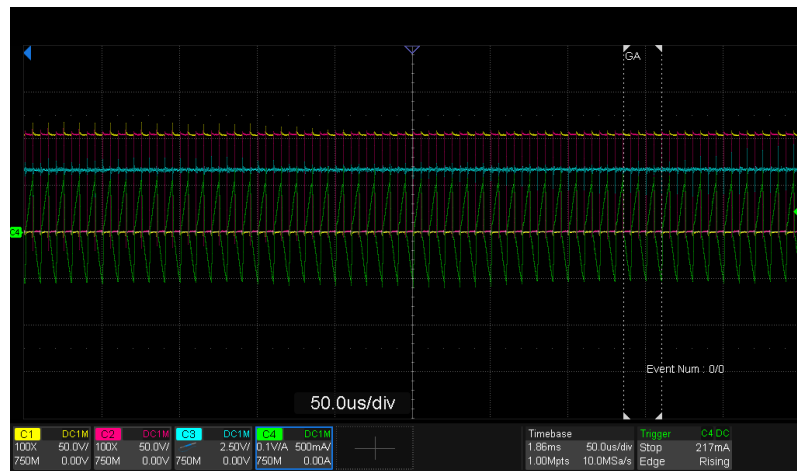
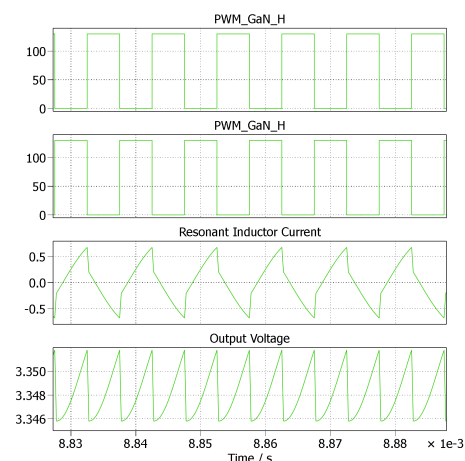
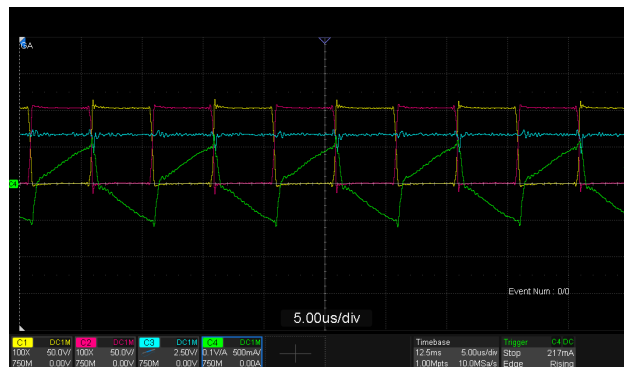


Figure 5.4: Experimental waveforms of the half-bridge LLC converter at 100 kHz switching frequency.



(a) Simulation Waves.



(b) Experimental waveforms obtained during bench testing. The yellow and magenta traces represent the switching nodes of the GaNs, the blue trace corresponds to the output voltage, and the green trace represents the resonant inductor current.

Figure 5.5: Comparison between simulated and experimental waveforms of the half-bridge LLC converter under the same operating conditions.

As shown in the figures above, the converter operated as expected, demonstrating behavior consistent with the simulation results. Under this configuration, the system exhibited the correct resonant inductor current waveform, proper semiconductor switching behavior, and the expected output voltage. These results confirm that, even though the test was performed outside the ideal resonant region, the converter maintained stable and predictable operation, validating the functionality of the overall design.

## Chapter 6

# Conclusions and Future Work

### 6.1 Conclusions

This dissertation presents the design, modeling, simulation, and experimental validation of an isolated 600 V to 24 V, 1 kW half-bridge LLC resonant DC/DC converter developed for the Formula Student FSFEUP electric vehicle. The converter was designed to comply with FSG safety rules, which require galvanic isolation between the high-voltage accumulator and the low-voltage system.

From a theoretical and design perspective, the converter fully meets all the functional and performance requirements. The analytical modeling, based on the FHA, involved the design of the resonant tank, component selection, control system, and PCB layout, all carried out according to standard and reliable engineering methodologies. Simulation results confirmed the expected performance, demonstrating correct resonant operation, high efficiency, and proper control behavior across all operating conditions.

In practice, however, the main challenge encountered was finding or manufacturing a transformer capable of meeting the full operational frequency range required by the converter. Although all theoretical analysis and simulations validated the design, the experimental prototype could not operate as intended because the transformer core reached saturation at the designed switching frequency range. This limitation prevented the converter from delivering its rated power and constrained its operational verification.

Despite these hardware limitations, the results still confirm that the converter design, control, and implementation methodology are correct and robust. The sensing, control, and protection systems functioned as expected, and the PCB design showed appropriate signal integrity and low parasitics. This demonstrates that the foundation of the converter design is solid, with the transformer being the only critical component preventing full operation.

Given the insights gained, a different design approach could be adopted in future iterations. Designing the converter for a resonant gain of one, operating at a fixed switching frequency, in its resonant frequency, would simplify the transformer requirements and allow easier component sourcing, even at the cost of some performance optimization. This trade-off would address one

of the main challenges encountered in this work: the limited availability of suitable magnetic components for wide frequency ranges in the market.

Although the final goal of achieving a fully operational, independent DC/DC converter ready for vehicle integration was not accomplished, this project established a comprehensive theoretical, analytical, and simulation framework that can be directly reused and improved upon. The methodology, parameter design process, and control strategy provide a strong foundation for future Formula Student teams or any engineer aiming to design high-voltage isolated converters.

In summary, the work demonstrates theoretical correctness, validated simulations, and complete control implementation, confirming that this thesis represents a significant technical contribution to the field of automotive power electronics and serves as a reference platform for future functional prototypes.

## 6.2 Future Work

For future work, the most evident step, given the solid design basis already established, would be to select or design a transformer capable of operating efficiently within the frequency range defined for this converter. Alternatively, it may be appropriate to redesign both the resonant tank and transformer to achieve the intended gain and operational behavior. Another possible approach would be to reconfigure the resonant tank to operate with a unitary gain across the entire range, accepting output voltage variations proportional to the input voltage. In such a configuration, output stabilization could be ensured through an additional post-regulation stage, implemented by a secondary converter if necessary.

Another important point for future development, with the sensing and measurement system already implemented and functioning correctly, future iterations could also focus on refining the control strategy. A more advanced controller could be developed to guarantee ZVS across the entire operating range and to improve the transient response of the converter.

Once the control strategy is validated in simulation, the next logical step would be the integration of a dedicated control board within the converter assembly. The existing design already provides a control connector and interface for this purpose, allowing a custom PCB to be connected directly to the converter. This board would perform all control and monitoring functions, achieving a compact and integrated converter system ready for installation in the Formula Student vehicle.

Ultimately, the DC/DC converter developed in this dissertation should not be regarded as a fixed or final solution. Instead, it represents a foundation for continuous improvement and innovation. The design methodology, analytical modeling, and modular hardware architecture presented here provide a robust platform upon which future iterations can build. Each development cycle can refine both the hardware and the control system, adapting to new efficiency targets, safety requirements, and technological advances. In this sense, the converter is not the endpoint of the design process but rather a starting point and stimulus for ongoing engineering progress within the field of automotive power electronics.

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# Appendix A

## Appendices

### A.1 Comprehensive LLC Converter Design and Analysis Script

MATLAB script for full LLC resonant converter analysis. It was used to design the LLC converter based on the parameters defined for this project.

```
1 % LLC Resonant Converter Design Script
2
3 clc;
4 clear;
5
6 %% ===== INPUT PARAMETERS =====
7 V_in_nom = 600; % Nominal input voltage [V]
8 V_in_min = 400; % Minimum input voltage [V]
9 V_in_max = 600; % Maximum input voltage [V]
10
11 V_out_nom = 24; % Nominal output voltage [V]
12 I_out = 1000/24; % Maximum output current [A]
13
14 V_f = 0.7; % Diode forward drop [V]
15 V_loss = 1.05; % Other voltage losses [V]
16
17 n_ps = 12; % Turns ratio
18
19 f_res = 100e3; % Resonant frequency [Hz]
20 Ln = 7; % Lm/Lr ratio
21
22 V_pk_pk = 0.24; % 1% of the desired output
23 eff = 0.9; % efficiency
24
25
26
27 %% ===== LLC Gain Range =====
```

```

28 M_G_min = (n_ps * (V_out_nom + V_f)) / (V_in_max / 2);
29 M_G_max = (n_ps * (V_out_nom + V_f + V_loss)) / (V_in_min / 2);
30
31 %% ===== Maximum Quality Factor =====
32 num = sqrt(1 + Ln * (1 - (1/(2*n_ps*(V_out_nom/V_in_min))^2)));
33 den = Ln * sqrt(((2*n_ps*(V_out_nom/V_in_min))^2) - 1);
34 Qe = num / den;
35
36 %% ===== Equivalent Load Resistance at Full Load =====
37 R_eq = (8 / pi^2) * (n_ps^2) * (V_out_nom / I_out);
38
39 %% ===== Resonant Tank Parameters =====
40 C_r = 1 / (2 * pi * f_res * Qe * R_eq); % [F]
41 L_r = 1 / ((2 * pi * f_res)^2 * C_r); % [H]
42 L_m = Ln * L_r; % [H]
43
44 %% ===== Resonant Circuit Design Check =====
45 L_r_new = 33 * 10^-6; % [H]
46 C_r_new = 81 * 10^-9; % [F]
47 L_m_new = 220 * 10^-6; % [H]
48
49 f_res_check = 1 / (2 * pi * sqrt(L_r_new * C_r_new)); % [Hz]
50 L_n_new = L_m_new / L_r_new;
51 Qe_full = sqrt(L_r_new / C_r_new) / R_eq;
52 Qe_110 = sqrt(L_r_new / C_r_new) / (R_eq / 1.1);
53
54 %% ===== Normalized Frequencies =====
55 f_sw_max = 1 * f_res_check;
56 f_sw_min = 0.4776 * f_res_check;
57
58 %% ===== Primary Side Currents =====
59 I_o_110 = 1.1 * pi * I_out;
60 I_OE = I_o_110 / (n_ps * 2 * sqrt(2));
61 I_M_aux = (2 * sqrt(2)) / pi;
62 I_M_fmin = (I_M_aux * (V_out_nom * n_ps)) / (2 * pi * f_sw_min * L_m);
63 I_R_total_fmin = sqrt(I_OE^2 + I_M_fmin^2);
64
65 I_M_fmax = (I_M_aux * (V_out_nom * n_ps)) / (2 * pi * f_sw_max * L_m);
66 I_R_total_fmax = sqrt(I_OE^2 + I_M_fmax^2);
67
68 %% ===== Secondary Side Currents =====
69 I_OES = n_ps * I_OE;
70 I_WS = (sqrt(2) * I_OES) / 2;
71 I_SAV = (sqrt(2) * I_OES) / pi;
72

```

```

73 %% ===== Resonant Inductor AC Voltage =====
74 V_LR_fmax = 2 * pi * f_sw_max * L_r_new * I_R_total_fmax;
75 V_LR_fmin = 2 * pi * f_sw_min * L_r_new * I_R_total_fmin;
76
77 %% ===== Resonant Capacitor AC Voltage =====
78 V_CR_fmin = I_R_total_fmin / (2 * pi * f_sw_min * C_r_new);
79 V_CR_fmax = I_R_total_fmax / (2 * pi * f_sw_max * C_r_new);
80
81 V_CR_rms_fmin = sqrt((V_in_max / 2)^2 + V_CR_fmin^2);
82 V_CR_rms_fmax = sqrt((V_in_max / 2)^2 + V_CR_fmax^2);
83
84 V_CR_peak_fmin = (V_in_max / 2) + sqrt(2) * V_CR_fmin;
85 V_CR_peak_fmax = (V_in_max / 2) + sqrt(2) * V_CR_fmax;
86
87 V_CR_valley_fmin = (V_in_max / 2) - sqrt(2) * V_CR_fmin;
88 V_CR_valley_fmax = (V_in_max / 2) - sqrt(2) * V_CR_fmax;
89
90 %% ===== MOSFET Ratings =====
91 V_MOSFET = 1.2 * V_in_max;
92 I_MOSFET = 1.1 * I_R_total_fmin;
93
94 %% ===== ZVS Design =====
95 C_eq = 250 * 10^-12; % [F]
96 I_m_min = (0.901 * n_ps * V_out_nom) / (2 * pi * f_res * L_m_new); % [A],
    worst-case minimum magnetizing current
97 E1 = 0.5 * (L_m_new + L_r_new) * (sqrt(2) * I_m_min)^2; % [J]
98 E2 = 0.5 * (2 * C_eq) * (V_in_nom)^2; % [J]
99 t_dead = n_ps * C_eq * f_res * L_m_new; % [s]
100
101 %% ===== Rectifier Diode Ratings =====
102 V_diode = ((V_in_max / 2) / n_ps) * 2;
103 I_diode = I_SAV;
104
105 %% ===== Output Capacitors =====
106 dc = V_out_nom / (V_in_min * eff);
107 C_MIN = (I_out * dc * (1-dc) * 1000) / (f_sw_min * V_pk_pk); % Capacitance
    [F]
108
109 I_rect = (I_out * pi) / (2 * sqrt(2)); % rectifier's full-wave output
    current
110 I_cap_rms = sqrt(I_rect^2 - I_out^2); % capacitor's RMS current rating at
    about 100 kHz
111 ESR_max = V_pk_pk / (pi * (I_out / 2)); % Example ESR [ohms]
112
113 polymer_cap = 330 * 1e-6; % cap capacitance [F]

```

```

114 n_polymer_cap = 5; % number of cap in parallel
115 ESR_cap = 12 * 1e-3; % ESR polymer capacitor rating [ohms]
116 I_Ripple_cap = 5; % Ripple current polymer capacitor rating [A]
117
118
119 %% ===== Display Results =====
120 fprintf('---_LLC_Converter_Design_Summary_---\n');
121 fprintf('Turns_ratio_(Np/Ns):_%.2f\n', n_ps);
122 fprintf('Gain_Range:_M_G_min=_%.3f_|_M_G_max=_%.3f\n', M_G_min, M_G_max)
    ;
123 fprintf('Quality_factor_max_(Qe):_%.3f\n', Qe);
124 fprintf('Equivalent_Load_Resistance:_%.2f_Ohm\n', R_eq);
125 fprintf('Resonant_Capacitor:_%.2f_nF\n', C_r * 1e9);
126 fprintf('Resonant_Inductor:_%.2f_uH\n', L_r * 1e6);
127 fprintf('Magnetizing_Inductor:_%.2f_uH\n', L_m * 1e6);
128
129 fprintf('\n---_Verify_the_Resonant-Circuit_Design_---\n');
130 fprintf('Resonant_Capacitor:_%.2f_nF\n', C_r_new * 1e9);
131 fprintf('Resonant_Inductor:_%.2f_uH\n', L_r_new * 1e6);
132 fprintf('Magnetizing_Inductor:_%.2f_uH\n', L_m_new * 1e6);
133 fprintf('Quality_factor_full_load:_%.3f\n', Qe_full);
134
135 fprintf('Switching_Freq:_Min=_%.1f_kHz_|_Max=_%.1f_kHz\n', f_sw_min ,
    f_sw_max);
136 fprintf('RMS_Primary-Side_load_current:_%.3f_A\n', I_OE);
137 fprintf('RMS_Magnetizing_Current_(Im):_fmax=_%.3f_A,_fmin=_fmax=_%.3f_A
    \n', I_M_fmax, I_M_fmin);
138 fprintf('Resonant_Tank_Current_(Total):_fmax=_%.3f_A,_fmin=_%.3f_A\n',
    I_R_total_fmax, I_R_total_fmin);
139 fprintf('Secondary-Side_RMS_load_current_(Total):_%.3f_A\n', I_OES);
140 fprintf('TransformerSs_center-tapped,_current_of_each_winding:_%.3f_A\n',
    I_WS);
141
142 fprintf('\n---_Select_the_Resonant_Inductor_---\n');
143 fprintf('Series_resonant_inductance_(Lr):_%.1f_uH\n', L_r_new * 1e6);
144 fprintf('Rated_current_(I_Lr):_%.1f_A\n', I_R_total_fmin);
145 fprintf('Terminal_AC_voltage:_(V_Lr):_fmax=_%.1f_V,_fmin=_%.1f_V\n',
    V_LR_fmax, V_LR_fmin);
146
147 fprintf('\n---_Select_the_Resonant_Capacitors_---\n');
148 fprintf('Series_resonant_Capacitor_(Lr):_%.1f_nF\n', C_r_new * 1e9);
149 fprintf('Rated_current_(I_Cr):_fmax=_%.1f_A,_fmin=_%.1f_A\n',
    I_R_total_fmax, I_R_total_fmin);
150 fprintf('AC_voltage:_(V_Cr):_fmax=_%.1f_V,_fmin=_%.1f_V\n', V_CR_fmax,
    V_CR_fmin);

```

```

151 fprintf('RMS_voltage:_(V_Cr_RMS):_fmax=_%.1f_V,_fmin=_%.1f_V\n',
        V_CR_rms_fmax, V_CR_rms_fmin);
152 fprintf('Peak_voltage:_(V_Cr_Peak):_fmax=_%.1f_V,_fmin=_%.1f_V\n',
        V_CR_peak_fmax, V_CR_peak_fmin);
153
154 fprintf('\n---_Design_for_ZVS_---\n');
155 fprintf('MOSFET_Rating:_.1f_V/_.2f_A\n', V_MOSFET, I_MOSFET);
156 fprintf('MOSFET_Equivalente_Capacitance:_.1f_pF\n', C_eq * 1e12);
157 fprintf('Worst-Case_Minimum_Magnetizing_Current_(Im_min):_.2f_A\n',
        I_m_min);
158 fprintf('Dead_Time_Should_be_more_than:_.2f_ns\n', t_dead * 1e9);
159
160 fprintf('\n---_Rectifier_Diodes_---\n');
161 fprintf('Output_Diode_Voltage_Rating:_.2f_V\n', V_diode);
162 fprintf('Output_Diode_Current_Rating:_.2f_A\n', I_diode);
163
164 fprintf('\n---_Output_Filter_---\n');
165 fprintf('Output_Cap_Ripple_Current:_.2f_A|_ESR:_.2f_mohms\n', I_cap_rms
        , ESR_max * 1e3);
166 fprintf('Minimum_Ceramic_Capacitance_to_reduce_the_ripple_voltage_to_.2f_
        mVpp_is_.1f_uF\n',V_pk_pk, C_MIN * 1e3);

```

Listing A.1: Comprehensive LLC Converter Design and Analysis Script

## A.2 Sweep of Normalized Inductance $L_n$ at Constant Quality Factor $Q_e$

MATLAB script for plotting gain curves by sweeping normalized inductance  $L_n$  at a fixed quality factor  $Q_e$ . This script visualizes the impact of varying  $L_n$  on the converter's voltage gain across a range of normalized frequencies.

```

1 clc;
2 clear;
3 close all;
4
5 % Parameters
6 Ln = [4, 5, 6, 7, 8, 10]; % Varying m values
7 wx = logspace(-1, 0.5, 10000); % Normalized switching frequency (
        logarithmic scale)
8 colors = ['r', 'g', 'b', 'c', 'm', 'k']; % Colors for the curves
9 Q = 0.25; % Constant Q value
10
11 % Initialize figure
12 figure;

```

```

13 hold on;
14
15 % Loop over m values and plot Gain
16 for y = 1:length(Ln)
17     K=((wx.^2).*(Ln(y)-1))./(((Ln(y)*(wx.^2)-1).^2)+((wx.^2).*(wx.^2)-1)
18         .^2).*(Ln(y)-1).^2.*(Q^2)).^0.5);
19     semilogx(wx, K, 'color', colors(y), 'LineWidth', 2, 'DisplayName', ['Ln
20         _=_' , num2str(Ln(y))]);
21 end
22
23 % Add horizontal lines
24 yline(1.029, '--k', 'LineWidth', 1.5, 'DisplayName', 'y_=1.029');
25 yline(1.672, '--k', 'LineWidth', 1.5, 'DisplayName', 'y_=1.672');
26
27 % Add legend, labels, and title
28 legend('show', 'Location', 'best', 'FontSize', 12);
29 title('|G|(\omega_x) vs \omega_x for Constant Q_e and Varying L_n', '
30     FontSize', 14);
31 xlabel('\omega_x (Normalized Switching Frequency)', 'FontSize', 12);
32 ylabel('|G|(\omega_x) (Gain)', 'FontSize', 12);
33 grid on;
34 xlim([0 2]);
35 hold off;

```

Listing A.2: Sweep of Normalized Inductance  $L_n$  at Constant Quality Factor  $Q_e$ 

### A.3 Sweep of Quality Factor $Q_e$ at Constant Normalized Inductance $L_n$

MATLAB script for plotting gain curves by sweeping quality factor  $Q_e$  at a fixed normalized inductance  $L_n$ . This script visualizes the impact of varying  $Q_e$  on the converter's voltage gain across a range of normalized frequencies.

```

1 clc;
2 clear;
3 close all;
4
5 % Parameters
6 %Q_values = 0.3103; % Varying Q values
7 Q_values = [0.1, 0.2, 0.25, 0.3, 0.35, 0.5, 0.8]; % Varying Q values
8 wx = logspace(-1, 0.5, 10000); % Normalized switching frequency (
9     logarithmic scale)
10 colors = ['r', 'g', 'b', 'c', 'm', 'k']; % Colors for the curves
11 Ln = 6; % Constant K value (ratio of Lp to Ls)

```

```

11
12 % Initialize figure
13 figure;
14 hold on;
15
16 % Loop over Q values and plot Gain
17 for y = 1:6
18     Q = Q_values(y);
19     K=((wx.^2).*(Ln-1))./( (((Ln*(wx.^2)-1).^2)+((wx.^2).*((wx.^2)-1).^2).*(
        Ln-1).^2.*(Q^2)).^0.5);
20     semilogx(wx, K, 'color', colors(y), 'LineWidth', 2, 'DisplayName', ['Qe
        _=' , num2str(Q)]);
21 end
22
23 % Add horizontal lines
24 yline(1.029, '--k', 'LineWidth', 1.5, 'DisplayName', 'y_1.029');
25 yline(1.672, '--k', 'LineWidth', 1.5, 'DisplayName', 'y_1.672');
26
27
28 % Add legend, labels, and title
29 legend('show', 'Location', 'best', 'FontSize', 12);
30 title('|G|(\omega_x)_vs_\omega_x_for_Constant_Ln_and_Varying_Qe', '
        FontSize', 14);
31 xlabel('\omega_x(Normalized_Switching_Frequency)', 'FontSize', 12);
32 ylabel('|G|(\omega_x)_Gain', 'FontSize', 12);
33 grid on;
34 ylim([0 3]);
35 xlim([0 2]);
36 hold off;

```

Listing A.3: Sweep of Quality Factor  $Q_e$  at Constant Normalized Inductance  $L_n$ 

## A.4 Gain Curve Intersection Analysis for LLC Converter at Fixed $Q_e$ and $L_n$

This MATLAB script computes and visualizes the gain curve of an LLC resonant converter by sweeping the normalized switching frequency  $w_x$ , using a fixed  $Q_e$  and  $L_n$ . It highlights the last intersection point with the maximum gain limit  $M_{g\_max}$ , and the second intersection point with the minimum gain limit  $M_{g\_min}$ , both of which define the allowable operating frequency range for maintaining regulation within the inductive region.

```

1 clc; clear; close all;
2
3 % ----- Parameters -----

```

```

4 Q_nom = 0.295; % Q nominal
5 Ln = 7; % L_n (ratio Lm/Lr)
6 wx = logspace(-1, 0.5, 10000); % Normalized switching frequency
7
8 % Curvas a traar: Qe, 0.75Qe e 0.1Qe
9 Q_list = [Q_nom, 0.75*Q_nom, 0.10*Q_nom];
10 leg_labels = { ...
11     sprintf('Qe=%%.3f', Q_nom), ...
12     '0.75Qe', ...
13     '0.1Qe'};
14
15 % Linhas horizontais (ganhos-alvo)
16 target_gain = 1.672; % M_g_max
17 min_gain = 1.029; % M_g_min
18
19 % ----- Figure -----
20 figure; hold on; grid on;
21
22 % Estilos para distinguir as curvas
23 styles = {'-', '--', ':'};
24
25 % Traar as curvas para cada Q
26 for i = 1:numel(Q_list)
27     Qi = Q_list(i);
28
29     % |G|(wx) para LLC
30     Kmag = ((wx.^2).*(Ln-1)) ./ sqrt( (Ln*(wx.^2) - 1).^2 + ...
31         ((wx.^2).*((wx.^2) - 1).^2).*(Ln-1).^2*(Qi^2) );
32
33     semilogx(wx, Kmag, 'LineWidth', 2, ...
34         'LineStyle', styles{1+mod(i-1,numel(styles))}, ...
35         'DisplayName', leg_labels{i});
36
37     if i == 1
38         K_nom = Kmag; % guardar para intersees
39     end
40 end
41
42
43 % ----- Intersees (apenas para Q nominal) -----
44 % M_g_max
45 diff_max = K_nom - target_gain;
46 idx_cross = find(diff_max(1:end-1).*diff_max(2:end) < 0);
47 if ~isempty(idx_cross)
48     idx = idx_cross(end); % ltima interseo

```

```

49     x1 = wx(idx); x2 = wx(idx+1);
50     y1 = K_nom(idx); y2 = K_nom(idx+1);
51     wx_interp_max = x1 + (target_gain - y1)*(x2 - x1)/(y2 - y1);
52     plot(wx_interp_max, target_gain, 'ko', 'MarkerFaceColor', 'y', ...
53         'DisplayName', sprintf('M_{g\_max}_int.:_\omega_x\_approx_.4f',
54             wx_interp_max));
54     fprintf('Intersection_at_Gain=_.3f:_.x_.4f\n', target_gain,
55         wx_interp_max);
55 else
56     fprintf('No_intersection_found_for_Gain=_.3f\n', target_gain);
57 end
58
59 % M_g_min (2 interseo)
60 diff_min = K_nom - min_gain;
61 idx_cross_min = find(diff_min(1:end-1).*diff_min(2:end) < 0);
62 if numel(idx_cross_min) >= 2
63     idx = idx_cross_min(2);
64     x1 = wx(idx); x2 = wx(idx+1);
65     y1 = K_nom(idx); y2 = K_nom(idx+1);
66     wx_interp_min = x1 + (min_gain - y1)*(x2 - x1)/(y2 - y1);
67     plot(wx_interp_min, min_gain, 'ko', 'MarkerFaceColor', 'g', ...
68         'DisplayName', sprintf('M_{g\_min}_2nd_int.:_\omega_x\_approx_.4
69             f', wx_interp_min));
69     fprintf('Second_intersection_at_Gain=_.3f:_.x_.4f\n', min_gain,
70         wx_interp_min);
70 else
71     fprintf('Less_than_2_intersections_found_for_Gain=_.3f\n', min_gain);
72 end
73
74 % ----- Linhas horizontais -----
75 yline(target_gain, '--k', 'LineWidth', 1.5, ...
76     'DisplayName', ['M_{g\_max}_= ', num2str(target_gain)]);
77 yline(min_gain, '--k', 'LineWidth', 1.5, ...
78     'DisplayName', ['M_{g\_min}_= ', num2str(min_gain)]);
79
80 % ----- Labels -----
81 legend('show', 'Location', 'best', 'FontSize', 11);
82 title(sprintf('|G|(\omega_x) vs \omega_x for L_n=_%g and multiple Q_
83     values', Ln), 'FontSize', 14);
83 xlabel('\omega_x (Normalized Switching Frequency)', 'FontSize', 12);
84 ylabel('|G|(\omega_x) (Gain)', 'FontSize', 12);
85 ylim([0 2.5]);
86 xlim([0 2]);
87 hold off;

```

Listing A.4: Gain Curve Intersection Analysis for LLC Converter at Fixed  $Q_e$  and  $L_n$

## A.5 MATLAB Script for LLC Resonant Converter Design and Gain–Frequency Analysis

This MATLAB script sizes and analyzes an LLC resonant converter and then plots its small-signal gain across the switching frequency. From the given specifications (input range of 400–600 V, output of 24 V at approximately 41.7 A, transformer turns ratio  $n_{ps} = 12$ , target resonant frequency  $f_{res} \approx 40$  kHz, and inductance ratio  $L_n = L_m/L_r = 10$ ), it computes the required conversion-gain window  $M_G$  for regulation ( $M_{G,min}$  at  $V_{in,max}$  and  $M_{G,max}$  at  $V_{in,min}$ ), the maximum effective quality factor  $Q_{e,max}$ , the equivalent reflected load  $R_{eq}$ , and the resonant tank parameters ( $L_r, C_r$ ) with a recalculated  $f_{res}$ .

The script also evaluates the effective quality factor at full load and at 75% and 10% load (by scaling  $R_{eq}$  accordingly), and sweeps the normalized frequency  $\omega_x = f/f_{res}$  to generate three gain curves using the chosen  $L_n$  and each  $Q_e$ . The figure overlays horizontal lines corresponding to  $M_{G,min}$  and  $M_{G,max}$  to visualize the regulation window, showing where the converter can operate within the inductive region. Console output summarizes the computed ranges and component values, including the gain limits,  $Q_e$ ,  $R_{eq}$ ,  $C_r$ ,  $L_r$ , and  $f_{res}$ .

```

1 % LLC Resonant Converter Design Script
2
3 clc;
4 clear;
5
6 %% ===== INPUT PARAMETERS =====
7 V_in_nom = 550; % Nominal input voltage [V]
8 V_in_min = 400; % Minimum input voltage [V]
9 V_in_max = 600; % Maximum input voltage [V]
10
11 V_out_nom = 24; % Nominal output voltage [V]
12 I_out = 1000/24; % Maximum output current [A]
13
14 V_f = 0.7; % Diode forward drop [V]
15 V_loss = 2.05; % Other voltage losses [V]
16
17 n_ps = 12; % Turns ratio
18
19 f_res = 40e3; % Resonant frequency [Hz]
20 L_n = 10; % Lm/Lr ratio
21
22 V_pk_pk = 0.24; % 1% of the desired output
23 eff = 0.9; % efficiency
24
25 L_m = 660e-6;
26
27 %% ===== LLC Gain Range =====

```

```

28 M_G_min = (n_ps * V_out_nom) / (V_in_max / 2);
29 M_G_max = (n_ps * V_out_nom) / (V_in_min / 2);
30 %% ===== Maximum Quality Factor =====
31 num = sqrt(1 + Ln * (1 - (1/(2*n_ps*(V_out_nom/V_in_min))^2)));
32 den = Ln * sqrt(((2*n_ps*(V_out_nom/V_in_min))^2) - 1);
33 Qe_max = num / den;
34
35 %% ===== Equivalent Load Resistance at Full Load =====
36 R_eq = (8 / pi^2) * (n_ps^2) * (V_out_nom / I_out);
37
38 %% ===== Resonant Tank Parameters =====
39 L_r = 65*10^-6;%L_m / Ln;
40 C_r = 1 / (L_r * (2 * pi * f_res)^2);
41 f_res = 1 / (2*pi*sqrt(C_r*L_r)); % Hz (recalculated)
42
43 Qe = sqrt(L_r/C_r) / R_eq;
44 Qe_75 = sqrt(L_r/C_r) / (R_eq*(1/0.75)); % = 0.75*Qe
45 Qe_10 = sqrt(L_r/C_r) / (R_eq*(1/0.10)); % = 0.10*Qe
46
47 fprintf('Gain_Range:_M_G_min_=%%.3f|_M_G_max_=%%.3f\n', M_G_min, M_G_max)
48 ;
49 fprintf('Quality_factor_max_(Qe_max):_%.3f\n', Qe_max);
50 fprintf('Quality_factor_new_(Qe):_%.3f\n', Qe);
51 fprintf('Equivalent_Load_Resistance:_%.2f_Ohm\n', R_eq);
52 fprintf('Resonant_Capacitor:_%.2f_nF\n', C_r * 1e9);
53 fprintf('Resonant_Inductor:_%.2f_uH\n', L_r * 1e6);
54 fprintf('Resonant_Frequency:_%.1f_kHz\n', f_res / 1e3);
55
56 %% ===== Ganho vs frecuencia (3 curvas) =====
57 wx = logspace(-1, 0.5, 10000); % f_norm = f / f_res
58 f_kHz = (wx * f_res) / 1e3; % frecuencia real em kHz
59
60 gain_fun = @(wx, Q) ((wx.^2).*(Ln-1)) ./ sqrt( (Ln.*(wx.^2) - 1).^2 + ...
61 (wx.^2).*((wx.^2) - 1).^2).*((Ln-1).^2).*(Q.^2) );
62
63 K_100 = gain_fun(wx, Qe);
64 K_075 = gain_fun(wx, Qe_75);
65 K_010 = gain_fun(wx, Qe_10);
66
67 figure; hold on;
68 yline(M_G_min, '--', 'LineWidth', 2, ...
69 'DisplayName', sprintf('M_{G,min}_=%.3f', M_G_min));
70 yline(M_G_max, '--', 'LineWidth', 1.5, ...
71 'DisplayName', sprintf('M_{G,max}_=%.3f', M_G_max));

```

```

72 semilogx(f_kHz, K_100, 'LineWidth', 2.2, ...
73     'DisplayName', sprintf('Qe=%.3f_(100%)', Qe));
74 semilogx(f_kHz, K_075, '--', 'LineWidth', 2.0, ...
75     'DisplayName', sprintf('Qe=%.3f_(75%)', Qe_75));
76 semilogx(f_kHz, K_010, ':', 'LineWidth', 2.0, ...
77     'DisplayName', sprintf('Qe=%.3f_(10%)', Qe_10));
78
79 title('|G|(fs)vsfs para Qe{max}, 75%e, 10%', 'FontSize', 14);
80 xlabel('fs (kHz)', 'FontSize', 12);
81 ylabel('|G|(fs)Gain', 'FontSize', 12);
82 grid on; box on; legend('show', 'Location', 'best', 'FontSize', 12);
83 ylim([0 2.5]); % limita o eixo Y
84 xlim([0 80]); % em kHz
85 hold off;

```

Listing A.5: Gain Curve Intersection Analysis for LLC Converter at Fixed  $Q_e$  and  $L_n$ 

## A.6 MATLAB/PLECS Script for Multi- $V_{in}$ Frequency Sweep at Full Load

This MATLAB/PLECS script automates a frequency sweep of the LLC converter model to evaluate output-voltage behavior across the entire switching-frequency range under constant full-load operation of 1 kW. For each input voltage in  $\{600, 550, 500, 450\}$  V, the script simulates the model, measures the steady-state output voltage over a defined time window, and plots four curves (one per input level). The intersections with the 24 V reference line mark the operating frequencies required to achieve regulation for each  $V_{in}$ . The script targets PLECS via the `plecs()` API.

```

1 %% Multi-Vin frequency sweep and plot
2 % --- user knobs ---
3 f_start = 15e3; % Hz
4 f_end = 50e3; % Hz
5 N_points = 20; % number of frequency points
6 Vin_list = [600 550 500 450]; % Volts
7 Vin_labels = ["600 V", "550 V", "500 V", "450 V"];
8
9 % Model variable names
10 VinVarName = 'V_DC'; % <-- change to your input voltage variable in the
    model
11 FswVarName = 'f_sw'; % <-- change to your switching frequency variable in
    the model
12
13 % Scope and measurement window
14 scopePath = 'freq-modulation-ac-sweep/Scope5'; % <-- change to your scope
15 StopTime = 2e-3; % s (short to speed up)

```

```

16 t_window = 0.5e-3; % s measure over the last 0.5 ms
17
18 % If your output voltage is NOT the first trace/channel, change these:
19 traceIndex = 1;
20 channelIndex = 1;
21
22 % Colors (blue, yellow, green, brown)
23 clr_blue = [0 0 1];
24 clr_red = [1 0 0];
25 clr_green = [0 0.5 0];
26 clr_brown = [0.60 0.30 0.00];
27 plot_colors = {clr_blue, clr_red, clr_green, clr_brown};
28
29 % --- setup ---
30 frequencies = linspace(f_start, f_end, N_points);
31 Vout = nan(N_points, numel(Vin_list));
32
33 % Clear scope traces once (optional)
34 try
35     plecs('scope', scopePath, 'ClearTraces');
36 catch
37     % ignore if scope path differs / scope not present
38 end
39
40 % --- sweep (simulate first, fill Vout) ---
41 for j = 1:numel(Vin_list)
42     Vin = Vin_list(j);
43     fprintf('==_Vin_=%.0f_V_==\n', Vin);
44
45     for i = 1:numel(frequencies)
46         f_sw = frequencies(i);
47
48         simOptions = struct( ...
49             'ModelVars', struct(FswVarName, f_sw, VinVarName, Vin), ...
50             'StopTime', StopTime ...
51             % , 'RelTol', 1e-3 % (optional) relax tolerance for speed
52         );
53
54         plecs('simulate', simOptions);
55
56         % Measure mean Vout in the last window
57         t1 = max(0, StopTime - t_window);
58         t2 = StopTime;
59         scopeData = plecs('scope', scopePath, 'GetCursorData', [t1 t2], '
                    mean');

```

```

60
61     % cursorData{traceIndex}{channelIndex}.mean(1)
62     Vout(i,j) = scopeData.cursorData{traceIndex}{channelIndex}.mean(1);
63
64     fprintf('f_sw=%%.0fHz,Vin=%%.0fV->Vout=%%.3fV\n', f_sw, Vin
65             , Vout(i,j));
66 end
67
68 % --- plot ---
69 figure; hold on; grid on;
70 x_kHz = frequencies/1e3;
71
72 % Plot lines and store handles (one per Vin)
73 try
74     hLines = gobjects(1, numel(Vin_list)); % new MATLAB
75 catch
76     hLines = zeros(1, numel(Vin_list)); % fallback for older MATLAB/Octave
77 end
78
79 for j = 1:numel(Vin_list)
80     hLines(j) = plot(x_kHz, Vout(:,j), 'LineWidth', 1.8, 'Color',
81                     plot_colors{j});
82     % small markers (kept out of legend)
83     plot(x_kHz, Vout(:,j), 'o', 'MarkerSize', 3, 'HandleVisibility','off',
84          ...
85          'Color', plot_colors{j});
86 end
87
88 xlabel('Switching_Frequency_(kHz)');
89 ylabel('Output_Voltage_(V)');
90 title('LLC_Output_Voltage_vs_Switching_Frequency_for_Multiple_Vin');
91
92 % Clean legend: exactly one item per line; freeze updates
93 lgd = legend(hLines, '600', '550', '500', '450', 1);
94 set(lgd, 'AutoUpdate', 'off');
95
96 % --- horizontal 24 V line ---
97 targetV = 24; % V
98 try
99     yline(targetV, '--', '24_V', ...
100           'LabelHorizontalAlignment','left', 'LabelVerticalAlignment','bottom'
101           , ...
102           'HandleVisibility','off'); % keep out of legend
103 catch

```

```

101     plot([min(x_kHz) max(x_kHz)], [targetV targetV], '--', '
        HandleVisibility','off');
102     text(min(x_kHz), targetV, '_24_V', 'VerticalAlignment','bottom', '
        HandleVisibility','off');
103 end
104
105 % --- find and highlight intersections with 24 V ---
106 for j = 1:numel(Vin_list)
107     y = Vout(:, j);
108     s = y - targetV;
109
110     s1 = s(1:end-1); s2 = s(2:end);
111     ok = ~isnan(s1) & ~isnan(s2);
112     idx = find(ok & ( (s1 .* s2 <= 0) & ~(s1==0 & s2==0) ));
113
114     col = plot_colors{j};
115
116     for k = idx(:).'
117         x1 = frequencies(k); x2 = frequencies(k+1);
118         y1 = y(k); y2 = y(k+1);
119
120         if y2 ~= y1
121             f_cross = x1 + (targetV - y1) * (x2 - x1) / (y2 - y1);
122         else
123             f_cross = x1;
124         end
125
126         % highlight the crossing (kept out of legend)
127         plot(f_cross/1e3, targetV, 'o', 'MarkerSize', 6, ...
128             'MarkerFaceColor', col, 'MarkerEdgeColor', 'k', 'HandleVisibility
129             ','off');
130
131         % dashed vertical trace to x-axis (kept out of legend)
132         plot([f_cross/1e3, f_cross/1e3], [0, targetV], '--', 'Color', col, '
133             HandleVisibility','off');
134
135         % annotation (kept out of legend)
136         text(f_cross/1e3, targetV, sprintf('_%.2f_kHz', f_cross/1e3), ...
137             'VerticalAlignment','bottom', 'Color', col, 'HandleVisibility','
138             off');
139     end
140 end

```

Listing A.6: Multi- $V_{in}$  frequency sweep and 24 V intersection highlighting at 1 kW full load

## A.7 Python Script for FHA Pole–Zero and Bode Plot Visualization

This Python script generates the pole–zero map and the Bode magnitude plot of the LLC converter small-signal model based on the first-harmonic approximation (FHA). It uses the analytical transfer function  $T_{FHA}(s)$ .

The script computes the roots of the numerator and denominator to identify poles and zeros, plots their distribution on the complex plane, and generates the corresponding Bode magnitude response. Both plots are saved as high-resolution PNG and PDF files for inclusion in the thesis.

Representative component values were used for illustration purposes ( $L_r = 65 \mu\text{H}$ ,  $L_m = 666 \mu\text{H}$ ,  $C_r = 246 \text{ nF}$ , and  $R_{ac} = 67.23 \Omega$ ), but the script can be reused with any parameter set.

```

1 import numpy as np
2 import matplotlib.pyplot as plt
3
4 # === LLC converter parameters ===
5 Lr = 65e-6 # resonant inductor [H]
6 Lm = 666e-6 # magnetizing inductor [H]
7 Cr = 246e-9 # resonant capacitor [F]
8 Rac = 67.23 # equivalent AC load [ohm]
9
10 # === FHA transfer function coefficients ===
11 # T(s) = (Cr*Lm*Rac*s^2) / (Cr*Lr*Lm*s^3 + Cr*Rac*(Lr+Lm)*s^2 + Lm*s + Rac
12     )
13 num = np.array([Cr*Lm*Rac, 0.0, 0.0])
14 den = np.array([Cr*Lr*Lm, Cr*Rac*(Lr+Lm), Lm, Rac])
15
16 # === Poles and zeros ===
17 zeros = np.roots(num)
18 poles = np.roots(den)
19
20 # === Resonant frequencies ===
21 fs = 1 / (2*np.pi*np.sqrt(Lr*Cr)) # series resonance
22 fp = (1 / (2*np.pi)) * np.sqrt((Lr + Lm)/(Lr*Lm*Cr)) # parallel resonance
23
24 # === Pole-zero map ===
25 plt.figure(figsize=(4,3.2))
26 plt.axhline(0, color='gray', linewidth=0.6)
27 plt.axvline(0, color='gray', linewidth=0.6)
28 plt.scatter(np.real(zeros), np.imag(zeros), marker='o', label='zeros')
29 plt.scatter(np.real(poles), np.imag(poles), marker='x', label='poles')
30
31 for p in poles:
32     if abs(np.imag(p)) > 1e-6:
33         plt.annotate("complex_pair", (np.real(p), np.imag(p)),
34                     xytext=(np.real(p)*1.2, np.imag(p)*1.2),

```

```

34         arrowprops=dict(arrowstyle='->', linewidth=0.6),
35         fontsize=8)
36     else:
37         plt.annotate("real_pole", (np.real(p), np.imag(p)),
38                     xytext=(np.real(p)*1.1, 0),
39                     arrowprops=dict(arrowstyle='->', linewidth=0.6),
40                     fontsize=8)
41
42 plt.xlabel('Real_()')
43 plt.ylabel('Imag_(j)')
44 plt.title('PoleZero_Map_(FHA)')
45 plt.legend(fontsize=8)
46 plt.tight_layout()
47 plt.savefig('pz_map.png', dpi=300)
48 plt.savefig('pz_map.pdf')
49
50 # === Bode magnitude ===
51 f = np.logspace(3.5, 5.5, 2500)
52 w = 2 * np.pi * f
53 s = 1j * w
54 H = (num[0]*(s**2)) / (den[0]*(s**3) + den[1]*(s**2) + den[2]*s + den[3])
55 mag = 20 * np.log10(np.abs(H))
56
57 plt.figure(figsize=(4.6, 3.2))
58 plt.semilogx(f, mag, color='orange')
59 plt.axvline(fs, linestyle='--', linewidth=0.8)
60 plt.axvline(fp, linestyle='--', linewidth=0.8)
61 plt.text(fs, np.interp(fs, f, mag), '_$_f_s$', va='bottom', fontsize=8)
62 plt.text(fp, np.interp(fp, f, mag), '_$_f_p$', va='bottom', fontsize=8)
63 plt.xlabel('Frequency_(Hz)')
64 plt.ylabel('Magnitude_(dB)')
65 plt.title('Bode_Magnitude_(FHA)')
66 plt.tight_layout()
67 plt.savefig('bode_mag.png', dpi=300)
68 plt.savefig('bode_mag.pdf')
69
70 print(f"Series_resonance:_{fs:.2f}_Hz")
71 print(f"Parallel_resonance:_{fp:.2f}_Hz")
72 print("Polezero_and_Bode_plots_saved_successfully.")

```

Listing A.7: Python script for FHA pole-zero map and Bode magnitude plot generation.

## **A.8 Printed Circuit Board Documents**

### **A.8.1 Bill of Materials**

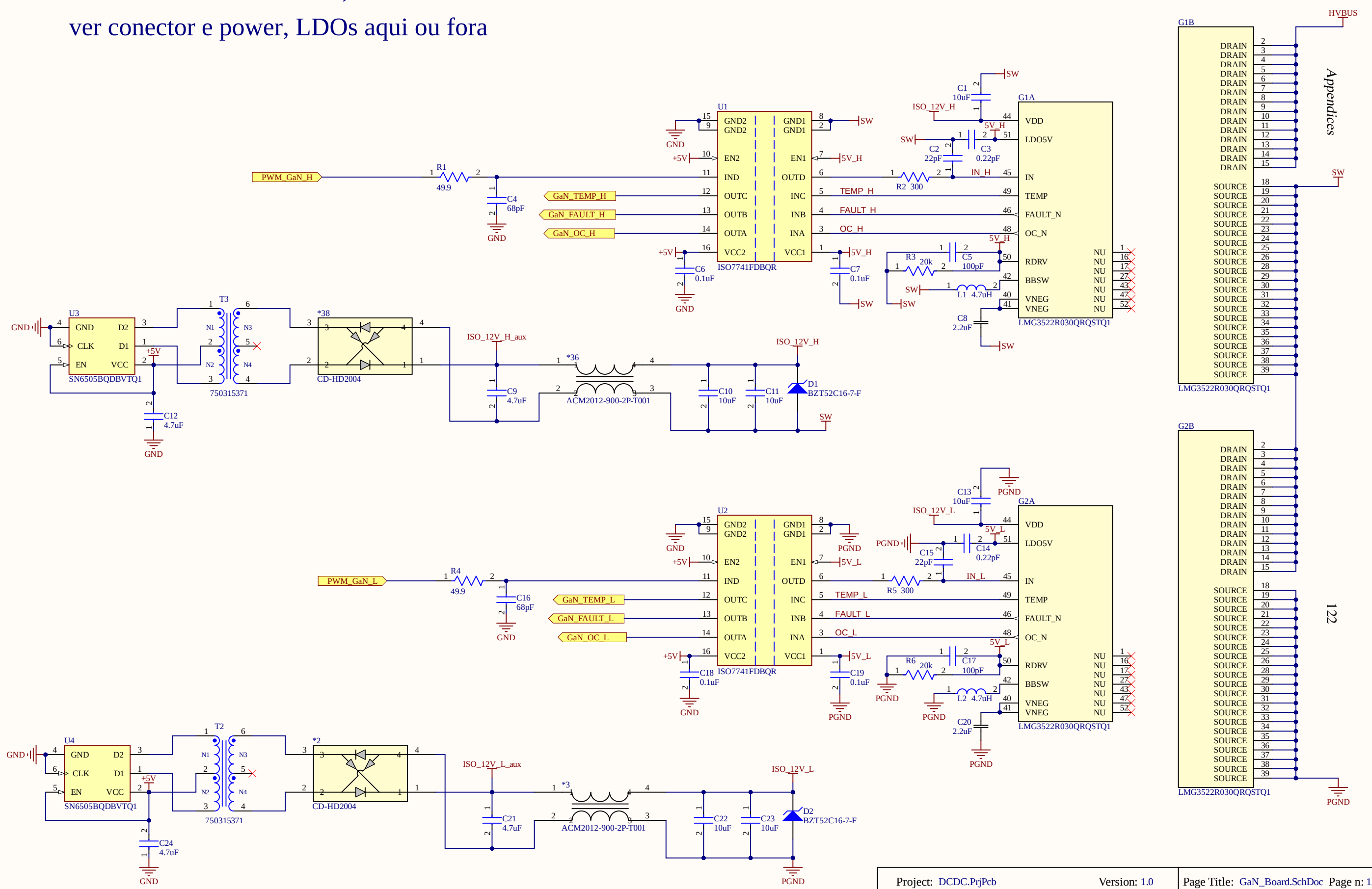
This section lists all components used in the prototype and their key attributes (reference, quantity, manufacturer, description, footprint). The complete BOM is provided in Appendix [A.8.1](#) and can be used for procurement and traceability.

| Line | Name                   | Description                                                                                                           | Quantity | Manufacturer 1            | Manufacturer Part Number 1 | Manufacturer Lifecycle 1       | Supplier 1 | Supplier Part Number 1      | Supplier Unit Price 1 | Supplier Subtotal 1 |
|------|------------------------|-----------------------------------------------------------------------------------------------------------------------|----------|---------------------------|----------------------------|--------------------------------|------------|-----------------------------|-----------------------|---------------------|
| 1    | LMG3522R030QRSTQ1      | GAN                                                                                                                   |          | Texas Instruments         | LMG3522R030QRSTQ1          |                                | Digikey    |                             |                       |                     |
| 2    | ISO7741FDBQR           | Interface Circuit, CMOS, PDSO16                                                                                       |          | Texas Instruments         | ISO7741FDBQR               | Volume Production              | Digikey    | 296-48140-1-ND              | 1.96                  | 3.92                |
| 3    | CD-HD2004              | Bridge Rectifier Diode, Schottky, 1 Phase, 2A, 40V V(RRM), Silicon                                                    |          | Bourns                    | CD-HD2004                  | Volume Production              | Digikey    | CD-HD2004CT-ND              | 0.71534               | 1.43067             |
| 4    | ACM2012-900-2P-T001    | Data Line Filter, 2 Function(s), 50V, 0.4A, 4 Pin(s)                                                                  |          | TDK                       | ACM2012-900-2P-T001        | Volume Production              | Digikey    | ACM2012-900-2P-T001         | 0.5999                | 1199.8              |
| 5    | 10uF                   | 25V, 10uF, Surface Mount, 1206                                                                                        |          | Taiyo Yuden               | TMK316AB7106KLHT           | Volume Production              | Digikey    | 963-TMK316AB7106KLHT        | 0.35                  | 0.7                 |
| 6    | 22pF                   | Ceramic Capacitor, Multilayer, Ceramic, 50V, 5% +Tol, 5% -Tol, C0G, 30ppm/Cel TC, 0.000022uF, Surface Mount, 0402     |          | Murata                    | GCM1555C1H220JA16D         | Volume Production              | Digikey    | 81-GCM1555C1H220JA6D        | 0.1                   | 0.2                 |
| 7    | 0.22pF                 | Ceramic Capacitor, Multilayer, Ceramic, 16V, 10% +Tol, 10% -Tol, X7R, 15% TC, 0.22uF, Surface Mount, 0402             |          | Murata                    | GCM1558R71C224KE02D        | Volume Production              | Digikey    | 81-GCM1558R71C224KE2D       | 0.01                  | 0.2                 |
| 8    | 68pF                   | 0.000068uF, 50V, 5% +Tol, 5% -Tol, C0G, 30ppm/Cel TC, Surface Mount, 0402                                             |          | TDK                       | C1005C0G1H680J050BA        | Not Recommended for New Design | Digikey    | C1005C0G1H680J050BA         | 0.048                 | 0.092               |
| 9    | 100pF                  | 50V, 0.0001uF, Surface Mount, 0402                                                                                    |          | TDK                       | CGA2B2C0G1H101J050BA       | Volume Production              | Digikey    | 40Y2199                     | 0.008                 | 0.032               |
| 10   | 0.1uF                  | Ceramic Capacitor, Ceramic, 50V, 10% +Tol, 10% -Tol, X7R, 15% TC, 0.1uF, Surface Mount, 0603                          |          | Murata                    | GCM155R71C224KE02D         | Volume Production              | Digikey    | 81-GCM155R71C224KE2D        | 0.03                  | 0.3                 |
| 11   | 2.2uF                  | Ceramic Capacitor, Multilayer, Ceramic, 25V, 10% +Tol, 10% -Tol, X7R, 15% TC, 2.2uF, Surface Mount, 0805              |          | TDK                       | CGA4J3X7R1E225K125AB       | Volume Production              | Digikey    | 39Y3548                     | 0.106                 | 0.212               |
| 12   | 4.7uF                  | 4.7uF, 25V, 10% +Tol, 10% -Tol, X6S, 22% TC, Surface Mount, 0603                                                      |          | Murata                    | GRM188C81E475KE11J         | Volume Production              | Digikey    | 490-GRM188C81E475KE11JCT-ND | 0.19936               | 0.79742             |
| 13   | 10uF                   | Ceramic Capacitor, Multilayer, Ceramic, 25V, 10% +Tol, 10% -Tol, X7S, 22% TC, 10uF, Surface Mount, 0805               |          | TDK                       | CGA4J1X7S1E106K125AC       | Volume Production              | Digikey    | 71AH2823                    | 0.184                 | 1.84                |
| 14   | 100nF                  | 0.1uF, 50V, 10% +Tol, 10% -Tol, X7R, 15% TC, Surface Mount, 0603                                                      |          | KEMET                     | C0603C104K5RAUTO           | Volume Production              | Digikey    | 80-C0603C104K5RAUTO         | 0.036                 | 0.576               |
| 15   | 1uF                    | 1uF, 25V, 10% +Tol, 10% -Tol, X7R, 15% TC, Surface Mount, 1206                                                        |          | KYOCERA AVX               | 1206S3105KA72A             | Volume Production              | Digikey    | 50AH3297                    | 0.083                 | 0.664               |
| 16   | 3.9nF                  | 3.9nF, 25V, 10% +Tol, 10% -Tol, X7R, 15% TC, Surface Mount, 0603                                                      |          | KEMET                     | C0603C392K3RACTU           | Volume Production              | Digikey    | 80-C0603C392K3R             | 0.23                  | 0.92                |
| 17   | 10nF, 0.01uF           | 0.01uF, 50V, 10% +Tol, 10% -Tol, X7R, 15% TC, Surface Mount, 0603                                                     |          | Murata                    | GCM188R71H103KA37J         | Not Recommended for New Design | Digikey    | GCM188R71H103KA37J          | 0.0121                | 121                 |
| 18   | 82nF                   | 0.082uF, Film Capacitor, Polypropylene, 1000V, 5% +Tol, 5% -Tol, Through Hole Mount                                   |          | KEMET                     | R760I28205050J             | Volume Production              | Digikey    | 399-R760I28205050J-ND       | 0.91469               | 2,74408             |
| 19   | 0.1uF                  | Ceramic, 630V, 10% +Tol, 10% -Tol, X7R, 15% TC, 0.1uF, Surface Mount, 1812                                            |          | Murata                    | GRM43DR72J104KW01L         | Volume Production              | Digikey    | GRM43DR72J104KW01L          | 0.3254                | 325.4               |
| 20   | 10pF                   | 10pF SMD/SMT 50V 0603                                                                                                 |          | 2 KYOCERA AVX             | 06035A100BA72A             | Volume Production              | TME        |                             | 0.04491               | 0.44914             |
| 21   | 330pF                  | 0.00033uF, 50V, 5% +Tol, 5% -Tol, C0G, 30ppm/Cel TC, Surface Mount, 0603                                              |          | KYOCERA AVX               | 06035A331UAT2A             | Volume Production              | TME        | 316660                      | 0.011                 | 0.099               |
| 22   | 1nF                    | Ceramic Capacitor, Multilayer, Ceramic, 50V, 10% +Tol, 10% -Tol, X7R, 15% TC, 0.001uF, Surface Mount, 0603            |          | KEMET                     | C0603C102K5RACTU           | Volume Production              | Digikey    | 51B220                      | 0.011                 | 0.099               |
| 23   | 1uF                    | Ceramic Capacitor, Multilayer, Ceramic, 25V, 10% +Tol, 10% -Tol, X7R, 15% TC, 1uF, Surface Mount, 0603                |          | TDK                       | CGA3E1X7R1E105K080AC       | Volume Production              | Digikey    | 810-CGA3E1X7R1E105K         | 0.15                  | 0.3                 |
| 24   | 10uF                   | Ceramic Capacit+G25+C25                                                                                               |          | Taiyo Yuden               | C3225X7S1H106K250AB        | Not Recommended for New Design | Digikey    | 26AM1916                    | 0.348                 | 8.7                 |
| 25   | 270uF                  | 270 uF 50 V Capacitores de polímero - aluminio Radial. lata - SMD 10mOhm 4000h a 135°C                                |          | 6 Panasonic Electronic    | EEH-ZU1H271UP              |                                | Digikey    |                             |                       |                     |
| 26   | 100nF                  | Multilayer Ceramic Capacitor, 0.1 uF, 50 V, ± 5%, X7R, 0805 [2012 Metric]                                             |          | Kyocera AVX               | KGM21NR71H104JT            | Unknown                        | Digikey    |                             |                       |                     |
| 27   | 22uF                   | 22uF 20% 16V (0603) CERAMIC                                                                                           |          | Samsung Electro-M         | CL10A226M07JZNC            |                                | Digikey    |                             |                       |                     |
| 28   | 680pF                  | Multilayer Ceramic Capacitor, 680 pF, 50 V, ± 10%, X7R, 0805 [2012 Metric]                                            |          | KEMET                     | C0805C681K5RACTU           | Volume Production              | Digikey    | C0805C681K5RACTU            | 0.0615                | 0.123               |
| 29   | 10uF                   | 650V 10 uF Film Capacitors                                                                                            |          | KEMET                     | C4AQCB5100A11J             |                                | Digikey    |                             |                       |                     |
| 30   | BZT52C16-7-F           | Zener Diode, 16V V(Z), 5.56%, 0.37W, Silicon, Unidirectional                                                          |          | Diodes Inc.               | BZT52C16-7-F               | Volume Production              | Digikey    | BZT52C16-7-F                | 0.014                 | 42                  |
| 31   | 282843-2               | Fixed Terminal Blocks 1TERMI-BLOK PCB MOUNT 90 2P.1                                                                   |          | TE Connectivity AMI       | 282843-2                   |                                | Digikey    |                             |                       |                     |
| 32   | Molex 2Pins_Horizontal | Re Hdr Assy Tin 1X23MM Micro-It Plus Sr 215766-1002                                                                   |          | Molex                     | 2157601002                 | Unknown                        | Digikey    |                             |                       |                     |
| 33   | 5536446-5              | ASSEMBLY RECEPTACLE EUROCARD.T                                                                                        |          | TE Connectivity AMI       | 5536446-5                  |                                | Digikey    |                             |                       |                     |
| 34   | 4.7uH                  | 4.7uH, 20%, 1 Element, Ferrite-Core, SMD, 0805                                                                        |          | TDK                       | MLZ2012M4R7HT000           | Volume Production              | Digikey    | MLZ2012M4R7HT000            | 0.0356                | 0.0712              |
| 35   | 65uH                   | 65uH 20% 17.2A Power Inductors - Leaded WE-HCFT 3533                                                                  |          | 1 Würth Elektronik        | 7443783533650              |                                | Farnell    |                             |                       |                     |
| 36   | 470nH                  | 470 nH Power Inductors - SMD                                                                                          |          | 2 Murata                  | DFE252012P-R47M+P2         |                                | Digikey    |                             |                       |                     |
| 37   | 2.2uH                  | 2.2uH Inductor                                                                                                        |          | 1 Traco Power             | TCK-160                    |                                | TME        |                             |                       |                     |
| 38   | 2.2uH                  | 2.2uH 20% 1mHz Metal 2A 0.097Ohm                                                                                      |          | 1 Samsung Electro-M       | CIGT252008LM2R2MNE         |                                | Digikey    |                             |                       |                     |
| 39   | 74651173R              | PCB Terminal, 50A                                                                                                     |          | Würth Elektronik          | 74651173R                  | Unknown                        | Digikey    | 732-74651173RCT-ND          | 3.35387               | 6,70774             |
| 40   | 49.9                   | Fixed Resistor, Metal Glaze/thick Film, 0.063W, 49.9ohm, 50V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 0402              |          | Vishay                    | CRCW040249R9FKED           | Volume Production              | Digikey    | CRCW040249R9FKED            | 0.0028                | 28                  |
| 41   | 300                    | Fixed Resistor, Metal Glaze/thick Film, 0.063W, 300ohm, 50V, 5% +/-Tol, 200ppm/Cel, Surface Mount, 0402               |          | Vishay                    | CRCW0402300RJNED           | Volume Production              | Digikey    | 72M6778                     | 0.003                 | 0.006               |
| 42   | 20k                    | 0.1W, 20Kohm, 50V, 0402, 5% +/-Tol, 200ppm/Cel, Surface Mount, 0402                                                   |          | Panasonic                 | ERJ-2GEJ203X               | Volume Production              | Digikey    | ERJ-2GEJ203X                | 0.004                 | 40                  |
| 43   | 10k                    | 10Kohm, 0.25W, 150V, 0.5% +/-Tol, 100ppm/Cel, Surface Mount, 0603                                                     |          | ROHM                      | ERJ-PA3D100ZV              | Volume Production              | Digikey    | 755-ESR03EZPD1002           | 0.124                 | 1,736               |
| 44   | 15k                    | 15Kohm, 0.1W, 75V, 5% +/-Tol, 200ppm/Cel, Surface Mount, 0603, Metal Glaze/thick Film                                 |          | Vishay                    | CRCW060315K0JNEA           | Volume Production              | Digikey    | 59M6768                     | 0.001                 | 0.001               |
| 45   | 3.3k                   | 3300ohm, 0.33W, 75V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 0603                                                       |          | Vishay                    | CRCW06033K30FKEAHP         | Volume Production              | Digikey    | 71-CRCW06033K30FKECH        | 0.16                  | 0.32                |
| 46   | 51                     | 51ohm, 0.1W, 350V, 5% +/-Tol, 200ppm/Cel, Surface Mount, 0603                                                         |          | ROHM                      | CRCW060351R0JNEA           | Volume Production              | Digikey    | 755-KTR03E2PJ510            | 0.079                 | 0.79                |
| 47   | 8.06k                  | 8060ohm, 0.1W, 100V, 0.1% +/-Tol, 25ppm/Cel, Surface Mount, 0603                                                      |          | Susumu                    | RG1608P-8061-B-T5          | Volume Production              | Digikey    | RG16P8.06KBCT-ND            | 0.11727               | 0.70381             |
| 48   | 180k                   | 180kohm, 0.1W, 75V, 1% +/-Tol, 50ppm/Cel, Surface Mount, 0603                                                         |          | Vishay                    | MCT06030C1803FP500         | Volume Production              | Digikey    | MCT06030C1803FP500          | 0.004                 | 0.004               |
| 49   | 8.2k                   | 8200ohm, 0.1W, 75V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 0603                                                        |          | Vishay                    | ERJ-3EKFR8201V             | Volume Production              | Digikey    | 71-CRCW06038K20FKEC         | 0.12                  | 0.12                |
| 50   | 10                     | 10ohm, 0.2W, 1.4142V, 1% +/-Tol, 0.200ppm/Cel, Surface Mount, 0603                                                    |          | Susumu                    | RL0816S-100-F              | Volume Production              | Digikey    | 754-RL0816S-100-F           | 0.14                  | 0.28                |
| 51   | 0.08                   | SHUNT, 0.08ohm, 2W, 0.4V, 1% +/-Tol, 75ppm/Cel, Surface Mount, 2816                                                   |          | Vishay                    | WSL2816R0800FEH            | Volume Production              | Digikey    | WSL2816R0800FEH             | 0.0293                | 0.0293              |
| 52   | 634k                   | 634kohm, 0.125W, 150V, 0.1% +/-Tol, 25ppm/Cel, Surface Mount, 0805                                                    |          | Yageo Group               | ERA-6AE6B343V              | Volume Production              | Digikey    | 603-RT0805BRD07634KL        | 0.171                 | 1.71                |
| 53   | 100k                   | RC0805FR-07100KL - SMD Chip Resistor, 100 kOhm, ± 1%, 125 mW, 0805 [2012 Metric], Thick Film, General Purpose         |          | Yageo Group               | RC0805FR-07100KL           | Volume Production              | Digikey    | RC0805FR-07100KL            | 0.0042                | 21                  |
| 54   | 453k                   | 453Kohms 1% 1/10watt SMD                                                                                              |          | Vishay                    | ERJ-3EKFA4533V             |                                | Digikey    |                             |                       |                     |
| 55   | 249k                   | 249K OHM 1% 1/3W                                                                                                      |          | Vishay                    | CRCW0603249KFKEAHP         |                                | Digikey    |                             |                       |                     |
| 56   | 9.31k                  | 9.31K ohm 1% 0603                                                                                                     |          | Bourns                    | CR0603-FX-9311ELF          |                                | Digikey    |                             |                       |                     |
| 57   | 34k                    | 34K 0.1% Vishay                                                                                                       |          | Vishay                    | TNPW060334K0BEEA           |                                | Digikey    |                             |                       |                     |
| 58   | DCDC2400-001           | Push-Pull Transformer 2kW 100kHz 1+1:12                                                                               |          | Premo                     | DCDC2400-001               |                                | PREMO      |                             |                       |                     |
| 59   | 750315371              | SMPS Transformer                                                                                                      |          | Würth Elektronik          | 750315371                  | Unknown                        | Digikey    | 710-750315371               | 3.07                  | 6.14                |
| 60   | SN6505BQDBVTQ1         | Interface Circuit, PDSO6                                                                                              |          | Texas Instruments         | SN6505BQDBVTQ1             | Volume Production              | Digikey    | 595-SN6505BQDBVTQ1          | 2.63                  | 5.26                |
| 61   | AMC3311QDWERQ1         | Automotive, 0 to 2-V input, precision reinforced isolated amplifier with integrated DC/DC converter 16-SOIC-40 to 125 |          | Texas Instruments         | AMC3311QDWERQ1             | Unknown                        | Digikey    |                             |                       |                     |
| 62   | OPA320AIDBVR           | Operational Amplifier, 1 Func, 150uV Offset-Max, CMOS, PDSO5                                                          |          | Texas Instruments         | OPA320AIDBVR               | Volume Production              | Digikey    | 595-OPA320AIDBVR            | 2.12                  | 8.48                |
| 63   | AMC3301QDWERQ1         | Isolation Amplifier, 1 Func, PDSO16                                                                                   |          | Texas Instruments         | AMC3301QDWERQ1             | Volume Production              | Digikey    | 296-AMC3301QDWERQ1CT-ND     | 7.88042               | 7.88042             |
| 64   | SN74AHCT1G126DBVR      | Bus Driver, AHCT/HCT/V-T Series, 1-Func, 1-Bit, True Output, CMOS, PDSO5                                              |          | Texas Instruments         | SN74AHCT1G126DBVR          | Volume Production              | Digikey    | 296-4710-1-ND               | 0.129                 | 0.25799             |
| 65   | V60D60C-M3/I           | Rectifier Diode, Schottky, 1 Phase, 2 Element, 30A, 60V V(RRM), Silicon, TO-263AC                                     |          | Vishay                    | V60D60C-M3/I               | Volume Production              | Digikey    | V60D60C-M3/I                | 1.3126                | 1.3126              |
| 66   | TMCS1133C2AQDVGR       | 150mV/A 1MHz Hall-effect current sensor with AFR and ALERT 10-SOIC -40 to 125                                         |          | Texas Instruments         | TMCS1133C2AQDVGR           | Volume Production              | Digikey    |                             |                       |                     |
| 67   | TMCS1133C2AQDVGR       | 50mV/A 1MHz Hall-effect current sensor with AFR and ALERT 10-SOIC -40 to 125                                          |          | Texas Instruments         | TMCS1133C2AQDVGR           | Volume Production              | Digikey    |                             |                       |                     |
| 68   | TPS628510DRLR          | 2.7-V to 6-V, 0.5-A, fixed-frequency, step-down converter                                                             |          | Texas Instruments         | TPS628510DRLR              |                                | Digikey    | 296-TMCS1133C2AQDVGRCT-ND   | 4.3272                | 8,65439             |
| 69   | TIM 3.5-0911SM         | TRACO DCDC SMD 4.5-12Vin 5V 700mA 3.5W                                                                                |          | Traco Power               | TIM 3.5-0911SM             |                                | Digikey    |                             |                       |                     |
| 70   | TPS629210QDRLRQ1       | Automotive 3-V to 17-V, 1-A, high-efficiency and low-IQ, synchronous buck conver                                      |          | Texas Instruments         | TPS629210QDRLRQ1           |                                | Digikey    |                             |                       |                     |
| 71   | ISO1050DUBR            | Isolated 5-V CAN transceiver                                                                                          |          | 1 Texas Instruments       | ISO1050DUBR                |                                | TME        |                             |                       |                     |
| 72   | RMCF0603FT1K00         | 1 kOhms ±1% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200 Thick Film                               |          | Stackpole Electronics Inc | RMCF0603FT1K00             | Volume Production              | DigiKey    |                             |                       |                     |
| 73   | RC0603JR-076K8L        | RES 6.8K OHM 5% 1/10W 0603                                                                                            |          | YAGEO                     | RC0603JR-076K8L            | Volume Production              | DigiKey    |                             |                       |                     |

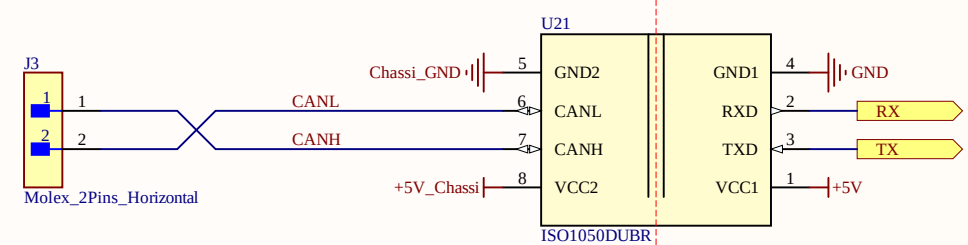
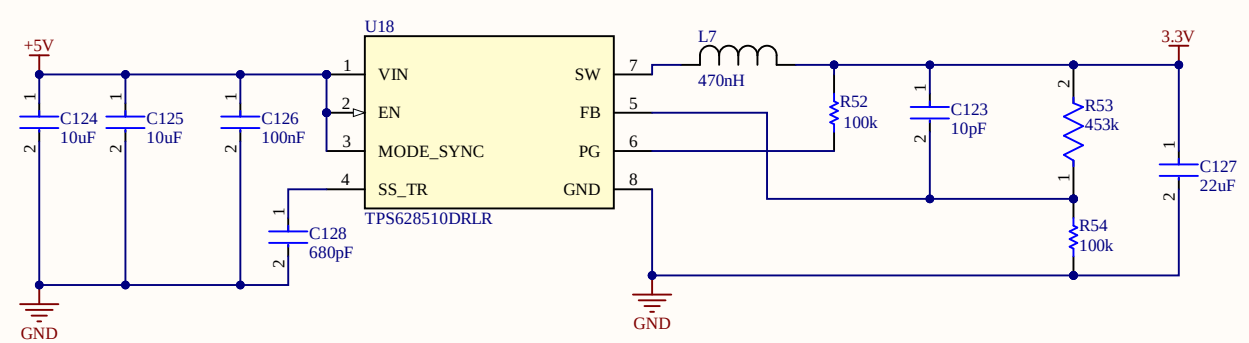
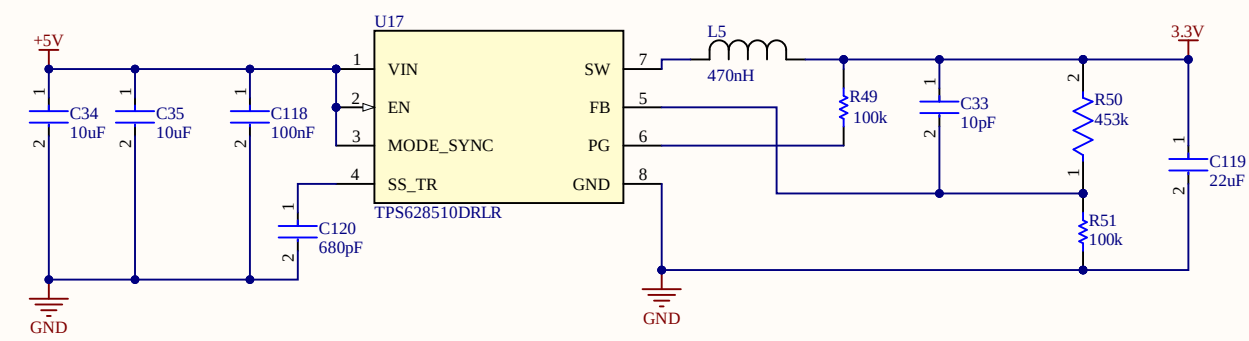
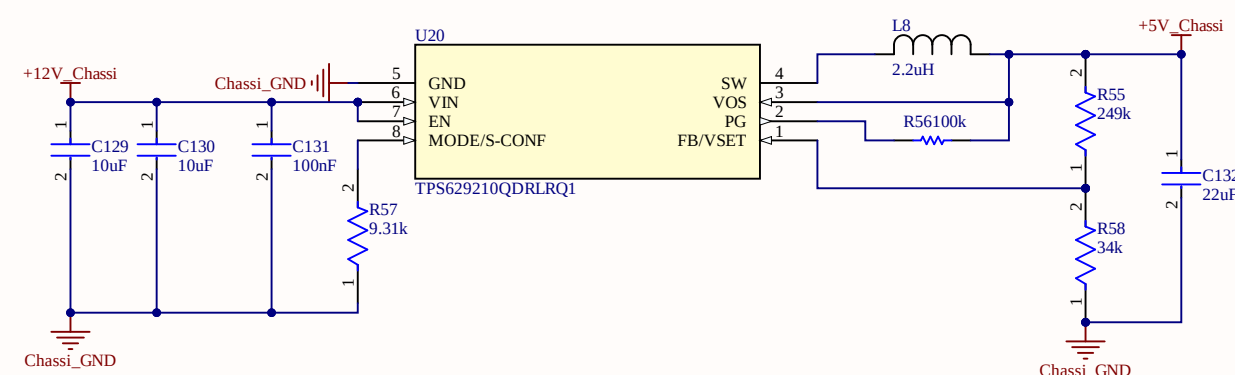
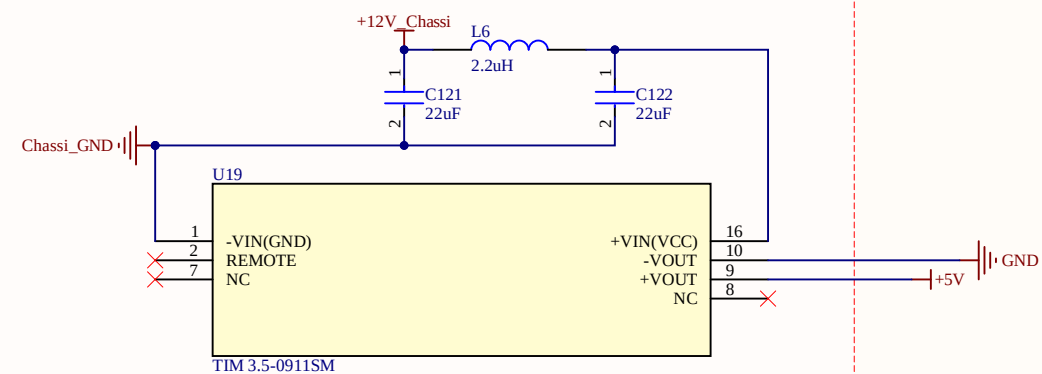
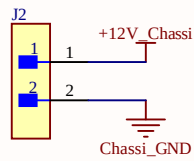
### **A.8.2 PCB Schematics**

This section presents the full schematics of the converter.

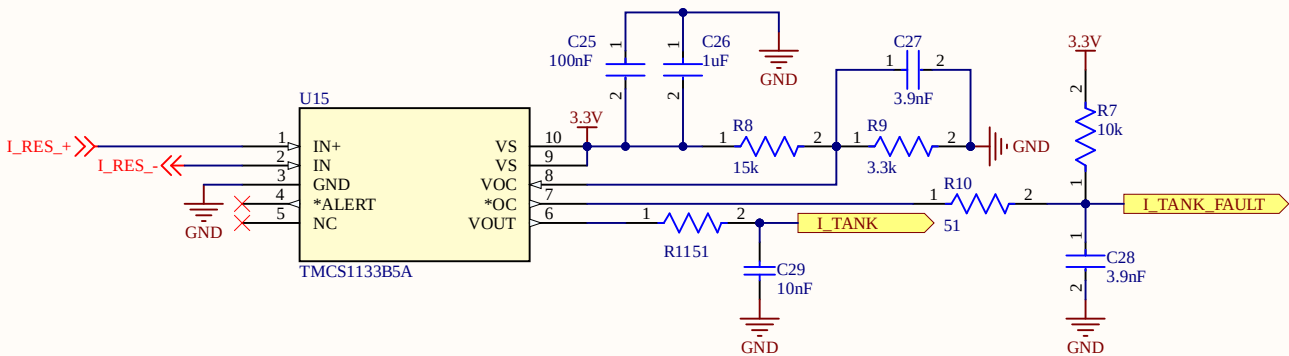
confirmar os RC nos outs C,B e A  
ver conector e power, LDOs aqui ou fora



# Reference To Car Chassi

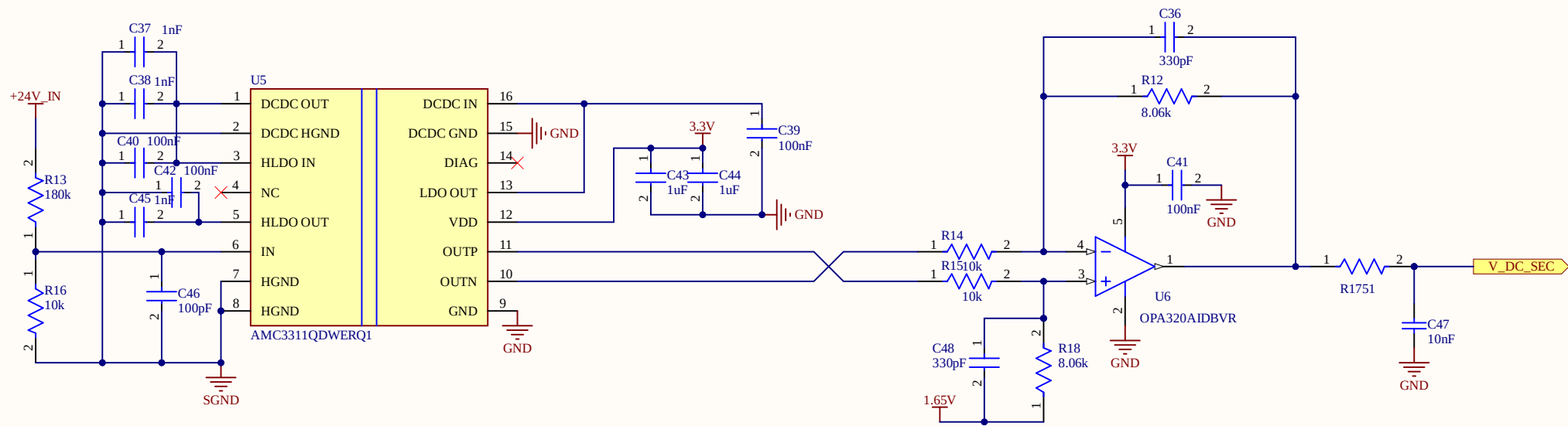


Resonant Tank Current Sensing



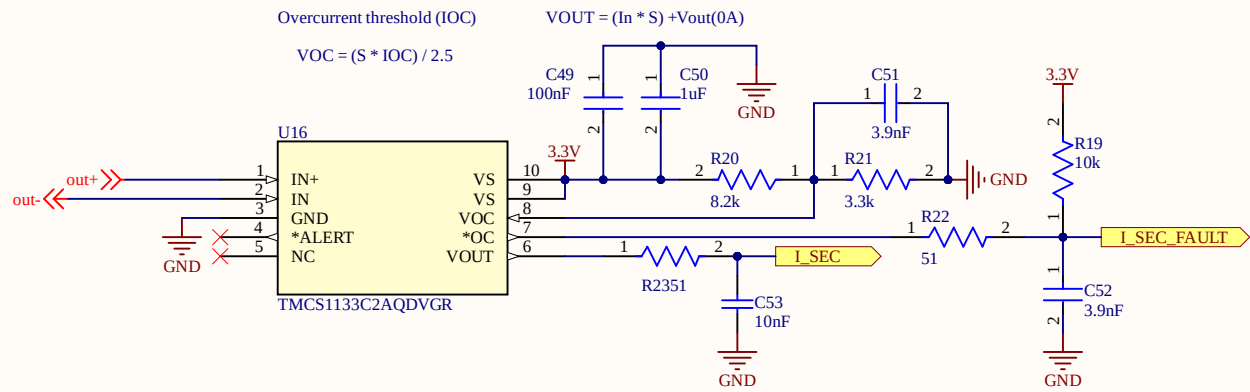
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| Date: *      |  | Sch author: '*'  |                    |           |
|              |  | PCB author: '*'  |                    |           |

Secondary Output Voltage Sensing

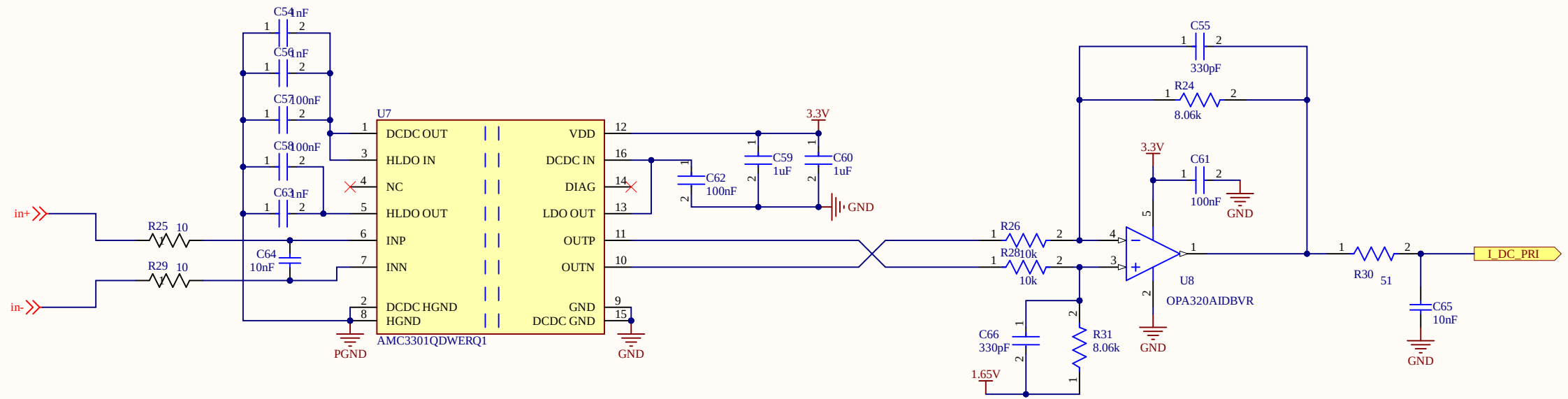


Secondary Output Current Sensing

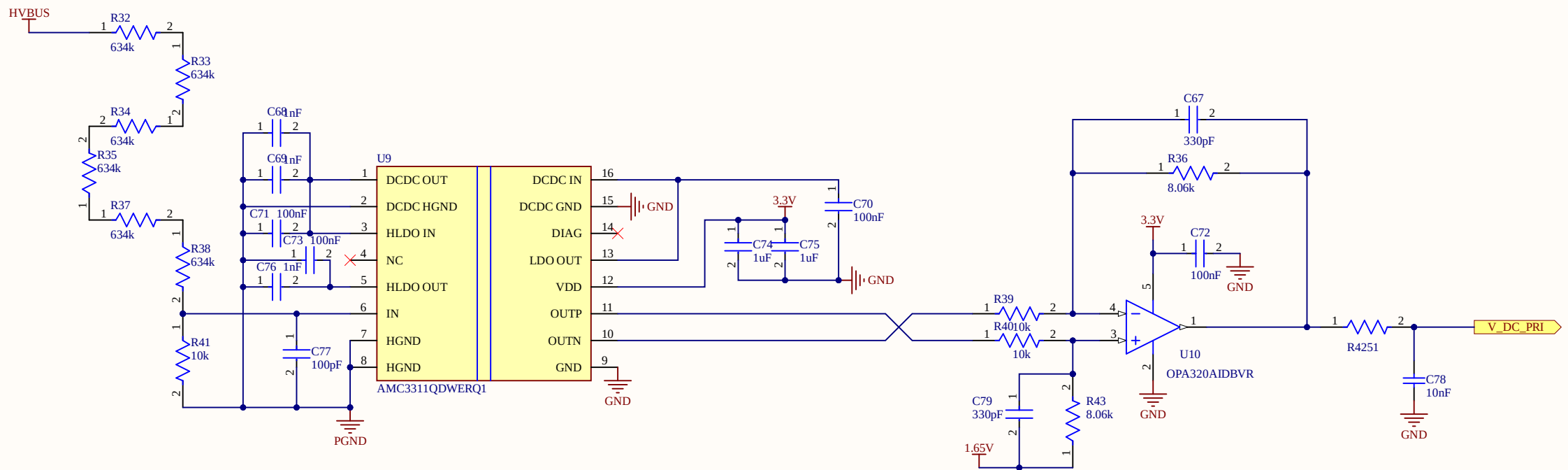
TMCS1133

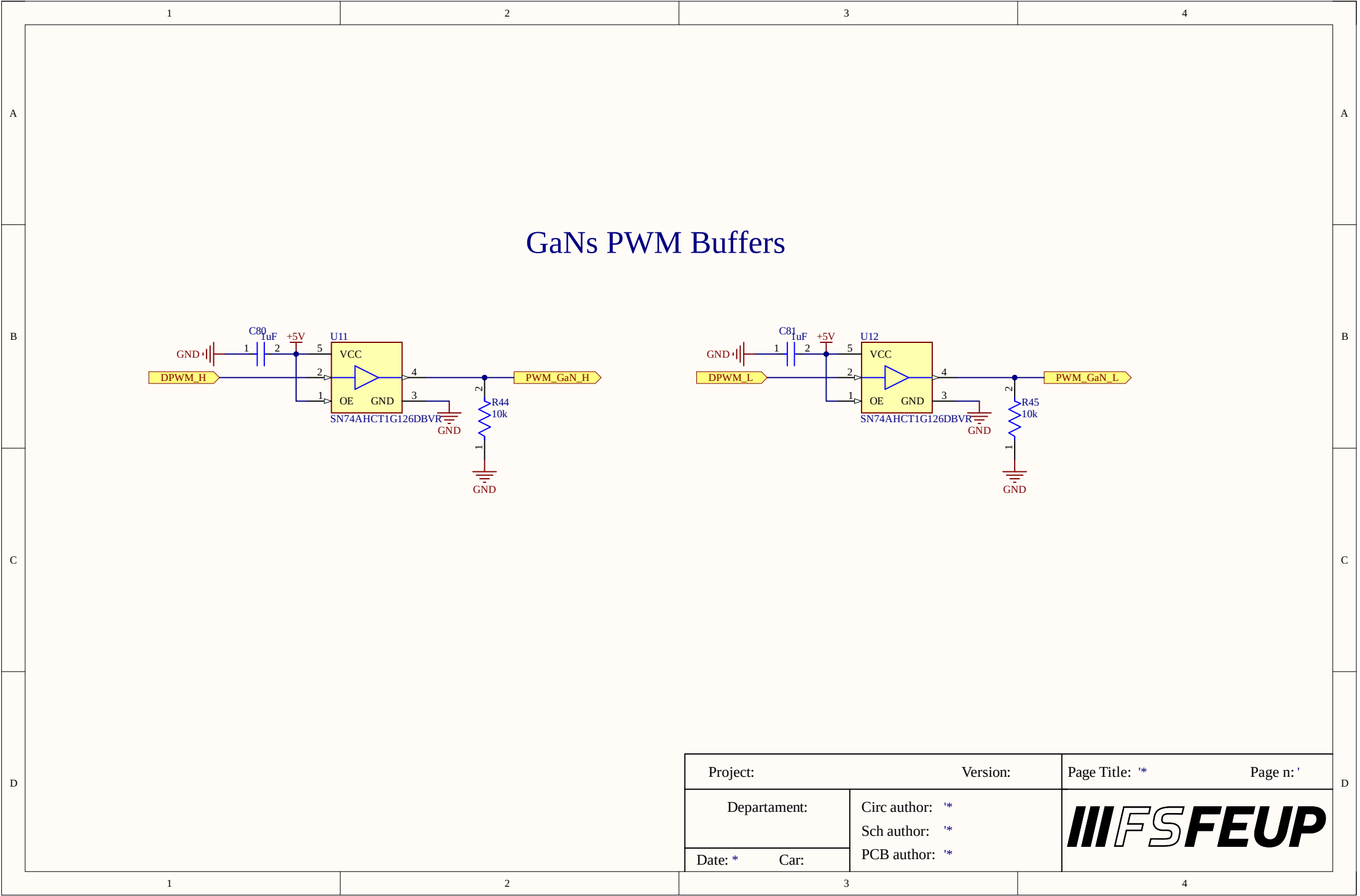


## Primary Input Current Sensing

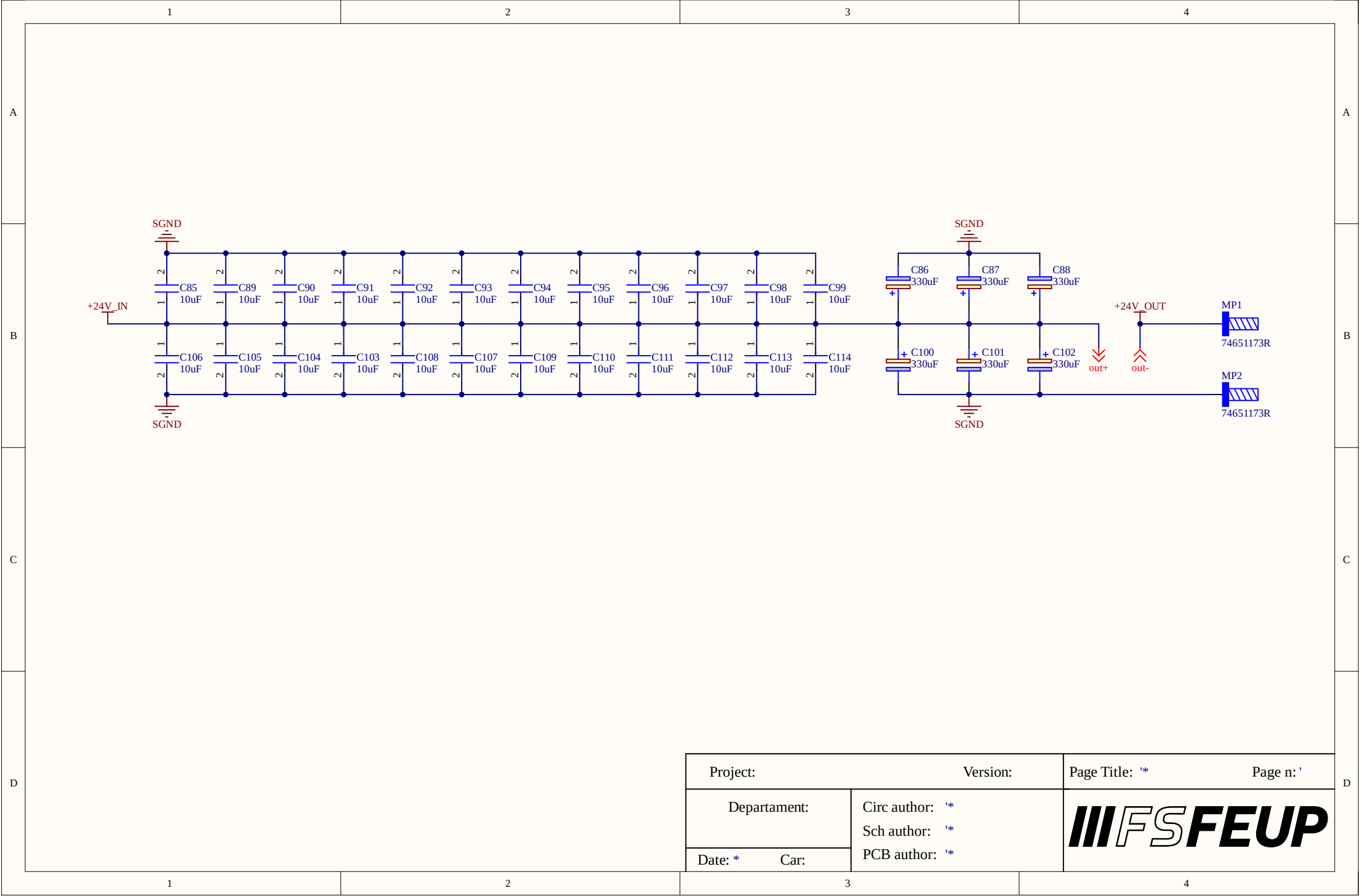


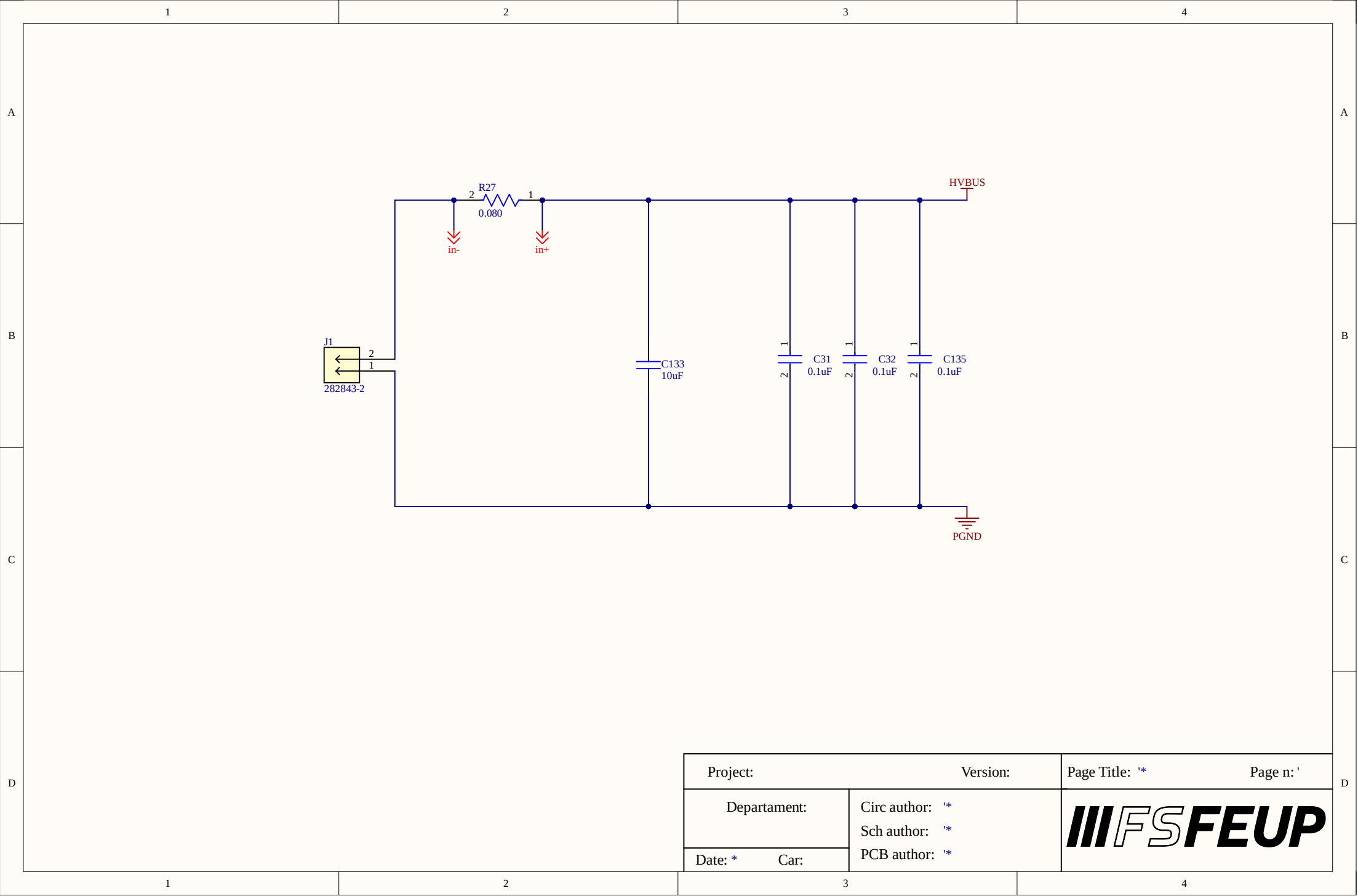
## Primary Input Voltage Sensing

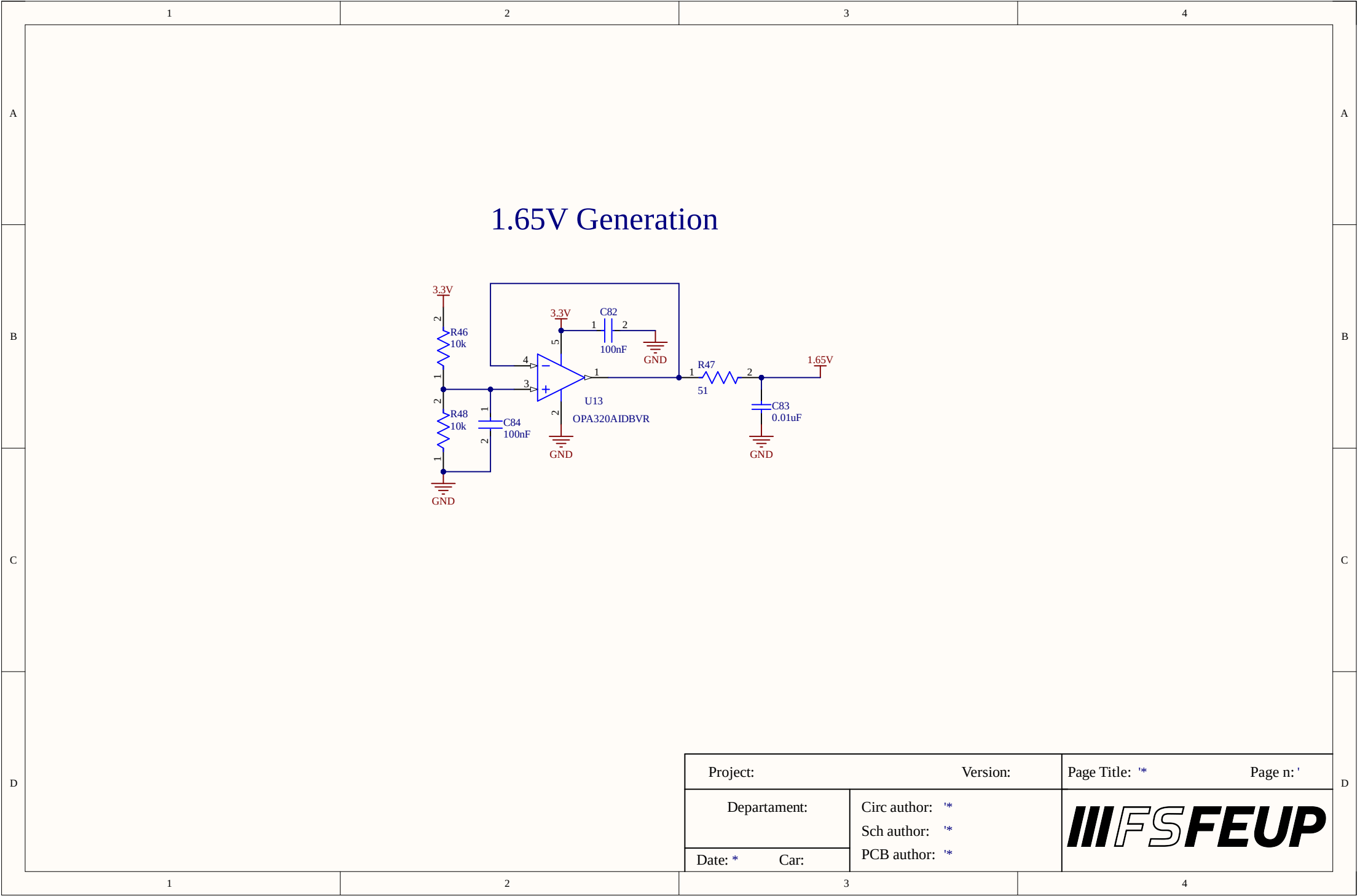












**A.8.3 PCB Assembly Drawings**

This section provides the top and bottom assembly views with reference designators, polarity/orientation marks, and mechanical keep-outs.

