

FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO

Design of a Reconfigurable Intelligent Surface with Memristors for Future 6G Applications

Carina Cardoso Silva



Mestrado em Engenharia Eletrotécnica e de Computadores

Supervisor: Prof. Vítor Manuel Grade Tavares

Co-supervisor: Prof. Luís Manuel de Sousa Pessoa

October 26, 2025

Design of a Reconfigurable Intelligent Surface with Memristors for Future 6G Applications

Carina Cardoso Silva

Mestrado em Engenharia Eletrotécnica e de Computadores

October 26, 2025

Resumo

Os sistemas de comunicação sem fios de próxima geração, 6G, pretendem elevar a conectividade a um novo patamar, atendendo às crescentes exigências de transferências de dados em altíssimas velocidades, cobertura onnipresente e redes energeticamente eficientes. De modo a alcançar estes objetivos ambiciosos, são necessários avanços revolucionários na tecnologia sem fios, sendo as Superfícies Inteligentes Reconfiguráveis (RIS) uma solução importante. Esta tecnologia proporciona a manipulação dinâmica de ondas eletromagnéticas, redirecionando os sinais de forma inteligente para melhorar a conectividade, a cobertura e a eficiência energética. Estas superfícies de baixo custo e baixo consumo energético podem ser estrategicamente implementadas em ambientes interiores e exteriores para otimizar o desempenho das redes 6G.

O circuito de controlo é um elemento central no funcionamento das RIS, sendo responsável pela gestão do comportamento de cada elemento na superfície. O controlo preciso de cada um desses elementos é essencial para alcançar funcionalidades como direcionamento de feixe (*beam steering*), melhoria de sinal e otimização dinâmica da cobertura. Isto é viabilizado pela integração de circuitos avançados capazes por modificar as propriedades eletromagnéticas da superfície por meio da aplicação de tensões ou correntes externas. Neste trabalho, memristors são utilizados como mecanismo de comutação dentro das células unitárias das RIS graças às suas propriedades não voláteis e operação eficiente em termos energéticos. Ao explorar o controlo baseado em memristors, esta dissertação procura contribuir para o design, a implementação e os testes de um circuito autónomo que permita o controlo de memristors, sendo capaz de alterar dinamicamente as suas características em resposta a diferentes condições de operação.

Assim, esta dissertação descreve as metodologias de hardware e software utilizadas para desenvolver o sistema de controlo das RIS, destacando a sua eficiência energética, escalabilidade e desempenho.

Abstract

The next-generation 6G wireless communication systems will bring connectivity to a whole new level to satisfy ever-increasing demands for ultra-high-speed data transfer, ubiquitous coverage, and energy-efficient networks. Achieving these ambitious goals requires revolutionary advancements in wireless technology, with Reconfigurable Intelligent Surfaces (RISs) emerging as an important solution. RIS technology enables dynamic manipulation of electromagnetic waves, allowing signals to be intelligently redirected to improve connectivity, coverage, and energy efficiency. These low-cost, low-power surfaces can be strategically deployed in both indoor and outdoor environments to optimize the performance of 6G networks.

Central to the operation of RIS is the control circuit, which governs the behaviour of each element on the surface. Precise control of these elements is essential to achieve functionalities such as beam steering, signal enhancement, and dynamic coverage optimization. This is accomplished by integrating advanced circuits that modify the electromagnetic properties of the surface through the application of external voltages or currents. For this work, memristors are employed as the switching mechanism within the RIS unit cells due to their non-volatile properties and energy-efficient operation. By exploiting memristor-based control, this dissertation seeks to contribute to the design, implementation, and testing of a standalone circuit that enables the control of memristors, capable of dynamically altering their characteristics in response to different operating conditions.

As a result, this dissertation outlines the hardware and software methodologies used to develop the RIS control system, emphasizing energy efficiency, scalability, and performance.

UN Sustainable Development Goals

The United Nations Sustainable Development Goals (SDGs) provide a global framework to achieve a better and more sustainable future for all. It includes 17 goals to address the world's most pressing challenges, including poverty, inequality, climate change, environmental degradation, peace, and justice, as seen in Figure 1¹.



Figure 1: United Nations Sustainable Development Goals.

The specific Sustainable Development Goals mentioned have the following names:

SDG 7 Ensure access to affordable, reliable, sustainable and modern energy for all.

SDG 8 Promote sustained, inclusive and sustainable economic growth, full and productive employment and decent work for all.

SDG 9 Build resilient infrastructure, promote inclusive and sustainable industrialization, and foster innovation.

SDG 11 Make cities and human settlements inclusive, safe, resilient, and sustainable.

¹The content of this publication has not been approved by the United Nations and does not reflect the views of the United Nations or its officials or Member States. (See <https://www.un.org/sustainabledevelopment>)

SDG 13 Take urgent action to combat climate change and its impacts.

SDG	Target	Contribution	Performance Indicators and Metrics
7	7.2	RIS technology improves energy efficiency in 6G networks, reducing power consumption while maintaining performance.	Percentage reduction in energy consumption of wireless networks using RIS.
	7.3	Promotes efficient energy use in urban areas by optimizing wireless signal propagation, reducing energy wastage.	Measurement of energy efficiency gains in network deployments.
8	8.2	Supports economic growth by enabling innovative technologies and services like smart cities and IoT, powered by efficient wireless networks.	Number of new applications and services enabled by RIS-enhanced networks.
9	9.4	Facilitates sustainable industrialization by integrating energy-efficient RIS systems into modern infrastructure.	Reduction in carbon emissions from communication infrastructure.
	9.5	Advances scientific research and technological innovation in telecommunications and materials science.	Number of patents, publications, or industry adoption of RIS technologies.
11	11.3	Enhances urban connectivity, improving infrastructure for inclusive, safe, and resilient smart cities.	Percentage of urban areas covered by RIS-enabled 6G networks.
	11.6	Reduces environmental impact by lowering the energy footprint of dense urban communication systems.	Measured energy savings in urban network implementations.
13	13.1	Contributes to climate action by reducing energy consumption in telecommunications, supporting sustainable networks.	Reduction in greenhouse gas emissions from wireless network operations.

Acknowledgements

The completion of this dissertation marks the culmination of a demanding but also rewarding five-year academic journey. This milestone was made possible only by the collaboration, mentorship, and unwavering support of numerous individuals and institutions. I extend my deepest gratitude to all who contributed, directly or indirectly, to the development of this work.

Firstly, I would like to express my sincere gratitude to my supervisor, Prof. Vítor Tavares, for his guidance and rigour, constant support, and detailed explanations throughout the course of this work. I would also like to thank my co-supervisor, Prof. Luís Pessoa, for his valuable insights and availability, which greatly enriched this work.

I would also like to thank INESC TEC's members of the Centre for Telecommunications and Multimedia (CTM), more specifically from the Optical and Electronic Technologies (OET) Research Laboratory, for creating a stimulating and collaborative environment. Particularly Mohamed Ghatas and Abdul Hameed, for their helpful technical assistance throughout the laboratory phase of this work. Furthermore, this work was developed within the TORIS (Towards fully printed reconfigurable intelligent surfaces) project in collaboration with CENIMATli3N, from NOVA FCT, to which I am also grateful.

Special thanks go to my colleagues and friends, for their moral support, proofreading help, and countless motivating conversations. The collective impact of your contributions, both academic and personal, cannot be overstated.

Finally, I extend my heartfelt gratitude to my parents for their ceaseless encouragement, patience, and unconditional love. And who have supported me throughout my life, always believing in me and pushing me to achieve my goals. Without them, this journey would not have been possible.

Thank you all.

Carina Cardoso Silva

“You must do the things you think you cannot do.”

Eleanor Roosevelt

Contents

1	Introduction	1
1.1	Motivation and Context	1
1.2	Problem Statement	3
1.3	Objectives	3
1.4	Contributions	3
1.5	Dissertation Structure	4
2	Literature Review and Background Work	5
2.1	The Future of Communications	5
2.1.1	Antenna Array Technology	5
2.1.2	Metasurfaces	5
2.1.3	Reconfigurable Intelligent Surfaces	6
2.2	Literature Review	7
2.2.1	RIS Reconfigurability Techniques	8
2.2.2	RIS Components	10
2.2.3	Notable Contributions	12
2.3	Memristors	16
2.3.1	Switching behaviour	19
2.4	Mathematical Modelling of Memristors	20
2.4.1	Linear Ion Drift memristive device model (HP Model)	20
2.4.2	Non-linear model	21
2.4.3	Simmons Tunnel Barrier Model	22
2.4.4	ThrEshold Adaptive Memristor (TEAM) Model	24
2.4.5	VTEAM–Voltage ThrEshold Adaptive Memristor Model	25
2.4.6	Vourkas Model	26
2.4.7	Compact (Bipolar/Unipolar) Model	27
2.4.8	Window Functions	28
2.5	SPICE Macromodels	30
2.5.1	LTspice	30
2.5.2	SPICE Models Comparison	31
2.6	Final Comments	32
3	Design and Implementation of a Switching Circuit for Memristor Controlling	35
3.1	Proposed Approach	35
3.2	Electrical Characterisation of Memristors Setup	36
3.3	Type of Measurements	39
3.4	Characterisation Software	40
3.5	Measurement Methodology	40

3.5.1	Typical Procedure	41
3.6	Measurement Results	42
3.7	Conceptual Circuit Description	47
3.7.1	SET control	47
3.7.2	RESET control	48
3.8	Design of the Fundamental Circuit Blocks for Memristor Controlling	49
3.8.1	Ramp Signal generation	49
3.8.2	Controlled Current Source	51
3.8.3	SET stage	52
3.8.4	RESET stage	53
3.8.5	Logic for selection of memristor path	55
3.9	Simulation Process and Results	56
3.10	Final remarks	62
4	Conclusion	65
4.1	Future Work	65
	References	67
A	SPICE Subcircuit Codes	73
B	SMU Scripts	79
C	Characterisation Measurements and Specifications	89
D	LTspice Implementation	91

List of Figures

1	United Nations Sustainable Development Goals.	v
1.1	Evolution of Mobile Networks: From 1G to 6G [6].	2
2.1	Reconfigurable surface [10].	6
2.2	Typical RIS (or IRS) Hardware Architecture [14].	7
2.3	3D view of mechanically proposed RIS unit cell in [20].	9
2.4	Tested RIS in [21].	10
2.5	An example of the tunable reflecting element based on PIN diode [14].	11
2.6	Structure of the designed 2-bit RIS element in [22]	13
2.7	The RIS configuration illuminated by a horn antenna (a) 3D structure including a 10-dBi horn antenna showing a reflected beam steered to an angle of 30° (b) patch and ground layers of 2×2 elements in the array [17].	14
2.8	Unit cell based on SRR. (A) Perspective view. (B) Top view. [24]	14
2.9	Schematic model of the metaparticle, adapted from [28].	15
2.10	Illustration of the proposed active RIS constructed from 4×4 elements [29]. . . .	15
2.11	The four fundamental passive two-terminal circuit elements: resistor, capacitor, inductor and memristor [38]. Courtesy of Encyclopædia Britannica.	18
2.12	I-V relationships of the four fundamental circuit elements: (A) resistor, (B) capacitor, (C) inductor, and (D) memristor [41].	19
2.13	Schematic representation of memristor I-V curve switching behaviour. (A) Unipolar switching; (B) Bipolar switching. CC refers to the compliance current. [30] .	20
2.14	Cross-section of the first HP TiO ₂ -memristor consisting of a high conductive (doped) and a low conductive (undoped) part placed in between two platinum electrodes [39].	21
2.15	Simmons tunnel barrier physical model. x is the state variable and the width of the oxide region, V corresponds to the applied voltage on the device, v_g is the voltage in the undoped region, and v is the device's internal voltage [49].	23
2.16	Proposed unipolar memristor model in [54].	28
2.17	Memristor testing circuit designed on LTspice.	31
3.1	Schematic of the RIS control circuit.	36
3.2	This diagram represents the memristor characterisation setup employed at INESC TEC OET Lab. It starts with a computer operating on the Windows platform, which interfaces with a Keysight B2902A SMU via a USA-A-USB-B cable. The SMU then communicates with the probes present in the probe station using banana jacks. The SMU also interfaces back with the computer, completing the setup. Adapted from [41].	37
3.3	SemiProbe Lab Assistant manual wafer probe station.	38

3.4	Motic SMZ-171 Microscope.	38
3.5	Laboratory setup used for the electrical characterisation of the memristors.	38
3.6	Flowchart illustrating the systematic protocol for evaluating memristors. Here, the "Retry Process" is inserted to emphasize trying to replicate previous results.	41
3.7	Illustration of the tested devices.	43
3.8	Device 8 from 2 nd Quadrant, ON sweep, iteration 1.	44
3.9	Device 8 from 2 nd Quadrant, Pulse train RESET, iteration 1.	45
3.10	Device 8 from 2 nd Quadrant, ON sweep, iteration 5.	45
3.11	Device 8 from 2 nd Quadrant, OFF sweep, iteration 5. Neither OFF sweep nor pulsing could switch the device to HRS.	46
3.12	Boxplots of ON (LRS) and OFF (HRS) resistances for working devices. Points show raw data; dashed lines indicate means.	47
3.13	Switching blocks for the memristor SET control.	48
3.14	Switching blocks for the memristor RESET control.	48
3.15	Circuit with highlighted blocks.	49
3.16	Ramp signal generation.	50
3.17	Current source.	51
3.18	Full controlled current source equivalent.	52
3.19	PMOS transistor that provides the current for the SET operation.	53
3.20	Components that provide the voltage for the RESET operation.	54
3.21	Non-inverting input for the opamp.	54
3.22	Final paths for the memristor control.	55
3.23	Logic Gates Implementation.	56
3.24	555 Timer IC Pin Diagram.	57
3.25	Output signal of the 555 timer circuit.	57
3.26	LTC6992 Voltage-Controlled Pulse Width Modulator example pin diagram [58].	58
3.27	Configuration for PWM signal to reach desired supply voltage.	59
3.28	Pulse signal generated by the LTC6992, after connecting the NPN transistor and pull-up resistor.	60
3.29	Ramp signal generated by the circuit.	60
3.30	Output signals of the logic gates/signals that are applied onto the PMOS transistors.	61
3.31	Excerpt of the output signal applied to the memristor during the SET operation.	61
3.32	Excerpt of the output signal applied to the memristor during the RESET operation.	62
D.1	LTspice Schematic of Memristor Control Circuit.	92
D.2	LTspice Schematic of Pulse Generation Components.	93

List of Tables

2.1	Summary of Reviewed Works on Reconfigurable Intelligent Surfaces (RIS) . . .	16
2.2	Comparison of Different Memristive Device Models.	32
3.1	Electrical parameters applied onto devices for ON current sweep.	42
3.2	Electrical parameters applied onto devices for OFF voltage sweep.	42
3.3	Electrical parameters applied onto devices for RESET pulse.	42
3.4	Electrical characterisation results of device no. 8.	44
3.5	Truth table for the logic gates.	55
C.1	Electrical characterisation results of device no. 1.	89
C.2	Electrical characterisation results of device no. 2.	89
C.3	Keysight B2902A Source and Measurement Specifications.	90

List of Acronyms

3D	Three-dimensional
5G	Fifth Generation
6G	Sixth Generation
B5G	Beyond 5G
CMI	Compact Model Interface
DC	Direct Current
EM	Electromagnetic
FET	Field-effect Transistor
FPGA	Field-Programmable Gate Array
GSG	Ground-Signal-Ground
HP	Hewlett-Packard
LoS	Line-of-Sight
MCU	Microcontroller Unit
MEMS	Micro-electromechanical Systems
MIM	Metal/insulator/metal
NLoS	Non-Line-of-Sight
PIN	Positive-Intrinsic-Negative
QoS	Quality-of-Service
RF	Radio Frequency
RIS	Reconfigurable Intelligent Surfaces
RLC	Resistor-Inductor-Capacitor Circuit
SMU	Source/Measure Unit
SNR	Signal-to-noise Ratio
SOLT	Short-Open-Load-Through
Tbps	Terabit per second
THz	Terahertz
UAV	Unmanned Aerial Vehicle
UE	User Equipment
VNA	Vector Network Analyser
VTEAM	Voltage ThrEshold Adaptive Memristor
ZB	Zettabyte

Chapter 1

Introduction

1.1 Motivation and Context

Currently, fifth-generation (5G) wireless networks are being deployed worldwide, but they are already becoming insufficient for the rapidly increasing pace of global wireless communications [1]–[3]. According to Chen, Liu, Hui, *et al.* [2], the extensive global mobile traffic is increasing at an annual rate of approximately 55%, with projections indicating it will surpass 5 ZB/month in 2030 [2], [4]. Moreover, the estimated number of global mobile subscriptions is projected to reach 8.8 billion in 2026 [4] and 17.1 billion in 2030 [2]. In addition, as indicated in [5], 6G networks are projected to serve higher numbers of users, reaching up to 10^7 users per square kilometre, while delivering downlink data rates of 1 Gbps. Hence, achieving an end-to-end communication latency even below 1 millisecond with 99.99999% network reliability is considered an essential goal [5].

This exponential growth of data-driven applications and the unprecedented demand for ultra-fast, energy-saving, and reliable connectivity (data delivery) are propelling the global telecommunications industry towards the sixth generation (6G) of wireless communication systems [3]. Coupled with a massive increase in spectrum, augmenting data throughput to great dimensions and lowering latency, 6G promises to drive new applications such as holographic communication and digital twinning. Nonetheless, attaining these ambitious goals, set out by the International Mobile Telecommunications-2030 (IMT-2030) for 6G networks [5], demands an architectural leap—one that challenges traditional paradigms and seeks innovative solutions to efficiently harness and manipulate wireless environments [1], [3].

Following this, migrating from 5G to 6G is essential, and thus, the energy and spectrum efficiency must be improved to provide the best quality-of-service (QoS) possible. Figure 1.1 highlights the societal and business call to achieve higher data rates and more fidelity in 6G, which requires the allocation of broader spectrum blocks at higher frequency bands than those currently in use [1].

With a higher frequency band in use comes the problem of unreliability in wireless propagation. Recently, with the idea of controlling the wireless channel itself through the use of RISs, this

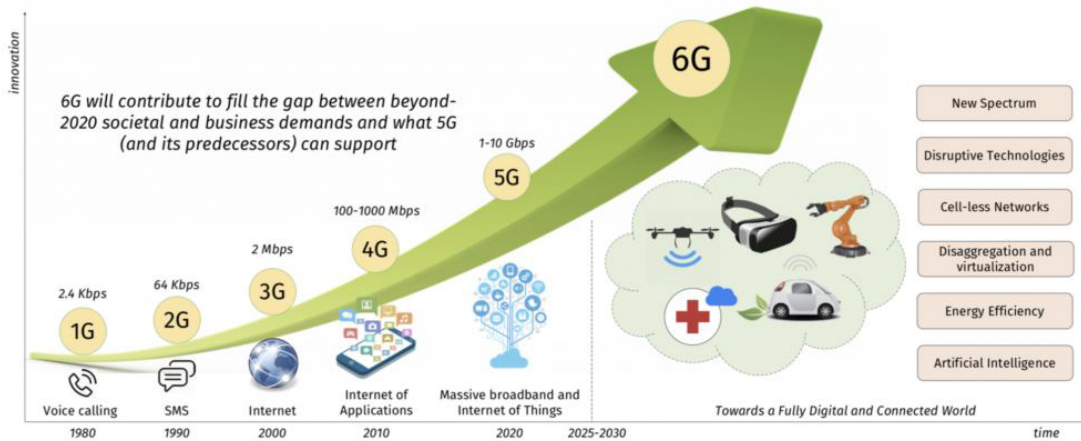


Figure 1.1: Evolution of Mobile Networks: From 1G to 6G [6].

can become a solvable problem. Instead of treating reflection and scattering in the environment as uncontrollable phenomena whose effects can only be modelled stochastically, they become part of the system parameters that may be optimised and can overcome many of the challenges of wireless communications [1].

The control of electromagnetic (EM) beams has been an important goal in several fields, including medical imaging, nanolithography, and, more recently, wireless communications. Techniques like reflectarrays, metamaterials, and spatial light modulators since the early 2000s have inspired the implementation of Reconfigurable Intelligent Surfaces (RIS) in wireless communications [2], [7], [8]. RIS, large intelligent surfaces (LIS), Reconfigurable or Intelligent Reflecting Surface (IRS), are capable of generating a dynamic directional beam at a low cost and with low complexity [8], [9]. A smart controller manages each unit cell of the RIS individually, enabling the adjustment of its reflection properties to dynamically shape a directional beam that adapts to the user's location [1], [9]. The primary advantage of a RIS lies in its ability to transform the wireless environment by altering the channel between the transmitter and receiver, ultimately enhancing overall system performance [10].

In this fashion, due to the low profile, lightweight, and small geometry with low cost and high flexibility of RISs, they can be integrated into existing networks without changing hardware and standards, but only the communication protocols [2]. For these reasons, they can be easily deployed in a variety of settings, be it stationary or moving objects, and even on people. On that account, RISs will have the opportunity to accommodate the 6G space-air-ground-underwater/sea integrated network in the future to further realise the vision of the IoT. Their applications range from satellite communication, unmanned aerial vehicle (UAV) communications, ultradense ground networks, underground and marine communications networks, for smart cities (smart homes, autonomous driving, smart factories, smart healthcare, etc.), industry 4.0, and positioning indoors and outdoors [2], [4].

1.2 Problem Statement

The aim of this dissertation is to design an electronic circuit responsible for controlling switching devices (memristors) for future integration with RISs in 6G. The memristor as a switching device is relevant in a way that one can turn on and off the antenna elements with the device not taking power once its internal state is defined. Memristors offer distinct advantages for RISs by allowing each surface element to retain its state without the need to apply constant power, thus enhancing both energy efficiency and reconfigurability.

By integrating memristors into RISs design, this work proposal aims to address the existing limitations of traditional RIS components and align the technology with the high-performance demands of 6G.

1.3 Objectives

Having selected a method for antenna beamforming through RIS and a means for efficient switching and control of the basic RIS units, the work of this dissertation involves building the electronic memristor control for a RIS. The main objectives of this dissertation's work include:

- Provide an intensive electrical characterisation of the available fabricated memristors and distinguish between the important measurement and sourcing of the devices;
- Develop the memristor-based electronic control of the RIS, based on the obtained results;
- Design and simulate the memristor-based electronic control circuitry.

1.4 Contributions

This dissertation contributes to the field of wireless communications by exploring the integration of memristors into Reconfigurable Intelligent Surfaces (RISs) for 6G networks. The key contributions include:

- A comprehensive review of memristor models and their applicability in RIS technology, providing a foundation for future research in this area.
- The design and implementation of a memristor-based control circuit for RIS unit cells, demonstrating the feasibility of using memristors for energy-efficient switching in wireless communication systems.
- Co-authoring a paper to be submitted to the 20th European Conference on Antennas and Propagation (EuCAP).

1.5 Dissertation Structure

In addition to the introduction, this dissertation contains three more chapters.

In Chapter 2, the literature review and background work are described. Chapter 3 discusses the design and implementation process, including an electrical characterisation of memristors and coverage of the simulation process and its outcomes. Finally, Chapter 4 encompasses the definitive conclusion of the accomplished efforts and future work directions.

Chapter 2

Literature Review and Background Work

This chapter highlights the fundamental aspects regarding Reconfigurable Intelligent Surfaces and Memristors that are essential for the full comprehension of this document.

2.1 The Future of Communications

2.1.1 Antenna Array Technology

Antenna array technology allows the directional transmission and reception of wireless signals, enabling advanced applications in communication, localisation, and sensing [11]. Moreover, electrically tunable reflecting antenna arrays can be used to dynamically adjust their radiation patterns [12]. As a result of this, for communication purposes, the arrays are used to form beams in desired directions to improve the signal-to-noise ratio (SNR), multiplex data signals in the spatial domain (to one or multiple devices), and suppress interference by spatial filtering [11]. In essence, antenna arrays are used as reflecting structures [12].

2.1.2 Metasurfaces

When an electromagnetic beam travels from one isotropic medium to another, the relationship between the angle of incidence and angle of reflection and refraction is governed by Snell's law. Particularly for the reflection, for regular surfaces of a medium, the angle of incidence is the same as the angle of reflection, as shown in Figure 2.1a [10].

However, in the Terahertz band, waves are more prone to be absorbed by atmosphere gases due to water vapour or oxygen molecules. A line-of-sight (LoS) link may enjoy high channel gain, but will probably suffer from a spatially-sparse low-rank channel, limiting the number of spatial streams and consequently the achievable rate of higher frequency bands. Being spatially sparse, these channels need a way to have a centralized beamformer to increase channel gains and to create a propagation path around major obstacles to restore a link in an outage [13].

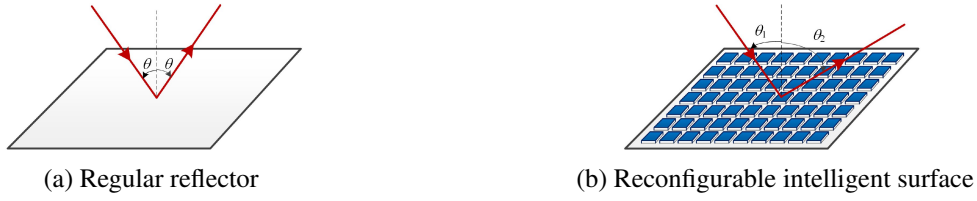


Figure 2.1: Reconfigurable surface [10].

If the regular surface previously shown is divided into a large number of closely spaced elements and each metasurface element is made to have appropriate phase shifts, the EM wave can be tuned to some other angle instead of the symmetric reflective wave based on Snell's law. Ideally, as shown in Figure 2.1b, if the phase shift of each metasurface element can be configured to any value, a reflected beam can be formed at any angle [10].

To create a reflected beam from an incident EM wave, it is essential to adjust the phase shift of the surface element accurately. This can be achieved using signal processing design techniques or machine learning-based approaches, leading to the development of a RIS [11].

2.1.3 Reconfigurable Intelligent Surfaces

Reconfigurable Intelligent Surfaces are a flat array of numerous ultra-thin meta-atoms (also called unit cells or elements), each capable of assuming multiple digitalised states, which correspond to distinct EM responses. Since the beginning of the 21st century, tunable meta-atoms have been an active area of research, including diverse technologies that vary with the operating frequency. For instance, PIN diodes and varactors are used for frequencies up to millimetre waves, while liquid crystals, graphene, vanadium dioxide, memristors, and microfluidics are employed for terahertz (THz) frequencies [7].

Each of these tunable-state meta-atoms can independently impose the required phase shift on the incoming signal. RIS can be categorized into two main types based on the materials used for the reflecting elements: antenna-array-based and metasurface-based structures. By meticulously controlling the phase shifts of each reflecting element, the reflected signals can be redirected towards the desired directions. The rapid advancements in metamaterials enable real-time adjustment of the reflection coefficient of each element, allowing the RIS to adapt to dynamically fluctuating wireless environments [1]. Using the metasurface implementation, a RIS element can not only scatter and phase-shift signals but also function as an anomalous mirror with controllable reflection angles and the ability to manipulate polarization [13]. These make them very interesting candidates for communication applications in 6G networks [1].

As illustrated in Figure 2.2, a typical RIS architecture (alternatively named in [14] as IRS), constructed using metamaterials, primarily includes a planar surface and an integrated controller. The planar surface generally consists of one or multiple layers, depending on the design requirements [15]. In this case, the design consists of three layers along with a controlling device. The outer layer consists of numerous metallic patches (tunable elements) embedded over a dielectric

substrate that directly communicates with the incoming signal. A copper plate is placed beneath the outer layer to prevent signal loss. The inner layer contains the control circuit board that interacts with the controller and regulates the phase shift and reflection coefficient of each reflective element [14], [16]. The RIS controller is built with a microcontroller unit (MCU) or a field-programmable gate array (FPGA) device, acting as a gateway for communication with the NGBS and other network components over a dedicated cable-wired or wireless connection. Typically, the Next-generation Base Station (NGBS) calculates the ideal phase shifts of the RIS and sends them to the RIS through the controller. An FPGA's higher clock speed makes it suitable for 6G communication applications that require fast switching operations [16].

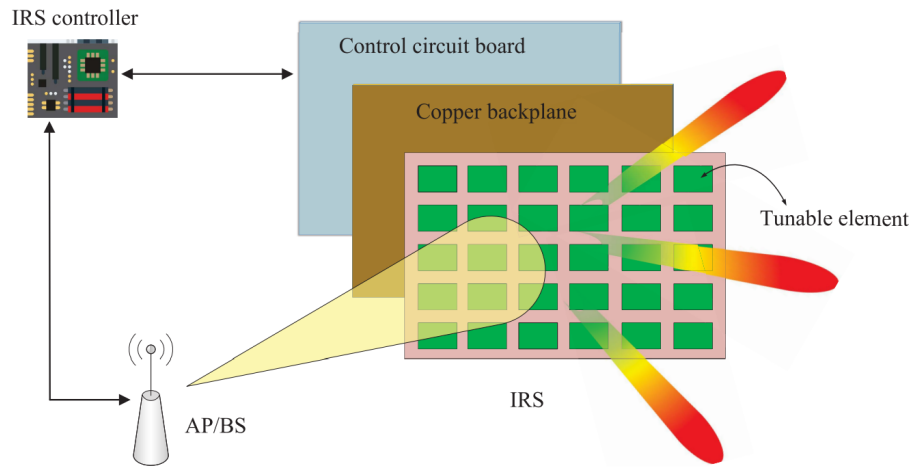


Figure 2.2: Typical RIS (or IRS) Hardware Architecture [14].

The importance of RISs lies in its potential to fundamentally reshape wireless communication systems. By enabling dynamic adjustment of signal reflections, RIS can enhance communication coverage, improve throughput, and increase energy efficiency—all while maintaining cost-effectiveness through its passive architecture. Its ability to operate noiselessly in full-duplex mode, combined with its energy-efficient design, positions RIS as a key enabling technology for beyond 5G (B5G) networks. The RIS-aided network would become transformational beyond connecting transceivers to become an innovative space with distributed intelligent communications, sensing, and computing platforms. To put it more succinctly, oftentimes, a RIS-assisted network is considered to be an intelligent radio environment where the propagation environment is transformed into a smart reconfigurable space capable of playing an effective role in transferring and processing information [4].

2.2 Literature Review

Despite its promise, RISs implementation for 6G systems presents several technical challenges, primarily in scalability, energy consumption, and latency management. Each meta-atom in a RIS

requires independent configuration to adapt dynamically to changing network demands, necessitating extensive control circuitry and consuming significant power. This issue intensifies as RIS arrays scale up to support broader coverage and higher data rates, making traditional semiconductor-based systems less viable for large-scale, sustainable deployment.

The power demand for large-scale RIS is particularly problematic in energy-sensitive 6G applications. Furthermore, RIS units need to operate with minimal latency to accommodate real-time applications, which places additional demands on the hardware and control systems managing each RIS element. These challenges underscore the need for innovative materials and electronic designs that can reduce power demands and support efficient, large-scale RIS operation [17].

This section presents an overview of existing approaches to the implementation of RIS, with a focus on key aspects such as control mechanisms for electromagnetic properties and practical deployment in real-world environments.

First, methods for controlling the electromagnetic behaviour of RIS unit cells will be discussed, given that such control is at the heart of the reconfigurability issue. Different techniques will be reviewed and compared regarding the actuation of the reflective surface of unit cells in view of feasibility, scalability, and performance. After that, the RIS components used to achieve such reconfigurability are reviewed one by one, together with their practical validation and performance in experimental settings. By comparing these approaches, this section aims at highlighting strengths and limitations of current RIS technologies, thus providing a fruitful basis for future research and development in the area.

2.2.1 RIS Reconfigurability Techniques

As mentioned above, a RIS is built from a reconfigurable metasurface, which can fully control the phase shifts incurred by individual scattering elements. In order to reconfigure the RIS elements, the electromagnetic properties of the reflective components of the antenna need to be changed. This can be achieved by imposing external stimuli on the scattering elements and thus alter their physical parameters, leading to the change of EM properties of the metasurface without refabrication [18].

As displayed in Figure 2.2, a typical RIS architecture is comprised of three layers and a smart controller. The outermost layer features a dense array of tunable metallic patches on a dielectric substrate, enabling direct manipulation of incident signals. A copper plate in the intermediate layer minimizes signal leakage during reflection. The innermost layer houses the control circuitry, responsible for activating the reflecting elements and dynamically adjusting their reflection amplitudes and/or phase shifts [14].

A smart controller, often implemented using an FPGA, governs the reflection adaptation for each IRS. This controller also acts as a gateway for communication with other network components (e.g., base stations, access points, and user terminals) via wired or wireless backhaul/control links [14]. To enhance environmental learning, dedicated sensors can be integrated within the first layer, potentially interlaced with the reflecting elements. These sensors collect data on surrounding radio signals, aiding the smart controller in optimizing reflection coefficients [14].

Although there are several approaches for reconfiguring RIS elements, the three main approaches are mechanical actuation, functional materials, like liquid crystals and graphene, and electronic devices like (PIN) diodes, field-effect transistors (FETs), MEMS switches and memristors [14], [19].

Mechanical Reconfiguration

In mechanical reconfiguration, the antenna's primary radiating element undergoes physical changes to adapt its characteristics. This approach stands out by avoiding the integration of active components, biasing circuits, or intricate switching systems, which are common in other reconfiguration techniques [19]. For instance, in [20], mechanical reconfiguration allows the proposed RIS unit cell to achieve a 180-degree phase shift at 28 GHz, depicted in Figure 2.3, while its design also contributes to cost-effective fabrication.

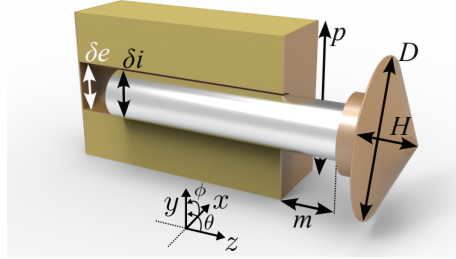


Figure 2.3: 3D view of mechanically proposed RIS unit cell in [20].

However, mechanical reconfiguration exhibits limitations in terms of performance adaptability and faces challenges in achieving multi-functional reconfigurable capabilities [19].

Optical Reconfiguration

This reconfiguration technique relies on photoconductive switches, semiconductor devices made from materials like silicon or gallium arsenide. In optical reconfiguration, these switches eliminate the need for metallic wires, and their bias lines provide superior performance, with less interference and higher isolation compared to electrical switches. Remarkably, they exhibit exceptionally fast switching speeds, operating within nanoseconds. By utilizing photoconductive switches, it becomes possible to optically control an antenna's operational bandwidths and its radiation pattern [19].

Electrical Reconfiguration

Lastly, this reconfiguration method relies on electronic switching components, including PIN diodes, varactors, MEMS and memristors to alter the antenna's characteristics. By incorporating these switches, the antenna's structure can be dynamically modified, resulting in a redistribution of

surface currents and subsequent changes in the antenna's frequency, radiation pattern, and polarization [19]. The implementation of reconfigurable antennas using switching elements is relatively straightforward and has attracted considerable research interest.

2.2.2 RIS Components

In the present section, different RIS components that can reconfigure metasurfaces will be examined, including PIN diodes, varactors, or MEMS switches, or memristors [19]. This is the approach that will be employed to reconfigure the RIS elements in this dissertation's work.

Patches

As stated earlier, the RIS's outer layer is made up of numerous tunable metallic patches, as seen in Figure 2.4, printed on a grounded dielectric substrate to directly manipulate incident signals [14], [21]. The rectangular patch, etched onto the bottom of the top layer substrate, receives electromagnetic waves from the feedhorn antenna and re-radiates them with a phase shift [22].

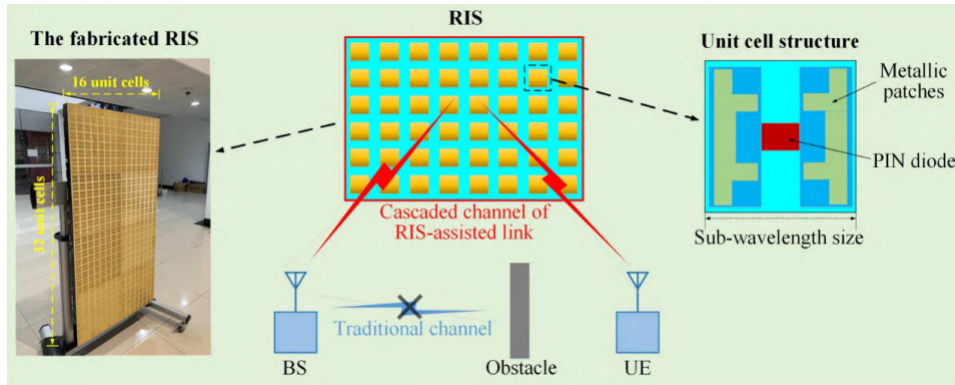


Figure 2.4: Tested RIS in [21].

Dielectric Substrate

As noted above, the metallic patches of RIS are printed on dielectric substrates [14]. The substrate selection significantly influences the performance of the RIS, impacting antenna radiation patterns, the frequency at which it operates, input impedance, and overall system efficiency [23].

Varactor Tuning Diodes

Varactor diodes are usually embedded into RIS architectures, either on their radiating patch or the feeding line [19]. Therefore, reconfigurable designs often incorporate varactors to achieve the frequency tuning function. The application of varying voltage levels results in a change in the varactor's capacitance, thereby modifying the antenna's frequency [19].

Typical values for the (reverse) voltage range are 0-20 V corresponding to an equivalent capacitance range of a few pico-Farad, e.g. 0.5- 3.5 pF, for commercially available diodes that are

compact enough to be integrated on GHz-band metasurfaces [18]. Additionally, varactor diodes enable smooth phase tuning with minimal power consumption, achieving the desired phase shifts by simply adjusting voltage levels [24].

In [24], the authors propose a varactor-based RIS design, loaded with these diodes for tuning the uni cells for mm-waves. It generates reconfigurable reflected beams from incident plane waves by changing the metasurface phase profile.

PIN Diodes

PIN diodes are widely used as switching components in several wireless systems. For reconfigurable antennas, an additional dimension for the RF and the direct current (DC) blocks is required and should be considered in the design of the antenna [19]. The equivalent circuit of the diode is carried out with lumped RLC boundary condition in the ON and OFF states [22], illustrated in Figure 2.5.

The designed RIS element, reported in [22], comprises a multi-layered structure featuring two dielectric substrates and three metallic layers. A rectangular patch, etched on the bottom surface of the top substrate, serves as the radiating element, receiving electromagnetic waves from the feedhorn antenna and subsequently re-radiating them with a controlled phase shift. A slotted stripline, etched on the top surface of the bottom substrate, is segmented into three sections by two PIN diodes. These segments are connected to inductance and DC bias circuits. The inductance isolates the DC bias circuit from the RF circuitry. By applying DC bias to the PIN diodes, their on/off states modulate the effective resonance length of the RIS element, enabling 2-bit phase shift control. The DC bias line is routed through a metallic via, minimizing layout-induced disturbances on the ground plane and enhancing the reflection performance of the RIS [22].

The PIN diode needs a high tuning speed, a high direct current (DC) bias current in the ON-state and a high power-handling capacity. It is very reliable and extremely low cost, making it a good choice for a reconfiguration technique [19], as also displayed in Table 2.1. Notwithstanding, existing energy efficiency optimization studies often oversimplify PIN diode power consumption by neglecting its characteristics of the ON and OFF states. This simplification leads to substantial errors in power estimation, hindering the achievement of optimal energy efficiency [25].

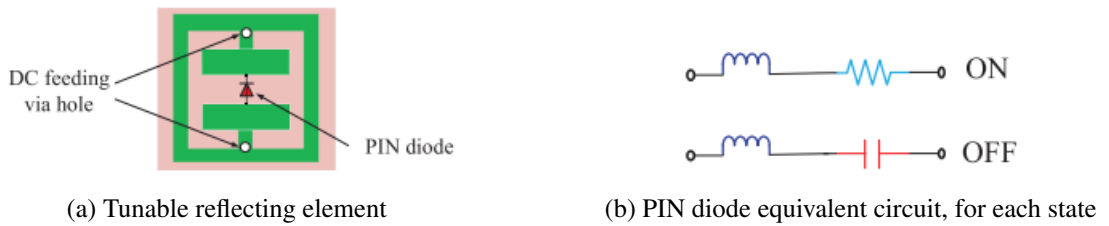


Figure 2.5: An example of the tunable reflecting element based on PIN diode [14].

MEMS

Micro-electromechanical system (MEMS) based switches operate through the use of mechanical movement to achieve a short or open circuit in RF circuits [19]. RF MEMS switches exhibit excellent properties such as low power consumption, high linearity, low loss, and high isolation. In addition to these advantages, MEMS can be integrated into the antenna design to achieve a higher degree of functionality [26]. However, when compared with other RF switches, MEMS require a high-control voltage and have a slow switching speed and a limited life cycle which aren't ideal conditions [19].

Memristors

As stated earlier, over the past few decades, various techniques have been employed to achieve reconfigurability in RISs, including PIN and varactor diodes, liquid crystals or graphene. However, these elements are ill-advised, as they manifest volatile switching behaviour, requiring constant power consumption to maintain the desired switch states. This brings about an energy demand that may not be a sufficiently environmental-friendly solution for this technology's widespread deployment across large areas of urban infrastructure [17].

To mitigate this problem, memristors have proved to be a fitting option to use for a higher range of frequencies, a core feature for future 6G applications. This solution considers the static power consumption issue, since it does not require an applied voltage to maintain its desired state of a RIS. Offering fast switching times, low resistance on the ON state, as well as a small size and low capacitance. Moreover, memristors are constantly being researched on to achieve more and more energy efficient manufacturing processes, which can turn them the decisive contender for a fully integrated RIS manufacturing process [17]. Memristors also offer the advantage of a small footprint, typically a few micrometers or less. Their low-temperature thin-film processing, which requires no specific substrate, enables direct fabrication on the RIS substrate, thus eliminating the need for soldering and traditional component packaging [27]. While the literature has introduced the memristor as an RF switch, it is still weak in realistic communication models that consider actual assumptions and factors regarding the use of memristors for RIS applications and, consequently, for real applications in the wireless communication world. This makes this work a pioneering effort in this area.

A dedicated description on memristors is presented in the Section 2.3 and in Chapter 3, where the electrical characterisation of memristors is discussed in detail. This characterisation is crucial for understanding their behaviour and performance in various applications, including their potential use in RISs.

2.2.3 Notable Contributions

The evolution of RIS has catalysed significant advancements in wireless communication, particularly in addressing the challenges posed by higher frequency bands and the stringent requirements of future 6G networks. Researchers have explored various innovative approaches to optimize the

design, functionality, and scalability of RIS systems, leading to numerous groundbreaking contributions. This section highlights notable advancements in the field, showcasing diverse methodologies for RIS implementation, including the development of tunable elements, advanced control circuits, and novel configurations. By summarizing these contributions, this section provides a comprehensive overview of the most notable contributions on the topic and lays the foundation for the research focus of this dissertation.

In [22], a novel 2-bit wideband beam-scanning Reconfigurable Intelligent Surface with 16×16 elements has been designed and simulated. 2-bit phase resolution is realised by placing two PIN diodes in the stripline for each element. The simulated results of the RIS element, in Figure 2.6, show that the designed element has good performance of phase resolution and low reflected gain loss within the designed bandwidth. The simulations of 2-bit RIS array clearly show that the reflected beams scan from 0° to 60° range at 5GHz. In this implementation, -3dB bandwidth is realised from 4.8GHz to 5.5GHz when the scanning angle is set at 0 degree.

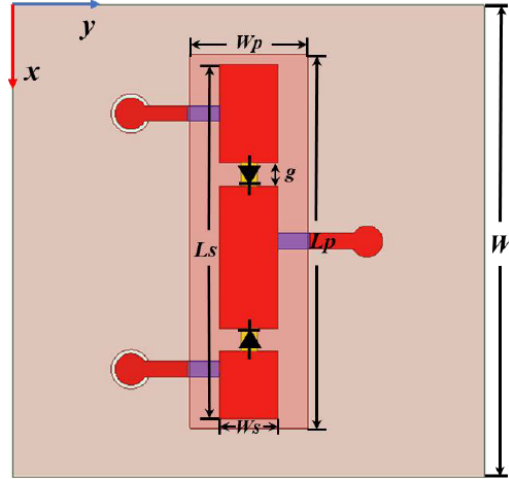


Figure 2.6: Structure of the designed 2-bit RIS element in [22]

In [17], a 1-bit memristor-based reconfigurable RIS unit cell was designed in the Ka-band, and validated using CST and HFSS simulation platforms. The required control circuit to enable the digital control of the memristor has also been proposed. The proposed unit cell achieves losses of less than 1 dB over a frequency band of 25-28.3 GHz and a phase difference of $180^\circ \pm 20^\circ$ at a central frequency of 26.7 GHz, with an operational bandwidth of approximately 1 GHz. Furthermore, an exemplary 16×16 RIS was designed and simulated based on the proposed unit cell to demonstrate its capability to achieve beam steering, as seen in Figure 2.7.

The authors in [24] report a varactor-based 1024-element RIS design and its numerical system-level performance analysis using an RCS-based approach. The varactor unit cell can be seen in Figure 2.8. The proposed RIS consists of a 2-bit unit cell loaded with varactor diodes, arranged in a 32×32 matrix operating at 24.5 GHz under incident plane waves. This RIS is envisioned for mm-wave scenarios, primarily to extend coverage in the azimuth plane. Beamsteering was demonstrated from -60° to 60° in the azimuth plane, with approximately 3 dB scan loss at each

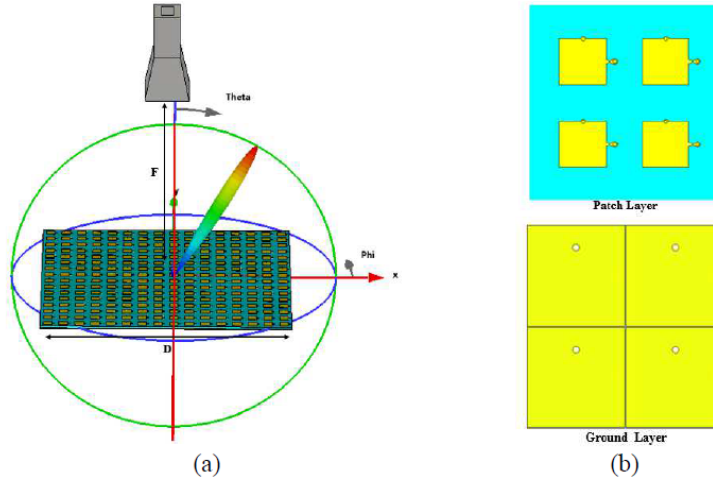


Figure 2.7: The RIS configuration illuminated by a horn antenna (a) 3D structure including a 10-dBi horn antenna showing a reflected beam steered to an angle of 30° (b) patch and ground layers of 2×2 elements in the array [17].

direction. Furthermore, an angle reciprocity analysis was conducted to validate the proposed RIS operation at both orientation angles. The results showed angular reciprocity for up to 110° , even under oblique incident waves in both directions, which, according to the authors, represents the highest RIS angular reciprocity reported in the literature.

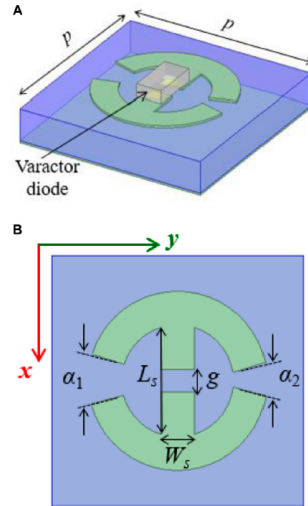


Figure 2.8: Unit cell based on SRR. (A) Perspective view. (B) Top view. [24]

A novel reconfigurable metasurface that integrates varactor and PIN diodes loaded on each metaparticle is presented in [28]. By controlling the different EM functionalities it can be dynamically switched as desired. The beam-splitting performance of the proposed metasurface is validated by constructing antiphase distribution, and its frequency reconfiguration property can be also realised by further changing voltage configurations imparted on the diodes. This functionality makes the metasurface achieve radar scattering section reduction at variable frequency

bands. Additionally, through innovative design of gradient phase distribution, this metasurface is verified to achieve single-beam steering and each of the steering angles is dependent on the gradient phase difference that is tunable. Another functionality of the proposed metasurface is polarization conversion due to its anisotropic structure. By employing the phase difference between two orthogonal directions, the incident linearly polarized wave can be transformed to the circular polarized wave with different handednesses [28].

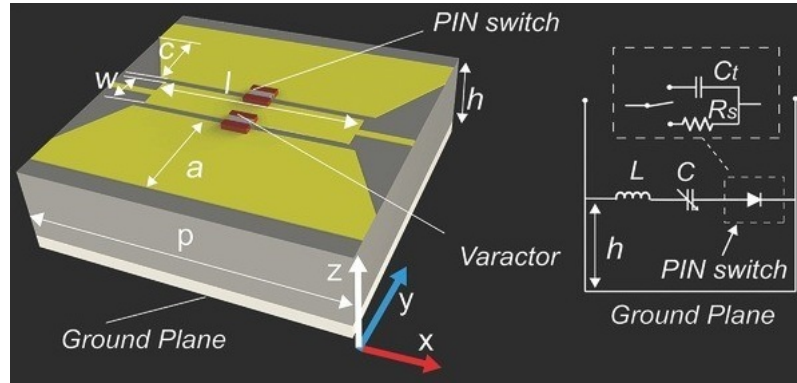


Figure 2.9: Schematic model of the metaparticle, adapted from [28].

In [29], a design for an active RIS with beam-scanning and amplification capability has been described. The active RIS comprises a number of active elements containing two main components: a two-layer patch antenna and a phase-reconfigurable reflection amplifier, as seen in Figure 2.10.

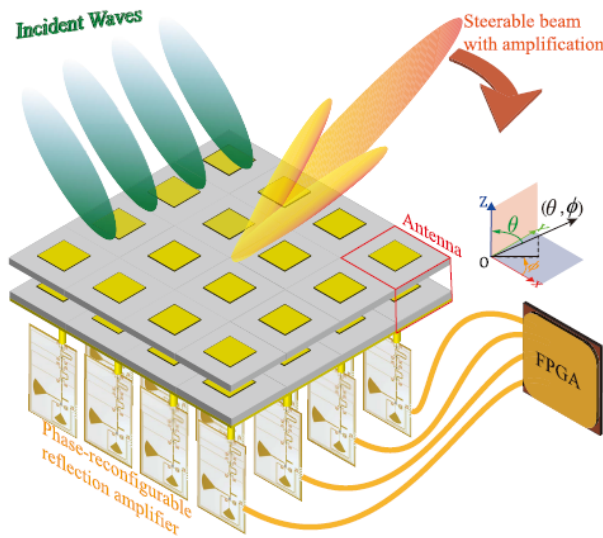


Figure 2.10: Illustration of the proposed active RIS constructed from 4×4 elements [29].

By employing a controlling system, here, an FPGA, the phases of the phase-reconfigurable reflection amplifiers are precisely adjusted. This dynamic control allows for beam steering and the

generation of complex wavefronts by configuring the elements with the desired phase shifts. Theoretical analysis and numerical examples were provided to quantify the trade-offs between the reflection amplifier's gain and the phase shifter's loss. Guided by the analysis, the reflection amplifier was designed to have a gain of about 13 dB, and the phase shifter was designed with 1.9-dB insertion loss and 25-dB return loss. In addition, an analytical method has also been described to calculate the scattered pattern by the active RIS with active devices, such as transistors. The proposed RIS with 2×2 elements could effectively steer a beam with 8.5-dB gain, and the scanning range depends on the size of the RIS.

A summary of the presented methodologies and their corresponding applications is provided in Table 2.1, offering a comprehensive snapshot of current advancements and applications of RIS technology.

Table 2.1: Summary of Reviewed Works on Reconfigurable Intelligent Surfaces (RIS)

Reference	Controller	Phase Control Mechanism	Year	Bandwidth Achieved	Functions of RIS
[28]	DC bias circuit	Hybrid phase control with varactor and PIN diodes	2017	Variable, RCS reduction at multiple bands	Beam splitting, frequency reconfiguration, polarization conversion, single-beam steering
[22]	DC bias circuit	PIN diodes	2021	4.8-5.5 GHz at 0° scan angle	Beam scanning (0° to 60° range), phase resolution, low reflected gain loss
[24]	DC bias circuit	Varactor diodes	2023	24.5 GHz	Beam steering (−60° to 60°), angular reciprocity
[29]	FPGA	RF Switches	2023	2401-2495 MHz	Beam scanning, amplification, phase reconfiguration, gain enhancement, active RIS
[17]	FPGA	Memristors	2024	25-28.3 GHz (1 GHz bandwidth)	Beam steering with 16×16 RIS, low reflection losses

2.3 Memristors

The first switching mechanisms were elucidated in the late 1990s with a wide variety of oxide systems [30]. Today, common studies depict memristive switching behaviour on the basis of a popular thin-film metal/insulator/metal (MIM) configuration, where the insulator layer is comprised of one or more metal oxides possessing semiconducting properties. For a physical Metal-Insulator-Metal (MIM) device to function as a memristor, it must exhibit tunable, quasi-stable internal resistive states. The instantaneous resistive state of the device depends on different key factors, of which

the applied electric field and compliance current can be externally manipulated during device characterisation. Other restricted synergistic determinants, including (i) electron mobility, (ii) gradient of species concentrations (cations and/or anions), and (iii) gradient of temperature within the insulator region, closely depend on the solid-state properties of the semiconducting material [30]. The fabrication process of memristor material involves a high likelihood of the material to lattice defects and grain boundaries [31]. Additionally, filament growth is an arbitrary process, leading to the device's random and unstable switching behavior. To improve performance, two main approaches are utilised: using material composites and modifying the material's surface and morphology. For example, techniques like thermal oxidation, annealing, and irradiation can successfully mitigate inherent material defects [31]. Therefore, for further tuning of the device, the fabrication process requires modification [30].

Resistive switching refers to the physical phenomenon where a dielectric material changes its (two-terminal) resistance under the action of a strong extrinsic electric field or current [32], [33]. The change of resistance is non-volatile (i.e., the resulting resistance states can be maintained for a long time following the removal of the externally applied electric field [33]) and reversible. These phenomena occur in numerous insulating materials, including oxides, nitrides, chalcogenides, semiconductors, and organic materials. However, typical devices for resistive switching systems are capacitor-like devices, where an oxide thin film is sandwiched between top and bottom electrodes [33]. This capacitor-like configuration is convenient, as a large electric field (typically $\sim 10\%$ of the dielectric strength, which in many solids is of the order of 10-100 MV/m) can be applied easily, and is relatively easy to fabricate [33].

To put it succinctly, resistive switching devices (also termed memristive devices or memristors) are two-terminal non-linear dynamic electronic devices that can have broad applications in the fields of non-volatile memory, reconfigurable logic, analogue circuits, and neuromorphic computing [34]. A key characteristic of memristors is the pinched hysteresis loop they exhibit in the current-voltage plane. Practically, the device “remembers” its most recent resistance state even when power is removed, which is why it is referred to as a memristor, short for “memory resistor” [35]. This device is considered to be a two-terminal, one-port electric circuit element, originally envisioned, postulated, and conceptualised by Leon Chua, as stated by Potrebíć, Tošić, and Bielek [36].

More specifically, Chua [37] noted that there are six different well-known mathematical relations connecting pairs of the four fundamental circuit variables: electric current i , voltage v , charge q and magnetic flux Q . One of these relations (the charge is the time integral of the current) is determined from the definitions of two of the variables, and another (the flux is the time integral of the electromotive force, or voltage) is determined from Faraday's law of induction. Thus, there should be four basic circuit elements described by the remaining relations between the variables (Figure 2.11). The ‘missing’ element—the memristor, with memristance M —provides a functional relation between charge and flux [38],

$$\phi = \Phi(q). \quad (2.1)$$

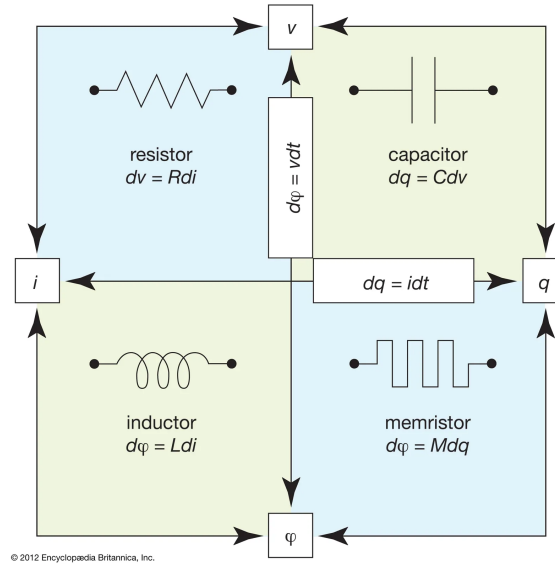


Figure 2.11: The four fundamental passive two-terminal circuit elements: resistor, capacitor, inductor and memristor [38]. Courtesy of Encyclopædia Britannica.

Conventionally, q is called the charge, and ϕ is called the flux of the memristor, but these quantities need not have any physical interpretations [36]. The function $\Phi(q)$ is a continuous and piecewise-differentiable function with bounded slopes. Differentiating equation (2.2) with respect to time t , the memristor port equation is obtained:

$$v = \frac{d\phi}{dt} = \frac{d\Phi(q)}{dq} \cdot \frac{dq}{dt} = M(q)i, \quad (2.2)$$

where the memristance at q , $M(q)$, is defined as:

$$M(q) = \frac{d\Phi(q)}{dq} \quad (2.3)$$

Just as memristor is an acronym for memory resistor, memristance stands for memory resistance. According to Potrebíć, Tošić, and Biolek [36], the instantaneous memristance is entirely dependent upon the cumulative history of the current traversing the device. Equations (2.3) and (2.4) define an ideal memristor [36]. The apparent absence of flux can be explained using Faraday's law of induction [39], rewriting the definition of a memristor as

$$M = \frac{d\Phi(q)}{dq} = \frac{vdt}{idt} = \frac{v}{i}. \quad (2.4)$$

This looks just like ordinary resistance (but the charge dependence ensures that it is really not), and hence, it works as an illustration that memristance in some cases degenerates to ordinary resistance. This happens, for example, if $M(q)$ is constant with time [39].

2.3.1 Switching behaviour

According to Chua [40], “Any two-terminal device which exhibits a pinched hysteresis loop in the v - i plane when driven by any bipolar periodic voltage or current waveform, for any initial conditions, is a memristor. The loop shrinks to a straight line whose slope depends on the excitation waveform, as the excitation frequency tends to infinity”. Therefore, memristors are uniquely identified by their “fingerprint” pinched hysteresis loop, a double-valued Lissajous pattern observed in the v - i plane, confined to the first and third quadrants [36], as observed in Figure 2.12.

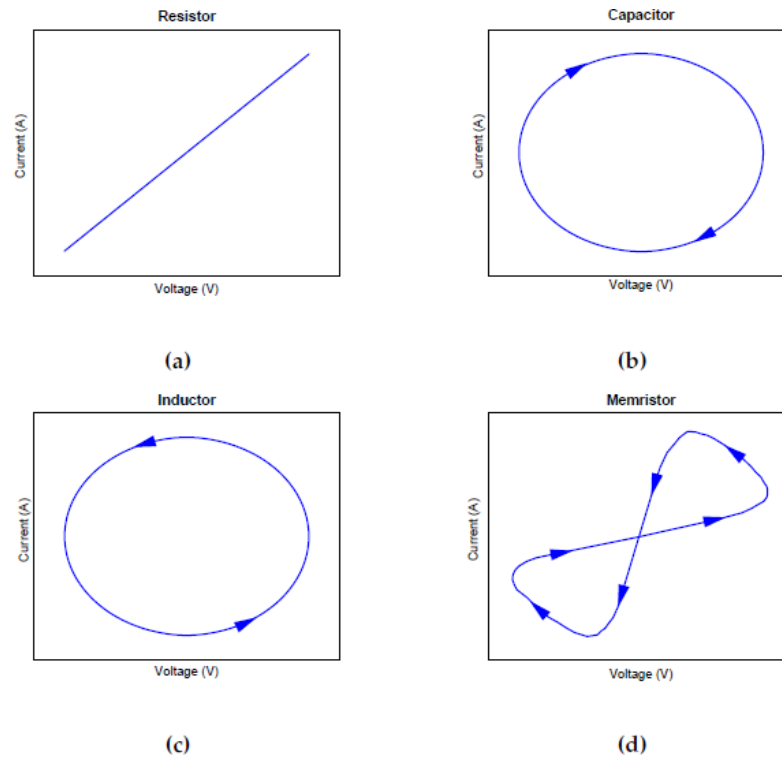


Figure 2.12: I-V relationships of the four fundamental circuit elements: (A) resistor, (B) capacitor, (C) inductor, and (D) memristor [41].

As reflected in Figure 2.13, a memristor can be in one of two states. The working mechanism of memristor relies on the transition between these two states, caused by the formation of conductive filament or the phase change of insulating materials [42], [43]. Conventionally, the transition from the Low Resistance State (LRS) to the High Resistance State (HRS) is denoted as a RESET, with the inverse transition from HRS to LRS being termed a SET [43]. During routine measurements, an artificial current limit, known as Current Compliance (CC), is commonly implemented to safeguard the device against damage from excessive current flow [44].

Two different switching modes, “unipolar” (or non-polar) and “bipolar”, are generally recognized for anionic and cationic memristor devices [30]. The schematics of I-V curve characteristic of unipolar and bipolar resistive switching are illustrated in Figure 2.13.

In an unipolar mode (Figure 2.13A), the change in the resistance state only depends on the magnitude of applied voltage and not the polarity. The SET process (towards ON state) is always

established at a higher voltage than that required for the RESET operation. The level of current reached at the RESET transition point is also greater than the compliance defined during the SET operation [45]. In a bipolar mode (Figure 2.13B), the use of opposite voltage polarities is a key requirement to switch the devices ON (SET) and OFF (RESET), respectively. Frequent asymmetry of the I-V curve characteristic is also observed with both switching modes and can be tailored through device fabrication or electrical forming [30], [45].

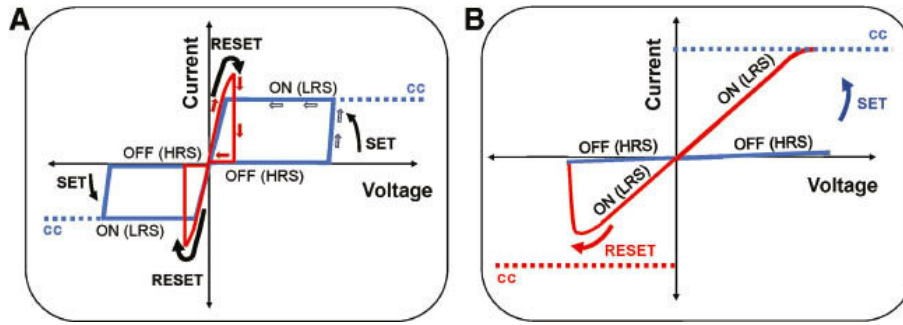


Figure 2.13: Schematic representation of memristor I-V curve switching behaviour. (A) Unipolar switching; (B) Bipolar switching. CC refers to the compliance current. [30]

2.4 Mathematical Modelling of Memristors

The theoretical groundwork for memristors, laid by Chua's device formulation in [37], sparked the development of a vast array of models, each striving to unravel the intricate mechanisms of memristor operation. This section outlines the mathematical models describing the behaviour of memristors. Models for both current-controlled and voltage-controlled devices will be considered. Beyond outlining these frameworks, the role of "window functions" is also explained.

2.4.1 Linear Ion Drift memristive device model (HP Model)

Nearly four decades after the memristor was theoretically postulated by Chua, it was first described as a physical system in 2008 by researchers at the Hewlett-Packard (HP) laboratory in California, USA [39]. The developed nano-sized memristor consisted of a thin-film titanium dioxide, TiO_2 , a layer that was "sandwiched" between two platinum electrodes and is shown in Figure 2.14. This memristor model is also very similar to the memristance that can be found in electrical measurements of the skin as seen in [39].

This device is illustrated in Figure 2.14, and this way of illustrating memristors, as a component separated into two parts, is very useful for understanding its basic principles. The memristor consists of one part that conducts current well (the doped part) and one part that is a much poorer electrical conductor (the undoped part) [39]. The total resistance—or strictly speaking, the memristance—of this two-component system is the sum of the doped and the undoped parts. What makes this system a memristor and not a resistor is the presence of a dynamic state variable defining the boundary between the two parts with high and low conductance. The state variable (w in

this particular case) describes how the memristance of the element evolves with time. The boundary between the two parts is dynamic and is moved back and forth by the passing charge carriers. For this particular HP memristor, the state variable w is proportional to the electric charge, q [39].

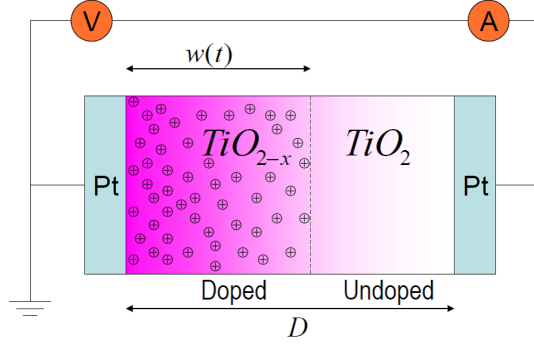


Figure 2.14: Cross-section of the first HP TiO₂-memristor consisting of a high conductive (doped) and a low conductive (undoped) part placed in between two platinum electrodes [39].

As postulated by Strukov, Snider, Stewart, *et al.* [38], the application of an external bias $v(t)$ across the device will move the boundary between the two regions by causing the charged dopants to drift. For the simplest case of ohmic electronic conduction and linear ionic drift in a uniform field with average ion mobility, μ_v , we obtain

$$v(t) = \left(R_{\text{ON}} \frac{w(t)}{D} + R_{\text{OFF}} \left(1 - \frac{w(t)}{D} \right) \right) i(t) \quad (2.5)$$

$$\frac{dw(t)}{dt} = \mu_v \cdot \frac{R_{\text{ON}}}{D} \cdot i(t) \quad (2.6)$$

which yields the following formula for $w(t)$:

$$\frac{w(t)}{D} = \mu_v \cdot \frac{R_{\text{ON}}}{D^2} \cdot q(t) \quad (2.7)$$

This model is known as the linear drift model because the velocity of the width (w) is linearly proportional to the current. In other words, the change in the memristor's state will be the same regardless of the voltage waveform, as long as the net flux across the memristor remains constant. Additionally, when voltage is applied, the state of the memristor will return to its initial position if the net induced flux is zero [46]. Moreover, inserting Equation (2.7) into (2.5), the memristance of the system is obtained, which for $R_{\text{ON}} \ll R_{\text{OFF}}$ simplifies to:

$$M(q) = R_{\text{OFF}} \left(1 - \frac{\mu_v R_{\text{ON}}}{D^2} q(t) \right). \quad (2.8)$$

2.4.2 Non-linear model

As summed up in [46], it is known that the memristor also exhibits non-linear behaviour due to the fact that the linear model does not take into account the boundary effect. The boundary

between the doped and undoped regions moves with a drift velocity of μ_D which decreases as it approaches the edges, $w \sim 0$ and $w \sim D$. Furthermore, the linear model does not consider the strong non-linearity of the electric field inside the memristor.

To address these limitations, Joglekar and Wolf [47] developed a modified mathematical model, commonly referred to as the *non-linear drift model*. This model introduces a window function to better describe the dynamics of the internal state variable. More window functions are discussed in Section 2.4.8.

In consonance with Prodromakis, Peh, Papavassiliou, *et al.* [48], a suitable window function for modelling non-linear behaviour must satisfy the following conditions:

1. It must account for the top and bottom electrode boundary conditions of the memristor.
2. It should be capable of imposing non-linear drift throughout the whole active core of the device.
3. It should ensure a smooth transition between linear and non-linear drift regimes.
4. The function must be scalable.
5. It should include a control parameter to adjust the model as desired.

Therefore, Equation (2.7) is modified as follows:

$$\frac{w(t)}{D} = \mu_v \cdot \frac{R_{ON}}{D^2} \cdot q(t) \cdot f(x), \quad (2.9)$$

where $x = \frac{w(t)}{D}$, and $f(x)$ is called the *window function*. This function constrains the state variable x to remain bounded between 0 and 1, preventing unphysical behaviour and enhancing model realism.

2.4.3 Simmons Tunnel Barrier Model

Linear and non-linear ion drift models are based on representing the two regions of oxide and doped oxide as two resistors in series. This model assumes non-linear and asymmetric switching behaviour due to an exponential dependence of the movement of the ionised dopants, namely, changes in the state variable.

In this model, rather than two resistors in series as in the linear drift model, there is a resistor in series with an electron tunnel barrier, as shown in Figure 2.15. The state variable is the Simmons tunnel barrier width [49]. In this case, the derivative of x can be interpreted as the oxygen vacancy drift velocity, and is

$$\frac{dx(t)}{dt} = \begin{cases} c_{off} \sinh\left(\frac{i}{i_{off}}\right) \exp\left[-\exp\left(\frac{x-a_{off}}{w_c} - \frac{|i|}{b}\right) - \frac{x}{w_c}\right], & i > 0 \\ c_{on} \sinh\left(\frac{i}{i_{on}}\right) \exp\left[-\exp\left(-\frac{x-a_{on}}{w_c} - \frac{|i|}{b}\right) - \frac{x}{w_c}\right], & i < 0 \end{cases} \quad (2.10)$$

where c_{off} , c_{on} , i_{off} , i_{on} , a_{off} , a_{on} , w_c , and b are fitting parameters.

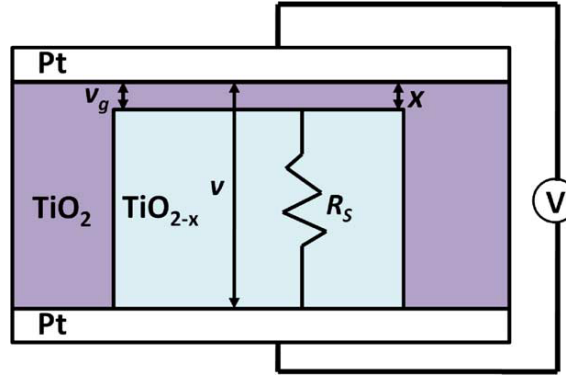


Figure 2.15: Simmons tunnel barrier physical model. x is the state variable and the width of the oxide region, V corresponds to the applied voltage on the device, v_g is the voltage in the undoped region, and v is the device's internal voltage [49].

The I–V characteristics can be defined by [46]:

$$i(t) = \frac{j_0 A}{\Delta w^2} [\phi_1 \exp(-B(\phi)^{0.5}) - (\phi_1 + e|v_g|) \exp(-B(\phi_1 + e|v_g|)^{0.5})] \quad (2.11)$$

where A is the cross-sectional area of the barrier and j_0 , Δw , B and v_g are all defined as follows [46]:

$$j_0 = \frac{e}{2\pi h} \quad (2.12)$$

$$B = \frac{4\pi\Delta w(2m)^{0.5}}{h} \quad (2.13)$$

$$\phi_1 = \Phi_0 - e|v_g| \left(\frac{w_1 + w_2}{w} - \left(\frac{1.15\lambda w}{\Delta w} \ln \left(\frac{w_2(w - w_1)}{w_1(w - w_2)} \right) \right) \right) \quad (2.14)$$

Moreover,

$$w_1 = \frac{1.2\lambda w}{\phi_0} \text{ and } \Delta w = w_2 - w_1 \quad (2.15)$$

$$w_2 = w_1 + w \left(1 - \frac{9.2\lambda}{3\phi_0 + 4\lambda - 2e|v_g|} \right) \quad (2.16)$$

$$\lambda = \frac{e^2 \ln(2)}{8\pi k w}, \quad (2.17)$$

where k is the dielectric constant and $\epsilon_0 = 8.85 \times 10^{-12}$ F/m is the vacuum permittivity. The electron charge is $e = -1.602 \times 10^{-19}$ C, its mass is $m = 9.31 \times 10^{-31}$ kg, and Planck's constant is $h = 6.626 \times 10^{-34}$ J · s.

Finally,

$$v(g) = v - v(R) = v - i(t)R(s), \quad (2.18)$$

where v_g is the memristor's voltage, $i(t)$ its current, R_s is the electron resistance, v_R is the voltage across the metallic channel series resistance, ϕ_0 is the effective barrier height, w the barrier thickness (in (2.10) and Figure 2.15, denoted as x), or state variable control.

The model does not require a window function [46]. However, some of its limitations are that it is complicated in its mathematical rigour and expression; it does not provide an explicit relationship between voltage and current; and may not be applicable to all types of memristors [46].

2.4.4 ThrEshold Adaptive Memristor (TEAM) Model

The Simmons tunnel barrier model is, in accordance with Kvatinsky, Friedman, Kolodny, *et al.* [49], the most accurate physical model of a TiO_2 memristive device. Despite this recognition, this model is quite complex, lacking an explicit relationship between current and voltage, and it is not general in nature (i.e., the model applies only to a specific type of memristive device) [49]. A complex SPICE model of the Simmons tunnel barrier model is presented in [50]. This model is also computationally inefficient.

Given these factors, a simpler model is sought, described by the authors as the TEAM model, though its accuracy must remain suitable for the application. This simplified model captures the same physical behavior, but it is achieved over simpler mathematical functions. Therefore, no change in the state variable is assumed below a certain threshold, and a polynomial dependence rather than an exponential dependence is used. These choices are applied to bolster analytical simplicity and computational efficiency [49]. According to Kvatinsky, Friedman, Kolodny, *et al.* [49], this model can be explained by the following equations:

$$\frac{dx(t)}{dt} = \begin{cases} k_{off} \left(\frac{i(t)}{i_{off}} - 1 \right)^{\alpha_{off}} f_{off}(x), & \text{for } 0 < i_{off} < i \\ 0, & \text{for } i_{on} < i < i_{off} \\ k_{on} \left(\frac{i(t)}{i_{on}} - 1 \right)^{\alpha_{on}} f_{on}(x), & \text{for } i < i_{on} < 0, \end{cases} \quad (2.19)$$

where $k_{off} > 0$, $k_{on} < 0$, and K_{off} , K_{on} , α_{off} , α_{on} are constants, i_{off} and i_{on} are current thresholds; x is the internal state variable; and f_{on} and f_{off} are window functions that constrain x between the bounds x_{on} and x_{off} [49].

As a result, if the memristance changes linearly with the state variable x , then:

$$v(t) = \left[R_{ON} + \frac{R_{OFF} - R_{ON}}{x_{off} - x_{on}} \right] \cdot i(t). \quad (2.20)$$

If any change in the resistance occurs, it becomes exponentially dependent on the state variable [49]. Under this assumption,

$$v(t) = R_{ON} \cdot e^{\left(\left(\frac{\lambda}{x_{off}} \right) (x - x_{on}) \right)}, \quad (2.21)$$

where λ is the fitting parameter and R_{ON} and R_{OFF} correspond to the effective resistances at the bounds, similar to the notation in the linear ion drift model [49], and satisfy

$$\frac{R_{OFF}}{R_{ON}} = e^\lambda. \quad (2.22)$$

The TEAM model can be applied to any memristor model [49]. However, it operates under certain assumptions, which are as follows:

1. The state variable is fixed below a certain threshold value.
2. A polynomial rather than exponential dependency exists between the current of the memristor and the internal state drift derivative.

2.4.5 VTEAM–Voltage ThrEshold Adaptive Memristor Model

In 2015, a Voltage ThrEshold Adaptive Memristor Model (VTEAM) was proposed by Kvatinsky, Ramadan, Friedman, *et al.* [51], which exhibits a voltage threshold, contrary to a current threshold. Since the resistance of a memristor does not change for currents below a certain threshold current, a memristor with a threshold voltage is more appropriate than a threshold current for certain logic and memory applications.

The (V)TEAM falls into the category of empirical models, which are fitted to real memristive devices by tuning a set of parameters. Put differently, the device's specific "fabrication details" are encoded in its experimental data, which serves as the direct basis for calibrating the parameters of the universal (V)TEAM model [52].

The model's current-voltage relationship can be chosen arbitrarily to best accommodate the behaviour of a specific memristive device [52]. In [49], [51], two simple models are suggested, which consider either a linear or exponential dependence of the memristance R_M on the state variable w :

$$R_M(w) = R_{on} + (R_{off} - R_{on}) \cdot \frac{w - w_{on}}{w_{off} - w_{on}} \quad (2.23)$$

or

$$R_M(w) = R_{on} \cdot \left(\frac{R_{off}}{R_{on}} \right)^{\frac{w - w_{on}}{w_{off} - w_{on}}}, \quad (2.24)$$

where R_{on} , R_{off} , and w_{on} , w_{off} are the limiting values of the memristance and the state variable w in the ON and OFF states, respectively.

Crucial to the (V)TEAM model are the state equations, which maintain the same form for both TEAM and VTEAM variants. Given below are the equations for the VTEAM:

$$\frac{dw}{dt} = \begin{cases} k_{\text{off}} \left(\frac{v}{v_{\text{off}}} - 1 \right)^{\alpha_{\text{off}}} f_{\text{off}}(w), & v > v_{\text{off}} \quad (\text{OFF}) \\ 0, & v_{\text{on}} < v < v_{\text{off}} \quad (\text{subTHR}) \\ k_{\text{on}} \left(\frac{v}{v_{\text{on}}} - 1 \right)^{\alpha_{\text{on}}} f_{\text{on}}(w), & v < v_{\text{on}} < 0 \quad (\text{ON}). \end{cases} \quad (2.25)$$

Here, v is the voltage across the device, v_{on} , v_{off} are the threshold voltages, k_{on} , k_{off} , α_{on} , α_{off} are the fitting parameters, and $f_{\text{on}}(w)$, $f_{\text{off}}(w)$ are the window functions whose role is to preserve the state variable within the physically realistic limits $w \in (w_{\text{on}}, w_{\text{off}})$. It is indicated on the right side of Equation (2.25) that the state equation has different forms for the OFF, ON, and subTHReshold regime of operation [51].

2.4.6 Vourkas Model

Vourkas, Batsos, and Sirakoulis [53] introduced a deeper understanding of a SPICE implementation of a threshold-based memristive device model. This model's programmable thresholds allow for distinct threshold values contingent on the polarity of the applied voltage. Such a feature is critical for accurately representing experimental characterisation data, given the empirical verification that both state variable motion and threshold voltages exhibit asymmetry under forward and reverse biasing [53]. The model's general definition is given by the following formulae:

$$I(t) = G(L, t) V_M(t) \quad (2.26)$$

$$\dot{L} = f(V_M, t) \quad (2.27)$$

in which L serves as both the tunnel barrier width and system's single state variable, indicating the internal memristor state. The device's conductance is given by G , while I and V_M represent the current and applied voltage, respectively [53]. For a specific, restricted range of the state variable L , the device's tunneling resistance (memristance), R_t , is determined by the following equation [53]:

$$R_t(L, V_M, t) = f_0 \cdot e^{2L(V_M, t)} \quad (2.28)$$

where f_0 is a model fitting parameter. The device's resistance, as a function of L , exhibits exponential behavior. Furthermore, the response of the tunnel barrier width to applied voltage is qualitatively described by the following heuristic equation [53]:

$$L(V_M, t) = L_0 \cdot \left(1 - \frac{m}{r(V_M, t)} \right), \quad (2.29)$$

where L_0 denotes the maximum achievable value for $L(V_M, t)$, and m functions as a fitting parameter that delineates the boundaries of the barrier width. Positioning tunneling as the predominant physical mechanism, Equation (2.29) introduces the initial and instantaneous positions of the tunneling barrier, which are inherently bounded by two defined values [53].

Furthermore, this model reveals that ON switching can be either faster or slower than OFF switching in many memristive devices. This model assumes that the switching rate of L is slow below a threshold voltage (V_{SET} or V_{RESET}) and fast above it. This threshold represents the minimum energy required to induce a physical structural change in the device. This assumption is encapsulated in the voltage-dependent function $r(V_M, t)$, whose time derivative, provided by the following expression, varies in speed based on the applied voltage [53]:

$$\frac{dr(V_M, t)}{dt} = \begin{cases} a \cdot (V_M + V_{th}) / (c + |V_M + V_{th}|), & V_M \in [-V_0, -V_{th}] \\ b \cdot V_M, & V_M \in [-V_{th}, +V_{th}] \\ a \cdot (V_M - V_{th}) / (c + |V_M - V_{th}|), & V_M \in [+V_{th}, +V_0] \end{cases} \quad (2.30)$$

The model allows for programmable thresholds by tuning the shaping parameters a , b , and c of $r(V_M, t)$ (Equation (2.30)). This function utilizes sigmoid behavior for voltages above thresholds and a linear relation below, with a , b , and c (where $a \gg b$ and $0 < c < 1$) governing the memristance change rate. A hard switching characteristic is imposed if $b = 0$. As the defining parameter for device dynamics and state, $r(V_M, t)$ is continuously monitored and constrained within r_{min} to r_{max} , consequently setting the device memristance to R_{ON} or R_{OFF} . If $r < r_{min}$, it is set to r_{min} ; if $r > r_{max}$, it is set to r_{max} . Consequently, the device memristance is correspondingly set to R_{ON} or R_{OFF} [53].

2.4.7 Compact (Bipolar/Unipolar) Model

García-Redondo, Gowers, Crespo-Yepes, *et al.* [54] present a novel solution based on the independent modelling of the device conduction mechanisms and device state. This model relies completely on physical magnitudes and their inter-relations, defining both the electrical and resistive switching behaviour. Although the model accommodates voltage and current thresholds, device switching within the state module is fundamentally built upon electrical charge, flux, or energy thresholds. This comprehensive approach applies equally to both bipolar and unipolar devices, significantly broadening the model's descriptive power. Additionally, the integrated conduction module provides an accurate fit for the physical component's conduction mechanisms [54]. An important feature of the model is that it is fully compatible with SPICE simulators— the presented model does not require implementation in Verilog-A or CMI to accurately match physical components [54].

The proposed model, illustrated in Figure 2.16, comprises two distinct subcomponents to accurately represent device behaviour. The Conduction Module, connected via the ports *Plus* and *Minus*, models the memristor's dynamic resistance. In addition, the State Module handles the device's internal state [54].

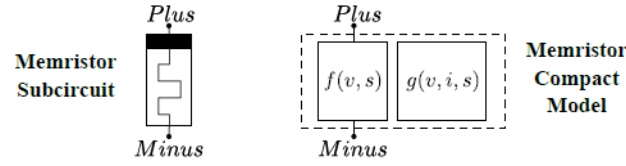


Figure 2.16: Proposed unipolar memristor model in [54].

The component's behaviour is characterised by its transient signal set, which includes the input voltage $v(t)$, the current $i(t)$ flowing through the device, and the device state vector $s(t)$. This vector encapsulates all relevant information, such as cycle count, switching thresholds, energy and resistance state. For simplicity in this paper, the time dependence in the electrical and state equations will be implicit; for instance, $v(t)$ will be referred to as v [54].

The relationships between these submodules can be expressed using the generalized system of equations:

$$\begin{aligned} i &= f(v, s) \\ \dot{s} &= g(v, i, s) \end{aligned} \tag{2.31}$$

This system of equations effectively describes the behaviour of most devices [54], with both physical and behavioural models specifying the functions f and g to define the model's operation. Another important model feature is its pristine (conductive filament pre-forming) state—the initial High Resistive State (HRS) before any electroforming—awareness and modelling, differentiating it from other models and enriching its capabilities [54].

2.4.8 Window Functions

At nanoscale dimensions, by just applying a few volts, a strong electric field is formed in the device, which causes a high non-linearity in the ionic drift-diffusion [55]. However, the previous formulas do not take in consideration this effect. To solve this problem, various attempts have been carried out to add non-linear behaviour to the state equation. To overcome this limitation, the first proposal considered multiplying the second term of the state equation with a *window function*, $f(x)$, as seen in (2.9).

Biolek Window Function

Biolek, Biolková, and Biolek [55] propose a window function that enables the memristor to revert from its terminal state. This function is designed to reflect the physical behaviour of the device, where a reversed bias should move the internal state variable away from either boundary once it is reached. Furthermore, the dynamics of the boundaries are asymmetric, depending on the direction of the voltage bias [55].

This window function is not only dependent on the internal state variable $x = \frac{w(t)}{D}$, but also on the direction of current flow through the memristor. To model this, a current-dependent step function, $\text{stp}(-i)$, is used as part of the formulation of the window function $f(x)$, defined as [55]:

$$f(x) = 1 - (x - \text{stp}(-i))^{2p} \quad (2.32)$$

where the step function is defined as:

$$\text{stp}(-i) = \begin{cases} 1, & \text{if } i \geq 0 \\ 0, & \text{if } i < 0 \end{cases} \quad (2.33)$$

This formulation allows the memristor model to remain responsive even at boundary limits, with asymmetric dynamics that better capture the device's physical switching characteristics [55].

Joglekar Window Function

Joglekar and Wolf [47] propose a window function that provides more accurate modelling of the internal state variable dynamics in memristive systems, particularly near the boundaries [56].

$$f_p(x) = 1 - (2x - 1)^{2p} \quad (2.34)$$

where $p \in \mathbb{Z}^+$ [47]. This window function effectively satisfies the memristor's boundary conditions and non-linear drift behaviour when $p \geq 1$.

Strukov Window Function

Strukov, Snider, Stewart, *et al.* [38] proposed a window function, $f(x)$, that should reach its maximum in the center of the device, $x = 0.5$, and decrease towards boundaries in which it will reach zero speed at the terminal states $x = 0$ or $x = 1$.

$$f(x) = \frac{w(D - w)}{D^2} \quad (2.35)$$

$$f(x) = x - x^2 \quad (2.36)$$

Prodromakis Window Function

In addition to this model, various other window function formulations have been explored in the literature. For example:

$$f(x) = 1 - (x - \text{sgn}(-i))^{2p}, \quad (2.37)$$

as proposed in [55] and

$$f(x) = 1 - ((x - 0.5)^2 + 0.75)^q, \quad (2.38)$$

as discussed in [48], where $\text{sgn}(\cdot)$ denotes the sign function, $p \in \mathbb{Z}^+$, and $q \in \mathbb{R}^+$.

2.5 SPICE Macromodels

Alongside its theoretical mathematical models, memristor, and indeed all device modelling, eventually requires testing and implementation. This section focuses on the practical implementation of previously discussed memristor models within SPICE tools, more specifically LTspice. Initially, existing macromodels for various memristor types are introduced. These models are then validated in SPICE by simulating a single memristor device. Following the individual simulations, the performance and characteristics of the simulation and the laboratory validations of the literature are compared. Based on this analysis, a representative memristor model is selected to be used in the development of more complex circuits and memristive logic gates, according to which one is most similar to the real device.

2.5.1 LTspice

Many software tools are being used for designing memristor circuits such as LTspice, PSpice, NGSpice, Cadence Virtuoso, and MATLAB/Simulink. Among them, LTspice is a very popular open-source tool for linear and non-linear circuit simulations. This tool is a free circuit simulation software developed originally by Linear Technology and now produced by Analog Devices. With LTspice, users can design and simulate memristor circuits using a graphical interface. The software allows users to simulate the behaviour of circuits under different conditions and different types of simulations. For simplicity, replicability and reproducibility, available resources, and simulation accuracy, LTspice is used to simulate all of this dissertation's designs.

Before developing the necessary control circuit and simulating it, one essential goal was to test and compare different SPICE models described as follows. Although Verilog-A is more flexible regarding the use of user-defined functions or variable data types (such as arrays), and some circuit simulators, such as *Cadence Spectre Circuit Simulator* allow Verilog-A code execution, widely used SPICE simulators like *LTspice* do not allow Verilog-A co-simulation, accepting SPICE-like code only. Consequently, the research community may benefit from SPICE compact models [54].

In this manner, this section presents the testing procedure conducted in LTspice¹ to examine the behaviour of different memristor models. The goal is to determine whether these models yield valid values for the resulting memristance. Each model has a specific set of parameters required for the simulations to function correctly. To avoid any simulation issues, the parameters chosen align

¹Simulations were run on LTspice XVII, using an Aspire A515-55G, Intel(R) Core(TM) i7-1065G7 CPU @ 1.30GHz, 8 GB RAM, Windows 11 Home.

with those used in the original papers where the simulations were first conducted. Furthermore, subsection 2.5.2 condenses the advantages and disadvantages of each model.

2.5.2 SPICE Models Comparison

The scripts used for testing the memristor models are displayed in Appendix A. The implemented testing methodology was to save the `.subckt` (sub-circuit model) files in LTspice's integrated "sub" directory (already on the platform's file structure). After this, creating a symbol out of these files, so that the model can be implemented onto the schematic. Finally, the testing circuit was created, as shown in Figure 2.17, and used throughout different model simulations (alternating between the chosen memristor component, and, if needed, modifying the voltage source to accommodate the device's behaviour). The results show the models' behaviour, most of them being similar to real-world devices.

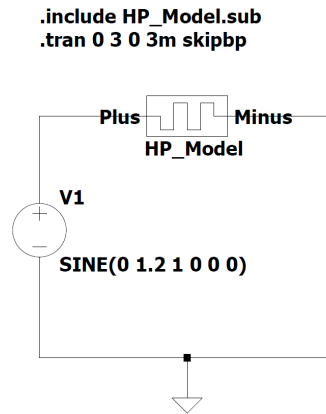


Figure 2.17: Memristor testing circuit designed on LTspice.

In conducting a review of the pertinent SPICE models for this master's thesis, it is crucial to articulate their respective attributes and drawbacks. To this end, Table 2.2 provides a comparative assessment of the explored models. The only model that was not tested was VTEAM, as LTspice cannot support Verilog-A code. A subcircuit implementation of the VTEAM model in SPICE could be performed, however, this was not pursued in this work. This analysis centers on aspects such as their control mechanisms, descriptive generality of real-world phenomena, accuracy in replicating experimental device characteristics, the incorporation of voltage or current thresholds, their applicability to both bipolar and unipolar devices, and its pristine state awareness. Additional data, from the tables in [49] and in [54], helped picture Table 2.2. Depending on a given application or use for the memristor, one can be chosen accordingly.

It is apparent within the scope of this thesis that the TEAM and Compact models represent the foremost memristor models for accurately simulating current-controlled and voltage-controlled devices. Nevertheless, the Compact model demonstrates a superior advantage, being the most complete option for the unipolar devices utilized in the scope of this work. Moreover, these models offer the highest level of accuracy and flexibility in simulating a wide range of memristive behaviours, making them ideal candidates for future research and development in the field.

Table 2.2: Comparison of Different Memristive Device Models.

Model	Linear ion drift [38]	Nonlinear ion drift [47]	Simmons tunneling barrier [49], [50]	Vourkas [53]	TEAM [49]	Compact Model [54]
State variable	$0 \leq w \leq D$ (Doped width)	$0 \leq w \leq 1$ (Normalized)	$a_{\text{off}} \leq x \leq a_{\text{on}}$ (Undoped width)	$L = f(V_M, t)$ (Tunnel barrier width)	$x_{\text{on}} \leq x \leq x_{\text{off}}$ (Undoped width)	$s = g(v, i, s)$ (State vector)
Control mechanism	Current	Voltage	Current	Voltage	Current	Voltage/current + charge/flux/energy
I-V relationship	Explicit	I-V explicit Memristance ambiguous	Ambiguous	Explicit	Explicit	Explicit
Matches memristive system	Yes	No	No	Yes	Yes	Yes
Pristine State Aware	No	No	No	No	No	Yes
Practical accuracy	Low	Low	High	High	High	High
Threshold exists	No	No	Practically	Yes	Yes	Yes
Bipolar/Unipolar	Bipolar	Bipolar	Bipolar	Bipolar	Bipolar	Both

2.6 Final Comments

A foundational understanding of Reconfigurable Intelligent Surfaces (RISs) and the diverse technologies enabling their functionality has been provided in this chapter, thereby establishing the context for the core contributions of this thesis.

The critical role of RISs in advancing future communication systems, particularly within the context of 6G networks, was initially established. The principles of antenna array technology and metasurfaces were then outlined, with their capacity to reshape electromagnetic wave propagation through dynamic phase manipulation at a granular level being illustrated. Solutions to challenges posed by higher frequency bands, such as the Terahertz spectrum, were also offered.

Following this, a detailed review of RIS components and reconfigurability techniques was presented, during which various approaches, ranging from mechanical and optical methods to electrical solutions employing PIN diodes, varactors, and MEMS switches, were highlighted. The inherent limitations of conventional active components, notably their power consumption and discrete control, were emphasized by this comparative analysis, revealing significant scalability and energy efficiency challenges for large-scale RIS deployments.

Crucially, the compelling advantages of memristors as a superior reconfigurable element for RIS were emphasized. Their non-volatility, ultra-low power consumption for state retention and nanoscale footprint position them as a transformative solution capable of overcoming the inherent drawbacks of existing technologies. Through their ability to enable highly dense, energy-efficient, and continuously tunable metasurface elements, the full potential of RIS for advanced beamforming, pervasive intelligent environments, and sustainable 6G communication can be greatly enhanced.

In summary, the evolution of RIS technology has been illuminated, the key challenges in its practical implementation identified, and the benefits that memristors offer in addressing these hindrances, firmly established throughout this review. This background constitutes the essential

understructure upon which the novel memristor-based RIS control approach will be presented and investigated in the subsequent chapters of this dissertation.

Chapter 3

Design and Implementation of a Switching Circuit for Memristor Controlling

The preceding chapter established the necessary foundation work and study of memristors and their models. The present chapter is centred on the practical implementation of the electronic circuit that controls memristors. In addition, following this logic, this chapter also addresses the electrical characterisation of memristors, which is crucial for understanding their behaviour and performance in various applications. The characterisation process involves measuring the current-voltage (I-V) characteristics of memristors, and their memristance, under different conditions, such as varying voltage or current levels.

3.1 Proposed Approach

The proposed approach for this work involves the integration of memristors into the control circuitry of RIS unit cells. This integration aims to capitalise on the unique properties of memristors, such as their non-volatility and low power consumption, to enhance the performance and efficiency of the RIS system. For the RIS to work properly, along with the unit cell layout (building block of the RIS), and testing of the integrated switches and beamforming, it needs integration with the necessary control circuitry [57].

The proposed design includes analogue control mechanisms to ensure precise switching and reliable performance. The concept for this design is presented in Figure 3.1, which illustrates the overall architecture of the control circuit. For the scope of this work, as denoted by CENIMATli3N Lab (NOVA), the MoS₂ unipolar memristor devices are controlled as follows:

- SET (to LRS, ON) → Current-controlled.
- RESET (to HRS, OFF) → Voltage-controlled.

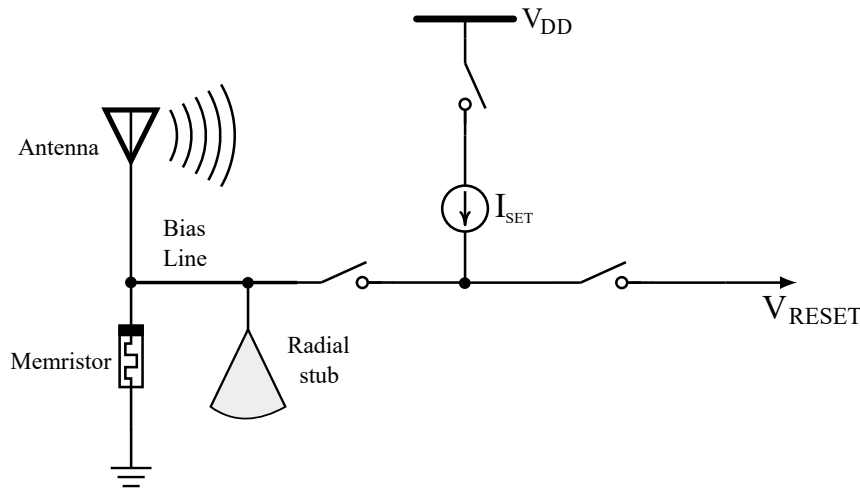


Figure 3.1: Schematic of the RIS control circuit.

In light of this, an important aspect of this work is the electrical characterisation of memristors, which is essential for understanding their behaviour and performance, namely the parameters that must be taken into account when designing the control electronics. The R_{ON} and R_{OFF} resistances, as well as the switching thresholds, are critical for the design choices.

The next section demonstrates the electrical characterisation of memristors. The subsequent section establishes and describes the building blocks (to perform either SET or RESET) for the circuit layout.

3.2 Electrical Characterisation of Memristors Setup

The electrical characterisation setup used in this work is based on the one employed at the INESC TEC OET Lab, as shown in Figure 3.2. The setup consists of a computer running Windows, which interfaces with a Keysight B2902A Precision Source/Measure Unit (SMU) via a USA-A-USB-B cable. The SMU is connected to probes in a probe station using banana connectors, allowing for precise measurements of the memristor devices.

USA-A-USB-B Cable

The USA-A-USB-B cable allows for communication between the computer and the SMU. As seen in Figure 3.2, the cable connects the computer's USB-A port to the SMU's USB-B port, facilitating the transfer of data and commands between devices.

Keysight B2902A Precision Source/Measure Unit

The Keysight B2902A Precision Source/Measure Unit (SMU) is a versatile instrument used for sourcing and measuring electrical signals with high precision. It is capable of sourcing voltage or current and measuring the resulting current or voltage, respectively. The B2902A SMU is equipped with a graphical user interface (GUI) that allows users to configure the measurement

parameters, such as voltage or current levels, and to view the results in real-time. The SMU can also be controlled remotely via a computer, enabling automated characterisation of memristor devices.

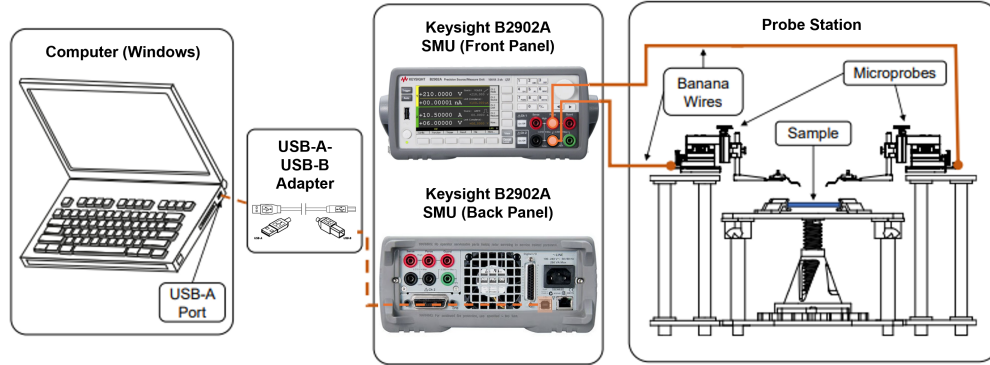


Figure 3.2: This diagram represents the memristor characterisation setup employed at INESC TEC OET Lab. It starts with a computer operating on the Windows platform, which interfaces with a Keysight B2902A SMU via a USA-A-USB-B cable. The SMU then communicates with the probes present in the probe station using banana jacks. The SMU also interfaces back with the computer, completing the setup. Adapted from [41].

The B2900A SMUs can source and measure voltages of ± 210 V and currents of ± 3 A (DC) or ± 10.5 A (pulsed). The B2902A possesses 100 fA and 100 nV measurement resolution and 1 pA and 1 μ V sourcing resolution. It also has 10 fA and 100 nV of resolution for both measurement and sourcing while also integrating four-quadrant sourcing and measuring capabilities, easily and accurately measure current and voltage using a single instrument without the need to manually change any connections.

With broad applicability in both research and industrial sectors, this instrument serves diverse functions. Key applications include the testing and characterisation of semiconductors and circuit boards, verification of electronic component integrity, and comprehensive material and device characterisation. The specifications for the Keysight B2902A SMU are listed in Table C.3.

Probe Station

The electrical characterisation of the memristive devices was performed on the SemiProbe Lab Assistant manual probe station, depicted in Figure 3.3. The Lab Assistant probe stations provide simplicity, ease of operation, portability, affordability, and modularity. Lab Assistant probe stations can be configured for DC or HF/Microwave testing configurations.

The used microscope is SMZ-171, in Figure 3.4, a flexible stereo microscope for advanced research work and, for instance, in industrial quality control. Figure 3.5 depicts the OET laboratory setup used for the electrical characterisation of the memristors *in situ*, which includes the probe station, the microscope, and the SMU (using the same logic from the diagram in Figure 3.2).

In this setup, particular attention was given to ensuring measurement accuracy and repeatability. The probe station allowed for precise positioning of the probes on the memristive devices,

while the stereo microscope facilitated accurate alignment and inspection of the contact points. To minimize parasitic effects and noise, shielded connections and careful grounding were employed throughout the setup.



Figure 3.3: SemiProbe Lab Assistant manual wafer probe station.



Figure 3.4: Motic SMZ-171 Microscope.

Furthermore, the SMU enabled both voltage and current-controlled experiments, making it possible to capture the dynamic switching characteristics of the memristors under different operating conditions. This combination of tools and factors ensured a comprehensive characterisation environment for extracting reliable electrical parameters of the devices.

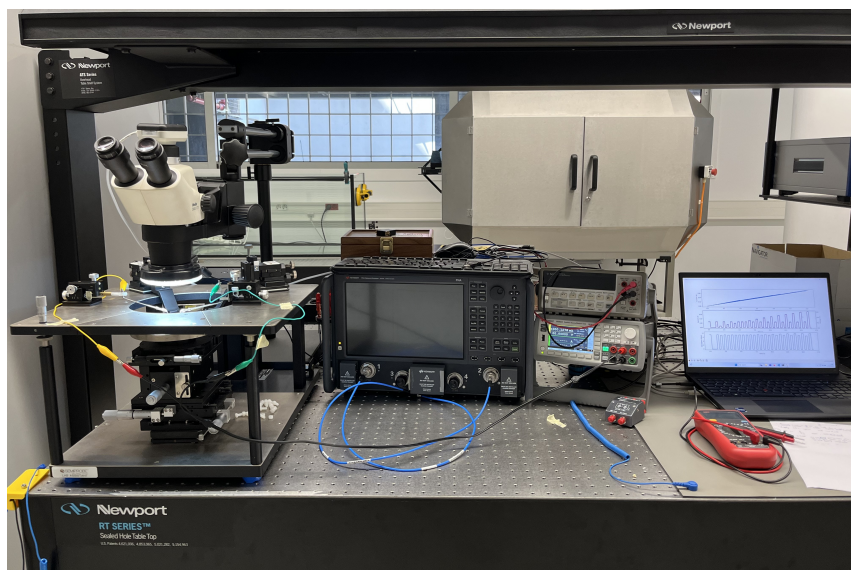


Figure 3.5: Laboratory setup used for the electrical characterisation of the memristors.

3.3 Type of Measurements

There are two main measurement/writing modes for characterising memristors: Pulsed and Sweep. Here, measurements can be understood as measuring and also applying to the memristor a given voltage or current value. Since an SMU is used, sourcing and measuring can be performed simultaneously. This dissertation focuses on pulsed measurements, due to the observed memristors' behaviour and also through the recommendations given by the CENIMATli3N lab, where the devices were fabricated, even though sweep measurements are frequently used in memristor characterisation and are available in the characterisation software. Here, sweeping procedures were only used if necessary for reading measurements, for instance, to confirm the device's state.

- **Pulsed Measurement and Writing:** In a pulsed measurement mode, voltage or current is delivered in distinct pulse forms. This method employs two types of pulses: one for SET and one for RESET. The purpose of applying the SET pulse train is to switch the memristor to a low resistance state (LRS), while the RESET pulse train aims to revert it to a high resistance state (HRS). Then, the resistance can be measured to check if the process was successful. The reading procedure can be obtained at any given moment, but it is important to keep track of the device's behaviour.
- **Sweep Measurements:** In a sweep measurement mode, a continuous linear potential of either voltage or current is implemented on the device. This potential increases linearly from 0 to its peak value of V/I_{max} , before descending back to 0. Each ladder step has an amplitude of V/I_{step} and persists for a duration of t_{step} . The resistance is calculated at specific moments, denoted by the blue markers, using the same voltage value as the write sweep [41].

Both types of measurements, pulsed and sweep, are essential for characterising the electrical properties of electronic devices and offer distinct benefits. Pulsed measurements are considered better because they lead to reduced power consumption, improved thermal stability, and, potentially, a longer device lifespan. This method is especially useful for analysing transient behaviours and allows flexibility in adjusting pulse parameters to meet specific characterisation requirements. Moreover, the consistent measurement conditions validate that the resistance readings are effective for comparable evaluation. In contrast, sweep measurements enable continuous and comprehensive characterisation across a range of voltages or currents, often leading to faster measurements and smoother, more intuitive data. This continuous variation is essential for analysing characteristics like hysteresis and is supported by the ease of implementation and the extensive resources and tools available for these measurement types.

In effect, the choice between these methods depends on the specific requirements of the characterisation task at hand. However, for this particular project, the tested and suggested methods proved that using pulsing for both SET and RESET states was more effective and recommended. Depending on which state the memristor may be in, the given voltage or current may need to be adjusted, mitigating potential damage to the device.

3.4 Characterisation Software

The software used in this procedure is a set of Python scripts that automates the process of applying either a current sweep, voltage sweep or pulse train of voltage and measuring the resulting voltage across the memristor device and vice versa. The scripts implementing the SMU's source and measurements are reported in Appendix B. These scripts provide automation for the source and measurement settings. The Python scripts are designed to control a Keysight B2902 Source/Measure Unit (SMU) (or a similar Keysight instrument that uses the SCPI command set over VISA) to perform electrical measurements on a device, specifically focusing on applying sweeps or pulses and measuring the results. It then processes, saves, and plots the collected data.

The software is organized into several files that may or may not be applied, depending on the desired application. The used files were:

- `MemOn_Sweep.py`: This script is applied in the beginning of the characterisation process, to try to change the memristor to the ON state through a sweeping process.
- `MemOff_Sweep.py`: This script is applied to try to change the memristor to the OFF state, through a sweeping process.
- `PulseTrain_SET.py`: This script applies a pulse train of current to the memristor device, measuring the resulting voltage across it and its i-v characteristic. It is used to set the memristor to a low resistance state (LRS).
- `PulseTrain_RESET.py`: This script applies a pulse train of voltage to the memristor device, measuring the resulting current across it and its i-v characteristic. It is used to reset the memristor to a high resistance state (HRS).

Then, the scripts are run in the command line by invoking the Python interpreter followed by the script name. Invoking the script initiates it, which then communicates with the SMU to perform the specified measurements. This outputs an image with the i-v characteristic, the voltage/current being sourced and the measured resistance, and a CSV file with the data collected during the measurement, which can be used for further analysis or plotting.

3.5 Measurement Methodology

Assessing and characterising memristors is complex due to several challenges. These include difficulty in reproducing and replicating device characteristics, the intricate nature of achieving an accurate electroforming process, and the non-trivial task of identifying optimal initial parameters for initiating the measurement process. Despite these hardships, a generalised systematic procedure for measuring these devices is shown in Figure 3.6.

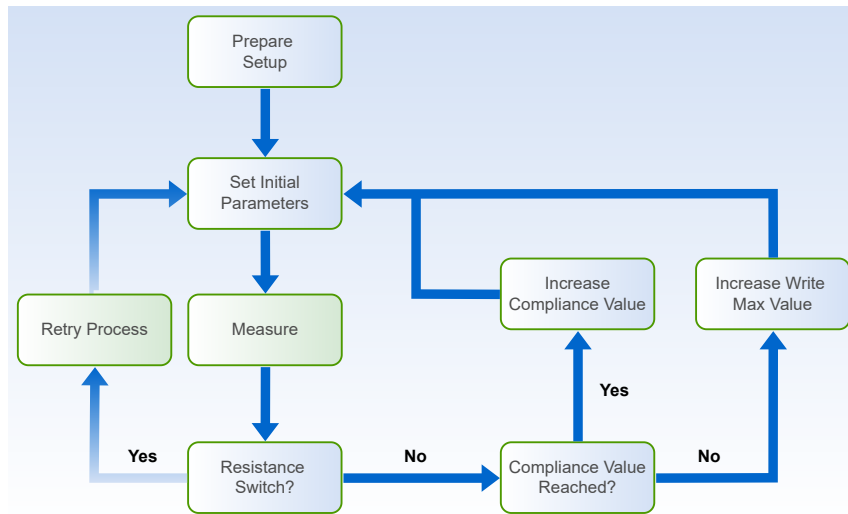


Figure 3.6: Flowchart illustrating the systematic protocol for evaluating memristors. Here, the "Retry Process" is inserted to emphasize trying to replicate previous results.

With the intention of not damaging the device, each measurement cycle begins with small parameter values, making minor changes as the first results emerge. In instances where no resistance switching is observed, this could be attributed to either an insufficient peak write value or the attainment of the compliance value. Subsequently, these values should be incrementally increased until resistance switching is evident. Upon detecting such a switch, one can try to revert to the previous state to determine the parameters associated with the reversal switching process and then proceed to repeat the measurement cycle.

A more detailed and specific description can be said about the administered measurement process, which is divided into two main parts: the SET and RESET operations, listed next.

3.5.1 Typical Procedure

The ideal procedure, to try and change the state of the device, is as follows:

1. **SET:**

- Current Sweep from $1\mu\text{A}$ to 5mA ;
- Voltage compliance: 20V .

2. **RESET**, divided into two stages:

(a) 1st stage:

- Voltage Sweep from 0 to 0.7V ;
- Current compliance: $50\text{--}100\text{mA}$.

(b) 2nd stage:

- Voltage Sweep from 0.7 to 1.2V ;

- Current compliance: 5mA (try to use lower than the maximum used during Current sweep SET).

For the 1st stage circumstances, compliance ensures the SET operation is constrained when the voltage is less than 0.7V. In ideal circumstances, if during the first RESET stage it does not reach a low enough resistance it will hit compliance during second stage right away. A typical solution for this is to either move the 1st stage sweep endpoint voltage to higher values or raise 2nd stage compliance (it should not be higher than the maximum current used for SET). The sweeps are only unidirectional (outwards) to reduce stress on devices, since memristors are extremely sensitive.

3.6 Measurement Results

Given the procedure and being the measured memristors provided by CENIMAT/i3N lab, fabricated with molybdenum disulphide (MoS_2), the next stage tackles the electrical characterisation of these devices. The measured devices for DC characterisation are from the quadrants with test fixture. Figure 3.7 contains the full depiction of the measured devices.

The measured devices were initially in pristine state, and so, in order to determine their initial state, a small sweep from -0.1V to 0.1 V was applied. Usually, the devices are encountered in a high resistance state (HRS), and the characterisation procedure was designed to switch them to a low resistance state (LRS) using sweeping procedures and then to try and turn it back.

From the twenty-one tested devices, only three exhibited clear resistance switching behaviour. These devices are represented by black rectangular boxes in Figure 3.7.

For instance, device no. 8, which is located in the dark box in the upper left quadrant of Figure 3.7, exhibited acceptable switching behaviour. The electrical characterisation of this device (and all of the other ones) was performed using the procedure described in Section 3.5 and the parameters shown in Tables 3.1, 3.2, and 3.3. The results of the electrical characterisation of this device are summarised in Table 3.4.

Table 3.1: Electrical parameters applied onto devices for ON current sweep.

Start Current	Stop Current	Overvoltage protection	Number of Sweep Points
0A	1mA	20V	500

Table 3.2: Electrical parameters applied onto devices for OFF voltage sweep.

Start Voltage	Stop Voltage	Overcurrent protection	Number of Sweep Points
0V	3V	Starts @ 1mA	500

Table 3.3: Electrical parameters applied onto devices for RESET pulse.

Max. Pulse Amplitude V_{max}	V_{step}	Overcurrent protection	Number of points
0.7V	50mV	Starts @ 1mA	1000

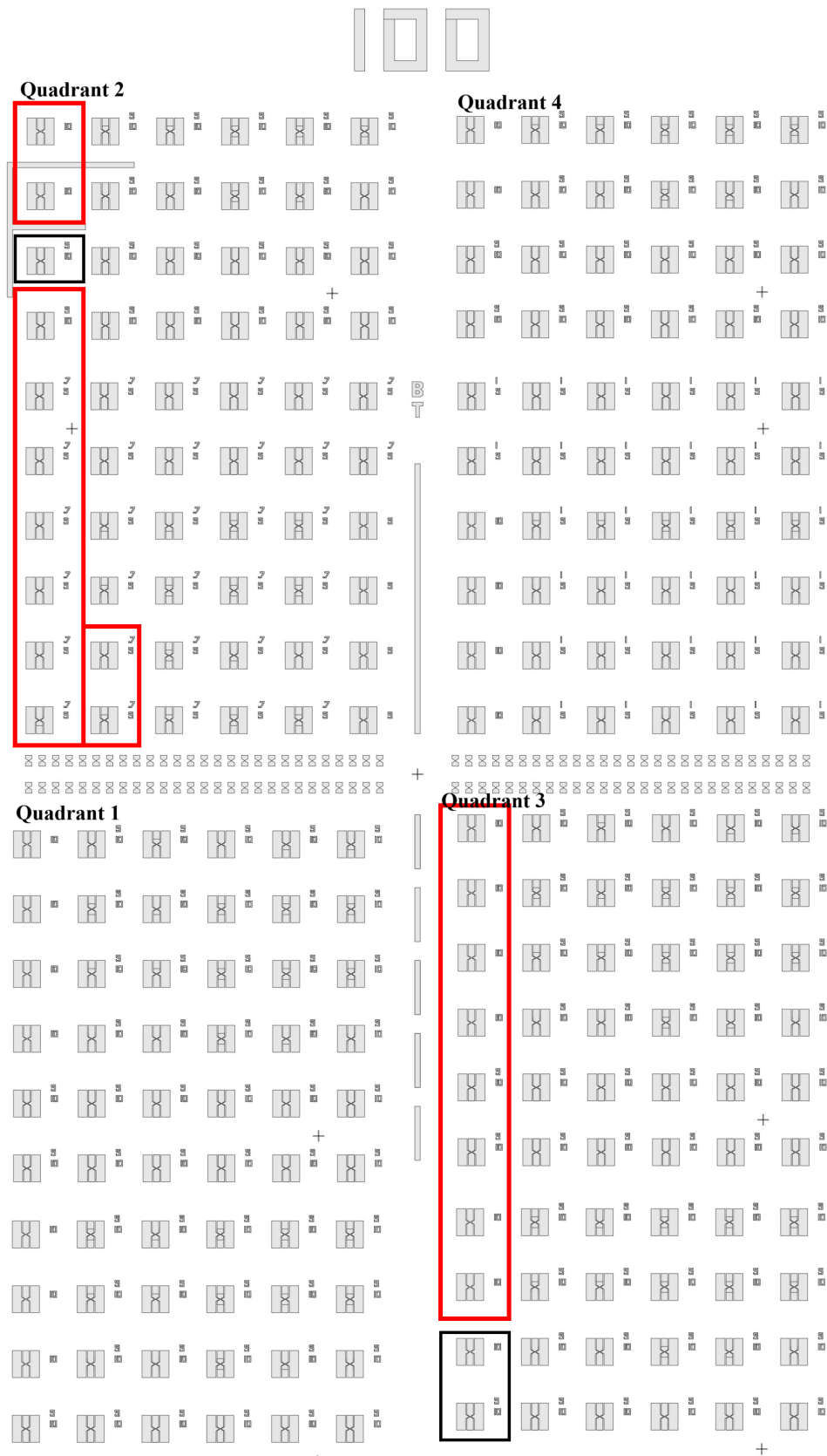


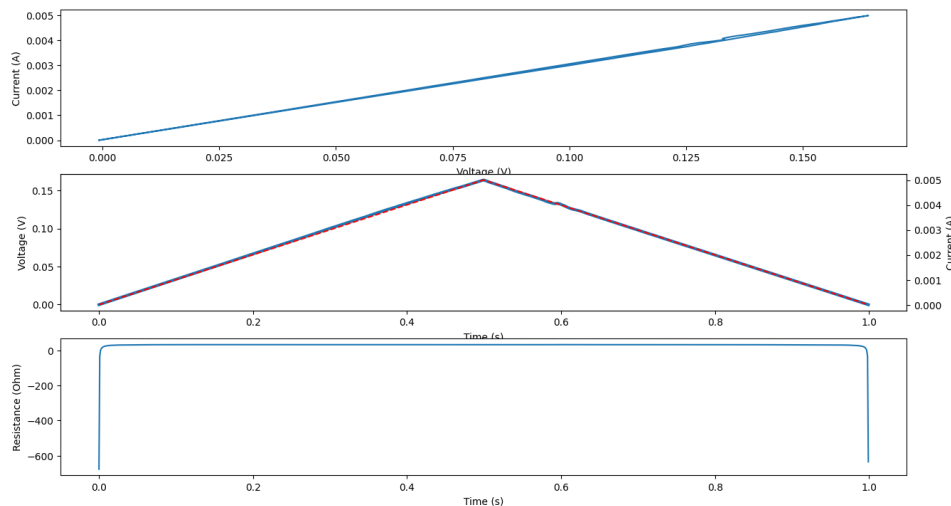
Figure 3.7: Illustration of the tested devices.

Table 3.4: Electrical characterisation results of device no. 8.

2 nd Quadrant	Iteration no.	ON Resistance (LRS)	OFF Resistance (HRS)
Device 8	1	31 Ω	100k Ω
	2	7 Ω	5M Ω to 52 Ω
	3	46 Ω	90k Ω
	4	-	90k Ω
	5	44 Ω	-

As it can be seen in Table 3.4, device no. 8 was measured four times, with the first three iterations showing an evident resistance switching behaviour, with the ON resistance (LRS) and OFF resistance (HRS) values varying across tests¹. The fourth iteration did not show a clear resistance switching behaviour, indicating that the device may have reached a stable state or that the measurement conditions were not optimal for observing the switching behaviour. Although trying to repeat the measurement more times could yield different results, it could also lead to the device being damaged or reaching a point where it no longer switches, which is what generally happened.

Figures 3.8, 3.9, 3.10, and 3.11 show the results of the electrical characterisation of device no. 8, that match the results in Table 3.4. The first and last iterations are shown, with the first iteration showing the ON sweep and the pulse train RESET, which was able to switch the device to HRS, and the last iteration showing the ON sweep and the OFF sweep, which did not switch the device to HRS, showing the device gets stuck in LRS. The hysteresis curves can be observed on the uppermost plot of each figure, which demonstrates the memristors' particular behaviour.

Figure 3.8: Device 8 from 2nd Quadrant, ON sweep, iteration 1.

¹A dash "-" denotes that the value did not change from the preceding result induced by the measurement conditions.

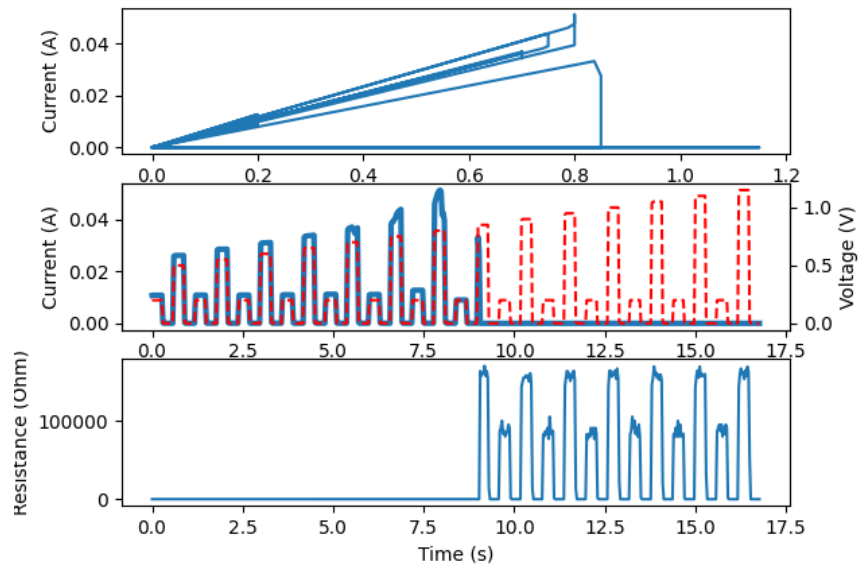


Figure 3.9: Device 8 from 2nd Quadrant, Pulse train RESET, iteration 1.

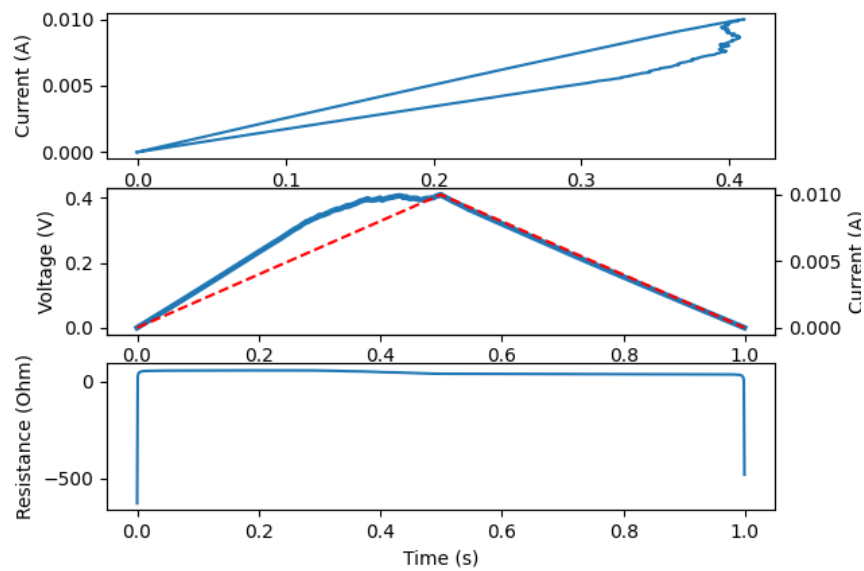


Figure 3.10: Device 8 from 2nd Quadrant, ON sweep, iteration 5.

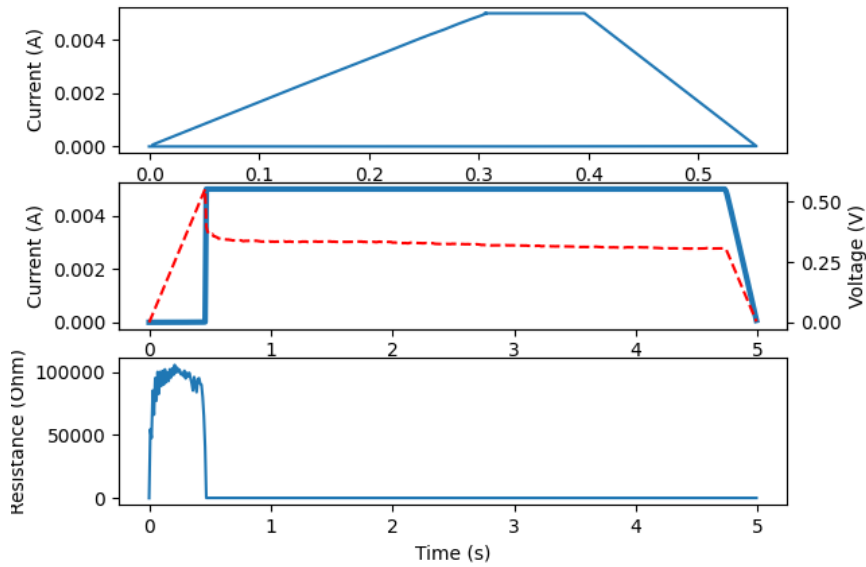


Figure 3.11: Device 8 from 2nd Quadrant, OFF sweep, iteration 5. Neither OFF sweep nor pulsing could switch the device to HRS.

What these results demonstrate, is that memristive devices are highly sensitive and their behaviour can vary significantly across iterations. This variability can be attributed to several factors, including the initial state of the device, the measurement conditions (such as temperature and humidity, electromagnetic interference, or the lack of a cleanroom), and the inherent properties of the memristive material used, in this case, molybdenum disulphide (MoS_2), which can also influence the switching behaviour and the resistance values observed during characterisation. These results also highlight that the best way to try and switch the device is through pulsing (voltage or current), as the sweeping procedure did not prove to be as effective.

These findings prove to be a difficulty in the operation of memristors, as their behaviour can be unpredictable and difficult to replicate. This notion is extremely important when trying to dimension any memristor-based application, which requires heightened attention when handling these devices. This is important to consider when designing the control circuitry that employs memristors in some way, since, being a relatively recent technology, there is still much to learn about their behaviour and how to effectively control them, which can translate into an imperfect performance from the devices.

Another visualisation of the results is shown in Figure 3.12, where the ON (LRS) and OFF (HRS) resistances for the working devices are presented as boxplots. Devices that did not conform to the expected switching behaviour are excluded from this depiction (because most of them had not any expected behaviour whatsoever, i.e., were completely out of specification).

Amidst the characterised samples, selecting an optimal candidate for further testing and integration into the switching circuit proved crucial. The foremost considerations for this choice were the device's behaviour and ability to change between states consecutively. Of all relevant devices,

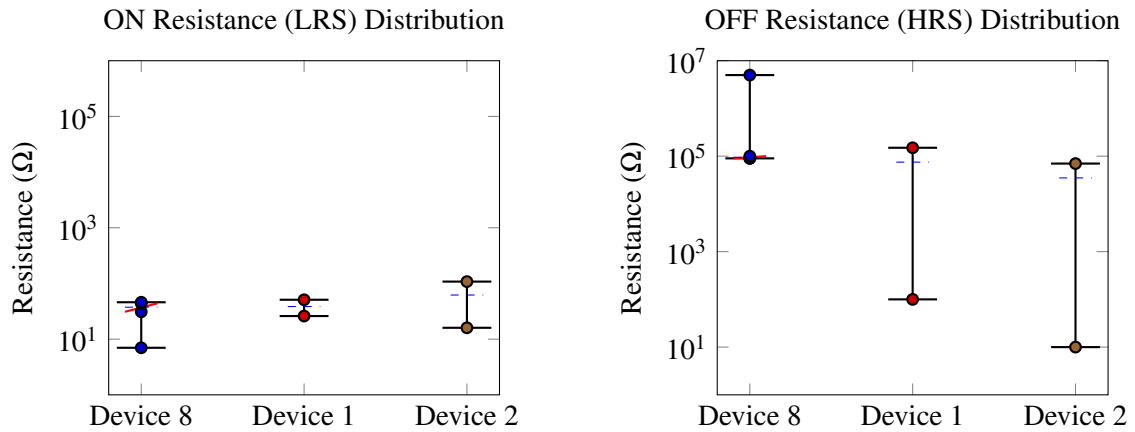


Figure 3.12: Boxplots of ON (LRS) and OFF (HRS) resistances for working devices. Points show raw data; dashed lines indicate means.

device no. 8 emerged as the most suitable candidate, demonstrating the most consistent resistance switching behaviour across multiple iterations. This device can be chosen for further testing and integration into the switching circuit and memristor-based applications.

3.7 Conceptual Circuit Description

In a preparatory stage, the design of the control circuit for memristors was conceptualised. Since *a priori* knowledge of the memristor's switching characteristics is necessary, the design was based on the understanding of how memristors operate, studied in Section 3.2, and how they can be controlled to achieve the desired switching behaviour.

As discussed earlier, this circuit is designed to induce the memristor's switching states, allowing it to operate as an RF switch. The circuit includes a bias line, a memristor, and two switches: one for setting the memristor (I_{SET}) and another for resetting the memristor (V_{RESET}), Figures 3.13 and 3.14, respectively. The goal is to toggle the state of the memristor between ON and OFF, enabling or disabling the RF signal path. With the circuit from Figure 3.1 in mind, the nodes I_{SET} and V_{RESET} will connect to the main circuit according to the desired operation.

In essence, what this circuit does is that it emulates the SMU's functionality onto a centralised design. The ramp is continuously generated, to provide several sweeps throughout time, and so is the pulse generation, with constant pulses. With the two integrated, a pulsed linear sweep is produced, mimicking the target behaviour. They are very similar in principle, the only change is what variable is being controlled, either current or voltage. The circuit blocks are designed accordingly and described in the following subsections.

3.7.1 SET control

This circuit is designed to introduce a current onto the memristor, to shift it to its SET state. Figure 3.13 shows a diagram with the function blocks to perform SET operation. This circuit will

try to adjust the resistance value (R_{ON}) of the memristor based on the measured resistance values. The real components with which it was implemented are described in Section 3.8.

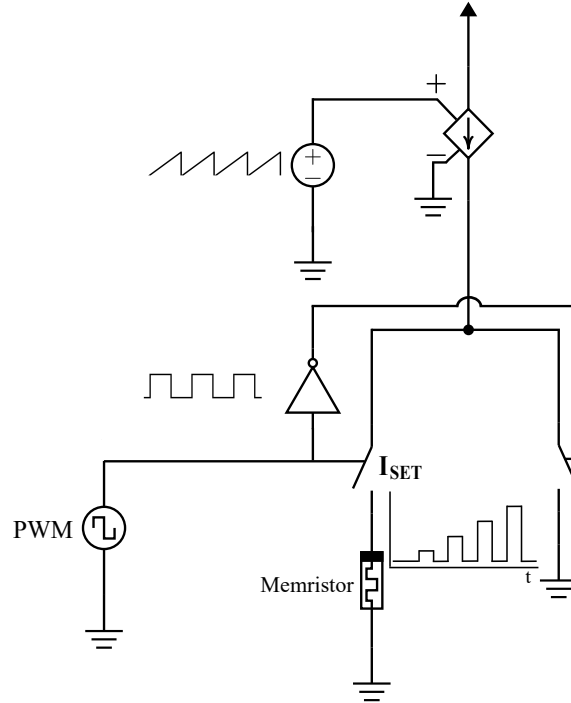


Figure 3.13: Switching blocks for the memristor SET control.

3.7.2 RESET control

This circuit is designed to introduce a voltage onto the memristor, to change it to its RESET state. As a result, Figure 3.14 shows a diagram with the function blocks to perform RESET operation. This circuit will try to adjust the resistance value (R_{OFF}) of the memristor based on the measured resistance values. As previously, the real components with which it was implemented are described in Section 3.8.

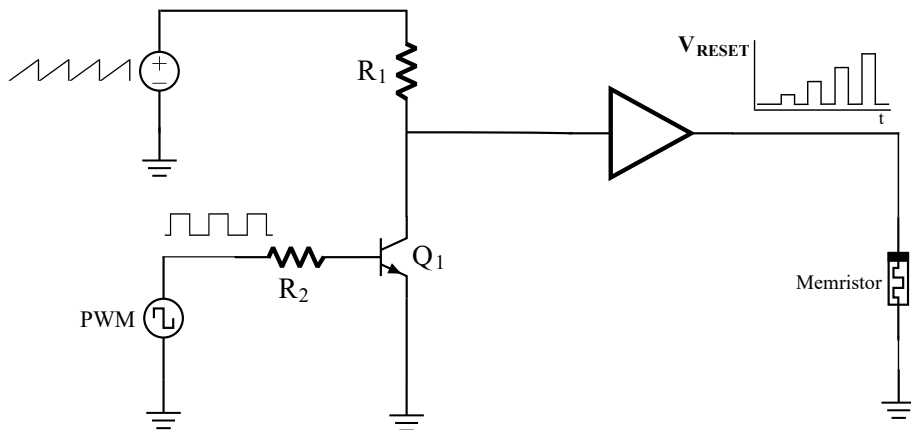


Figure 3.14: Switching blocks for the memristor RESET control.

3.8 Design of the Fundamental Circuit Blocks for Memristor Controlling

Once these frameworks are defined, the next step is to map them onto circuit components that embody their working principles in a physical implementation. In Figure 3.15, the circuit is described as a single structure to tackle the state change of a memristor. As with many circuits, this can be divided into several functional blocks, each designed to perform a specific task in obtaining the desired results.

These blocks were carefully designed and implemented based on the requirements of the overall system. Figure 3.15 highlights these blocks in different colours for clarity. The reasoning behind the design choices, and how they were tested and validated, are discussed in detail in the next subsections.

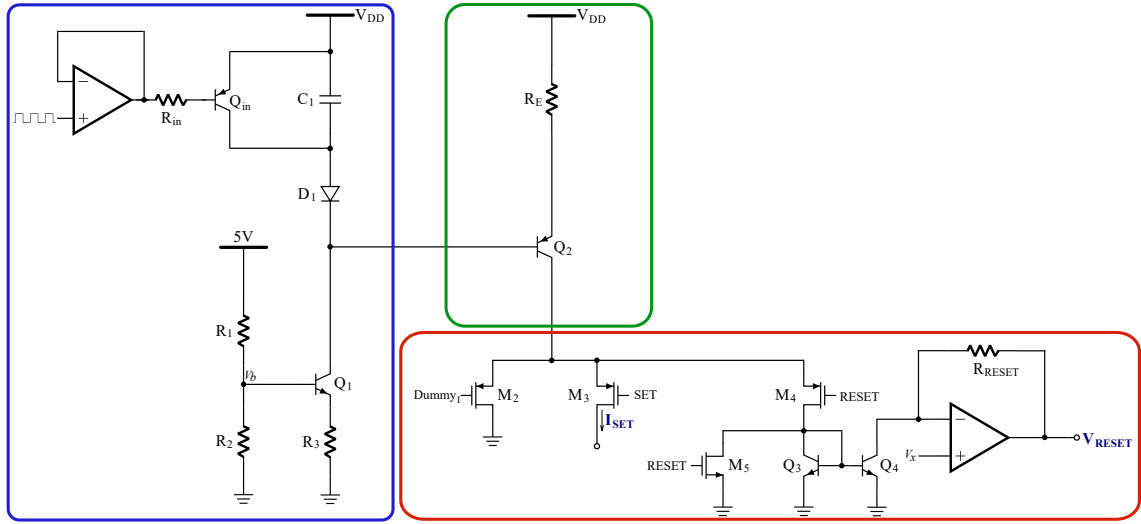


Figure 3.15: Circuit with highlighted blocks.

3.8.1 Ramp Signal generation

The proper control of memristors involves stimulation pulse and sweep signals, which were recreated first in the lab environment through the use of an SMU. The idea is to create a standalone circuit that can generate these signals, which can be used to control and change the memristor's internal resistance state. Fundamentally, a ramp waveform must be created to control the memristor's switching behaviour, as it allows for a gradual change in voltage or current, which is key for the proper operation of these devices.

As illustrated in Figure 3.16, the ramp signal is generated using a combination of an operational amplifier and a resistor in series, a PNP bipolar junction transistor, a capacitor, and a diode, to create a smooth and controlled voltage change over time. This ramp is constantly repeated using the pulse signal created by the 555 timer IC, triggering the ramp generation circuit at regular intervals.

The op-amp outputs the same voltage that is applied to its non-inverting input. This configuration is used to buffer the signal and provide a low output impedance. The resistor in series with the op-amp limits the current flowing into the base of the PNP transistor, protecting it from excessive current. This configuration, from Figure 3.16, consists on having the PNP transistor's emitter connected to a positive voltage supply and to the capacitor, while the collector is connected to the capacitor and a diode. The base is driven by a control signal, which turns the PNP ON and OFF. When the PNP is ON, it allows current to flow from the supply to the capacitor, causing it to discharge. When the PNP is OFF, the capacitor holds its charge until it is discharged through the diode.

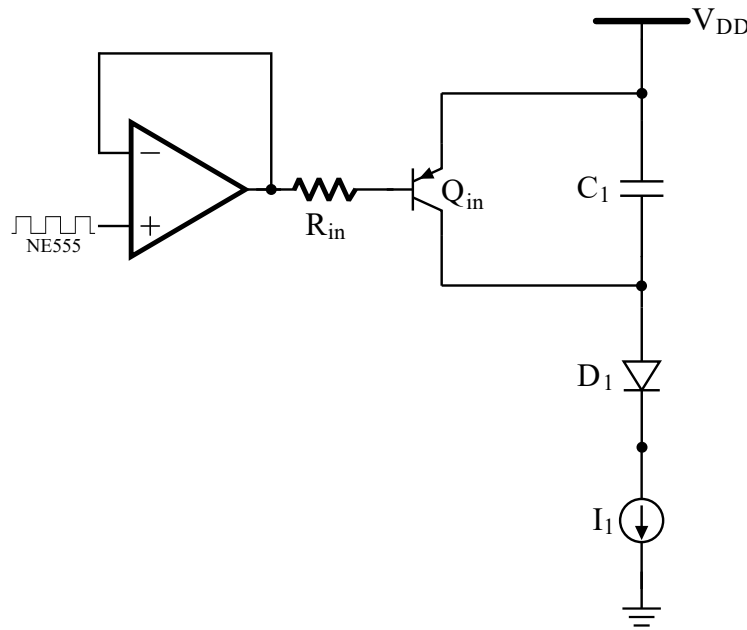


Figure 3.16: Ramp signal generation.

Here, from the diode cathode onwards, a current source is necessary to provide the ramp signal for the rest of the circuit, which combined with the opamp, R_{in} , Q_{in} , C_1 , and D_1 translates the control voltage that is used in the voltage controlled current source shown in Figure 3.13. Moreover, the diode ensures that the ramp signal starts from a known reference point (0V) and prevents any unwanted negative voltages that could affect the operation of the circuit. This creates a ramp-like voltage waveform proportional through time across the capacitor, which can be used to control the circuit. This voltage value can be calculated by:

$$\Delta V_{ramp} = \frac{I}{C} \cdot \Delta t, \quad (3.1)$$

where I is the current provided by the current source, C is the capacitance of the capacitor, and Δt is the time interval.

This current source is then implemented with actual circuit components, as shown in the orange rectangle of Figure 3.17, in order to perform the wanted operation. This is achieved by using

an NPN transistor and resistors. Resistors R_1 and R_2 form a simple voltage divider network (with a lower voltage supply, at 5V) used to bias the NPN transistor into conduction. Since this voltage divider lightly loads the transistor, the base voltage, V_B can be easily calculated by using the simple voltage divider formula as follows:

$$V_B = V_{DD} \cdot \frac{R_2}{R_1 + R_2}. \quad (3.2)$$

The NPN transistor acts as the active regulator that controls the total current flow. By correctly setting the emitter voltage, this can be easily adjusted. Using Ohm's law, the current flowing through the emitter, I_E , can be calculated as:

$$I_E = \frac{V_B - V_{BE}}{R_3}, \quad (3.3)$$

where V_{BE} is the voltage drop between the base and emitter of the NPN transistor, typically around 0.7V for silicon transistors. Essentially, this configuration outputs the needed current at the collector, since $I_C \approx I_E$. In addition to this, when combined together, the circuits in Figure 3.17 form the stage represented by blue in Figure 3.15. This stage basically creates the control voltage (the ramp signal) that is used in the voltage controlled current source shown in Figure 3.13.

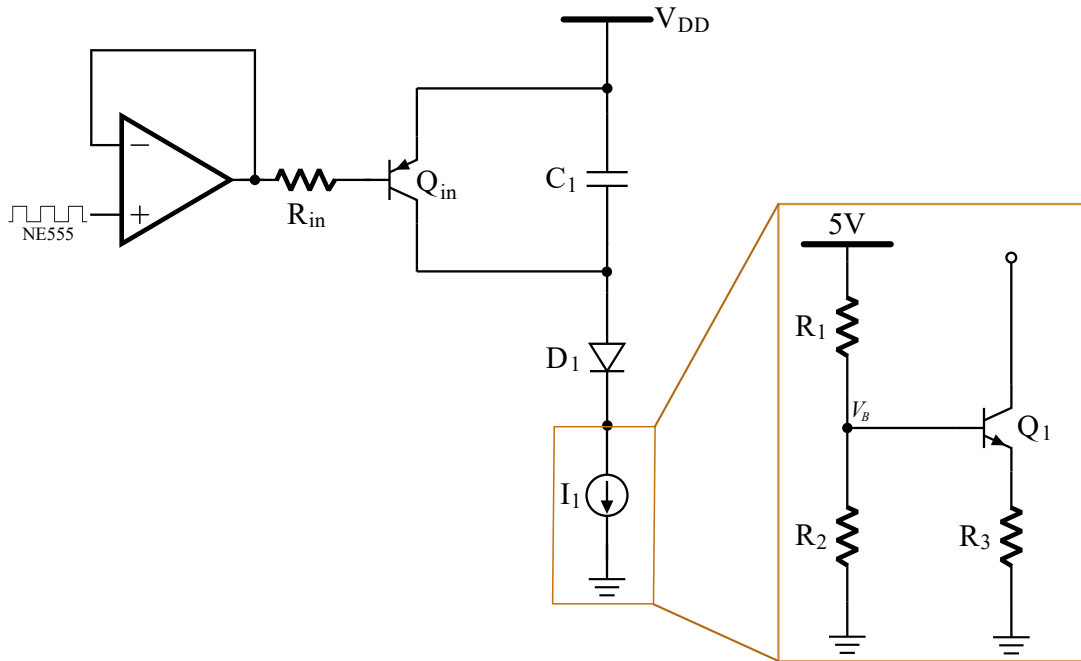


Figure 3.17: Current source.

3.8.2 Controlled Current Source

As mentioned earlier, the voltage ramp signal that is used in the voltage controlled current source shown in Figure 3.13 has been created and is ready to be used. This voltage ramp will feed the controlled current source. The full circuit from Figure 3.17 can be simplified as a simple voltage

source indicating the ramp waveform, as shown in Figure 3.18a. This voltage source is used as the control for the controlled current source, which is also represented in Figure 3.18a.

This controlled current source is implemented using a PNP transistor and resistor R_E , as seen in Figure 3.18b., which is used to provide a constant current to the following paths that will be operating the memristor. With R_E in series, the current delivered to the next stage is controlled and limited. The base voltage of the PNP transistor is driven by the ramp signal, and the emitter voltage is connected to a positive voltage supply. The emitter-base junction sets a constant current through the emitter resistor, which in turn sets the collector current, allowing current to flow accordingly from there. Basically, the symbols used in Figure 3.18a are in reality translated by the components as in Figure 3.18b, performing the desired functionality.

In a broader perspective, the previously explained stages work together to provide a stable and controlled current to the memristor, as indicated in Figure 3.18, which in turn corresponds to the green-highlighted stage in Figure 3.15.

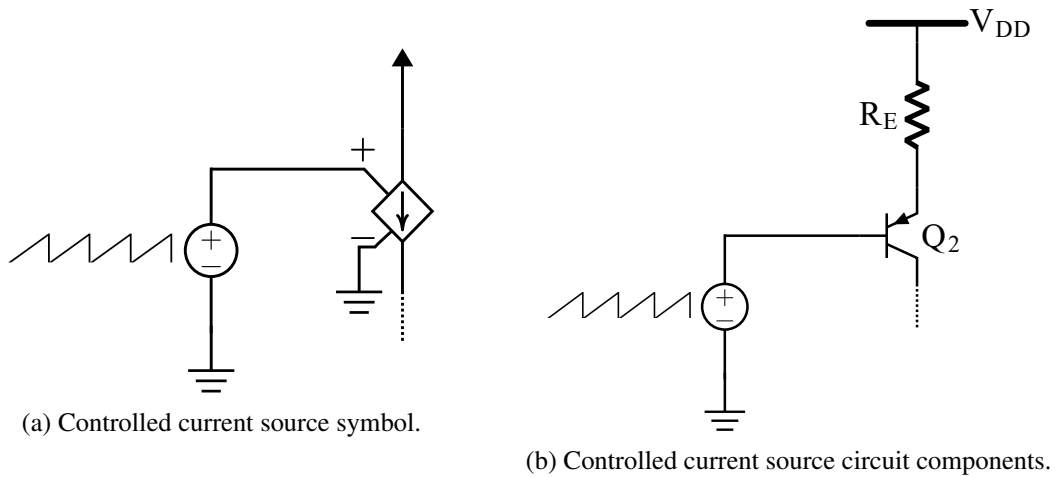


Figure 3.18: Full controlled current source equivalent.

3.8.3 SET stage

The SET stage is responsible for controlling the current applied to the memristor during the SET operation. This stage is quite simple, as it only requires a PMOS, M_3 , to follow the current behaviour that is being applied to it, and to feed it onto the memristor. Basically, the PMOS is responsible for outputting the necessary current ramp. The M_2 transistor works as a dummy transistor, to ensure that the current always has a path to flow through.

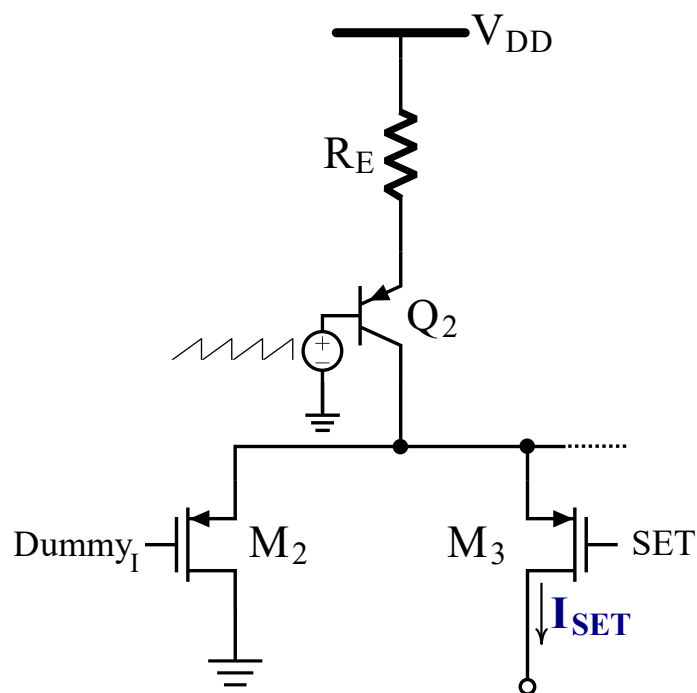


Figure 3.19: PMOS transistor that provides the current for the SET operation.

3.8.4 RESET stage

As for the RESET stage, it is responsible for controlling the voltage applied to the memristor during the RESET operation. The concept employed in Figure 3.14 was the first way to think of the implementation for this part of the circuit. However, the actual implementation is slightly different, as shown in Figure 3.20. The CENIMAT laboratory later instructed on how the RESET operation should be performed, and so, the circuit was adapted to these new requirements. Since both operations were now to be performed in a pulsed manner, the circuit was modified to accommodate this change. Since the easiest way to use the ramp along with the pulse was the PMOS, that outputs the current for the SET operation, the same concept was applied to the RESET operation, basically converting this signal into a voltage. This saves components and space, as the ramp is already being generated through the rest of the circuit.

This stage is more complex, as it requires a voltage signal coming from the rest of the circuit which is current-based. As a result of this, a current to voltage converter is required to convert the current signal into a voltage signal. First, the PMOS is used to follow the current behaviour, similarly to the SET stage. Then, a current mirror is applied to copy the desired current through one active device by controlling the current in another active device. Later, an op-amp is used to convert the current signal into a voltage signal. In addition, the non-inverting input of the op-amp is connected to a voltage divider, which sets the reference voltage for the op-amp.

This current to voltage converter is implemented using an operational amplifier in a non-inverting configuration. The op-amp is configured to have a gain of 1, meaning that the output

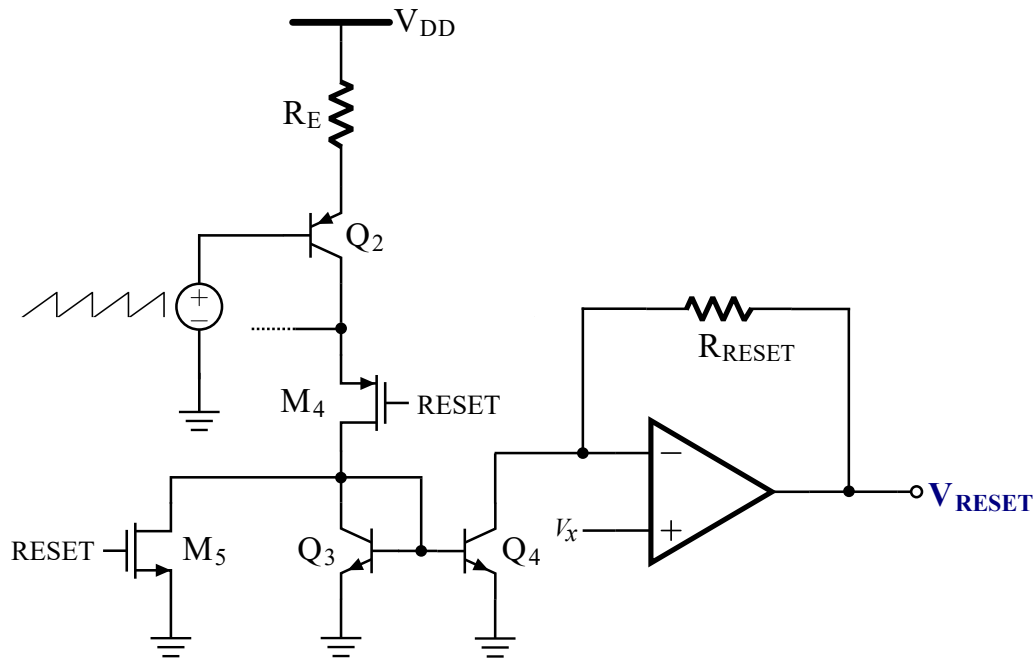


Figure 3.20: Components that provide the voltage for the RESET operation.

voltage follows the input voltage. This way, the voltage applied to the memristor during the RESET operation is controlled by the ramp signal generated in the first stage of the circuit.

The voltage denoted by V_x , at the non-inverting input of the op-amp, in Figure 3.20, is determined by the voltage V_x in Figure 3.21. Connecting the base to the collector of the NPN transistor, makes it operate as a diode, with a voltage drop of approximately 0.7V. This ensures that the voltage at the non-inverting input of the op-amp is always around this value. Both the SET and RESET operating components are included in the red contoured selection in Figure 3.15.

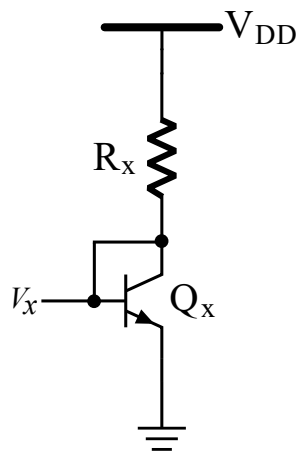


Figure 3.21: Non-inverting input for the opamp.

Concluding, the final paths for the memristor control are shown in Figure 3.22, where the possible paths for each operation are shown (either I_{SET} or V_{RESET}).

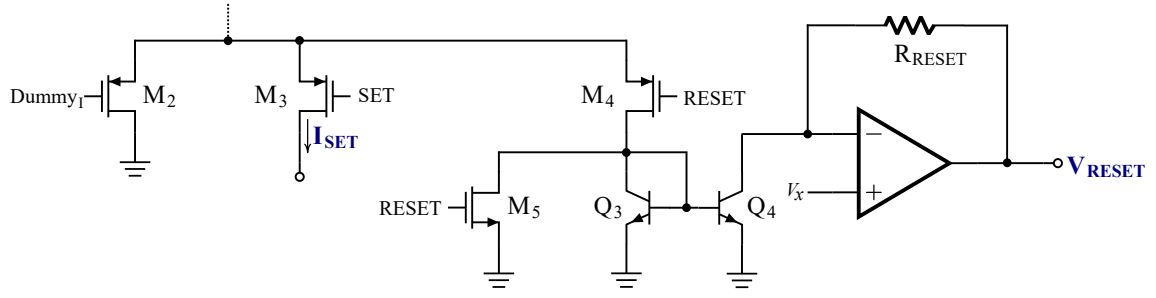


Figure 3.22: Final paths for the memristor control.

3.8.5 Logic for selection of memristor path

Now, given all the paths and blocks, the next step is to select which path to use, either SET or RESET. For this purpose, the proposed approach is to use an assortment of logic gates to achieve this goal. In order to find out what were the required logic gates and to make a design one step ahead, a truth table was created, Table 3.5. The idea here is to have two inputs, one for SET and another for RESET. There are three available paths to follow. A simple PMOS, that just conducts current for the circuit not to be floating, *per se*, a path for SET and another for RESET.

The first possible path is represented by PMOS1, the second possible path is represented by PMOS2 and the third possible path is represented by PMOS3. Keeping in mind that a PMOS is turned on "low", the truth table was then elaborated as follows:

Table 3.5: Truth table for the logic gates.

S1	S0	PMOS1	PMOS2	PMOS3
0	0	1	1	1
0	1	0	0	1
1	0	0	1	0
1	1	1	1	1

From the truth table, it is possible to derive the following Boolean expressions for each path:

$$\text{PMOS1} = \overline{S_1 \cdot \overline{S_0}} + \overline{\overline{S_1} \cdot S_0} = \overline{S_1 \oplus S_0}, \quad (3.4)$$

$$\text{PMOS2} = \overline{\overline{S_1} \cdot S_0} = S_1 + \overline{S_0}, \quad (3.5)$$

$$\text{PMOS3} = \overline{S_1 \cdot \overline{S_0}} = \overline{S_1} + S_0. \quad (3.6)$$

The first expression, PMOS1, defines an XNOR gate, which means that PMOS1 will be ON, meaning 0, when either S1 or S0 is ON, but not both. This was done to avoid both paths being ON at the same time, as this cannot happen. Moreover, this was also done so that PMOS1 wouldn't turn on by itself, as a means to save power.

As for PMOS2, the output is 0 (ON) only when $S1 = 0$ AND $S0 = 1$, and for PMOS3, the output is 0 (ON) only when $S1 = 1$ AND $S0 = 0$. Two approaches can be taken, either using NAND gates or OR gates, using the most suitable expression for either one. Both of these could be translated into NAND gates with an inverter on one of the inputs. Additionally, the NAND gate holds particular importance in digital integrated circuits because any Boolean logic function can be constructed solely from NAND gates. This characteristic, known as "functional completeness," is also shared by the NOR gate. Digital systems often leverage this property, allowing complex logic circuits to be built efficiently using only NAND gates. Although in this case it is not crucial for the implementation, it is still a good practice to maintain it. The final implementation of the logic gates is shown in Figure 3.23. M2 and M3 represent the signals coming from the controlled pulses from a possible external FPGA or microcontroller, that dictate when to perform either operation. These gates control the gates of the PMOS transistors that select the path for the memristor control. It is important to note that these signals (SET, RESET and DUMMY), operate "alongside" the PWM signal (seen in Figures 3.14 and 3.13), which will be explained next.

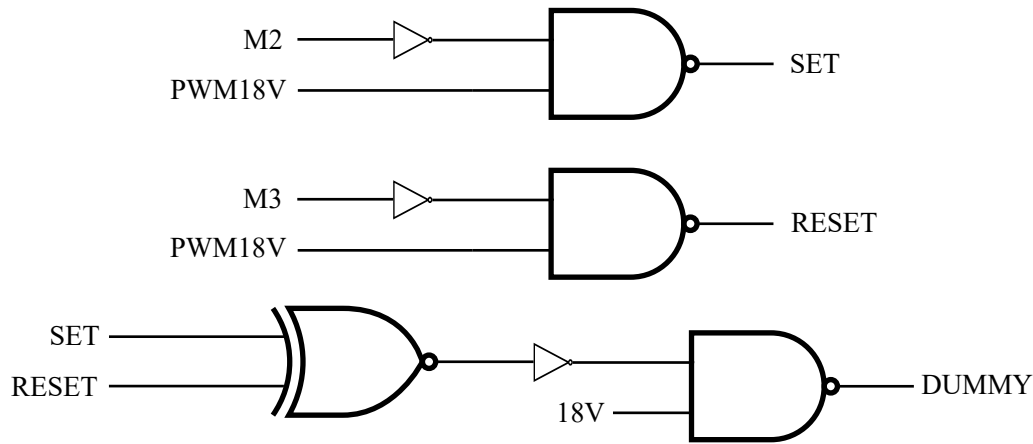


Figure 3.23: Logic Gates Implementation.

3.9 Simulation Process and Results

Once the circuit was designed, it was simulated using LTspice. In this section, a compilation of the simulation results is presented. All the results shown were done performing a non-linear, time-domain transient simulation of the circuit, with a time span of 120ms.

The supply voltage is set to +18V throughout the whole implementation. The used library for the logic gates and MOSFET transistors is the *CD4000* library, which is a family of CMOS logic integrated circuits (the same one used for the implementation of the logic gates). It is indeed an old library, but it is one of the few libraries that supports 18V operation and is readily available.

555 Timer

For the implementation of the pulse signal that controls the pulses for the ramp in LTspice, the 555 timer was used. This IC is a highly stable device for generating accurate time delays or oscillation. This timer was chosen for its versatility, and operates from a wide range of power, ranging from +5V to +18V supply voltage. The pin diagram is shown in Figure 3.24. The timer can be activated by ensuring the correct external resistors and capacitors are connected for the astable mode (continuous oscillation) to start automatically, and its implementation can be seen in Appendix D.

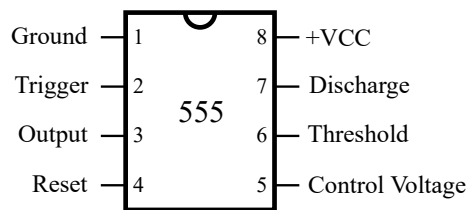


Figure 3.24: 555 Timer IC Pin Diagram.

After connecting the power supply to VDD (pin 8) and ground to pin 1, the external resistors and a capacitor are connected to pins 6 and 7 to establish an oscillation frequency. Pin 5 is not used, and is connected to ground via a 10nF capacitor to eliminate any noise. The output on pin 3 will continuously switch between high and low states at a frequency determined by the values of the connected resistors and capacitor. Figure 3.25 shows the 555 timer circuit output signal shape, used to generate the pulse signal that dictates the timing for the ramp generation circuit, along with the pulse produced by it.

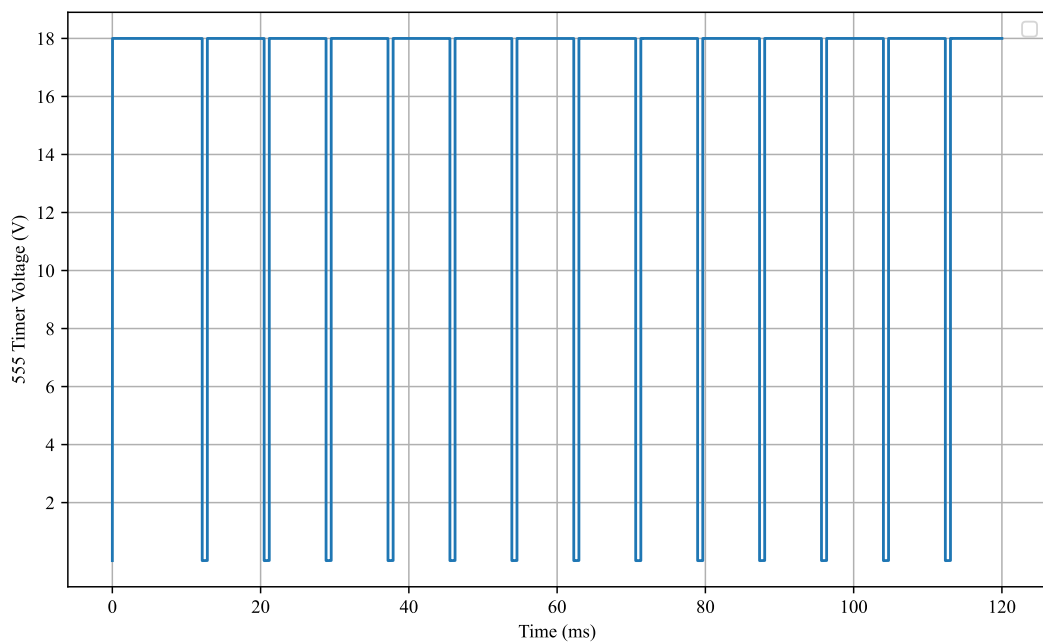


Figure 3.25: Output signal of the 555 timer circuit.

Voltage-Controlled Pulse Width Modulator

This pulse signal is applied to the logic gates to provide a pulsing signal for the inputs of the logic gates, more particularly. was performed using the LTC6992, a voltage-controlled pulse width modulator (PWM). The LTC6992 is a silicon oscillator with voltage-controlled pulse width modulation that can be used to generate a PWM signal with a variable duty cycle based on an input voltage from 0V to 1V [58], applied on the MOD pin in Figure 3.26.

This device is particularly useful for applications where precise control of the output signal is required, such as in motor control, LED dimming, and other power management tasks. The LTC6992 was selected over similar devices due to its simplicity and ease of use.

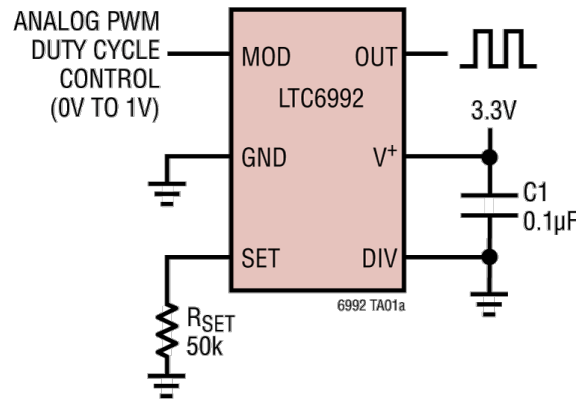


Figure 3.26: LTC6992 Voltage-Controlled Pulse Width Modulator example pin diagram [58].

As the LTC6992 can only operate up to a maximum power supply voltage of 5.5V, the provided voltage to the VDD pin is 5V. The master oscillator frequency is determined by a single R_{SET} resistor connected to the SET pin, which is set to 392 k Ω , in this case, resulting in an ideal frequency of $f_{out} = 2$ kHz. The duty cycle of the output signal is controlled by the voltage applied to the MOD pin, which is set to 0.5V in this case, resulting in a duty cycle of approximately 50%. As recommended by the TimerBlox Web Tools by Analog Devices, Inc., the remaining resistor values are set to $R_1 = 1$ M Ω and $R_2 = 280$ k Ω .

Considering that the given supply voltage to the device is 5V, the output signal cannot reach higher than that value. For this reason, an NPN transistor and pull-up resistor, shown in Figure 3.27, are required to ensure that the output signal sources the desired voltage level of +18V. A pull-up resistor of 5k Ω is connected to the NPN transistor's collector, which provides the PWM signal, with the desired voltage level, to the necessary circuit components. Since the input signal is applied to the base, the 1k Ω resistor is required to feed current into the base of the NPN transistor.

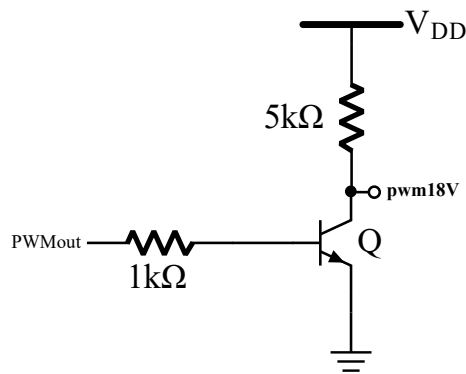


Figure 3.27: Configuration for PWM signal to reach desired supply voltage.

Figure 3.28 shows the pulse signal generated by the LTC6992, which is used to control the timing of the signals applied to the PMOS transistors, with the aid of the logic gates implementation.

Figure 3.29 shows the ramp signal generated by the circuit, which is used to control the current and voltage applied to the memristor. The initial gradual increase (or decrease, depending on where we view the ramp) of the signal can be explained by the initial transient behaviour of the circuit, which is expected following a sudden change in conditions, in this case, the charging of the capacitor in the ramp generation circuit. During this initial period of time, the voltage varies before settling into a steady-state condition or regime.

Figure 3.30 shows the output signals of the logic gates, which are used to select the appropriate path for the memristor control, which then activates the PMOS transistors accordingly. These signals are applied to the gates of the PMOS transistors, controlling their operation. The signals are generated based on the logic defined in the truth table, ensuring that only one path is active at any given time. As stated previously, the signals are designed to be complementary, meaning that when one signal is high, the other is low, and vice versa. This ensures that the dummy PMOS and only one other PMOS transistor (either the one responsible for the SET or RESET) is turned on at any given time, preventing any potential conflicts or short circuits in the circuit.

Figures 3.31 and 3.32 show the final output signals applied to the memristor, which are used to change its resistance state. These signals exhibit spikes during the transitions, caused by capacitive coupling. However, it is important to note that this effect is normal and will not significantly affect the performance of the memristor. Despite the memristor being a bit sensitive, the short temporal width of these spikes prevents the device from reacting quickly enough to introduce a measurable change in state.

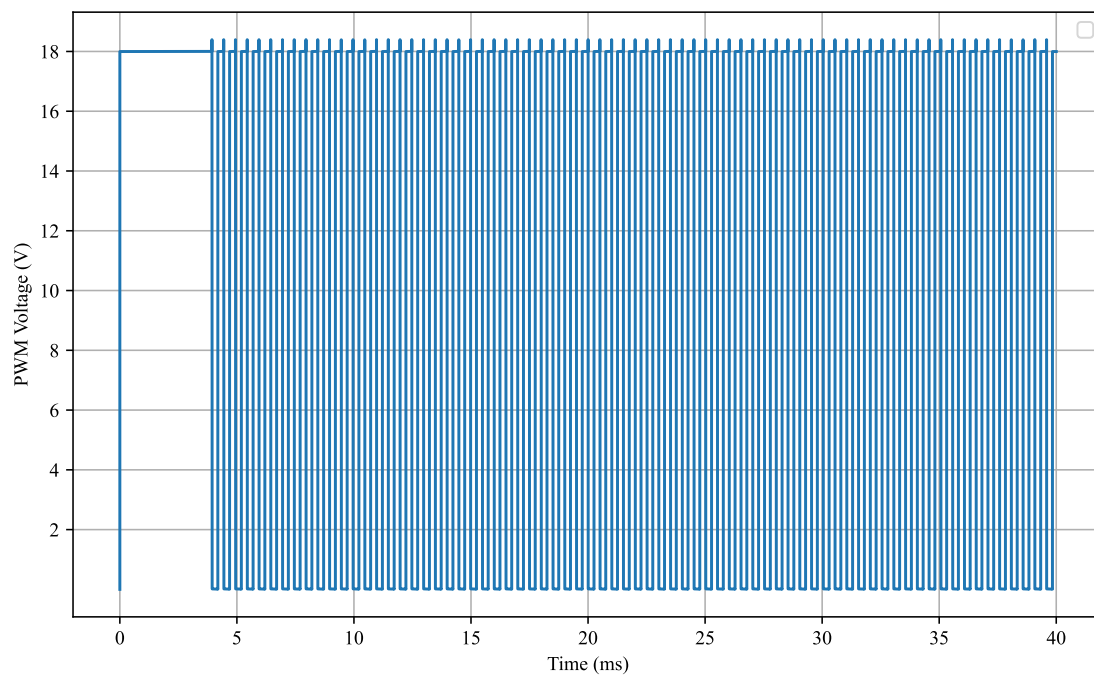


Figure 3.28: Pulse signal generated by the LTC6992, after connecting the NPN transistor and pull-up resistor.

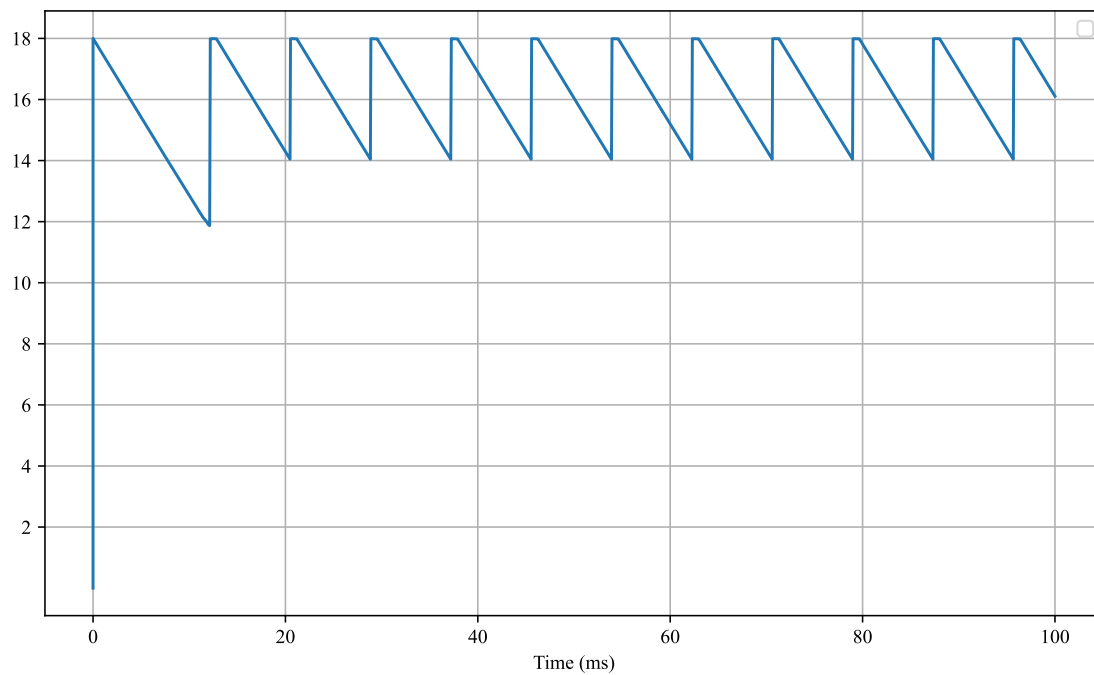


Figure 3.29: Ramp signal generated by the circuit.

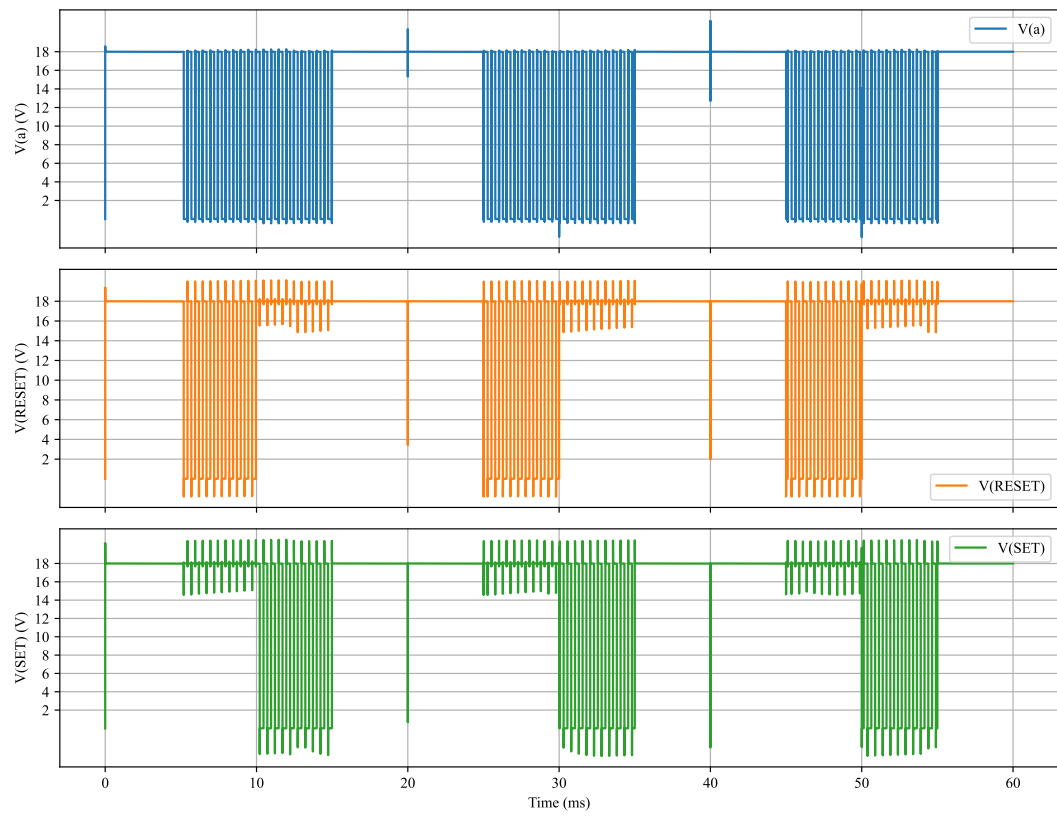


Figure 3.30: Output signals of the logic gates/signals that are applied onto the PMOS transistors.

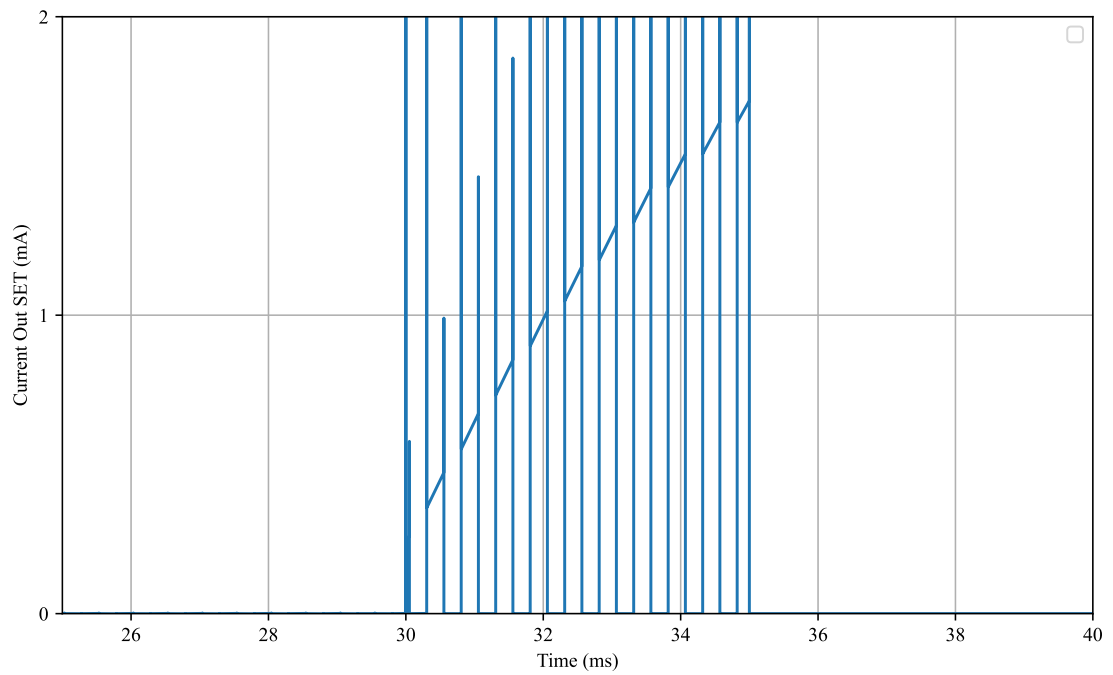


Figure 3.31: Excerpt of the output signal applied to the memristor during the SET operation.

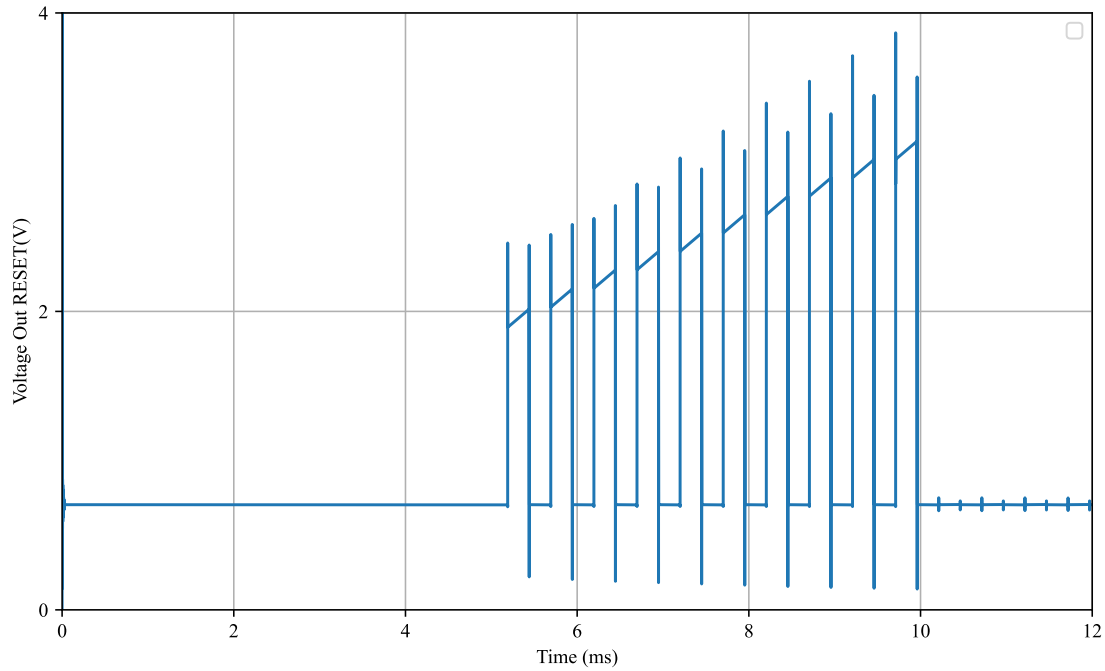


Figure 3.32: Excerpt of the output signal applied to the memristor during the RESET operation.

3.10 Final remarks

Current RIS prototypes often rely on conventional technologies like PIN diodes or varactors for controlling the phase and amplitude of reflected signals. While functional, these components can be energy-intensive, relatively bulky, and offer limited continuous tunability. Memristors, with their inherent non-volatility, nanoscale footprint, and analogue resistance states, present a radical alternative. Using memristors allows for far more granular, energy-efficient, and potentially faster control over each individual RIS element.

This chapter has presented a circuit design that allows for the control of memristors, using standard and accessible components, which basically emulates the functionality of a Source Measure Unit (SMU) to apply pulsing or sweeping techniques in a more practical and cost-effective manner. This causes the memristor to shift its state and provide an ON or OFF state, useful for RF applications, and, obviously, in RIS systems.

The proposed circuit design is advantageous for several reasons:

- **Practicality:** The circuit is designed to be practical for real-world applications. This way, the circuit can control the memristor with a standard voltage source, which is more representative of how memristors would be used in actual electronic and communication systems.
- **Integration:** It can be easily integrated into larger systems, allowing for more complex operations and interactions with other components. Most real-world applications integrate electronic devices with other circuit components, not with laboratory equipment like SMUs.

- **Cost-Effectiveness:** Using a simple circuit with standard components is generally more cost-effective than relying on specialized equipment like SMUs or other expensive laboratory equipment. SMUs are expensive and not always available in all laboratories or production environments, nor would they be employed for future 6G deployment while standard voltage sources are more accessible and affordable. An SMU alone is expensive and bulky (the one used for testing cost ≈ 10000 €), while the proposed circuit can be implemented with inexpensive, compact components.
- **Scalability:** The circuit approach can be scaled up for larger systems or multiple memristors, whereas using multiple laboratory equipment can be impractical and expensive.
- **Flexibility:** The circuit can be adjusted or modified to suit different experimental needs or configurations (other voltage values, e.g.), providing greater flexibility than a fixed setup.

In essence, the circuit provides a more realistic, cost-effective, and scalable way to operate memristors in practical applications. More importantly, it provides a better implementation for using memristors as switches, specifically when creating 6G systems (which will require a multitude of building blocks and components to be used in the future).

Chapter 4

Conclusion

This chapter summarises the key findings of this dissertation, discusses their implications, and suggests directions for future research.

This dissertation's work imposed the need to explore the potential of memristors in RF switching applications, particularly in the context of Reconfigurable Intelligent Surfaces (RIS) for 6G networks. By organising a successful study onto the nature of memristors, and how to control them, the work has contributed to the understanding of how these devices can be integrated into the groundwork of advanced communication systems.

Three main stages were followed in this work, a more theoretical stage, where the behaviour of memristors was studied and simulated, a measurement stage, where the memristors were characterised and tested in a laboratory environment, and finally, a design stage, where the circuit was designed, tested and validated through simulations.

A significant contribution of this work is the comprehensive exploration of memristors, encompassing aspects of design, analysis, and modeling which is a key bedrock for future research. The central objective was to evaluate the potential for integrating these components into RIS systems. To achieve this, a variety of instruments and electronic frameworks were implemented and applied to test and utilise the memristor's capabilities.

One of the main findings is the effectiveness of the proposed control circuit for memristors in RF switching applications. The circuit demonstrated reliable performance in toggling the memristor states, showing promise for future integration into RIS systems.

In essence, the successful development and validation of a functioning control circuit for memristor-based RF switching stands as a testament to the practical viability of the proposed approach, marking a significant step towards real-world implementation in advanced wireless communication systems, namely for 6G networks.

4.1 Future Work

Although the produced results are pleasing and meet the desired objectives, there are still several areas for future research and development.

Future work could focus on optimising the control circuit for better performance and efficiency, potentially exploring alternative materials for memristors that do not suffer from the same limitations of present-day materials, such as those that are more resistant to electromigration and oxidation. Overall, and as seen in this work, the ongoing exploration of memristor capabilities holds the potential for significant breakthroughs in numerous technological applications. More specifically, future work could include the design and fabrication of a complete RIS prototype incorporating the memristor-based control circuit and benchmarking its performance against traditional designs.

References

- [1] C. Pan, H. Ren, K. Wang, J. F. Kolb, M. El-kashlan, M. Chen, M. Di Renzo, Y. Hao, J. Wang, A. L. Swindlehurst, X. You, and L. Hanzo, "Reconfigurable intelligent surfaces for 6g systems: Principles, applications, and research directions," *IEEE Communications Magazine*, vol. 59, no. 6, pp. 14–20, 6 2021, ISSN: 15581896. DOI: [10.1109/MCOM.001.2001076](https://doi.org/10.1109/MCOM.001.2001076).
- [2] R. Chen, M. Liu, Y. Hui, N. Cheng, and J. Li, "Reconfigurable intelligent surfaces for 6g iot wireless positioning: A contemporary survey," *IEEE Internet of Things Journal*, vol. 9, no. 23, pp. 23 570–23 582, 2022. DOI: [10.1109/JIOT.2022.3203890](https://doi.org/10.1109/JIOT.2022.3203890).
- [3] A. Araghi, M. Khalily, M. Safaei, A. Bagheri, V. Singh, F. Wang, and R. Tafazolli, "Reconfigurable intelligent surface (ris) in the sub-6 ghz band: Design, implementation, and real-world demonstration," *IEEE Access*, vol. 10, pp. 2646–2655, 2022. DOI: [10.1109/ACCESS.2022.3140278](https://doi.org/10.1109/ACCESS.2022.3140278).
- [4] C. Nwifo, O. Simpson, and Y. Sun, "Reconfigurable intelligent surfaces (ris) and their role in next-generation wireless networks: An overview," *Transactions on Emerging Telecommunications Technologies*, vol. 36, 6 May 2025, ISSN: 21613915. DOI: [10.1002/ett.70164](https://doi.org/10.1002/ett.70164).
- [5] M. V. Katwe, A. Kaushik, L. Mohjazi, M. Abualhayja'a, D. Dardari, K. Singh, M. A. Imran, M. M. Butt, and O. A. Dobre, "An overview of intelligent meta-surfaces for 6g and beyond: Opportunities, trends, and challenges," *IEEE Communications Standards Magazine*, vol. 8, no. 4, pp. 62–69, 2024. DOI: [10.1109/MCOMSTD.0001.2400032](https://doi.org/10.1109/MCOMSTD.0001.2400032).
- [6] K. Vaigandla, S. Bolla, and R. Karne, "A survey on future generation wireless communications - 6g: Requirements, technologies, challenges and applications," *International Journal of Advanced Trends in Computer Science and Engineering*, vol. 10, pp. 3067–3076, 5 Oct. 2021. DOI: [10.30534/ijatcse/2021/211052021](https://doi.org/10.30534/ijatcse/2021/211052021).
- [7] E. Basar, G. C. Alexandropoulos, Y. Liu, Q. Wu, S. Jin, C. Yuen, O. A. Dobre, and R. Schober, "Reconfigurable intelligent surfaces for 6g: Emerging hardware architectures, applications, and open challenges," *IEEE Vehicular Technology Magazine*, Jul. 2024, ISSN: 1556-6072. DOI: [10.1109/MVT.2024.3415570](https://doi.org/10.1109/MVT.2024.3415570). [Online]. Available: <https://ieeexplore.ieee.org/document/10596064>.
- [8] Q. Wu and R. Zhang, "Beamforming optimization for wireless network aided by intelligent reflecting surface with discrete phase shifts," *IEEE Transactions on Communications*, vol. 68, pp. 1838–1851, 3 Mar. 2020, ISSN: 15580857. DOI: [10.1109/TCOMM.2019.2958916](https://doi.org/10.1109/TCOMM.2019.2958916).
- [9] F. H. S. Fonseca, G. I. Morais, G. C. Clemente, and C. J. B. Pagan, "Tunable 2-bit unit cell based in a square loop for reconfigurable intelligent surface application," in *2022 Asia-Pacific Microwave Conference (APMC)*, 2022, pp. 875–877. DOI: [10.23919/APMC55665](https://doi.org/10.23919/APMC55665).

- 2022.9999789. [Online]. Available: <https://ieeexplore.ieee.org/document/9999789>.
- [10] M. Dajer, Z. Ma, L. Piazzzi, N. Prasad, X. F. Qi, B. Sheen, J. Yang, and G. Yue, “Reconfigurable intelligent surface: Design the channel – a new opportunity for future wireless networks,” *Digital Communications and Networks*, vol. 8, pp. 87–104, 2 Apr. 2022, ISSN: 2352-8648. DOI: [10.1016/j.dcan.2021.11.002](https://doi.org/10.1016/j.dcan.2021.11.002).
 - [11] E. Björnson, H. Wymeersch, B. Matthiesen, P. Popovski, L. Sanguinetti, and E. de Carvalho, “Reconfigurable intelligent surfaces: A signal processing perspective with wireless applications,” *IEEE Signal Processing Magazine*, vol. 39, no. 2, pp. 135–158, Mar. 2022, ISSN: 1558-0792. DOI: [10.1109/msp.2021.3130549](https://doi.org/10.1109/msp.2021.3130549). [Online]. Available: <http://dx.doi.org/10.1109/MSP.2021.3130549>.
 - [12] V. Tapio, I. Hemadeh, A. Mourad, A. Shojaeifard, and M. Juntti, “Survey on reconfigurable intelligent surfaces below 10 ghz,” *EURASIP J. Wirel. Commun. Netw.*, vol. 2021, no. 1, Sep. 2021, ISSN: 1687-1472. DOI: [10.1186/s13638-021-02048-5](https://doi.org/10.1186/s13638-021-02048-5). [Online]. Available: <https://doi.org/10.1186/s13638-021-02048-5>.
 - [13] M. A. Elmoallamy, H. Zhang, L. Song, K. G. Seddik, Z. Han, and G. Y. Li, “Reconfigurable intelligent surfaces for wireless communications: Principles, challenges, and opportunities,” *IEEE Transactions on Cognitive Communications and Networking*, vol. 6, pp. 990–1002, 3 Sep. 2020, ISSN: 23327731. DOI: [10.1109/TCCN.2020.2992604](https://doi.org/10.1109/TCCN.2020.2992604).
 - [14] Q. Wu, S. Zhang, B. Zheng, C. You, and R. Zhang, “Intelligent reflecting surface-aided wireless communications: A tutorial,” *IEEE Transactions on Communications*, vol. 69, no. 5, pp. 3313–3351, 5 May 2021, ISSN: 15580857. DOI: [10.1109/TCOMM.2021.3051897](https://doi.org/10.1109/TCOMM.2021.3051897).
 - [15] A. K. Singh, A. K. Maurya, R. Prakash, P. Thakur, and B. B. Tiwari, “Reconfigurable intelligent surface with 6g for industrial revolution: Potential applications and research challenges,” *Paladyn, Journal of Behavioral Robotics*, vol. 14, no. 1, p. 20 220 114, 2023. DOI: [doi:10.1515/pjbr-2022-0114](https://doi.org/10.1515/pjbr-2022-0114). [Online]. Available: <https://doi.org/10.1515/pjbr-2022-0114>.
 - [16] S. R. Hasan, S. R. Sabuj, M. Hamamura, and M. A. Hossain, “A comprehensive review on reconfigurable intelligent surface for 6g communications: Overview, deployment, control mechanism, application, challenges, and opportunities,” *Wireless Personal Communications*, vol. 139, no. 1, pp. 375–429, Nov. 2024, ISSN: 1572-834X. DOI: [10.1007/s11277-024-11630-1](https://doi.org/10.1007/s11277-024-11630-1). [Online]. Available: <https://doi.org/10.1007/s11277-024-11630-1>.
 - [17] M. Elsaid, S. I. Inácio, H. M. Salgado, and L. M. Pessoa, “Memristor-based 1-bit reconfigurable intelligent surface for 6g communications at d-band,” in *2024 International Conference on Electromagnetics in Advanced Applications (ICEAA)*, 2024, pp. 694–699. DOI: [10.1109/ICEAA61917.2024.10701868](https://doi.org/10.1109/ICEAA61917.2024.10701868).
 - [18] F. Liu, A. Pitilakis, M. S. Mirmoosa, O. Tsilipakos, X. Wang, A. C. Tasolamprou, S. Abadal, A. Cabellos-Aparicio, E. Alarcón, C. Liaskos, N. V. Kantartzis, M. Kafesaki, E. N. Economou, C. M. Soukoulis, and S. Tretyakov, “Programmable metasurfaces: State of the art and prospects,” in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2018, pp. 1–5. DOI: [10.1109/ISCAS.2018.8351817](https://doi.org/10.1109/ISCAS.2018.8351817).
 - [19] N. O. Parchin, H. J. Basherlou, Y. I. Al-Yasir, A. M. Abdulkhaleq, and R. A. Abd-Alhameed, “Reconfigurable antennas: Switching techniques— a survey,” *Electronics (Switzerland)*, vol. 9, 2 Feb. 2020, ISSN: 20799292. DOI: [10.3390/electronics9020336](https://doi.org/10.3390/electronics9020336).

- [20] M. Baena-Molina, Á. Palomares-Caballero, G. Martínez-García, R. Padial-Allué, P. Padilla, and J. F. Valenzuela-Valdés, “1-bit ris unit cell with mechanical reconfiguration at 28 ghz,” in *2024 18th European Conference on Antennas and Propagation (EuCAP)*, 2024, pp. 1–5. DOI: [10.23919/EuCAP60739.2024.10500936](https://doi.org/10.23919/EuCAP60739.2024.10500936).
- [21] I. P. Hong, “Reviews based on the reconfigurable intelligent surface technical issues,” *Electronics*, vol. 12, no. 21, Nov. 2023. DOI: [10.3390/electronics12214489](https://doi.org/10.3390/electronics12214489).
- [22] Q. Hu, X. Zeng, C. Mao, H. Yang, Q. Wu, J. Tang, X. L. Zhao, and X. Y. Zhang, “Design of a novel 2-bit wideband beam-scanning reconfigurable intelligent surface,” in *IEEE International Workshop on Electromagnetics: Applications and Student Innovation Competition, iWEM 2021 - Proceedings*, Institute of Electrical and Electronics Engineers Inc., 2021, ISBN: 9781665418287. DOI: [10.1109/iWEM53379.2021.9790574](https://doi.org/10.1109/iWEM53379.2021.9790574).
- [23] H. Mosallaei and K. Sarabandi, “Antenna miniaturization and bandwidth enhancement using a reactive impedance substrate,” *IEEE Transactions on Antennas and Propagation*, vol. 52, pp. 2403–2414, 9 Sep. 2004, ISSN: 0018926X. DOI: [10.1109/TAP.2004.834135](https://doi.org/10.1109/TAP.2004.834135).
- [24] L. G. da Silva, Z. Chu, P. Xiao, and A. C. S, “A varactor-based 1024-element ris design for mm-waves,” *Frontiers in Communications and Networks*, vol. 4, 2023, ISSN: 2673530X. DOI: [10.3389/frcmn.2023.1086011](https://doi.org/10.3389/frcmn.2023.1086011).
- [25] J.-C. Chen, “Improving energy efficiency in pin-diode-based ris-assisted wireless systems,” *IEEE Wireless Communications Letters*, vol. 13, no. 12, pp. 3370–3374, 2024. DOI: [10.1109/LWC.2024.3465650](https://doi.org/10.1109/LWC.2024.3465650).
- [26] H. Rajagopalan, Y. Rahmat-Samii, and W. A. Imbriale, “Rf mems actuated reconfigurable reflectarray patch-slot element,” *IEEE Transactions on Antennas and Propagation*, vol. 56, pp. 3689–3699, 12 2008, ISSN: 0018926X. DOI: [10.1109/TAP.2008.2007388](https://doi.org/10.1109/TAP.2008.2007388).
- [27] T. Mingates, M. Ghatas, J. Deuermeier, J. Neilson, A. Kelly, J. Coleman, L. Mendes, J. Vaz, S. Matos, L. Lucci, A. Clemente, Z. Sofer, L. Pessoa, E. Fortunato, R. Martins, and A. Kiazadeh, “Unipolar and non-volatile rf switches using mos2 by liquid-liquid interface assembly for millimeter wave applications,” *PREPRINT (Version 1)*, May 2025. [Online]. Available: <https://doi.org/10.21203/rs.3.rs-6726705/v1>.
- [28] C. Huang, C. Zhang, J. Yang, B. Sun, B. Zhao, and X. Luo, “Reconfigurable metasurface for multifunctional control of electromagnetic waves,” *Advanced Optical Materials*, vol. 5, 22 Nov. 2017, ISSN: 21951071. DOI: [10.1002/adom.201700485](https://doi.org/10.1002/adom.201700485).
- [29] J. Rao, Y. Zhang, S. Tang, Z. Li, C. Y. Chiu, and R. Murch, “An active reconfigurable intelligent surface utilizing phase-reconfigurable reflection amplifiers,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 71, pp. 3189–3202, 7 Jul. 2023, ISSN: 15579670. DOI: [10.1109/TMTT.2023.3237029](https://doi.org/10.1109/TMTT.2023.3237029).
- [30] B. Mohammad, M. A. Jaoude, V. Kumar, D. M. A. Homouz, H. A. Nahla, M. Al-Qutayri, and N. Christoforou, “State-of-the-art of metal-oxide memristor devices,” *Nanotechnology Reviews*, vol. 5, no. 3, pp. 311–329, Jun. 2016, ISSN: 21919097. DOI: [10.1515/ntrev-2015-0029](https://doi.org/10.1515/ntrev-2015-0029). [Online]. Available: <https://doi.org/10.1515/ntrev-2015-0029>.
- [31] K. Gou, Y. Li, H. Song, R. Lu, and J. Jiang, “Optimization strategy of the emerging memristors: From material preparation to device applications,” *iScience*, vol. 27, no. 12, p. 111 327, 2024, ISSN: 2589-0042. DOI: <https://doi.org/10.1016/j.isci.2024.111327>. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/S2589004224025525>.

- [32] M. J. Rozenberg and P. Levy, “Resistive switching in oxide non-volatile electronic memories,” LPS, CNRS – Université Paris-Sud, Tech. Rep., 2010. [Online]. Available: <https://equipes.lps.u-psud.fr/theorie/wp-content/uploads/sites/15/2021/12/marcelo.pdf>.
- [33] J. S. Lee, S. Lee, and T. W. Noh, “Resistive switching phenomena: A review of statistical physics approaches,” *Applied Physics Reviews*, vol. 2, 3 Sep. 2015, ISSN: 19319401. DOI: [10.1063/1.4929512](https://doi.org/10.1063/1.4929512).
- [34] Y. Yang and W. Lu, “Nanoscale resistive switching devices: Mechanisms and modeling,” *Nanoscale*, vol. 5, pp. 10 076–10 092, 21 Nov. 2013, ISSN: 20403364. DOI: [10.1039/c3nr03472k](https://doi.org/10.1039/c3nr03472k).
- [35] M. K. Song, J. H. Kang, X. Zhang, W. Ji, A. Ascoli, I. Messaris, A. S. Demirkol, B. Dong, S. Aggarwal, W. Wan, S. M. Hong, S. G. Cardwell, I. Boybat, J. S. Seo, J. S. Lee, M. Lanza, H. Yeon, M. Onen, J. Li, B. Yildiz, J. A. del Alamo, S. Kim, S. Choi, G. Milano, C. Ricciardi, L. Alff, Y. Chai, Z. Wang, H. Bhaskaran, M. C. Hersam, D. Strukov, H. S. Wong, I. Valov, B. Gao, H. Wu, R. Tetzlaff, A. Sebastian, W. Lu, L. Chua, J. J. Yang, and J. Kim, “Recent advances and future prospects for memristive materials, devices, and systems,” *ACS Nano*, vol. 17, pp. 11 994–12 039, 13 Jul. 2023, ISSN: 1936086X. DOI: [10.1021/acsnano.3c03505](https://doi.org/10.1021/acsnano.3c03505).
- [36] M. Potrebíć, D. Tošić, and D. Biolek, “Rf/microwave applications of memristors,” in *Studies in Computational Intelligence*. Springer Verlag, Feb. 2017, vol. 701, pp. 159–185. DOI: [10.1007/978-3-319-51724-7_7](https://doi.org/10.1007/978-3-319-51724-7_7).
- [37] L. Chua, “Memristor-the missing circuit element,” *IEEE Transactions on Circuit Theory*, vol. 18, no. 5, pp. 507–519, Sep. 1971, ISSN: 0018-9324. DOI: [10.1109/TCT.1971.1083337](https://doi.org/10.1109/TCT.1971.1083337).
- [38] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, “The missing memristor found,” *Nature*, vol. 453, pp. 80–83, 7191 May 2008, ISSN: 00280836. DOI: [10.1038/nature06932](https://doi.org/10.1038/nature06932).
- [39] G. K. Johnsen, “An introduction to the memristor - a valuable circuit element in bioelectricity and bioimpedance,” *Journal of Electrical Bioimpedance*, vol. 3, pp. 20–28, 1 2012, ISSN: 18915469. DOI: [10.5617/jeb.305](https://doi.org/10.5617/jeb.305).
- [40] L. Chua, “Resistance switching memories are memristors,” *Applied Physics A: Materials Science and Processing*, vol. 102, pp. 765–783, 4 Mar. 2011, ISSN: 09478396. DOI: [10.1007/s00339-011-6264-9](https://doi.org/10.1007/s00339-011-6264-9). [Online]. Available: <https://doi.org/10.1007/s00339-011-6264-9>.
- [41] R. E. S. da Silva, “Towards brain-inspired computing: Memristor-based single layer neural networks,” Master’s thesis, Instituto Superior Técnico, Universidade de Lisboa, Nov. 2023. [Online]. Available: <https://scholar.tecnico.ulisboa.pt/records/ZPqcl9zIl2gF0YFoigOB1fsZQSZGN08Sr5Oh>.
- [42] J. Yu, Y. Wang, S. Qin, G. Gao, C. Xu, Z. L. Wang, and Q. Sun, *Bioinspired interactive neuromorphic devices*, Nov. 2022. DOI: [10.1016/j.mattod.2022.09.012](https://doi.org/10.1016/j.mattod.2022.09.012).
- [43] S. Kim and J. Lee, “Tcad simulation of resistive switching devices: Impact of reram configuration on neuromorphic computing,” *Nanomaterials*, vol. 14, 23 Dec. 2024, ISSN: 20794991. DOI: [10.3390/nano14231864](https://doi.org/10.3390/nano14231864).

- [44] T. H. Kim, S. Kim, K. Hong, J. Park, Y. Hwang, B. G. Park, and H. Kim, "Multilevel switching memristor by compliance current adjustment for off-chip training of neuromorphic system," *Chaos, Solitons and Fractals*, vol. 153, Dec. 2021, ISSN: 09600779. DOI: [10.1016/j.chaos.2021.111587](https://doi.org/10.1016/j.chaos.2021.111587).
- [45] J. J. Yang, D. B. Strukov, and D. R. Stewart, "Memristive devices for computing," *Nature Nanotechnology*, vol. 8, pp. 13–24, 1 2013, ISSN: 1748-3395. DOI: [10.1038/nnano.2012.240](https://doi.org/10.1038/nnano.2012.240).
- [46] E. Apollos, "Memristor theory and mathematical modelling," *International Journal of Computer Applications*, vol. 178, pp. 1–8, 27 Jun. 2019. DOI: [10.5120/ijca2019919089](https://doi.org/10.5120/ijca2019919089).
- [47] Y. N. Joglekar and S. J. Wolf, "The elusive memristor: Properties of basic electrical circuits," *European Journal of Physics*, vol. 30, no. 4, p. 661, May 2009. DOI: [10.1088/0143-0807/30/4/001](https://doi.org/10.1088/0143-0807/30/4/001). [Online]. Available: <https://dx.doi.org/10.1088/0143-0807/30/4/001>.
- [48] T. Prodromakis, B. P. Peh, C. Papavassiliou, and C. Toumazou, "A versatile memristor model with nonlinear dopant kinetics," *IEEE Transactions on Electron Devices*, vol. 58, pp. 3099–3105, 9 Sep. 2011, ISSN: 0018-9383. DOI: [10.1109/TED.2011.2158004](https://doi.org/10.1109/TED.2011.2158004).
- [49] S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Team: Threshold adaptive memristor model," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, pp. 211–221, 1 Jan. 2013, ISSN: 15498328. DOI: [10.1109/TCSI.2012.2215714](https://doi.org/10.1109/TCSI.2012.2215714).
- [50] H. Abdalla and M. D. Pickett, "Spice modeling of memristors," in *2011 IEEE International Symposium of Circuits and Systems (ISCAS)*, IEEE, 2011, pp. 1832–1835, ISBN: 9781424494743. DOI: [10.1109/ISCAS.2011.5937942](https://doi.org/10.1109/ISCAS.2011.5937942).
- [51] S. Kvatinsky, M. Ramadan, E. G. Friedman, and A. Kolodny, "Vteam: A general model for voltage-controlled memristors," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, no. 8, pp. 786–790, Aug. 2015. DOI: [10.1109/TCSII.2015.2433536](https://doi.org/10.1109/TCSII.2015.2433536).
- [52] D. Biolek, Z. Kolka, V. Biolková, Z. Biolek, and S. Kvatinsky, "(v)team for spice simulation of memristive devices with improved numerical performance," *IEEE Access*, vol. 9, pp. 30 242–30 255, 2021, ISSN: 21693536. DOI: [10.1109/ACCESS.2021.3059241](https://doi.org/10.1109/ACCESS.2021.3059241).
- [53] I. Vourkas, A. Batsos, and G. C. Sirakoulis, "Spice modeling of nonlinear memristive behavior," *International Journal of Circuit Theory and Applications*, vol. 43, no. 5, pp. 553–565, 2013. DOI: <https://doi.org/10.1002/cta.1957>. eprint: <https://onlinelibrary.wiley.com/doi/pdf/10.1002/cta.1957>. [Online]. Available: <https://onlinelibrary.wiley.com/doi/abs/10.1002/cta.1957>.
- [54] F. García-Redondo, R. P. Gowers, A. Crespo-Yepes, M. López-Vallejo, and L. Jiang, "Spice compact modeling of bipolar/unipolar memristor switching governed by electrical thresholds," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 8, pp. 1255–1264, 2016. DOI: [10.1109/TCSI.2016.2564703](https://doi.org/10.1109/TCSI.2016.2564703).
- [55] D. Biolek, V. Biolková, and Z. Biolek, "Spice model of memristor with nonlinear dopant drift," *Radioengineering*, vol. 18, no. 2, pp. 210–214, Jun. 2009, ISSN: 1805-9600. [Online]. Available: <https://api.semanticscholar.org/CorpusID:19016545>.
- [56] J. Yu, X. Mu, X. Xi, and S. Wang, "A memristor model with piecewise window function," *Radioengineering*, vol. 22, no. 4, pp. 969–974, Dec. 2013. [Online]. Available: <https://api.semanticscholar.org/CorpusID:30024669>.

- [57] G. C. Trichopoulos, P. Theofanopoulos, B. Kashyap, A. Shekhawat, A. Modi, T. Osman, S. Kumar, A. Sengar, A. Chang, and A. Alkhateeb, "Design and evaluation of reconfigurable intelligent surfaces in real-world environment," *IEEE Open Journal of the Communications Society*, vol. 3, pp. 462–474, 2022, ISSN: 2644125X. DOI: [10.1109/OJCOMS.2022.3158310](https://doi.org/10.1109/OJCOMS.2022.3158310).
- [58] A. D. Inc., "Ltc6992-1: Timerblox: Voltage-controlled pulse width modulator (pwm) data sheet (rev.d)," Tech. Rep., 2012. [Online]. Available: <https://www.analog.com/media/en/technical-documentation/data-sheets/LTC6992-1-6992-2-6992-3-6992-4.pdf>.
- [59] C. de S. Dias and P. F. Butzen, "A novel spice model of memristive devices with threshold current based control," in *2018 31st Symposium on Integrated Circuits and Systems Design (SBCCI)*, IEEE, Aug. 2018, pp. 1–6, ISBN: 9781538674314. DOI: [10.1109/SBCCI.2018.8533256](https://doi.org/10.1109/SBCCI.2018.8533256).
- [60] F. García-Redondo. (Apr. 2017). Vlsi memristor/rram spice compact model, [Online]. Available: https://github.com/fgr1986/vlsi_memristor_compact_model. (accessed: 02.06.2025).

Appendix A

SPICE Subcircuit Codes

This appendix presents the SPICE subcircuit descriptions and behavioural models used throughout the simulation and validation phases of this work. These models, written in standard SPICE syntax, represent memristive devices and were designed to capture their dynamic resistance switching behaviour under various input stimuli.

Listing A.1: HP memristor code (SPICE subcircuit) [55]

```
1      * HP Memristor SPICE Model
2      * For Transient Analysis only
3      * created by Zdenek and Dalibor Biolek
4      *
5      * Ron, Roff - Resistance in ON / OFF States
6      * Rinit - Resistance at T=0
7      * D - Width of the thin film
8      * uv - Migration coefficient
9      * p - Parameter of the WINDOW-function
10     * for modeling nonlinear boundary conditions
11     * x - W/D Ratio, W is the actual width
12     * of the doped area (from 0 to D)
13     *
14     .SUBCKT memristor Plus Minus PARAMS:
15     + Ron=1K Roff=100K Rinit=80K D=10N uv=10F p=1
16     *****
17     * DIFFERENTIAL EQUATION MODELING *
18     *****
19     Gx 0 x value={ I (Emem) *uv*Ron/D^2*f (V(x),p) }
20     Cx x 0 1 IC={ (Roff-Rinit) / (Roff-Ron) }
21     Raux x 0 1T
22     *****
23     * RESISTIVE PORT OF THE MEMRISTOR *
24     *****
25     Emem plus aux value={-I (Emem) *V(x) * (Roff-Ron) }
26     Roff aux minus {Roff}
27     *****
28     * Flux computation *
```

```

29 *****
30 Eflux flux 0 value={SDT(V(plus,minus))}
31 *****
32 *Charge computation*
33 *****
34 Echarge charge 0 value={SDT(I(Emem))}
35 *****
36 * WINDOW FUNCTIONS
37 * FOR NONLINEAR DRIFT MODELING *
38 *****
39 *proposed by Strukov
40 .func f(x,p)={x-x*2}
41 *proposed by Joglekar
42 ;.func f(x,p)={1-(2*x-1)**(2*p)}
43 *proposed by Biolek
44 ;.func f(x,i)={1-(x-stp(-i))**(2*p)}
45 *proposed by Prodromakis
46 ;.func f(x,p)={1-(((x-0.5)**2)+0.75)**p}
47
48 .ENDS HP_Model

```

Listing A.2: Simmons memristor code (SPICE subcircuit) [50]

```

1 .SUBCKT simmons_model plus minus PARAMS:
2 + phio=0.95 Lm=0.0998 w1=0.1261 foff=3.5e-6
3 + ioff=115e-6 aoff=1.2 fon=40e-6 ion=8.9e-6
4 + aon=1.8 b=500e-6 wc=107e-3
5
6 G1 plus internal value={
7     sgn(V(x)) * (1 / V(dw))^2 * 0.0617 *
8     (V(phiI) * exp(-V(B) * V(sr)) -
9     (V(phiI) + abs(V(x))) * exp(-V(B) * V(sr2)))}
10
11 Esr sr 0 value={ sqrt(V(phiI)) }
12 Esr2 sr2 0 value={ sqrt(V(phiI) + abs(V(x))) }
13 Rs internal minus 215
14
15 Eg x 0 value = {V(plus) - V(internal)}
16 Elamda Lmda 0 value = {Lm / V(w)}
17
18 Ew2 w2 0 value={w1 + V(w) - (0.9183/(2.85 + 4 * V(Lmda) - 2 * abs(V(x))))}
19
20 EDw dw 0 value = {V(w2) - w1}
21 EB B 0 value = {10.246 * V(dw)}
22
23 ER R 0 value={ (V(w2) / w1) * (V(w) - w1) / (V(w) - V(w2)) }
24
25 EphI phiI 0 value={phio - abs(V(x)) * ((w1 + V(w2)) / (2 * V(w))) -
26     1.15 * V(Lmda) * V(w) * log(V(R)) / V(dw)}
27

```

```

28      C1 w 0 1e-9 IC = 1.2
29      R w 0 1e8MEG
30
31      Ec c 0 value={ abs(V(internal) - V(minus)) / 215 }
32
33      Emon1 mon1 0 value={{(V(w) - aoff) / wc} - (V(c) / b)}
34
35      Emon2 mon2 0 value={{aon - V(w)} / wc - (V(c) / b)}
36
37      Goff 0 w value={foff * sinh(stp(V(x)) * V(c) / ioff) *
38                      exp(-exp(V(mon1)) - V(w) / wc)}
39
40      Gon w 0 value={fon * sinh(stp(-V(x)) * V(c) / ion) *
41                      exp(-exp(V(mon2)) - V(w) / wc)}
42
43      .ENDS simmons_model

```

Listing A.3: Vourkas memristor code (SPICE subcircuit) [53]

```

1      * Voltage-controlled memristor Simulation Program with Integrated Circuit
      Emphasis model netlists *
2      *****
3      * rmin, rmax : Boundary values for r *
4      * rinit      : Initial vaue of f (Resistance at T=0)*
5      * Lo         : Tunnel barrier width *
6      * VtL, VtR   : Threshold voltages *
7      * alpha,     *
8      * beta, gamma: Parameters for modeling nonlinear *
9      *             threshold-based behaviour *
10     * m, fo       : Model's fitting parameters *
11     * yo          : Smoothing function's parameter *
12     *****
13     *Netlist corresponding to schematic of Fig. 1a
14     .SUBCKT vourkas_model plus minus PARAMS:
15     * Parameters' values
16     + rmin=100 rmax=390 rinit=390 alpha=1E6 beta=10 gamma=0.1 VtR=1.5 VtL=-1.5 yo
      =0.0001
17     + m=82 fo=310 Lo=5
18
19     * Governing equation for memristance change
20     Gr 0 r value={dr_dt(V(plus)-V(minus)) * (st_f(V(plus)-V(minus)) * st_f(V(r)-
      rmin) + st_f(-(V(plus)-V(minus))) * st_f(rmax-V(r)))}
21
22     * Capacitor to store memristance value
23     Cr r 0 1 IC={rinit}
24
25     * Auxiliary high-value resistor
26     Raux r 0 1E12
27
28     * Current equation: Imem = V / R(L)

```

```

29  Gpm plus minus value={ (V(plus)-V(minus)) / ((fo * exp(2*L(V(r)))) / L(V(r))) }
30
31  * Function for non-linear threshold-based behavior
32  .func dr_dt(y)={-alpha * ((y - VtL) / (gamma + abs(y - VtL))) * st_f(-y + VtL)
    - beta * y * st_f(y - VtL) * st_f(-y + VtR) - alpha * ((y - VtR) / (gamma +
    abs(y - VtR))) * st_f(y - VtR)}
33
34  * Smoothing function
35  .func st_f(y)={1 / (exp(-y / yo) + 1)}
36
37  * L(V) function
38  .func L(y)={Lo - Lo * m / y}
39
40  .ENDS yourkas_model

```

Listing A.4: Threshold current-based control memristor code (SPICE subcircuit) [59]

```

1  * A Novel SPICE Model of Memristive Devices with Threshold Current Based
    Control *
2
3  .subckt current_Th_memristor plus minus PARAMS: Ron=4K Roff=80K Rinit=80K alpha
    =0 beta=3E13 C1=0.2 It=10u
4
5  Bx 0 x I= {if((Im( ) > 0) & (V(x) < Roff), f1(Im( )), if((Im( ) < 0) & (V(x) >
    Ron), f2(Im( )), 0))} ;removed ternary operator, since ltspice does not
    support it
6  Rmem plus minus r={V(x)}
7  Cx x 0 1 IC={Rinit}
8
9  .func Im( ) = { (V(plus,minus)/V(x)) }
10 .func f1(y) = { ((Roff-V(x))/Roff) + C1)*beta*y + (((Roff-V(x))/Roff) + C1)
    *0.5*(alpha-beta)*(abs(y+It)-abs(y-It)) }
11 .func f2(y) = { ((V(x)-Ron)/Roff) + C1)*beta*y + (((V(x)-Ron)/Roff) + C1)
    *0.5*(alpha-beta)*(abs(y+It)-abs(y-It)) }
12
13 .ends current_Th_memristor

```

Listing A.5: VLSI unipolar NiHfO₂Si model (SPICE subcircuit) [54], [60]

```

1  *****
2  ** VLSI unipolar_NiHfO2Si model
3  *****
4
5  *****
6  ** v1.1, 17/05/2016
7  *****
8  ** Author: Fernando Garcia-Redondo
9  ** fgarcia@die.upm.es, fernandeando.com
10 ** Technical University of Madrid
11 **

```

```

12  ** https://github.com/fgr1986/vlsi_memristor_compact_model
13  ** http://vlsi.die.upm.es/memristor_spice_model
14  ****
15
16  ****
17  ** License:
18  ** Copyright of the model is maintained by the developers,
19  ** and the model is distributed under a Dual-License mode.
20  ** 1) GPL License apply for academic purposes.
21  ** If you use this model in your work, you are requested to cite [1] in the
    reference.
22  ** GitHub Repository and Downloads
23  ** 2) Commercial license for other purposes not meeting GPL license: Contact *
    fgarcia@die.upm.es*
24  ** Full License: LICENSE.txt
25  **
26  ** [1] SPICE Compact Modeling of Bipolar/Unipolar Memristor Switching Governed
    by Electrical Thresholds
27  ** Fernando Garcia-Redondo et. al.
28  ** IEEE Transactions on Circuits and Systems--I: Regular Papers
29  ** 2016, DOI: 10.1109/TCSI.2016.2564703
30  ****
31
32  ****
33  ** How to
34  ** 1) Select the corresponding model
35  ** 2) Select the input depending on the desired model
36  ** 3) Run with LTSpice (see test_bench additional files)
37  ****
38
39  ** Ideal diode reference
40  ** .INC ./idealDiode.sub
41
42  ** Ideal diode subcircuit
43  ** .SUBCKT idealDiode p n PARAMS:
44  **   +d_is=1.8e-5 d_n=1.22
45  ** G_d p n value={d_is*( exp( v(p, n)/d_n ) -1)}
46  ** .ENDS idealDiode
47
48  .SUBCKT unipolar_memristor Plus Minus PARAMS:
49      ** [A]
50      + cI=1e-2
51      ** conduction parameters:
52      ** resistance and diode
53      + r_off=3.3e6 d_is_off=5e-9 d_n_off=0.29
54      + r_on=8e2 d_is_on=18e-6 d_n_on=0.38
55      ** energy threshold parameters
56      + p_th_set=1.35e-6 p_th_reset=1e-3 p_cicle_th=p_th_set+p_th_reset
57      + p=4

```

```

58      ** internal params
59      + v_off=0 v_on=1e-7
60
61      ** following voltage source
62      E_copy v_copy 0 value={V(Plus, Minus)}
63
64      ** power computation
65      E_total_energy te 0 value={idt(I(G_cond)*V(Plus, Minus),0)}
66
67      .ic V(st)=p_th_set;
68      .ic V(rt)=p_th_reset;
69      ** Threshold Monitors
70      E_set_th st 0 value={floor( V(te)/p_cycle_th ) * p_cycle_th + p_th_set}
71      E_reset_th rt 0 value={ceil( V(te)/p_cycle_th ) * p_cycle_th}
72      R_set st 0 r=1k
73      R_reset rt 0 r=1k
74
75      ** E_state=0 -> off state; E_state=1 -> on state
76      .ic V(s)=v_on
77      E_state s 0 value={ IF(V(s)<v_on, IF( V(te)>=floor( V(te)/p_cycle_th ) *
78          p_cycle_th + p_th_set, v_on, v_off ), IF( V(te)>=V(rt), v_off, v_on ) ) }
79      R_state s 0 r=1k
80
81      ** cycle count
82      .ic V(cycle)=0;
83      .ic V(sEvent)=0;
84      E_cycle cycle 0 value={floor( V(te)/p_cycle_th ) }
85      E_sEvent sEvent 0 value={2*V(cycle) + 1*( V(te)-V(cycle)*p_cycle_th ) >
86          p_th_set ) }
87      R_cycle cycle 0 r=1k
88      R_event sEvent 0 r=1k
89
90      ** conduction
91      ** on modeling
92      ** d_off v_copy aux_off idealDiode is=d_is_on n=d_n_off
93      G_off v_copy aux_off value={d_is_off*( exp( v(v_copy, aux_off)/d_n_off ) -1)
94          }
95      Roff aux_off 0 r=r_off
96
97      ** off modeling
98      ** d_on v_copy aux_on idealDiode is=d_is_on n=d_n_on
99      G_on v_copy aux_on value={d_is_on*( exp( v(v_copy, aux_on)/d_n_on ) -1)}
100      Ron aux_on 0 r=r_on
101
102      ** hard switch with complain current
103      G_cond Plus Minus value={max( -cI, min(cI, IF(V(s)==v_off, i(Roff), i(Ron)) )
104          ) }
105
106      .ENDS unipolar_memristor

```

Appendix B

SMU Scripts

The scripts implementing the source measurement unit are reported here in the following appendix. These scripts provide automation for the source and measurement settings, ensuring accurate and efficient measurements. They complement the experimental set-up, enabling real-time data collection and analysis during the testing phases.

This Python script is designed to control a Keysight B2902 Source/Measure Unit (SMU) (or a similar Keysight instrument that uses the SCPI command set over VISA) to perform electrical measurements on a device, specifically focusing on applying a pulse train of current and measuring the resulting voltage. It then processes, saves, and plots the collected data. A similar one was already existing, that applies a pulse train of voltage and measure the resulting current, which is not included here.

Listing B.1: SET Pulse Sequence

```
1
2 #####
3 # (C) Keysight Technologies 2016
4 #
5 # You have a royalty-free right to use, modify, reproduce and distribute
6 # the Sample Application Files (and/or any modified version) in any way
7 # you find useful, provided that you agree that Keysight Technologies has
8 # no warranty, obligations or liability for any Sample Application Files.
9 #
10 # Modifications by Carina Silva, 2025
11 #####
12 from matplotlib.pyplot import plot, subplot, show, legend, xlabel, ylabel
13 import pyvisa as visa
14 import os
15 import csv
16 import numpy as np
17 import sys
18
19 # Set Sweep Style
```

```

20 DC = False
21 SWEEP = False # if double sweep repeat = 2
22 PULSE = False
23 LIST = True
24
25 # Set Measurement
26 VOLT = True # new flag created for measurement settings (in this case we
    want to measure the voltage, given a previously applied current)
27 CURR = False
28 RES = False
29
30 # List settings for Pulse Period - Current (values for current pulses will
    be stored in ValueList)
31 Ts = 1e-3 # sampling frequency
32 Tw = 1e-2 # pulsewidth (on time in 10 mili second)
33 Tp = 2e-2 # period (Off time in 10 mili second)
34 RAmp = 2e-6 # read amplitude
35 SAmp = 0.0 # start amplitude
36 WAmp = 5e-3 # write amplitude max
37 step = 0.2e-3 # current step
38 Off = 0.0 # Off current
39 N = 1000
40
41 if LIST:
42     # Generate ValueList
43     NH = Tw / Ts # Number of samples on high
44     NL = (Tp - Tw) / Ts # Number of samples on low
45     List = []
46     for amp in np.arange(SAmp, WAmp, step): # loop High from "SAmp" to "
        WAmp" with a step of "step"
47         InHigh = [amp for i in range(int(NH))] # List of NH values at high
48         InLow = [Off for i in range(int(NL))] # List of NL values at low
49         InRead = [RAmp for i in range(int(NL))] # List of NL values at
            read voltage
50         # Make List of Read + Low + High + Low
51         List.extend(InRead)
52         List.extend(InLow)
53         List.extend(InHigh)
54         List.extend(InLow)
55         N = len(InHigh) # Number of points of single period
56         ValueList = f'{List}'
57         ValueList = ValueList[1:-1]
58
59 Repeat = np.arange(SAmp, WAmp, step).size * 4 # number of periods -> *4
    because (Read + Low + High + Low)

```

```
60
61 PATH = os.getcwd()
62
63 # Change VISA_ADDRESS to a serial VISA address, e.g. 'ASRL2::INSTR'
64 VISA_ADDRESS = 'USB0::0x0957::0xCE18::MY51145218::0::INSTR'
65 filename = f'{PATH}/PulseTrain_SET{sys.argv[1]}.csv'
66
67 try:
68     # Create a connection (session) to the serial instrument
69     resourceManager = visa.ResourceManager()
70     session = resourceManager.open_resource(VISA_ADDRESS)
71     session.timeout = 250000
72
73     # For Serial and TCP/IP socket connections enable the read Termination
74     # Character, or read's will timeout
75     if session.resource_name.startswith('ASRL') or session.resource_name.
76         endsuffix('SOCKET'):
77         session.read_termination = '\n'
78
79     # If you've setup the serial port settings in Connection Expert, you
80     # can remove this section.
81     # Otherwise, set your connection parameters
82     # session.set_visa_attribute(visa.constants.VI_ATTR_ASRL_BAUD, 9600)
83     # session.set_visa_attribute(visa.constants.VI_ATTR_ASRL_DATA_BITS, 8)
84     # session.set_visa_attribute(visa.constants.VI_ATTR_ASRL_PARITY, visa.
85     # constants.VI_ASRL_PAR_NONE)
86     # session.set_visa_attribute(visa.constants.VI_ATTR_ASRL_FLOW_CNTRL,
87     # visa.constants.VI_ASRL_FLOW_DTR_DSR)
88
89     # Send the *IDN? and read the response
90     session.write('*IDN?')
91     idn = session.read()
92
93     # Reset B2902
94     session.write("*RST")
95     # Disable Output Before Source Edit
96     session.write(":OUTP:ON:AUTO OFF")
97     session.write(":OUTP OFF")
98     # Set Source Off to Zero
99     session.write(":OUTP:OFF:MODE ZERO")
100
101     # Source Settings
102     session.write(":SOUR:FUNC:MODE CURR") # Set Source to Curr
103     # session.write(":SENS:CURR:PROT 5") # Set Protection Voltage Limit
104     session.write(":SOUR:CURR:RANG:AUTO ON") # Set Fixed Current Range
```

```

100 session.write(":SOUR:CURRE:RANG 0.010") # 10mA Fixed Range
101
102 if DC:
103     session.write(":SOUR:VOLT 1.0") # Set DC Voltage
104 elif PULSE: # Can Be Set with Sweep
105     session.write(":SOUR:FUNC:SHAP PULS") # Set Shape to Pulse
106     session.write(":SOUR:PULS:DEL 5e-4") # Delay time 0 ms
107     session.write(":SOUR:PULS:WIDT 1E-2") # Pulse width 2 ms
108     session.write(":SOUR:VOLT 0.0") # Base 0.1 V
109     session.write(":SOUR:VOLT:TRIG 0.1") # Peak 1 V
110 elif SWEEP:
111     session.write(":SOUR:VOLT:MODE SWE")
112     session.write(":SOUR:SWE:STA DOUB")
113     session.write(":SOUR:VOLT:STAR -1") # Start Voltage
114     session.write(":SOUR:VOLT:STOP 1") # Stop Voltage
115     session.write(f":SOUR:VOLT:POIN {N}") # Number of Sweep Points
116 elif LIST: # We're currently using this: LIST=True
117     session.write(":SOUR:CURRE:MODE LIST")
118     session.write(f":SOUR:LIST:CURRE {ValueList}")
119
120 # Measurement settings
121 if VOLT:
122     session.write(":SENS:FUNC \"VOLT\"")
123     session.write(":SENS:VOLT:RANG:AUTO ON") # Fixed Voltage Range
124     # session.write(":SENS:VOLT:RANG 0.1") # Max Voltage
125     session.write(":SENS:VOLT:PROT 20") # Overvoltage Protection
126     COMPLIANCE in Volt
127 elif CURR:
128     session.write(":SENS:FUNC \"CURR\"")
129     session.write(":SENS:CURRE:RANG:AUTO ON") # Fixed Current Range
130     session.write(":SENS:CURRE:RANG 0.1") # Max Current
131     session.write(":SENS:CURRE:PROT 0.0020") # Overcurrent Protection
132     COMPLIANCE in Ampere (5mA=0.005 @20V)
133     # session.write(":SENS:CURRE:APER 1e-2") # Aperture
134 elif RES:
135     session.write(":SENS:FUNC \"RES\"")
136     session.write(":SENS:RES:MODE AUTO")
137     session.write(":SENS:RES:RANG:AUTO:LLIM 20")
138     session.write(":SENS:RES:RANG:AUTO:ULIM 2E4")
139
140 # Trigger Settings
141 session.write(":TRIG:SOUR TIM")
142 session.write(f":TRIG:TIM {Ts}")
143 if PULSE:
144     session.write(f":TRIG:COUN {Repeat}")

```

```

143     else:
144         session.write(f":TRIG:COUN {N * Repeat}")
145
146     session.write(":TRIG:TRAN:DEL 1e-3")
147     session.write(":TRIG:TRAN:DEL 0.5e-5")
148
149     # Output Filter
150     session.write(":OUTP:FILT OFF")
151     session.write(":OUTP:FILT:AUTO OFF")
152     session.write(":OUTP:FILT:FREQ 1E+5") # 10 kHz
153
154     session.write(":SENS:REM OFF") # Set 4-wire Connection
155
156     # Output On
157     session.write(':OUTP ON')
158     session.write(':INIT (@1)')
159
160     session.write(":OUTP OFF")
161     if VOLT:
162         session.write(":FETC:ARR:VOLT? (@1)")
163         VResultString = session.read()
164     if CURR:
165         session.write(":FETC:ARR:CURR? (@1)")
166         ResultString = session.read()
167     if RES:
168         session.write(":FETC:ARR:RES? (@1)")
169         ResultString = session.read()
170
171     session.write(":FETC:ARR:CURR? (@1)")
172     ResultString = session.read()
173     session.write(":FETC:ARR:TIME? (@1)")
174     TimeString = session.read()
175     Current = [float(s) for s in ResultString.split(',')]
176     Voltage = [float(s) for s in VResultString.split(',')]
177     Time = [float(s) for s in TimeString.split(',')]
178     Resistance = np.asarray(Voltage) / np.asarray(Current)
179
180     # Save Sweep in csv File
181     with open(filename, mode='w') as SaveFile:
182         SaveFile = csv.writer(SaveFile, delimiter=',', quotechar='"',
183                               quoting=csv.QUOTE_MINIMAL)
184         SaveFile.writerow(Time)
185         SaveFile.writerow(Voltage)
186         SaveFile.writerow(Current)

```

```

187     subplot(3,1,1)
188     plot(Voltage, Current)
189     xlabel('Voltage (V)')
190     ylabel('Current (A)')
191     ax1 = subplot(3,1,2)
192     ax1.plot(Time, Current, linewidth=3)
193     ax2 = ax1.twinx()
194     ax2.plot(Time, Voltage, '--r')
195     ax1.set_xlabel('Time (s)')
196     ax1.set_ylabel('Current (A)')
197     ax2.set_ylabel('Voltage (V)')
198     ax3 = subplot(3,1,3)
199     ax3.plot(Time, Resistance)
200     ax3.set_ylabel('Resistance (Ohm)')
201     ax3.set_xlabel('Time (s)')
202     show()
203
204     session.write('')
205
206     # Close the connection to the instrument
207     session.close()
208     resourceManager.close()
209
210     except visa.Error as ex:
211         print('An error occurred: %s' % ex)
212
213     print('Done.')

```

Listing B.2: Sweep Sequence

```

1
2 #####
3 # (C) Keysight Technologies 2016
4 #
5 # You have a royalty-free right to use, modify, reproduce and distribute
6 # the Sample Application Files (and/or any modified version) in any way
7 # you find useful, provided that you agree that Keysight Technologies has
8 # no
9 # warranty, obligations or liability for any Sample Application Files.
10 #
11 # Modifications by Carina Silva, 2025
12 #####
13 from matplotlib.pyplot import plot, subplot, show, legend, xlabel, ylabel
14 import pyvisa as visa
15 import os
16 import csv

```

```
16 import numpy as np
17
18 # Set Sweep Style
19 DC = False
20 SWEEP = True # if double sweep repeat = 2
21 PULSE = False
22 LIST = False
23
24 # Set Measurement
25 CURR = True
26 RES = False
27
28 # List settings for Pulse Period
29 Ts = 1e-3 # sampling frequency 10e-3
30 Tw = 1e-2 # pulsewidth (time)
31 Tp = 5e-2 # period
32 Amp = 0.7 # amplitude
33 Off = 0.0 # rest voltage
34 Repeat = 2 # number of periods
35 N = 500
36
37 if LIST:
38     # Generate ValueList
39     NH = Tw / Ts
40     NL = (Tp - Tw) / Ts
41     InHigh = [Amp for i in range(int(NH))]
42     InLow = [Off for i in range(int(NL))]
43     InHigh.extend(InLow)
44     N = len(InHigh) # Number of points of single period
45     ValueList = f'{InHigh}'
46     ValueList = ValueList[1:-1]
47
48 PATH = os.getcwd()
49
50 # Change VISA_ADDRESS to a serial VISA address, e.g. 'ASRL2::INSTR'
51 VISA_ADDRESS = 'USB0::0x0957::0xCE18::MY51145218::0::INSTR'
52 filename = f'{PATH}/MemOnSweep.csv'
53
54 try:
55     # Create a connection (session) to the serial instrument
56     resourceManager = visa.ResourceManager()
57     session = resourceManager.open_resource(VISA_ADDRESS)
58     session.timeout = 100000
59
```

```

60     # For Serial and TCP/IP socket connections enable the read Termination
        Character, or read's will timeout
61     if session.resource_name.startswith('ASRL') or session.resource_name.
        endsWith('SOCKET'):
62         session.read_termination = '\n'
63
64     # Send the *IDN? and read the response
65     session.write('*IDN?')
66     idn = session.read()
67
68     # Reset B2902
69     session.write("*RST")
70     # Disable Output Before Source Edit
71     session.write(":OUTP:ON:AUTO OFF")
72     session.write(":OUTP OFF")
73     # Set Source Off to Zero
74     session.write(":OUTP:OFF:MODE ZERO")
75
76     # Source Settings
77     # session.write(":SOUR:FUNC:MODE VOLT") # Set Source to Volt
78     # session.write(":SENS:VOLT:PROT 5") # Set Protection Voltage Limit
79     # session.write(":SOUR:VOLT:RANG:AUTO ON") # Set Fixed Voltage Range
80     # session.write(":SOUR:VOLT:RANG 10") # 2V Fixed Range
81
82     session.write(":SOUR:FUNC:MODE CURR") # Set Source to Current
83     session.write(":SOUR:CURR:RANG:AUTO ON")
84     # session.write(":SOUR:CURR:RANG 10E-3") # Fixed Range
85
86     if DC:
87         session.write(":SOUR:VOLT 1") # Set DC Voltage
88     elif PULSE: # Can Be Set with Sweep
89         session.write(":SOUR:FUNC:SHAP PULS") # Set Shape to Pulse
90         session.write(":SOUR:PULS:DEL 5E-4") # Delay time 0 ms
91         session.write(":SOUR:PULS:WIDT 1E-2") # Pulse width 2 ms
92         session.write(":SOUR:VOLT 0.0") # Base 0.1 V
93         session.write(":SOUR:VOLT:TRIG 0.1") # Peak 1 V
94     elif SWEEP:
95         session.write(":SOUR:CURR:MODE SWE")
96         #session.write(":SOUR:SWE:TYPE LIN")
97         session.write(":SOUR:SWE:STA DOUB")
98         session.write(":SOUR:CURR:STAR 1E-3") # Start Current
99         session.write(":SOUR:CURR:STOP 5E-3") # Stop Current
100        session.write(f":SOUR:CURR:POIN {N}") # Number of Sweep Points
101        # session.write(":SENS:CURR:NPLC ?") # Measurement Speed
102    elif LIST:

```

```

103     session.write(":SOUR:VOLT:MODE LIST")
104     session.write(f":SOUR:LIST:VOLT {ValueList}")
105
106     # Measurement settings
107     if CURR:
108         session.write(":SENS:FUNC \"VOLT\"")
109         session.write(":SENS:VOLT:RANG:AUTO ON") # Fixed voltage Range
110         session.write(":SENS:VOLT:RANG 20") # Max Voltage
111         session.write(":SENS:VOLT:PROT 20") # Overvoltage Protection
112         # session.write(":SENS:CURR:APER 1e-2") # Aperture
113     elif RES:
114         session.write(":SENS:FUNC \"RES\"")
115         session.write(":SENS:RES:MODE AUTO")
116         session.write(":SENS:RES:RANG:AUTO:LLIM 20")
117         session.write(":SENS:RES:RANG:AUTO:ULIM 2E4")
118
119     # Trigger Settings
120     session.write(":TRIG:SOUR TIM")
121     session.write(f":TRIG:TIM {Ts}")
122     if PULSE:
123         session.write(f":TRIG:COUN {Repeat}")
124     else:
125         session.write(f":TRIG:COUN {N * Repeat}")
126
127     session.write(":TRIG:TRAN:DEL 1e-3")
128     session.write(":TRIG:TRAN:DEL 0.5e-5")
129
130     # Output Filter
131     session.write(":OUTP:FILT ON")
132     session.write(":OUTP:FILT:AUTO OFF")
133     session.write(":OUTP:FILT:FREQ 1E+5") # 10 kHz
134
135     session.write(":SENS:REM OFF") # Set 4-wire Connection
136
137     # Output On
138     session.write(':OUTP ON')
139     session.write(':INIT (@1)')
140
141     session.write(":OUTP OFF")
142     if CURR:
143         session.write(":FETC:ARR:CURR? (@1)")
144         ResultString = session.read()
145     if RES:
146         session.write(":FETC:ARR:RES? (@1)")
147         ResultString = session.read()

```

```

148 session.write(":FETC:ARR:VOLT? (@1)")
149 VResultString = session.read()
150 session.write(":FETC:ARR:TIME? (@1)")
151 TimeString = session.read()
152 Current = [float(s) for s in ResultString.split(',')]
153 Voltage = [float(s) for s in VResultString.split(',')]
154 Time = [float(s) for s in TimeString.split(',')]
155 Resistance = np.asarray(Voltage) / np.asarray(Current)
156
157 # Save Sweep in csv File
158 with open(filename, mode='w') as SaveFile:
159     SaveFile = csv.writer(SaveFile, delimiter=',', quotechar='"',
160                           quoting=csv.QUOTE_MINIMAL)
161     SaveFile.writerow(Time)
162     SaveFile.writerow(Current)
163     SaveFile.writerow(Voltage)
164
165 subplot(3,1,1)
166 plot(Voltage, Current)
167 xlabel('Voltage (V)')
168 ylabel('Current (A)')
169 ax1 = subplot(3,1,2)
170 ax1.plot(Time, Voltage, linewidth=3)
171 ax2 = ax1.twinx()
172 ax2.plot(Time, Current, '--r')
173 ax1.set_xlabel('Time (s)')
174 ax1.set_ylabel('Voltage (V)')
175 ax2.set_ylabel('Current (A)')
176 ax3 = subplot(3,1,3)
177 ax3.plot(Time, Resistance)
178 ax3.set_ylabel('Resistance (Ohm)')
179 ax3.set_xlabel('Time (s)')
180 show()
181
182 session.write('')
183
184 # Close the connection to the instrument
185 session.close()
186 resourceManager.close()
187
188 except visa.Error as ex:
189     print('An error occurred: %s' % ex)
190
191 print('Done.')

```

Appendix C

Characterisation Measurements and Specifications

Table C.1: Electrical characterisation results of device no. 1.

3 rd Quadrant	Iteration no.	ON Resistance (LRS)	OFF Resistance (HRS)
Device 1	1	51 Ω	150k Ω
	2	26 Ω	100 Ω to 26 Ω
	3	Remained in LRS state	Remained in LRS state
	4	-	-
	5	-	-

Table C.2: Electrical characterisation results of device no. 2.

3 rd Quadrant	Iteration no.	ON Resistance (LRS)	OFF Resistance (HRS)
Device 2	1	108 Ω	70k Ω
	2	16 Ω	$\approx$ 10 Ω
	3	Remained in LRS state	Remained in LRS state
	4	-	-
	5	-	-

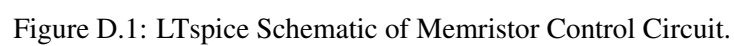
Table C.3: Keysight B2902A Source and Measurement Specifications.

Specification	Range	Resolution	Accuracy (% reading + offset)	Noise
Voltage Sourcing				
Accuracy	± 200 mV	1 μ V	0.015% + 225 μ V	≤ 10 μ V
	± 2 V	10 μ V	0.02% + 350 μ V	≤ 20 μ V
	± 20 V	100 μ V	0.015% + 5 mV	≤ 200 μ V
	± 200 V	1 mV	0.015% + 50 mV	≤ 2 mV
Current Sourcing				
Accuracy	± 100 nA	1 pA	0.06% + 100 pA	≤ 2 pA
	± 1 μ A	10 pA	0.025% + 500 pA	≤ 25 pA
	± 10 μ A	100 pA	0.025% + 1.5 nA	≤ 60 pA
	± 100 μ A	1 nA	0.02% + 25 nA	≤ 2 nA
	± 1 mA	10 nA	0.02% + 200 nA	≤ 6 nA
	± 10 mA	100 nA	0.02% + 2.5 μ A	≤ 200 nA
	± 100 mA	1 μ A	0.02% + 20 μ A	≤ 600 nA
	± 1 A	10 μ A	0.03% + 1.5 mA	≤ 70 μ A
	± 1.5 A	10 μ A	0.05% + 3.5 mA	≤ 100 μ A
	± 3 A	100 μ A	0.4% + 7 mA	≤ 120 μ A
Voltage Measurement				
Accuracy	± 200 mV	100 nV	0.015% + 225 μ V	—
	± 2 V	1 μ V	0.02% + 350 μ V	—
	± 20 V	10 μ V	0.015% + 5 mV	—
	± 200 V	100 μ V	0.015% + 50 mV	—
Current Measurement				
Accuracy	± 100 nA	100 fA	0.06% + 100 pA	—
	± 1 μ A	1 pA	0.025% + 500 pA	—
	± 10 μ A	10 pA	0.025% + 1.5 nA	—
	± 100 μ A	100 pA	0.02% + 25 nA	—
	± 1 mA	1 nA	0.02% + 200 nA	—
	± 10 mA	10 nA	0.02% + 2.5 μ A	—
	± 100 mA	100 nA	0.02% + 20 μ A	—
	± 1 A	1 μ A	0.03% + 1.5 mA	—
	± 1.5 A	1 μ A	0.05% + 3.5 mA	—
	± 3 A	10 μ A	0.4% + 7 mA	—

Appendix D

LTspice Implementation

This appendix provides the LTspice full implementation of the memristor control circuit designed in Chapter 3. The schematic includes all components and connections necessary to simulate the SET and RESET operations of the memristor, as well as the measurement and feedback mechanisms.



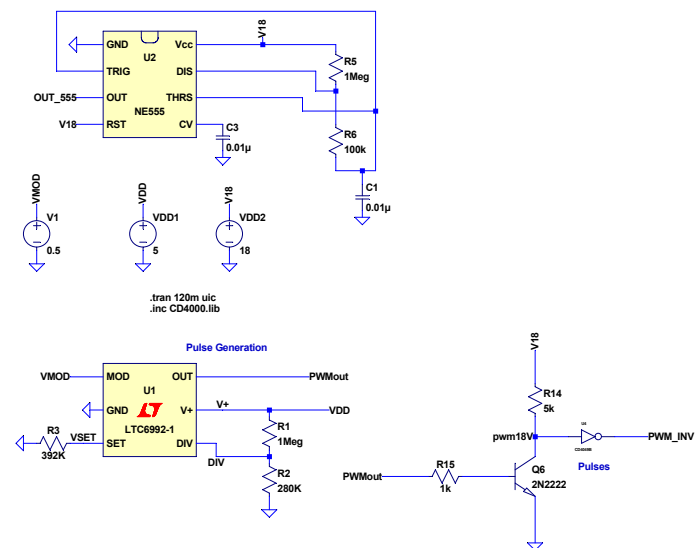


Figure D.2: LTspice Schematic of Pulse Generation Components.