FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO

Characterization and optimization of warpage in the semiconductor fan-out wafer-level packaging technology

Beatriz Quezada Mariz Ferreira

Masters in Mechanical Engineering

Supervisor: Professor Doutor José Ferreira Duarte

Supervisor at Amkor Technology Portugal: Eng. Filipa Oliveira

July 22, 2024

Characterization and optimization of warpage in the semiconductor fan-out wafer-level packaging technology

Beatriz Quezada Mariz Ferreira

Masters in Mechanical Engineering

July 22, 2024

Resumo

A constante evolução dos dispositivos tecnológicos, aliada à sua continua miniaturização, tem estimulado as empresas de tecnologia de ponta a adotarem processos de fabrico capazes de lidar com novas exigências e requisitos.

Na indústria de fabrico de semicondutores, estas novas exigências decorrem, precipuamente, do aumento gradual do diâmetro do substrato para a produção dos mesmos, as *wafers*, ao passo que, inversamente, a sua espessura tem vindo continuamente a diminuir. Destas alterações substanciais, surgidas para melhorar a rentabilidade das *wafers* e a utilização de material, advêm novos desafios, nomeadamente o aparecimento de empeno (*warpage*) nas mesmas.

Este desafio, que pode ser sucintamente definido como a diferença entre as distâncias mínima e máxima da *wafer* em relação a um plano de referência, resulta principalmente das diferentes gamas de temperatura, que surgem nas fases do processo de fabrico (*packaging*) de semicondutores, coligadas com os diferentes coeficientes de expansão térmica dos materiais adjacentes presentes na *wafer*.

Estas *wafers*, com *warpage*, terão um impacto adverso não só nas diferentes fases do fluxo produtivo, mas também no próprio transporte e manuseamento das mesmas. Além disso, *wafers* com um elevado grau de *warpage* podem partir, resultando num desperdício de material e consequente menor eficiência na utilização da matéria-prima.

Assim, a deteção precoce deste desafio e a garantia que, ao longo do processo, o *warpage* se encontra dentro de limites aceitáveis, tornam-se essenciais para minimizar o custo e o tempo total do ciclo de produção, além de assegurar a fiabilidade do produto final.

Esta dissertação de mestrado, desenvolvida num dos maiores fabricantes mundiais de *packaging* de semicondutores, a Amkor Technology, teve como principal objetivo a análise do comportamento de várias *wafers* ao longo de várias fases do processo produtivo, de forma a caraterizar e otimizar o *warpage* de uma forma abrangente.

Este estudo envolverá a exploração do impacto de parâmetros variáveis do processo nos níveis de *warpage*, aplicando simultaneamente técnicas corretivas para os minimizar, conforme necessário. Adicionalmente, será também estudada a influência das camadas poliméricas individuais adicionadas progressivamente ao longo do processo nesse mesmo aspeto.

Sugere-se que, para estudos futuros, seja incluído uma caraterização mais completa dos ensaios experimentais, uma utilização de diferentes componentes de fabrico aquando do processo de produção, uma análise do impacto de distintas técnicas de correção de *warpage* durante o mesmo passo do processo produtivo e por último, um estudo dos intervalos de tempo entre a utilização de uma determinada técnica corretiva e o momento em que a mesma deixa de ser eficaz.

Palavras-Chave: Empeno; Tecnologia de packaging eWLB; Packaging de Semicondutores; Wafer

Abstract

The constant evolution of technological devices, allied with their continuous miniaturization, has urged cutting-edge technology companies to adopt manufacturing processes capable of handling novel demands and requirements.

In the semiconductor manufacturing industry, these new requirements stem primarily from the gradual increase in the diameter of the substrate for their production, the wafers, while conversely, their thickness has been continuously decreasing. From these substantial changes, which have emerged to improve the profitability of wafers and the use of its material, originate new challenges, namely the appearance of warpage on them.

This challenge, which can be succinctly defined as the difference between the minimum and maximum distances of the wafer to a reference plane, mainly originates from the diverse range of temperatures that arise in the different stages of the semiconductor packaging process, combined with the different coefficients of thermal expansion of the adjacent materials present in the wafer.

These warped wafers will have a negative impact not only on the different phases of the packaging process flow, but also on the transportation and handling of the wafers themselves. Additionally, wafers with a high degree of warpage may fracture, resulting in material waste and consequent lower efficiency in raw material utilization.

Therefore, the early detection of warpage and the assurance that the interim warpage throughout the process is within acceptable limits, becomes essential to minimize both the cost and total time of the production cycle, while guaranteeing the reliability of the final product.

This Master's dissertation, developed at one of the world's largest manufacturer of semiconductor packaging, Amkor Technology, has as its main objective the analysis of the behaviour of several wafers across multiple stages of the packaging flow to comprehensively characterize and optimize warpage.

This study will involve the exploration of the impact of variable process parameters on warpage levels while simultaneously applying corrective techniques to minimize them, as necessary. In addition, the influence of the individual polymeric layers added progressively throughout the packaging process will also be investigated.

The suggested future studies include a more through characterization of the chosen experimental runs, the use of different manufacturing components during the production process, an analysis of the impact of different warpage correction techniques during the same step of the production process and lastly, a study of the time windows between the use of a particular correction technique and the moment when it ceases to be effective.

Keywords: Warpage; eWLB packaging technology; Semiconductor packaging; Wafer

Acknowledgments

This endeavor would not have been possible without the instrumental contributions and insights provided by numerous people at every stage of its development. Henceforth, I take this opportunity to express my sincerest appreciation to each and every one of them.

To Professor Doutor José Ferreira Duarte for his invaluable guidance, careful suggestions and insightful criticism, which were pivotal for the successful conclusion of this work with a high scientific value and content. I am deeply appreciative of his support and the considerable time dedicated to this project.

To Eng. Filipa Oliveira for her unwavering commitment and kind encouragement, demonstrated through countless hours of assistance in spite of her demanding schedule. Her consistent availability for meetings, prompt responses to all my questions and the endless phone calls made to ensure this project could be executed on schedule, were crucial for its completion. On a more personal note, her exemplary work ethic allied with her discipline and eagerness to embrace new challenges will undoubtedly always serve as a source of inspiration for both my personal and professional paths. It has truly been a great honour and an immense privilege to work with you and learn from you.

I would like to also extend my deepest gratitude to Eng. Eoin O' Toole for granting me the privilege of doing this dissertation at such a prestigious company and for all his indispensable contributions throughout this period. To Eng. Daniela Silva, Eng. António Raimundo and Eng. Bárbara Barbosa for their assiduous support and willingness to share their extensive knowledge with me. To Eng. Diana Morais for patiently teaching me all the fundamentals of this complex world. Her generosity and mentorship, played an instrumental role in my decision to return to ATEP to pursue my Master's dissertation.

Finally, I extend my heartfelt appreciation to every member of the Research and Development Team at ATEP for warmly welcoming me once again and for the unwavering support extended to me throughout these months. I am additionally grateful for all the invaluable knowledge I have gained with them, both work-related and beyond.

Beatriz Quezada

Contents

List of Figures

List of Tables

Abbreviations and Symbols

3D	Three-Dimensional
ATEP	Amkor Technology Portugal
CTE	Coefficient of Thermal Expansion
DL1	First Dielectric Layer
DL2	Second Dielectric Layer
DOE	Design of Experiments
EDA	Electronic Design Automation
EMC	Epoxy Mold Compound
eWLB	Embedded Wafer Level Ball Grid Array Packaging Technology
Tg	Glass Transition Temperature
IC	Integrated Circuit
LBS	Laser, Ball Attach, Singulation
MT	Mold Thickness
OSAT	Outsourced Semiconductor Assembly and Test
PI	Polyimide
POR_{MT}	Process of Reference for Mold Thickness Values
POR_{ST}	Process of Reference for Silicon Thickness Values
RDL	Redistribution Layer
Recon	Reconstituted
ST	Silicon Thickness
UBM	Under Bump Metallization
UV	Ultra Violet
VOR	Volume Occupation Ratio

Glossary

Back-End Manufacturing
Second major stage of the semiconductor manufacturing process that includes a group of fabrication steps, mainly of assembly, packaging and testing, performed after all the features/circuits have been created on the wafer. See packaging, semiconductor, wafer.

Blank Silicon Dies
Dies composed of a silicon substrate, directly originated from the front-end developer, without any added layers on top. See die, front-end manufacturing.

Die
Small individual block, cut out from the front-end wafer containing a functional circuit. See front-end wafer.

Dielectric Material
Electrical insulator material that does not allow any passage of flow and that can be polarized by an applied electric field, that is, by relocating its positive charges in the direction of the field while the negative charges are shifted in the opposite direction.

Electroplating
Process for creating metal coatings on a solid substrate by the deposition of a thin coherent layer of dissolved metal cations in another material by means of a direct electric current. Frequently referred to as electrochemical deposition or electrodeposition.

Embebbed Wafer Level Ball Grid Array Packaging Technology
Technology used to produce semiconductors packaging. See packaging.

Front-end Manufacturing
First major stage of the semiconductor manufacturing process that includes a group of fabrication steps to physically create, layer by layer, an electronic circuitry in a raw pure silicon wafer. See semiconductor, wafer.

Front-end Wafer
Thin slice of a semiconductor substance, usually crystalline silicon obtained from sand (silica), used as a substrate for the manufacture of semiconductors. See semiconductor.

Full Loop Wafers
Wafers, produced by the front-end manufacturer, with all the layers of material a productive material would typically encompass. See front-end manufacturing, wafer.

Functional Dies
Dies from the front-end developer with the silicon substrate and numerous other layers developed in the front-end stage. See die, front-end manufacturing.

Mold Compound
Multi-component polymer used in the semiconductors device's packaging with excellent mechanical, electrical and thermal properties. See packaging, semiconductors device.

Overmold
Difference, on the wafer, between the mold compound thickness and the silicon die thickness. See die, mold compound.

Package
Enclosure polymeric structure, obtained in the final phase of the manufacture of semiconductors, that performs as a connection between the electrical components and the external environment while simultaneously acting as a protection against any moisture exposure, mechanical threats and chemical contamination. See semiconductor.

Packaging
Group of manufacturing steps used to produce the encapsulation (package) of semiconductor. See package, semiconductor.

Photo-mask
Opaque plate, with specific transparent areas, that allows light to pass through in defined areas of a surface, while shielding the remaining areas.

Photo-resist Material
Light-sensitive polymeric material that when exposed to ultraviolet light, if positive, loses its resistance and turns into a soluble material. If negative, when exposed to ultraviolet light, turns into an insoluble material.

Reconstituted Wafer
Artificial wafer in which the silicon dies cut from the front-end wafer are embedded in a mold compound. See die, front-end wafer, mold compound.

Semiconductor
Combination of numerous interconnected electronic components on a flat surface, that rely on the properties of a semiconductor material to convert electrical signals into digital information. Commonly referred to as chips or microchips. See semiconductor material.

Semiconductor Material
Material with variable electrical conductivity that typically falls between that of an insulator and a conductor, depending on the environmental parameters.

Short Loop Wafers
Wafers, produced by the front-end manufacturer, with only a parcel of the layers a productive material would characteristically incorporate. Typically used for testing and reliability purposes. See front-end manufacturing, wafer.

Testing Dies
Dies from the front-end manufacturer especially designed to possess leakage and contact resistance testing capacities. See die, front-end manufacturing.

Chapter 1

Introduction

Semiconductors, also frequently denoted to as integrated circuits (ICs), are numerous interconnected electronic components on a flat surface, that function by converting electrical signals into digital information that will later be interpreted by various electronic equipment. (Cardoso, 2021).

These devices' production process, often seen as one of the most challenging manufacturing processes to exist, can typically be allocated into 3 major stages: design, front-end manufacturing (fabrication) and back-end manufacturing (assembly, testing and packaging). (Ramsey, 2023)

In this day and age, the industrial world strives to minimize potential delays that may end up jeopardizing the correct execution of their distinct manufacturing processes. When it comes to the semiconductors back-end manufacturers, where the semiconductors packaging production is incorporated in, one of the most common aspects that frequently culminates in process delays is the presence of warpage in the wafers (a thin slice of crystalline silicon used in the manufacture of semiconductors).

The aforementioned challenge that can be succinctly defined as the difference between the minimum and maximum distances of the wafer to a reference plane, mainly stems from the diverse temperature fluctuations used in the different steps of the semiconductors' packaging process. As there will be a mismatch in the coefficients of thermal expansion among the different adjacent materials present in the wafer, these temperature variations will induce significant thermal and mechanical stresses that will ultimately culminate in warped wafers. (Yao et al., 2016)

Most equipment available at ATEP – Amkor Technology S.A., has been designed to process wafers that are highly rigid and whose behavior is similar to that of a true elastic material, instead of the reconstituted wafers that they normally handle. Subsequently, and as the reconstituted wafers have a tendency to exhibit higher levels of warpage, the available equipment fails to appropriately handle them, which leads to the aforesaid process delays and the consequent increased production costs. (Teixeira and Ribeiro, 2012)

Furthermore, as the technological industry evolves and as electronic components tend to continue to shrink in size, wafers are becoming gradually thinner and the levels of warpage in them has been exponentially increasing. (Ng and Asundi, 2011) Ergo, addressing this issue and discovering methods to overcome it has become an unavoidable step to attain the highest possible yield

and reliability in the production of semiconductors packaging.

This dissertation's main motivation will consist on optimizing this matter, by performing a complete and comprehensive warpage characterization throughout the entirety of the semiconductors packaging flow.

1.1 Dissertation's framework

This subsequent section will provide the reader with a brief overview of the dissertation's framework, where its objectives and structure will be succinctly highlighted. In addition, a concise description of the company where the work was developed in will also be provided.

It is important to emphasise that given the industrial setting in which this dissertation was developed in, and due to some confidential characteristics, some non-essential information for the reader's comprehension will be omitted throughout it.

1.1.1 Objectives

This work, which was carried out as part of the Master's degree in Mechanical Engineering with specialisation in Materials and Technological Processes at the Faculty of Engineering of the University of Porto (Portugal), was developed over the course of 21 weeks, spanning from February to July, at ATEP - Amkor Technology, S.A..

During these weeks, an analysis of the behaviour of several wafers, of two distinct front-end manufacturers, across multiple stages of the packaging process was conducted to comprehensively characterize and optimize warpage.

This study involved exploring the impact of variable process parameters on warpage levels while simultaneously applying corrective techniques to minimize them, as required. Furthermore, in this study, the consequence on warpage of the dielectric layers progressively added throughout the packaging process was also explored.

These aforesaid goals were accomplished through an analysis of the warpage measurements, collected using different equipment, during the course of the packaging production. These measurements enabled the gathering of essential data to determine the optimal combination of some wafer characteristics and to determine which correction recipe(s) are best suited for each particular manufacturing step.

This analysis will not only improve the entire performance of the packaging process and the reliability of the final products but will also reduce the cycle time and any additional costs.

Ergo, to develop this work, a detailed plan with four distinct stages was established, each meant to achieve a specific set of targets.

This plan follows the steps outlined below.

- **Phase 1:** The first stage of this dissertation entailed becoming acquainted with the overall concept of warpage, including its measurement and correction techniques. After a proper

familiarization with the different concepts, all the necessary data and information was gathered. Moreover, methods for conducting warpage measurements directly on the production equipment were learned to expedite the experimental runs within the manufacturing process.

- **Phase 2:** The second stage involved planning the various experimental runs, each with its own set of unique wafer characteristics, as well as preparing the all necessary materials for the study.
- **Phase 3:** The third stage marked the beginning of the experimental activities. These included the execution of warpage measurements, using the different equipment, and, when necessary, the application of warpage correction techniques throughout the entirety of the packaging flow.
- **Phase 4:** The final stage entailed a through analysis of the acquired results as an attempt to identify the best combination of wafer characteristics while ascertaining the most influential parameters on warpage. Additionally, it also involved the drawing of conclusions regarding various strategies to mitigate warpage.

1.1.2 Structure

The current chapter starts with a brief introduction of the dissertation's main topics and objectives, along with a short description of the company where the dissertation was developed in.

This introductory chapter is followed by four other chapters.

In Chapter 2, a theoretical background with all the different concepts needed for the correct comprehension of this paper will be succinctly shown. Moreover, in Chapter 3, the methods and materials used, as well as all the experiments performed, will be explained and detailed. Following this chapter, in Chapter 4, the different conclusions reached will be presented, evaluated and summarized. To conclude, in Chapter 5, prospects for future work will be outlined and possible avenues for improvement will be explored. Furthermore, recommendations for mitigating warpage will be elaborated upon.

1.1.3 Introduction to the company

This Mechanical Engineering Master's dissertation was developed at Amkor Technology Portugal (ATEP), located in Vila do Conde, Portugal.

The now called ATEP has gone through several changes since its creation in 1996 under the name of Siemens Semiconductor Portugal.

Firstly, in 1999, due to an internal restructure within the Siemens group, the company was renamed to Infineon Technologies AGs. Later, in 2006, a specific division of Infineon Technologies became an independent company called Qimonda. This novel company, due to an economical crisis, ended up being dissolved and after a major restructure process, in 2010, Nanium S.A. was formed. Lastly, in 2018, Nanium S.A. was purchased in its entirety by one of the world's largest

outsourced semiconductor packaging, design, and test services groups - Amkor Technology Inc - which originated ATEP.

By leveraging over 28 years of global experience in the semiconductor industry and an in-house capability covering the entire development chain, ATEP has solidified itself as a partner of the major semiconductor companies all across Europe.

Nowadays, Amkor Technology's facilities in Portugal, depicted in Figure 1.1, count with more than 800 employees spread throughout technical and social areas of 36.900 m^2 and a clean-room area of 20.600 m^2.

(a) ATEP's facilities.

(b) ATEP's clean room.

Figure 1.1: ATEP facilities and clean room located in Vila do Conde, Portugal. (ATEP, 2024)

Chapter 2

State of the art

2.1 Semiconductors Packaging

According to Pan et al. (2024), semiconductors devices *"are the cornerstone of rapid information flow in the circular economy era and are crucial for society as a whole"*. These components, also commonly referred to as integrated circuits (ICs), can be defined as several interconnected electronic components on a flat surface, responsible for the functionality of nearly all the electronic equipment found in innumerable fields (telecommunications, healthcare, automotive, military equipment, etc.). (Saint and Saint, 2024) These components made up of various diodes, capacitors, transistors and resistors function by converting electrical signals into digital information that will later be interpreted by different equipment. (Cardoso, 2021)

The production of these components is frequently seen as one of the most challenging and demanding manufacturing processes to exist, since it can take up to 20 weeks to complete the hundreds of steps (400 - 1400) needed to produce a single integrated circuit. (Ramsey, 2023) As such, this complex manufacturing process can typically be allocated into 3 major stages: design, front-end manufacturing (fabrication) and back-end manufacturing (assembly, testing and packaging).

The first stage, design, consists on the creation of detailed design specifications dependent on the intended final functionality of the semiconductor, usually with the aid of complex Electronic Design Automation (EDA) software. Furthermore, in this step the design engineers also manufacture various photo-masks, necessary for the making of electronic circuits later in the manufacturing process. (Saint and Saint, 2024)

The second stage (front-end manufacturing - fabrication), consists on the physical creation, layer by layer, of an electronic circuitry with, typically, a raw pure silicon wafer as the starting point. At the end of this stage, the wafers (depicted in Figure 2.1) will have several dies (single ICs), that will be individually diced in the third stage. Since this is not the focus of this paper, more details about this process will not be further elaborated upon.

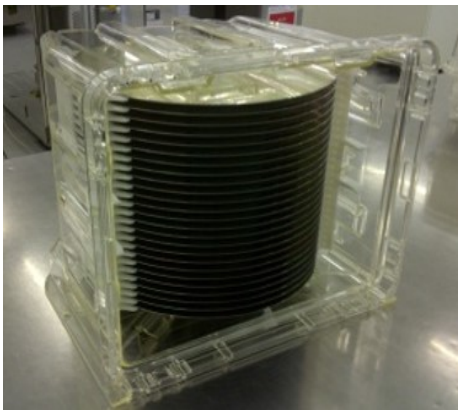


Figure 2.1: Wafers at the end of the front-end manufacturing stage. (ATEP, 2024)

Lastly, the third stage (back-end manufacturing - assembly, testing and packaging) mainly consists on the fabrication of packages, that will encapsulate the semiconductors, and its respective testing.

By comprising numerous layers of different materials, these packages (exemplified in Figure 2.2) will perform as a connection between the electrical components and the external environment while also acting as a protection against any moisture exposure, mechanical threats and chemical contamination that the semiconductor may potentially face.

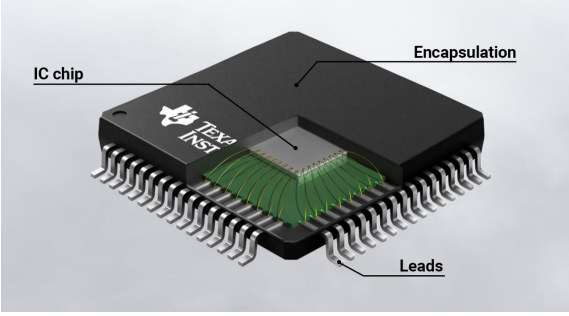


Figure 2.2: Example of a typical semiconductors package. (Instruments, 2021)

Albeit some companies are capable of performing these 3 major steps in-house, the majority of them opts to rely some functions to OSAT (Outsourced semiconductor assembly and test) companies, mainly in the third stated step. This is done to ensure that they can focus on the central competence of the two first stages: design and front-end manufacturing, which will, in turn, decrease operational costs and augment the capital efficiency of their investments. (Wu and Chien, 2008)

2.1.1 Embebbed Wafer Level Ball Grid Array Packaging Technology

The continuous size reduction of electronic devices, along with the demand for high-volume semiconductors production, has led OSAT companies to develop lighter yet denser packaging technologies, when compared to the ones traditionally used. This concern mainly arose since conversely

to the semiconductor's size, the number of connection points (points where electrical connections can be executed) has been progressively increasing. Subsequently, it can be rather challenging to find sufficient space on the semiconductor's surface to directly place all these points.

Amidst various revolutionary packaging technologies created to try and solve this issue, Infineon created the Embebbed Wafer Level Ball Grid Array (eWLB) Packaging Technology. This solution is based on a reconstituted (recon) wafer that increases the possible number of connection points on the package by increasing the available area for their placement. (Meyer et al., 2008)

In order to add the extra space around each individual die, this low-cost packaging solution, makes the package design independent from die size. (Wojnowski et al., 2008) This is done by embedding the silicon dies in an epoxy mold compound (EMC) in a predetermined position (as reflected in Figure 2.3).

Apart from allowing to obtain an higher connection points' density, this technology also allows to obtain a higher electrical, mechanical and thermal performance. Further, it also grants the possibility of shrinking the die size by about 30 % when compared with other conventional types of packages. (Hammerschmidt, 2007)

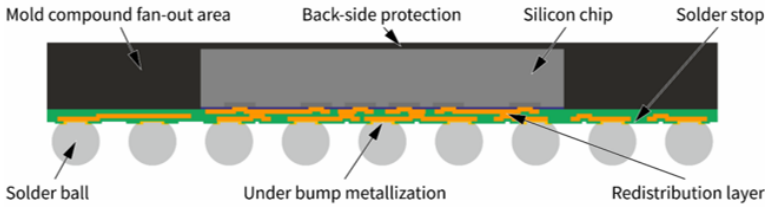
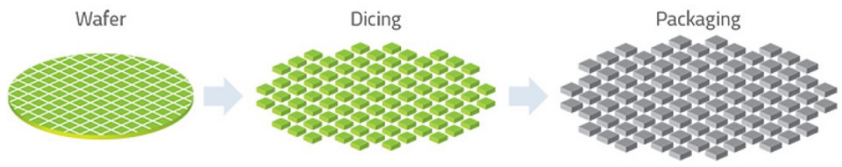


Figure 2.3: Schematic of the eWLB packaging technology. (Infineon, 2019)

This novel packaging technology, contrary to traditional packaging processes, functions on the premise that before dicing the silicon wafer into individual dies, all the packaging components must be properly applied, as shown in Figure 2.4.



(a) Traditional Packaging Process Flow.

(b) eWLB Packaging Process Flow.

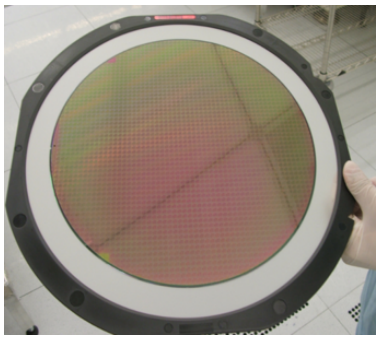
Figure 2.4: Illustrative flow of the different packaging technologies process flow. (Lee, 2017)

Please refer to Section 2.1.1.1 for more details concerning the manufacturing development of this packaging technology.

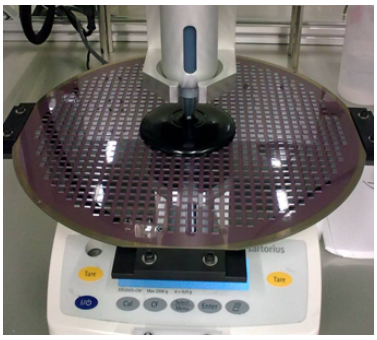
2.1.1.1 eWLB Production Process

As formerly mentioned, the manufacturing process of semiconductors can be divided into three distinct stages: design, the front-end phase (that focus on the silicon front-end wafer fabrication) and the back-end phase (that focus on packaging and testing of the reconstituted wafers).

Further, this back-end phase, where the eWLB packaging technology is included, can also be divided into 4 stages: wafer preparation, wafer reconstitution, RDL (Redistribution layer) and LBS (Laser, Ball attach, Singulation) - as in Figure 2.5.

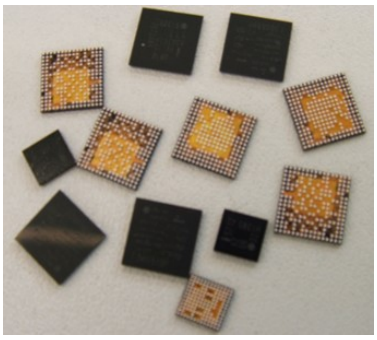


(a) Wafer Preparation.



(b) Wafer Reconstruction.

(c) Redistribution layer.



(d) Laser, Ball Attach, Singulation.

Figure 2.5: Phases of the eWLB packaging technology. (ATEP, 2024)

It should be stated that all this production process is conducted inside a clean room - a room that has an environment in which several parameters (temperature, humidity, particle per square meter and differential pressure) are highly controlled, monitored and maintained.

In the first phase of this novel technology - Wafer Preparation - the silicon wafer, from the front-end developer, is prepared to ensure these are suitable for further fabrication.

To do this, and after carefully checking the wafer's integrity, a thin protective tape is applied on the wafer's active side, as represented in Figure 2.6

Figure 2.6: Illustrative depiction of the application of the protective tape.

After the application of this tape, the front-end wafers are submitted to a grinding process, in their non-active side (opposite side to the tape), until they reach a specific nominal thickness, previously agreed with the front-end developer (as seen in Figure 2.7).

Figure 2.7: Illustrative depiction of the grinding of the front-end wafer.

Following this, as illustrated in Figure 2.8, the front-end ground wafer is mounted on a frame and the protective tape is removed.

Figure 2.8: Illustrative depiction of the mounting on a frame.

As the concluding step of the wafer preparation phase, this frame acts as a base for the individual dies (depicted in Figure 2.9), which are diced, in their active side, using a blade.

Figure 2.9: Illustrative depiction of the dicing of the front-end wafer.

The outcome of this entire phase is depicted in Figure 2.10.

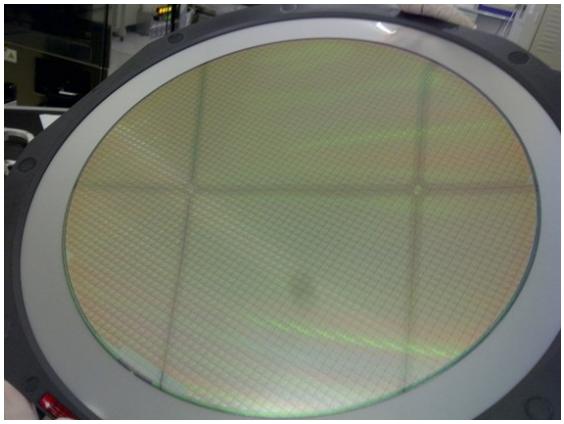


Figure 2.10: Wafer at the end of the Wafer Preparation stage. (ATEP, 2024).

After completing this step, the wafers will move to the Reconstitution (Recon) phase.

This phase begins with the application of a thin temporary adhesive film on a metallic plate, also known as a mold carrier (Figure 2.11a), that will hold the individual silicon dies, previously cut, in place (Figure 2.11b). It is important to note that the dies are placed with their active side facing the adhesive and that to increase the adhesion between this film and the dies, these components are submitted to a curing process.

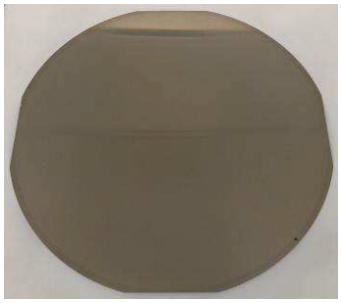
Despite this group of steps being rather simple, it can take a long time to complete, primarily given the die's small size and its high quantity in each individual wafer. (Pönninger et al., 2010)

After these steps, a high-thermal conductivity epoxy mold compound (a multi-component viscoelastic substance with a polymer-based matrix and inorganic filler particles (Brunnbauer et al., 2023)) is poured over the entire surface of the mold carrier (Figure 2.11c). This material will turn the previously placed dies into wafer format with a compression molding technique, providing mechanical protection, while also expanding the available area for the placement of solder balls (later detailed in this work). (Meyer et al., 2008)

After the removal of the adhesive film and the metallic plate, with the help of high temperatures, and a proper curing process of the mold compound, a reconstituted wafer is obtained, in which the silicon dies are embedded in the mold compound (Figure 2.11d).

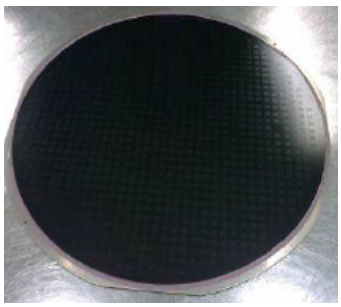
If this reconstituted wafer present no defects, it follows to the next step in which it will undergo a mechanical cut to ensure that the dimensional limits of the wafers are precisely met.

These Reconstruction phase steps are shown in Figure 2.11.

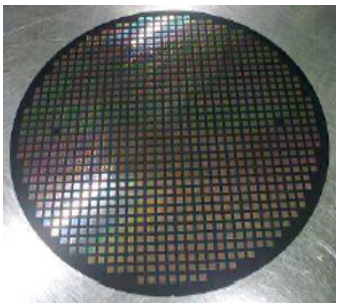


(a) Application of the film in the mold carrier.

(b) Placement of the individual dies on top of the film.



(c) Pouring of the mold compound on top of the individual dies.



(d) Removal of the adhesive and the mold carrier.

Figure 2.11: Illustrative flow of the wafer reconstruction phase. (ATEP, 2024)

The reconstituted wafer can now follow to the next back-end phase, namely the Redistribution Layer phase, which will build the distribution channels that connect the silicon dies to the outside.

Within this phase, the first step consists on controlling how well the placement of the silicon dies was executed. Afterwards, the wafers are cleaned with a plasma treatment, to ensure they have no trace of humidity left on them and to remove possible undesirable residues or particles.

Following this, a thin layer of a photoresist dielectric material (DL1) is dispensed on the reconstituted wafer in a liquid state, as represented in Figure 2.12. This type of material, characterized

by its low electrical conductivity, is used since it can sustain an electric field with very minimal leakage. (Reddy, 2014)

It should be emphasized that this dielectric material can be positive or negative. If positive, when exposed to ultra-violet (UV) light, it will become soluble to the photoresist developer. On the other hand, if negative, the areas exposed to UV light will become insoluble in the developer.

Figure 2.12: Illustrative depiction of the deposition of the first dielectric layer.

Hence, after this dielectric layer has been dispensed, several pre-designed patterns are transferred to the reconstituted wafer's surface with the aid of a high intensity UV light and an expose system, developed in the design stage. This makes it conceivable to obtain a layer with specific small opening for the die's dicing streets.

As can be seen, in the example depicted in Figure 2.13, the used material is negative, meaning only the irradiated material will remain on the reconstituted wafer.

Figure 2.13: Illustrative depiction of the irradiated first dielectric layer.

With this step concluded and after submitting the reconstituted wafer to a curing process to increase the strength of the dielectric layer that remains on it, a thin layer of sputtered material (normally, titanium and copper) is applied on the wafer.

This layer, shown in Figure 2.14, commonly referred to as seed layer, will function as the conductive substrate for the copper bonds to be built up later by the process of electroplating.

Figure 2.14: Illustrative depiction of the deposited seed layer.

Following this, another photoresist layer is applied so that other pre-designed patterns can be transferred to the wafer leaving, once again, only openings on the dicing streets and on the pads where the solder balls will later be applied. Conversely to DL1, the layer deposited as shown in Figure 2.15, is typically a positive resist - the areas exposed to light become soluble and disappear.

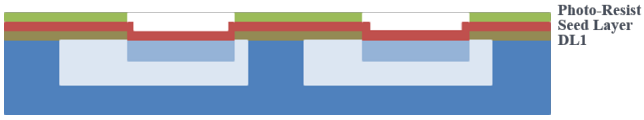


Figure 2.15: Illustrative depiction of the irradiated photo-resist layer.

It should be clarified that this layer is not composed of a dielectric material and it will only act as a sacrificial layer whose sole function is to define the copper electrodeposition zones.

As such, after the deposition and proper developing of this layer, copper is then placed in these open spots via electroplating, as represented in Figure 2.16.

Figure 2.16: Illustrative depiction of the wafer after the copper electroplating.

The next step in the RDL phase consists on properly removing this photoresist material and excess seed layer by wet etching, that is, by immersing the material in a liquid bath of a chemical etchant (Singh et al., 2013). The final result of this step is illustrated in more detail in Figure 2.17.

Figure 2.17: Illustrative depiction of the removal of several layers.

Depending on the product's specifications, this process of adding multiple dielectric layers can be performed several times. As seen in Figure 2.18, another dielectric layer (DL2) was applied. This layer will later be submitted to the same UV light in order to reveal its streets (Figure 2.19).

Figure 2.18: Illustrative depiction of the deposition of the second dielectric layer.

Figure 2.19: Illustrative depiction of the irradiated second dielectric layer.

The last process in this phase, albeit optional, consists of the under bump metallization process (UBM). In this, another copper layer is deposited over the irradiated positive sections of another photoresist material, which is itself on top of another seed layer above the DL2 layer. This creates an interface between the IC and the solder bump that will be added later (as shown in Figure 2.20).

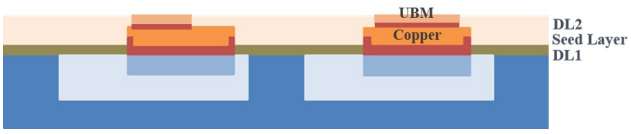


Figure 2.20: Illustrative depiction of the deposition of the UBM layer.

After this phase has been finalized, the wafer can now enter the LBS (Laser, Ball attach, Singulation) phase.

This phase starts with the deposition of a thermally activated metallic flux with the assistance of a stencil. After this flux has been properly dispensed, the balls are then accordingly placed on top of each opened street, previously created in the RDL phase.

These balls, whose main function consists of making the electrical connections between the silicon die and the outside of the integrated circuit, will be soldered to the pads when the reconstituted wafer is submitted to temperatures that reach the flux's activation temperature.

The final result of this step can be seen in Figure 2.21.

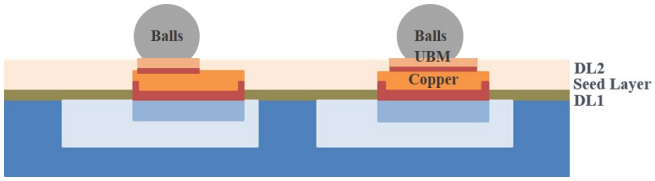


Figure 2.21: Illustrative depiction of the soldered solder balls.

After soldering the balls, the reconstituted wafers can follow two distinct paths: Path 1 and Path 2.

In Path 1, the reconstituted wafers are submitted to yet another grinding process until they reach a pre-determined final thickness. It is crucial to highlight that this grinding step is only executed after the wafers go through the majority of the process flow to ensure they are not very flexible throughout it.

Following this grinding process, the reconstituted wafers go through a proper laser marking for easier identification and are, according to the client's preference, singularized or not into individual units, inspected, placed on trays/frames, packed and shipped back to the front-end developer.

Conversely, in Path 2, the reconstituted wafers with the solder balls accordingly placed are shipped directly to the front-end developer. This developer will then proceed to grind the wafers and perform all the subsequent required steps.

This concludes the sequential flow of the Embebbed Wafer Level Ball Grid Array packaging technology, succinctly shown in Figure 2.22.

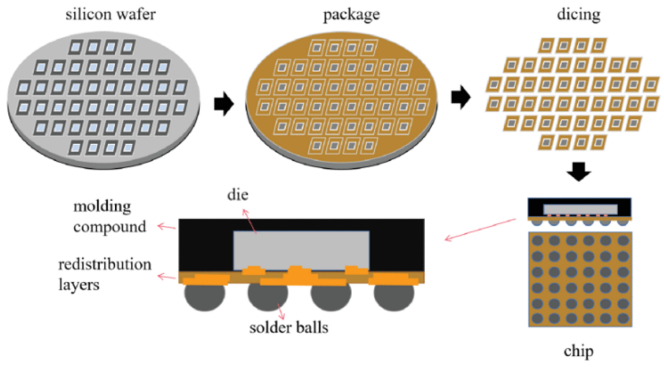


Figure 2.22: Sequential flow of the eWLB packaging technology. (Gao et al., 2022)

2.1.1.2 Component Specifications

To gain a better understanding of some of the components, mentioned in Section 2.1.1.1, that have a great impact on the previously stated challenge, warpage, this upcoming section will delve into specific details about them.

1. **Epoxy Mold Compound**

   The rigid thermoset polymer mold compound utilized by ATEP is composed of an epoxy resin, fillers, hardeners and some other additional additives.

   The fillers will contribute to its fundamental mechanical properties, such as mechanical resistance and thermal conductivity, while the inclusion of epoxy resin and hardeners will improve the mold compound's wettability, as well as its thermal and electrical stability. (Cardoso, 2021)

   As can be seen in Figure 2.23, in the eWLB packaging technology, this mold compound is poured over the dies in a liquid state at room temperature.

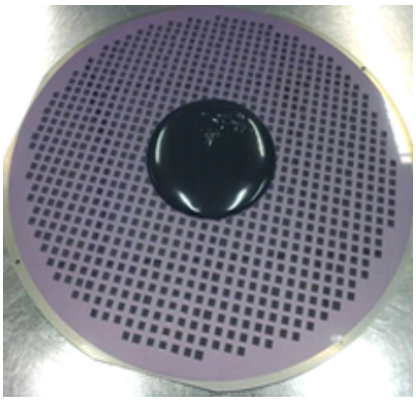


Figure 2.23: Pouring of the epoxy mold compound over the silicon dies. (ATEP, 2024)

   This thermoactive material represents a branch of polymers that exchange electrons to form new chemical bonds during curing. (Greene, 2021) The curing, that can occur due to heating or through the addition of a curing agent, will culminate in well-defined polymers with irreversible networks grown in three-dimensional (3D) directions. (AlMaadeed et al., 2020)

   It is important to note that the curing of this material tends to be a challenging task since these types of polymers exhibit chemical and thermomechanical coupled behavior, with molecules cross-linking through the curing process. (Baek et al., 2022)

   Additionally, this low-molecular-weight material has a specific temperature range in which the polymer chains start to move - the glass transition temperature (Tg). (Yusoff et al., 2023)

   As represented in Figure 2.24, when temperatures above Tg are employed, the EMC will transit from a solid state into a softer one. Moreover, the material's coefficient of thermal expansion will increase by 2-3 times, while conversely its hardness and modulus of elasticity will decrease. (Kokatev et al., 2019)

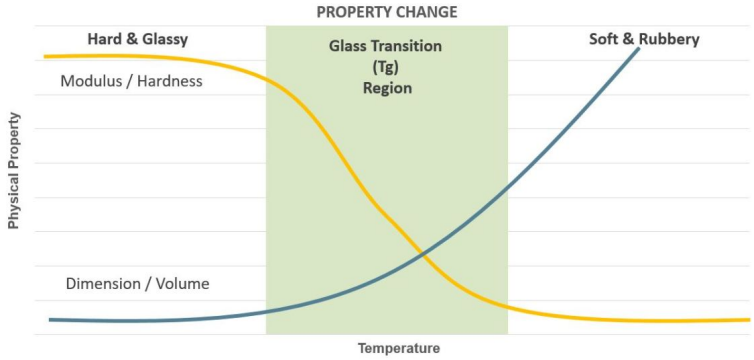


Figure 2.24: Effect of surpassing the glass transition temperature on the EMC properties. (Perabo, 2018)

It is important to emphasize that despite usually being defined as a material constant, this temperature can vary throughout the packaging process when submitted to the various thermal processes included on it. (Kokatev et al., 2019)

For instance, when the wafer is submitted to a curing stage, its 3D molecules' arrangement varies. (Cardoso, 2021) This variation may cause the molecular motion to become more restricted and consequently the Tg values will be greater. This will be due to the fact that more energy will be required to transition from one state to another.

2. **Dielectric Layers**

   The dielectric layers applied in the third phase of the eWLB packaging technology will be Polyimide (PI) layers.

   This material is an organic polymer with excellent mechanical properties and high levels of heat resistance. (Tomikawa, 2021) Additionally, it also possesses good insulating properties, coupled with a low dielectric constant that guarantees the packaging's electrical performance without any degradation. (Thapa, 2020)

   It is imperative that this material's curing temperature remains below the EMC's glass transition temperature since the dielectric layers are fabricated on top of it. (Thapa, 2020)

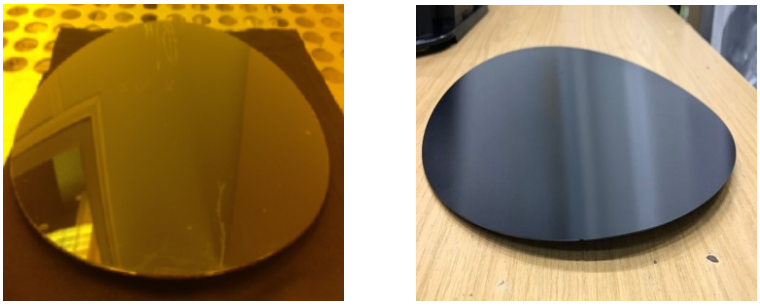
As can be concluded, there are not only a large number of steps in the eWLB packaging process, but also these steps have various processing temperatures that induce significant stresses on the wafer, leading to the appearance of warpage in them.

2.2 Warpage

As previously stated, with the recent technological advancements, the production of semiconductors has suffered innumerate changes. One of these consists on the fact that the wafers' diameter has been gradually increasing and conversely, when it comes to their thickness, the opposite has been happening.

Even though these changes come to increase a sole wafer's profitability and material usage, they also come with some challenges, namely, the appearance of warpage in them.

Warped wafers (exemplified in Figure 2.25) can be rather hard to handle on various steps of the packaging process and can be considerably detrimental to the equipment handling them. As a result, early detection of it becomes essential to minimize both the cost and the overall cycle time.



(a) Example 1. (Cardoso, 2021) (b) Example 2. (ERS, 2021)

Figure 2.25: Examples of warped wafers.

In the literature, there are numerous definitions used to define warpage. However, the most commonly used one consists on it being the difference between minimum and the maximum distance of the wafer to a reference plane, as seen in Figure 2.26.

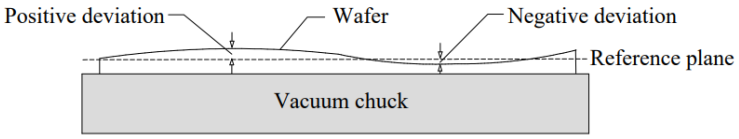
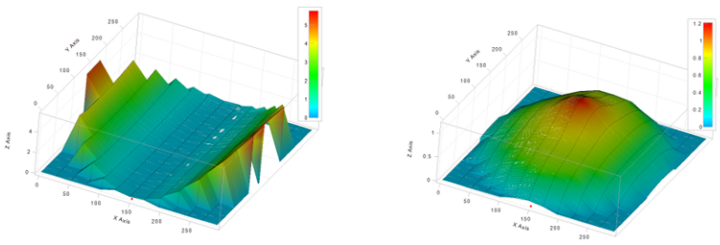


Figure 2.26: Schematic of a warped reconstituted wafer. (Quirk and Serda, 2001)

This warpage, according to the convention used for the concavity of the reconstituted wafers, can assume two distinct forms: a positive shape or a negative shape (both depicted in Figure 2.27).

The warpage will be negative if it has a concave shape, i.e. if the center of the wafer is lower than the periphery. Contrarily, the warpage will be positive if it has a convex shape, i.e. if the center of the wafer is higher than the periphery.



(a) Negative shaped wafer. (b) Positive shaped wafer.

Figure 2.27: 3D representation of warped wafers with different forms. (ATEP, 2024)

There are various parameters that all intertwined with each other, influence not only the amount of warpage present in a wafer, but also the shape of it.

According to Campos et al. (2015) the greatest warpage contributions come from three main factors:

1. The material's dissimilar responses to thermal stresses;
2. The material properties and characteristics;
3. The disposition of the different materials within the package.

An essential material property, particularly relevant in the context of thermal stresses, is the coefficient of thermal expansion (CTE). This property measures the change in a unit length of material due to a 1 ºC temperature variation. This indicates that, when heating, a material with a higher CTE value will expand more than a material with a lower CTE. Moreover, upon cooling, it will contract more as well. (Phansalkar et al., 2022)

Furthermore, it is worth noting that a material's CTE is not a constant value. Depending on the temperature that the material is submitted to, this value can assume various levels.

For instance, and as previously stated, if the temperature rises past the glass transition temperature, the epoxy mold compound will begin to soften and lose some of its tensile strength. Consequently, the CTE tends to generally rise.

Given that there are three dissimilar main components (the silicon die, the EMC and the dielectric layers) in the reconstituted wafer, there will be a mismatch between their CTE values. As such, they will contract and expand at different rates, inducing mechanical stresses on the wafer.

The curing of the mold compound, which occurs at temperatures above its Tg, is a crucial processing step that takes place after the mold has been deposited on top of the silicon dies. In this, the CTE mismatch between materials is the primary reason for the appearance of warpage.

Figure 2.28a represents the wafer after the curing process, before the start of the cooling stage. The mold compound's higher CTE value will make it so it contracts more than the silicon die. Therefore, the silicon die will be fully contracted while the mold compound will keep on contracting. Since they share a common interface between them, this superior contraction force exerted by the mold compound, which is located on top of the silicon die and has a greater thickness value, will not only create additional stresses on the wafer but also create an additional bending moment, pulling the silicon die inward (Figure 2.28b).

It should be noted that this phenomenon only occurs since the EMC's thickness is sufficient to overcome the counter force that the silicon die, fully contracted, tries to impose upon it.

(a) Beginning of the step. (b) End of the step.

Figure 2.28: Illustrative depiction of the CTE mismatch impact on warpage after the curing process, above Tg, of the epoxy mold compound.

Apart from this difference in their CTE values, the mold compound and silicon die will also highly vary in thickness depending on the front-end developer's specifications. This factor, schematically represented in Figure 2.29, coupled with these components' inherent characteristics will also greatly influence the level of warpage present on a wafer.

It is worth highlighting that the difference between the silicon and the mold compound thickness is known as the overmold thickness (Figure 2.29 - c).

Figure 2.29: Schematic of the silicon die (a), mold compound (b) and overmold (c) thicknesses.

Lastly, concerning relevant parameters associated with the material properties and characteristics, is whether the wafers are full loop or short loop wafers.

Short loop wafers can be defined as front-end wafers that have only gone through a subset of the total packaging flow of the front-end developer. These wafers, typically used for process reliability tests, will only have a set of specific layers while conversely, full loop wafers go through a more comprehensive and detailed production process and end up with all the layers a productive material would typically have.

In a preceding study to the elaboration of this dissertation, during my summer internship at Amkor Portugal, it was found, as illustrated in Figure 2.30, that the difference between these two types of wafers is significant. In the analysed processing steps, full loop wafers tend to have higher values of warpage throughout the packaging flow when compared to short loop wafers.

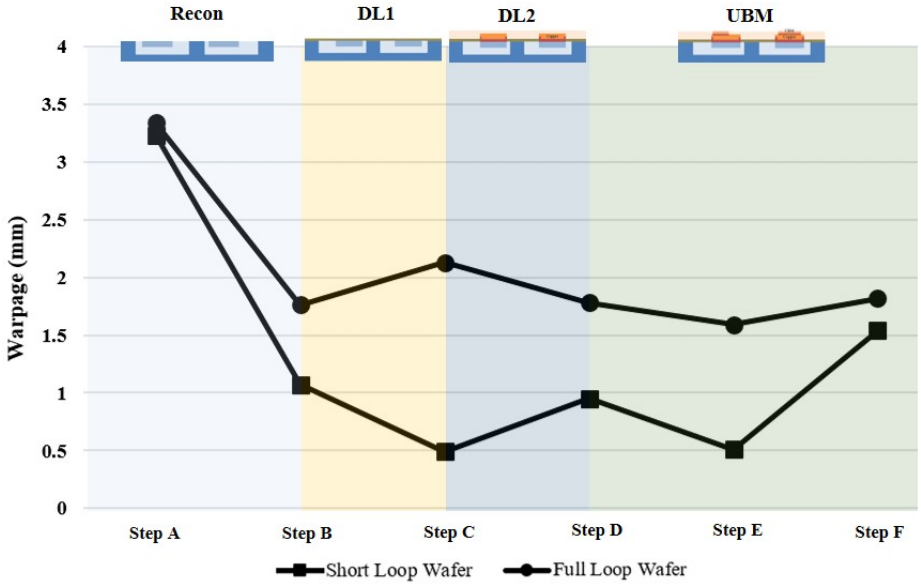
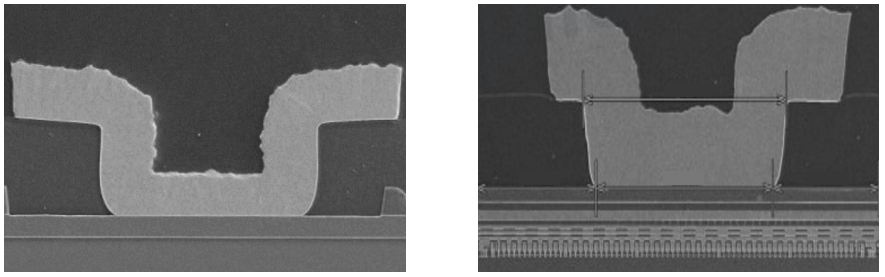


Figure 2.30: Differences between warpage in Full Loop and Short Loop wafers in different steps of the packaging production process. (ATEP, 2024)

For a depiction of the visual differences between these two types of wafers, please refer to Figure 2.31.



(a) Short Loop. (ATEP, 2024) (b) Full Loop. (ATEP, 2024)

Figure 2.31: Example of Short/Full Loop wafers.

When it comes to the disposition of the different materials within the packaging, one of the most relevant aspects is the wafer's volume occupation ratio (VOR).

In the design phase of the wafers, the mold compound and silicon thicknesses vary significantly according to the specific front-end developers' requirements. These thicknesses will, in consequence, impact the volume of the wafer and directly lead to differences in this parameter.

The volume ocuppation ratio, shown in Equation 2.1, depicts the percentage of volume that is occupied by the dies in a single wafer. According to it, if the volume of the die and the number of dies remains constant, the higher the wafer volume, the lower the volume occupation ratio.

$$VOR = \frac{Volume\ of\ the\ die * Number\ of\ dies}{Volume\ of\ the\ wafer} * 100 \tag{2.1}$$

At last, another aspect thought to have some impact on warpage, yet almost negligible, is the population of each wafer, that is, if they are fully or partially populated.

To understand this concept, it is first imperative to define the difference between three different terms: blank silicon dies, functional dies and testing dies. The list below outlines their difference.

- **Functional Dies:** Dies from the front-end developer with the silicon substrate and numerous other layers developed in the front-end stage.
- **Blank Silicon Dies:** Dies composed of a silicon substrate, directly originated from the front-end developer, without any added layers on top.
- **Testing Dies:** Dies from the front-end developer especially designed to possess leakage and contact resistance testing capacities.

A fully populated wafer is a wafer fully composed of functional dies and testing dies, whereas a partially populated one has all three types of dies: functional, blank silicon and testing dies. The latter is commonly used for testing purposes since it does not consume as much front-end developer's productive and functional material.

By discerning the results, shown in Table 2.1 and Figure 2.32, of a study executed for this dissertation, by a group of engineers with a high numerical simulation expertise, it is possible to conclude that in the beginning and the end of the process, using functional or blank silicon dies - on a fully populated wafer - will have a slight impact on warpage, albeit almost insignificant.

Please note testing dies were not used in this simulation as their quantity in each wafer is not significant when compared to the other types of dies.

Table 2.1: Warpage study's simulation design of experiments. (ATEP, 2024)

Leg	Die	Stage of the process
Leg 1	Functional	Beginning of the process
Leg 2	Blank Silicon	Beginning of the process
Leg 3	Functional	End of the process
Leg 4	Blank Silicon	End of the process

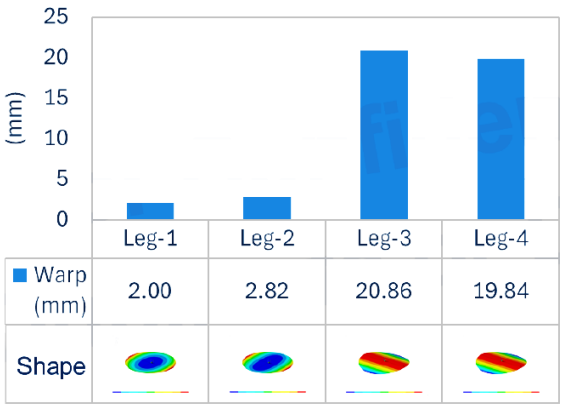


Figure 2.32: Wafer warpage study between functional dies and blank silicon dies. (ATEP, 2024)

Please note the obtained warpage values are from a numerical simulation and, as such, may have some considerable discrepancy when compared to the results obtained experimentally.

2.2.1 Warpage Measurement Techniques

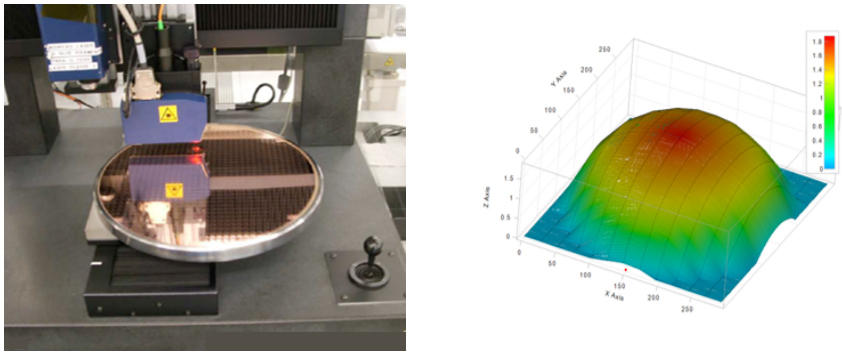
With the purpose of properly assessing the wafers's warpage levels and in order to see if it is possible for the product to move to the next step in the manufacturing chain, various warpage measurements have to be conducted throughout the manufacturing process.

For the development of this work, two different measuring equipment were used: an optical scanning profilometer from Nanofocus and a Sorter.

2.2.1.1 Nanofocus Optical Profilometer

The Nanofocus Optical Profilometer (seen in Figure 2.33a), specifically developed for research and development areas, is used to perform a non-contact surface characterization of the wafers

with the aid of a high-precision point sensor. (Cardoso, 2021) By scanning these wafers in a square line pattern, this sensor will make it feasible to acquire three-dimensional images of them (exemplified in Figure 2.33b).



(a) Configuration of the device. (Cardoso, 2021)

(b) 3D image obtained by the equipment. (ATEP, 2024)

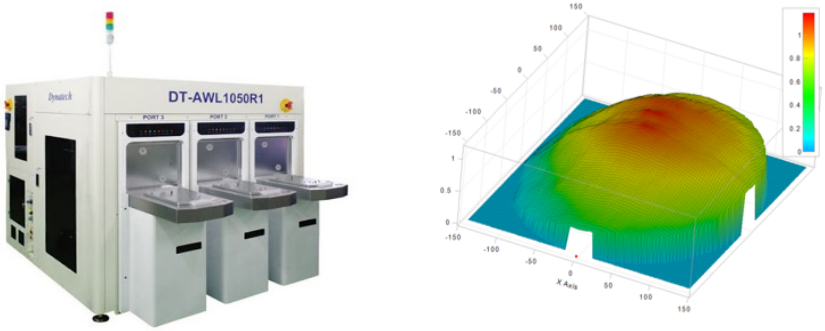
Figure 2.33: Nanofocus Optical Profilometer configuration and obtained results.

In this equipment, the level of warpage will be the maximum value of all the obtained surface profile's heights (Z axis) using the equipment's referential coordinate system with automatic acquisition. (Peixoto, 2014) This equipment measures this height in, approximately, 46 points.

It is important to emphasise that, while measuring with this equipment, the wafer must be placed, by the worker, with its active side facing up, in a plain chuck. Thence, measurements with this equipment may be compromised by the manual handling of the wafers.

2.2.1.2 Sorter

The other measuring equipment shown in Figure 2.34a, Sorter, operates similarly to the Nanofocus equipment as it performs a complete scan of the wafers in a square line pattern and equally obtains 3D dimensional images of them (Figure 2.34b).



(a) Configuration of the device. (DynaTech, 2024)

(b) 3D image obtained by the equipment. (ATEP, 2024)

Figure 2.34: Sorter Equipment configuration and obtained results.

Contrarily to the Nanofocus equipment, the Sorter equipment can operates in two settings: Plain Chuck (Figure 2.35a) and Pre-Aligner, while measuring a significantly higher quantity of points - 500.000 points compared to Nanofocus' 46 points.

This frequently employed measurement technique, Pre-Aligner, consists on simulating a non-flat surface (depicted in Figure 2.35b), which centers the wafer within a central column, leaving the wafer's outer borders suspended.

This technique is crucial since a high number of equipment used on the semiconductors packaging industry relies on a Pre-Aligner component to execute its function. As a result, ensuring that the levels of warpage are adequate for the equipment to effectively handle these wafers, becomes an essential procedure.

(a) Simulation of a Plain Chuck. (b) Simulation of a Pre-Aligner.

Figure 2.35: Warpage measured by the Sorter Equipment. (ATEP, 2024)

At last, this equipment will not only provide specific warpage levels but also allow to evaluate the wafers' stiffness. This is achieved by observing the extent to which the wafers' edges are suspended relative to the middle column. If the points on the edges remain at the same level as the points of the wafers supported by the middle column, it implies the wafers are rigid. Conversely, if the wafers' edges are significantly suspended, it denotes that the wafers are flexible.

2.2.2 Warpage Correction Techniques

Out of specification (out-of-spec) warped wafers can be classified as wafers that have warpage levels that have an absolute value that is too high to properly be processed in a particular step of the packaging production process.

As mentioned earlier, this higher level of warpage can lead to, not only the breakage of the wafers while processing but also, in extreme cases, to the damage of the processing equipment. As a consequence, it becomes inevitable to make the wafers go through different correction techniques throughout the manufacturing process to decrease these levels.

It should be noted that the values may be inside the allowable limits and some wafers still need to undergo these aforesaid correction techniques. This may happen when there is a possibility the warpage shapes are not conform to the shape some equipment can handle or if the stiffness levels are deemed to be too low.

To implement these correction techniques, two distinct pieces of equipment, which will be referred to as Equipment A and B can be utilized. Both of them employ one basic mode of thermal energy transport - thermal conduction - to perform these corrections.

This mode is defined with Fourier's law of heat conduction without any flow of matter. Fourier stated that the rate of heat transfer is directly proportional to the gradient of temperature and the area perpendicular to the gradient through which the heat flows. (Dincer and Erdemir, 2021)

In this law, mathematically translated in Equation 2.2, Q represents the rate of heat flow through a material with a specific thermal conductivity (k), across a specific area (A) and thickness (Δx), across which the temperature change is ΔT.

$$Q = -k * A * \frac{\Delta T}{\Delta x} \tag{2.2}$$

2.2.2.1 Equipment A

Equipment A comprises multiple flat chucks, set at different temperatures, to produce thermal stresses that will induce mechanical alterations in the wafers. These chucks can be operated manually or automatically.

The warped wafer is initially positioned on a ho chuck, that gradually raises the wafer's temperature past the mold compound's Tg value, as seen in Figure 2.36a. As the temperature increases, both the silicon and the mold compound will expand, although the latter will expand more due to its higher CTE. By expanding, the wafer will release its internal stresses and flatten out (as observed in Figure 2.36b).

Next, the platform is tilted until the wafer begins to slide and reaches the cold chuck (Figure 2.36c). Once there, it will be exposed to a thermal shock that will freeze its molecules. This makes it so they remain in the same flattened state they had when they were on positioned on top of the hot chuck.

(a) Before staring the warpage correction technique.

(b) During the warpage correction technique.

(c) After the warpage correction technique.

Figure 2.36: Illustrative steps of equipment A's correction technique flow.

As the environment within this equipment is not controlled, correction of warpage levels in it can only be performed until the application of the seed layer. This is due to the fact that after

the deposition of the sputtered layer, there could potentially be oxidation of the wafers and its consequent degradation.

As such, it is important to emphasise that, for this illustration, the wafer is simplified to only having a silicon layer and a mold compound layer, in spite of the fact that realistically, it could also encompass the first dielectric layer on top - depending on the manufacturing step where the product was on.

The temperatures imposed in each chuck are highly dependent on the specific characteristics and features of each individual wafer. With the prior knowledge acquired by ATEP, it was possible to develop a flowchart with the optimal temperature range for different combination of characteristics and features.

This flowchart is represented in Figure 2.37.

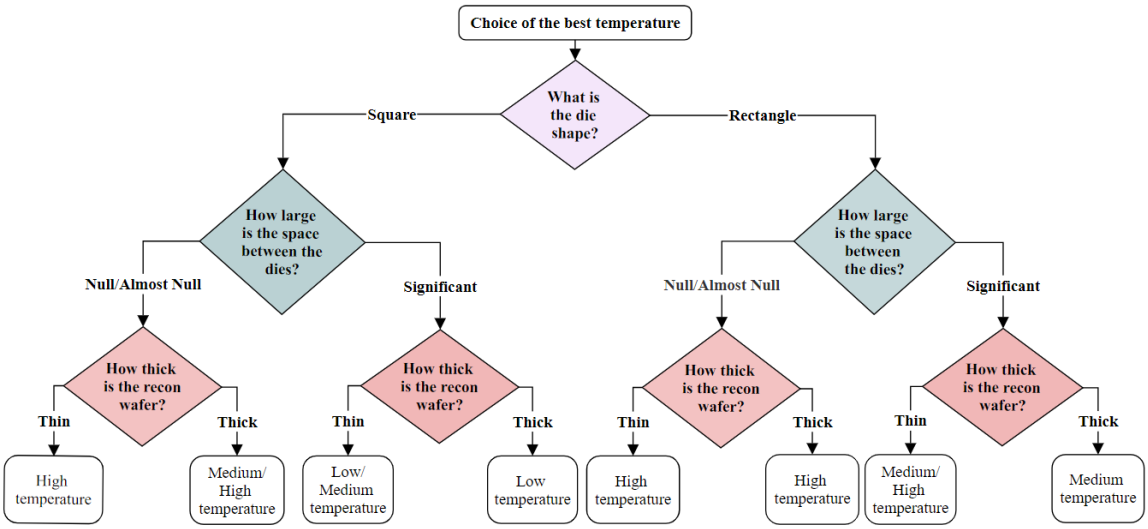


Figure 2.37: Equipment A's correction techniques flowchart for reconstituted wafers.

Due to confidential reasons, the numerical values for the wafers' usual spacing between dies and usual thickness can not be revealed and, as such, they will be simplified to it being either null/significant and thin/thick, respectively.

As can be observed, a distinction was not made between the wafer being fully or partially populated. This is a consequence of the fact that the warpage correction techniques are firstly tested on partially populated wafers of a certain product. If these techniques are proven to be effective, then the same ones are applied to the fully populated ones. Typically, these correction techniques have been demonstrated, through testing, to also correctly lower the warpage values in fully populated wafers. If eventually this is not the case, small adjusts to this flowchart will be executed.

2.2.2.2 Equipment B

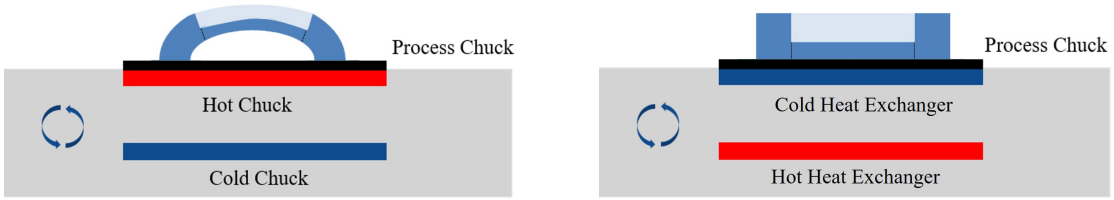
The other equipment, Equipment B, that can be either automatically or manually operated, typically has 3 main components: a process chuck, a hot heat exchanger and a cold heat exchanger

(both located underneath the process chuck) - as depicted in Figure 2.38.

The hot heat exchanger, heated to a high temperature, will come in near contact with the wafer placed on top of the process chuck, transferring heat to it (as shown in Figure 2.38a). By increasing its temperature and due to its properties, the wafers will, once again, expand, release some of its internal stresses and become more malleable - which facilitates the reshaping of it. After the specified temperature is reached, there is a mechanical auxiliary device that retains the wafer in its flatten out state.

Afterwards, with this mechanical auxiliary device on place, the cold heat exchanger will come in contact with the process chuck, gradually lowering its temperature (as represented in Figure 2.38b).

It is important to emphasise that the two heat exchangers are never in near contact with the wafer at the same time.



(a) Before starting the warpage correction technique.

(b) After the warpage correction technique.

Figure 2.38: Illustrative steps of equipment B's correction technique flow.

Ergo, by combining these thermal fluctuations with the assistance of the mechanical auxiliary device that flattens the wafer, reductions in warpage levels are typically observed.

Furthermore, it is also crucial to highlight that this equipment never operates above the mold compound's Tg value but can reach temperatures proximal to it. This constraint is due to the fact that this equipment's processing time is significantly longer than Equipment A's processing time. If temperatures above Tg were employed, for long periods of time, there could be induced some silicon die shift, as the mold compounds transitions to a highly malleable state at elevated temperatures.

In addition, this equipment has a controlled environment with a N2 flux system. Not only will this prevent the aforementioned possible wafer oxidation but it will also give the equipment the chance of better controlling the rate in which the environment heats or cools down. This is due to the fact that the temperature of the flux can be easily monitored and changed throughout the process.

It is important to note that a flow chart with the optimal temperature range for different combinations of wafer characteristics has not been developed for this equipment. This is due to the fact that while developing this dissertation, an effort was made to standardize the recipe used throughout the entire packaging process. As a result, only one recipe is used, the specifics of which will be discussed later.

To sum up, the main differences between these two pieces of equipment are as follows: Equipment A has its use limited until a specific part of the process and relies on thermal stresses to induce mechanical alterations in the wafer. Moreover, its warpage correction techniques are much faster than the ones performed with Equipment B. In contrast, Equipment B, uses both thermal and mechanical stresses to induce mechanical alterations in the wafers and can be used throughout the entirety of the manufacturing process.

2.3 Flowchart

To provide the reader with an easier understanding of this work and its key steps, a chart, depicted in Figure 2.39, was developed.

As can be seen, two distinct products, refereed to as Product A and Product B, were used. Each product featured 3 different experimental runs, with a varying characteristic, mold compound thickness (MT), and consequently different VOR values. Additionally, the silicon die thickness (ST) will remain constant within a specific product.

These two products will undergo the traditionally used ATEP's manufacturing process (Wafer Prep, Recon, RDL and LBS), with warpage measurements in between some specific steps, taken using two different equipment – Nanofocus and Sorter. Throughout the flow, if the warpage levels are deemed to be outside of the permissible limits, the entire run will be submitted to a warpage correction technique, either in Equipment A or Equipment B.

It is important to note that due to their different nature, each experiment will require different warpage correction techniques throughout the process and consequently have different manufacturing timings.

These differences, coupled with the initial different characteristics of each experimental run, will make it possible to study the influence certain parameters have on the occurrence of warpage.

In addition, through a comprehensive analysis of the measurements taken both before and after implementing each correction technique, it becomes possible to delve into the impact of varying correction temperatures and timings on the wafer's flatness. This examination allows to infer the efficiency of each recipe in minimizing warpage levels, as closely to zero as possible, while also achieving the specific wafer shape necessary for each step of production.

Moreover, all the measured warpage values of both products A and B, will allow to extract conclusions regarding the impact that different ranges of processing temperatures, used in the various steps, have on the warpage levels.

As a further research related to this study, an extra experimental run with the same characteristics as Experiment 4 will be studied. Although with identical material characteristics, this experiment will undergo some steps of ATEP's manufacturing process without the application of the first dielectric layer. This will allow to study the influence of this layer in warpage levels.

Lastly, it should be emphasized that due to confidential reasons, the numerical values of the aforementioned material characteristics can not be disclosed and as such, references values for the mold and silicon thicknesses were stipulated - POR_{MT} and POR_{ST}, accordingly (for each studied

material). To these values, each experimental run will have an increase of either 5 % or 10 % in the varying thickness value.

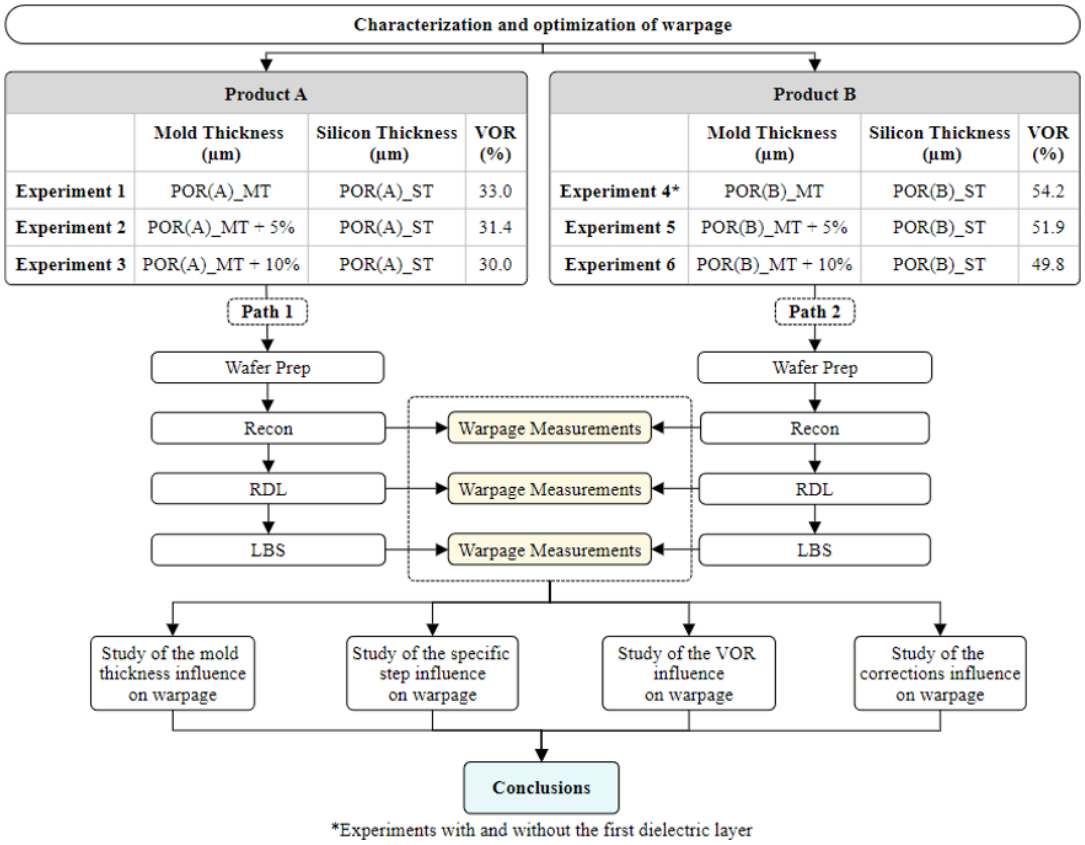


Figure 2.39: Chronological flowchart of the stages developed throughout the dissertation.

It should also be established that these experimental runs were chosen considering the time restrictions implemented by the duration of the dissertation's period. This led to prioritizing the most significant study characteristic: mold compound thickness value. Unlike the silicon thickness, the mold compound thicknesses will differ on the various experimental runs and their final thickness, after the last grinding step, will meet the front-end developers' specifications.

Nonetheless, it is still acknowledged that for a better understanding of the different wafer characteristics impact on warpage, both the silicon and the mold compound thickness values should ideally vary at least three levels.

As such, and even though these new variations were not experimentally implemented, this dissertation will still characterize these new hypothetical experimental runs using the Design of Experiments tool, specifically the Taguchi Method, in the subsequent chapters.

2.4 Design of Experiments

Design of experiments (DOE) is a statistical and mathematical tool, introduced by the British mathematician and statistician, Ronald A. Fisher, to perform systematic experiences, while making

deliberate and simultaneous changes to the input variable(s), in order to observe the resulting change to the output variable(s). (Reis and Silva, 2023)

A simplified version of this tool can be read in Figure 2.40.

In this, the factors represent the process variables that influence the process response (outputs), while the levels are a representation of the different characteristics that the factors can adopt in the various experiments. Moreover, the non-controllable factors represent the group of factors that cause variability on the process, but that can not be controlled.

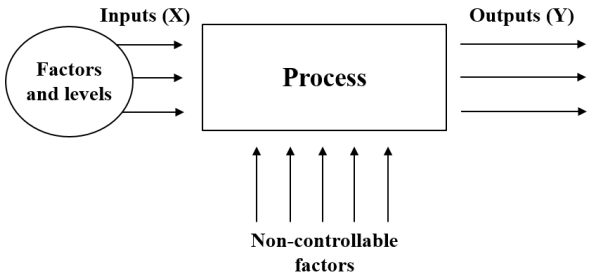


Figure 2.40: Process map diagram according to Taguchi's methodology. (Peixoto, 2014)

According to Reis and Silva (2023), the four main objectives of this tool consist on determining which input variables: have the greatest influence on the output variables; best lead to the desired output(s); guarantee the least variability on the output variables and are the least impacted by the non-controllable factors.

This tool not only decreases the prevision's error, as well as it increases the probability of the gathered experimental data being a reliable representation of reality. Additionally, with the use of this tool, the chances of the obtained data being pertinent to the technical objective of the study at hand are also increased exponentially. (Reis and Silva, 2023)

The choice of the best experiment to choose from highly depends on three main factors: the objective of the study, the cost of each experimental study and the number of factors and respective levels. (Reis and Silva, 2023)

Moreover, usually, this method can be divided into two different categories: the full fractional design method, that involves testing all possible combinations for a given set of factors, and the fractional factorial design method, that involves selecting a subset of factor combinations to investigate. (Kechagias et al., 2020)

In the semiconductor packaging industry, there are multiple highly complex relationships between the input parameters and process characteristics. As so, it would be exorbitantly time consuming to perform all of the possible combinations in order to fully grasp the relationships between these parameters.

Therefore, a DOE method, more specifically the Taguchi Method, has become widely adopted in this industry worldwide. (Yuangyai and Nembhard, 2010) This method does not limit the number of variables and does not preclude any investigation in how the different variables interact with each other.

2.4.1 Taguchi Method

Dr. Genichi Taguchi, a Japanese engineer and statistician, developed a robust statistical approach, specifically designed for industrial applications that emphasizes the need of pushing quality back to the design stage. (Unal and Dean, 1991) In this approach he aimed to find the minimum number of experiments that have to be conducted to obtain precise and reliable results, within the allowable limit of factors and levels. (Meena et al., 2018)

This method efficiently examines how different process factors affect the mean and the variance of a process performance characteristics. Additionally, by reducing the number of experimental runs, there is an optimization of the time, cost and resources used throughout the development of these experiments.

Taguchi's approach is based on the use of orthogonal arrays, that is, a set of systematically arranged test cases that allows to only test pairs of combinations, instead of having to test all the possible combinations. (Boparai and Sandhu, 2023) In other words, this approach allows to study a large number of variables with the smallest number of experiments possible. Moreover, each variable can be assessed independently of all the other variables, so each variable's effect does not affect the estimation of a different one.

It is important to emphasize that Orthogonal arrays were not invented by Dr. Genichi Taguchi. However, the Japanese engineer simplified their use by providing tabulated sets of standard orthogonal arrays and corresponding linear graphs to fit specific projects - as exemplified in Figure 2.41. As can be seen in the given example, the columns are mutually orthogonal - all combinations of factor levels occur at an equal number of times.

In the example depicted in Figure 2.41, the experiment had 11 different parameters, spanning from A to L, each at 2 levels. If the Taguchi method had not been used, to test all these factors, 2048 experiments would be needed. With the Taguchi Method, this number decreases to 12 experiments.

Experiment No.	Process Parameter Level										
	A	B	C	D	E	F	G	H	J	K	L
1	1	1	1	1	1	1	1	1	1	1	1
2	1	1	1	1	1	2	2	2	2	2	2
3	1	1	2	2	2	1	1	1	2	2	2
4	1	2	1	2	2	1	2	2	1	1	2
5	1	2	2	1	2	2	1	2	1	2	1
6	1	2	2	2	1	2	2	1	2	1	1
7	2	1	2	2	1	1	2	2	1	2	1
8	2	1	2	1	2	2	2	1	1	1	2
9	2	1	1	2	2	2	1	2	2	1	1
10	2	2	2	1	1	1	1	2	2	1	2
11	2	2	1	2	1	2	1	1	1	2	2
12	2	2	1	1	2	1	2	1	2	2	1

Figure 2.41: Orthogonal array based on the Taguchi method. (Kaharudin et al., 2016)

Ergo, and according to this method, if both the mold and silicon thickness varied 5 % or 10 % of their initial respective thickness value, this would result in a study with different 2 factors, with

3 levels each, as shown in Table 2.2.

Table 2.2: Factors and levels for the warpage study analysis according to the Taguchi Method.

Factor	**Level 1**	**Level 2**	**Level 3**
1 - Mold Thickness (μm)	$POR(A/B)_{MT}$	$POR(A/B)_{MT}$ + 5 %	$POR(A/B)_{MT}$ + 10 %
2 - Silicon Thickness (μm)	$POR(A/B)_{ST}$	$POR(A/B)_{ST}$ + 5 %	$POR(A/B)_{ST}$ + 10 %

This means that 9 different experimental runs, for each product, would be needed to perform a comprehensive analysis of the influence of these factors, as illustrated in the orthogonal array matrix (L9 (3^2)), depicted in Table 2.3.

Table 2.3: Orthogonal matrix for the potential conducted experiments for the warpage study analysis.

Experiment	**Factor 1**	**Factor 2**
1	Level 1	Level 1
2	Level 1	Level 2
3	Level 1	Level 3
4	Level 2	Level 1
5	Level 2	Level 2
6	Level 2	Level 3
7	Level 3	Level 1
8	Level 3	Level 2
9	Level 3	Level 3

It is once again emphasized that albeit it is acknowledged that having these 9 experiments would be the most scientifically correct way to obtain accurate results, in an industrial setting and knowing the time restrictions imposed by the dissertation's period, it is not be feasible to perform these many experiments.

Chapter 3

Materials and Methods

This third chapter will start by thoroughly characterizing each studied material while highlighting their quantities and properties. In addition, it will provide a comprehensive overview of all warpage measurements and warpage correction techniques performed throughout this research period.

3.1 Materials

For the development of this work, two batches of wafers from two different front-end developers were used. Due to confidential reasons, these will be referred to as Material A and Material B for the remaining of this paper.

Even though the front-end specifications differ depending on the material being studied, they still have some common characteristics across them.

Amongst those is the fact all wafers will be 300 mm in diameter and will incorporate, throughout the packaging process, the same added components. This will include the use of the same epoxy mold compound, the use of silicon substrates with the same coefficient of thermal expansion value and the use of the same layering materials.

It is important to note that these layering material thicknesses, although slightly different from each other, will represent approximately 2-3 % of the POR_{MT} value.

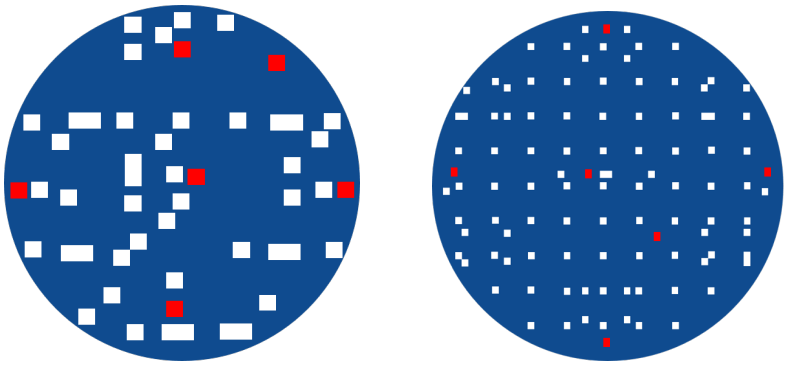
The specific details of each component can be read in the list below.

- The chosen mold compound will have a polymer-based matrix with a glass transition temperature between 160 ºC and 175 ºC. Moreover, its coefficient of thermal expansion will be 30 ppm/ºC above Tg and 7.5 ppm/ºC below it.
- The silicon substrate used will have a CTE equal to 2.7 ppm/ºC and will remain constant independently of the temperature used.
- The polyimide dielectric will have a glass transition temperature of 229 ºC and a coefficient of thermal expansion of 55 ppm/ºC. Details about this value below or above Tg are not disclosed.

Please note that for the simplification of the obtained warpage results, the glass transition temperature values of each material will be considered as a constant throughout the entirety of the packaging production process. While it is acknowledged that Tg may slightly vary depending on the manufacturing step, accounting for these variations would complicate the interpretation of the findings.

As seen in Figure 3.1, both selected materials will be fully populated materials, meaning that the wafers of each batch will be populated with functional dies (represented in white), blank silicon dies (represented in blue) and testing dies (represented in red).

Moreover, all these wafers will be full loop wafers, incorporating all the substrate layers a productive material would have.

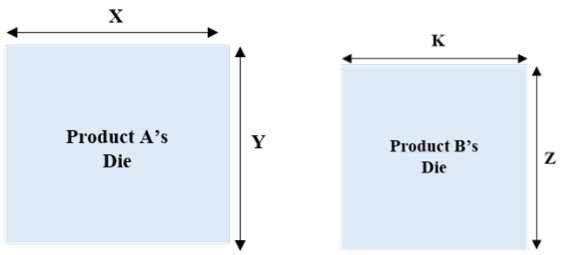


(a) Product A. (b) Product B.

Figure 3.1: Reconstituted wafer map of the different materials in which white represents the functional dies, blue represents the blank silicon dies and red represents the testing dies.

Material A will have 94.92 % of their total die count as blank silicon dies, 4.52 % as functional dies and 0.56 % as testing dies. On the other hand, material B's wafers will have 96.23 % of their total die count filled with blank silicon dies, 3.55 % filled with functional dies and 0.22 % filled with testing dies.

In addition, even though the size of each die can not be displayed, it is worth emphasizing that all types of dies will have identical dimensions within the same studied material. On the other hand, as observed in Figure 3.2, they will differ depending on the product, with product A having much superior dimensions.



(a) Product A. (b) Product B.

Figure 3.2: Die size of each material where Y > X > Z > K.

It is important to highlight that these wafer configurations were chosen using the minimum number of functional dies needed to correctly perform some of the steps throughout the packaging process (e.g. RDL steps). Moreover, selecting this minimum number of dies is a common practice at Amkor Technology Portugal during the setup phases of new products. Therefore, this will serve as an accurate simulation of a typical scenario in the semiconductor packaging industry.

At last, as said previously, filling the wafer with mostly blank silicon dies allows to perform these experiments without using any front-end manufacturer's productive material, while gathering the same results.

3.1.1 Experimental Runs

The first step conducted to assess the warpage behavior of these two materials consisted on defining the value of the varying parameter each experimental run would have.

Following the company's request and due to its known contribution to significant warpage levels, the chosen parameter was the EMC thickness. Hence, the silicon thickness will remain constant throughout the study.

It should be duly noted that given the limited flexibility to alter the silicon die thickness due to the known constraints from front-end developers regarding this matter, it is not as crucial to study this parameter, especially when only one parameter can be selected due to this dissertation's time restrictions.

Moreover, as said formerly in section 2.2, by varying the epoxy mold compound thickness value, there will naturally be an alteration both in the VOR percentages of each run and on the overmold thickness.

Over again, due to confidential reasons, the numerical values of the mold compound and silicon thickness cannot be disclosed and, as such, reference values for both of them were stipulated – the Process of Reference (POR) values.

Since they represent thicknesses frequently requested by the front-end developer, the mold compound POR value will have an increase by either 5 % or 10 %. Ergo, each material, for the analysis of the mold compound thickness influence, will encompass three legs.

Table 3.1 and Table 3.2 show the runs, now refereed to as legs, executed in each product and their respective characteristics.

Table 3.1: Legs of Product A and its respective characteristics.

	Material A		
	Mold Thickness (μm)	**Silicon Thickness (μm)**	**VOR (%)**
Leg 1	$POR(A)_{MT}$	$POR(A)_{ST}$	33.0
Leg 2	$POR(A)_{MT}$ + 5%	$POR(A)_{ST}$	31.4
Leg 3	$POR(A)_{MT}$ + 10%	$POR(A)_{ST}$	30.0

Table 3.2: Legs of Product B and its respective characteristics.

	Material B		
	Mold Thickness (μm)	**Silicon Thickness (μm)**	**VOR (%)**
Leg 4	$POR(B)_{MT}$	$POR(B)_{ST}$	54.2
Leg 5	$POR(B)_{MT}$ + 5%	$POR(B)_{ST}$	51.9
Leg 6	$POR(B)_{MT}$ + 10%	$POR(B)_{ST}$	49.8

To increase the reliability of results, it is important to note that Product A's legs will have 3 wafers each, while Product B's legs will have 2 wafers each. This discrepancy in the number of wafers present in each material is justified by the fact that the availability of Product A is much greater than Product B's availability.

Furthermore, 3 extra product B's wafers with the same characteristics as Leg 4 will be used to study the influence of the application of the first dielectric layer on warpage levels. This new leg will be refereed to as leg 7.

For an easier understanding of how each leg will be used to study these wafer characteristics' differences impact on warpage, refer to Table 3.3.

Table 3.3: Different studies conducted with Material A and B.

Legs used for comparison	**Objective**
Legs 1, 2 and 3	Study the influence of an increased mold thickness on warpage when the silicon thickness remains constant on Product A.
Legs 1, 2 and 3	Study the influence of an increased VOR percentage on warpage on Product A.
Legs 4, 5 and 6	Study the influence of an increased mold thickness on warpage when the silicon thickness remains constant on Product B.
Legs 4, 5 and 6	Study the influence of an increased VOR percentage on warpage on Product B.
Legs [1-3] and [4-6]	Study the influence of different ranges of temperatures, used in each specific step, on warpage.
Legs [1-3] and [4-6]	Study the impact of varying warpage correction techniques' temperatures and timings on warpage.
Legs 4 and 7	Study the influence of the application of the first dieletric layer on warpage.

3.2 Methods

This following section will explain, in detail, the methodology adopted for these experimental runs, including the steps where warpage was measured and the different warpage correction techniques applied during the packaging fabrication.

3.2.1 Warpage Measurement Techniques

The two materials will undergo the traditionally used ATEP's packaging process in their respective paths, previously explained in Section 2.1.1.1, with warpage measurements in between some specific steps.

Material A will follow Path 1, in which the wafers are submitted to an extra grinding step until they reach a pre-determined final thickness. Conversely, Material B will undergo Path 2, in which they are shipped directly to the front-end developer, without any extra grinding step.

For an easier understanding of the different steps where warpage will be measured and the different range of temperatures used in them (shown in more detail in Table 3.4), refer to Table 3.5 and Table 3.6, for Material A and B, respectively.

It is noteworthy that the warpage correction techniques, and consequent measurements, are not included in these tables as they may differ depending on the specific leg and material.

Table 3.4: Temperature ranges used for the analysis of the results.

Range	**Temperature (°C)**
Low	50 - 109
Medium	110 - 169
High	170 - 230

Table 3.5: Steps of measurement throughout the manufacturing process for Product A.

Step	**Brief Description**	**Layers on the wafer**	**Temperature Range**	**Temperature (°C)**
1A	Curing of the epoxy mold compound.	-	High	Tg + 15
2A	Cleaning of the surface of the wafer with the aid of plasma.	-	Low	Tg - 100
3A	Curing of the first dielectric layer.	DL1	High	Tg + 15
4A	Deposition of the seed layer.	DL1 + Seed Layer	Low	Tg - 55
5A	Cleaning of the surface of the wafer with the aid of plasma.	DL1 + Seed Layer	Low	Tg - 100
6A	Curing of the second dielectric layer.	DL1 + Seed Layer + DL2	High	Tg + 15
7A	Deposition of the second seed layer.	DL1 + Seed Layers + DL2	Low	Tg - 55
8A	Cleaning of the surface of the wafer with the aid of plasma.	DL1 + Seed Layers + DL2	Medium	Tg - 50
9A	Final grinding.	DL1 + Seed Layers + DL2	Medium	Tg - 40
10A	Reinforcing of the curing of the dielectric layers and drying of the wafers.	DL1 + Seed Layers + DL2	High	Tg + 50
11A	Application of the solder balls.	DL1 + Seed Layers + DL2	High	Tg + 55

Table 3.6: Steps of measurement throughout the manufacturing process for Product B.

Step	Brief Description	Layers on the wafer	Temperature Range	Temperature (°C)
1B	Curing of the epoxy mold compound.	-	High	Tg + 15
2B	Cleaning of the surface of the wafer with the aid of plasma.	-	Low	Tg - 100
3B	Curing of the first dielectric layer.	DL1	High	Tg + 15
4B	Deposition of the seed layer.	DL1 + Seed Layer	Low	Tg - 55
5B	Cleaning of the surface of the wafer with the aid of plasma.	DL1 + Seed Layer	Low	Tg - 100
6B	Curing of the second dielectric layer.	DL1 + Seed Layer + DL2	High	Tg + 15
7B	Deposition of the second seed layer.	DL1 + Seed Layers + DL2	Low	Tg - 55
8B	Cleaning of the surface of the wafer with the aid of plasma.	DL1 + Seed Layers + DL2	Medium	Tg - 50
9B	Reinforcing of the curing of the dielectric layers and drying of the wafers.	DL1 + Seed Layers + DL2	High	Tg + 50
10B	Application of the solder balls.	DL1 + Seed Layers + DL2	High	Tg + 55

Throughout these aforementioned measurements, if the warpage levels of solely one wafer out of an entire leg are deemed to be out of specification, the entire leg will undergo a warpage correction technique - following the cycle depicted in Figure 3.3.

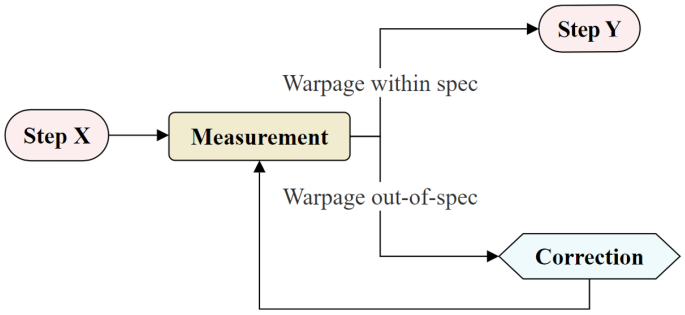


Figure 3.3: Flow of warpage correction techniques procedure.

Please refer to Table 3.7 for the specifications for each measurement taken with each equipment and measuring technique.

Table 3.7: Warpage measurements specifications.

	Minimum specification (mm)	Maximum specification (mm)
Nanofocus Measurement	-2.2	2.2
Sorter: Pre-Aligner Measurement	-3.5	3.5
Sorter: Plain Chuck Measurement	-2.2	2.2

These specifications were obtained by an analysis of the historical records of the two materials throughout the flow. According to these records, the specified values are the previous limit warpage levels that the wafers had while still being capable of going through the packaging flow.

Moreover, it is important to highlight that before the deposition of the seed layer, a warpage correction technique will always be conducted as it has been proven, prior to the dissertation's period, that formatting the wafers to a specific shape, even if these are inside the allowable limits, contributes to the minimization of warpage throughout the remaining of the packaging process.

At last, as mentioned before in Section 2.2.1, the Sorter equipment is able to perform the same Plain Chuck measurement as the Nanofocus equipment. Nonetheless, for this experimental study, both of these different types of measurements were conducted. This will not only increase the reliability of the obtained results but also allow to determine whether the results obtained with the manually operated machine can be considered dependable.

3.2.2 Warpage Correction Techniques

When it came to the warpage correction techniques applied if the warpage values were not within acceptable limits, different recipes were used throughout the process. While the specific characteristics of these recipes cannot be disclosed, Table 3.8 succinctly delineates them and the variations among them.

Table 3.8: Warpage correction recipes used in the warpage study analysis.

	Equipment	**Temperature (ºC)**	**Mode**
Recipe 1	A	Tg + 55	Automatic
Recipe 2	B	Tg - 5	Automatic
Recipe 3	A	Tg + 5	Automatic
Recipe 4	A	Tg + 15	Automatic

Upon showing the results, in the following section, it will be easily observed that several adjusts were performed. Table 3.9 shows which recipe was used in each adjust.

Table 3.9: Adjusts performed throughout the packaging process in the warpage study analysis.

Adjust Name	**Recipe**	**Product**	**Adjust Name**	**Recipe**	**Product**
Adjust 1 (A)	Recipe 3	A	Adjust 1 (B)	Recipe 1	B
Adjust 2 (A)	Recipe 3	A	Adjust 2 (B)	Recipe 1	B
Adjust 3 (A)	Recipe 4	A	Adjust 3 (B)	Recipe 1	B
Adjust 4 (A)	Recipe 3	A	Adjust 4 (B)	Recipe 2	B
Adjust 5 (A)	Recipe 4	A	Adjust 5 (B)	Recipe 2	B
Adjust 6 (A)	Recipe 2	A	Adjust 6 (B)	Recipe 2	B
Adjust 7 (A)	Recipe 2	A	Adjust 7 (B)	Recipe 2	B

Chapter 4

Results

4.1 Experimental results

This section will provide a comprehensive analysis of the acquired experimental results, using the methodology previously described, along with a thorough interpretation of the findings.

4.1.1 Analysis of the temperature impact on warpage levels

After gathering all the measured values throughout the packaging process for both products A and B, it became feasible to draw conclusions regarding the overall impact that different ranges of temperatures, used in the manufacturing steps, have on warpage and its shapes.

It is important to highlight that, as previously stated, multiple concurrent factors have an impact on warpage and as such, temperature will not be its sole determinant. Nonetheless, this experimental study will provide a general understanding of this temperature impact.

The collected measurements after each studied step were divided into three different categories - low, medium and high - based on the processing temperature used in each step (please refer to Table 3.4 for details on the temperature ranges used for this division).

Following this, all this data was inputted into the data analysis software, MiniTab, and the obtained results are present in Figure 4.1. Please be informed that, in this figure, the shown data accounts for all the measured warpage values of product A and B.

For an individual analysis of these products, consult Figure 4.2 and Figure 4.3.

With regards to the overall analysis of the products, the results went accordingly to what was expected. As previously explained, warpage mainly stems from the differences in the CTE values of the various adjacent materials present in the wafers. As such, and knowing that these CTE differences become more pronounced at elevated temperatures, it was initially presumed that higher temperatures would lead to higher warpage values.

As examined by plotting a mean line on all measured warpage values, for all three measurement techniques (Nanofocus, Sorter: Pre-Aligner and Sorter: Plain Chuck), an identical trend was consistently observed: higher processing temperatures culminated in higher warpage. Conversely, lower warpage values were obtained in steps that used lower processing temperatures.

Since all the steps within the high temperature range employ temperatures that are greater than Tg, contrary to the ones within the medium and low temperature ranges, it is possible to conclude that surpassing this value will, on average, lead to increased warpage values.

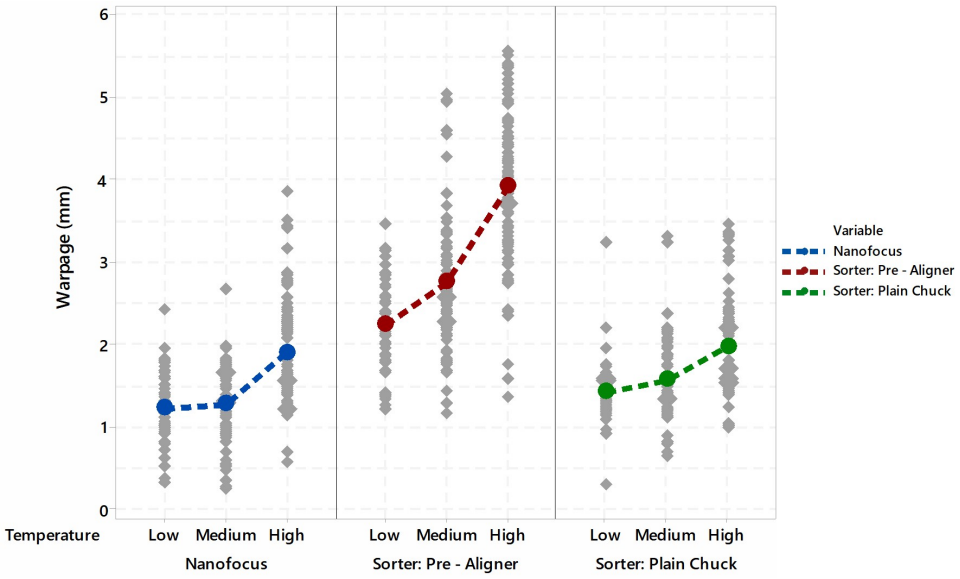


Figure 4.1: Results of the analysis of the temperature impact on warpage levels in both products.

Following this analysis, when individually evaluating each product, the prior mentioned trend was not entirely followed, particularly for Product A.

As shown in Figure 4.2, some unanticipated results arose in which low range processing temperature steps entailed higher warpage values than medium range temperature steps for the Nanofocus and Sorter: Plain Chuck measurements. Nonetheless, the highest warpage values were still recorded in the steps that employed temperatures within the high temperature range.

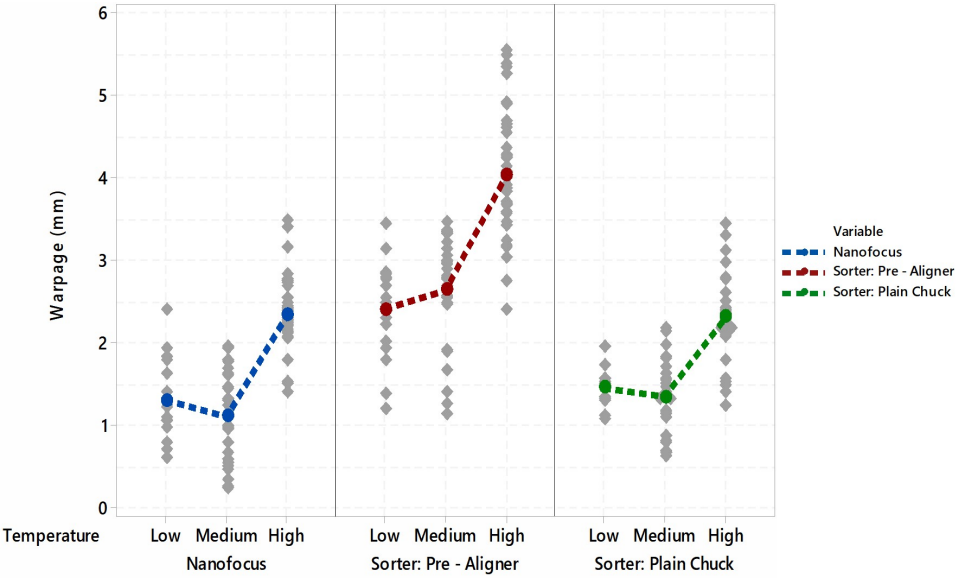


Figure 4.2: Results of the analysis of the temperature impact on warpage levels in Product A.

For Product B (Figure 4.3), the most interesting results came from the Sorter: Plain Chuck analysis. In this measurement, the warpage values gathered from high processing temperature steps were similar to those obtained from medium processing temperature steps.

The slight difference between them can be deemed negligible as there are a lot of noise factors, including the time windows between the execution of the step and its subsequent measurement, which might slightly influence these values.

At last, despite these unforeseen results, the highest warpage values were, irrespective of the measuring equipment, still obtained from steps that involved the highest processing temperatures.

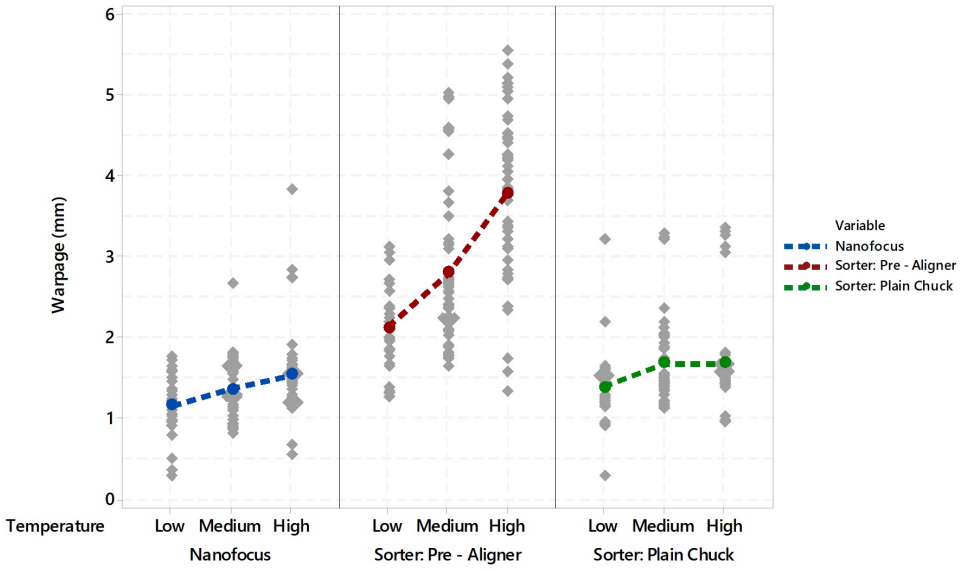


Figure 4.3: Results of the analysis of the temperature impact on warpage levels in Product B.

To sum up, and regardless of the fact that there was some discrepancy on the results depending on the product and the measuring technique, it is easily observable that higher warpage values typically stem from steps that employ higher processing temperatures.

4.1.2 Analysis of the addition of the first dielectric layer on warpage levels

In this conducted experiment, a comparison between two legs with the same wafer characteristics was executed to discern the influence of the addition of the first dielectric layer, a thin layer of a photoresist dielectric material, on warpage levels.

Leg 4 will encompass the average warpage measurements of its wafers with the addition of this layer, in each specific step of the beginning of the process, while oppositely Leg 7 will be the representation of the average results without it.

The expectations for this experiment were that the leg that entailed DL1 would have measured warpage values very similar to the leg that did not entail it.

This is given the fact that despite having a higher CTE, the dieletric layer's thickness will not be enough for it possess the ability to effectively expand/contract freely while moving the mold compound and silicon die in its expansion/contraction direction.

It should be noted that since the three different measurement techniques explained in Section 2.2.1 were executed, the acquired results with each one of them will be individually analyzed.

The results obtained with the Nanofocus equipment, illustrated in Figure 4.4, show that, independently of the leg being analyzed, the measured warpage values remain similar throughout the initial steps of the packaging process.

The slight divergence between legs, specifically after Step 1B, can be deemed as a measurement uncertainty triggered by the time discrepancy between the execution of the step and the measurement that follows. As an example, for Leg 4, this time windows was of 5 days. Contrarily, in Leg 7, this interval was only 2 days. This incongruity stems from the fact that, in an industrial setting, it is rather complicated to control the rhythm in which the experimental runs advance in the process.

Upon gathering the results after the application and curing of the first dielectric layer (After Step 3B), it is possible to observe that both studied legs exhibited similar warpage values. Therefore, it can be concluded that this layer has no significant impact, either negative or positive, on the warpage levels.

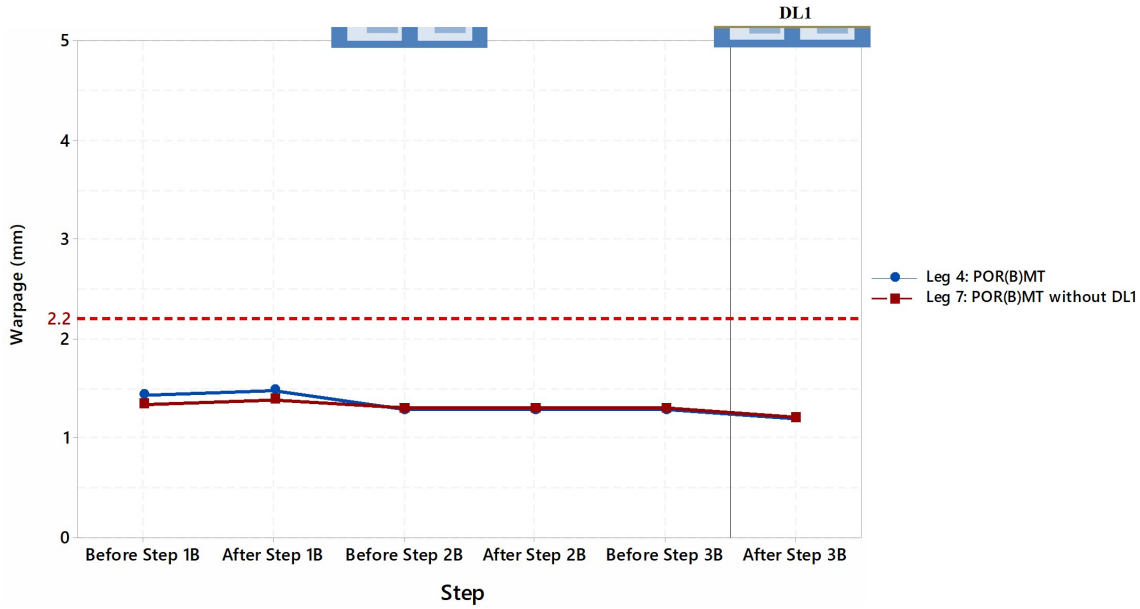


Figure 4.4: Nanofocus Warpage measurements results for the study of DL1 influence.

In contrast, the results obtained with the Pre-Aligner setting in the Sorter equipment (Figure 4.5), depict that both legs - with or without DL1 – only display akin warpage results up until they reach the execution of Step 2B.

After this step, the differences between the obtained values, between legs, can be justified by the fact that the measurements for Leg 4 had to be performed twice due to an equipment malfunction. As such, more time passed between the execution of Step 2B and the subsequent measurement.

After the deposition and curing of the dielectric layer (After Step 3B), the leg with the addition of the first dielectric layer (Leg 4) shows superior, and even outside of permissible limits, warpage values. These results were contrary to expectations as, theoretically speaking and previously mentioned, the leg that entailed the first dielectric layer should have warpage values very similar to the leg that did not entail it.

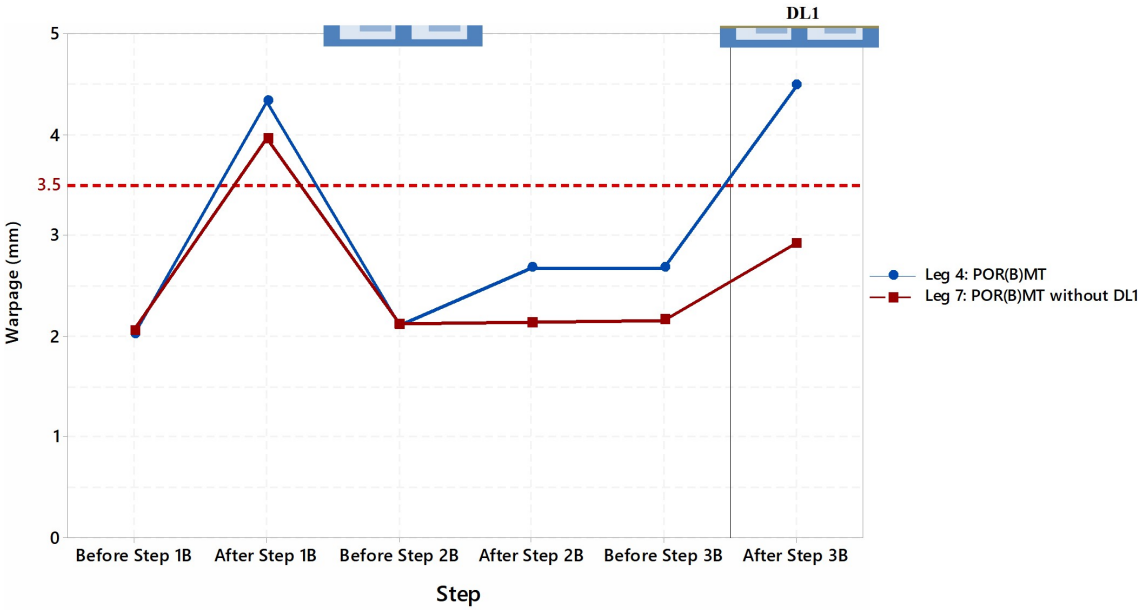
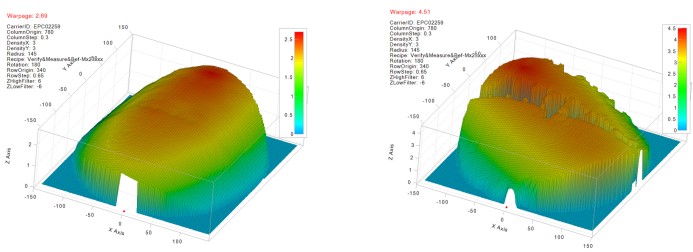


Figure 4.5: Sorter: Pre-Aligner Warpage measurements results for the study of DL1 influence.

Since by the sole observation of this graphical display, no conclusions were reached, Figure 4.6 and Figure 4.7, depict the 3D scanning of the wafers obtained with this measuring technique - before and after the curing of the wafers.

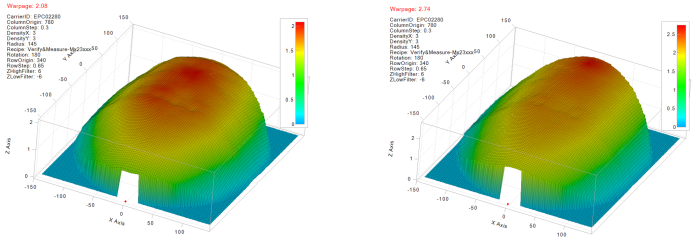
It was rather interesting to observe that the wafers that went through the curing process with the addition of DL1, displayed an irregular pattern with a line-like shape across their middle (Figure 4.8). This odd behaviour, stemming from a measurement error, where some warpage values were not recorded, can explain the discrepancies between the expected and obtained results.

Please note that these measurements were not able to be repeated, since the leg advanced to the next manufacturing step before the results could be interpreted.



(a) Before cure with DL1. (b) After cure with DL1.

Figure 4.6: Leg 4's Sorter: Pre-Aligner measurement scan results for the study of DL1 influence.



(a) Before cure without DL1. (b) After cure without DL1.

Figure 4.7: Leg 7's Sorter: Pre-Aligner measurement scan results for the study of DL1 influence.

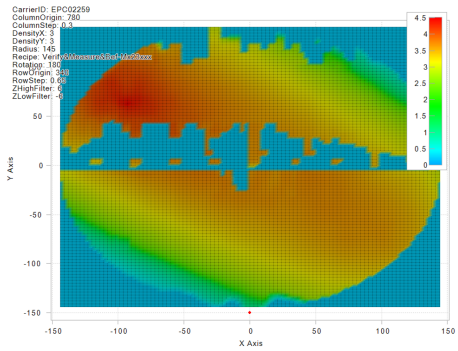


Figure 4.8: Leg 4's Sorter: Pre-Aligner scan results in a top view perspective.

Lastly, the results gathered from the Plain Chuck setting of the Sorter equipment (Figure 4.9), show that, throughout the entire process, the leg with the addition of DL1, had residually lower warpage values than Leg 7. These results went accordingly to expected and the minimal differences can, once again, be explained by the time windows between operation and measurement.

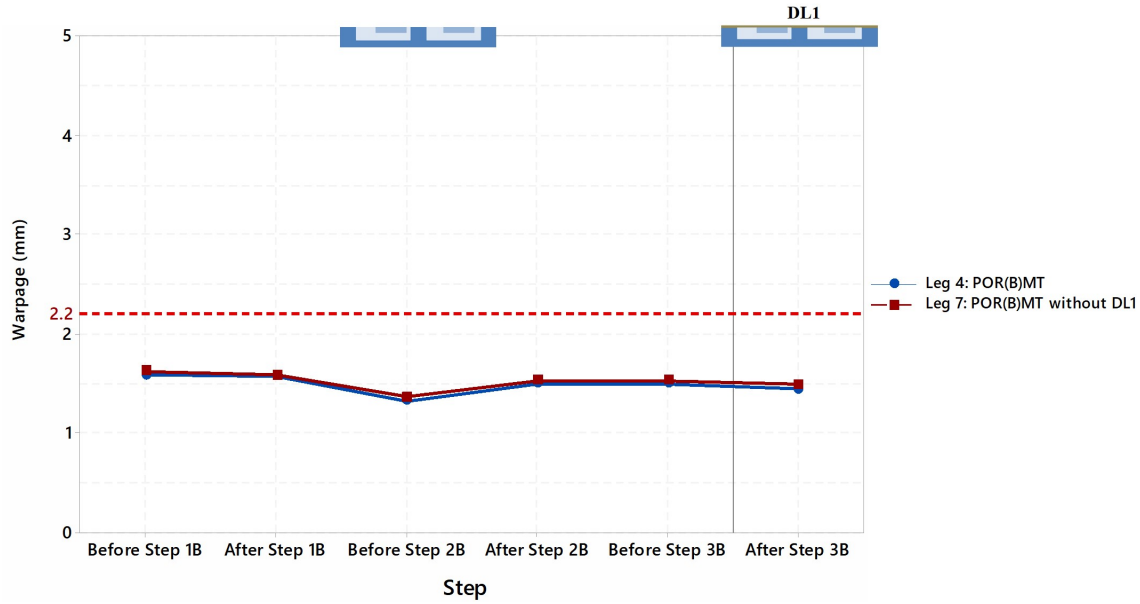


Figure 4.9: Sorter: Plain Chuck Warpage measurements results for the study of DL1 influence.

To review, the plain chuck measurements in both Nanofocus and Sorter demonstrate that the first dielectric layer has no noticeable influence, either positive or negative, on warpage. Therefore, these results demonstrate that its low thickness value is not yet enough to counteract the inwards contraction forces imposed by the mold compound. At last, results for the Sorter: Pre-Aligner measurements should be, as future work, repeated in order to validate their accuracy.

4.1.3 Analysis of the mold compound thickness and volume occupation ratio percentage impact on warpage levels

Through the collection of the measured warpage values, during the packaging flow, it became feasible to generate graphic representations of the materials warpage levels at each stage, depending on the different epoxy mold compound thickness of each leg.

It is important to note that in these graphics, each depicted leg will represent an average of the measured values obtained from the wafers of that leg.

It is also important to highlight that even knowing the warpage values measured with a specific equipment may be within specification, they might not be when measured with other equipment. Consequently, a warpage correction technique will still be executed.

In the graphical analyses, shown in the following sections, these instances are typically characterized by having a negative slope after the execution of a step. Please note that for an easier understanding on which steps warpage was not within acceptable limits in, at least, one of the measuring equipment, the graphics include a line beneath their names.

4.1.3.1 Product A

The measured warpage values of Product A, for each of the studied legs, obtained through the different measuring techniques, can be found in Figure 4.10, Figure 4.11, and Figure 4.12.

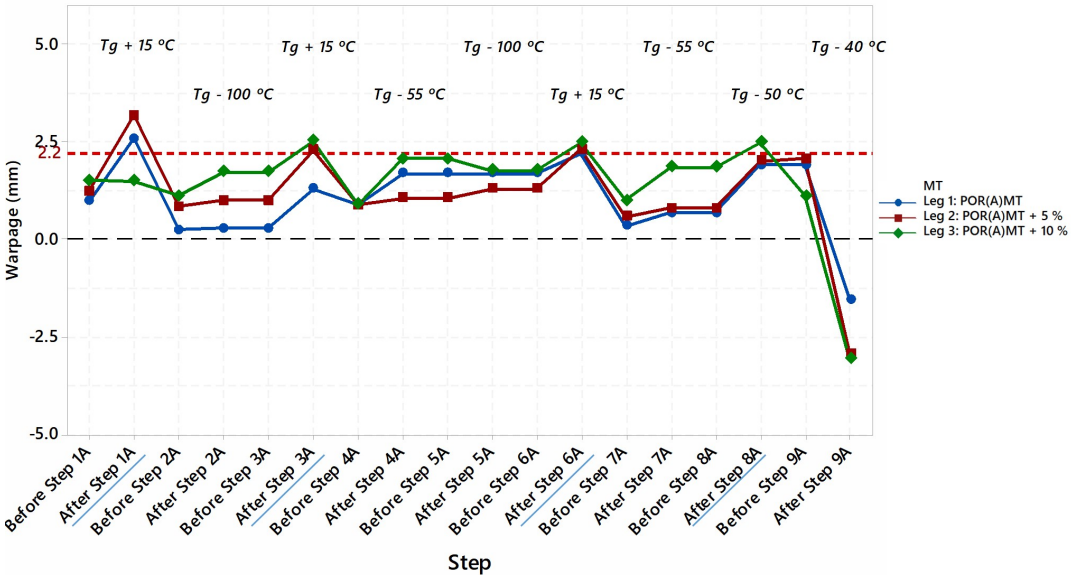


Figure 4.10: Nanofocus Warpage levels throughout the packaging process for Material A.

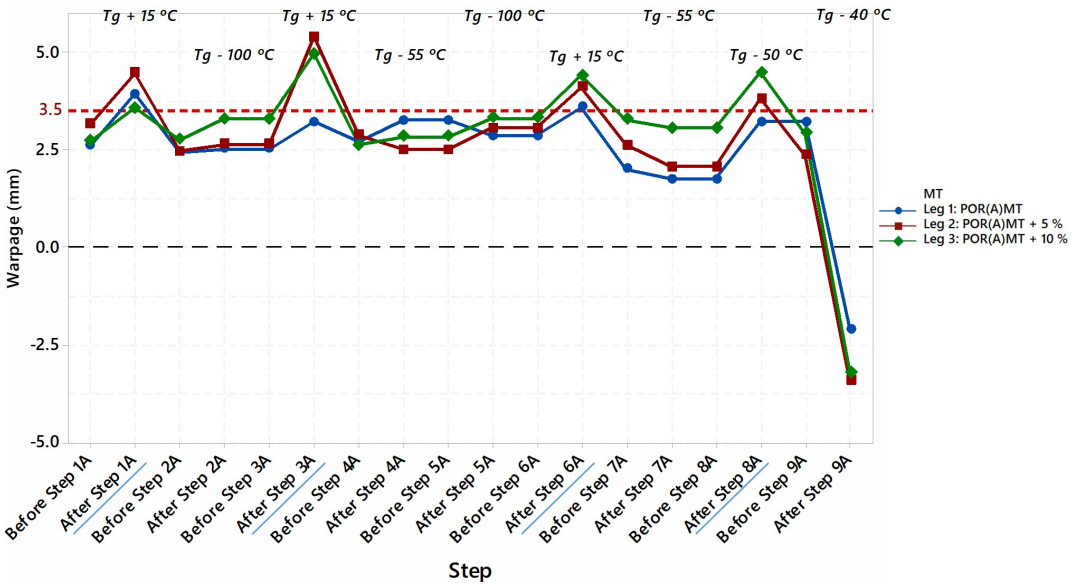


Figure 4.11: Sorter: Pre-Aligner Warpage levels throughout the packaging process for Material A.

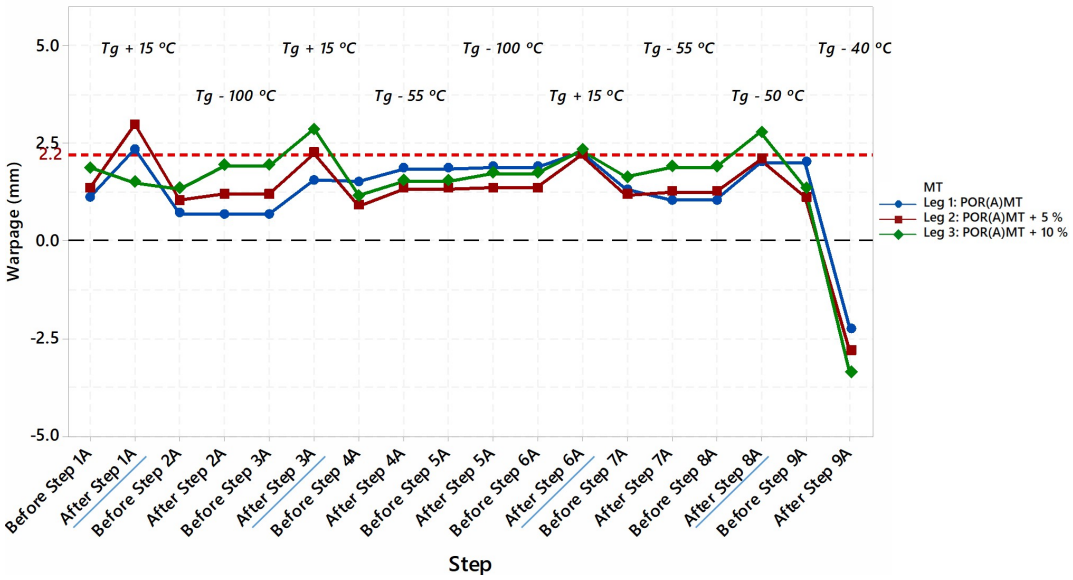


Figure 4.12: Sorter: Plain Chuck Warpage levels throughout the packaging process for Material A.

At first, it is important to note that this product did not complete the entirety of the manufacturing packaging process, stopping at Step 9A. This was due to the fact that this material became available later during the dissertation period, and due to the fact that, in industrial setting, it is challenging to control timings and to prioritize experimental activities over production activities.

Individually analyzing each step and measuring technique for each leg does not lead to any definitive conclusions. This is due to the fact that there are steps, depending on the measuring equipment, in which different mold compound thicknesses may be the most advantageous for minimizing warpage. Additionally, even when comparing the results obtained from the same

measuring equipment, the optimal mold compound thickness for minimizing warpage will also vary throughout the production process.

Since, before the grinding step - Step 9A, only one value of mold compound thickness can be used throughout the entire packaging process, an overall interpretation of the graphical data across the entire packaging process, was opted to be performed. This will be done by performing an analysis of the percentage of Product A's packaging process in which each leg exhibits the highest warpage value, depending on the measuring technique used.

The findings of this aforementioned analysis are shown in the list below.

- **Nanofocus Measurements:** Leg 3 had the highest warpage values throughout 88.89 % of the process, followed by Leg 2 with 11.11 % and Leg 1 with 0.00 %.
- **Sorter: Pre-Aligner Measurements:** Leg 3 had the highest warpage values throughout 55.56 % of the process, followed by Leg 2 with 27.78 % and Leg 1 with 16.67 %.
- **Sorter: Plain Chuck Measurements:** Leg 3 had the highest warpage values throughout 61.11 % of the process, followed by Leg 1 with 33.3 % and Leg 2 with 5.56 %.

As easily concluded, the leg that has a 10 % increase in their mold compound thickness (Leg 3) when compared to the POR_{MT} value, consistently displays the highest measured warpage values, regardless of the measuring technique used.

Moreover, regarding the choice of leg that is the most beneficial for minimizing warpage levels across Product A's production process, no definite conclusions were reached.

This is given the fact that different conclusions were gotten depending on the measuring technique utilized: if one takes into consideration solely the Nanofocus measurements, Leg 1 is the best at minimizing warpage levels; however if ones takes into consideration solely the Sorter: Plain Chuck measurements, Leg 2 is the most beneficial. In addition, the Sorter: Pre-Aligner measurements depict the same conclusions, regarding this matter, as the results obtained with the Nanofocus measurements.

It is important to note that the aforementioned findings allows to infer that the two measuring equipment (Nanofocus and Sorter), when measuring in the same Plain Chuck setting, may provide unakin measured warpage values - especially between Steps 4A and 6A. Please note small discrepancies between the obtained values with these two types of measurements were anticipated, mainly since they have a distinct quantity of measuring points. In addition, the timing between execution of the step and subsequent measurement is not equal in these two measurements, which contributes to these slight disparities.

To summarize the results, the gathered data indicates that using higher values of epoxy mold compound thicknesses, for Product A, will not be the optimal solution to minimize the warpage levels throughout the majority of the process. Thence, lower mold compound thickness values should be opted for. Please note that if a single process path must be chosen, Leg 1 should be selected for minimizing warpage levels, as two out of three measurement devices indicated this as the most beneficial option.

The last performed analysis related to having different mold compound thicknesses, will consist on studying the influence of varying volume occupation ratio percentages on warpage. There is a direct correlation between these two, as an higher mold compound thickness leads to a higher wafer volume (assuming the wafer's diameter remains constant), and consequently, a lower VOR percentage (according to Equation 2.1). Please refer to Table 3.1, for the VOR values of each leg.

Based on the conclusions drawn previously with regards to the influence of the mold compound thickness, it is evident that Leg 3 - which has the lowest VOR percentage (30.0 %) - will generally exhibit the highest warpage levels.

On the other hand, Leg 1, with a VOR percentage of 33.0 %, will typically show lower warpage levels throughout most of the packaging process, for the Nanofocus equipment. Contrarily, according to the results obtained with the Sorter: Plain Chuck setting, a VOR percentage of 31.4 % will be the optimal value to minimize warpage.

To recapitulate, a higher VOR percentage tends to correlate with lower warpage values. Ergo, the volume of the wafer should be as minimum as possible to achieve higher VOR percentages, and potentially reduce warpage.

4.1.3.2 Product B

The measured warpage values for Product B, in all three different measurement techniques, can be read in Figure 4.13, Figure 4.14 and Figure 4.15.

It should be duly noted that the rationale followed for Product A, will also be applied in this Product. That is, an overall interpretation of the attained data through the packaging process of Product B, will be opted to be performed. This interpretation will, once again, be done by analyzing the percentage of Product B's manufacturing steps in which each leg has the greatest warpage value, contingent on the measurement technique used.

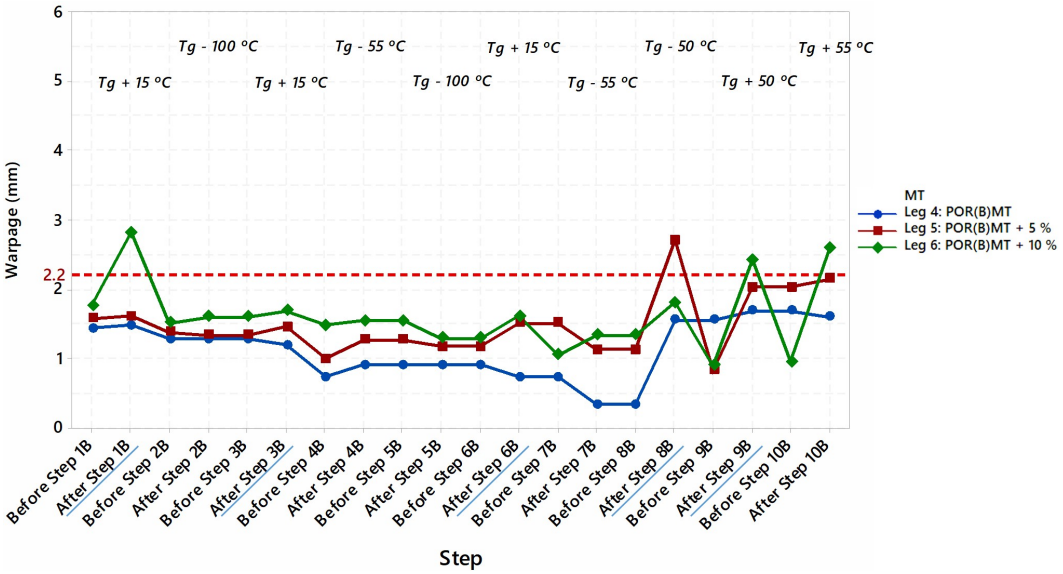


Figure 4.13: Nanofocus Warpage levels throughout the packaging process for Material B.

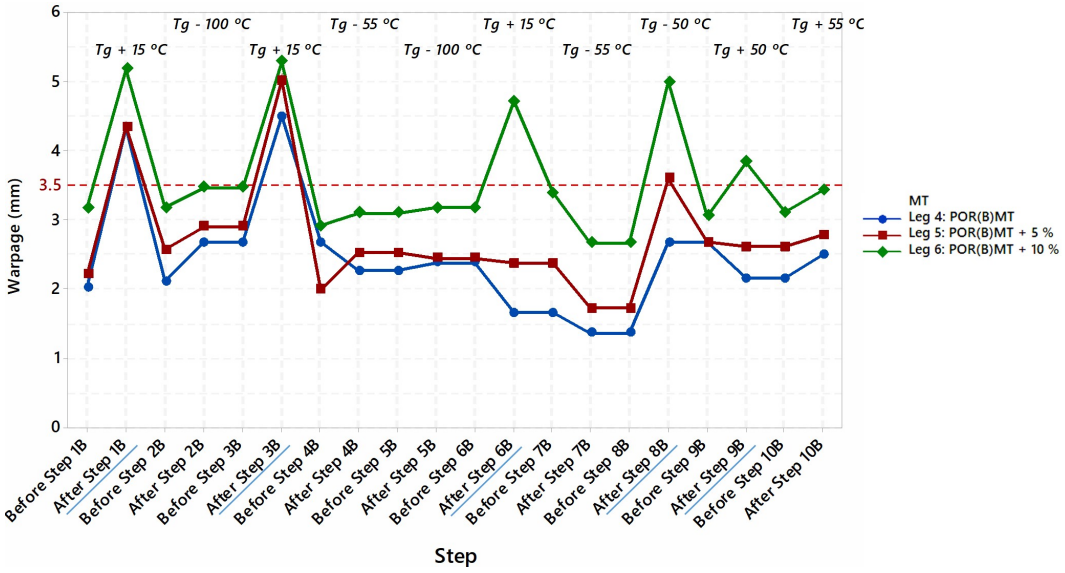


Figure 4.14: Sorter: Pre-Aligner Warpage levels throughout the packaging process for Material B.

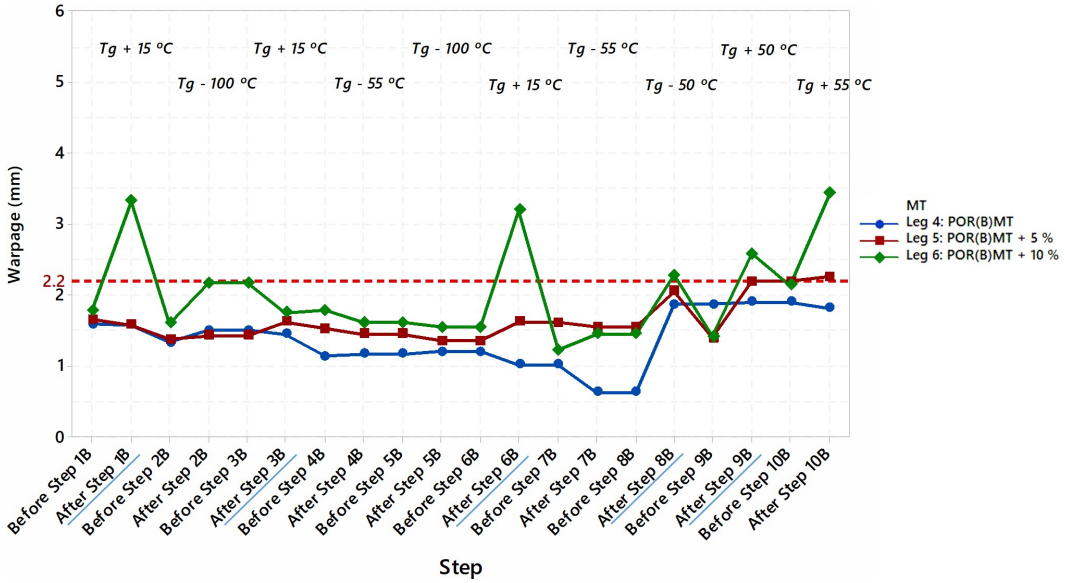


Figure 4.15: Sorter: Plain Chuck Warpage levels throughout the packaging process for Material B.

The results for the aforementioned analysis can be read in the list below.

- **Nanofocus Measurements:** Leg 6 had the highest warpage values throughout 80.00 % of the process, followed by Leg 5 with 15.00% and Leg 4 with 5.00 %.
- **Sorter: Pre-Aligner Measurements:** Leg 6 had the highest warpage values throughout 100 % of the process, followed by Leg 4 and Leg 5 with 0.00 %, each.
- **Sorter: Plain Chuck Measurements:** Leg 6 had the highest warpage values throughout 75.00 % of the process, followed by Leg 5 with 20.00 % and Leg 4 with 5.00 %.

Ergo, it becomes possible to conclude that the leg with the greatest mold compound thickness, Leg 6, exhibits the highest measured warpage values, independently of the measuring equipment.

Furthermore, when it comes to the leg of Product B that entails the lowest warpage values over the course of all the steps, and conversely to Product A, it was possible to reach some conclusions with regards to this topic. The results obtained from all three different measurements infer that Leg 4, the leg with the thinner mold compound, should be the chosen leg to obtain the lowest warpage values.

Regarding the previously made analysis of the discrepancy between the Nanofocus and the Sorter: Plain Chuck measured values, the same conclusions, when compared to the ones reached with Product A, were gathered. Therefore, one can state that, independently of the product, the reliability of the results obtained with these two techniques, seems to be very similar, with some differences between some specific steps.

To conclude, the gathered warpage data allows to state that using higher values of epoxy mold compound thicknesses, for Product B, is not the optimal solution to minimize the warpage levels throughout the majority of the process. On the other hand, using the thinner allowed epoxy mold compound thickness, is proved to be the most efficient method to do this.

As previously executed for Product A, the final analysis will consist on exploring the influence of the impact that having different volume occupation ratio percentages has on warpage.

As indicated, in Table 3.2, these percentages vary according to the leg being studied, with the leg that encompasses the highest mold compound having the lower VOR percentage.

From the conclusions previously gathered regarding the influence of the mold compound thickness, it is evident that Leg 6 - which presents the lowest VOR percentage (49.8 %) - will be the leg that overall, irrespective of the measuring technique, shows the highest warpage values. Conversely, Leg 4, with a VOR percentage of 54.2 %, will generally exhibit warpage levels throughout the majority of the process, with few exceptions.

To sum up, a higher VOR percentage tends to result in lower warpage values. This corroborates the results obtained with Product A, that the volume of the wafer should be ideally as small as possible to guarantee higher VOR percentages.

4.1.4 Analysis of the specific step impact on warpage levels

In this second analysis, the influence that each specific step and their distinct processing temperatures have on warapge will be thoroughly examined. Conversely to the analysis performed in Section 4.1.1, this analysis will focus on examining each specific step individually, rather than the overall range of temperatures used in each of them.

It is crucial to highlight that, as previously stated, warpage is highly influenced by a variety of concurrent factors, meaning that temperature alone does not dictate its outcome. As such, this analysis will also briefly explore the impact of having simultaneous factors - such as the different number of material layers in the wafer - on the warpage increment at each step.

This latter analysis will be possible since there are steps in the packaging process that share the same processing temperature but differ in layer count. Moreover, there are also steps that share the same amount of layers but differ on the processing temperatures.

In the graphical representations, that will be shown in the subsequent chapters, it will be possible to observe the warpage increment (in mm) before and after a specific process step throughout the entire packaging production process. Moreover, the temperatures at which each step is processed will also be indicated.

If needed, refer to Tables 3.5 and 3.6, for the meaning of each step, in Products A and B.

It should be duly noted that given the small sample size of this study, with only three or two wafers in each leg (depending on the product being analyzed), it was challenging to obtain consistent results with regards to the influence of each specific processing step.

The results revealed substantial variation not only between the various legs but also between measuring equipment. In fact, in some instances, completely different conclusions were reached for the same step due solely to the measuring technique utilized. In addition, similar contradictions were drawn depending on the specific leg under investigation, making it hard to reach definitive conclusions.

4.1.4.1 Product A

The warpage increment results obtained, for Product A, from the Nanofocus measureming equipment are depicted in Figure 4.16.

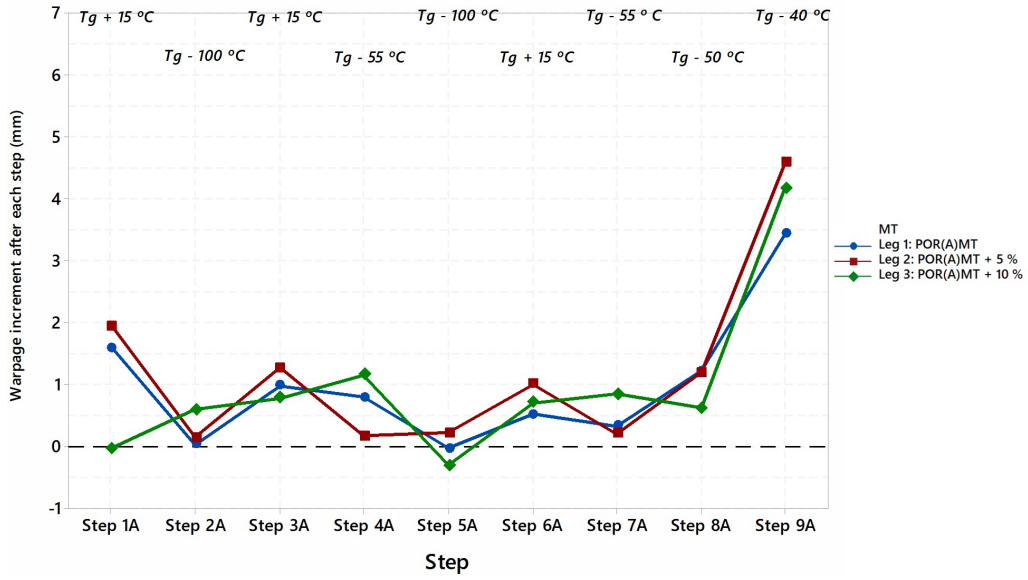


Figure 4.16: Nanofocus Warpage increment throughout Material A's process.

By analyzing these measurements' graphical representation, it becomes evident that, in Product A, there are some steps that showed an higher increment on warpage due to the temperature employed - specifically Steps 1A, 3A, 6A and 8A, and steps that showed an higher increment due to a reduction of the epoxy mold compound thickness - Step 9A.

These results, in Steps 1A, 3A and 6A, go according to expected, as these steps are steps in which a curing process is executed and temperatures above Tg are employed, leading to an higher mismatch of the different CTE of the materials.

Conversely, the results obtained for Step 8A were surprising given the fact that a step with such low temperature induced such significant levels of warpage increment. This was even more surprising particularly due to the fact that by the eighth step, two dielectric layers have already been already deposited on the wafers. Ergo, no entirely plausible explanation has been identified for this sudden spike in warpage increments.

The results obtained in Step 9A, which corresponds to the final grinding of the mold compound, also aligned with the previously held expectations. It should be noted that the increment in warpage during this step was substantial, but this is primarily due to the warpage shifting to a negative value. This observable phenomenon is understandable, as the dielectric layers will now be capable of exerting a greater force compared to the ones produced by the EMC, which now has a relatively smaller thickness. Consequently, in absolute terms, this step induces the most significant change in warpage, even causing the wafer to invert its shape from positive to negative.

Additionally, and still on this matter, although it is not the primary focus of this analysis, it was rather interesting to observe that the leg previously characterized by the lowest mold compound thickness (Leg 1) exhibited the smallest increment in warpage values after being submitted to this grinding process. This outcome aligns with expectations, as the thickness changes for this leg are less drastic. Consequently, with its prior layer thickness, the dielectric layers could already exert some force on the mold compound.

Thirdly, by the analysis of the obtained results, it is easy to conclude that, excluding some odd measured points, in Product A, Steps 2A, 5A and 7A (which employ a temperature equal to Tg - 100 ºC, Tg - 100 ºC and Tg - 50 ºC, respectively), showed the least increment in warpage levels. These results went accordingly to expected since lower temperatures would, according to theory, induce a lower CTE mismatch between the adjacent materials.

Furthermore, it was interesting to analyze that the influence of temperature on warpage decreases the more advanced the material is on the process.

This observation can be illustrated by comparing the results of Steps 1A, 3A and 6A, which have the same processing temperature but different amount of layers in the wafer. It is evident that the wafers in step 6, which includes the second layer, have a greater resistance to the increment on warpage levels, regardless of the studied legs.

Please note that the correction technique applied prior to Step 4A — regardless of whether warpage is within acceptable limits — appears to exacerbate the subsequent increment in warpage levels. The application of this correction technique seems to be the only plausible explanation, as temperatures very well below Tg, result in a significant and unexpected increase in warpage, after the execution of the step.

However, as will be discussed later, this warpage correction technique positively affects the shape of the wafer, which, in this case, is more critical than the numerical warpage values.

Additionally, it is crucial to highlight that the warpage increment observed with Leg 3, exhibits an unusual pattern when compared with the other legs after Step 1A. This discrepancy can be attributed to the fact that this particular leg underwent a warpage correction technique prior to the execution of this step as its warpage levels were outside of the permissible limits beforehand, whereas the other legs did not undergo such correction.

At last, this allows to infer that implementing a warpage correction technique prior to the curing of the epoxy mold compound could potentially reduce the increment in warpage at the beginning of the packaging manufacturing process.

The warpage increment results obtained in each step, for Product A, from the Sorter: Pre-Aligner measuring technique are depicted in Figure 4.17.

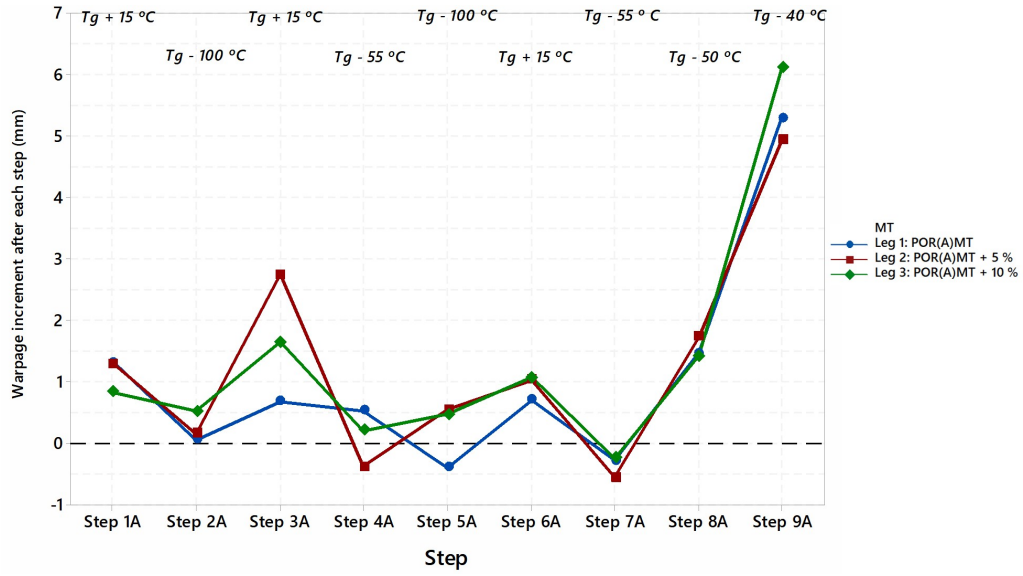


Figure 4.17: Sorter: Pre-Aligner Warpage increment throughout Material A's process.

With these, it is possible to infer that steps involving a temperature 15 degrees above Tg typically exhibited a higher warpage increment compared to those employing temperatures of Tg - 55 ºC and Tg - 100 ºC (with the exception, previously emphasized, for Step 8A).

With this technique, Steps 2A, 5A and 7A also encompass very little warpage increments, and consequently validate the aforementioned findings gathered with the Nanofocus device.

Additionally, steps that apply the same processing temperatures (when above Tg) later in the production process, also generally showed lower warpage increments (once again, with the exception of Step 8A). This is, once again, due to the higher quantity of material layers capable of counteracting the contraction forces acting upon the mold compound.

Moreover, an even higher warpage value, consistent with those typically observed using this measurement technique, was recorded following the execution of Step 9A. This reinforces that this particular step significantly impacts warpage and underscores the necessity for proper correction to facilitate subsequent steps, if the warpage values are outside the permissible limits.

It was also possible to gather that in Product B, Steps 2A, 4A and 5A (which employ a temperature equal to Tg - 100 ºC, Tg - 55 ºC and Tg - 100 ºC, respectively), showed the least increment in warpage levels. This corroborates the Nanofocus results obtained for these specific steps.

Some other significant findings emerged from these measurements.

Firstly, the warpage difference before and after the execution of each step 1A is now positive, which means the warpage, according to this measuring technique, increases. This difference between measurement techniques can be explained by the fact that, in this second measuring equipment, the wafer is only solely supported by a middle column, leaving its outer edges suspended. If the wafers are very flexible, then the measured difference between minimum and the maximum distance of the wafer to a reference plane will be higher.

Moreover, unlike the Plain Chuck measurements performed by the Nanofocus equipment, there is no abrupt and unexpected increment in warpage during Step 4A. In fact, Leg 2 even shows a decrease in warpage levels after this step. This indicates that the wafer's flexibility does not increase significantly in this step.

Please note that this does not imply the warpage levels are low in this step; rather, it highlights that the increment in warpage as the wafers go through this processing machine is minimal.

The third notable finding is that the wafers' flexibility decreases after Step 7A, regardless of the studied leg. This decrease correlates with the observed reduction in warpage increments after this step, implying that when measured using the middle column of this technique, the wafers bend less downward, thus indicating reduced flexibility or increased rigidity.

At last, the results gathered after the execution of Step 8A, serve as a confirmation of the sudden increase in the warpage values, previously obtained by the Nanofocus equipment. This indicates that the wafers after this step become highly flexible and could potentially be rather hard to handle and process, if not properly corrected.

Lastly, the results obtained with the Sorter: Plain Chuck are represented in Figure 4.18.

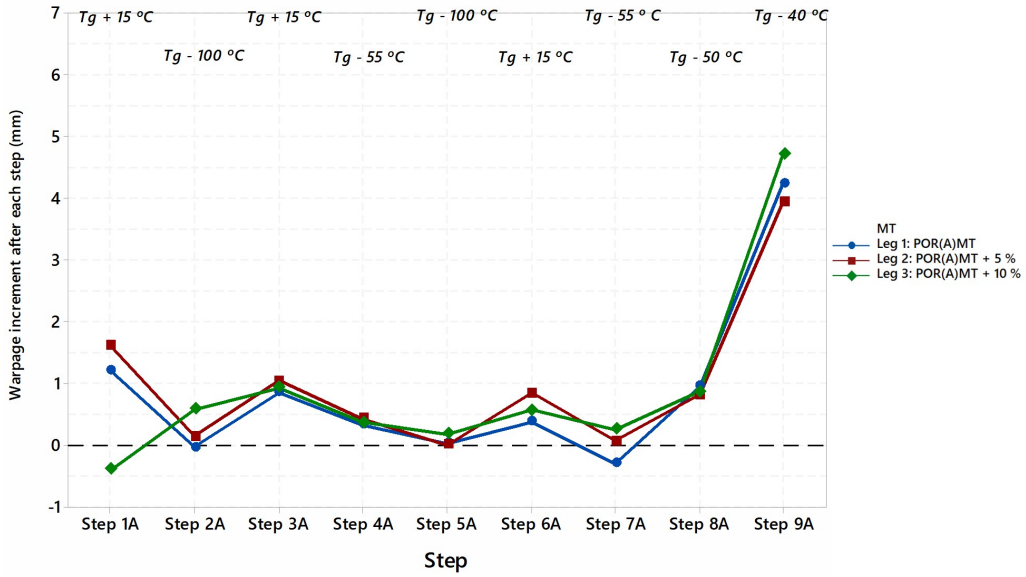


Figure 4.18: Sorter: Plain Chuck Warpage increment increment throughout Material A's process.

These results yield the same value as the Nanofocus measurements and additionally show more consistent findings across the different legs.

This allows to conclude that, in fact, across steps that apply temperatures above the glass transition temperature threshold, the increment in the measured warpage levels will be higher. In addition, the warpage increment will be noticeably lower in the later manufacturing steps, even when the same processing temperature is applied (once again, with an exception made for Step 8A and Step 9A).

Moreover, in these results, it is once again confirmed that steps in which the cleaning of the surface of the wafers with the aid of plasma at 100 degrees below the glass transition temperature is executed - Step 2A and Step 5A - show the least increment in warpage.

To sum up, the obtained results of which steps, on average, show the overall highest/lowest warpage increment whenever the wafers go through their processing machine, are represented in Table 4.1.

Table 4.1: Steps with the overall highest/lowest warpage increment for Product A.

	Steps with the overall highest warpage increment	**Steps with the overall lowest warpage increment**
Nanofocus	1A, 3A, 6A, 8A and 9A	2A and 5A
Sorter: Pre - Aligner	1A, 3A, 6A, 8A and 9A	2A, 4A and 5A
Sorter: Plain Chuck	1A, 3A, 6A, 8A and 9A	2A and 5A

Additionally, please refer to Appendix A.1 - Table A.1, Table A.2 and Table A.3 - to review the specific numerical values utilized during the development of the aforementioned graphical representations.

4.1.4.2 Product B

The warpage increment results obtained in each step for Product B, from the different measurement techniques: Nanofocus, Sorter: Pre-Aligner and Sorter: Plain Chuck, are depicted in Figure 4.19, Figure 4.20, and Figure 4.21, respectively.

When comparing to Product A, the results obtained with this product were far more challenging to extract conclusions from since there is a much greater dispersion of results, for all the different measurement techniques.

These challenges first began when analyzing the warpage increments obtained by the Nanofocus equipment - shown in Figure 4.19 - as no noticeable trends were observed amongst them.

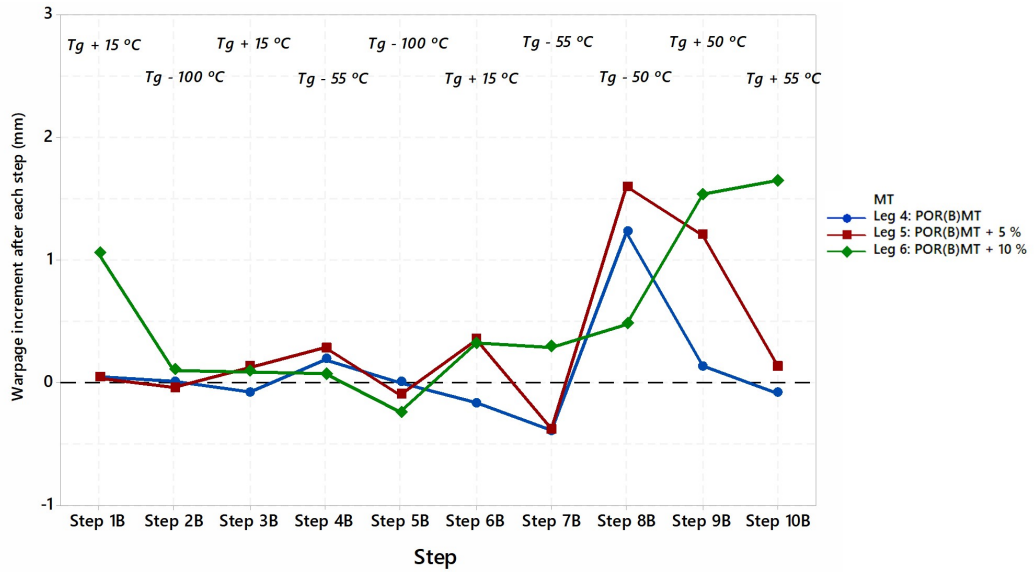


Figure 4.19: Nanofocus Warpage increment throughout Material B's process.

Firstly, it is important to note that it was interesting to depict the difference between legs in Step 1B, as this step does not seem to have any influence on two of the legs: Legs 4 and 5. Since this is the step in which the curing of the mold compound occurs, it is logical that legs with more mold exhibit a greater increase in warpage due to the associated effects of the curing process and increased appearance of stresses. Nonetheless, such big differences between warpage increment, respective of the leg, were not anticipated.

In addition, it was intriguing to perform a closer analysis on some steps, specifically Step 8B, Step 9B and Step 10B. These steps deviate from the general trend of the majority of the packaging steps showing similar increments on warpage levels, while simultaneously showing unexpected results.

As observed in Product A, in Step 8B, executed well below Tg and in which the wafers already have the two dielectric layers on them, an excessively high increment on warpage was, once again, observed, particularly pronounced in Leg 5. This supports the results from Product A, indicating that this step does significantly increase the warpage levels within the reconstituted wafers.

Furthermore, in the subsequent Step 9B, which employs temperatures 50 degrees above Tg, there was an unexpectedly lower increment in warpage observed in two of the legs (Legs 4 and 5) compared to the previous Step 8B. An explanation for these results was sought and it was concluded that the abrupt thermal shocks in Step 8B contribute significantly to the observed warpage. In Step 8B, wafers are not gradually heated to a specific temperature, leading to sudden thermal stress. Conversely, in Step 9B, there are five distinct heating stages, which impose a much slower heat transfer to the wafer, leading to a reduction in the thermal stresses, thereby minimizing the resulting warpage increment, even when submitted to temperatures 100 degrees greater than the previous step.

Please note that an aspect that goes accordingly to expected in this aforementioned Step 9B

is that the leg with the lowest mold compound thickness (Leg 4), better resisted a warpage increment, as its thinner mold compound allowed the dielectric layers to exert more force on the wafer, flattening them out more.

Moreover, in Step 10B, it is worth noting that this step, which employs 5 additional degrees than the previous one, shows a significantly lower increase in warpage levels for two of the studied legs, particularly relevant in the second leg. Conversely, the increment of warpage, in this step, in Leg 6, will be higher than in the previous step.

This last mentioned discrepancy between legs was firstly attributed to the fact that this leg underwent a warpage correction technique after Step 9B, whereas the other legs did not. Nonetheless, it is noteworthy that the reduction in warpage observed for Legs 4 and 5 was unanticipated when compared to the preceding step, given its similar processing temperatures and gradual heating.

To corroborate this hypothesis that submitting legs to a warpage correction technique, after a specific process step, may culminate in them having a higher warpage increment in the subsequent step, additional instances were identified where only one out of the three studied legs underwent such correction techniques.

As such, Step 6B can be used as another example, in which Leg 6 was the sole leg subjected to a warpage correction technique. As can be observed, in Step 7B, this leg did not show a higher increase in warpage compared to the previous step, thereby disproving the hypothesis.

To conclude the analysis performed with this measurement equipment, it is possible to infer that, generally speaking, Steps 8B and 9B will lead to the greatest warpage increments, whereas Steps 5B and 7B will lead to minimal warpage increments.

Moving on to the analysis of the results obtained with the Sorter: Pre-Aligner measurements, shown in Figure 4.20, markedly different results were gathered.

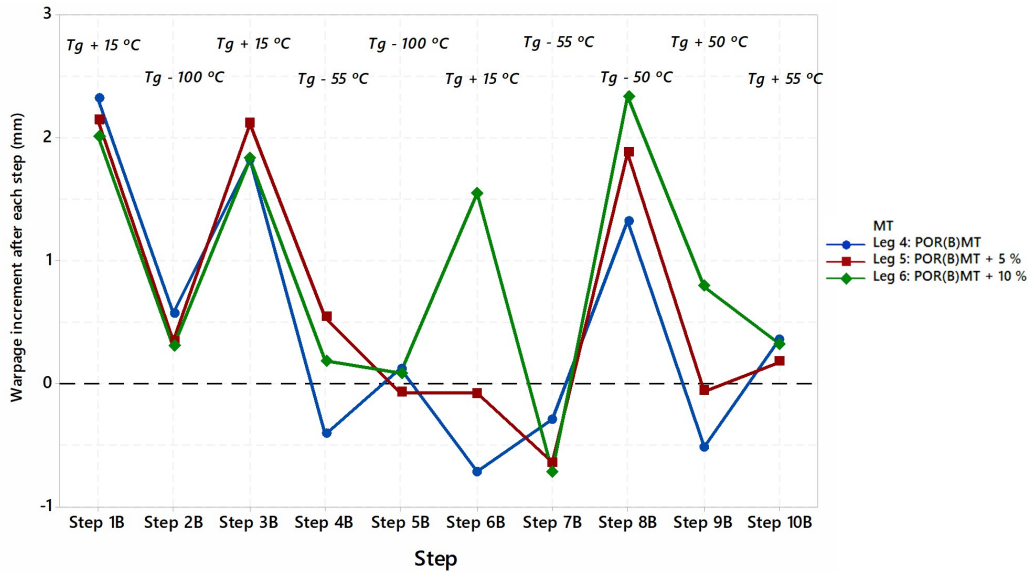


Figure 4.20: Sorter: Pre-Aligner Warpage increment throughout Material B's process.

At first, it is evident that until the application of DL1 (Step 3B), there is a clear trend: steps

that employ temperatures above the Tg value, lead to a greater increment in warpage. However, upon the application of the first dielectric layer, this trend is no longer apparent.

Regarding the analysis previously made for Step 8B, these measurements confirm that there is indeed a warpage increment in this step and once again, Legs 4 and 5 show a lower increment in the subsequent step. Surprisingly, and contrary to the Nanofocus results, the leg with the highest mold compound thickness also exhibits a lower increment in Step 9B.

As such, since this measuring techniques correlates with flexibility, it can be inferred that Step 8B will generate very high flexibility on the wafers, when compared to earlier steps.

In Step 10B, which employs even greater processing temperatures, the warpage increment is lower, when compared to the previous step, for Leg 6. For the other two legs, the temperature effect is more pronounced, resulting in a slightly larger increment in warpage. These results are the complete opposite when compared to the previously obtained ones with the Nanofocus equipment.

In addition, the conclusion that submitting legs to a correction technique will result in it having a higher warpage increment in the subsequent step is also not supported by the findings provided by these measurements. As an instance, after Step 9B and a warpage correction technique, Leg 6 does not exhibit a higher increment in warpage in Step 10B.

To summarize, no clear trends were able to be observed in this analysis. However, it can be stated that the addition of dielectric layers tends to introduces uncertainty regarding the expected results at each processing step.

Finally, the results obtained with the Sorter: Plain Chuck measurements (depicted in Figure 4.21) are closely akin with the exception of some odd points, to the results of the Nanofocus measurements until Step 6B. The sudden unexpected high warpage increment, for Leg 6, in this step, seems to have no scientific explanation and can be attributed to measurement uncertainty.

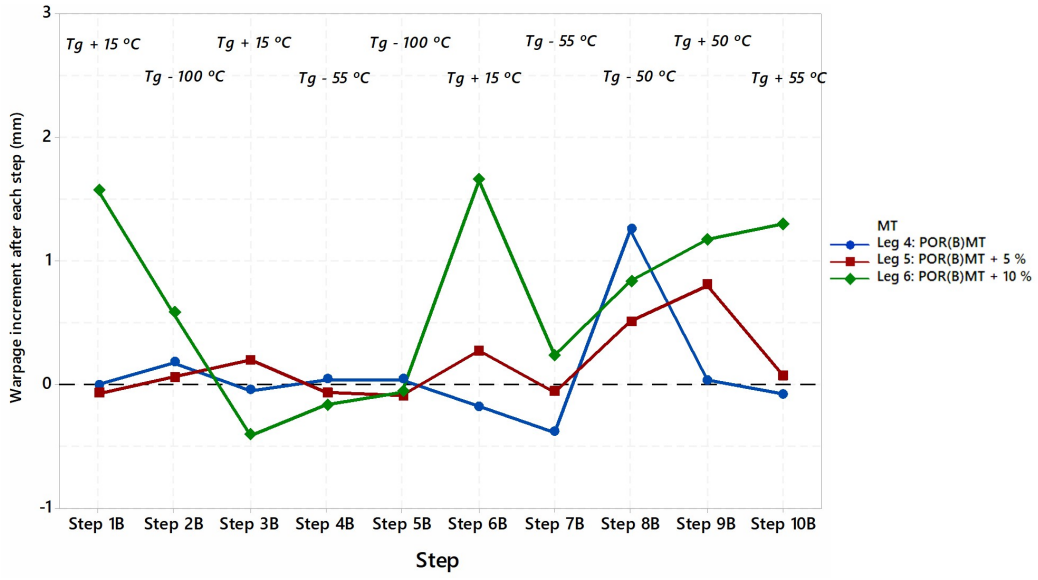


Figure 4.21: Sorter: Plain Chuck Warpage increment increment throughout Material B's process.

When considering the results with the lowest warpage increment, the data obtained with this

device differed markedly from the previously mentioned results. Specifically, Steps 3B, 4B, and 5B had the least impact on warpage. This was particularly surprising for Step 3B, where the curing of the wafers was performed 15 degrees above the glass transition temperature.

Moreover, in Step 8B, the same Nanofocus and Sorter: Pre-Aligner trend is observed despite with a different arrangement of the legs, though this aspect is not the focus of this analysis.

In addition, in Step 9B, two legs show an increase in warpage when subjected to temperatures 50 degrees higher than the mold compound's Tg, contrary to just one leg showing an increase in the Nanofocus equipment.

At last, in Step 10B, Leg 6 is the sole leg that when submitted to even higher temperatures, exhibits an higher increment of warpage. In contrast, the other two legs demonstrate a reduction in warpage increment under similar conditions. These findings completely align with the obtained ones from the Nanofocus equipment and contradict the previously mentioned hypothesis that performing a warpage correction technique will lead to an even higher increase in warpage in the subsequent step.

To summarize, the analysis of the specific steps' impact on Product B was rather inconclusive. Few conclusions could be drawn since the gathered data points failed to demonstrate any noticeable patterns that could lead to a solid conclusion. As such, this process can be said to have a very high degree of randomness, that most likely derives from the limited number of samples.

The acquired findings, while not definitively conclusive, suggest that certain steps notably increment warpage when processing wafers using the dedicated equipment, whereas other steps have less impact.

For a succinct description on which steps increase or decrease warpage, please refer to Table 4.2.

Table 4.2: Steps with the overall highest/lowest warpage increment for Product B.

	Steps with the overall highest warpage increment	**Steps with the overall lowest warpage increment**
Nanofocus	8B and 9B	5B and 7B
Sorter: Pre - Aligner	1B, 3B and 8B	7B
Sorter: Plain Chuck	8B and 9B	3B, 4B and 5B

Please refer to Appendix A.1 - Table A.4, Table A.5 and Table A.6 for the numerical values used for the elaboration of the aforesaid graphical plots.

4.1.5 Analysis of the application of warpage correction techniques on warpage levels

This next section will delve into the impact that each different warpage correction technique had on the proper decrease of the warpage levels, when needed.

The insights that are hoped to be extracted with this analysis include: whether there is a direct correlation between the degrees of temperature used in each correction and the decrease in the

warpage levels; how the same warpage correction technique impacts warpage levels differently, within the same leg, depending on where they are in the manufacturing process and lastly, whether it is possible to standardize the usage of solely one correction recipe, in each equipment, for a certain product.

Graphical analysis with the data collected from the different measuring techniques were elaborated, on MiniTab, to illustrate the warpage increase or decrease resulting from each of the performed adjusts, with the corresponding temperature indicated next to it.

Please note that whenever the temperature is represented in black, it indicates that the correction technique was performed with Equipment A. On the other hand, if the temperature is shown in red, it indicates that the correction technique was performed with Equipment B.

Additionally, take into consideration that each adjust was applied during different stages of the process, where the product had a varying number of layers. Therefore, once again, the temperature used in each recipe will not be the only factor contributing to the increase or decrease in warpage.

At last, it is important to emphasize that although the average of warpage in a leg may have been within acceptable limits, one sole wafer may not be. As such, this wafer is sufficient to submit the entire batch of wafers to a correction technique. Additionally, please note that one measurement technique providing out of specification warpage values, is also enough for the leg to undergo a warpage correction technique.

4.1.5.1 Product A

This analysis will start by identifying the steps in which a certain correction technique had to be applied in, for Product A. Please refer to Table 4.3 for an easier understanding of these steps.

It is important to highlight that Adjust 1 (A) is not refereed to in Table 4.3, since it was executed prior to the commence of the gathering of the results. Nonetheless, since it was proved that it had an impact on warpage increments (in Section 4.1.4.1), it was opted to still be mentioned.

Additionally, when two adjusts are performed within the same step, for the same leg, it means the first adjust was not efficient at decreasing the warpage levels to acceptable limits.

Lastly, please note that an adjust after Step 9 was not conducted due to the time constraints imposed by the dissertation period. This adjust should have been performed given that, as previously stated, the warpage values after this step exceeded the permissible limits.

Table 4.3: Steps in which Product A was submitted to a warpage correction technique.

	Leg 1	**Leg 2**	**Leg 3**
After Step 1A	Adjust 2 (A)	Adjust 2 (A)	Adjust 2 (A)
After Step 3A	-	Adjust 3 (A)	Adjust 3 (A)
Before Step 4A	Adjust 4 (A)	Adjust 4 (A)	Adjust 4 (A)
Before Step 4A	-	Adjust 5 (A)	Adjust 5 (A)
After Step 6A	Adjust 6 (A)	Adjust 6 (A)	Adjust 6 (A)
After Step 8A	-	Adjust 7 (A)	Adjust 7 (A)

As observed, the amount of correction techniques applied in each leg were not the same. The legs that encompassed the highest mold compound thicknesses, Legs 2 and 3, presented the higher number of correction techniques - six - whereas, conversely, Leg 1 only had three adjusts.

An individual analysis of the warpage values, before and after a specific correction technique, collected through the different equipment will be performed.

Please refer to Appendix A.2, for the actual data used for the development of the following graphical representations

The results obtained from the Nanofocus measurements (Figure 4.22), show an interesting trend. The same adjust is more effective for wafers that have the thinnest mold compound layer (the POR_{MT} value), as evidenced by Leg 1 constantly displaying the highest warpage decrease when subjected to the same adjust.

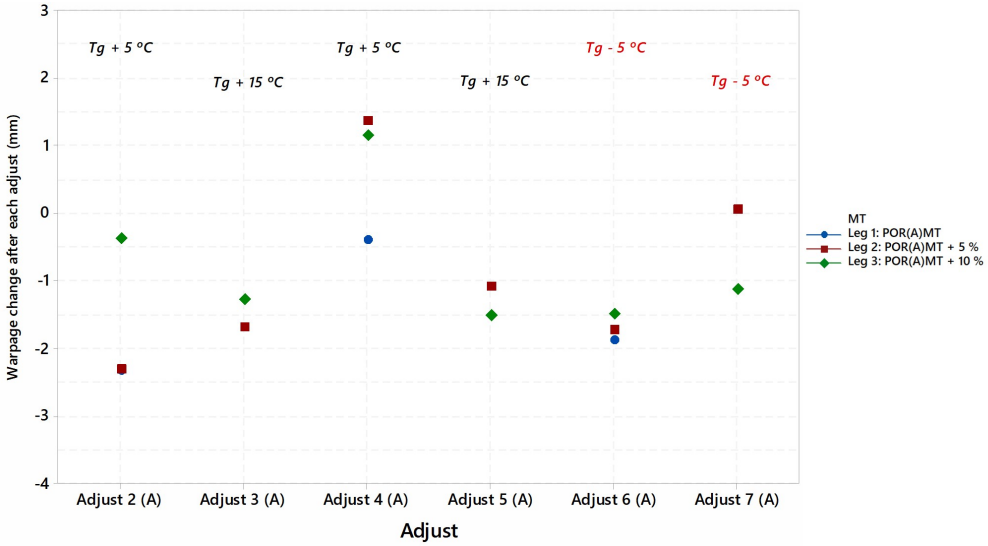
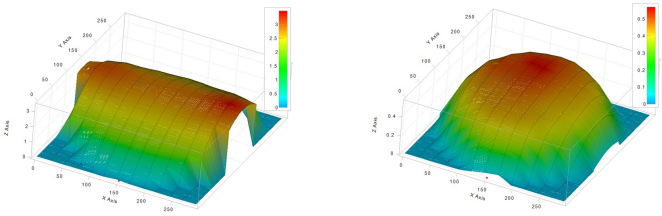


Figure 4.22: Nanofocus warpage change after the application of warpage correction techniques for Product A.

Additionally, it was also intriguing to observe that the correction technique applied before the Step 4A - despite the warpage values being within specification prior, but necessary for reasons mentioned in Section 3.2.1 — led to an increase of warpage for both Leg 2 and Leg 3. Nevertheless, as seen in Figure 4.23, the desired shape for the remainder of the process was achieved.



(a) Before adjust. (b) After adjust.

Figure 4.23: 3D Nanofocus scan of Leg 2 wafers - before and after Adjust 4 (A). (ATEP, 2024)

Moreover, the fourth performed adjustment (Adjust 5 (A)), executed to bring the warpage levels within acceptable limits after the application of Adjust 4 (A), proved to be efficient in doing so. This brings some insights into the fact that applying a warpage correction technique with solely 10 more degrees, when the product is at the same process stage, can have a vastly different impact on warpage.

Please note that to further confirm this hypothesis, tests should be conducted where wafers, immediately before Step 4A, are subjected to this recipe with an additional 10 degrees. Otherwise, the effect of the initial warpage correction might influence the observed improvement in the second adjust.

Regarding the analysis of temperature impact on wafers with the same layers on adjusts with varying temperatures, no definitive conclusions could be drawn. The only steps in which this could be compared was between Adjusts 3 (A) and 4 (A) and Adjusts 4 (A) and 5 (A). These adjusts were not considered fit for this analysis since Adjust 4 (A) was performed on wafers with warpage values within specification.

Additionally, the only two adjusts that could be used to compare the impact of having different numbers of layers on warpage reduction when subjected to the same temperature in the same equipment were Adjust 2 (A) and Adjust 4 (A). Due to the aforementioned reasons, this analysis will also not be conducted.

Moreover, as observed, the single recipe, used through the entirety of the warpage correction techniques performed in Equipment B, was generally capable of decreasing the warpage values down to acceptable limits. On the contrary, Equipment A required two distinct recipes. It is important to highlight that Adjust 3 (A)'s recipe was selected based on prior evidence, established before the dissertation period, that Recipe 3 would not be effective.

The anomaly point presented in Adjust 7 (A) - Leg 2 - was, once again, due to the fact that there was a large time window between the application of the warpage correction technique and the subsequent measurement. Nevertheless, they remained within valid specifications and the correction technique was considered successful since the warpage decreased when measured with the Sorter: Pre-Aligner method (which will be elaborated further on).

Ergo, based on these Nanofocus findings, it is apparent that definitive conclusions regarding the impact of varying temperatures were not established. This ambiguity may stem from an insufficient number of data points or the minimal number of adjusts required during the packaging manufacturing of Product A.

Please note that since these results were rather inconclusive regarding some matters, an alternative approach was explored, in which the difference in warpage post-adjust relative to the warpage value before adjust was graphically plotted.

The results can be seen in Figure 4.24.

As observed, the results obtained were very similar to the previous ones, and no further conclusions could be reached. It is noteworthy that across the three measurement types, certain warpage correction techniques achieved a reduction in initial warpage values by almost 90 %. Moreover, the

majority of adjusts - excluding a few observed anomalies - consistently demonstrated a warpage reduction exceeding 50 %.

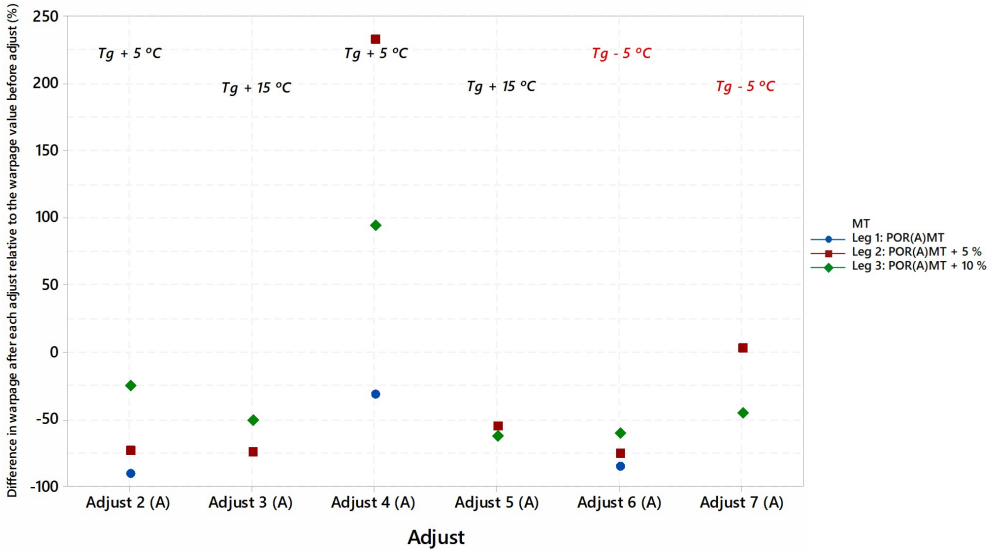


Figure 4.24: Nanofocus warpage difference after each adjust relative to the warpage value before adjust for Product A.

Secondly, with regards to the results obtained with the Sorter: Pre-Aligner measuring technique, depicted in Figure 4.25, it can be asserted that similar findings were obtained in a broader scale, as this measuring technique tends to record higher warpage values.

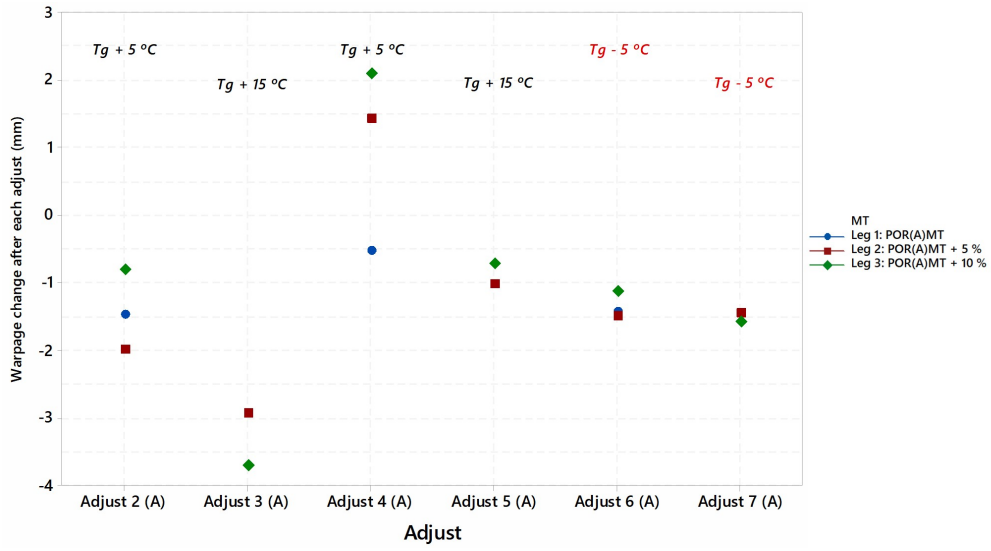


Figure 4.25: Sorter: Pre-Aligner warpage change after the application of warpage correction techniques for Product A.

As noted, the adjusts were typically more effective for legs with a thinner mold compound, particularly the one with the POR_{MT} mold thickness value. An exception was observed in Adjust 2 (A), which derived from the fact that, contrarily to other legs, more time elapsed between the

execution of the warpage correction technique and the subsequent measurement. In Leg 2, after Adjust 2 (A) this interval was only 31 minutes, compared to 7 hours for Leg 1.

This brings some insights at the fact that warpage is not constant and can vary even when wafers are not subjected to any temperatures and are simply waiting for the next manufacturing step. Thence, this proves that expediting the process and performing the processing steps within known time windows will be crucial to the decrease of warpage throughout the process.

Furthermore, the same results concerning Adjust 4 (A), obtained from the Nanofocus measurements, were corroborated.

In addition, once again, Adjust 5 (A), performed to bring warpage levels within acceptable limits after the application of Adjust 4 (A), proved to be efficient. This emphasises that, in fact, applying a warpage correction technique with only a 10-degree temperature difference, even when the product is at the same process stage, can have greatly different impacts on warpage.

Regarding the analysis of the temperature impact on wafers with the same layers during adjusts, this analysis cannot be executed due to the insufficient number of comparison points between adjustments. The same limitation applies when comparing the impact of different numbers of layers on warpage reduction when subjected to the same temperature in the same equipment.

Further, the single recipe, used throughout the entirety of all the warpage correction techniques executed in Equipment B, also consistently reduced warpage values to within acceptable limits.

As done previously, Figure 4.26 depicts the warpage difference after each adjust relative to the initial warpage value (%) when measured with the Sorter: Pre-Aligner measurement technique.

As observed, the applied recipes appeared to decrease the warpage values measured when the wafers were positioned on the central column of the equipment by approximately 25-30 %. Comparing these results with the Nanofocus results suggests that the wafer adjusts are not as effective in reducing flexibility as they are in decreasing the numerical warpage values.

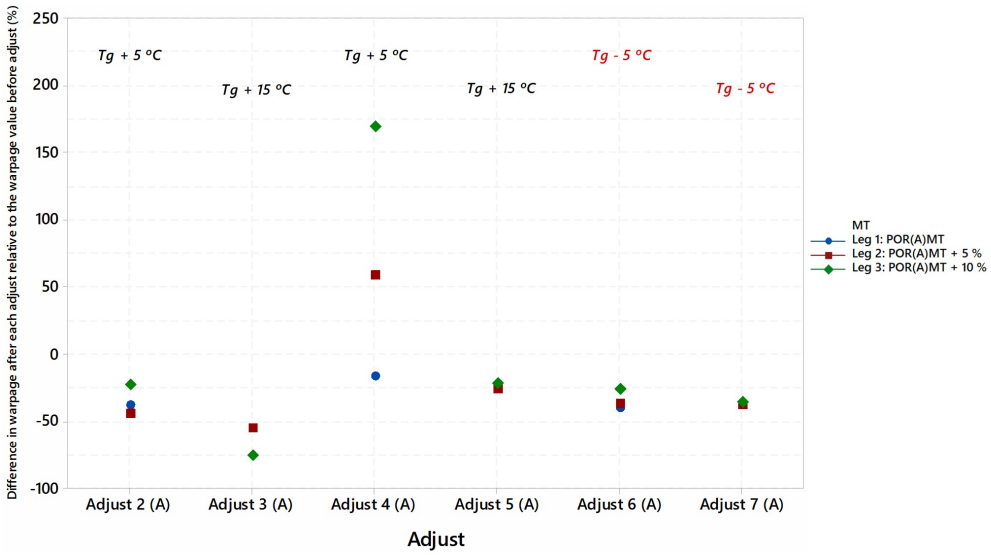


Figure 4.26: Sorter: Pre-Aligner warpage difference after each adjust relative to the warpage value before adjust for Product A.

Finally, the Sorter: Plain Chuck measurements, shown in Figure 4.27, endorse all the hypothesis previously formulated with the Nanofocus equipment, that is: the same adjust tends to be more effective for wafers with a thinner mold compound, when compared to the ones that employ the POR_{MT} + 10 % EMC value; Adjust 4 (A) leads to an increment on warpage and lastly, no correlations were found between applying varying temperatures and the subsequent reduction in warpage levels.

Please note that in the Sorter: Plain Chuck measurements, Adjust 2 (A) resulted in a slightly lower decrease in warpage for Leg 1 compared to Leg 2. This can be, once again, justified by the different time windows previously mentioned, as these two different types of measurement (Sorter: Pre-Aligner and and Sorter: Plain Chuck) are performed at the same time.

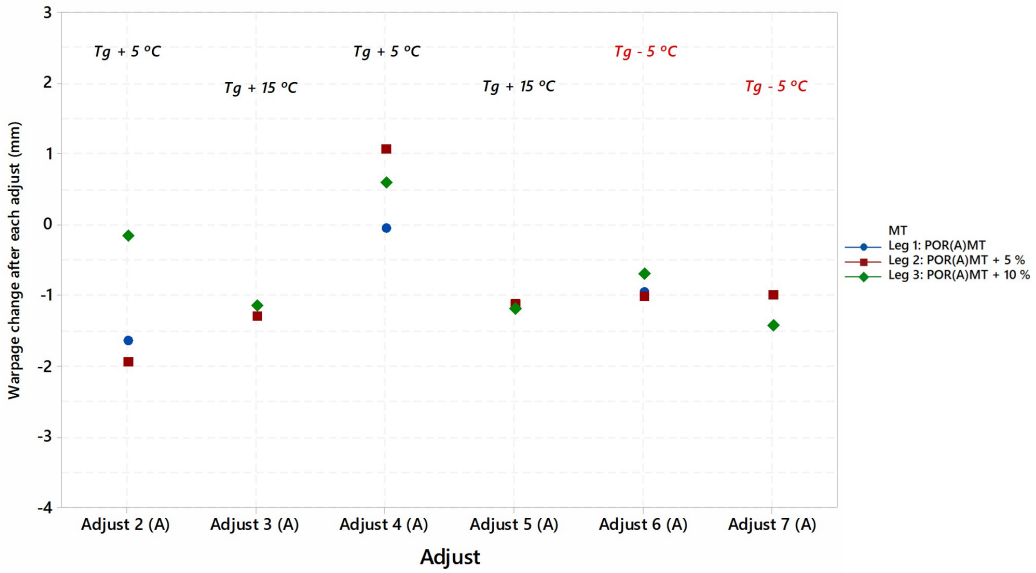


Figure 4.27: Sorter: Plain Chuck warpage change after the application of warpage correction techniques for Product A.

At last, as done previously, Figure 4.28 depicts the warpage difference after each adjust relative to the warpage value before the adjust for the Sorter: Plain Chuck measurements.

As concluded from the previously analyzed Nanofocus results, all adjustments seem to achieve an approximately 50 % reduction in warpage values, with a few outliers, when measured using this technique.

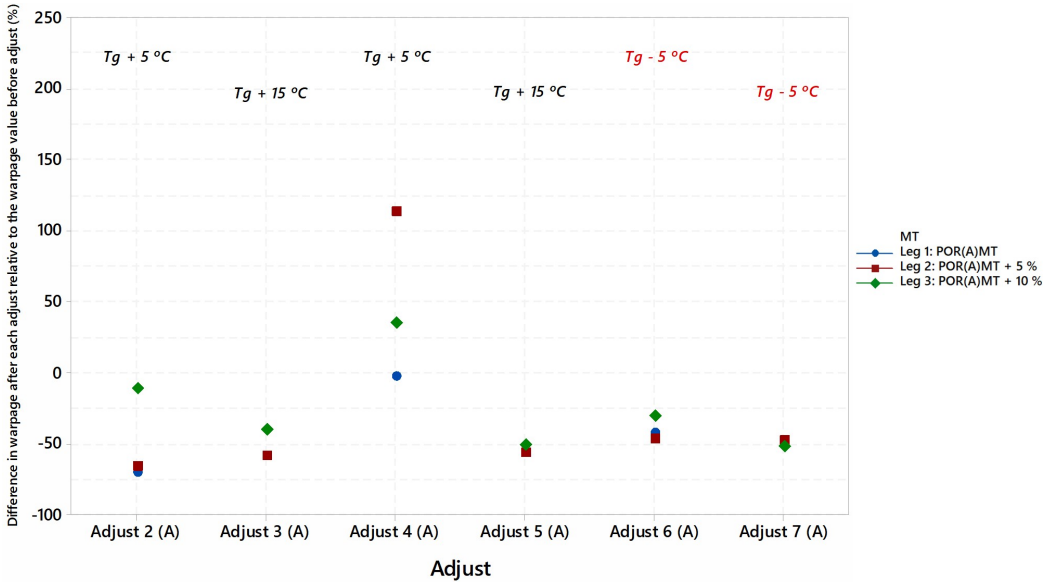


Figure 4.28: Sorter: Plain Chuck warpage difference after each adjust relative to the warpage value before adjust (%) for Product A.

To sum up, for Product A, adjusts are more effective when applied to legs with a smaller mold compound thickness. Furthermore, no definitive conclusions could be reached regarding the effect of temperature on the warpage correction techniques applied within this product, due to the sparse number of adjusts performed and the minimal variability among them.

4.1.5.2 Product B

As executed earlier for Product A, this analysis will commence by identifying the steps in which a warpage correction technique had to be applied for Product B.

Please refer to Table 4.4 for a better understanding of the above.

Table 4.4: Steps in which Product was submitted to a warpage correction technique.

	Leg 4	**Leg 5**	**Leg 6**
After Step 1B	Adjust 1 (B)	Adjust 1 (B)	Adjust 1 (B)
After Step 3B	Adjust 2 (B)	Adjust 2 (B)	Adjust 2 (B)
Before Step 4B	Adjust 3 (B)	Adjust 3 (B)	Adjust 3 (B)
After Step 6B	-	-	Adjust 4 (B)
After Step 8B	-	Adjust 5 (B)	Adjust 5 (B)
After Step 8B	-	Adjust 6 (B)	**-**
After Step 9B	-	-	Adjust 7 (B)

The amount of warpage correction techniques applied in each leg were distinct. The leg that encompassed the highest mold compound thickness value, Leg 6, presented the higher number of

correction techniques - six. This was followed by Leg 5 with five adjusts and Leg 4 with three adjusts.

This observation firmly supports the conclusion that using wafers with a higher mold compound thickness compared to the POR_{MT} slows down the manufacturing process. This is due to the need for additional manufacturing steps that take extra time to reduce warpage levels to acceptable limits.

As previously done, an individual analysis of the warpage values before and after a specific warpage correction technique, collected through the different equipment and techniques, will be performed.

Please consult section A.2 for the values of the experimental data used for the graphical representation of these increments upon each warpage adjust.

For the findings extracted from the Nanofocus equipment (graphically represented in Figure 4.29), various conclusions were drawn.

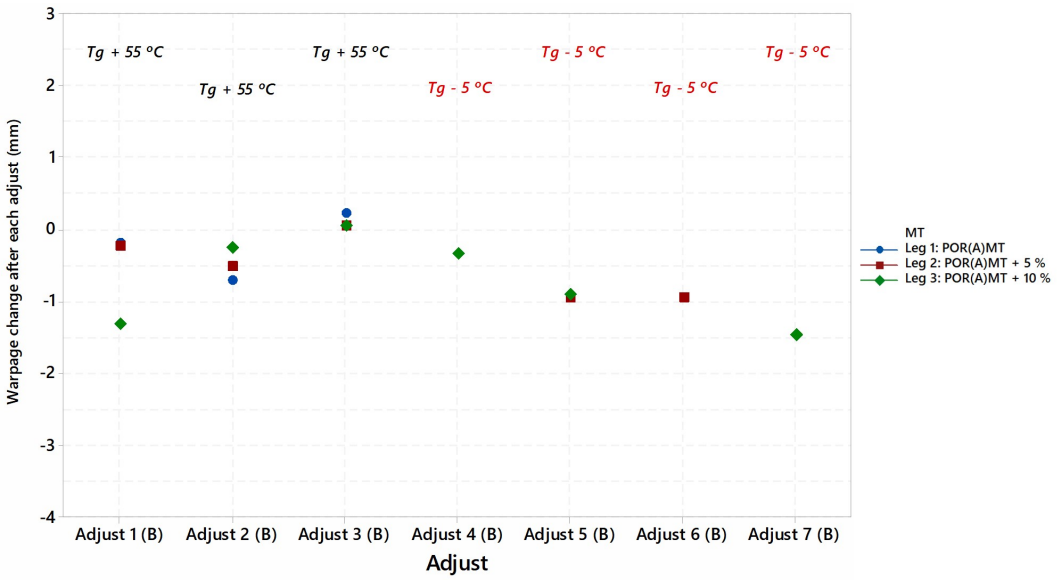


Figure 4.29: Nanofocus warpage change after the application of warpage correction techniques for Product B.

Firstly, the correlation observed in Product A, where the adjusts were more efficient on wafers with thinner mold compound layer, is no longer visible. Per the contrary, in two of the steps, this leg showed the least amount of decrease.

Additionally, it can also be concluded, that Leg 1 did not require any warpage correction technique performed in Equipment B. Moreover, by observing this graphical representation, it is feasible to conclude that, on average, the adjusts performed in Equipment B tend to be more slightly more efficient in decreasing the warpage levels.

The analysis of using different temperatures in steps with the same number of added layers, or vice versa, proved to be particularly challenging in this scenario. This difficulty arises since only

two recipes were used - one in each equipment - and it is not feasible to compare temperatures when they are applied by different equipment.

Some other intriguing findings within this product reveal that employing two consecutive warpage correction techniques within the same step - Adjusts 5 (B) and 6 (B) - showed no discernible impact, as the warpage reduction was relatively similar despite the initial attempt not working.

Additionally, it was intriguing to observe that as the adjusts continued to be performed on the wafers using Equipment B, the warpage levels seemed to decrease progressively.

Please observe the behaviour of Leg 6, on Figure 4.29, for a better understanding of this phenomenon.

At last, it can be concluded that the chosen recipe for Equipment A effectively reduced warpage levels across all studied legs, with the exception of Adjust 3 in Leg 1, which can be attributed once again to the significant time lapse between adjust execution and subsequent measurement. Similarly, this line of reasoning applies to Product B, which required only one warpage correction recipe.

Given the inconclusive nature of these results, as done for Product A, another approach was employed, wherein the difference in warpage after each adjust relative to the initial warpage value was graphically represented.

The results of this analysis can be seen in Figure 4.30.

In this instance, definitive conclusions regarding which warpage adjust most effectively reduced warpage levels in percentage terms could not be drawn. It appears that all adjustments achieved a reduction in warpage ranging from 30 % to 50 %, with Adjust 3 (A) showing the smallest percentage decrease.

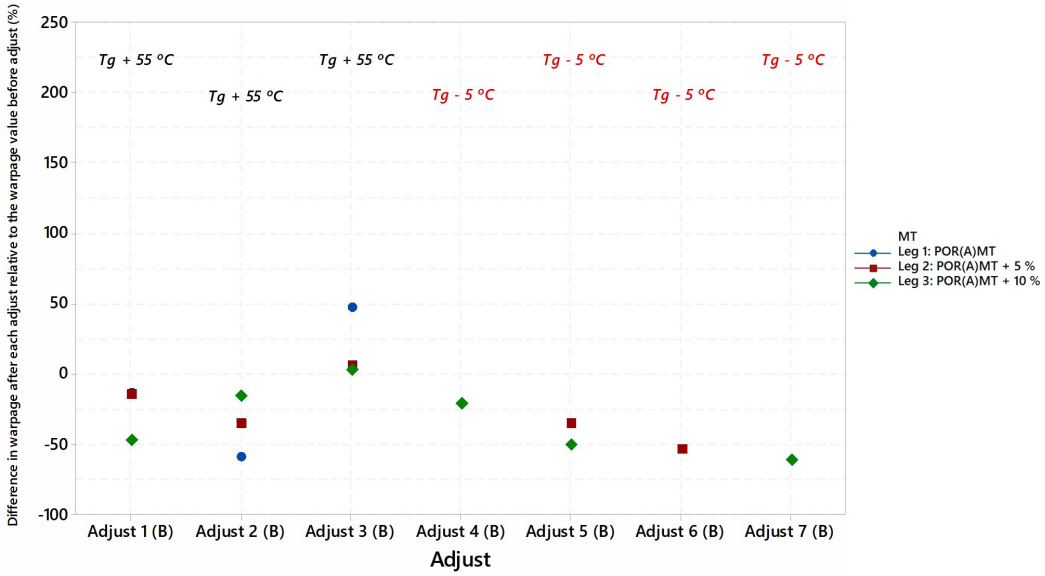


Figure 4.30: Nanofocus warpage difference after each adjust relative to the warpage value before adjust for Product B.

For the Sorter: Pre-Aligner results, shown in Figure 4.31, similar results were obtained as with the Nanofocus equipment, especially in the correction techniques performed with Equipment A.

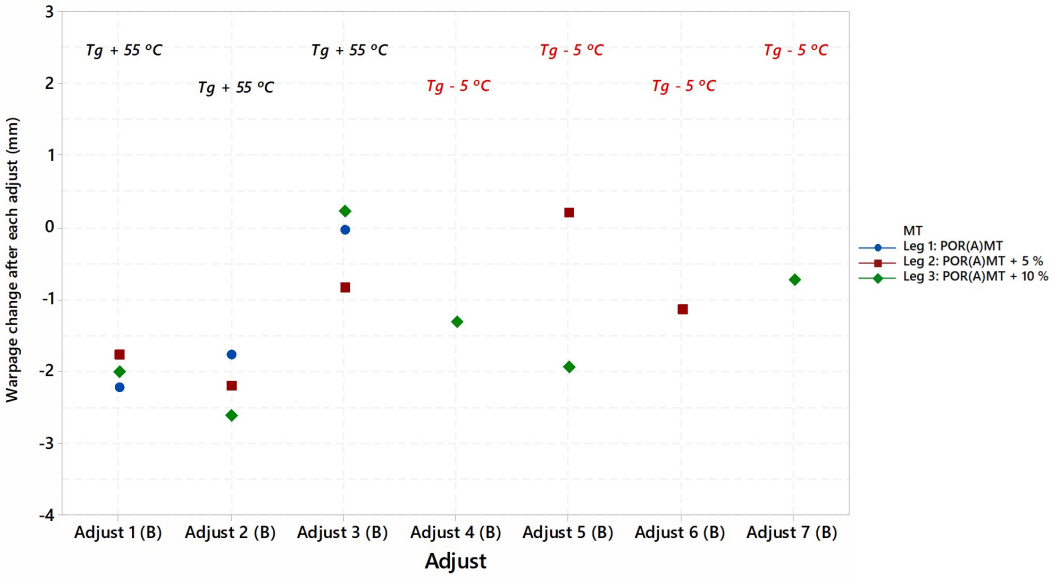


Figure 4.31: Sorter: Pre-Aligner warpage change after the application of warpage correction techniques for Product B.

In these correction techniques, the order of the legs changes, but the adjusts consistently prove to be efficient in decreasing warpage levels - with a small exception made for Adjust 3 (B) - performed when the wafers were within acceptable warpage limits. The obtained warpage values will also differ significantly due to the way the equipment positions the wafer for measurement - on a centered middle column in the case of the Pre-Aligner.

These changes in leg order allow to corroborate the theory previously stated in the Nanofocus results that, contrarily to Product A, the adjusts are not more efficient on wafers with thinner mold compound layers.

Moreover, in Adjust 5 (B) there was the appearance of an odd point for Leg 5, in which the warpage value increased after adjust (contrary to the observed Nanofocus results).

This anomaly was investigated, and it was concluded that the time between the execution of the adjust and the subsequent measurement was more than 24 hours - 26 hours to be exact. This lengthy interval likely caused the warpage correction technique to lose its effectiveness and for the warpage to appear again.

Furthermore, Adjust 7 (B) proved effective as it reduced the warpage levels, but according to this equipment, it was not as effective as the Nanofocus measurement indicated. Thus, it can be inferred that this adjustment reduced warpage more significantly than it reduced flexibility.

The Sorter: Pre-Aligner warpage difference after each adjust relative to the warpage value before adjust, for Product B, is presented in Figure 4.32.

As seen, the percentages decrease were consistently around 25-40 % and no definitive conclusions could be extracted as to which adjusts were more effective or the impact of temperature on the percentage reduction in warpage.

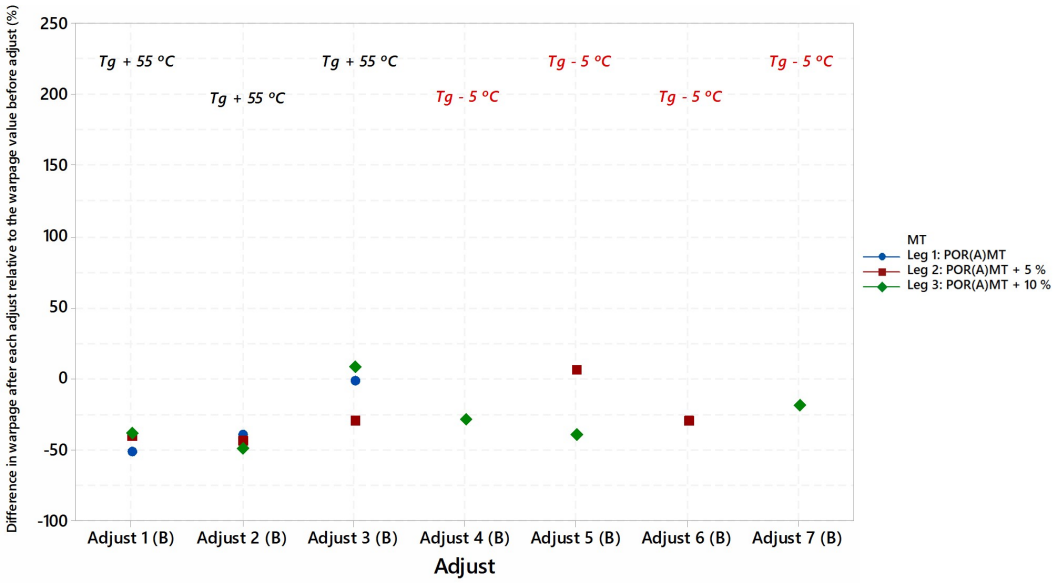


Figure 4.32: Sorter: Pre-Aligner warpage difference after each adjust relative to the warpage value before adjust for Product B.

Lastly, the results obtained from the Sorter using the Plain Chuck measurements yielded surprising outcomes that did not entirely align with those obtained from the Nanofocus measurements, despite their similar measurement methodologies.

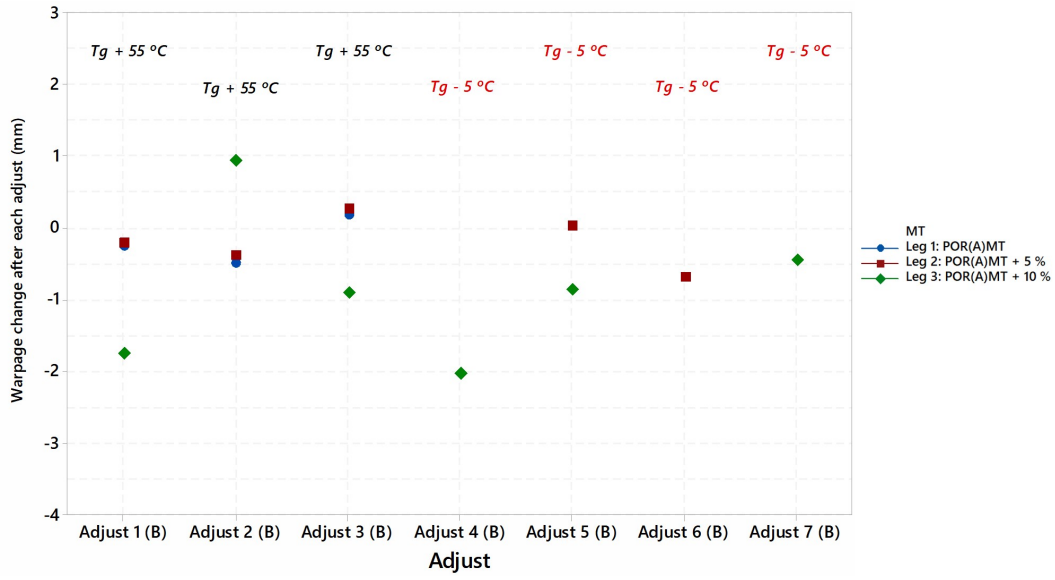


Figure 4.33: Sorter: Plain Chuck warpage change after the application of warpage correction techniques for Product B.

One result that did align with the Nanofocus findings, was the fact that the wafers with the thinnest mold compound layer, once again, are not the ones that show the highest warpage decrease. Conversely, Leg 3, which has the greatest mold compound thickness, consistently exhibits the highest decrease in warpage, with the exception of Adjust 2 (B).

Now, discussing the results that diverged from those obtained with the Nanofocus equipment. At the beginning of the process, where the initial adjusts were executed, the results were similar - despite having different warpage values, the overall observed trends had a high degree of similarity. However, from Adjust 4 (B) until Adjust 7 (B), a decrease in the effectiveness of the warpage correction techniques was observed, evidenced by the lower warpage change after each adjust as more adjusts were consecutively applied.

The Sorter: Plain Chuck warpage difference post-adjust relative to the warpage value prior-adjust, for Product B, can be read in Figure 4.34.

Notably, for Product B, the warpage percentages exhibit a decreasing trend as the legs progress through the packaging process and accumulate multiple adjusts. This trend is particularly evident by the observation of Leg 3's behavior during Adjusts 4(B) through 7(B), all of which were conducted on wafers with two dielectric layers present on them.

Lastly, no conclusive broad analysis can estimate the approximate percentage by which these adjusts reduce warpage, as the results vary significantly.

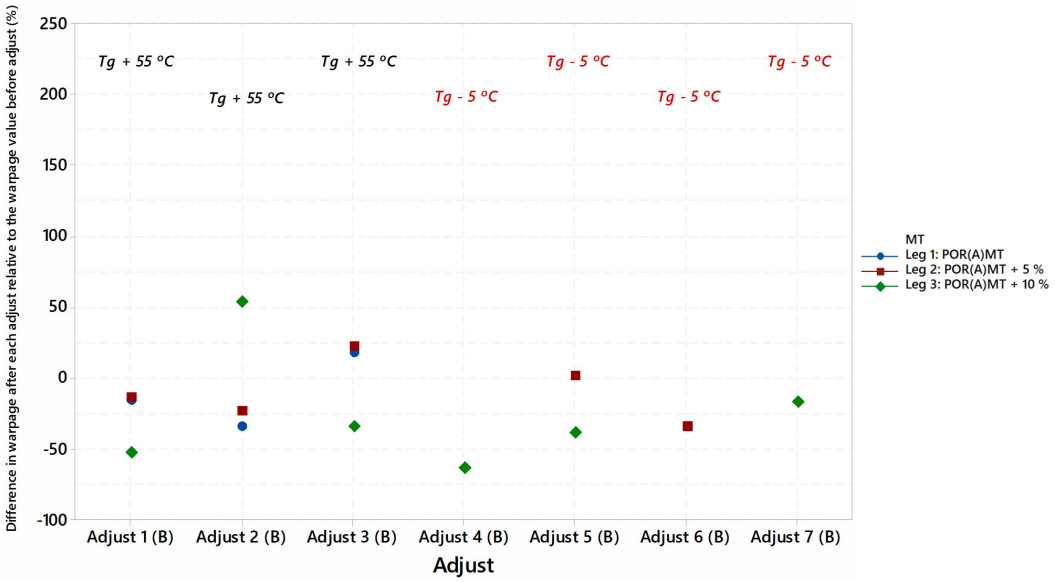


Figure 4.34: Sorter: Plain Chuck warpage difference after each adjust relative to the warpage value before adjust for Product B.

To conclude Product B's analysis, as easily derived from this analysis, it was not possible to draw definitive conclusions, since the gathered results tend to differ depending on the measuring technique utilized. To gain more insights into the impact of temperatures, additional warpage correction techniques, applying different recipes, would need to be tested in each of the equipment.

In summary of both products, a key takeaway is that it was proven that the warpage correction technique recipe chosen for Equipment B, regardless of the specific product, is effective at decreasing warpage levels in every step after the deposition of the seed layer. This could help standardize the same adjust throughout the latter stages of the packaging manufacturing process, potentially saving a significant amount of resources.

Chapter 5

Conclusion and Future Work

This final chapter will present and summarize the various conclusions reached throughout the course of this research, as well as outline some potential prospects for future work and avenues for improvement. Additionally, it will also offer recommendations for reducing the impact of warpage levels throughout the process and mitigating the process delays typically caused by them.

5.1 Conclusion

The study elaborated as a part of the Master's degree in Mechanical Engineering at Amkor Technology Portugal, and that had as its main goal the analysis of the behaviour of several wafers, of two distinct front-end manufacturers, across multiple stages of the packaging process to comprehensively characterize and optimize warpage, yielded several conclusions, varying in the degree of experimental validation.

This next section will succinctly present these findings.

5.1.1 Results of the analysis of the temperature impact on warpage levels

When it comes to the analysis presented in subsection 4.1.1, which examined the impact of temperature on warpage levels, it was determined that increased processing temperatures consistently led to higher warpage, as evidenced by all three measurement techniques employed. Conversely, lower processing temperatures consistently led to reduced warpage levels, although variations were observed depending on the measurement technique used.

As such, given that all the steps involving increased processing temperatures exceed the glass transition temperature threshold, it becomes conceivable to deduce that exceeding this value leads to higher warpage values. Hence, if feasible, the majority of the processing steps should ideally be performed below this value or as close to it as possible.

Please note that it is acknowledged that certain steps necessarily and indispensably require temperatures higher than Tg for their proper execution (e.g. the application of the solder balls), and therefore such recommendation can not be followed.

5.1.2 Results of the analysis of the addition of the first dielectric layer on warpage levels

In the analysis detailed in subsection 4.1.2, which explored the effects of the addition of the first dielectric layer on warpage levels, it was possible to conclude, using Nanofocus and Sorter: Plain Chuck measurements, that the low thickness of the first dielectric is insufficient to counteract the inward contraction forces imposed by the mold compound after curing. Consequently, it can be said that this layer does not significantly impact warpage levels, either negatively or positively.

It should be highlighted that the results from the Sorter: Pre-Aligner measurements require further repetition to validate their accuracy. This is particularly important since the gatherings obtained with this measurement technique would be valuable when it comes to the study of the flexibility of the wafers, with or without the first dielectric layer.

5.1.3 Results of the analysis of the mold compound thickness and volume occupation ratio percentage impact on warpage levels

Regarding the analysis that studied the mold compound thickness influence on warpage levels, described in subsection 4.1.3, it is imperative to state that the steps could not be individually analyzed for their impact due to variations in the optimal thickness depending on the measurement equipment used. Additionally, even when comparing the results obtained from the same measuring equipment, the optimal mold compound thickness for minimizing warpage also varied throughout the packaging production process.

Secondly, when comparing the two Products in this matter, an uniform conclusion was drawn: the legs that had a 10 % increase in their mold compound thickness compared to the POR_{MT} value - Legs 3 and 6 in Products A and B, respectively - consistently displayed the highest measured warpage values, regardless of the measuring technique used.

In addition, when it comes to the most beneficial leg to minimize warpage levels, the legs with the lowest mold compound thicknesses were identified as the optimal choices. Specifically, Legs 1 and 4 in Products A and B, respectively, were found to be the most advantageous.

Please note that this conclusions was more consistent for Product B, as all measurement equipment indicated that Leg 4 should be chosen. Conversely, for Product A, one of the equipment suggested that Leg 1 might not be the optimal choice for achieving the lowest warpage values.

To summarize the obtained results, the gathered data indicates that using higher values of epoxy mold compound thicknesses, regardless of the product, is not optimal for minimizing warpage levels throughout most of the process. Thence, lower mold compound thickness values should always be preferred.

In the analysis of the analysis of the volume occupation ratio percentage impact on warpage levels, also shown in subsection 4.1.3, it was concluded that legs with lower VOR percentages - indicating the highest mold compound thickness - should not be chosen to reduce warpage levels. Conversely, legs with higher VOR values, which indicates smaller wafer volumes and consequent smaller mold compound thicknesses (for wafers with 300 mm in diameter), should be opted for.

5.1.4 Results of the analysis of the specific step impact on warpage levels

Analyzing the impact of specific steps on warpage levels, as shown in subsection 4.1.4, was one of the most challenging aspects of this study, that required significant effort to derive scientifically meaningful conclusions. The results obtained in this analysis also deviated somewhat from the initial analysis where the impact of different temperature ranges on warpage levels was studied.

To easily understand the distinct conclusions drawn from the obtained warpage increment values of both products, in all the different measurement techniques, please consult Table 5.1.

Table 5.1: Steps with the overall highest/lowest warpage increment for both products.

		Steps with the highest warpage increment	**Steps with the lowest warpage increment**
Nanofocus	*Product A*	1A, 3A, 6A, 8A and 9A	2A and 5A
	Product B	8B and 9B	5B and 7B
Sorter: Pre-Aligner	*Product A*	1A, 3A, 6A, 8A and 9A	2A, 4A and 5A
	Product B	1B, 3B and 8B	7B
Sorter: Plain Chuck	*Product A*	1A, 3A, 6A, 8A and 9A	2A and 5A
	Product B	8B and 9B	3B, 4B and 5B

As evident, Steps 1A, 3A, 6A, and 8A overall increase warpage levels on Product A, whereas Steps 8B and 9B seem to be the steps in Product B that most generally increments warpage values. Furthermore, Steps 2A and 5A have minimal impact on warpage levels for Product A, and Steps 5B and 7B have it for Product B.

These results align with expectations for Steps 1A, 3A, and 6A, where curing processes and temperatures above Tg lead to higher mismatches in the different CTE values. Moreover, the grinding of the wafer in Step 9A justifies the higher warpage increment that appears on the wafers of this product. In addition, the steps using temperatures further from Tg - Steps 2A and 5A - showing the lowest increments also went according to the previously held expectations.

The results also corroborated for Product B, where a step involving plasma cleaning (Tg - 100 ºC) and seed layer deposition (Tg - 55 ºC) exhibited the smallest increase in warpage. In contrast, steps such as Step 8B (wafer cleaning) and Step 9B (mold compound grinding) showed the highest increments in warpage.

The most critical observation for both products is that Step 8A/B, executed well below Tg with two dielectric layers already applied to the wafers, showed a significantly high increase in warpage without a plausible explanation for this occurrence.

Additionally, for Product B, it was interesting to conclude that the curing steps were not the steps in which the highest increase on warpage values were observed, but rather the other two aforementioned steps.

Furthermore, it was interesting to note that the influence of temperature, above the glass transition temperature, on warpage decreases as the materials progresses through the process. When the

products are in a processing step that includes the second dieletric layer, they are more resistant to an increase in warpage levels, regardless of the studied legs.

In conclusion, the results from this analysis vary considerably depending on the product, suggesting that packaging materials should not be generalized across both products.

When comparing Product A to Product B, which has smaller dies, extracting conclusions from the results for Product B was notably more challenging due to a greater dispersion of results across all measurement techniques.

5.1.5 Results of the analysis of the application of warpage correction techniques on warpage levels

The results regarding the application of warpage correction techniques proved to be the most challenging to derive actionable conclusions from. Overall, and succinctly, it can be said that different conclusions were gathered depending on the product being studied, which emphasizes that the adjusts for each product should not be generalized, as their unique characteristics cause them to react very differently to these adjusts.

For Product A, the results regarding its adjusts are summarized as follows: legs with higher mold compound thicknesses always necessitate more adjusts throughout the packaging process; the same adjust proves more effective for wafers with the POR_{MT} thickness value; applying a warpage correction technique with just a 10-degree difference, at the same processing stage, can significantly and positively impact warpage reduction; the singular recipe used in Equipment B consistently decreases warpage values regardless of the product's stage in the packaging process, whereas Equipment A needed two different recipes; most adjusts reduce warpage by about 50 % when measured with Nanofocus, 25-30 % with Sorter: Pre-Aligner, and approximately 50 % with Sorter: Plain Chuck and lastly analyzing temperature variations in steps with the same number of layers was not feasible due to insufficient data.

Regarding Product B, the findings concerning its adjustments can be summarized as follows: legs with higher mold compound thicknesses consistently require more adjusts throughout the production process; the same adjusts are not more efficient when applied to legs with the POR_{MT} thickness value: repeating the same adjust in Equipment B tends to decrease warpage more in the second adjustment, even when the same processing temperatures are applied; the sole recipe used in Equipment A and B consistently decreases warpage values, with the exception of a few outliers, regardless of the stage in the packaging process; most adjusts reduce warpage by approximately 30-50 % when measured with Nanofocus, 25-40 % when measured with Sorter: Pre-Aligner, and the results were inconclusive when measured with Sorter: Plain Chuck and lastly, once again, analyzing temperature variations in steps with the same number of layers, or vice versa, was not feasible due to the lack of data and little variation amongst the employed adjusts.

Therefore, based on these aforementioned conclusions, it is now possible to finalize Table 3.3, previously presented in chapter 3. The results are outlined in Table 5.2.

Table 5.2: Results of the different studies conducted with Material A and B.

Legs used for comparison	**Objective**	**Results**
Legs 1, 2 and 3	Study the influence of an increased mold thickness on warpage on Product A.	The higher the mold thickness, the higher the warpage levels.
Legs 1, 2 and 3	Study the influence of an increased VOR percentage on warpage on Product A.	The higher the VOR percentage, the lower the warpage levels.
Legs 4, 5 and 6	Study the influence of an increased mold thickness on warpage on Product B.	The higher the mold thickness, the higher the warpage levels.
Legs 4, 5 and 6	Study the influence of an increased VOR percentage on warpage on Product B.	The higher the VOR percentage, the lower the warpage levels.
Legs [1-3] and [4-6]	Study the influence of different ranges of temperatures, used in each specific step, on warpage.	The higher the range of processing temperatures, the higher the warpage levels.
Legs [1-3] and [4-6]	Study the impact of varying warpage correction techniques' temperatures and timings on warpage.	Inconclusive results.
Legs 4 and 7	Study the influence of the application of the first dieletric layer on warpage.	DL1 has no influence on warpage levels, either positive or negative.

5.2 Future Work

While this study provided a thorough characterization of warpage in the semiconductor packaging industry, there are several areas that warrant further investigation to strengthen the findings.

One avenue for future research, already previously described in Section 2.4, is that to better understand the effects of different wafer characteristics on warpage, both the silicon and the mold compound thickness should ideally vary by at least three levels. As an instance, both could vary by 5 % or 10 % of their respective initial thickness, which would result in a study with 9 different experimental runs for each product - as shown in Table 5.3 and Table 5.4.

Table 5.3: Orthogonal matrix for Product A's future study experiments.

Experiment	**Factor 1**	**Factor 2**
1	$POR(A)_{MT}$	$POR(A)_{ST}$
2	$POR(A)_{MT}$	$POR(A)_{ST}$ + 5 %
3	$POR(A)_{MT}$	$POR(A)_{ST}$ + 10 %
4	$POR(A)_{MT}$ + 5 %	$POR(A)_{ST}$
5	$POR(A)_{MT}$ + 5 %	$POR(A)_{ST}$ + 5 %
6	$POR(A)_{MT}$ + 5 %	$POR(A)_{ST}$ + 10 %
7	$POR(A)_{MT}$ + 10 %	$POR(A)_{ST}$
8	$POR(A)_{MT}$ + 10 %	$POR(A)_{ST}$ + 5 %
9	$POR(A)_{MT}$ + 10 %	$POR(A)_{ST}$ + 10 %

Table 5.4: Orthogonal matrix for Product B's future study experiments

Experiment	**Factor 1**	**Factor 2**
1	$POR(B)_{MT}$	$POR(B)_{ST}$
2	$POR(B)_{MT}$	$POR(B)_{ST}$ + 5 %
3	$POR(B)_{MT}$	$POR(B)_{ST}$ + 10 %
4	$POR(B)_{MT}$ + 5 %	$POR(B)_{ST}$
5	$POR(B)_{MT}$ + 5 %	$POR(B)_{ST}$ + 5 %
6	$POR(B)_{MT}$ + 5 %	$POR(B)_{ST}$ + 10 %
7	$POR(B)_{MT}$ + 10 %	$POR(B)_{ST}$
8	$POR(B)_{MT}$ + 10 %	$POR(B)_{ST}$ + 5 %
9	$POR(B)_{MT}$ + 10 %	$POR(B)_{ST}$ + 10 %

Moreover, further examination of the use of different components within the same materials could develop insight into how the materials' intrinsic and mechanical properties impact warpage. This could include using different mold compound compositions while keeping all other wafer components (e.g. dielectric layers and silicon substrate) the same.

Additionally, a third prospect for future work could involve examining how various warpage correction techniques impact warpage levels during the same stage of processing and draw conclusions regarding which one of them minimizes warpage the most.

This research would be challenging given that once a specific wafer undergoes a certain correction, it will no longer follow the same processing path as the other wafers in the same batch - subsequent steps can't be tested uniformly since the wafers would have experienced different correction temperatures, altering their characteristics. Nevertheless, it is still possible to study this by focusing on a specific step where all the wafers have the same characteristics before any corrections are applied.

Lastly, it could be valuable to study the time windows between the employment of a specific warpage correction technique and the point at which the correction is no longer effective, triggering the warpage levels to return to their initial state. This would allow a more efficient management of the company's resources and facilitate a better planning of daily production activities.

References

AlMaadeed, M. A. A., Ponnamma, D. and El-Samak, A. A. (2020), Chapter 1 - polymers to improve the world and lifestyle: physical, mechanical, and chemical needs, *in* M. A. A. AlMaadeed, D. Ponnamma and M. A. Carignano, eds, 'Polymer Science and Innovative Applications', Elsevier, pp. 1–19.

ATEP (2024), 'Official Internal documents.'.

Baek, J.-H., Park, D.-W., Oh, G.-H., Kawk, D.-O., Park, S. S. and Kim, H.-S. (2022), 'Effect of cure shrinkage of epoxy molding compound on warpage behavior of semiconductor package', *Materials Science in Semiconductor Processing* **148**, 106758.

Boparai, K. S. and Sandhu, G. S. (2023), Free form fabrication of mechanical meta-materials with configurable thermal properties, *in* 'Reference Module in Materials Science and Materials Engineering', Elsevier.

Brunnbauer, L., Zeller, V., Gajarska, Z., Larisegger, S., Schwab, S., Lohninger, H. and Limbeck, A. (2023), 'Classification of epoxy molding compounds by tandem la-icp-ms/libs to enhance the reliability of electronic devices', *Spectrochimica Acta Part B: Atomic Spectroscopy* **207**, 106739.

Campos, J., O'Toole, E., Pinto, R., Cardoso, A., Toussaint, P.-L. and Vernhes, P. (2015), Development of fan-in wlp with mechanical protection and dynamic warpage characterization of ewlb, *in* '2015 IEEE 65th Electronic Components and Technology Conference (ECTC)'.

Cardoso, J. (2021), 'Investigação Experimental do Warpage e Rigidez em Wafers WLP de 300 mm'.

Dincer, I. and Erdemir, D. (2021), Chapter 4 - system analysis, *in* I. Dincer and D. Erdemir, eds, 'Heat Storage Systems for Buildings', Elsevier, pp. 115–178.

DynaTech (2024), 'Fully automated wafer sorter loader (auto jar packing unpacking system)', http://www.dynatech.co.kr/products03-01/. Accessed: 2024-05-14.

ERS (2021), 'convERSations: Debbie-Claire Sanchez'.

Gao, R., Ma, R., Li, J., Su, M., Hou, F. and Cao, L. (2022), 'Selection and characterization of photosensitive polyimide for fan-out wafer-level packaging', *IEEE Transactions on Components, Packaging and Manufacturing Technology* **12**(2), 368–374.

Greene, J. P. (2021), 2 - polymer materials, *in* J. P. Greene, ed., 'Automotive Plastics and Composites', Plastics Design Library, William Andrew Publishing, pp. 17–25.

Hammerschmidt, C. (2007), 'Infineon boosts pin count for wafer-level packaging', *EE Times* .

Infineon (2019), 'Recommendations for Board Assembly of Infineon Wafer Level Ball Grid Array Packages'.

Instruments, T. (2021), 'The power of packaging'.

Kaharudin, K. E., Salehuddin, F., Zain, A. S. M. and Aziz, M. (2016), 'Implementation of taguchi method for lower drain induced barrier lowering in vertical double gate nmos device', *Journal of Telecommunication, Electronic and Computer Engineering* **8**, 11–16.

Kechagias, J. D., Aslani, K.-E., Fountas, N. A., Vaxevanidis, N. M. and Manolakos, D. E. (2020), 'A comparative investigation of taguchi and full factorial design for machinability prediction in turning of a titanium alloy', *Measurement* **151**, 107213.

Kokatev, A. N., Iakovleva, N. M., Stepanova, K. V., Ershova, N. Y. and Belov, K. V. (2019), 'Monitoring of properties of epoxy molding compounds used in electronics for protection and hermetic sealing of microcircuits', *IOP Conference Series: Materials Science and Engineering* **665**.

Lee, C. (2017), 'What's what in advanced packaging', https://semiengineering.com/whats-what-in-advanced-packaging/. Accessed: 2024-04-03.

Meena, A., Mali, H. S., Patnaik, A. and Kumar, S. R. (2018), 13 - investigation of wear characteristics of dental composites filled with nanohydroxyapatite and mineral trioxide aggregate, *in* S. Thomas, P. Balakrishnan and M. Sreekala, eds, 'Fundamental Biomaterials: Polymers', Woodhead Publishing Series in Biomaterials, Woodhead Publishing, pp. 287–305.

Meyer, T., Ofner, G., Bradland, S., Brunnbauer, M. and R.Hagen (2008), Embedded wafer level ball grid array (ewlb), *in* '2008 10th Electronics Packaging Technology Conference', pp. 994–998.

Ng, C. S. and Asundi, A. K. (2011), 'Warpage measurement of thin wafers by reflectometry', *Physics Procedia* **19**, 9–20. International Conference on Optics in Precision Engineering and Nanotechnology (ICOPEN 2011).

Pan, Y., Song, Y., Zhang, C.-C., Zhu, Q. and Wu, J. (2024), 'Semiconductor industry's transformation path under circular economy: Evidence from micro-level efficiency evaluation', *Computers Industrial Engineering* **189**, 109934.

Peixoto, N. (2014), 'Caracterização do "warpage" e sua variabilidade no processo produtivo de encapsulamento de circuitos integrados'.

Perabo, C. (2018), 'Glass Transition Temperature (tg) of Epoxy Molding Compounds', *CapLinq Blog* .

Phansalkar, S. P., Kim, C. and Han, B. (2022), 'Effect of critical properties of epoxy molding compound on warpage prediction: A critical review', *Microelectronics Reliability* **130**, 114480.

Pönninger, A., Uhrmann, T. and Matthias, T. (2010), 'Wafer level packaging –processes and manufacturing equipment'.

Quirk, M. and Serda, J. (2001), *Semiconductor Manufacturing Technology*, Prentice Hall.

Ramsey, B. (2023), 'The complicated (and expensive) process of manufacturing semiconductors', https://intelligence.supplyframe.com/pt/complex-expensive-manufacturing-semiconductors/.

Reddy, S. (2014), 'Dielectric materials for semiconductor chips', *EEHerald* .

Reis, A. and Silva, R. P. (2023), Planeamento de experiências, *in* 'Slides de apoio às aulas de Tecnologias Avançadas de Produção II (FEUP)'.

Saint, J. L. and Saint, C. (2024), 'Integrated circuit', https://www.britannica.com/technology/integrated-circuit.

Singh, T., Mcmillan, H., Mooney, K., Alkilani, A. and Donnelly, R. (2013), 6 - microneedles for drug delivery and monitoring, *in* X. J. Li and Y. Zhou, eds, 'Microfluidic Devices for Biomedical Applications', Woodhead Publishing Series in Biomaterials, Woodhead Publishing, pp. 185–230.

Teixeira, J. and Ribeiro, M. (2012), 'Method to measure wafer stiffness in fan-out wafer level package', *IMAPSource Proceedings* pp. 720–728.

Thapa, R. (2020), 'Polyimides (pi) polybenzoxazoles (pbo): Advanced dielectric polymers for wafer bumping wafer level packaging', waferdies.com/polyimides-pi-and-polybenzoxazoles-pbo-advanced-dielectric\-polymers-for-wafer-bumping-wafer-level-packaging/. Accessed: 2024-05-16.

Tomikawa, M. (2021), Polyimides for micro-electronics applications, *in* B. Nandeshwarappa and S. Chandrashekharappa, eds, 'Polyimides', IntechOpen, Rijeka, chapter 5.

Unal, R. and Dean, E. B. (1991), 'Taguchi approach to design optimization for quality and cost: an overview', *1991 Annual Conference of the International Society of Parametric Analysis* **8**, 11–16.

Wojnowski, M., Pressel, K., Sommer, G. and Engl, M. (2008), 'Package trends for today's and future mm-wave applicationsinfineonboosts', *The 38th European Microwave conference* .

Wu, J.-Z. and Chien, C.-F. (2008), 'Modeling strategic semiconductor assembly outsourcing decisions based on empirical settings', *OR Spectrum* **30**, 401–430.

Yao, W., Belhenini, S., Roqueta, F., Pujos, C., Bruno, E., Gardes, P. and Tougui, A. (2016), Intrinsic stress effects on the warpage of silicon substrate during thin film deposition, photolithography and etching processes, *in* '2016 17th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)', pp. 1–6.

Yuangyai, C. and Nembhard, H. (2010), Chapter 8 - design of experiments: A key to innovation in nanotechnology, *in* W. Ahmed and M. J. Jackson, eds, 'Emerging Nanotechnologies for Manufacturing', Micro and Nano Technologies, William Andrew Publishing, Boston, pp. 207–234.

Yusoff, S., Ramli, H., Zainal, N., Halim, S. and Chan, C. (2023), 4 - thermoplastic-based polymer blend nanocomposites for energy storage, *in* S. Thomas, A. Ajitha and M. Jaroszewski, eds, 'Polymer Blend Nanocomposites for Energy Storage Applications', Micro and Nano Technologies, Elsevier, pp. 109–160.

Appendix A

Appendices

A.1 Appendix A

Table A.1: Product A's Leg 1 increment on warpage measured by different techniques.

	Increment on warpage (mm)		
	Nanofocus	**Sorter: Pre-Aligner**	**Sorter: Plain Chuck**
Step 1A	1.61	1.33	1.22
Step 2A	0.04	0.07	-0.02
Step 3A	1.00	0.70	0.87
Step 4A	0.81	0.54	0.34
Step 5A	-0.02	-0.38	0.04
Step 6A	0.53	0.72	0.39
Step 7A	0.34	-0.27	-0.28
Step 8A	1.23	1.48	0.96
Step 9A	3.44	5.30	4.26

Table A.2: Product A's Leg 2 increment on warpage measured by different techniques.

	Increment on warpage (mm)		
	Nanofocus	**Sorter: Pre-Aligner**	**Sorter: Plain Chuck**
Step 1A	1.95	1.30	1.62
Step 2A	0.15	0.17	0.15
Step 3A	1.28	2.76	1.06
Step 4A	0.18	-0.37	0.44
Step 5A	0.23	0.56	0.02
Step 6A	1.02	1.05	0.85
Step 7A	0.21	-0.55	0.08
Step 8A	1.21	1.74	0.83
Step 9A	4.59	4.94	3.95

Table A.3: Product A's Leg 3 increment on warpage measured by different techniques.

	Increment on warpage (mm)		
	Nanofocus	**Sorter: Pre-Aligner**	**Sorter: Plain Chuck**
Step 1A	-0.02	1.30	-0.38
Step 2A	0.61	0.17	0.59
Step 3A	0.80	2.76	0.94
Step 4A	1.16	-0.37	0.38
Step 5A	-0.29	0.56	0.20
Step 6A	0.71	1.05	0.59
Step 7A	0.86	-0.55	0.27
Step 8A	0.63	1.74	0.88
Step 9A	4.18	6.11	4.73

Table A.4: Product B's Leg 4 increment on warpage measured by different techniques.

	Increment on warpage (mm)		
	Nanofocus	**Sorter: Pre-Aligner**	**Sorter: Plain Chuck**
Step 1B	0.04	2.31	-0.01
Step 2B	0.00	0.57	0.17
Step 3B	-0.08	1.82	-0.06
Step 4B	0.18	-0.41	0.04
Step 5B	0.00	0.11	0.03
Step 6B	-0.17	-0.72	-0.19
Step 7B	-0.40	-0.30	-0.39
Step 8B	1.22	1.31	1.25
Step 9B	0.13	-0.52	0.03
Step 10B	-0.09	0.35	-0.08

Table A.5: Product B's Leg 5 increment on warpage measured by different techniques.

	Increment on warpage (mm)		
	Nanofocus	**Sorter: Pre-Aligner**	**Sorter: Plain Chuck**
Step 1B	0.03	2.14	-0.08
Step 2B	-0.05	0.34	0.05
Step 3B	0.12	2.11	0.19
Step 4B	0.28	0.53	-0.07
Step 5B	-0.10	-0.08	-0.09
Step 6B	0.34	-0.08	0.27
Step 7B	-0.39	-0.65	-0.07
Step 8B	1.59	1.87	0.51
Step 9B	1.20	-0.07	0.80
Step 10B	0.13	0.17	0.06

Table A.6: Product B's Leg 6 increment on warpage measured by different techniques.

	Increment on warpage (mm)		
	Nanofocus	**Sorter: Pre-Aligner**	**Sorter: Plain Chuck**
Step 1B	1.05	2.00	1.56
Step 2B	0.10	0.30	0.57
Step 3B	0.08	1.82	-0.42
Step 4B	0.07	0.18	-0.17
Step 5B	-0.02	0.08	-0.07
Step 6B	0.31	1.54	1.65
Step 7B	0.28	-0.72	0.23
Step 8B	0.47	2.33	0.83
Step 9B	1.53	0.78	1.16
Step 10B	1.64	0.32	1.29

A.2 Appendix B

The gathered warpage data used for the elaboration of the graphical representations, shown in Section 4.1.5, can be read in Table A.7, Table A.8 and Table A.9, for Product A. Additionally, these are shown in Table A.10, Table A.11 and Table A.12, for Product B.

Table A.7: Warpage change, for Product A, after the application of each adjust measured by the Nanofocus equipment.

	Leg 1 (mm)	**Leg 2 (mm)**	**Leg 3 (mm)**
Adjust 2 (A)	-2.33	-2.31	-0.37
Adjust 3 (A)	-	-1.68	-1.28
Adjust 4 (A)	-0.40	1.36	1.16
Adjust 5 (A)	-	-1.08	-1.51
Adjust 6 (A)	-1.87	-1.73	-1.49
Adjust 7 (A)	-	0.07	-1.12

Table A.8: Warpage change, for Product A, after the application of each adjust measured by the Sorter: Pre-Aligner equipment.

	Leg 1 (mm)	**Leg 2 (mm)**	**Leg 3 (mm)**
Adjust 2 (A)	-1.47	-1.97	-0.80
Adjust 3 (A)	-	-2.93	-3.70
Adjust 4 (A)	-0.51	1.43	2.09
Adjust 5 (A)	-	-1.02	-0.72
Adjust 6 (A)	-1.42	-1.49	-1.12
Adjust 7 (A)	-	-1.45	-1.56

Table A.9: Warpage change, for Product A, after the application of each adjust measured by the Sorter: Plain Chuck equipment.

	Leg 1 (mm)	**Leg 2 (mm)**	**Leg 3 (mm)**
Adjust 2 (A)	-1.63	-1.94	-0.16
Adjust 3 (A)	-	-1.30	-1.14
Adjust 4 (A)	-0.04	1.06	0.60
Adjust 5 (A)	-	-1.11	-1.18
Adjust 6 (A)	-0.96	-1.03	-0.69
Adjust 7 (A)	-	-0.98	-1.41

Table A.10: Warpage change, for Product B, after the application of each adjust measured by the Nanofocus equipment.

	Leg 4 (mm)	**Leg 5 (mm)**	**Leg 6 (mm)**
Adjust 1 (A)	-0.20	-0.24	-1.31
Adjust 2 (A)	-0.70	-0.51	-0.25
Adjust 3 (A)	0.23	0.05	0.04
Adjust 4 (A)	-	-	-0.33
Adjust 5 (A)	-	-0.94	-0.91
Adjust 6 (A)	-	-0.94	-
Adjust 7 (A)	-	-	-1.47

Table A.11: Warpage change, for Product B, after the application of each adjust measured by the Sorter: Pre-Aligner equipment.

	Leg 4 (mm)	**Leg 5 (mm)**	**Leg 6 (mm)**
Adjust 1 (A)	-2.22	-1.78	-2.00
Adjust 2 (A)	-1.77	-2.19	-2.61
Adjust 3 (A)	-0.04	-0.83	0.24
Adjust 4 (A)	-	-	-1.32
Adjust 5 (A)	-	0.21	-1.95
Adjust 6 (A)	-	-1.13	-
Adjust 7 (A)	-	-	-0.72

Table A.12: Warpage change, for Product B, after the application of each adjust measured by the Sorter: Plain Chuck equipment.

	Leg 4 (mm)	**Leg 5 (mm)**	**Leg 6 (mm)**
Adjust 1 (A)	-0.25	-0.20	-1.74
Adjust 2 (A)	-0.49	-0.37	0.93
Adjust 3 (A)	0.17	0.27	-0.90
Adjust 4 (A)	-	-	-2.03
Adjust 5 (A)	-	0.04	-0.86
Adjust 6 (A)	-	-0.69	-
Adjust 7 (A)	-	-	-0.44