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Development of a LoRaWAN End Node Focusing on Antenna Miniaturization Techniques

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Abstract

Compact LoRaWAN end nodes are becoming increasingly sought-after due to their wide range of applications on the Internet of Things industry. The battery life and communications range of these devices are significantly related to antenna efficiency, because highly efficient antennas require low input power to achieve the intended radiated power, reducing power consumption and increasing battery life. However, smaller antenna sizes, needed for compact devices, negatively impact efficiency and other antenna parameters. In fact, antennas that are considerably smaller than the wavelength achieve this size reduction at the cost of reduced efficiency, bandwidth, gain and even distortions to the radiation pattern. For that reason, it is challenging to design small but performant antennas.

This dissertation covers the development and testing of a compact, low-power and very thin LoRaWAN end node. This was made possible by using a printed inverted-F antenna design and by placing the device's electronics in the antenna's densely via stitched ground planes (technically, ground block). The proposed antenna has 60 MHz bandwidth, an efficiency of 96.43% and a simulated realized gain of 2 dBi.

The end node occupies an area of 67.11 cm² (about the size of an adult's palm) and has a thickness of 1.793 cm (mainly limited by battery size as the device without battery is just 4 mm thick).

Resumo

Tem existido um aumento crescente na procura de terminais compactos LoRaWAN, devido à sua ampla gama de aplicações na indústria da Internet das Coisas. A vida útil da bateria e o alcance de comunicação destes dispositivos estão significativamente relacionados com a eficiência da antena, uma vez que antenas altamente eficientes requerem baixa potência de entrada para atingir a potência radiada pretendida, reduzindo o consumo de energia e aumentando a vida útil da bateria. No entanto, o tamanho reduzido de antenas miniatura, necessário para dispositivos compactos, afeta negativamente a eficiência e outros parâmetros da antena. Na verdade, antenas consideravelmente menores do que o comprimento de onda em que operam alcançam esta redução de tamanho em detrimento da eficiência, largura de banda ou ganho reduzido e até mesmo distorções no padrão de radiação. Por esta razão, é desafiante projetar antenas pequenas, mas com bom desempenho.

Esta dissertação abrange o desenvolvimento e teste de um terminal LoRaWAN compacto, de baixo consumo e fino. Isto foi possível através do uso de uma antena em F invertido impressa e colocando a eletrónica do dispositivo nos dois planos de terra densamente interligados por vias (tecnicamente um de bloco de terra). A antena proposta possui uma largura de banda de 60 MHz, uma eficiência de 96,43% e um ganho simulado de aproximadamente 2 dBi.

O terminal apresenta uma área total de 67,11 cm² (aproximadamente do tamanho da palma de uma mão de adulto) e uma espessura de 1,793 cm (principalmente limitada pelo tamanho da bateria, sem a qual a espessura do dispositivo é somente 4 mm)."

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"We stigmatize mistakes. And we're now running national educational systems where mistakes are the worst thing you can make — and the result is that we are educating people out of their creative capacities. For most of us the problem isn't that we aim too high and fail. It's just the opposite: we aim too low and succeed. Human communities depend upon a diversity of talent, not a singular conception of ability. And at the heart of the challenge is to reconstitute our sense of ability and intelligence. Being in your element is not only about aptitude, it's about passion: it is about loving what you do."

Sir Ken Robinson

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Abbreviations

ABP	Activation By Personalization
ADC	Analog-to-Digital Converter/Conversion
CPWG	CoPlanar Waveguide with Ground
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter/Conversion
DGS	Defected Ground Structure
DSDGS	Dumbbell-Shaped Defected Ground Structure
DUT	Device Under Test
eMMB 5G	Enhanced Mobile Broadband 5G
ERP	Equivalent Radiated Power
ETSI	European Telecommunications Standards Institute
eMMB FR4	Flame Retardant number 4 with glass-reinforced epoxy
FSCM	Frequency Shift Chirp Modulation
GA	Genetic Algorithm
GPIO	General-Purpose Input/Output
GPS	Global Positioning System
HPBW	Half Power Beam Width
ICT	Information and Communication Technologies
IFA	Inverted-F Antenna
INESC TEC	Instituto de Engenharia de Sistemas e Computadores, Tecnologia e Ciência
IoT	Internet of Things
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Sound
LDO	Low DropOut
LPWAN	Low-Power Wide-Area Network
LoRa	Semtech's proprietary FSCM modulation
LoRaPHY	LoRa PHYsical layer protocol
LoRaWAN	LoRa Wide-Area Network
LoS	Line of Site
MAC	Medium Access Control
MCU	Micro-Controller Unit
MIC	Message Integrity Code
MPIFA	Meandered Printed Inverted-F Antenna
N/A	Not Applicable
NB-IoT	Narrow-Band Internet of Things
NMOS	N-type Metal Oxide Silicon field effect transistor

OTA	Over-The-Air
OTAA	Over-The-Air Activation
PCB	Printed Circuit Board
PIFA	Printed Inverted-F Antenna
PLF	Polarization Loss Factor
PMOS	P-type Metal Oxide Silicon field effect transistor
SRAM	PseudoStatic Random Access Memory
RFID	Radio-Frequency ID
RSSI	Received Signal Strength Indicator
RTC	Real-Time Clock
SF	Spreading Factor
SPI	Serial Peripheral Interface
SMD	Surface Mount Device
SNR	Signal-to-Noise Ratio
SMA	SubMiniature version A
SRAM	Static Random Access Memory
TTN	The Things Network
UART	Universal Asynchronous Receiver- Transmitter
VNA	Vector Network Analyzer
Wi-Fi	IEEE 802.11 set of standards
WiMax	Worldwide interoperability for Microwave access (IEEE 802.16 set of standards)
2D	2 Dimensions/2-Dimentional
3D	3 Dimensions/3-Dimentional
5G	3GPP's fifth-generation technology standard for broadband cellular networks

Symbols

BW	Bandwidth
T_{chip}	Chip period
C	Number of chips per symbol
T_{symbol}	Symbol period
N	Number of different symbols
M	Number of bits per symbol
r	Distance (spherical coordinate system)
θ	Inclination angle (spherical coordinate system)
ϕ	Azimuthal angle (spherical coordinate system)
$\mathcal{E}$	Electric field vector
$\mathcal{H}$	Magnetic field vector
$\mathcal{W}$	Instantaneous Poynting field vector
$\mathcal{P}$	Instantaneous power density
W_{av}	Average power density
W_{rad}	Radiated power density
P_{av}	Average radiated power
P_{rad}	Radiated power
U	Radiation intensity
e_{cd}	Conduction-dielectric efficiency
P_{in}	Input power
R_{rad}	Radiation resistance
R_{loss}	Loss resistance
G	Gain
A_{eff}	Effective area
Z_{in}	Input impedance
R_{in}	Input resistance
X_{in}	Input reactance
$\hat{\rho}_{\text{a}}$	Antenna polarization vector
$\hat{\rho}_{\text{w}}$	Wave polarization vector
ψ_{p}	Angular separation between $\hat{\rho}_{\text{w}}$ and $\hat{\rho}_{\text{a}}$
D	Antenna directivity
f	Wave frequency
f_{r}	Resonant frequency
λ	Wavelength
λ_0	Wavelength of light in free-space vacuum
v	Wave velocity
v_0	Speed of light in free-space vacuum

n	Refractive index
ϵ_r	Relative electric permittivity
ϵ_{eff}	Effective electric permittivity
μ_r	Relative magnetic permeability
L	Antenna length
W	Antenna width
W_S	Short width
ΔL_{eff}	Difference between the physical and electrical antenna length

Chapter 1

Introduction

1.1 About the Proponents

Wavecom - Soluções Rádio SA [1] is a Portuguese communications engineering firm specialized in Information and Communication Technologies (ICT) and on the Internet of Things (IoT). They provide solutions for Radio-Frequency ID (RFID) localization, high-density Wi-Fi coverage, microwave point-to-point links, smart systems and several other wireless technologies.

Instituto de Engenharia de Sistemas e Computadores, Tecnologia e Ciência (INESC TEC) [2] is a Portuguese private non-profit institution focused on scientific research, technological development, advanced consulting, and pre-incubation of new technology-based companies.

Wavecom was the proponent of this Master's dissertation, which was made possible due to the collaboration of INESC TEC. This work is about IoT product development and antenna design research. Wavecom defined the product requirements, which are described at the beginning of Chapter 5. INESC TEC provided all the required lab equipment, software tools and technical supervision.

1.2 Context

The European Union's *Internet of Things Policy* and its *Digital Targets for 2030* aim to promote emerging IoT technologies and to empower IoT businesses by investing around €95.5 million in related research and development, until 2027 [3]. These and other new digitalization objectives for European states, institutions and companies have led to a quick spread of Low Power Wide Area Networks (LPWANs). In these networks, compact and low-power end-nodes are becoming increasingly sought-after, because these characteristics allow devices to contribute to the optimization of processes and resources in various industries and areas of society. These include the logistics and storage industries, smart agriculture, fleet management, parking availability management, crowd monitoring, smart cities and many other applications where terminals are required to run on batteries for extended periods of time and/or to fit in small spaces (for instance, in smart building applications as shown in [4]).

For most applications, LoRaWAN end-nodes consist of mainly sensors and very simple actuators, if any. This means that radio transmission usually represents one of the biggest contributions for the total power consumption. Additionally, these devices may transmit and receive several LoRaWAN messages per day, which, after the years of battery life end nodes are supposed to have, start to add up to a considerable sum. This is why efficient antennas are required, especially for the more space constricted application [5]. However, this creates the challenge of designing efficient, compact end-nodes that can achieve a comparable communication range to their normal-sized counterparts.

1.3 Motivation

The first United States patent for LoRa was submitted in 2010 [6] and the LoRa Alliance was officially formed in 2015 [7]. LoRa is a recent technology and, because of that, academic research in the topic is limited. This has been noted by other authors such as Trinh *et al.* in [8, p. 171]. Due to the growing popularity of LPWANs, network-level research has been increasing. Nevertheless, LoRa hardware research, specially LoRa antenna design research, has yet to follow this trend. The lack of research work on this topic is, by itself, one of the motivating factors for this dissertation, despite not being the main one.

Reducing the size of an antenna always comes at a cost, be it gain, radiation pattern distortion, efficiency or bandwidth. For each use case, antenna designers select which of these parameters they are willing to trade for a reduction in size. Consequently, it is not possible to use one single miniaturization technique to develop antennas for every technology. This is because the antenna parameter that can be affected is different for each use-case. For instance, broadband wireless communication technologies used for the transmission of multimedia content, such as Wi-Fi, WiMax or Enhanced Mobile Broadband 5G (eMMB 5G), cannot support a reduction in bandwidth as a way to reduce size. When designing antennas for these communication standards it is best to reduce efficiency instead of bandwidth. For Bluetooth antennas it might be preferable to reduce size at the cost of gain and not at the cost of efficiency or bandwidth, since Bluetooth is made for short-range and low-power communications. In other words, the techniques used to miniaturize antennas are dependent on the use case of the device. This is exemplified in Table 1.1.

LoRa devices, having completely different characteristics in terms of power usage and bandwidth, can benefit from miniaturized antennas developed specifically for this technology, rather than generic miniature antennas made for the required frequency bands. Due to the very small bandwidth of LoRa systems, techniques that reduce bandwidth in exchange for a decrease in size are enticing, even though they are not viable for other technologies. LoRa operates on a band that is 17 MHz wide, using only 125 kHz per channel. As a comparison, for the 2.4 GHz band, the IEEE 802.11b/g/n Wi-Fi standard defines 14 22 MHz overlapping channels with a separation of 5 MHz, resulting in a total bandwidth of around almost 100 MHz. Besides, efficiency and gain should be preserved as much as possible, as these are extremely important for LoRa antennas, due to the long-range and low-power requirements of LPWANs.

LoRa operates on the EU863-870 ISM band (in most of Europe), with a wavelength of around 30 cm. This means that antennas that are even 5 to 6 times smaller than the wavelength are still significantly large and, to achieve small devices, integration of the antenna with the end node's electronics is almost inevitable. As a result, more research needs to be conducted in order to understand which antenna designs are most suitable for integration with the rest of the device's systems.

Therefore, miniature antennas, made using LoRa-specific techniques and designed for easy integration with the rest of the device's electronics, can contribute to the development of compact end nodes that are still energy efficient and have long-range. This was the main motivation for this dissertation.

Technology	Target	Objective	Miniature antennas should...	
			preserve...	at the cost of...
Bluetooth	Personal Area Networks	short range low power medium data rates	efficiency	gain
Wi-Fi	Local Area Networks	medium range high data-rates	bandwidth	efficiency
LoRaWAN	Wide Area Networks	long range low power low data rates	gain efficiency	bandwidth

Table 1.1: Comparison of the parameters that antenna designers usually compromise in order to achieve size reduction, depending on the target technology [9].

1.4 Objectives

The first objective of this dissertation was to develop a compact LoRaWAN end-node, using a miniature antenna designed specifically for LoRa devices, that achieves a small size using miniaturization techniques customized for this technology and that can be easily integrated with the rest of the end-node's systems. The compactness of the device inevitably affects gain and efficiency, but this work focuses on also preserving range and power consumption so that the end-node can be used for several use-cases. In other words, this work aims to achieve the best possible performance/size ratio. This objective involves the design, simulation and characterization of a miniaturized LoRa antenna as well as integrating it in a LoRaWAN end-node by designing and testing a printed circuit board (PCB) with multiple sensors, a microcontroller unit (MCU), power management electronics and the antenna itself.

Another objective was to extensively characterize the antenna and test the end-node in real-world scenarios, understanding how it performs in complex radio situations that might involve

multipath fading, Fresnel zone obstructions and several factors that are particularly difficult to replicate in a laboratory environment.

1.5 Contributions

This work makes significant contributions to both the industry and the state of the art in the field of compact LoRaWAN end nodes and antenna design. By successfully developing and testing a compact, low-power, and thin LoRaWAN end node, the dissertation addresses the growing demand for compact devices in the IoT industry.

The proposed antenna design demonstrates a very interesting performance/size ratio. The dissertation's findings shed light on the challenges associated with designing small but performant LoRa antennas and offer insights into mitigating the negative impacts of reduced antenna size, such as decreased efficiency, bandwidth, gain, and distortion in the radiation pattern.

The research conducted on dumbbell-shaped defected ground structures for sub-gigahertz antennas and their impact on gain not only expands the current understanding of the viability of such techniques, but also proposes alternative techniques for enhancing gain in these specific frequency bands. These findings provide valuable insights for future antenna designs and pave the way for further advancements in compact LoRa devices.

Furthermore, the dissertation presents practical solutions for optimizing battery life and power consumption in compact end nodes. The implemented power management system, selective activation of components, and support for external sensors and actuators contribute to energy efficiency and flexibility in various application scenarios.

Overall, this Master's dissertation significantly contributes to the industry and the state of the art by addressing the challenges and requirements of compact LoRaWAN end nodes. The developed end node, along with its antenna and power management system, offers practical and efficient solutions for IoT applications, opening up new possibilities for the development of compact and high-performance devices in the field.

1.6 Document Structure

Chapter 2 covers some fundamental aspects of the concepts relevant to this dissertation. These include the LoRa modulation as well as the LoRaWAN standard, its protocol stack and network architecture. Fundamentals of antenna theory, particularly the most important parameters for antenna characterization, are also covered in this chapter.

Chapter 3 covers the state of the art regarding antenna miniaturization techniques. The first sections provide a general overview of these techniques as well as some of the most common miniature antenna designs, with an emphasis on inverted-F antennas (IFAs), which is the type of antenna used in this dissertation. This chapter also focuses on research regarding miniature LoRa antennas, what types of antenna miniaturization techniques were previously implemented in the development of LoRa antennas and what results were achieved. The final part of the chapter

describes where this dissertation fits in the state of the art and what impact it aims to have in the field of miniature LoRa antennas and compact, low-power LoRaWAN end nodes.

Chapter 4 covers the development of a narrowband Printed Inverted-F Antenna (PIFA), which serves as a miniature LoRa antenna for the end node. This chapter also describes experimental simulations that were made with the goal of evaluating the effects of different miniaturization techniques, DGSs and ground plane configurations on the antenna. The conclusion drawn in these simulations led to the choices made in the final antenna design.

Chapter 5 covers the development of the end node, focusing on the different variants that were designed and on all systems including power, communications and sensors. This chapter also describes the research work related to the choice of batteries, transmitter, MCU and other important parts of the device.

Chapter 6 covers the experimental setup and a detailed description of the antenna characterization and device tests that were put together during the project. These include Vector Network Analyser (VNA) and anechoic chamber characterizations, range tests and power consumption tests.

Chapter 7 lays out the main takeaways of this dissertation and describes future work that could be done in the wake of this work.

Chapter 2

Background

2.1 LoRa

LoRa is a proprietary modulation (patents [6] and [10]) that enables low bit rate, low-power and long-range communications. It was originally developed for the metering industry [11], however it quickly became a very impactful technology in the more broad field of IoT, where devices frequently need to meet strict power consumption requirements.

LoRa works on license-free sub-gigahertz radio frequency bands such as the EU863-870 ISM band. It can achieve data rates between 0.3 kbit s^{-1} and 27 kbit s^{-1} , depending on a parameter called spreading factor, that is covered in Subsection 2.1.1, and also depending on the system's bandwidth. Due to the characteristics of the modulation, LoRa systems usually have a high link budget and receivers with sensitivities of around -140 dBm are very common. According to Semtech, the proprietary firm, LoRa devices are capable of communications of up to 15 km [12]. Despite this, the world distance record for ground-to-air LoRa communications is 832 km, using just 25 mW of transmitting power [13]. The record for ground-to-ground communications is 212 km [14]. These results highlight the resilience and long-range capabilities of LoRa technologies and the impact they can have on the IoT industry, specially for long-range, low-power and low-availability applications.

2.1.1 The LoRa Modulation

LoRa is the modulation used by the physical layer protocol of the LoRaWAN specification (covered in Section 2.2), know as LoRaPHY (covered in Subsection 2.1.2). It is best described as a Frequency Shift Chirp Modulation (FSCM) as noted by Vangelista:

A close inspection of LoRa reveals that the information bearing element is the frequency shift at the beginning of the symbol and the chirp is similar to a kind of carrier. For this reason, in our opinion, LoRa is better described as a Frequency Shift Chirp Modulation (FSCM) [15, p. 1818].

A linear frequency chirp, LoRa chirp or, for the purposes of this document, just chirp, is a signal in which frequency varies linearly with time. Chirps can have a constant positive (up-chirp) or

negative (down-chirp) frequency variation. Each LoRa chirp sweeps over the complete range of frequencies that represent the bandwidth of the system, BW .

The duration of each LoRa chirp depends on the number of time chips of each symbol. A time chip is a portion of time that depends on the system bandwidth and is given by $T_{\text{chip}} = \frac{1}{BW}$. The number of time chips per symbol, C , depends on the spreading factor, SF , and is given by $C = 2^{SF}$. Therefore, the duration of each symbol, T_{symbol} , is $T_{\text{symbol}} = C \times T_{\text{chip}} = 2^{SF} \times T_{\text{chip}}$.

Because LoRa systems operate with a fixed bandwidth, the duration of each time chip is fixed as well. Hence, SF is the parameter that really affects how much a symbol "spreads" in time. The higher the SF , the longer the symbol period. Table 2.1 shows the radio packet airtime for each SF , when sending 1 byte of application data with the least overhead possible. Figure 2.1 shows the spectrogram of the same symbol transmitted with $SF7$ to $SF12$, demonstrating the effect of the SF in the spectrogram of a symbol.

SF	Airtime (ms)	Bandwidth (kHz)
7	23.2	250
7	46.3	125
8	82.4	
9	164.9	
10	288.8	
11	577.5	
12	1155.1	

Table 2.1: Symbol airtime for different SFs , when sending one byte of application data..

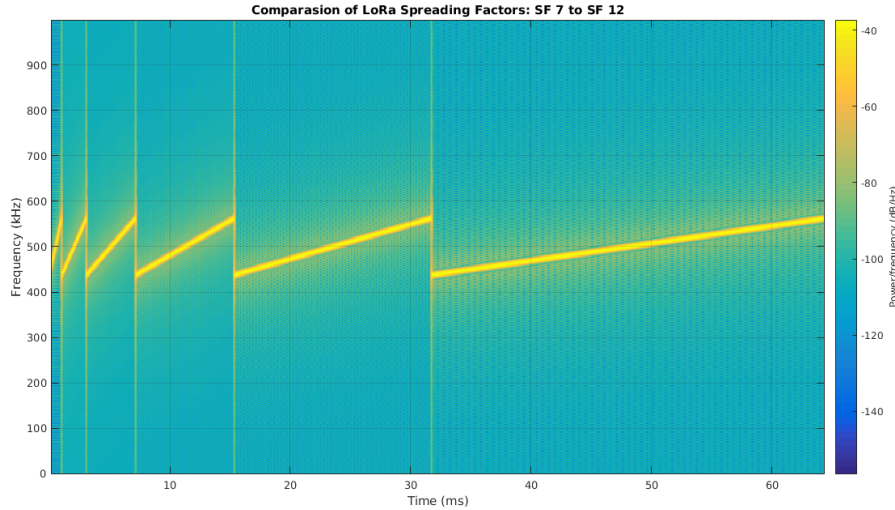


Figure 2.1: Spectrogram of the same symbol (up-chirp) using different SFs from $SF7$ to $SF12$ [16].

Each LoRa symbol consists of a chirp with a vertical discontinuity located at one of the time chips. This discontinuity is simply a frequency shift from the frequency the signal is at in the beginning of the chip to the lowest frequency available. After the chip, the signal continues the frequency sweep from that lowest frequency until reaching the starting frequency again, covering

the whole bandwidth. In other words, each LoRa symbol is a linear frequency sweep rolled back to the lowest frequency somewhere during the symbol period. This means the number of different symbols, N , for each SF is equal to the number of time chips ($N = C$). Figure 2.2 shows different symbols for SF7.

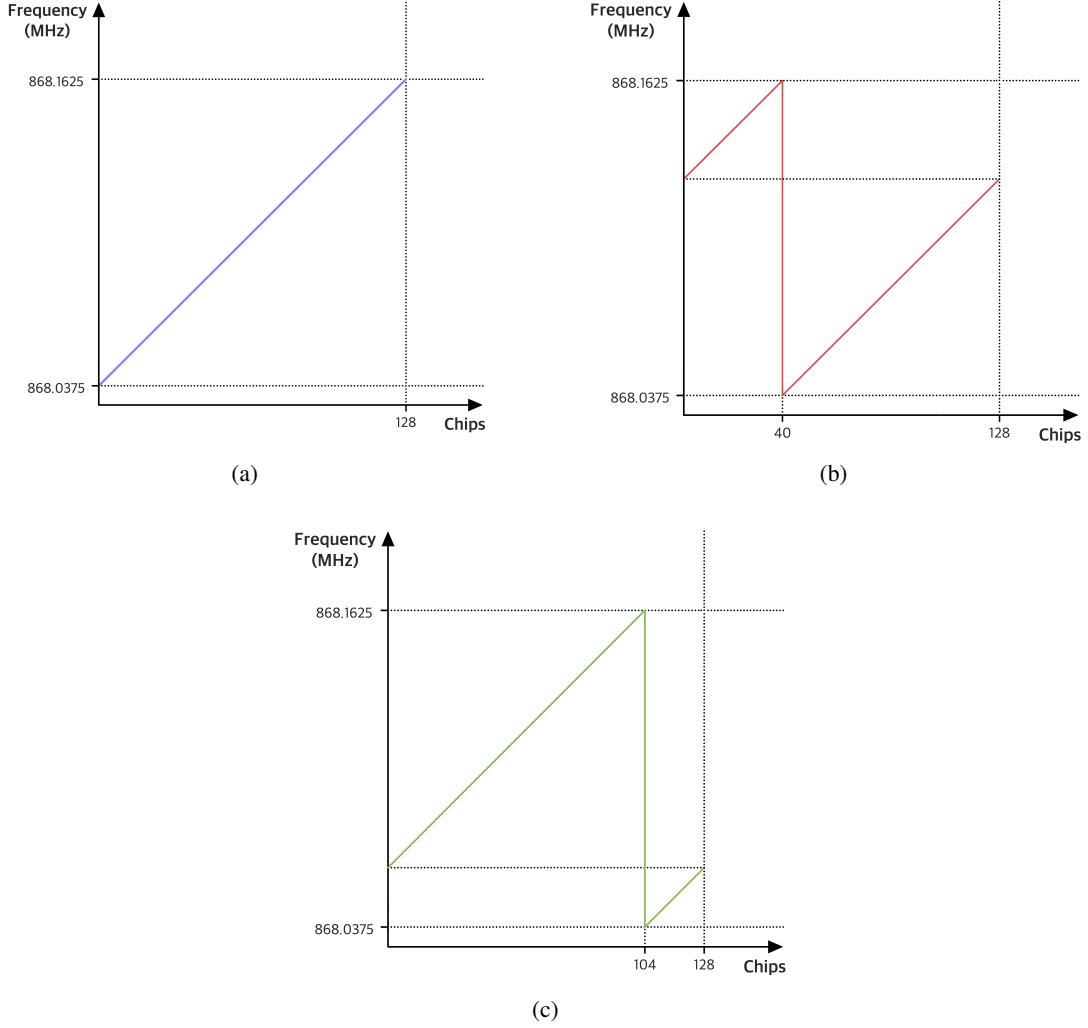


Figure 2.2: Example of three downlink LoRa symbols for the 868.1 MHz channel with $SF = 7$: (a) symbol 0 (up-chirp), (b) symbol 39 and (c) symbol 103.

The number of bits per symbol, M , is equal to the SF ($M = SF$). This means that for larger SFs, each symbol carries more information. At first sight, this might seem to imply that larger spreading factors provide larger bitrates. However, and according to Table 2.1, for an increase of 1 in the SF, it takes double the time to transmit each symbol (because we have $\frac{2^{SF_m+1}}{2^{SF_m}} = 2^{SF_m+1-SF_m} = 2$ times more time chips). The effect of this increase in symbol period overcomes the effect of the increase in bits per symbol and the resulting net effect is an actual decrease in bit rate with the increase of the SF. Table 2.2 shows the bit rate and airtime for each SF, using the LoRaWAN regional parameters for Europe [17].

SF	Bit Rate (bit/s)	Airtime (ms)	Bandwidth (kHz)
7	11000	23.2	250
7	5470	46.3	125
8	3125	82.4	
9	1760	164.9	
10	980	288.8	
11	440	577.5	
12	250	1155.1	

Table 2.2: Bit rate and airtime (when sending 1 byte of application data) as a function of SF.

Because LoRa uses correlation-based demodulators, larger SFs (and, consequently, larger symbol periods) generate increased processing gain and higher reception sensitivity, but reduce bitrate [18]. This balance between range and bitrate is a crucial consideration when designing LoRa systems, due to the duty cycle restrictions imposed on the EU863-870 ISM band. Lower bitrates lead to longer message transmissions and reduce the number of messages a device is allowed to transmit per day without violating regulations. Additionally, longer transmissions also result in higher power consumption which is a disadvantage in low-power applications.

2.1.2 LoRaPHY

LoRaPHY is the physical layer protocol of the LoRaWAN protocol stack. Physical layer radio packet formats depend on the type of message, which can be an uplink or downlink message. Figure 2.3 shows packet formats for each of these message types.

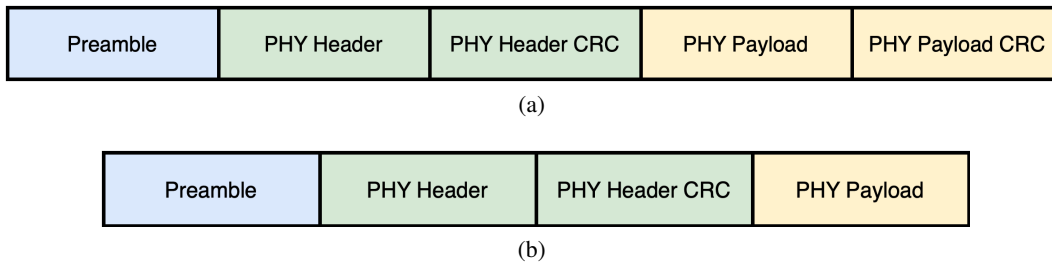


Figure 2.3: LoRa Radio Packet Format for (a) uplink and (b) downlink communications .

The LoRa modulation is proprietary. Nevertheless, by waveform analysis, it is possible to get some information about packet structure at the radio level. As noted by El Rachkidy *et al.*:

In uplink communications, the preamble consists of up-chirps and the data consists of down-chirps. In downlink communications, the preamble consists of down-chirps and the data consists of up-chirps [19, .p 2].

Radio packet preambles are between 10 and 65539 symbols long (default is 12) and should be used by the receiver to synchronize with the incoming data flow. LoRa radio packet headers indicate the payload length, the forward correction error code rate and the presence of the optional

payload cyclic redundancy check (CRC) that is present only on uplink messages. Headers also have a mandatory CRC field. The payloads of the physical layer radio packets contain the link layer frames described in Subsection 2.2.2.

2.2 LoRaWAN

LoRaWAN is a LPWAN standard maintained by the LoRa Alliance, an open, non-profit association with the mission of promoting the standard, which the organization claims to be the leading IoT LPWAN specification.

The LoRaWAN specification defines the protocol stack, the regional parameters and the network architecture. The protocol stack comprises the LoRaPHY physical layer protocol and the LoRaWAN network protocol [20], which actually covers both the link and network layers. The network parameters [17] specify important variables. Namely, channel frequency, channel bandwidth and the transmission windows for LoRaWAN communications all over the world. The network architecture standardizes the overall network structure, the function and naming of each device type and the relations and interactions between network nodes.

2.2.1 Network Architecture

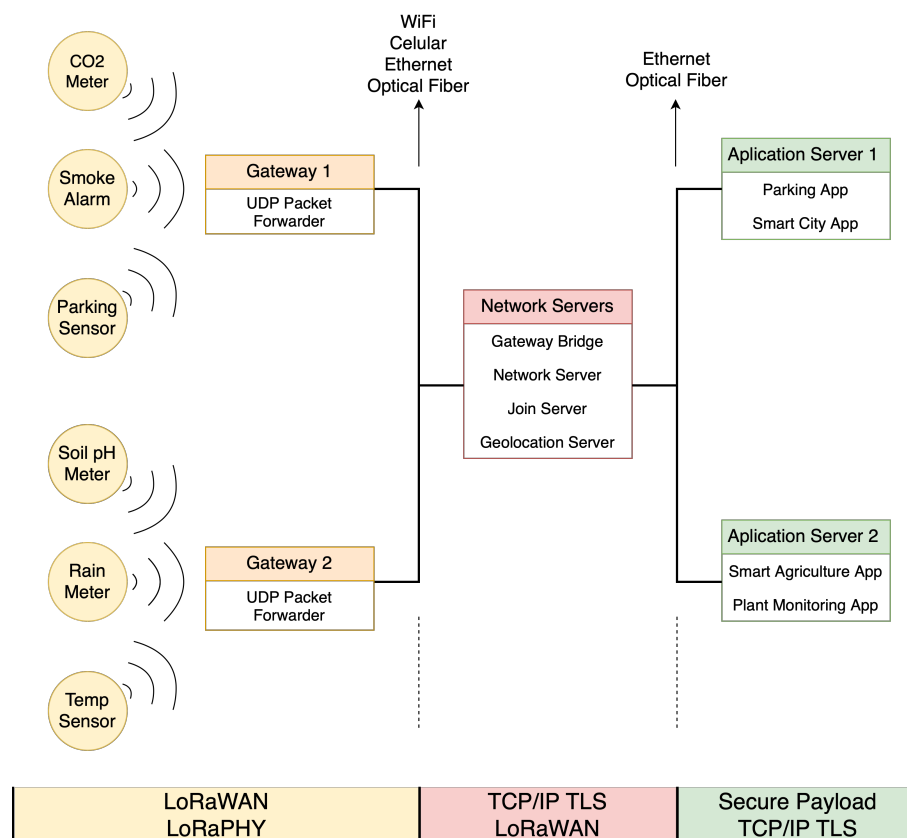


Figure 2.4: LoRaWAN network in a star topology.

LoRaWAN networks use a star topology, as illustrated in Figure 2.4. These networks consist of end-nodes/end-devices, gateways, network servers and application servers.

The working of gateways is explained in The Things Network (TTN) website:

Each gateway is registered (using configuration settings) to a LoRaWAN network server. A gateway receives LoRa messages from end devices and simply forwards them to the LoRaWAN network server. Gateways are connected to the Network Server using a backhaul like Cellular (3G/4G/5G), WiFi, Ethernet, fiber-optic or 2.4 GHz radio links [21].

Network servers manage the whole network. They filter duplicate messages received from several gateways, route uplink application payloads to the correct application server, provide acknowledgments of messages, send Adaptive Data Rate (ADR) messages, handle join requests and execute many more security- and network-related functions.

Application servers process application-layer payloads and generate downlink application messages (downlink Medium Access Control (MAC) commands, which are network and end-node control messages are generated by network servers).

End-nodes are usually made up of microcontrollers connected to sensors, actuators, or both. These devices are usually battery-powered, have LoRa modulators and implement the LoRaWAN protocol stack in firmware. Every end-device must be registered with a network before sending and receiving messages. The process of joining a network is called "end-device activation". An end-node can be permanently tied to a pre-selected network using Activation By Personalization (ABP) or it can search and request to join a network using over-the-air activation (OTAA).

Devices that are part of a network with location-aware gateways can have GPS-free geolocation capabilities using a trilateration technique based on timestamps sent from the network [22].

2.2.2 LoRaWAN Network Protocol

The LoRaWAN Network Protocol is the link and network layer protocol of the LoRaWAN protocol stack (illustrated in Figure 2.5).

Link layer frames are the payload of the physical layer LoRaPHY radio packets described in Subsection 2.1.2. Some frame types are used only during the join process of new end-nodes. However, the main type of link layer message, the one that is shown in Figure 2.5, contains three fields: a header, a payload and a message integrity code (MIC). Link layer frame headers include some information about the message type. Message types include confirmed and unconfirmed data messages, join and rejoin requests, MAC command and even proprietary message types, used to implement non-standard types. The payload contains the network layer packets. The MIC serves a different purpose than the CRC fields in the physical-layer protocol. Whilst CRC fields are used for error detection and correction, MIC fields are used for security purposes, allowing the receiver to determine if the message has been changed.

The link layer payload can be considered the network layer packet of the LoRaWAN specification. Still, the official documentation refers to these network layer packets as "MACPayload"

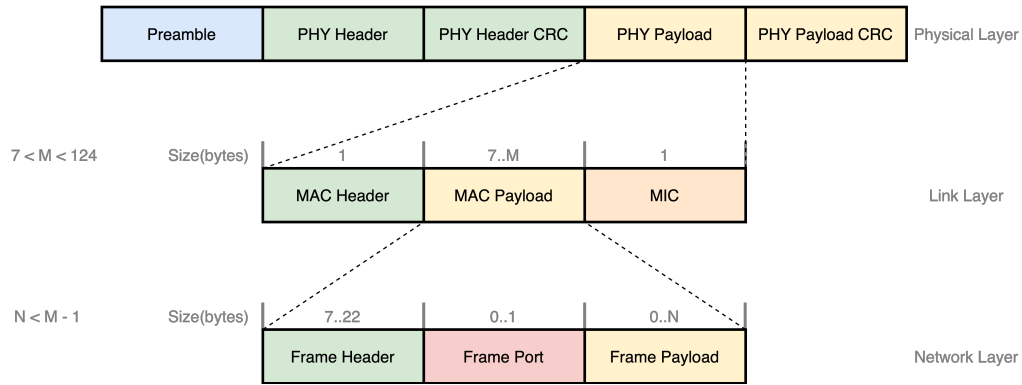


Figure 2.5: Representation of LoRaPHY radio packets, LoRaWAN link layer frames and network layer packets. The size of the physical radio packets is not specified because it is measured in symbols (not bytes) and it is highly variable as preamble and header length depends on the hardware (not on the LoRaWAN standard).

frames, since the ISO/IEC 7498-1 model definitions of link and network layers do not strictly apply to LoRaWAN networks. These frames contain a frame header, an optional port field and an optional payload. The header contains the end-device device address, a frame counter, an adaptive data rate field and several other frame options fields. The port field allows for protocol testing and for future standardized application extensions. The payload contains the encrypted application-layer data.

2.2.3 Device Classes

The LoRaWAN standard supports three device classes: class A (from "All End-Devices"), class B (from "Beacon") and class C (from "Continuously Listening"). Device classes are backwards compatible, meaning that class C devices are class A and class B compatible and class B devices are class A compatible (but not class C compatible). The main difference between classes has to do with reception and transmission windows. The transmission window schemes for each class are illustrated in Figure 2.6.

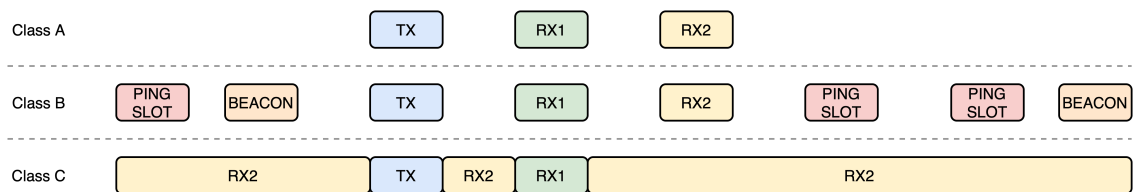


Figure 2.6: LoRaWAN classes' transmission windows.

Class A focusses on obtaining extremely low power consumption at the cost of device availability. For devices from this class, the default state is a low power one, such as a light sleep or even complete device hibernation. Essentially, class A end-nodes only wake for transmission, having two reception windows available after the end of transmission. The time interval between the transmission window and the reception windows is specified in the regional parameters' specification of the LoRaWAN standard [17]. Even though two reception windows are open after transmission,

only one of them can actually be used for downlink messages, meaning that if a message is received in the first reception window the second one will not be available. Class A devices are very rarely available to receive downlinked commands from the network. Thus, most class A end-nodes are unidirectional or telemetry oriented devices that broadcast data without accepting, or accepting very few, commands. These include meters such as water, temperature, noise, current, voltage and light sensors or monitoring devices like parking, Time of Flight and motion sensors. Class A devices are commonly included in time-insensitive and loss-tolerant applications.

Class C is the complete opposite of class A. It focusses on device availability and neglects energy saving. Unlike most class A end-nodes, devices from this class are usually connected to mains power and not battery powered. They are continuously available for reception, except during transmission. Class C end-nodes usually need to receive large amounts of data or several commands from downstream messages and are implemented in more time and response-sensitive applications.

Class B devices are an intermediate class that aims to achieve low power consumption while still offering frequent, but intermittent, reception windows, called ping slots. Devices from this class need to search and receive network beacons that allow synchronization with the network and avoid drifts between the device's internal clock and network timing. A device might be unable to receive beacons due to being out of a gateway's range, the network being down or interference. In such event, class B devices gradually widen their reception windows to accommodate a possible drift of the device's internal clock and to try to recover the network beacon. Class B devices ought to operate "beaconless" for at least two hours before downgrading to class A operation, resetting or turning off.

2.2.4 EU863-870: Restrictions

The EU863-870 band, the one LoRa devices operate in, is an unlicensed but extremely restrictive band. Understanding its characteristics is important when developing LoRa devices.

Sub-Band Designation	Frequency Range (MHz)	Maximum Duty Cycle	Maximum ERP (mW)
K	863-865	0.1%	25
L	865-868	1%	25
M	868-868.6	1%	25
N	868.7-869.2	0.1%	25
P	869.4-869.65	10%	500
Q	869.7-870	1%	25

Table 2.3: ETSI duty cycle and ERP restrictions for each sub-band of the EU863-870 band [23].

Three main sets of restrictions are imposed on the band. The first are the Equivalent Radiated Power (ERP) and duty cycle restrictions imposed by the European Telecommunications Standards

Institute (ETSI), the body responsible for the standardization of information and communication technologies in Europe. These are presented in Table 2.3.

The Things Network, the largest global open LoRaWAN network, explains the correct use of each EU863-870 sub-band:

Usually, the limitations of sub-bands K, L, M, N and Q are applied for uplink transmissions and the limitations of sub-band P are mainly applied for downlink transmissions. Usually, a number of end devices in a LoRaWAN network is way higher than a number of gateways. Gateways can therefore run into their duty cycle limit quicker than end devices. LoRaWAN's RX2 channel is normally chosen to fall into sub-band P in order to benefit from the higher duty cycle limit, and provide 10x more downlinks to gateways instead of end devices. By default, the RX1 receive window for downlinks uses the same frequency as the preceding uplink, while the RX2 receive window uses a fixed frequency, with the default being 869.525 MHz at DR0 using SF12 with 125 kHz. In Europe 869.525 MHz is used for Class B beacon transmissions and ping slots. [24].

On top of ETSI's restrictions there are the restrictions imposed by the LoRa Alliance. With which all devices must comply if they are to be certified LoRaWAN devices. These are presented in Figure 2.7. This figure shows that default channels, which must be supported by every single LoRaWAN device, are all 868 MHz-based. This is why LoRa antennas are designed to operate at this frequency, even if it is not the centre frequency of the band. It is also important to note that the LoRa Alliance does not certify devices with gains larger than 0 dBd (2.15 dBi).

The last set of restrictions only apply to devices on non-private networks. Network operators might impose even more limitations on top of both ETSI and LoRa Alliance restrictions. For instance, the aforementioned The Things Network imposes an additional set of restrictions on devices called Fair Access Policy.

Default frequency band	863-870 MHz
Mandatory channel frequencies (join-request)	868.10 868.30 868.50
Mandatory data rates	0-5 (minimum set supported for certification)
Optional data rates	6-7 or 6-11
Number of channels	16 3 default + 5 optional by CFList These 5 optional channels and the remaining 8 channels can be modified /populated by NewChannelReq command
Default channels	0, 1, 2
Duty cycle	< 1%
Dwell time limitation	No
Max EIRP / ERP	+16 dBm (40 mW) / +14 dBm (25 mW) This is the power radiated by the isotropic antenna / half-wave dipole antenna (not the transmitter power)
Max antenna gain	2.15 dBi or 0 dBd
Default RX2 data rate	DR0 (SF12 / 125 kHz)
Default RX2 frequency	869.525 MHz

Figure 2.7: LoRa Alliance's restrictions for the EU863-870 [25].

2.3 Antenna Fundamentals

An antenna is a device that serves as the interface between electromagnetic waves propagating in a medium and electric currents flowing in metal conductors. An antenna's performance is characterized by a number of fundamental parameters. These are covered in the subsections that follow.

To understand various antenna parameters, a 3D representation of the space surrounding the antenna is needed. In this document, 3D space is represented using the spherical coordinate system shown in Figure 2.8. In this system, an antenna is located at the origin of the coordinate system, O , and r represents the distance from a given point, P , to the antenna. θ and ϕ represent, respectively, the inclination and azimuthal angles of a given point. x , y , z represent the orthogonal axis of 3D Cartesian space.

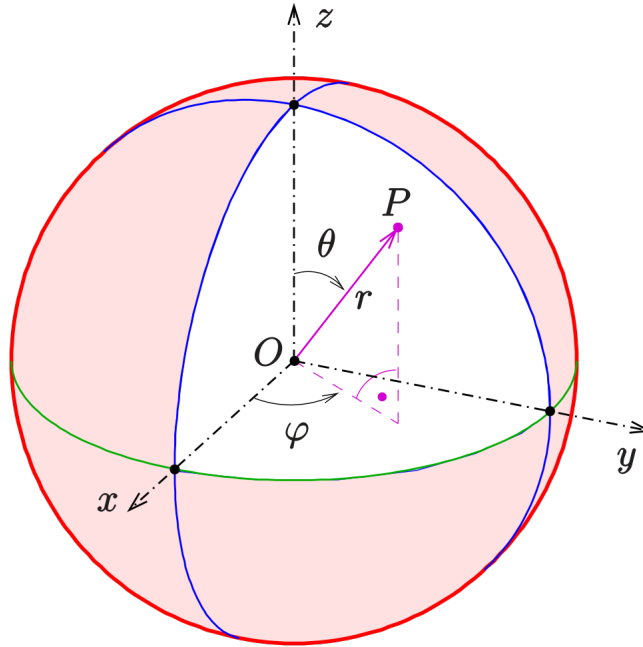


Figure 2.8: Spherical coordinate system used in this document [26].

This section is based on important antenna theory textbooks. Namely, *Antenna Theory: Analysis and Design* by Constantine A. Balanis [27], *Antenna Analysis* by Robert E. Collins [28] and *Antennas and Radiowave Propagation* by Edward A. Wolff [29]. All terms and definitions are based on the *IEEE Standard for Definitions of Terms for Antennas* [30].

2.3.1 Radiated Power Density, Radiated Power and Radiation Intensity

The instantaneous power, $\mathcal{P}$, passing through a closed surface, S , is given by Equation 2.1, where $\mathcal{W}$ is the instantaneous Poynting vector that results from the cross-product of the electric field,

$\mathcal{E}$, and the magnetic field, $\mathcal{H}$, i.e., $\mathcal{W} = \mathcal{E} \times \mathcal{H}$, ds is the element of oriented surface, da is the element of area and $\hat{\mathbf{n}}$ is the unit vector normal to the oriented surface.

$$\mathcal{P} = \oiint_S \mathcal{W} \cdot ds = \oiint_S \mathcal{W} \cdot \hat{\mathbf{n}} da \quad [\text{W}] \quad (2.1)$$

$\mathcal{W}$ is a power density. However, due to the variation of the $\mathcal{E}$ and $\mathcal{H}$ fields in time, it is useful to instead work with the average¹ power density shown in Equation 2.2. It is important to note that, in the far-field region, instantaneous power density is mostly dominated by the real part of the Poynting vector, i.e. the average power density. This is shown in [28, p. 24] and in [27, p. 36]. Therefore, the average power density, W_{av} , is most commonly referred to as simply power density, W_{rad} .

$$W_{\text{av}}(r, \theta, \phi) = W_{\text{rad}}(r, \theta, \phi) = \text{avg}(\mathcal{W}(r, \theta, \phi; t)) = \frac{1}{2} \Re\{\mathcal{E} \times \mathcal{H}^*\} [\text{W m}^{-2}] \quad (2.2)$$

Having W_{rad} , it is possible to calculate the average radiated power using Equation 2.3. Once again, in the far-field region the radiated power is mostly dominated by the real (average) radiated power. Hence, the average radiated power, P_{av} , is usually referred to as simply radiated power, P_{rad} .

$$P_{\text{av}} = P_{\text{rad}} = \oiint_S W_{\text{rad}} \cdot ds = \frac{1}{2} \oiint_S \Re\{\mathcal{E} \times \mathcal{H}^*\} \cdot ds \quad [\text{W}] \quad (2.3)$$

Radiation intensity is the power radiated per unit solid angle [27, p. 37]. It represents the power radiated in a certain direction and is given by Equation 2.4. Importantly, radiation intensity does not depend on the distance from the antenna, because of the inverse-square law. This is because, for a solid angle, the square decrease in power density with distance, r , is offset by its square increase with surface area.

$$U(\theta, \phi) = r^2 W_{\text{rad}}(r, \theta, \phi) \quad [\text{W sr}^{-1}] \quad (2.4)$$

2.3.2 Loss Resistance, Radiation Resistance and Efficiency

In a real antenna, not all the input power is converted into radiated power due to energy losses. Ohmic losses in the antenna's metallic conductors create loss resistance. Loss resistance also includes the losses between the reflector and feed horn in parabolic antennas.

The other source of losses we can consider is radiation resistance. Radiation resistance comes from the emission of electromagnetic waves. It is not a conventional resistance that dissipates energy as heat, but it is expressed in Ω as the value of ohmic resistance that would dissipate the same amount energy as heat, as is dissipated by the emission of electromagnetic waves [28, p. 25].

The acceleration and deceleration of oscillating electrons causes the emission electromagnetic waves. Because these waves carry momentum a recoil force will be exerted on the electron, to preserve the law of momentum conservation. This force is known as the Abraham–Lorentz force. It

¹In the equations presented throughout the document, $\text{avg}(A)$ represents the average of expression A .

opposes the force applied by the electric field, reducing the electron's momentum and, consequently, its velocity. This works as a resistance opposing the electric current on the antenna's conductors, which is called radiation resistance.

Radiation and loss resistances have an impact on input impedance, covered in Subsection 2.3.4. They also directly relate to the antenna's radiation efficiency, also known as conduction-dielectric efficiency, e_{cd} , which is the ratio of radiated power to input power, P_{in} . This is shown in Equation 2.5, where R_{loss} is the loss resistance and R_{rad} is the radiation resistance.

$$e_{cd} = \frac{P_{rad}}{P_{in}} = \frac{R_{rad}}{R_{rad} + R_{loss}} \quad (2.5)$$

There are several factors that affect an antenna's radiation efficiency. Most importantly, and in the scope of this dissertation, antenna size directly affects radiation efficiency. Antennas that are much smaller than the wavelength they operate at are inevitably inefficient due to having a small radiation resistance, while presenting large loss resistance caused by the small cross-section of conductors in miniature antennas.

Radiation efficiency does not account for impedance mismatches that generate reflection losses at the interface between the transmission line and the antenna. Reflection efficiency, e_r , accounts for these losses and is given by Equation 2.6, where Γ is the reflection coefficient of the impedance discontinuity in the interface.

$$e_r = 1 - |\Gamma|^2 \quad (2.6)$$

An antenna's total efficiency, e_{total} , is, therefore, given by Equation 2.7.

$$e_{total} = e_{cd}e_r \quad (2.7)$$

2.3.3 Gain, Realized Gain and Effective Area

Antenna gain is defined as the ratio between the radiation intensity in a certain direction and the radiation intensity that would exist if the input power were radiated isotropically [29, p. 12]. There are 4π sr in a sphere. Hence, if the input power were to be isotropically radiated, the power radiated in any given direction would be $\frac{P_{in}}{4\pi} \text{ W sr}^{-1}$. Antenna gain is, therefore, calculated as shown in Equation 2.8.

$$G(\theta, \phi) = \frac{U(\theta, \phi)}{\frac{P_{in}}{4\pi}} = \frac{4\pi U(\theta, \phi)}{P_{in}} \quad (2.8)$$

Gain, unlike directivity (covered in Subsection 2.3.6), is also related to antenna efficiency. As implied by Equation 2.5, the power radiated by an antenna is given by $P_{rad} = e_{cd}P_{in}$. Rewriting P_{in} as a function of P_{rad} results in Equation 2.9.

$$G(\theta, \phi) = \frac{4\pi U(\theta, \phi)}{P_{rad}} e_{cd} \quad (2.9)$$

Even though antenna gain is defined for a specific direction, unless otherwise specified, it is presumed to refer to the direction of maximal ² radiation intensity, as shown in Equation 2.10.

Gain is a unitless measure that can be expressed in dB. However, to be able to compare different antennas, it is more useful to compare the radiation intensity in a certain direction with the radiation intensity that would be produced by a reference antenna. If the radiation intensity is compared to that of the ideal isotropical radiator, which is the case for equations 2.8, 2.9 and 2.10, antenna gain is commonly expressed in dBi, as a way to identify the reference antenna. Any reference antenna can be used. The most common one, apart from the ideal isotropic radiator, is the half-wave dipole, implied by the use of dBd.

$$G = \frac{4\pi \times \max(U(\theta, \phi))}{P_{\text{in}}} e_{\text{cd}} \quad (2.10)$$

According to the *IEEE Standard for Definitions of Terms for Antennas* [30], "gain does not include losses arising from impedance mismatches (reflection losses) and polarization mismatches (losses)". Realized gain, G_{re} , takes into account impedance mismatch losses by considering the effects of the reflection efficiency, described in Subsection 2.3.2. Realized gain is, therefore, given by Equation 2.11.

$$G_{\text{re}} = G e_r = \frac{4\pi \times \max(U(\theta, \phi))}{P_{\text{in}}} e_{\text{total}} \quad (2.11)$$

Gain is related to the effective area through Equation 2.12. The effective area of an antenna represents the portion of energy from a passing electromagnetic wave that is collected by the antenna [27, p. 83]. Generally, it is calculated relative to the energy the isotropic radiator would have collected. Similarly to gain, effective area is, by default, expressed relative to the direction of maximal gain, yielding Equation 2.13.

$$A_{\text{eff}}(\theta, \phi) = \frac{\lambda^2}{4\pi} G(\theta, \phi) \quad [\text{m}^2] \quad (2.12)$$

$$A_{\text{eff}} = \frac{\lambda^2}{4\pi} G \quad [\text{m}^2] \quad (2.13)$$

2.3.4 Input impedance, Impedance Matching and Bandwidth

Input impedance, or feed point impedance, is the impedance seen from the feed point of the antenna and is given by Equation 2.14. It has an imaginary part, input reactance, X_{in} , and a real part, input resistance, R_{in} , which is the sum of the loss and radiation resistance.

$$Z_{\text{in}} = R_{\text{in}} + jX_{\text{in}} = (R_{\text{loss}} + R_{\text{rad}}) + jX_{\text{in}} \quad [\Omega] \quad (2.14)$$

²In the equations presented throughout the document, $\max(A)$ represents the maximum value that can be result from expression A.

Impedance matching is an important step in the tuning process of an antenna to avoid losses from reflections in the interfaces between the different components of a radio system, namely between the feeding transmission line and the antenna. It is important to note that, while antenna radiation efficiency is also a source of energy loss, it is completely different and independent of losses due to poor impedance matching. Losses from unmatched impedances are caused by reflected power, while losses from antenna radiation inefficiency are caused by ohmic and radiation resistance, as seen before. Even when all impedances in a radio system are perfectly matched and all the input power is transmitted to the antenna, energy will be lost due to the radiation inefficiency of an antenna.

Bandwidth is the frequency range over which the antenna is considered to be impedance matched to the feed line (generally, when the S_{11} parameter is below -10 dB), the gain is within expected values and the radiation pattern is not distorted. In other words, bandwidth is the range of frequencies over which the antenna works well [27, p. 65]. When operating outside the bandwidth it was designed to, an antenna can work differently than expected. For example, directional antennas might start to behave more omnidirectionally, with less gain and start to reflect power back to the transmitter due to poor impedance matching, with risk of damaging the device.

2.3.5 Polarization and Polarization Loss Factor

Polarization refers to the electric field's orientation in the electromagnetic waves that are transmitted by the antenna. It is defined for a given direction, however "when the direction is not stated, the polarization is taken to be the polarization in the direction of maximum gain" [27, p. 66]. The orientation of the electric field can be constant or change over time. Orienting an antenna made of linear conductors (linear antenna) vertically will result in vertical polarization, while orienting the same antenna horizontally will result in horizontal polarization. For non-linear antennas or for arrays of linear antennas that are not aligned, the orientation of the electric field changes as the wave travels through space. If the electric field vector movement in time describes an ellipse or circle, polarization is considered elliptical and circular, respectively.

Antenna polarization is very important, because when the receiving antenna's polarization matches the one of the transmitted wave there is optimum reception. Otherwise, especially for linear antennas that are orthogonally oriented, reception will be poor. For circularly polarized antennas, signals with either vertical or horizontal polarization can be received, at the cost of a 3 dB reduction in signal strength (and vice-versa).

The Polarization Loss Factor (PLF) represents the amount of energy lost due to the mismatch between the polarization vector of a receiving antenna, $\hat{\rho}_a$ and the polarization vector of an incident wave, $\hat{\rho}_w$ [27, p. 71]. It can also be calculated using the angle between those two vectors, ψ_p . The PLF is given by Equation 2.15.

$$PLF = |\hat{\rho}_w \cdot \hat{\rho}_a|^2 = |\cos(\psi_p)|^2 \quad (2.15)$$

2.3.6 Field Regions, Radiation Pattern and Directivity

The space that surrounds an antenna can be divided into three regions: the reactive near-field (also known as inductive near-field), the radiating near-field (also known as the Fresnel region) and the far-field (also known as the Fraunhofer region) [27, p. 31]. Near-field behaviours, such as near-field diffraction, dominate close to the antenna, whilst far-field behaviours, like the inverse-square law for power as a function of distance, dominate at greater distances.

The radiation pattern of an antenna shows, by definition, only the far-field. It is a plot of the antenna's gain as a function of direction [28, p. 25]. Radiation patterns can be 3D or 2D. 2D radiation patterns are essentially a section cut of the 3D version of the plot for different values of ϕ or θ . For linearly polarized antennas, it is important to consider two important cuts: the E-plane, aligned with the electric field vector and in the direction of maximum radiation intensity, and the H-plane, aligned with the magnetic field vector and in the direction of maximum radiation. Figure 2.9 shows an example of 3D and 2D plots of a Yagi-Uda's radiation pattern, which is a very common type of directional antenna.

Radiation patterns also serve as a way to visually evaluate the directivity of an antenna, $D(\theta, \phi)$, given by Equation 2.16. Directivity is, in essence, a measure of antenna gain without taking efficiency into account, i.e., the gain of the antenna if it were 100% efficient.

$$D(\theta, \phi) = \frac{4\pi U(\theta, \phi)}{P_{\text{rad}}} \quad (2.16)$$

Similarly to antenna gain, unless specified otherwise, directivity is presumed to be given by Equation 2.17.

$$D = \frac{4\pi \times \max(U(\theta, \phi))}{P_{\text{rad}}} \quad (2.17)$$

Directivity is also related to antenna gain through Equation 2.18.

$$D = e_{\text{cd}} G \quad (2.18)$$

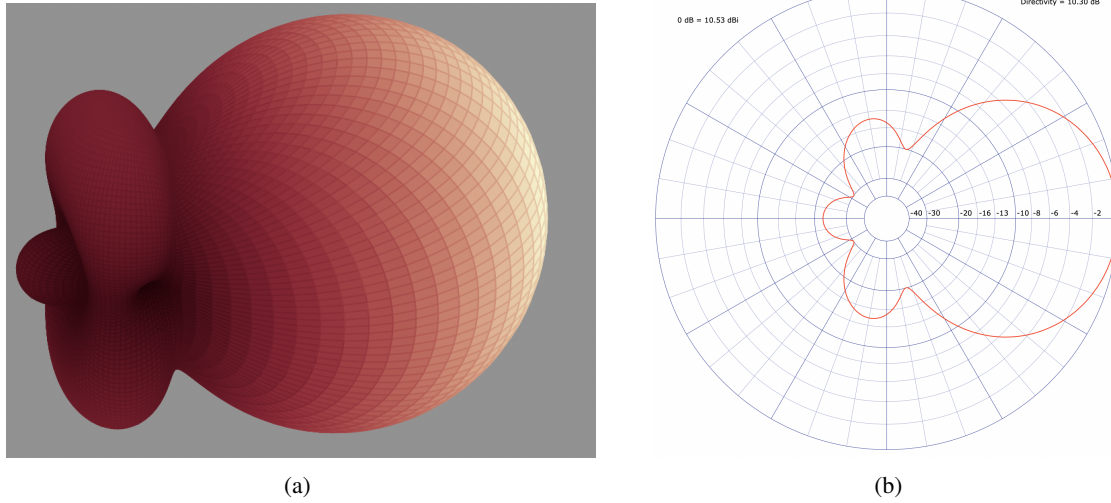


Figure 2.9: (a) 3D radiation pattern of a 6 element Yagi-Uda antenna at 14 MHz and (b) H-plane of the same antenna. The H-plane is represented by a 2D section cut for $\phi = 0$. Made using *cocoaNEC*.

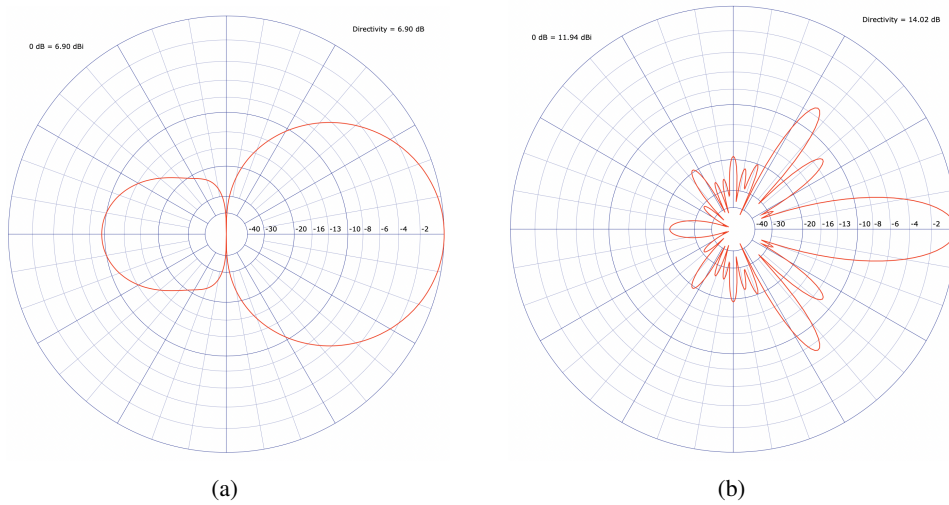


Figure 2.10: (a) A 2-element Yagi and (b) a Rhombic antenna's E-plane at 14 MHz, made using *cocoaNEC*.

A concept known as Half Power Beam Width (HPBW) is directly related to the visual evaluation of antenna directivity. HPBW represents the angular separation between the two points of the radiation pattern's main lobe that have a magnitude 3 dB smaller than that of the lobe peak [27, p. 40]. This main lobe is also called the beam of the antenna. The more directional an antenna is, the smaller the HPBW and the narrower the antenna's beam. Figure 2.10 shows a comparison between the E-plane of a 2-element Yagi and a Rhombic antenna. The directivity of the Rhombic antenna is much larger than that of the Yagi's. Therefore, its main lobe is much narrower, exemplifying the relation between directivity and beam width that was explained previously.

Antennas that have narrow beams in a specific direction are called directional antennas. Antennas that radiate evenly in a plane are known as omnidirectional antennas. There are several factors that affect antenna directivity. One important factor for this dissertation is antenna size, because strong directivity is hard to achieve when designing antennas that are considerably smaller than their operating wavelength.

Chapter 3

Literature Review

3.1 Antenna Miniaturization Techniques

For a long time, it has been known that reducing the size of an antenna directly reduces its Q factor, which is a measure of the bandwidth of the antenna relative to the centre frequency it operates in. Nevertheless, a new and more realistic calculation for the maximum efficiency of small antennas was recently proposed in [31]. Ideally, new designs should allow the efficiency of miniaturized antennas to be as close as possible to these proposed limits. In other words, the main purpose of antenna miniaturization techniques is to reduce the form factor of antennas, while still achieving reasonable bandwidth, matching properties, range and radiation characteristics.

The subsections that follow are based on a review of antenna miniaturization techniques published in the February 2018 edition of the *IEEE Antennas & Propagation Magazine* [32] and on a reference compilation of printed antenna designs, edited by Rod Waterhouse [33].

3.1.1 Topology-Based Techniques

Topology-based techniques work by modifying the antenna's geometry, current distribution and electrical dimension to achieve the desired radiation characteristics, while keeping the physical size of the antenna as small as possible. Some examples of designs that involve these miniaturization techniques include inverted-F antennas (covered in Subsection 3.2.3) and patch antennas (covered in Subsection 3.2.2).

3.1.1.1 Antennas Based on Space-Filling Curves

Antennas based on space-filling curves use a repeated set of geometric curves to fit the radiating element in a smaller space. These include fractal antennas, such as the Koch dipole, meander antennas (covered in Subsection 3.2.1) and many other designs based on previously discovered space-filling geometries.

3.1.1.2 Defected Ground Structures as a Reactive Loading Technique

Slowing wave propagation in an antenna can be a useful technique for size reduction. Frequency is an immutable characteristic of an electromagnetic wave, even when considering gravitational redshift and other relativist phenomena [34]. When a wave travels through different mediums, its speed will vary. Because the frequency of a wave is given by $f = \frac{v_{\text{medium}}}{\lambda_{\text{medium}}}$ and since it is immutable, the change in speed will be accompanied by a change in wavelength, so that the wave frequency is always the same.

This "principle of constant frequency" means that slowing wave propagation in an antenna will also decrease the guided wavelength. Since the optimal antenna length is directly related to wavelength, we can actually reduce the form factor of an antenna simply by slowing wave propagation. It is possible to slow wave propagation on an antenna using a great variety of techniques, one of the most common being ground engineering.

Creating Defected Ground Structures (DGSs), consists in modifying the conventional uniform ground plane of planar antennas to improve gain, reduce size or even to create multi-band or wideband resonance. Introducing ground plane discontinuities, comparable in size to the wavelength, disturbs the return path of currents. This creates additional inductance, capacitance (due to the displacement currents between the edges of the defect) and resistance (specifically, radiation resistance from the fields radiated from the discontinuity), effectively loading the antenna and making the antenna's electrical size larger than its physical form factor, helping to reduce antenna size.

DGSs originated from Photonic Band Gap (PBG) structures used in other fields as optical resonators that could be tailor-made to improve performance through the appropriate design of defects in crystal lattices [35]. If scaled appropriately, these discontinuities can work for a wide range of frequency bands, other than visible light [36]. In fact, they have been profusely used for microwave and millimeter-wave transmission lines and planar antennas, in order to suppress harmonics and achieve smaller sizes.

DGSs have been proven to drastically reduce the size of miniaturized antennas, as noted by several literature reviews such as [37] and [38]. Even so, ground engineering, particularly the use of DGSs, has considerable drawbacks. Designing microwave or millimeter-wave components using ground engineering poses challenges primarily due to the complexities involved in the modelling of defects and defected structures. There are numerous design parameters that significantly impact the resonating properties of DGSs. As a result, it becomes arduous to accurately find the ideal values for these parameters during the design process. Additionally, ground engineering only works for planar antennas, it can reduce directivity, due to the effect that DGSs have on front-to-back ratio and radiation from the defect might cause interference and electromagnetic compatibility issues.

3.1.1.3 Other Topology-Based Reactive Loading Techniques

DGSs are not the only technique that provides reactive loading of antennas. Reactive loading can be done by adding periodic impedance discontinuities along the antenna's radiating element and

ground plane as shown in Chapters 7 through 9 in [33]. Antennas can also be loaded using lumped elements, using shunt-capacitors, for instance. It can also be accomplished using distributed loading or other slow-wave techniques.

3.1.2 Material-Based Techniques

Material-based techniques aim to change the electromagnetic properties of an antenna in order to reduce the guided wavelength. These techniques make use of the phenomena described in Subsubsection 3.1.1.3 to slow wave propagation in the antenna. However, the decrease in wave speed is achieved by changing the materials of the antenna structure, instead of changing the antenna topologically.

3.1.2.1 Substrate Engineering

The speed of an electromagnetic wave in a medium is given by $v_{\text{medium}} = \frac{v_0}{n_{\text{medium}}}$ and, similarly, its wavelength is given by $\lambda_{\text{medium}} = \frac{\lambda_0}{n_{\text{medium}}}$, where v_0 and λ_0 are, respectively, the speed and wavelength of light in free-space and n_{medium} is the refractive index of the medium. We can slow wave propagation in an antenna by increasing the permittivity of the substrate, because the refractive index is given by $n_{\text{medium}} = \sqrt{\epsilon_r \mu_r}$, where μ_r is the relative magnetic permeability and ϵ_r is the relative electric permittivity of the substrate (also known as dielectric constant).

The main challenges associated with using engineered substrates are that materials with high permittivity are usually more expensive than the conventional FR4 epoxy and higher permittivities in a substrate can reduce bandwidth and difficult impedance matching. Additionally, these techniques are only suitable for microstrip antennas. Nevertheless, these limitations can be overcome to some degree. For example, engineering a substrate with a non-uniform permittivity can help with impedance matching. Perforating the substrate in the regions that are not beneath the metallic patch of an antenna can help reduce the effective permittivity of the substrate on the edges, helping with impedance matching. It is also important to note that, while using high permittivity materials for substrates will reduce radiation efficiency, it can also be beneficial when trying to match antenna impedance to materials with equally high permittivity (for instance, when impedance matching antennas with the human body, in biomedical applications).

3.2 Common Miniaturized Antenna Designs

3.2.1 Meander Antennas

Meander antennas make use of carefully designed bends of a large straight radiating element to fit it into a smaller space. Meander lines can take several shapes, from square to spiral-like or even zigzag lines. These antennas are shorter not just due to their curves, but also because meander lines capacitively load the radiating element, making it electrically longer than its physical size.

However, bending the radiating element also comes at a cost, which is antenna gain. There is a reduction in gain, because in most meander designs, currents on several arms of the meander

shape are 180° out of phase, cancelling each other's radiation on the far-field. Figure 3.1a shows a 12-segment square meander dipole antenna tuned for 5 GHz. This antenna would be 3 cm in length if it was a straight radiator (Figure 3.1b). The meander version of this radiator fits in a 1 cm space which is 3 times smaller than the straight version of the antenna. However, because of the out of phase arms (which can be identified using Figure's 3.1a colour scheme) the antenna has a significantly smaller maximum gain when compared to its straight counterpart. A quick *cocoaNEC* simulation shows that the maximum gain of the straight dipole is 2.25 dBi, whereas the meander dipole's maximum gain is 1.53 dBi (in both cases, assuming perfect conductors and free-space propagation). Figure 3.1c shows the radiation pattern of both antennas, where the penalty in gain is clearly noticeable.

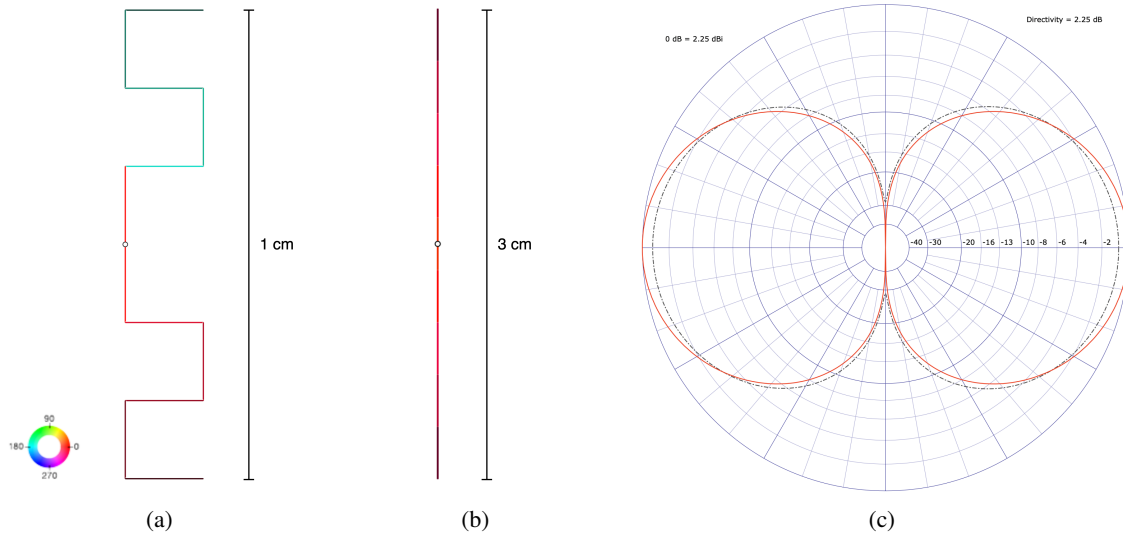


Figure 3.1: (a) Geometry and current phase of the meander dipole. (b) Geometry of the straight dipole. (c) Radiation pattern for the E-plane of the meander dipole (grey) and of the straight dipole (red).

3.2.2 Patch Antennas

Patch antennas are a type of antenna with a low profile, commonly used in portable devices and known because of their simple fabrication process. Patch antennas are also the original type of microstrip antenna, invented and described by John Q. Howell at the 1972's *Antennas and Propagation Society International Symposium*. Microstrip patch antennas consist of any geometrical patch of metal mounted over a larger ground plane, forming a resonant microstrip transmission line that radiates mainly due to the fringing fields along the edges.

The resonant frequency of a patch antenna is related to the patch dimensions, as it is given by: $f_r = \frac{v_0}{2\sqrt{\epsilon_{\text{eff}}(L+2\Delta L_{\text{eff}})}}$, where ϵ_{eff} is the effective permittivity (which is related to the width of the patch and the substrate height), v_0 is the free-space speed of light, L is the length of the patch and ΔL_{eff} is the difference between the physical and electrical length of the patch [39].

The input impedance of a patch antenna is directly related to the feed point of the antenna. The antenna can be directly fed at its 50Ω point, using an inset microstrip feed line (Figure 3.2a) or a coaxial coplanar feed probe. Alternatively, the antenna can be fed from one of the patch's edges, using a microstrip $\frac{\lambda}{4}$ line, as an impedance adaptor, at the cost of reduced bandwidth (Figure 3.2b). More complex methods, such as proximity and aperture coupling, can be used as well.

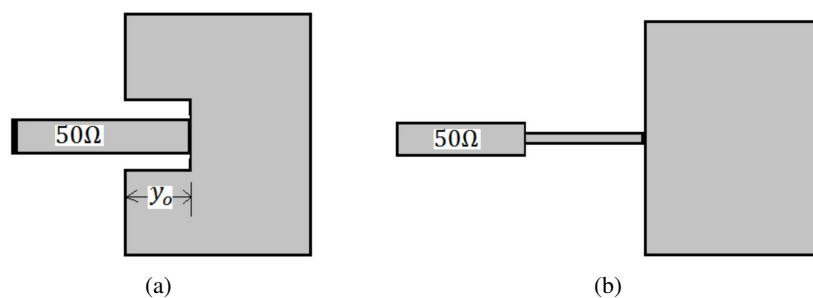


Figure 3.2: Examples patch antennas with (a) inset feed and (b) microstrip adaptor feed [39].

3.2.3 Inverted-F Antennas

Inverted-F antennas are a miniaturized variation of the monopole antenna and an evolution of the inverted-L antenna. IFAs consist of a radiating element that runs parallel to a ground plane and is grounded at one end.

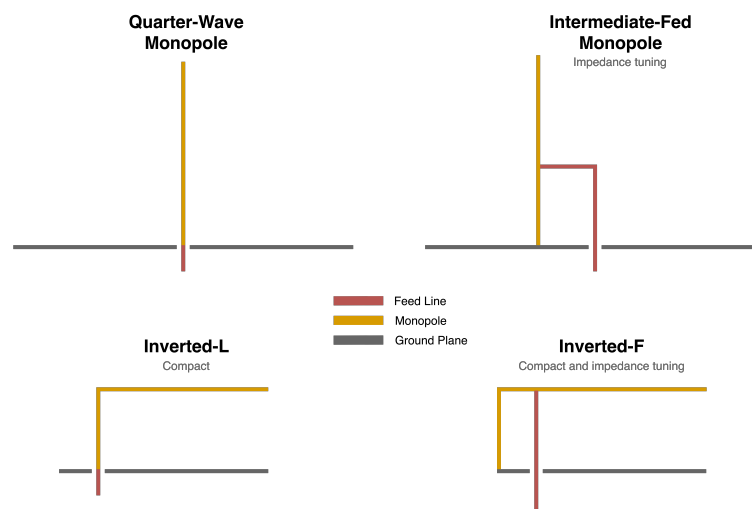


Figure 3.3: Evolution of the quarter-wave monopole, invented in 1895 by Guglielmo Marconi, until becoming the modern inverted-F antenna, first proposed in 1958 in [40].

Quarter-Wave monopoles achieve approximately double the gain of half-wave dipoles (with just half the size) but present very low radiation resistance (36.5 ohms compared to the 73.1 ohms of the dipole). Solving this problem was possible with the intermediate-fed monopole shown in Figure 3.3. The benefit of this antenna is that the input impedance relies on the distance between the feed point and the grounded end. This is because the segment of the antenna between the feed

point and the ground plane acts as a short-circuit stub. Consequently, by adjusting the placement of the feed point along the radiating element, the designer can achieve impedance matching between the antenna and the feed line.

The inverted-L antenna, also shown Figure 3.3, is a miniaturized variant of the quarter-wave monopole that is shorter and more compact. It achieves this size reduction, because the bend in the radiating element essentially creates a capacitance between it and the ground plane, capacitively loading the antenna and reducing its size due to the phenomena explained in Subsubsection 3.1.1.3. However, this antenna type does share the same problem of having low input impedance (even lower than that of the monopole).

IFAs allow for input impedance tuning while still being shorter and more compact than the quarter-wave monopole, presenting the benefits of both the inverted-L antenna and the intermediate-fed monopole. IFAs got their name because they are similar in shape to the letter F. The top horizontal line of the F is grounded. The other horizontal line is the feed line of the antenna. The length of the vertical line of the F, mainly affects the resonant frequency. The size of the ground plane affects the radiation pattern as well as input impedance. Lastly, the position of the feed point mainly relates to input impedance, as explained before. The relation between the geometry of an IFA and its input impedance, resonant frequency and radiation pattern is shown in Figure 3.4.

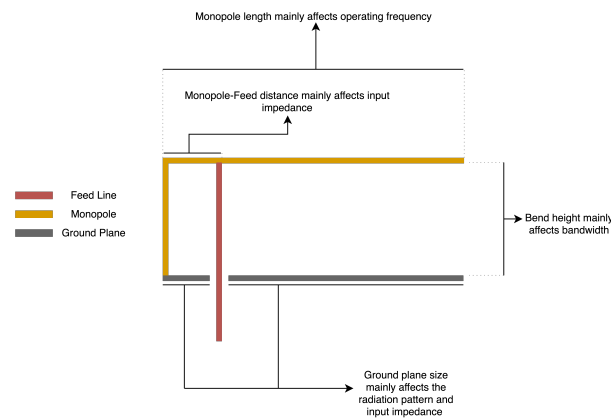


Figure 3.4: How the topology of an IFA affects its fundamental parameters.

Planar implementations of IFAs (Figure 3.5) are called planar IFAs, which are a variation of the patch antenna that is known as shorted patch antenna. They are extremely relevant to modern RF electronics, since they can easily be implemented in PCBs by using vias as feeds for the radiating element and as shorting pins at one of its ends. Planar IFAs, though suitable for PCBs, do not integrate easily with other electronic components. This is due to the fact that disturbing the wide radiating element and the ground plane of these antennas with cuts for traces, pads and vias should be avoided or kept to a minimum, severely restricting the designer's routing choices on both sides of a 2-layer PCB. For this reason, planar inverted-F antennas often necessitate a separate board fixed to the main board to suspend the antenna and provide an air dielectric or a more suitable material for optimal RF performance. Nevertheless, one advantage of planar IFAs is that their dimensions are easy to calculate. The resonating frequency of this kind of antenna is given by

$f_r = \frac{c}{4(L+W-W_s)}$ [33, p. 199], where L , W and W_s are the antenna length, antenna width and short width, respectively.

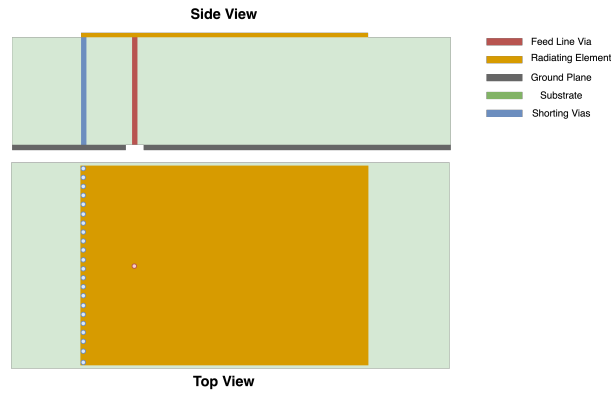


Figure 3.5: Top and side views of a planar IFA.

Printed IFAs, or PIFAs¹, offer a design that can be more easily integrated in the main board together with the rest of the electronics. To achieve this, the ground plane is removed from underneath the radiating element and placed on the same plane below it as shown in Figure 3.6. As a result, the radiating element will be thinner and only one side of the board is covered by the antenna, allowing for a simpler integration of the antenna in the same board as the rest of the circuitry. This implementation also means PIFAs have a radiating element that is shorter than $\frac{\lambda}{4}$, due to the capacitive loading caused by the increased radiator-ground capacitance when compared to the quarter-wave monopole.

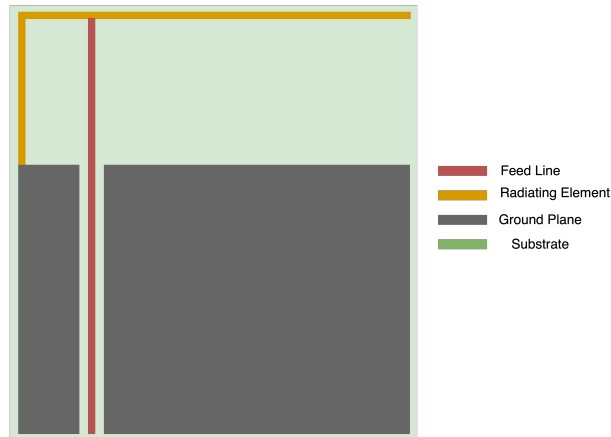


Figure 3.6: Generic PIFA.

To save space, PIFAs can be combined with meander antennas to form a hybrid antenna, called Meandered PIFAs (MPIFAs), that are shorter than a normal PIFA, but have less gain (as explained in Subsection 3.2.1). An example of this design can be found in Figure 3.7.

¹There is little consensus among authors on the exact meaning of "PIFA". For clarification and for the purposes of this document, "PIFA" refers to the printed implementations of the inverted-F antenna and "planar IFA" refers to the planar implementations.



Figure 3.7: 2.4 GHz meandered PIFA (top part of the image) used by an ESP8266 module made by Espressif Systems.

To achieve multi-band planar IFAs, spur lines, slots or strips can be added to the radiating element. PIN diode configurations can be also be applied, creating what is known as switched-band planar IFAs. Additionally, reduced-size planar and printed inverted-F antennas can also be achieved, since practically all the miniaturization technique mentioned on the previous section are suitable for this kind of antenna.

3.3 Miniaturization of LoRa Antennas

LoRa has unique power and bandwidth requirements, as noted by Ferrero and Toure:

Requirements for IoT applications are usually completely different from classical user needs. Dedicated communication technologies have been recently proposed to provide long-range, robust and low-power communications known as LPWAN. Most LPWAN standards as LoRa and Sigfox are using the ISM band at 868 MHz [41, p. 243].

While it is possible to use generic small antennas for the required frequency bands, LoRa devices can benefit from antennas that are optimized for their specific characteristics. The small bandwidth of LoRa systems facilitates the use of techniques that reduce antenna bandwidth in exchange for a reduction in size, which may not be viable for other technologies. In addition, LoRa antennas have specific requirements for efficiency and gain, as they are used in low-power, long-range IoT systems. These parameters may not be as critical in other use-cases, but they are crucial for ensuring the effectiveness of LoRa antennas. Consequently, when designing a compact and low-power end-node, miniaturization techniques should focus on a great reduction in size at the cost of reduced bandwidth and possibly some radiations pattern distortion. Efficiency and gain should be preserved as much as possible to maintain good range and power consumption characteristics.

As mentioned in Section 1.3, research on miniature LoRa antennas is limited. [42] represents one of the most recent reviews about design challenges for IoT communication technologies, such as Narrow-Band IoT (NB-IoT), Wi-Fi and LoRa. This review analyses the findings of several studies on the advantages and disadvantages of antenna design types, performance enhancement techniques and the designs proposed on several research works. It also performs a Strengths,

Weaknesses, Opportunities and Threats (SWOT) analysis on LoRa and NB-IoT technologies. This section covers the most relevant LoRa antenna designs mentioned in [42] and also describes various other antenna designs that are relevant to this dissertation, but not mentioned on the review. A summary of the research work presented in this section can be found in Table 3.1, at the end of this chapter.

In [8], two miniature antennas were designed specifically for LoRa with the goal of evaluating the viability of making metal logos a part of the device's antenna. The results show a robust radiation pattern with little distortion. Nevertheless, 0.8 dBi was the maximum gain that was obtained among all the design variations included in the study. Some design variants presented gains as low as -1.6 dBi which, even considering how forgiving LoRa's typical link budgets are, still falls short of what is required for some smart agriculture projects in remote locations and very dense urban or forest areas. In [41], a similar antenna (Figure 3.8) was used in real-world field tests in an urban area. Nevertheless, no tests were performed with a distance greater than 500 m, at which the Signal to Noise Ratio (SNR) was -12 dB. In the best case scenario, LoRa systems can demodulate signals that are 20 dB below the noise floor. It is interesting to note the resilience of LoRa technologies to the point of allowing for logo designs to be implemented directly as a part of the antenna, however, it would be useful to test longer range use-cases of miniaturized antennas in order to understand the maximum achievable distance of a small antenna that was designed with a focus on improving range rather than facilitating logo design in end-devices.

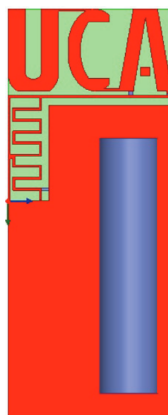


Figure 3.8: Miniature antenna used in [41], where the logo is part of the antenna itself .

In [43], a small PIFA is developed for wearable applications. The maximum gain of this antenna was 1.25 dBi. The antenna was made to work on both the EU863-867 and the EU433 bands. It presented a respectable radiation pattern, being just slightly distorted at 868 MHz. The main downside of this design was its size, with a length of almost 17 cm and an area of around 150 cm^2 . Fortunately, for PIFAs it is relatively easy to incorporate the device electronics into the ground region of the antenna, which means that for the entire end-node could be implemented without it being much larger than the antenna itself. Still, in this dissertation it would be important to test the effect of DGSs (Subsubsection 3.1.1.2) on PIFA antennas. The proposed design does use a slotted defect to achieve dual resonance. Even so, with around 90 MHz of bandwidth, there

is a considerable reduction in size at the cost of even more bandwidth that could be achieved by implementing more significant DGSs, while still preserving enough gain and bandwidth for most LoRa systems.

Reference [44] presents a wideband and compact antenna, designed to work in the most common LoRa bands. This design implemented a double-leaf-shaped patch radiator with a slotted DGS (Figure 3.9b), which took considerably smaller space than previous research work presented on the document. With an area of just 7.48 cm^2 , it achieved an efficiency of 97%, which is rather impressive for an antenna significantly smaller than the wavelength. Nevertheless, no real-world testing was done. The gain of the antenna (2.56 dB) was said to be calculated "by taking the ratio of power in a particular direction to the power that could be transmitted by a perfect ideal antenna under the same conditions" [44, p. 2]. In my opinion, from this statement, it is not entirely clear what is the reference antenna for these measurements. As a result, it is difficult to compare [44] to the rest of the literature. It would be valuable to replicate this design and to research the effects of slotted DGSs in more compact designs like PIFAs.

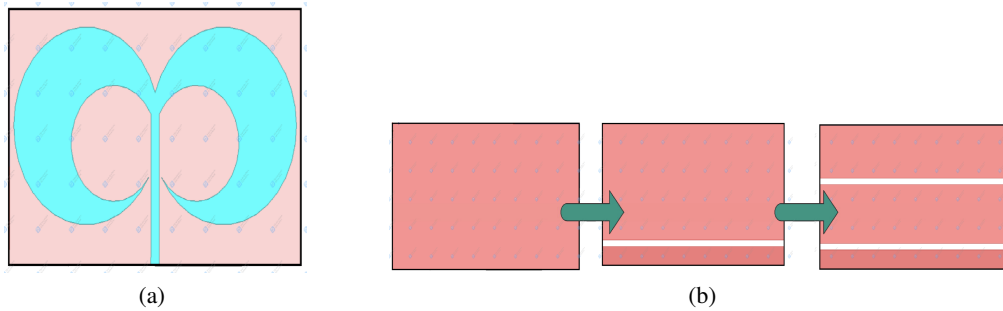


Figure 3.9: (a) Top and (b) bottom designs of the leaf-shaped patch antenna mentioned in [44].

Reference [45] is a design note describing a MPIFA that is not specifically designed for LoRa, but resonant in the same frequency bands. The maximum gain of the antenna is -0.12 dB relative to the input power of 10 dBm . The device is compact and the semi-omnidirectional radiation pattern presents little distortion. However, to achieve the required dimensions a non-standard FR4 substrate thickness is used. In Chapter 4, a simulation that replicates this design is described. Through that simulation, it is concluded that the thickness of the substrate is quite relevant to achieve the dimensions proposed on the design note. This is relevant, since non-standard FR4 substrates may come as obstacles for commercial applications depending on the added costs of using such substrates. This design also takes advantage of the simple impedance matching characteristics of PIFAs to make it possible to add lumped elements at the feeding point, allowing for compensation of detuning caused by plastic encapsulations.

Another design note, [46], describes a PCB helix antenna for the EU863-857 and AU915 bands. This is a very common antenna design and researching viable PCB implementations of such a popular antenna is important. This implementation is particularly relevant for compact end-nodes that need to have a very flat profile, which is a common requirement for use-cases in the logistics and vehicle tracking industries. Even so, the input impedance of the antenna is not

matched to $50\ \Omega$, having an input impedance of $Z_{in} = 10 - j88\ \Omega$. [46] refers to a better option, [47], when more space is available. This design note describes a monopole antenna that is closer to $50\ \Omega$ with $Z_{in} = 30 + j11\ \Omega$. Both of these antennas need external matching components to achieve better efficiency, critical for low-power IoT systems. These two designs, as well as the previously mentioned PIFA, are shown in Figure 3.10.

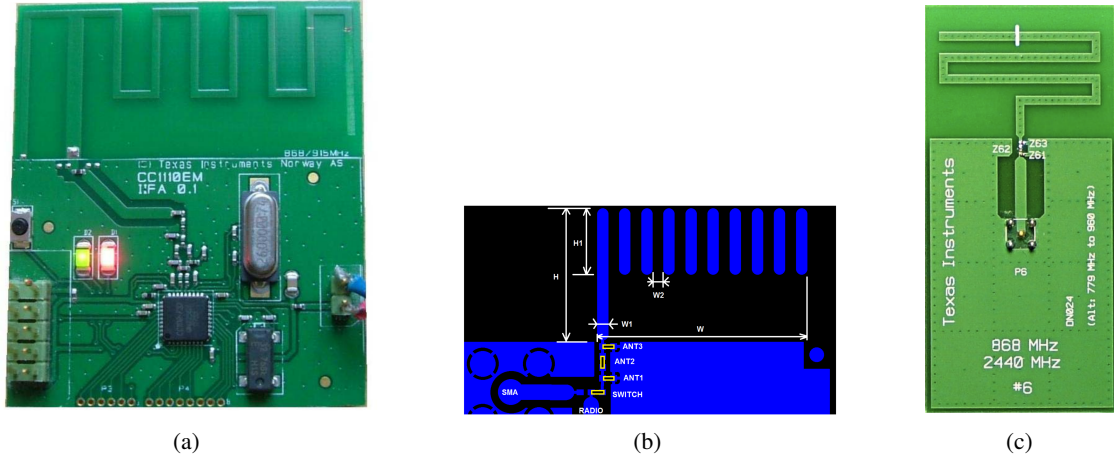


Figure 3.10: (a) MPIFA, (b) helical and (c) monopole antennas proposed in design notes [45], [46] and [47], respectively.

Reference [48] describes the development of UWB-inspired disk-shaped monopole antennas, using a cardboard substrate. It was tested in a real-world urban environment with a distance of up to 1.2 km. It was also found that the height of the antennas is more crucial to the LoRa radio link than the distance between the gateway and end-node. The results obtained during this research work are relevant, because they show that it is possible to design highly performant LoRa antennas without using expensive material-based techniques.

3.4 Final Remarks

The papers, reviews, articles and design notes mentioned during this chapter highlight the importance of antenna designs made specifically for LoRa applications. They show that it is essential to establish the required features of a LoRa antennas beforehand, since it is challenging to design generic LoRa antennas that work for every use-case. Some studies, such as [8] and [41], achieve very compact designs, making them great antennas for the logistics and tracking industries, where end-nodes need to fit inside packaging and other tight spaces. Nonetheless, the obtained gains might not be suitable for some applications, specially in longer range ones such as smart agriculture. Other works, namely [43], manage to obtain impressive gains for omnidirectional miniature antennas, but are still too large. It would be interesting to study the impacts of some techniques as a complement to the ones implemented in these designs, particularly testing antennas that use DGSs to obtain considerable size reduction. One common factor to almost all the presented studies is that very few

mention real-world long-range tests. LoRa technologies differentiate themselves from others in the IoT market due to their long-range capabilities. Yet, the farthest distance considered in these studies was 500 m and 1.2 km for [41] and [48], respectively.

This dissertation aims to develop and test new designs as well as enhancements of previously proposed miniature LoRa antennas, focusing on the commercial viability of such antennas and ensuring that there is a decent balance between range, size and efficiency. The work involves the design and testing of PIFAs with DGSs, meandered PIFAs and several other hybrid designs. It focuses on planar antennas made on FR4 and other inexpensive substrates, similarly to some works presented in this chapter. Material-based techniques are usually less viable for low-cost applications and were rarely used in the research works that were covered both in this document and in [42]. Therefore, such techniques are out of the scope of this dissertation. This work focuses on achieving the size reduction that is usually wanted when using miniature antennas, but aims at developing a balanced antenna that can still preserve some gain and efficiency allowing for a compact device and low-power, long-range applications as well. Additionally, the designs with the best results are meant to be integrated in a simple multi-sensor LoRaWAN end-node. This allows for the analysis of the challenges that come with incorporating miniature LoRa antennas in PCB end-devices. It also allows for real-world tests that ought to be more realistic and extensive than the ones conducted in many of the works presented in this chapter, such as in [41], by testing longer range use-cases in urban and rural situations.

This dissertation describes the development of a commercially viable device that fits into the category of compact LoRaWAN end-nodes due to the use of a miniature antenna, but that also preserves good range and efficiency so that it can be used in a multitude of use-cases. Material-based techniques and other expensive solutions were avoided as much as possible. This work does not try to develop a wideband antenna nor a device that can operate on several bands. It focuses on creating a narrowband, low-bandwidth, efficient and compact end-node for the EU863-867 band.

Ref.	Max. Gain	Max. Eff.	Features
[41]	0.8 dBi	74%	+ Very small design + Real-world test + PCB antennas can perform better than electrically short monopoles - Not tested further than 500 m
[43]	1.25 dBi	84%	+ Good efficiency + Good gain + Uses slot defects to achieve dual resonance - Large size - Could explore the use of other DGSs to achieve a smaller size - No real-world tests - Use-case specific (wearables)
[44]	2.56 dB (unclear ref.)	97%	+ Very good efficiency + Very small size, achieved using DGSs - Unclear reference antenna for gain measurements - No real-world testing
[45]	-0.12 dB (relative to 10dBm of input power)	N/A	+ Compact device + Tested on real hardware - Uses non-standard substrate thickness
[46]	2.33 dBi	65%	+ Flat profile and small size (helix) + Good gain + Good gain/size ratio - Low efficiency - Needs impedance matching with external components
[47]	5.05 dBi	97.67%	+ Very good gain + Very good efficiency - Does not show radiation pattern - Large size - Needs impedance matching with external components
[48]	-10 dBi	N/A	+ Real-world tests up to 1.2 km + Presents a performant and inexpensive solution + The main LoS link factor for LoRa is height - Distorted radiation pattern - Small gain

Table 3.1: Feature summary of the mentioned research works and design notes.

Chapter 4

Antenna Development

4.1 Antenna Type Selection

At the outset of the project, it was assumed that the development of designs based on multiple antenna types would be possible. However, during the research phase, where different kinds of antennas were modelled and investigated, it became clear that each design had its own peculiarities, needing different strategies to tune, impedance match and miniaturize. Besides, for each design, it would be necessary to investigate how to fit the antenna with the rest of the device's electronics. Consequently, multiple rounds of prototypes would be needed. As a result, this approach would have allocated a large amount of time just to develop the antenna and would not allow enough time to develop a complete LoRaWAN end node. Therefore, it was decided that the project would focus on trying to improve several aspects of one type of antenna, after an educated pre-selection. The selection process ought to be based on knowledge that came from early simulations of different antennas and from the making of the previous literature review chapter.

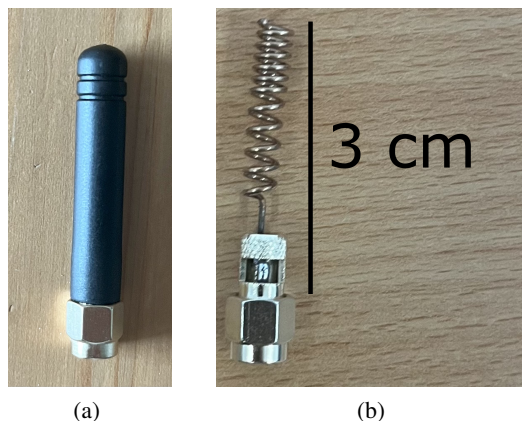


Figure 4.1: Typical LoRa rubber ducky antenna (a) with and (b) without plastic cover.

According to feedback from Wavecom, and from a reverse-engineering analysis of existing products handed over by the company, it became apparent that the single most used antenna

for LoRaWAN end nodes in today's market is the rubber ducky antenna. This is a very common type of normal-mode helical whip antenna (Figure 4.1). Whip antennas are a variation of the quarter-wave monopole that does not have a well-defined ground plane and uses nearby surfaces as a rudimentary ground plane. Helical antennas are a miniature version of the quarter-wave monopole, consisting of one or more conducting wires wound in the form of a helix [27, p. 549]. The rubber ducky antenna is a hybrid implementation of both the helical and whip designs, making it easy and inexpensive to fabricate and develop. Nonetheless, it presents the following drawbacks:

- Due to not having an effective ground plane, performance is somewhat dependent on its surroundings and positioning;
- Best antenna placement is perpendicular to the circuit board, which should add at least 3 cm to the total device thickness;
- Due to the use of a helical conductor, input impedance is around $25\ \Omega$ to $35\ \Omega$, increasing return losses for typical $50\ \Omega$ systems;
- Input impedance can change with position relative to the circuit board;
- These antennas usually present low gain and efficiency;
- Its radiation characteristics are highly dependent on geometry;
- Axial ratios for these antennas are relatively low and field polarization is more elliptical than linear, even in normal-mode operation [27, p. 253];
- Normal-mode helical whip antennas are mostly used for short-range hand-held two-way radios, which directly contradicts most of LoRa's long-range use-cases.

Considering its drawbacks and the device thickness increase that rubber ducky antennas cause, it was decided that the antenna developed for this dissertation should differentiate itself from current mainstream antennas by focusing on a planar design that is both compact and thin.

Planar designs do lead to much thinner devices. However, if integration of the antenna directly on the end node's board is not possible, the total device area becomes very large, and the end node becomes commercially uninteresting, regardless of how thin it might be.

The integration of electronic components within the same board as patch and patch-based antennas, such as the planar IFA, poses challenges. Typically, these antenna designs are implemented on substrates with high electrical permittivity or high magnetic permeability. By utilizing such substrates, antennas can be made significantly smaller. Consequently, these antennas are usually placed outside the main board that accommodates the remaining electronics. However, this approach encounters a drawback when considering the EU863-870 band. In order to operate within this frequency range, either prohibitively expensive or excessively large substrates would be required. Furthermore, it is important to acknowledge that these types of antennas necessitate undisturbed radiating elements without any electronics or traces overlapping them. As a result,

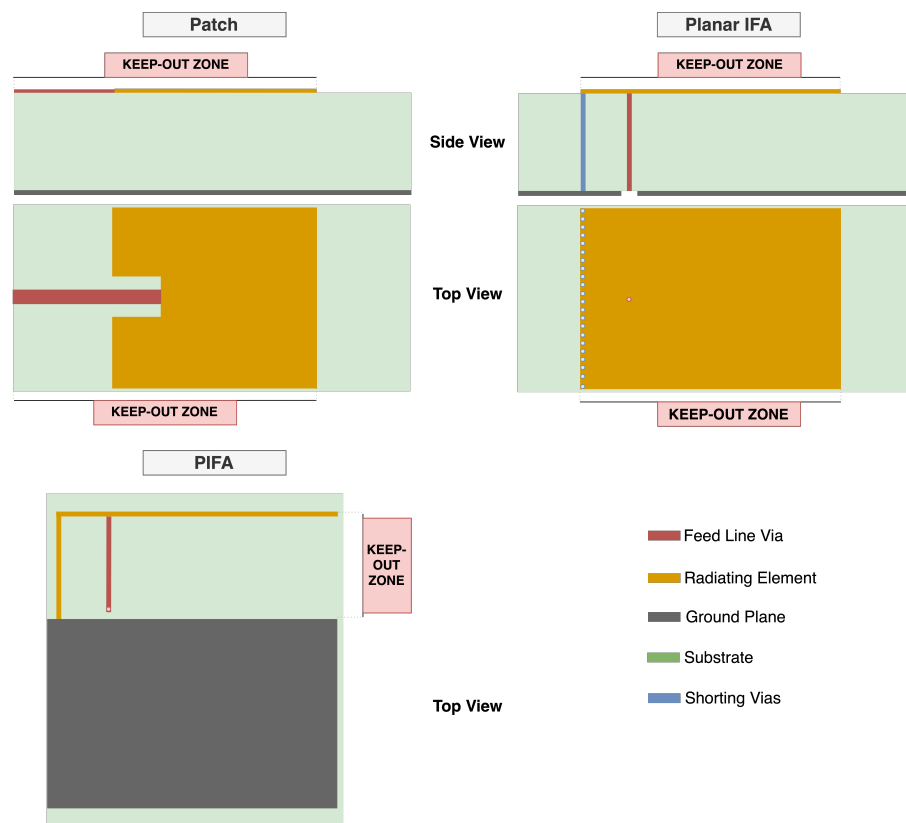


Figure 4.2: Keep-out zones for different planar antenna designs.

large areas, referred to as keep-out zones, are established where electronic components cannot be placed.

The dimensions of keep-out zones for a planar IFA and patch antenna operating at a frequency of 868 MHz were estimated using the design equations mentioned in Subsections 3.2.2 and 3.2.3, and the results are presented in Table 4.1. The keep-out zones for these antennas, as well as for the smallest bottom-fed PIFA described later in this chapter, are depicted in Figure 4.2. It is evident that these keep-out zones impose significant limitations on component layout, particularly considering the limited usability of ground planes beneath these zones and the unviability of through-hole vias in these board regions.

Antenna	Approx. Keep-Out Zone (mm ²)
Patch	8630
Planar IFA	1860
Bottom-Fed PIFA	1106

Table 4.1: Keep-out Zones for a 868 MHz planar IFA, patch antenna and for the smallest version of the Bottom-Fed PIFA presented in Subsection 4.3.8.

From the facts presented in this section it was concluded PIFA designs would be the most

interesting to explore. PIFA's ground planes should be able to easily accommodate the electronic components of the device, if correctly dimensioned. Additionally, PIFA's radiating elements are thinner, making keep-out zones smaller, which should lead to a more compact device. The next sections illustrate this advantages in more detail.

4.2 Design Workflow

Designing a narrowband miniature LoRa antenna is not a completely straightforward process. This section describes the design workflow that was used to create and enhance the end node's antenna.

To develop the antenna, 3 types of simulation models were used: geometry-oriented, feed-oriented and realistic. Each of these models represents a different design phase. The need to use 3 different types of model arises from the fact that not only the available computational resources were limited, but also that some antenna design processes are extremely resource-hungry, taking a lot of time to complete, regardless of hardware limitations. Extremely detailed simulations yield precise and realistic results. Yet, it can take several days to run such simulations on the mid-level computer that was used. Moreover, hundreds of simulations are required during the initial design phases, rendering super realistic models unsuitable for such stages, even when using high-end computers. Therefore, in some occasions, such as for optimizations, it is best to use simple models that can be simulated faster, whilst for validation purposes, in more advanced design iterations, there are benefits to using detailed and computationally heavy simulation models.

Figure 4.3 shows an example of a geometry-oriented model. These models represent the basic topology of the antenna, without any detailed features that might increase simulation time. In order to make such models light and easy to simulate a few approximations ought to be applied. Namely:

- Densely via stitched regions of the PCB are replaced with copper blocks;
- Isolated vias are replaced with solid cylinders (essentially, vias without holes);
- A faster, iterative electromagnetic solver is used;
- The electromagnetic field simulation and other simulation parameters are restricted to a narrow band of relevant frequencies;
- A reduced number of frequency simulation points is used. Ideally, the minimum number of points for the electromagnetic solver to converge;
- Ideal 50 Ω lumped ports are used to excite the antenna.

The detailed description of the first design stage can be found in Section 4.3. This phase had two main objectives: finding the antenna dimensions that yield the desired fundamental parameters (such as bandwidth, return loss, radiation efficiency and gain); and understanding the effects on the antenna of different topologies and miniaturization techniques. The former being covered in Subsection 4.3.1 and the latter in remaining subsections.

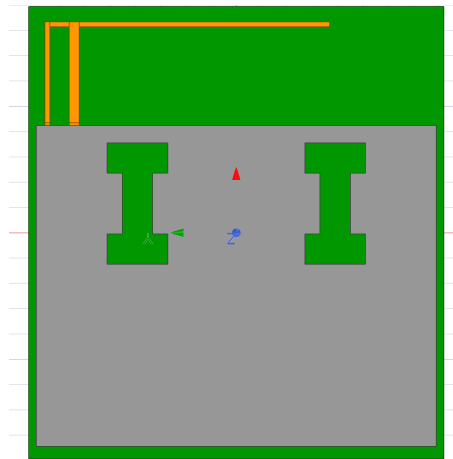


Figure 4.3: Example of a geometry-oriented model.

After the main geometry optimizations of Subsection 4.3.1, it was possible to achieve satisfactory values of return loss and bandwidth close enough to the desired frequency (868 MHz). A quick process of manual tuning was then needed to achieve the exact target operating frequency resulting in a geometry that could be exported to the PCB design software (Fusion Electronics¹), where the first version of the antenna's PCB was designed, using real vias and via stitching (instead of the previously mentioned approximations). These features are added in Fusion Electronics in order keep the geometry-oriented model lightweight, as explained before, but also because its PCB design toolset is much more suitable for PCB design than HFSS's, making the implementation of features such as vias much simpler with this software. Figure 4.5a synthesizes the first design phase, described in this paragraph, in a simple flowchart.

The second design phase is described in Figure 4.5b. The goal of this phase is to compensate for the use of an unrealistic feed in the previous one. For this purpose, 3D models of the real feeds (be it an SMA connector or a LoRa modem chip) were imported to HFSS and materials were carefully assigned to each part of the models. This feed-oriented models take much longer to simulate than the previous geometry-oriented one. This means that optimizations take much longer as well and that tuning is primarily done manually. The changes that the feed imposes on the design are directly applied to the PCB layout in Fusion Electronics. This allows for a final simulation model made with the files exported from Fusion Electronics. The result is a realistic model that exactly matches the final PCB, with realistic vias, via stitching, solder mask and no approximations. These models, shown in Figure 4.4, are extremely slow to simulate on the available resources, taking around 20 hours to run the simulation. They were used solely for validation purposes and small changes as fully optimizing and tuning realistic models is not practically feasible. Solder mask thickness and manufacturing tolerances are aspects that are challenging to realistically account for during simulations, especially when considering the low-cost manufacturing services that this dissertation

¹Autodesk Fusion 360 is a Computer-Aided Design (CAD), Computer-Aided Manufacturing (CAM) and Electronics Design Automation (EDA) software. Its EDA suite is called Autodesk Fusion 360 Electronics or simply Fusion Electronics. Because this was the most used suite of the program, and to simplify reading experience, Autodesk Fusion 360 is referred to as just Fusion Electronics.

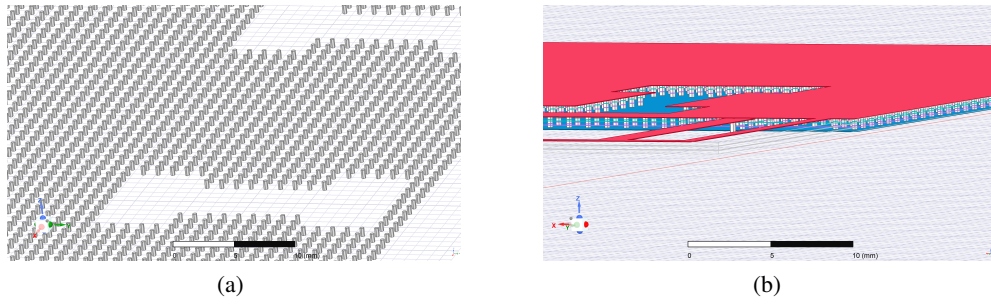


Figure 4.4: Close-up images of a realistic simulation model, showing (a) vias and (b) the top and bottom copper layers. The substrate has been omitted for better visibility of the PCB's inner elements.

aims at. Additionally, for narrowband antennas, as is the case, these aspects can truly affect the tuning process. Hence, a third design phase, described in Figure (c), where the changes applied to the design are based on real-world prototypes, is needed.

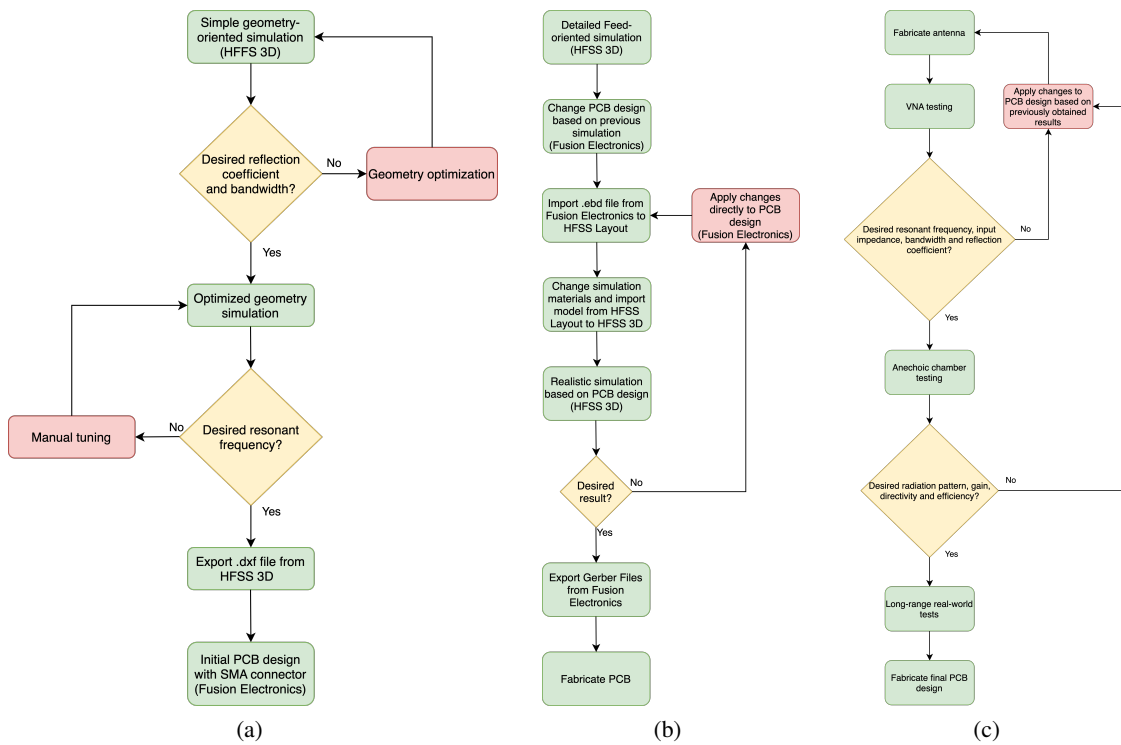


Figure 4.5: Flowcharts for the (a) first, (b) second and (c) third design phases.

4.3 First Design Phase: Exploratory Simulations

4.3.1 Tuning and Geometry Optimizations

There are at least 7 topological parameters that need to be finely adjusted in order to achieve the desired characteristics. These are:

- Radiator length;
- Radiator-Ground spacing (also known as bend height);
- Ground plane width;
- Ground plane size;
- Feed-Short spacing;
- Copper thickness;
- Substrate thickness.

This means that tuning the antenna manually is not simple and, consequently, automated parametric optimizations are required. These are made entirely possible by the simulation program that was used, HFSS².

For the optimization process it is necessary to choose one or more goals and an optimization algorithm, which can be iterative, gradient-based, Artificial Intelligence (AI) based or even custom-made using Matlab. Genetic Algorithm (GA) optimizers are recommended by ANSYS for problems with large solution spaces [49]. They have been proven useful for antenna design [50][51], including for the design of PIFAs [52]. GAs present better results when compared to gradient-based algorithms, because the latter might converge on undesirable or underperforming local minima, if solving for large solution spaces. GA optimizers can, however, take much longer to converge. Nonetheless, obtained results are almost always better when using this kind of optimization algorithm. This is why the GA optimizer provided within HFSS was used not only for tuning the antenna but also for impedance matching the feed line, finding the ideal format and size of DGSs and finding the smallest possible ground plane size that provided a quasi-isotropic radiation pattern.

The subsections that follow describe a great variety of working designs for miniature LoRa antennas. These showcase the effects of some antenna parameters on performance and the effects of other modifications, such as adding DGSs. Although many designs are proposed, some of them are found unsuitable for the project. The last section, 4.5, presents the antenna dimensions that were actually fabricated for the end node, based on conclusion drawn throughout the chapter.

²Ansyes Electronics Desktop is a software platform that bundles several simulation programs made by Ansys, such as HFSS 3D, HFSS Layout, Maxwell, Icepack and more. Only HFSS 3D and HFSS Layout were used for the project described in this document. Therefore, and to simplify reading experience, Ansys Electronics Desktop is referred to as just HFSS, throughout document.

4.3.2 Radiation Pattern and Polarization

Figure 4.6 depicts the typical radiation pattern of a PIFA. On the E-plane, the radiation pattern is slightly tilted, due to the bend in the radiating element. However, this does not affect the omnidirectionality of the antenna, as the H-plane is always approximately isotropic. For the case of the PIFA that is shown, the H-plane is made by the union of two semi-planes: $\Phi = -60^\circ \wedge \Phi = 120^\circ$. In this plane the front-to-back ratio is around 0.3 dB, meaning that almost the same power is radiated in both Φ directions and, therefore, although very slightly directional, the antenna is mostly omnidirectional.

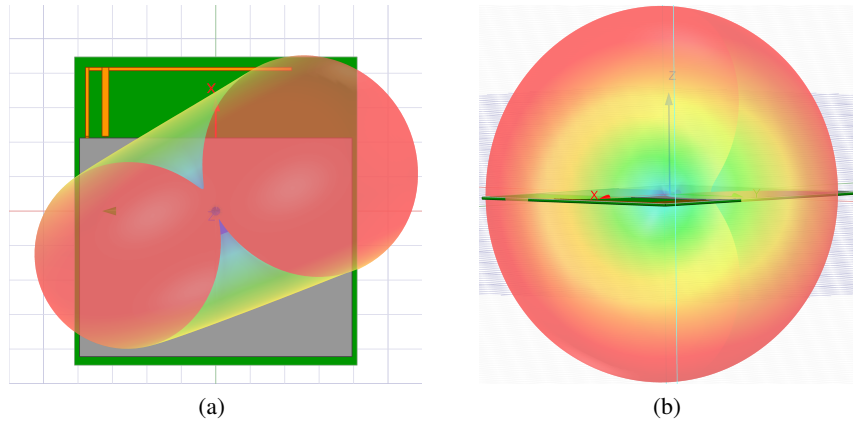


Figure 4.6: (a) Top and (b) side views of the 3D radiation pattern for the simulated PIFA with a dumbbell-shaped DGS and fed with an ideal 50Ω lumped port.

The polarization of the antenna is also mostly linear as shown by the axial ratio plot shown in Figure 4.7. In the directions of maximal gain, the axial ratio is always greater than 25 dB. Essentially, this means that the antenna is polarization-efficient and most radiated power has approximately perfect polarization, reducing PLF, which is the amount of energy lost due to polarization mismatch (described in Subsection 2.3.5).

4.3.3 PIFA vs Meandered PIFA

MPIFAs, a common variation of PIFAs, are used for space-critical applications. As explained in Subsection 3.2.1, meander lines capacitively load the radiating element, which has a large impact on antenna size. This means that MPIFAs can be significantly smaller than their non-meandered counterparts, however presenting all the drawbacks explained previously. The main goal of the exploratory simulations described in this section was to analyse the advantages and disadvantages of MPIFAs for LoRa and determine if they were suitable for the end node that was being developed.

Figure 4.8 shows the geometry-oriented simulation models of a MPIFA and a PIFA. As shown in Table 4.2, the MPIFA version takes around 52% less space than the PIFA implementation. However, it presents 50% smaller gain and a return loss 4.5 times larger, as depicted in Figure 4.9.

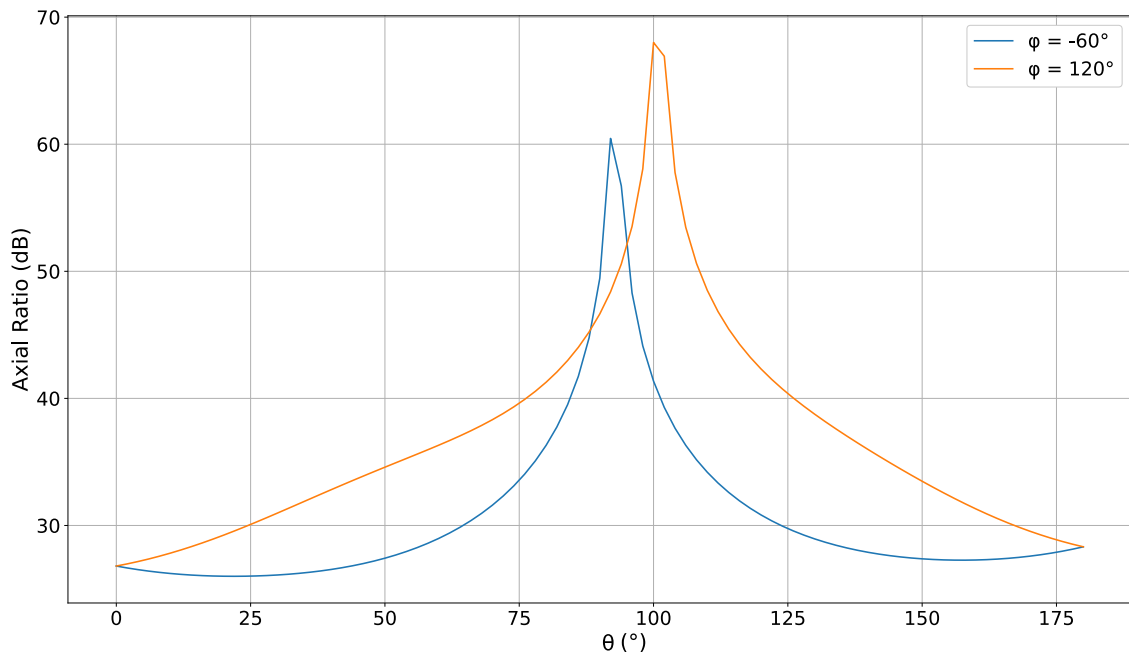


Figure 4.7: Axial plot for the two semi-planes that constitute the H-plane of the antenna.

Antenna	Return Loss (dB)	Gain (dBi)	Bandwidth (MHz)	Efficiency	Size (mm ²)
MPIFA	-21.47	0.80	17	77%	3157.77
PIFA	-27.97	1.59	62	97%	6637.23

Table 4.2: Parameter comparison between the PIFA and MPIFA designs used for the exploratory simulations about the effect of meanders on PIFAs for LoRa.

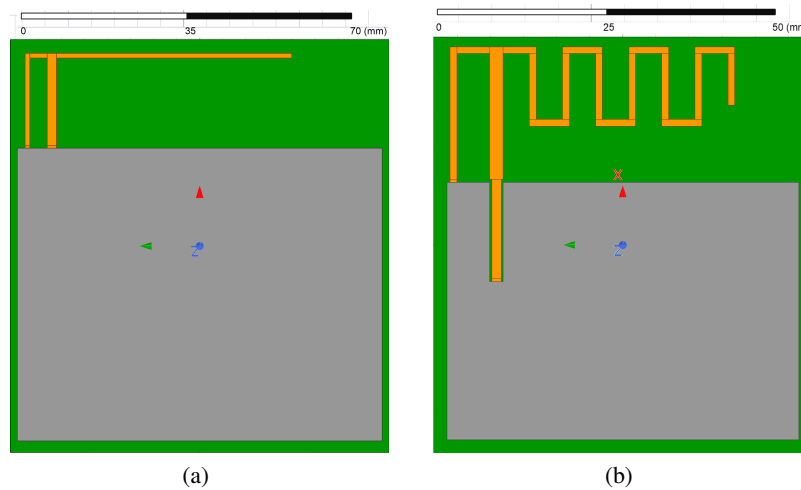


Figure 4.8: Geometry-oriented models for the (a) PIFA and (b) MPIFA.

It is important to note that increased return loss leads to considerable less total efficiency (explained in Subsection 2.3.2), which is a particularly important parameter for low-power applications, such as LoRa antennas.

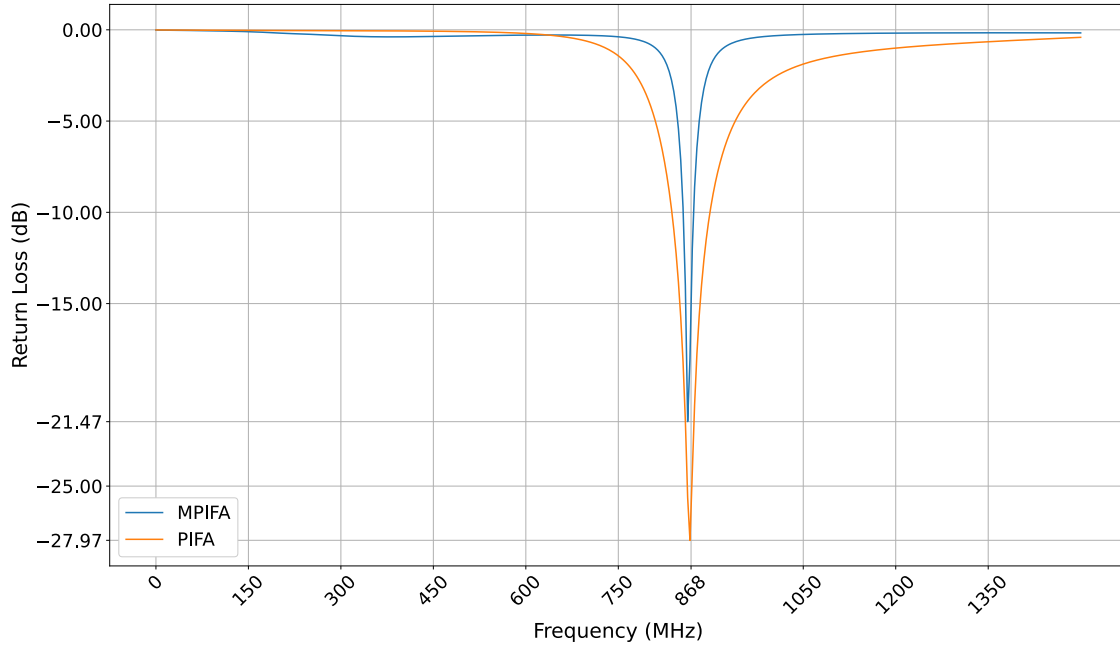


Figure 4.9: Comparison between the return loss of the (red) MPIFA and (black) PIFA.

Considering the significant reductions in gain and efficiency, and considering that the size of both implementations was within Wavecom’s requirements, it was decided that a non-meandered PIFA would be used for the LoRaWAN end node as its better gain and efficiency would allow for longer range and battery life, and increase the number of use-cases of the device.

4.3.4 Defected Ground Structures for Single-Layer PIFAs

As mentioned in Section 3.1, DGSs can effectively improve antenna performance. Nevertheless, these structures are more prominently used for microwave and millimeter-wave applications [36, p. 86]. There is little research on the effects of DGSs for sub-gigahertz frequency bands, such as the ones LoRa operates in. Moreover, DGSs are particularly difficult to model (in terms of their effects) for any frequency band [36] [38], discouraging their use. This section describes the simulations that were conducted with the purpose of understanding the effects of DGSs in single-layer PIFAs and deciding whether DGSs should be implemented in the end-node’s antenna.

There is a multitude of DGS shapes and designs that have been proposed throughout the years, some of them tailored for multi-band operations (such as slot-based DGSs), others with the purpose of providing size reduction or even performance enhancement.

Following the efforts and knowledge acquired with the work described in Chapter 3, it was decided that further research into Dumbbell-Shaped DGSs (DSDGSs) for the EU863-870 ISM band could be potentially useful for this project. DSDGSs were chosen for the following reasons:

- When DSDGSs were first proposed (in [36]), they were presented as an easier way to implement DGS with the corresponding equivalent lumped-element circuit;

- The relationship between the dimensions of a DSDGS's and the added capacitance, inductance and resistance that it induces is clearer than for other DGS shapes, making it easier to tune, considering the already challenging frequency band;
- DSDGSs have been shown to substantially improve the gain of PIFAs in [53], albeit for much higher frequencies;
- It is easy to visually access the ideal orientation of DSDGS based on the E-field vectors over a certain surface, which helps the placement of this type of DGS.

DSDGSs can be modelled using the circuit shown in Figure 4.10. The defect's equivalent model capacitance value is dominated by the gap distance, g_d , while inductance is mainly affected by the separation between the rectangular cuts and the area of those cuts. The model's resistance is mainly due to the defect's radiation resistance, which is harder to correlate to any physical dimension of the DSDGS.

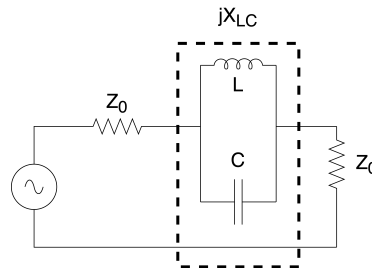


Figure 4.10: Equivalent circuit of the implemented DSDGS [36]. The dotted box denotes the DSDGS section (in this case, a perfect LC resonator without resistance) and Z_0 is the in/out impedance seen from the ports.

The first step in developing the defected ground plane was finding the approximate dimensions and number of DGSs that started to have an impact on the antenna's performance. This was done manually and the values that were found to have somewhat of an impact on the antenna's gain were used as starting points for the optimization process.

Due to the amount of parameters that affect the DGS's properties, a parametric GA-based optimization was used. The optimization process, which is thoroughly explained in Subsection 4.3.1, yielded the dimensions, number and position of DGSs that produced the best gain enhancement. The resulting configuration is shown in Figure 4.11.

Figure 4.12 depicts the orientation and magnitude of the E-field vector over the ground plane surface. The E-field vectors run parallel to the radiating element across most of the ground plane, indicating that best result should be achieved with vertical orientation of the DSDGS. That same figure also demonstrates that the implemented defects do disturb currents in the ground plane, which is necessary to generate the displacement currents responsible for the reactive loading that enhances the antenna's performance.

Figures 4.13 show that the DSDGS does increase antenna gain by around 0.4 dB, making the defected PIFA's radiation pattern similar to that of the half-wave dipole.

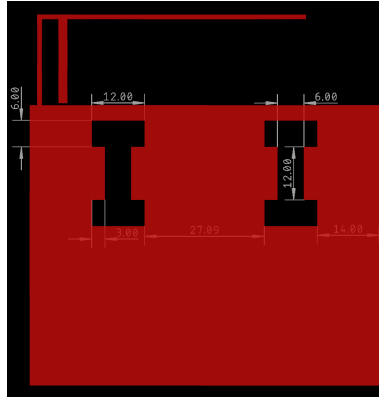


Figure 4.11: Optimized dimensions for the DSDGS.

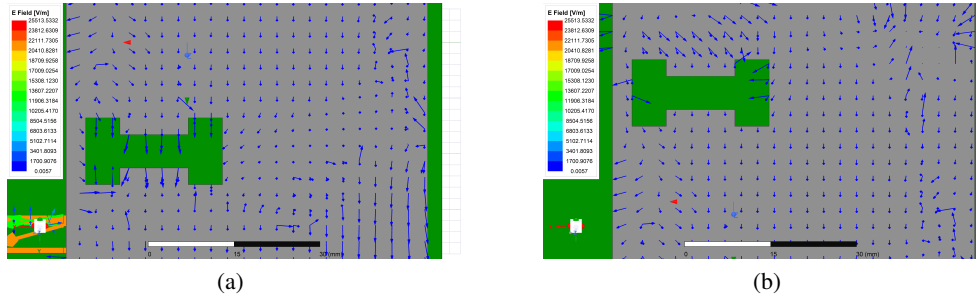


Figure 4.12: Detailed view of the E-field vectors near the (a) left DGS and the (b) right DGS.

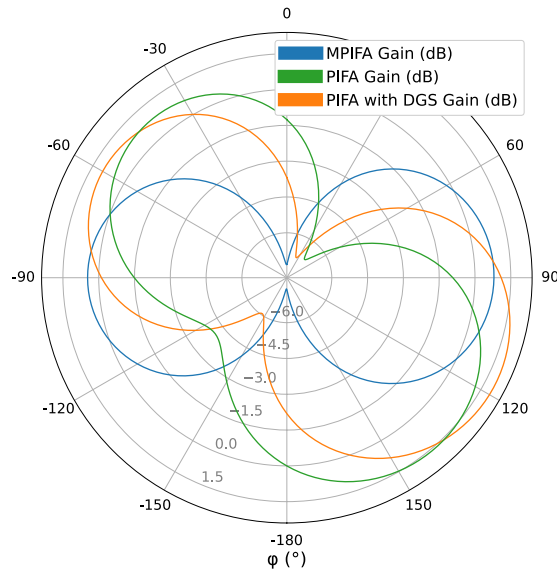


Figure 4.13: Comparison, on the E-plane, between the meandered PIFA, the PIFA and the PIFA with a dumbbell-shaped DGS.

Figure 4.14 compares the return loss of the MPIFA and PIFA presented in Subsection 4.3.3 with that of the PIFA with DSDGS presented in this subsection. The DGS also drastically enhanced impedance matching and reduced return loss to about -35 dB.

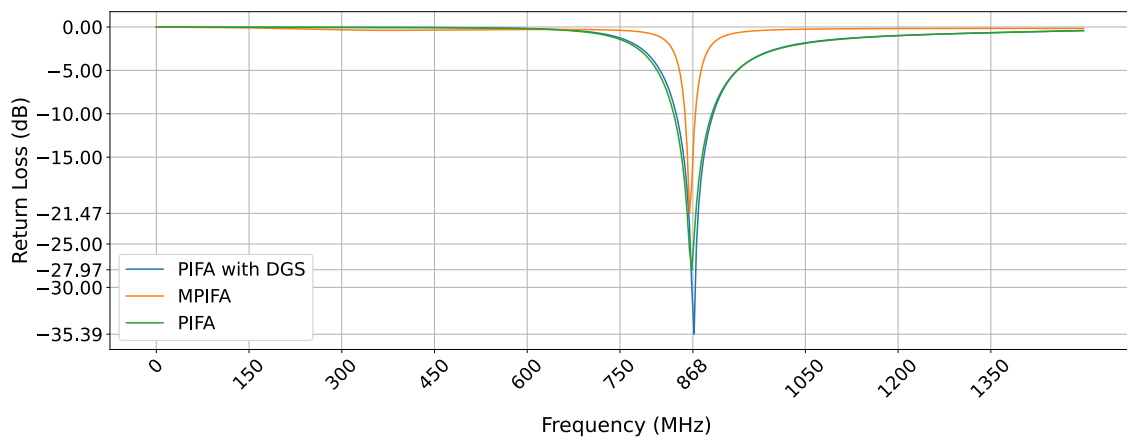


Figure 4.14: Return loss for the PIFA, MPIFA and PIFA with DGS.

Table 4.3 summarizes the main aspects of the proposed MPIFA, PIFA and PIFA with DGS designs. From this results it can be concluded that, MPIFAs are useful solely for extremely space limited applications, since the gain performance of this design is rather poor. Even though a traditional PIFA occupies a larger area it is still a single-layer planar design which results in an antenna that has a very useful and compact size, suitable for the IoT industry, considering that 6600 mm^2 roughly corresponds to the area of an adult's palm. Assuming that the electronics can be integrated into the antenna's ground plane, the size of the proposed PIFA and PIFA with DGS designs are also within Wavecom's requirements. The addition of DSDGS does improve the PIFA's gain to a value that is close to the maximum allowed for the EU863-870 ISM band, as mentioned in Subsection 2.2.4. Nevertheless, it does complicate integration with the rest of the device's systems, due to taking up a large portion of the ground plane. Solutions to this challenge are covered in the next subsections.

It is important note that these results were obtained for the traditional one-layer implementation of PIFAs with only a single ground plane layer. As noted in Section 4.3.6, DGSs have been found to be much less effective on PIFAs with multiple ground planes or with solid ground blocks.

Antenna	Return Loss (dB)	Gain (dBi)	Bandwidth (MHz)	Efficiency	Size (mm^2)
MPIFA	-21.47	0.80	17	77%	3157.77
PIFA	-27.97	1.59	62	97%	6637.23
PIFA with DGS	-35.39	1.92	60	97%	6637.23

Table 4.3: Comparison of some fundamental parameters of the MPIFA, PIFA and PIFA with DGS.

4.3.5 Ground Plane Considerations

PIFAs are a variation of the quarter-wave monopole antenna. Consequently, the ground plane is an essential part of the antenna, as is the case for monopoles. An ideal ground plane would

be a uniform and infinite perfect conductor placed just below and perpendicular to the radiating element. The more a ground plane is disturbed with electronic components, the less uniform, the less conductive, and the smaller it becomes due to the cutout's for component pads. This subsection describes the exploratory investigations that were conducted as a way to determine which ground configuration would better compensate for the disturbance of electronic components and have the best impact on antenna performance.

The ideal ground plane configuration for the antenna designs proposed in this section would consist of a 4-layer PCB, where the two top-most layers would be densely via stitched and the two bottom-most layers would help with routing for the electronics. Figure 4.15, uses Fusion Electronics' stack manager to present the two types of vias that would be needed for this configuration. The Blind type (which connects layers 1 and 2) would make via stitching possible on solely the upper layers and the Thru type would connect all ground planes. This would be the ideal solution, because via stitching only the top-most layers would provide RF shielding between the antenna (top) part and the (bottom) digital electronics part of the device, while still providing a decently large and dense ground plane that should improve the antenna's gain and overall performance. The bottom-most layers would work as an almost independent double layer PCB, helping with the task of trace routing, which would be impossible using only one layer of copper.

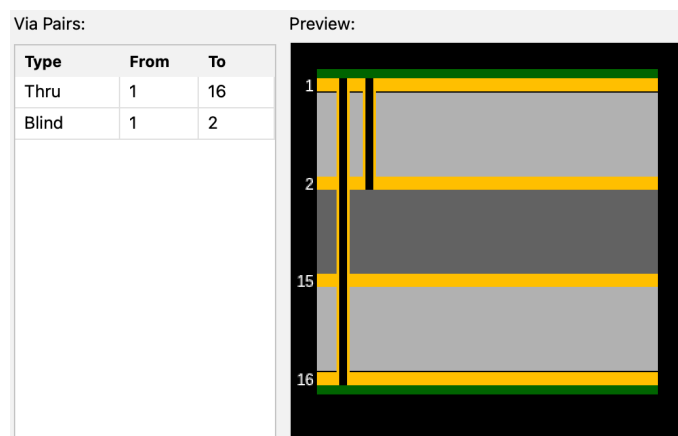


Figure 4.15: Fusion Electronics' stack manager, depicting thru (through-hole) and blind vias.

This solution does have a quite relevant drawback, though. Which is that blind vias are orders of magnitude more expensive to manufacture than thru vias. The configuration that was proposed in the last paragraph would indeed cost upwards of €150 per board, even on a mass production scheme. This is definitely outside the low-cost goal of this project, where each board should cost no more than €5 to manufacture. As a result, other solutions for ground plane configuration had to be investigated.

One possible setup, would be to use a 4-layer PCB, depicted in Figure 4.16a, with 4 ground planes to increase ground plane size and to provide some shielding. These ground planes would be connected at the back of the board as shown in Figure 4.16b (note that this is a geometry-oriented simulation and, therefore, via stitched regions are approximated by copper blocks).

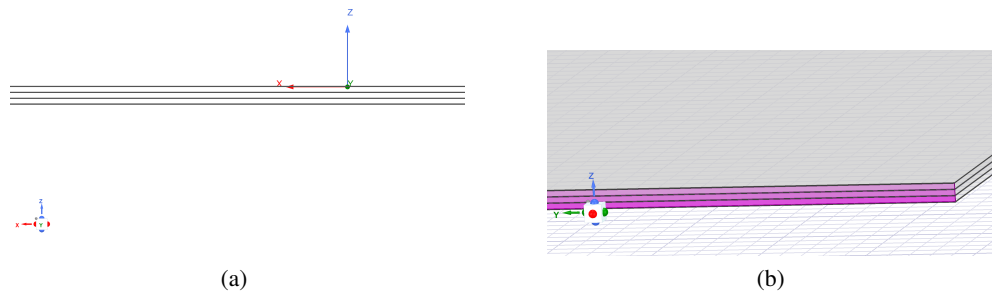


Figure 4.16: Details of (a) the side view and of (b) the (pink) ground plane connection at the back of the board (substrate is omitted) for the configuration with 4 ground planes and thru type vias.

Depicted in Figure 4.17 is yet another configuration that was considered, using a simple 2-layer PCB with via stitching limited to the back of the board, connecting the two ground planes. This would provide very little RF shielding and a rather small ground plane volume, decreasing the antenna's performance. Nevertheless, it is the solution with the easiest implementation.



Figure 4.17: Detailed side back view of the configuration with 2 ground planes (substrate omitted for better visibility).

The last solution that was considered, was to use two densely via stitched ground planes (Figure 4.18), forming a uniform ground plane block that increases total ground plane volume and, consequently, the antenna's performance. With this configuration, although there is not an explicit ground plane shield between the RF and digital components, due to the densely via stitched PCB, return currents from the electronics are relatively contained to the regions near the copper traces, reducing inference between RF and digital components. Additionally, the return current from the antenna feed is contained in the front bottom part of the board as shown in Figure 4.19. This region of the board was intentionally left vacant of digital components to reduce interference.

Figure 4.20 depicts the return loss for these three situations: 4 ground planes, 2 ground planes and a single ground plane block, which represents an approximation of two densely via stitched ground planes. This figure demonstrates how ground plane configuration mostly affects return loss at 868 MHz and harmonics. A higher count of ground planes certainly adds more layout and trace routing flexibility when it comes to designing the PCB. However, it creates some undesired

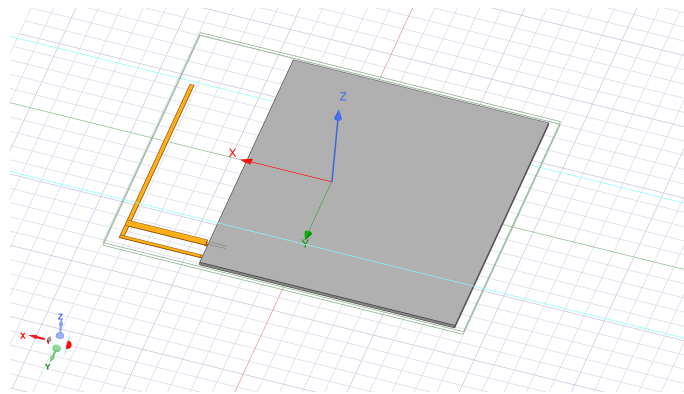


Figure 4.18: Geometry-Oriented model of a ground block configuration, made up of two densely stitched ground planes.



Figure 4.19: Magnitude of the E-field (current distribution) for the back part of the ground block.

additional resonant frequencies at around 550 MHz, where the return loss, specially for the double ground plane configuration, almost reaches the critical value of -10 dB.

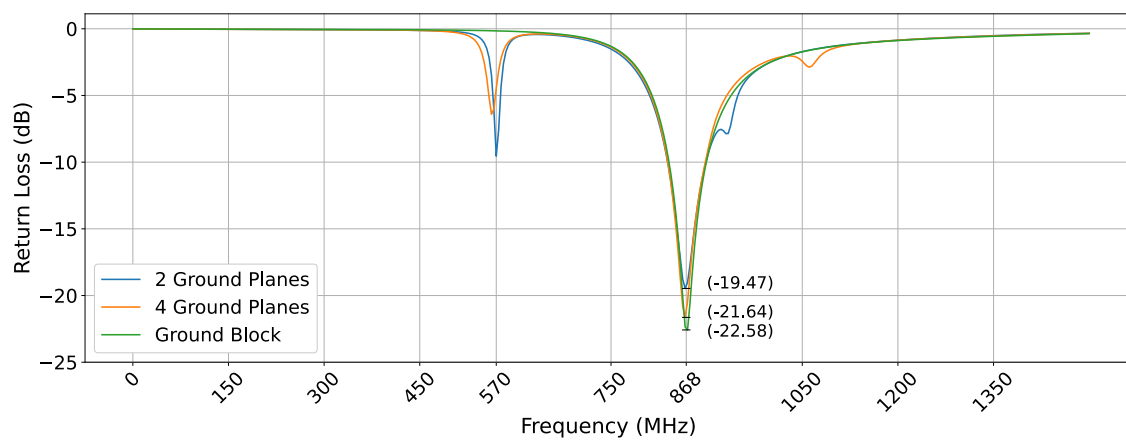


Figure 4.20: Return loss for different ground plane configurations, namely: (red) four ground planes, (blue) two ground planes and (green) a single ground plane block.

4.3.6 Defected Ground Structures with a Solid Ground Block

The DSDGS was not removed from the design when transforming the ground plane into a solid ground block, since the objective was to study the effects of this ground configuration in an antenna with DGS and to understand if such configuration allowed for easier integration with electronic components on the bottom side of the board (since the top side was mostly used for the DGS). However, it was later discovered that using a ground block instead of a ground plane also increases the gain of the PIFA design. In fact, it has an effect rather similar to the use of the DSDGS described in Subsection 4.3.4. This lamentably means that, initially, it was not understood that the gain enhancement for a PIFA with DGS and a solid ground block was not due to the DSDGS but rather to the increase in ground volume. The correct explanation that is responsible for the actual gain increase was only fully understood much later in the project.

Upon realizing that the interpretation of simulation results was wrong, and that ground volume increase was the actual cause of gain enhancement for ground configurations other than single-layer, alternative solutions that could make DSDGSs work tried to be implemented. Now that a 2-layer implementation is used, DGSs can be used to load the feed line of the antenna instead of the ground plane directly, similarly to how DGSs are conventionally used in microstrip and CPWG transmission lines. This was not possible with the single layer implementation of the ground plane and allows for the defects to be placed near the regions of higher E-field magnitude. Figure 4.21 shows the location of the new DSDGS. Please note that the orientation of the DGS is now horizontal due to orientation of the E-field vectors on that region, that can be seen in Figure 4.21.

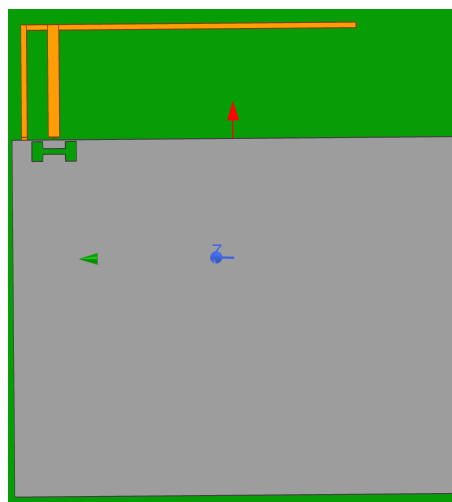


Figure 4.21: Alternative DSDGS placement, that takes advantage of the CPWG feed line configuration to load it.

Unfortunately, this alternative solution only slightly increased gain (around 0.1 dB) even after shape optimizations were conducted (in the same manner of previously described DGSs). Additionally, this solution deforms the uniform ground plane beneath the feed line, transforming it into a line that is no longer a standard CPWG. Because of this, the perfect impedance match was lost and realized gain actually decreased. Using the methods explained in Subsection 4.3.1, the

short-feed distance was changed and tried to be optimized for impedance compensation. Even so, it proved difficult to match gain and realized gain and to find any configuration that substantially enhanced at least one of them.

Therefore, it was concluded that, contrary to the case of PIFAs with ground planes, for PIFAs with ground blocks, DGSs, or at least DSDGSs, do not have a substantial impact on antenna performance. Due to this, two boards, one with and another without DGS, were fabricated, resulting in two designs for the antenna prototypes and two end node prototypes, each corresponding to a different design (PIFA and PIFA with DGS). This is further explained in Section 4.5 and in the next chapter.

4.3.7 Feeding Considerations

When using the solid ground block configuration mentioned in Subsection 4.3.5, it is possible to integrate electronic components with the antenna easily. These components can be placed on both sides of the board without affecting antenna performance significantly. However, the placement of the transceiver module was found to significantly affect antenna gain.

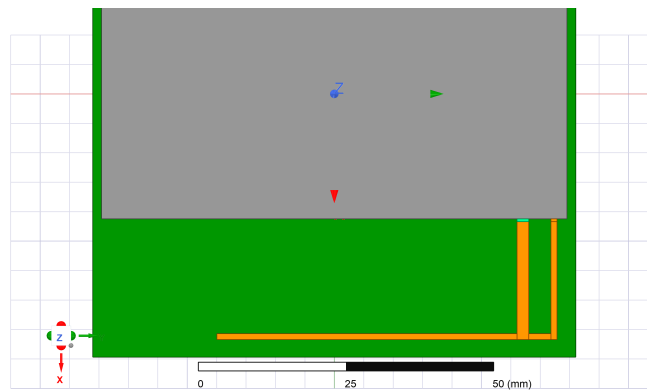


Figure 4.22: Geometry-oriented model of the top-fed PIFA with ground block.

Top-fed and bottom-fed geometry-oriented models are shown in Figure 4.22 and Figure 4.23. The top-fed PIFA design is easier to implement in a real prototype as the transceiver module can be placed near the antenna feed line, possibly needing a very short CPWG transmission line or even none at all. The bottom-fed model was harder to implement as the use of a feeding via is required, which creates a hybrid transmission line configuration, shown in Figure 4.23. This transmission line consists of a CPWG section and a non-standardized portion, requiring impedance matching through parametric optimization (described in Subsection 4.3.1). The primary objective was to determine the outer via diameter that minimized return loss.

Figure 4.24 depicts the 3D radiation pattern of both feeding techniques. The bottom-feeding technique enhanced antenna gain by 0.4 dB, achieving 2 dBi of gain (and the same value for realized gain, due to the perfectly matched feedline impedance enabled by the aforementioned parametric optimization). The return loss of approaches is shown in Figure 4.25.

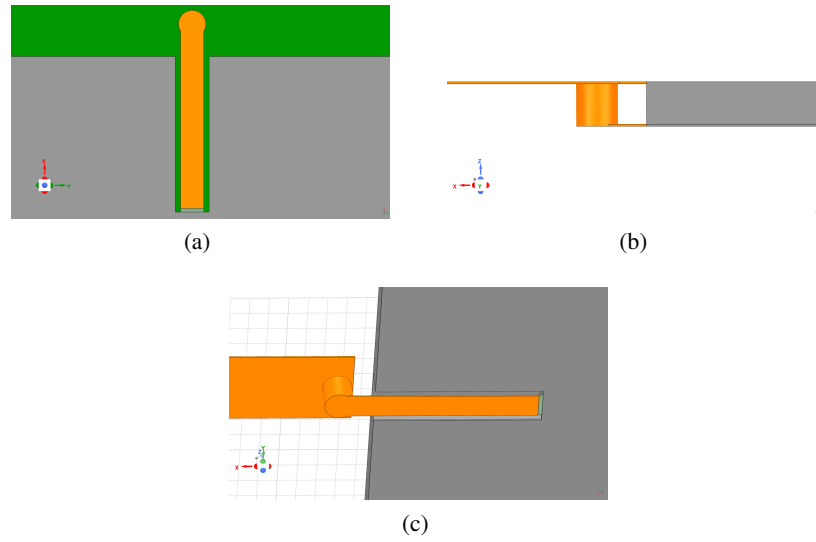


Figure 4.23: Detailed view of the bottom-fed PIFA geometry-oriented model, depicting (a) the hybrid CPGW and parametrically optimized transmission line, (b) a side and (c) perspective view of the feeding via. (substrate omitted for better visibility)

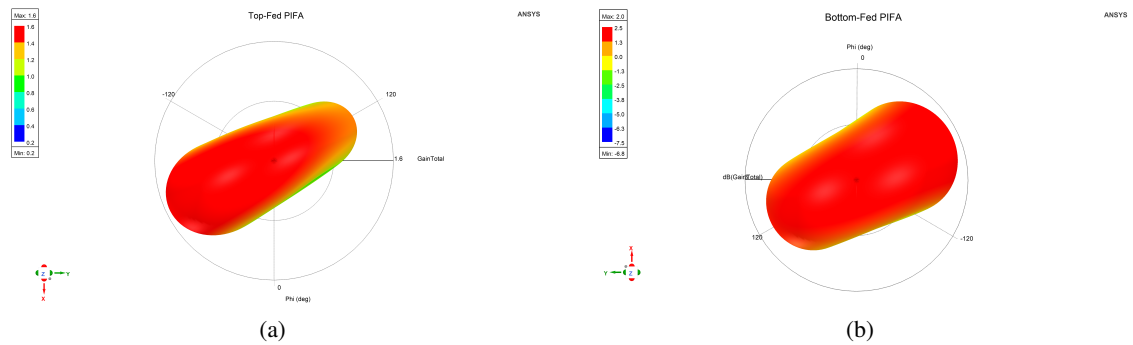


Figure 4.24: 3D radiation pattern for the (a) top and (b) bottom feeding techniques.

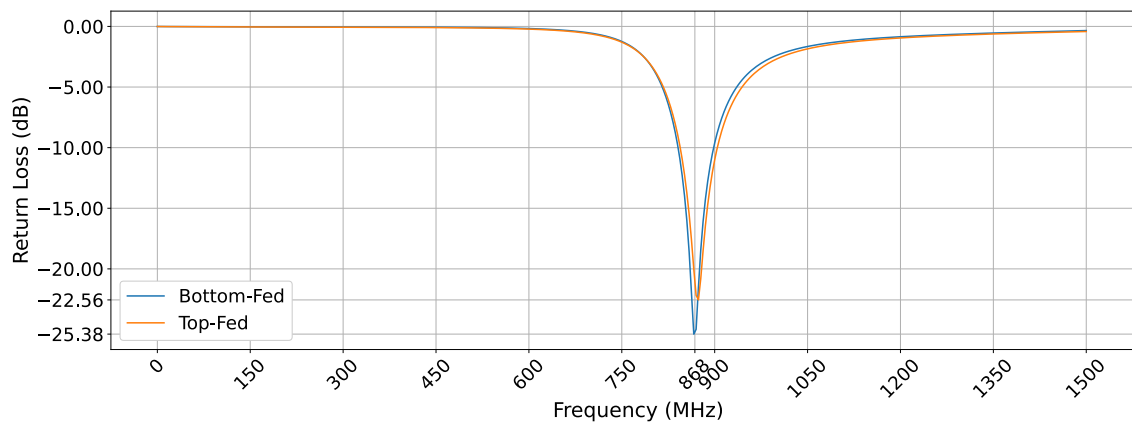


Figure 4.25: Return loss of both the bottom and top feeding techniques.

4.3.8 Effects of Radiator-Ground Spacing on Bandwidth, Gain and Efficiency

As noted in Subsection 3.2.3, the spacing between the radiating element and the ground plane mainly affects bandwidth, as a shortening of this distance increases radiator-ground capacitance which, in turn, reduces bandwidth and increases the operating frequency.

Figure 4.26 show three geometry oriented models representing two PIFA implementations with different radiator-ground spacings. Figure 4.27 and Table 4.4 compare the return loss, realized gain and radiation efficiency of each design variant.

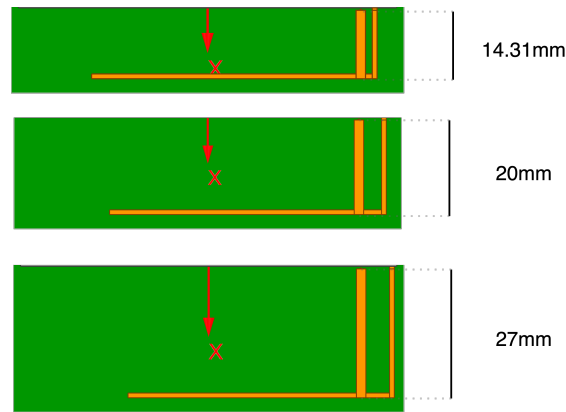


Figure 4.26: Geometry-Oriented models with different radiator-ground spacings.

The PIFA with the shortest spacing between the radiating element and ground plane offers a 6.8% reduction in area at the cost of around 20 MHz of bandwidth (approximately a 50% reduction). Solely from a bandwidth and size perspective, this design is more effective as it removes unnecessary bandwidth at the cost of size. This technique, however, also reduces gain by 0.2 dBi. Additionally and as explained in Section 4.3.1, perfectly tuning PIFAs with bandwidths below 40 MHz becomes challenging, which can make such narrowband designs undesirable for mass production and commercial applications.

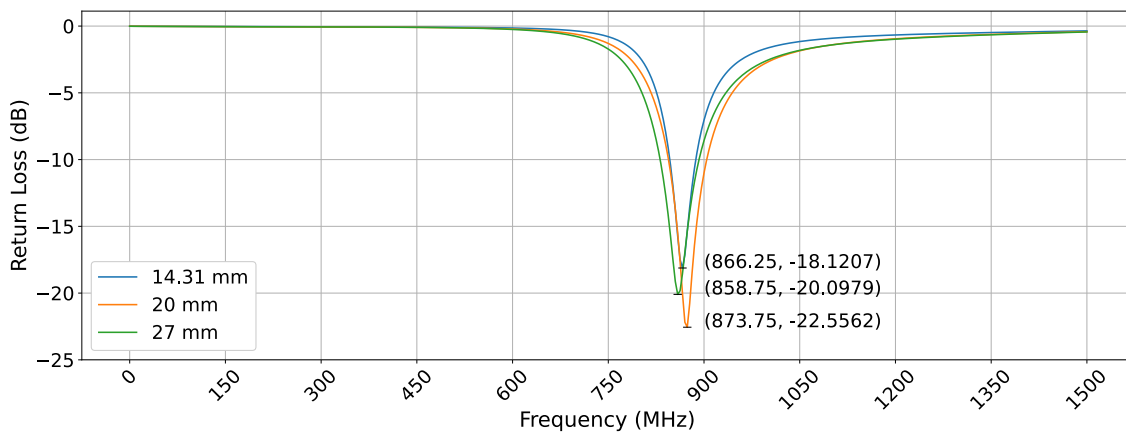


Figure 4.27: Effects of radiator-ground spacing on return loss.

Radiator-Ground Spacing (mm)	Bandwidth (MHz)	Radiation Efficiency	Gain(dBi)	Realized Gain (dBi)	Area(mm ²)
14.31	41	96.43%	1.7	1.7	6184.84
20	60	96.43%	1.9	1.9	6638.81
27	61	96.38%	2	2	7190.86

Table 4.4: Summary of the effect of radiator-ground spacing.

4.4 Second Design Phase: Feed-Oriented and Realistic Simulations

4.4.0.1 Feed-Oriented Simulations

To characterize the antenna, following the procedures described in Section 6.1, an implementation of a PIFA fed with a SubMiniature version A (SMA) connector was needed, so that the antenna could be connected to laboratory equipment. This version of the antenna ought to be as similar as possible to the chip-fed PIFA, so that valid conclusions can be drawn.

Figure 4.28 shows the 3D models of the transceiver and SMA connector that were imported into HFSS. Each part of both models was assigned a specific material (be it Teflon, copper, FR-4) based on their respective datasheets [54] [55]. For the transceiver module, this also included defining an output impedance of 50Ω and making cutouts in the ground plane for the pads (except for those connected to ground). The SMA connector model was excited using a wave port, as recommended by Ansys for this kind of connector [56].

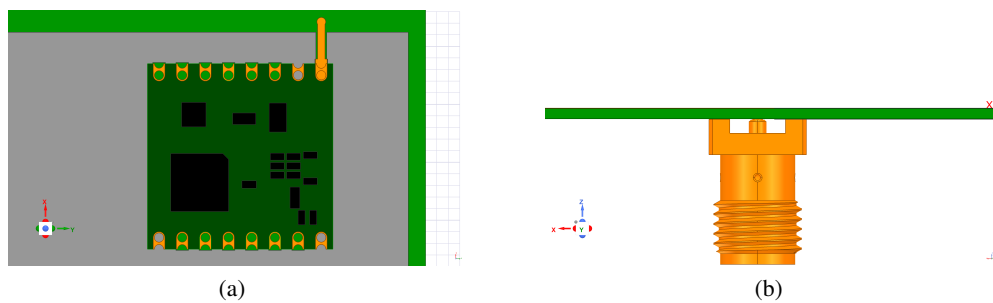


Figure 4.28: 3D models used for (a) the transceiver module and (b) the SMA connector. The ground pads of the transceiver module are actually connected to the ground block in the simulation model to achieve the most realistic results possible.

Figure 4.29 compares the return loss for the bottom-fed PIFA without DGS, when fed with a SMA connector and with the transceiver chip. Clearly the SMA connector has a big impact on the antenna. This can be due to two factors. Firstly, the SMA model made available by the manufacture (and the connector's datasheet), only represented the outer parts of the SMA connector. Consequently, the inner parts of the model had to be completed using measurements taken from a real connector. This process might not have been precise enough, resulting in poorer results. Secondly, the SMA connector adds a very significant amount of metal to the ground plane of the antenna, which has a great impact on input impedance (explained in Section 3.2.3), making

increasing its return loss. This tried to be corrected as much as possible without changing the dimensions of the antenna substantially. Otherwise, the SMA-fed antenna would be significantly different from the chip-fed one, which is not the purpose of adding the connector. The results presented in Figure 4.29, represent the best return loss that could be achieved for an SMA-fed version of the antenna that still had comparable dimensions to the chip-fed version.

Chapter 6 does show that SMA-fed version of the antenna had a poorer performance than the chip-fed version. Nevertheless, the tests with real world prototypes of Chapter 6 showed that the SMA connector had a much smaller impact on the antenna than estimated by the simulations, which made it a useful prototype for testing.

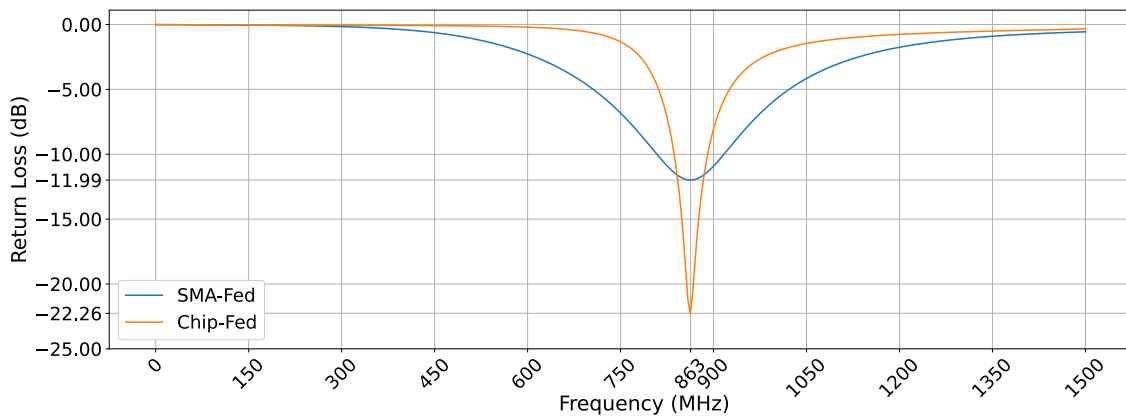


Figure 4.29: Return loss of the SMA-fed PIFA(black) and of the chip-fed PIFA (red).

4.4.0.2 Realistic Simulations

Realistic simulations models were used to validate the final antenna design. From the exploratory simulations described in the previous sections, results two final designs: one PIFA with DSDGS and another one without. Both antennas were bottom-fed and had solid ground block instead of single-layer ground planes. Figure 4.30 shows some realistic HFSS models extracted from Fusion Electronics.

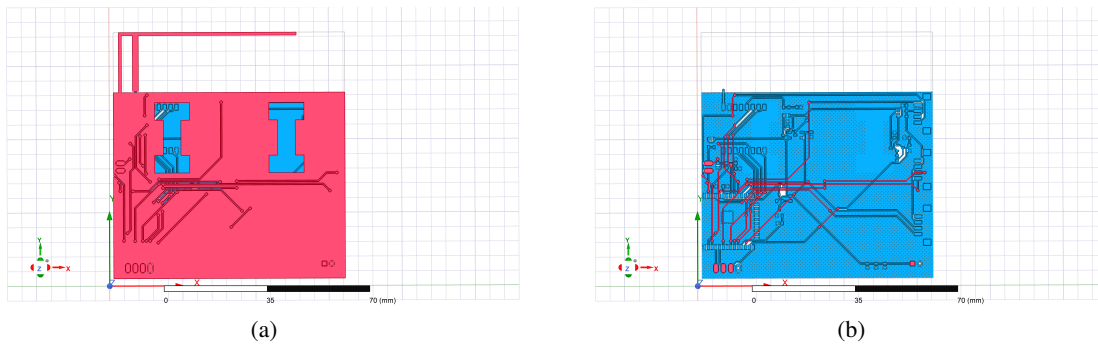


Figure 4.30: (a) Top and (b) bottom layers of a realistic model for the PIFA with ground block and DSDGS.

These realized gain simulations shown in Figure 4.31 successfully validated the designs and showed that the approximations used for geometry-oriented simulations were valid. The simulated gain and radiation pattern shape were completely unaffected by the use of realistic models.

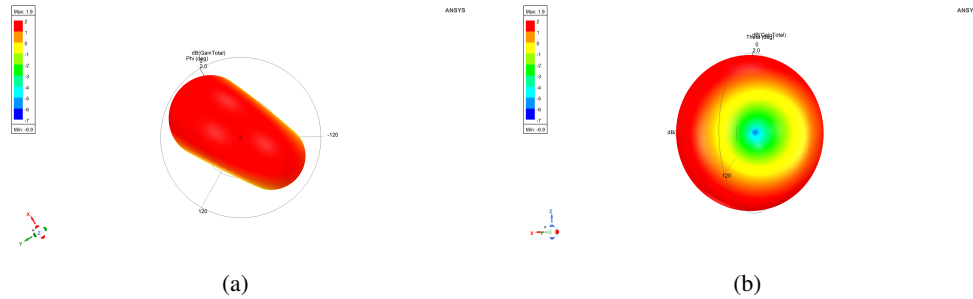


Figure 4.31: Realized gain simulations using a realistic simulation model for the (a) top and (b) side views of a realistic simulation model for the PIFA with DGS.

4.5 Third Design Phase: PCB Prototypes

The third design phase mainly consisted on tuning the antennas using real world prototypes. Figure 4.32 depict two different prototypes used to determine the effect of soldermask on the antenna. It was found that, although in HFSS even a thin soldermask layer had a significant impact on the resonating frequency, with real world prototypes soldermask had little to no influence on the antenna. As a result it was decided that the final antenna prototypes should have soldermask covering the antenna, since it adds an extra layer of protection to the device and the soldering process (Figure 4.33) is facilitated when tented vias are used.

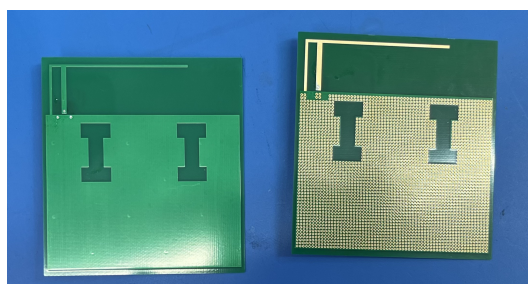


Figure 4.32: Early prototypes used to evaluate the effects of soldermask on the antenna.

Subsection 4.3.6 explained that increased gain in PIFAs with ground blocks is due to the increased ground volume and bottom-feeding and not due to the implemented DSDGS, which only had effect on PIFAs with single-layer ground plane. This understanding came late during the development process when a version of the PIFA with DGS had already been fabricated. As a result, two antenna prototypes were fabricated and compared. To differentiate these, Table 4.5 distinguishes both designs and the names used to refer to each board throughout the document.

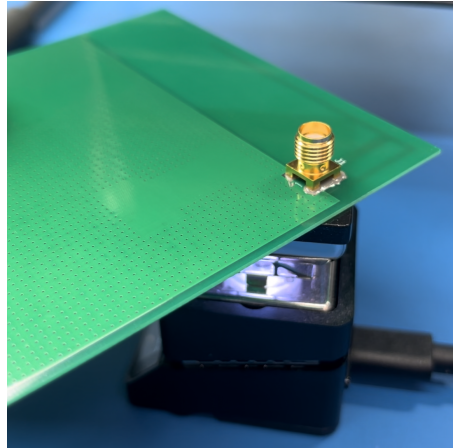
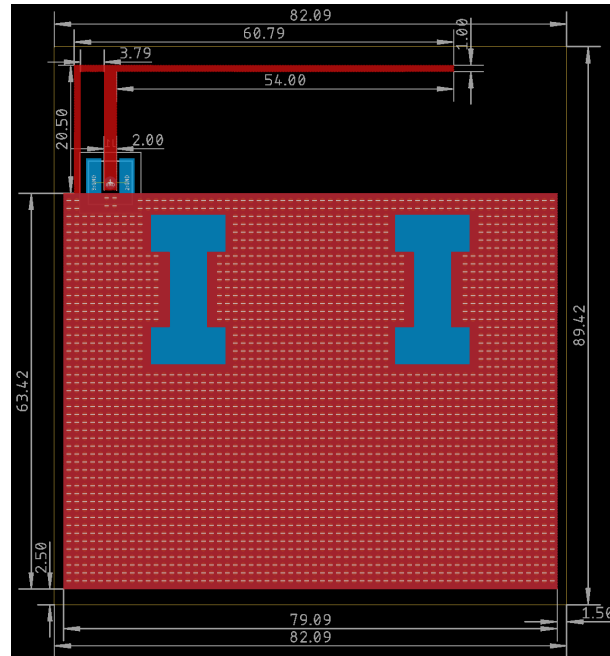


Figure 4.33: Soldering process, using a small heat bed and solderpaste.

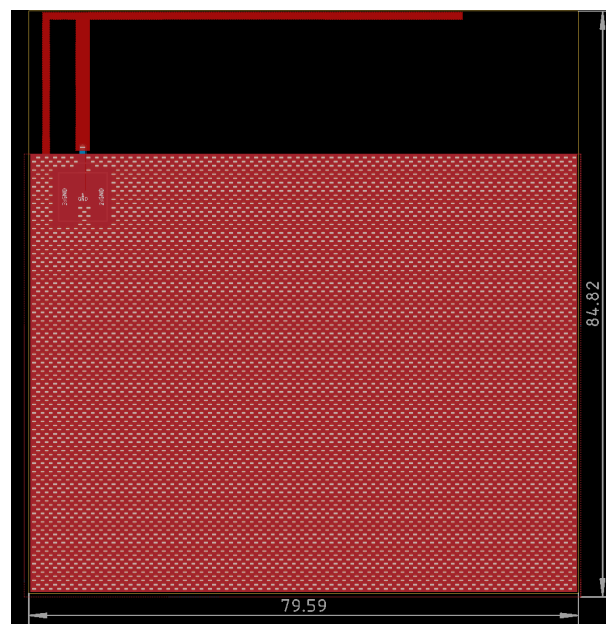
Board Name	Antenna	Dimensions
SMA1	PIFA with ground block. Bottom-fed using a SMA connector.	Figure 4.34a
SMA2	PIFA with ground block and DSDGS. Bottom-fed using a SMA connector.	Figure 4.34b

Table 4.5: Summary of the fabricated antennas and the respective names used throughout the next chapter to mention them.

The final antenna prototypes were fabricated based on the findings described during this chapter. The inclusion of meander lines, radiator-ground spacing and ground plane configuration were all decided taking into account the simulated results of this chapter. Trying to achieve the best performance/size ratio possible, the topology and dimensions presented in Figure 4.34 were ultimately chosen for the end node's antenna.



(a)



(b)

Figure 4.34: Dimensions of the fabricated PIFAs (a) with and (b) without DGS. Dimensions that are the same for both designs do not show in (b).

Chapter 5

End-Node Development

5.1 Wavecom's Requirements

Wavecom established some key requirements for the end node, mainly in terms of size, performance and applicability.

The device should be flexible in terms of applicability and be suitable for multiple use-cases. With this in mind, Wavecom specifically required the use of *Grove* connectors, a type of connectors made by *Seed Studio* that supports several kinds of sensors and communication protocols.

In terms of size, no specific restrictions were defined. However, the device should have an interesting performance/size ratio, i.e., the device should be small enough to have a wide range of use-cases, but the compromise in performance should be carefully considered as the device should have at least 6 years of battery life and a realized gain close to that of the half-wave dipole.

5.2 End-Node Design

5.2.1 System Architecture

Figure 5.1 depicts a high-level overview of the end-node's systems and how they interact. The main parts of the end node are the Micro-Controller Unit (MCU), the communications system and the power system, described in the next subsections. These constitute the absolute minimum for a working end node:

- **MCU:** implements the link- and network-layer protocols of the LoRaWAN stack, prepares and sends uplink data packets to the transceiver module, controls sleep cycles, manages power distribution to different parts of the board, stores relevant data such as session keys, frame counters and other protocol-related information;
- **Communications system:** made up by the antenna and the transceiver module that is responsible for implementing the physical layer protocol of the standard;

- **Power system:** powers every other system on the board and is made up of a battery and several Low Dropout Voltage (LDO) regulators that can be enabled/disabled by the MCU for power management.

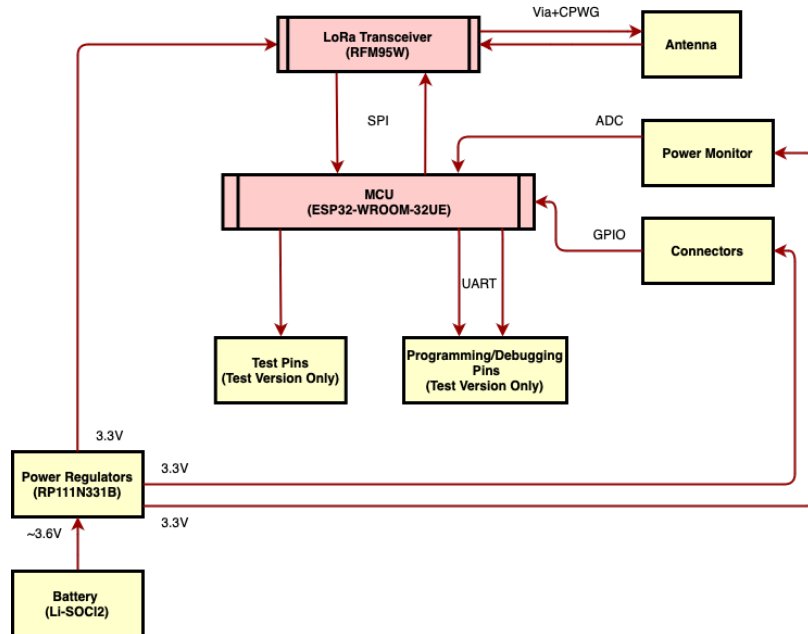


Figure 5.1: System architecture for the non-rechargeable variant.

Figure 5.1 also shows other less critical systems:

- **Programming pins** used to upload firmware to the MCU via Universal Asynchronous Receiver-Transmitter (UART), these are used only during the early development phase and are not included in final version of the end node. The MCU can be programmed Over The Air (OTA) without needing external pins (which can also represent a security vulnerability);
- **Test pins:** two sets of two male 2.54 mm pin headers serve testing purposes. The set connected to the power system allows the use of a power supply instead of a battery and the one connected to the MCU power pins enables the use of an ammeter. These are useful to measure current draw and were important for the power consumption test delineated in the next chapter;
- **Connectors:** three horizontal Grove Surface Mount Device (SMD) connectors provide an interface for a multitude of digital and analogue sensors and actuators;
- **Power Monitor:** used to measure battery voltage, so that a crude estimate of battery capacity can be included in data packets.

5.2.2 Micro-Controller Unit

The end node's Micro-Controller Unit (MCU) is a ESP32-D0WDR2-V3 System-on-a-Chip (SoC), which is integrated within the ESP32-WROOM-32 module. This MCU features a Xtensa dual-core 32-bit architecture and a variable clock speed ranging from 80 MHz to 240 MHz. It offers abundant resources, including up to 520KB of SRAM, 2MB of PSRAM and up to 16MB of external flash memory [57]. It also includes integrated Wi-Fi and Bluetooth capabilities. Additionally, the ESP32-D0WDR2-V3 supports various wired communication protocols and peripherals such as Serial Peripheral Interface (SPI), Inter-Integrated Circuit (I2C), Inter-IC Sound (I2S), UART, Digital-to-Analog Conversion (DAC), Analog-Digital Conversion (ADC) and General-Purpose Input/Output pins (GPIO), making it versatile for interacting with external devices and sensors. Its rich set of features and powerful performance make the ESP32-WROOM-32 module an excellent choice for a multi-purpose IoT device, especially considering its low-power and deep-sleep capabilities.

The module is also adaptable to different use cases. Depending on whether Wi-Fi capabilities are needed for certain applications, different versions of the module can be used. Figure 5.2 shows the E and UE versions, which have the same pinout and are fully interchangeable, making it possible to save space on the board if the integrated Wi-Fi antenna is not needed.

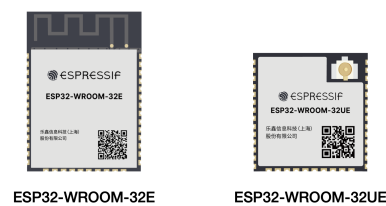


Figure 5.2: The different variants of the MCU module, which are fully interchangeable allowing for more versatility of the end node.

Another important factor that influenced the selection of this MCU is the deep-sleep capabilities it has. One of the most important part of any class A LoRaWAN end node is being able to hibernate the device during periods where there are no tasks to perform. Figure 5.3 shows the different sleep mode of the ESP32-WROOM-32 module and how difference features become unavailable as power consumption is restricted. Ideally, the device would enter *hibernation* mode during sleep periods. However, the only part of the module that can be used during *hibernation* mode is the Real-Time Clock (RTC) timer, which may not be enough for some applications. Naturally, from a perspective of power consumption, it is desirable that the MCU enters the deepest sleep mode possible for any given task. To determine that mode two aspects need to be considered: wake-up trigger mechanism and sleep functionalities.

The wake-up mechanism for most class A LoRaWAN devices is a simple timer that ensures the device wakes up a certain amount of times per day to read sensors and send data. Some devices might also wake up using external triggers from sensors and class B devices might wake up to listen to network beacons and spontaneous downlink messages. This would require the use of the MCU's

GPIO pins connected to the transceiver and to sensors as wake up triggers. Fortunately, the deepest mode of sleep, *hibernation* mode, supports both of these wake-up mechanisms.

As to the functionalities that the device needs during sleep, those are mainly related to memory use. Class A devices presuppose applications that are not dependent on device availability. As a result, rejoining a network and regenerating sessions key every time an uplink message needs to be transmitted would increase network congestion and decrease Quality of Service (QoS) and is not necessary for LoRaWAN class A end nodes. Instead, two other approaches are recommended in Semtech's LoRa developer portal [58], which involve either acknowledging a small percentage of uplink messages or occasionally sending link check requests. These approaches help minimize the number of messages that a device sends to the network while not being online, without triggering a re-join procedure for every transmission. However, to prevent a re-join, device need to store session keys, duty cycle counters, frame counters and other protocol-related data during. With ESP32 MCU we can accomplish this using the external flash memory or RTC memory. Flash memory is non-volatile, therefore the device could enter the deepest sleep mode possible, *hibernation* mode. Nevertheless, the external flash memory of the ESP32-WROOM-32 module has a maximum of 100 000 write/erase cycles [59]. On the other hand, RTC memory, that can be indefinitely used, is volatile and needs to be powered during sleep if data is to be stored. Consequently, when using RTC memory, the deepest sleep mode the MCU can enter is *Deep-Sleep: RTC timer + RTC memory* mode. The firmware used to validate the device in Chapter 6 uses the sleep mode and stores session data in RTC memory. Energy consumption test in that same chapter demonstrate that, for the small amount of stored data that is needed using RTC memory and entering *Deep-Sleep: RTC timer + RTC memory* mode is practically equivalent to entering *hibernation* mode.

Power mode	Description			Power Consumption
Modem-sleep	The CPU is powered on.	240 MHz *	Dual-core chip(s)	30 mA ~ 68 mA
			Single-core chip(s)	N/A
		160 MHz *	Dual-core chip(s)	27 mA ~ 44 mA
			Single-core chip(s)	27 mA ~ 34 mA
		Normal speed: 80 MHz	Dual-core chip(s)	20 mA ~ 31 mA
			Single-core chip(s)	20 mA ~ 25 mA
Light-sleep	-			0.8 mA
Deep-sleep	The ULP coprocessor is powered on.			150 μ A
	ULP sensor-monitored pattern			100 μ A @1% duty
	RTC timer + RTC memory			10 μ A
Hibernation	RTC timer only			5 μ A
Power off	CHIP_PU is set to low level, the chip is powered off.			1 μ A

Figure 5.3: Sleep modes for the ESP32-D0WDR2-V3 chip.

5.2.3 Transceiver Module

The RFM95W transceiver incorporates a LoRa modem and presents a sensitivity of over -140 dBm. The integrated power amplifier, combined with the high sensitivity, result in a link budget that make the module an ideal choice for applications requiring extensive range and reliability. It also features over-current protection, low power consumption and sleep modes. This module interfaces with the MCU over SPI.

5.2.4 Power System

The power system is one of the most important parts of a LoRaWAN end node, especially in the case of this dissertation, where the aim is to create a highly flexible device suitable for a variety of use-cases. This need for flexibility might, at first sight, imply that a rechargeable battery would suit the project better. A rechargeable device would serve a wider range of applications, as it could be used with or without solar panels, for example. Rechargeable batteries, particularly lithium-ion ones, have decent capacity and high maximum continuous and pulse current ratings, which means they can handle transmission power spiked easily. However, lithium-ion batteries also have considerable self-discharge rates, which actually makes them inviable for non-rechargeable use-cases. Figure 5.4a shows the estimated battery life for a LoRaWAN end node, using a generic 3600 mA h lithium-ion battery with a typical self-discharge rate of 5% (3% from the battery and 2% from the protection circuit), for different values of messages sent per day and for different active times (i.e., the time that the device stays awake reading the sensors and transmitting the message). Figure 5.4b plots the same curve for a lithium thionyl chloride battery, which is a type of primary battery that present practically negligible self-discharge rates. For these graphs the MCU's worst-case active and sleep power consumption stated in the datasheet [57] was used. During the power consumption tests of Chapter 6, power consumption was found to be much for typical IoT loads and these results were recalculated.

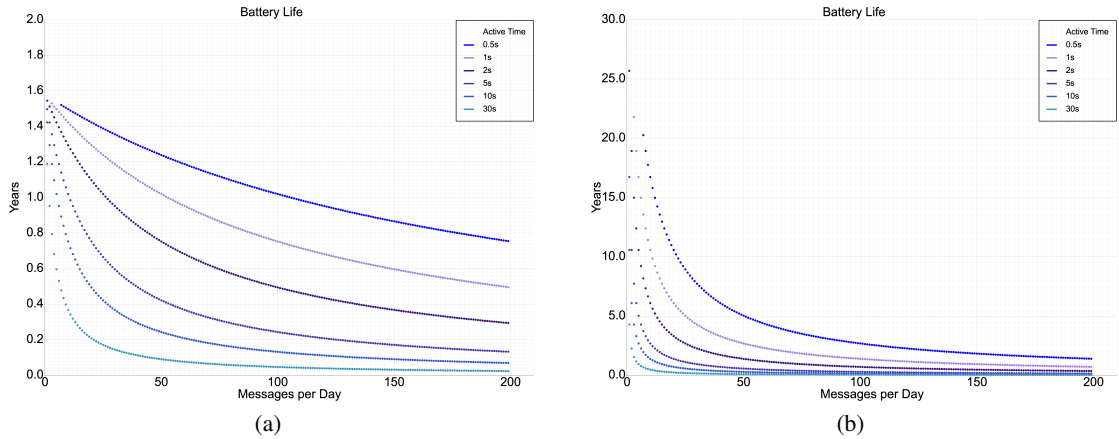


Figure 5.4: Estimated battery life as a function of messages per day and for different active times. (a) refers to a rechargeable lithium-ion battery and (b) refers to a primary lithium thionyl chloride battery.

From these results, it is obvious that lithium-ion batteries and most types of rechargeable batteries, are not suitable for low power applications. Wavecom required a device with at least 6 years of battery life or more. For this reason it was decided that primary, lithium thionyl chloride, batteries ought to be used on the device.

Apart from the battery, the power system also consists of three LDO regulators are used to independently power the 3 Grove connectors, the transceiver module and the MCU. All these regulators have *chip enable* pins, which allows finer power management. The regulator that powers

the MCU has its *chip enable* pin physically shorted to VCC and the remaining two can be turned on and off using the MCU's GPIO pins. Although using three power regulators occupies a larger space on the board, it gives much more flexibility in terms of power management and, consequently, increases battery life. For instance, some sensors require the so-called *warm up time*, a period where the sensor needs to be powered but cannot yet be read because measurements are still stabilizing, this is particularly common in Infra-Red (IR), Volatile Organic Compound (VOC) and several other sensor types. If the system had only one voltage regulator that powered the whole board, after waking up, the MCU would and the transceiver module would be wasting energy while waiting for the sensor to be ready for taking measurements. With a three LDO setup, after waking up, the MCU can turn on just the sensors and return to sleep while waiting for them to warm up (the ESP32 is able to keep the output state of GPIO pins even when asleep, so the *chip enable* pin of the LDO is kept HIGH even if the MCU is asleep). After waking up again, the ESP32-WROOM-32 module can read the sensors, turn them off, and turn the transceiver on for transmission. This means that, at every moment in time, only the systems that are strictly needed for a task are the ones that are powered on.

5.2.5 Sensors

In compliance with the requirements presented at the beginning of the chapter, 3 Grove connectors were added to the board. These have four pins, two of which are for power and the remaining serve as multipurpose pins that are connected to the MCU's GPIO pins as to provide as much flexibility as possible. Table 5.1 summarizes the capabilities of each connector.

Connector	MCU Pins	Features
J3	26, 27	GPIO, OneWire, UART, I2C, PWM, RTC, Touch(27), ADC (if not using WiFi), DAC(26).
J4	21, 22	GPIO, OneWire, UART, PWM, I2C.
J5	36, 39	ADC, GPIO, RTC.

Table 5.1: Capabilities of each Grove connector on the board.

The end node has only one on-board sensor: the power monitoring circuit. This is a simple voltage divider circuit that is connected to one of the MCU's internal ADC channels. The voltage divider was dimensioned to lower the measured voltage from the typical maximum of 4.2 V of fully charged lithium-based batteries to acceptable values for the MCU. In addition, resistor values were also chosen so that the voltage measurements fit into the most linear part of the ADC's measurement curve. The firmware also corrects for differences in measured voltages caused by variation of ADC reference voltage using the manufacturers' Application Program Interface (API). The power monitor is also the only part of the device where more expensive, but also more precise, thin film resistors are used.

5.3 PCB Prototypes

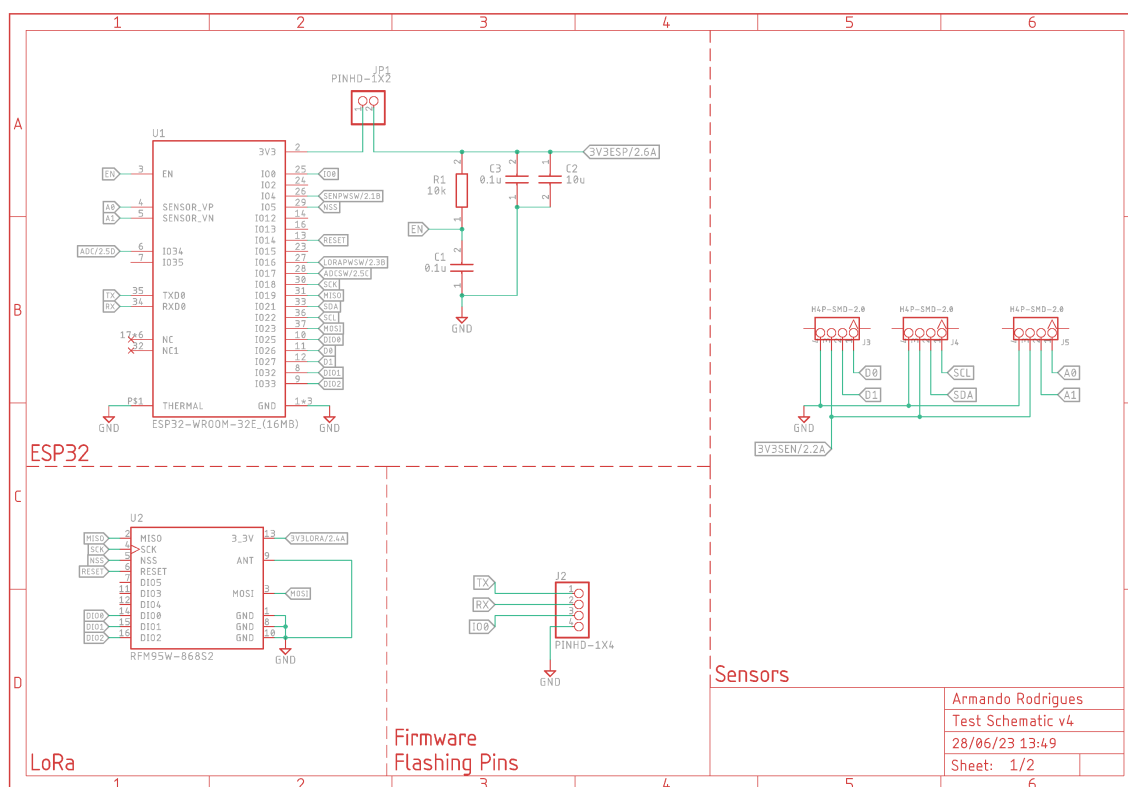
The system architecture detailed throughout this chapter was implemented in the circuit schematic shown in Figure 5.5. The only on-board sensor, the power monitor, can be turned on or off using the Q1 PMOS transistor which is controlled by the MCU using an NMOS driver. This is necessary, because the battery voltage can be higher than the maximum recommended GPIO voltage of the MCU, especially when the battery is fully charged. Therefore, the MCU cannot control the PMOS directly, needing an NMOS driver. This setup is also used for the *enable pin* of the voltage regulators. The connector used for the battery is a JST connector, which provides mechanical reverse voltage protection as it can only be plug-in in one orientation (during development this connector was replaced with pin headers to facilitate testing).

For the same reasons of Section 4.5, two boards were fabricated. These are presented in Table 5.2 and the respective dimensions shown in Figure 5.6b.

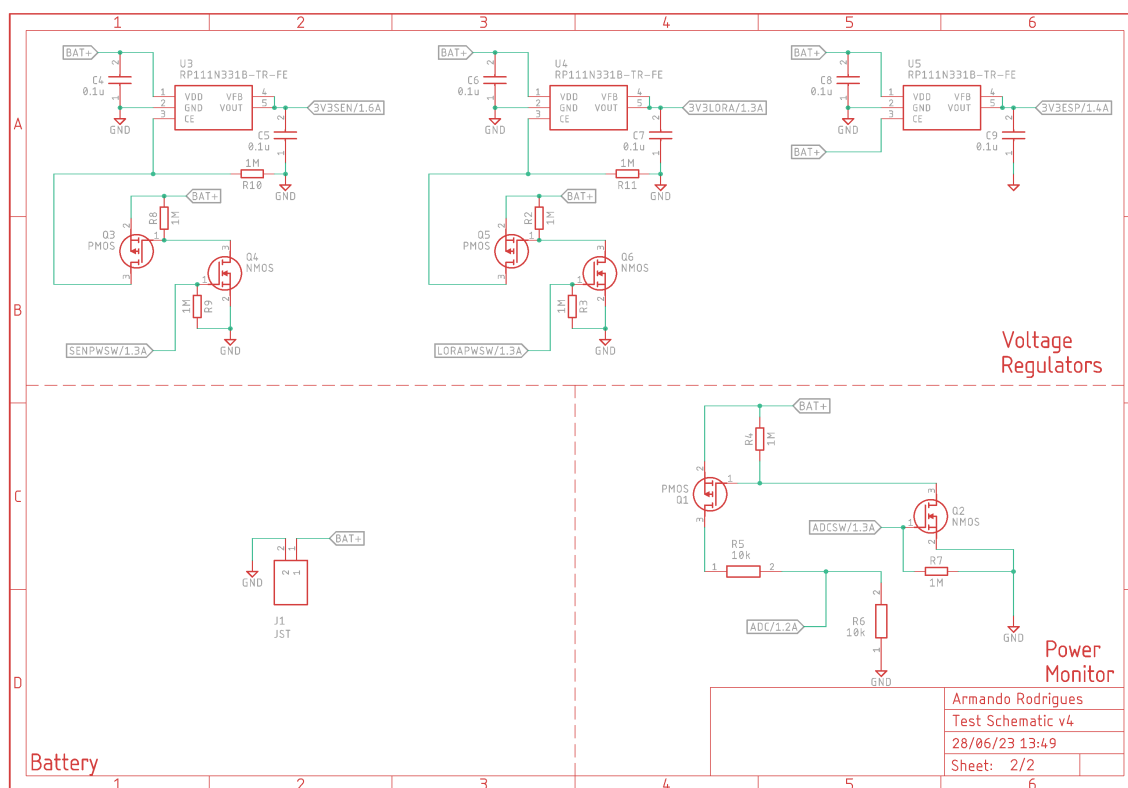
Board Name	Antenna	Dimensions
Node1	PIFA with ground block. Bottom-fed using a SMA connector.	Figure 5.6a
Node2	PIFA with ground block and DSDGS. Bottom-fed using a SMA connector.	Figure 5.6b

Table 5.2: Fabricated end node boards.

The smaller components were soldered using a heat bed and the rest of the components were manually soldered. Figure 5.7 shows the top and bottom parts of the Node1 board, already soldered and without batteries.



(a)



(b)

Figure 5.5: Schematic sheets for the (a) MCU and communications system and for the (b) power system.

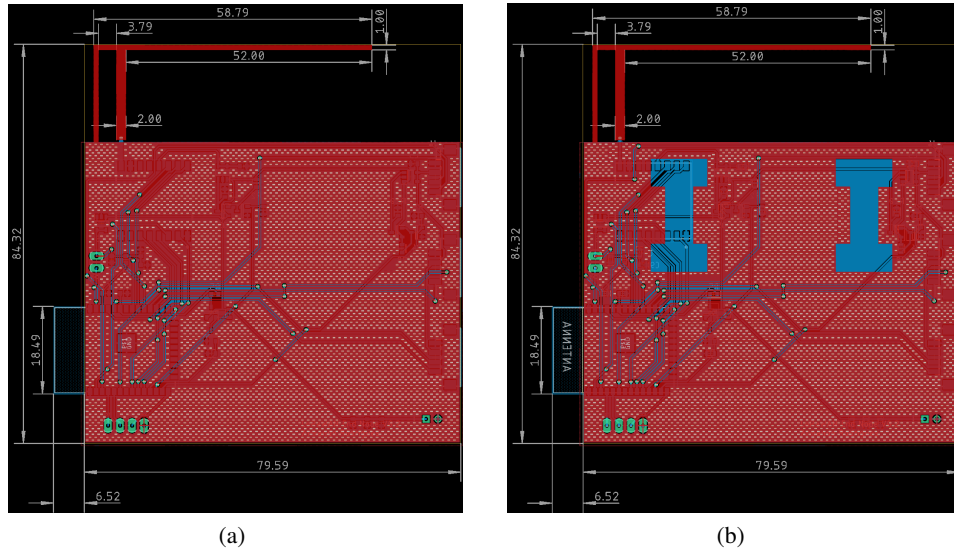


Figure 5.6: Gerber files and dimensions of the (a) Node1 and (b) Node2 boards.



Figure 5.7: (a) Top and (b) bottom sides of the Node1 board.

Chapter 6

Antenna Characterization and Device Tests

6.1 Antenna Characterization

This section covers the tests used to characterize the PIFAs of both the SMA1 and SMA2 boards. It is important to point out that the SMA2 board was fabricated only much later during this work. As a result only the tests of Subsection 6.1.1 included both boards, the rest using just the SMA1 board. Nevertheless, in that same subsection it is found that, as predicted by the simulations, the performance of both the SMA1 and SMA2 board is very similar and the results of each board on any given test are likely valid for both boards.

6.1.1 VNA Testing

6.1.1.1 Test Setup

The Vector Networks Analyzer (VNA) used for the tests described in this subsection was the *N9914A FieldFox Handheld RF Analyzer* [60]. The measurements' reference plane was brought to the antenna by careful calibration using a *85052D Economy Mechanical Calibration Kit* [61].

6.1.1.2 Results

Figure 6.1 shows the measured and simulated return loss for both antennas. The main takeaways from these tests are that the measured bandwidth and return loss are both smaller than the simulated values and that the SMA connector did not have such a big impact on the antenna's return loss as was predicted by the simulations. Additionally, it is empirically confirmed in this test that DSDGSs do not have a significant impact on PIFAs with ground blocks. Figure 6.2 compares the return loss of both antennas, showing that they are, indeed, very similar and also show that SMA2 is resonating slightly above the intended frequency. This is due to a small error in the gerber files that had to be physically corrected on the board and, consequently, slightly changed the antenna's resonating

frequency (which does not have any significant impact on the antenna's performance). The results of this test are summarized on Table 6.1.

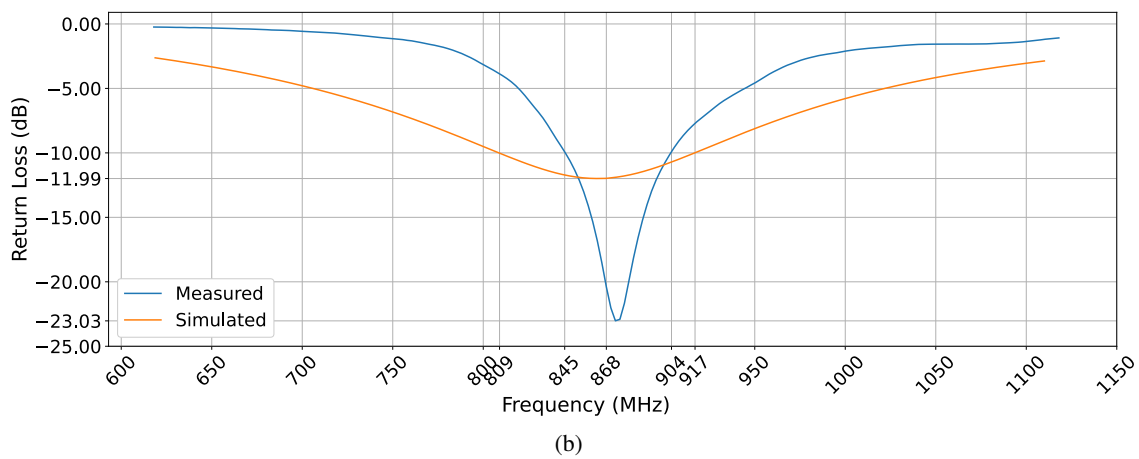
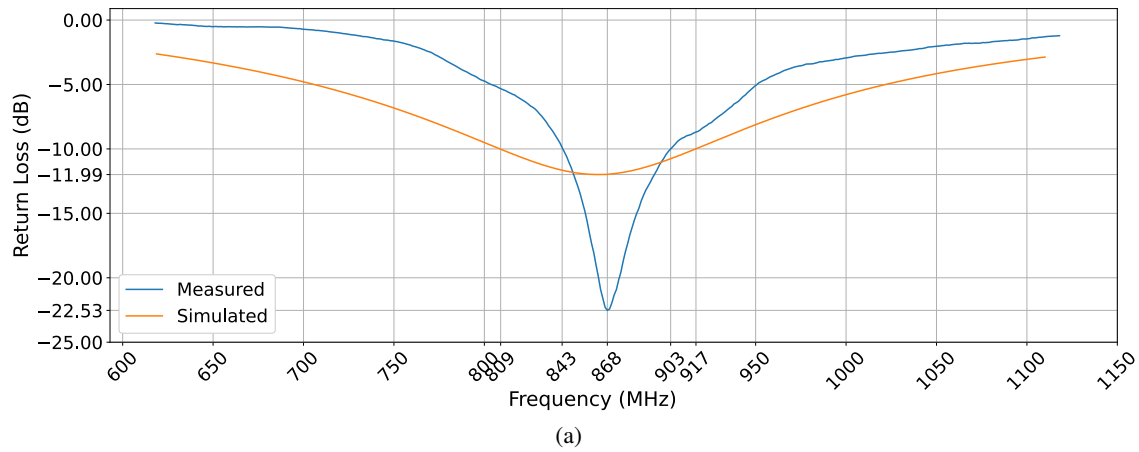


Figure 6.1: Simulated vs measured return loss for the (a) SMA1 and (b) SMA2 boards.

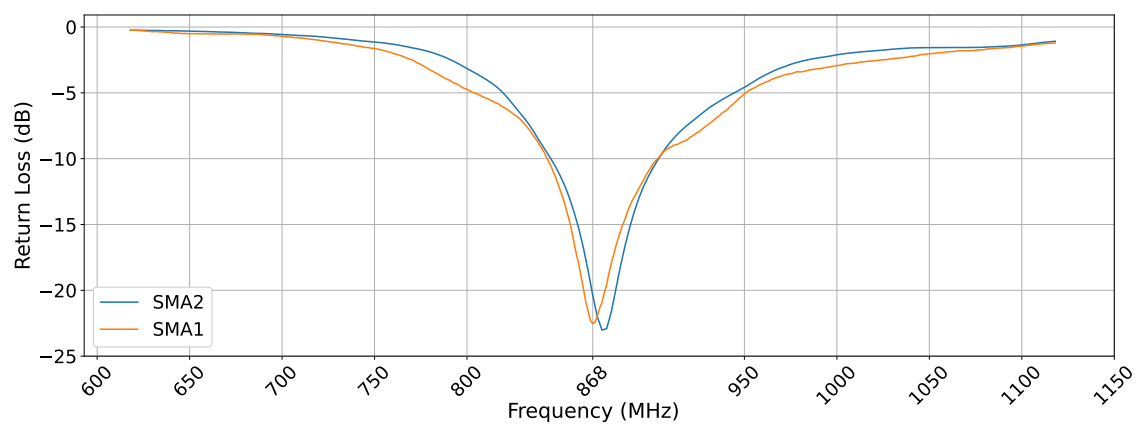


Figure 6.2: Return loss for the PIFA with (orange) and without (blue) DGS.

Board	Antenna	Return Loss @868MHz (dB)	Min. Return Loss (dB)	Bandwidth (MHz)
SMA1	PIFA with DGS	-22.53	-22.53	60
SMA2	PIFA without DGS	-20.39	-23.03	59

Table 6.1: Results of the VNA characterization.

6.1.2 Anechoic Chamber Testing

The PIFA with DGS (SMA1 board) had its radiation pattern validated with anechoic chamber tests. The PIFA without DGS (SMA2 board) was not tested for its radiation pattern shape. However, it is most likely that both antennas have very similar radiation patterns (as supported by the simulations mentioned in Chapter 4 and the aforementioned VNA tests).

6.1.2.1 Test Setup

Figure 6.3 shows both the SMA1 board and the measuring antennas used for this test. The latter being a wide-band log-periodic antenna with a realized gain of 8.85 dBi.

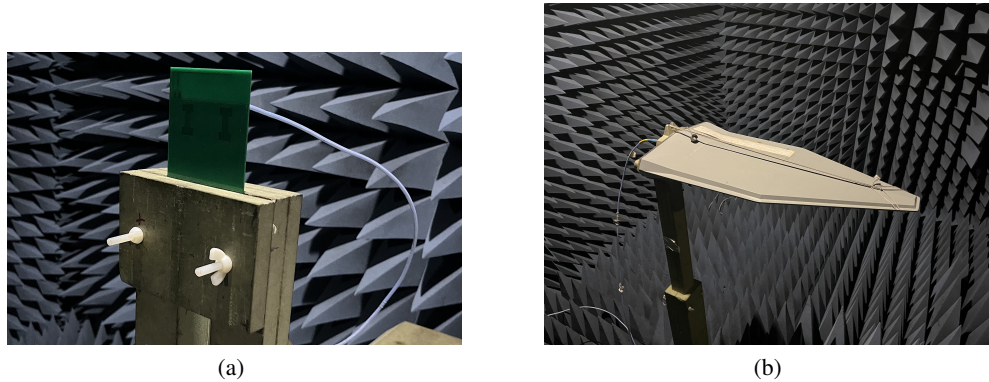


Figure 6.3: (a) SMA1 board and (b) the 8.85 dBi wide-band log-periodic antenna used as the measuring device.

Figure 6.4 shows the return loss for both the measuring antenna and the PIFA with DGS (SMA1 board). Here, it becomes evident that the cable connected to the SMA1 board is damaged, making the antenna resonate 10 MHz below its actual resonating frequency. This cable is a very long RF cable installed on the underside of the chamber. Due to time restrictions, the difficult replacement process and due to not having any cable to replace the damaged one, the test was partially invalidated, especially in terms of gain measurements. Because of this, anechoic chamber testing was used mainly to evaluate the radiation pattern's shape and gain was more grossly calculated using the test described in Subsection 6.1.3. The VNA used to take measurements in the anechoic chamber was the same FieldFox instrument used for VNA tests. In order to remove some noise, facilitate measurements and avoid having to take several readings and post-process data, real-time

8-point averaging and smoothing operations were performed. Figure 6.5 depicts the results of these operations.

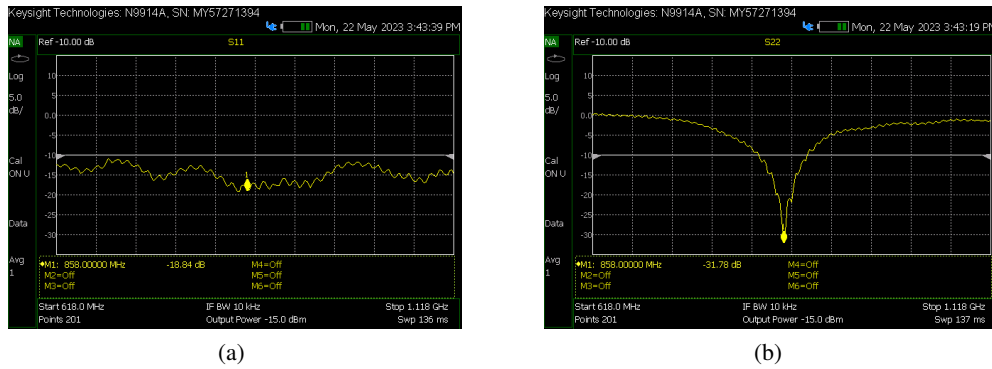


Figure 6.4: Return loss for (a) the measuring device and (b) the SMA1 board. It is possible to see that the faulty cable causes the antenna's resonating frequency to decrease.

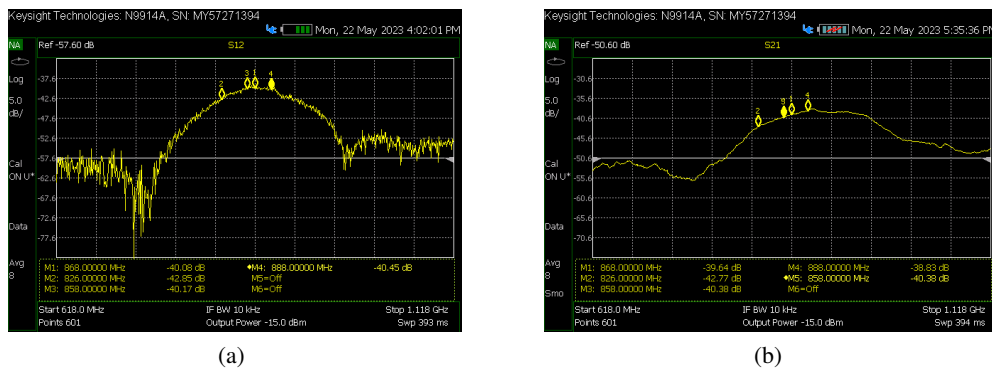


Figure 6.5: Measured S21 (a) before and (b) after smoothing and averaging.

6.1.2.2 Results



Figure 6.6: Simulated (black) and measured (orange) radiation pattern's shape comparison for the (a) E-Plane and on the (b) H-Plane.

Figure 6.7 shows the measured gain on the E- and H-plane of the antenna. It indicates a realized gain of around 1.7 dBi on the main lobe of the E-Plane and a negative gain on the second lobe. This is better than the feed-oriented simulations (that showed a very significant impact of the SMA, with a realized gain of around 0.3 dBi) but still far worse than the chip-fed version of the antenna. In fact, and according to the simulations of Chapter 4, the chip-fed version of the antenna should have a realized gain of almost 2 dBi and a front-to-back ratio of 0.3 dBi. Results similar to these simulations were actually obtained for the gain measurement tests described in Subsection 6.1.3. Even though the SMA connector did seem to have an impact on antenna gain, Figure 6.6 shows that the shape of the radiation pattern was in agreement with previous simulations.

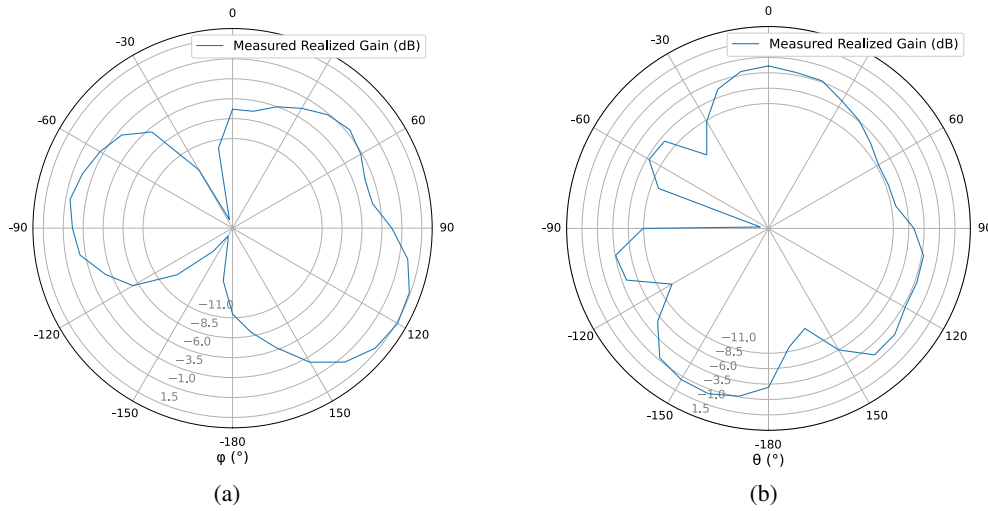


Figure 6.7: Measured radiation pattern's shape comparison for the (a) E-Plane and on the (b) H-Plane.

6.1.3 Realized Gain Measurements

The previous subsection explained why the SMA connector had too much of an impact on the antenna gain (even though it did not affect return loss as much as expected), which combined with a faulty cable on the anechoic chamber setup (that could not be replaced) made those tests useful in terms of radiation pattern shape validation but of hardly any use to evaluate the chip-fed antenna's realized gain. With this in mind, and as a way to measure the realized gain of the chip-fed antenna, a simple link budget test was conducted.

6.1.3.1 Test Setup

The test setup consisted of a *DLOS8* gateway, responsible for measuring Received Signal Strength Indicator (RSSI) and Signal-to-Noise Ratio (SNR). The half-wave sleeve dipole shown in Figure 6.8 was connected to the gateway using a cable whose loss had been previously characterized.

The gateway and the Node1 board used for this test were placed exactly 8 m apart. At this distance the widest radius of the first Fresnel ellipsoid (midway between the two antennas) is



Figure 6.8: 2.15 dBi half-wave sleeve dipole used for the LoRaWAN gateway.

just 80 cm, which is much lower than the height of the antennas. This effectively means that neither the ground nor any surrounding objects could significantly impact the test. The end node was programmed to send messages every few seconds and the gateway then reported the received RSSI and SNR to the network servers (Figure 6.10).

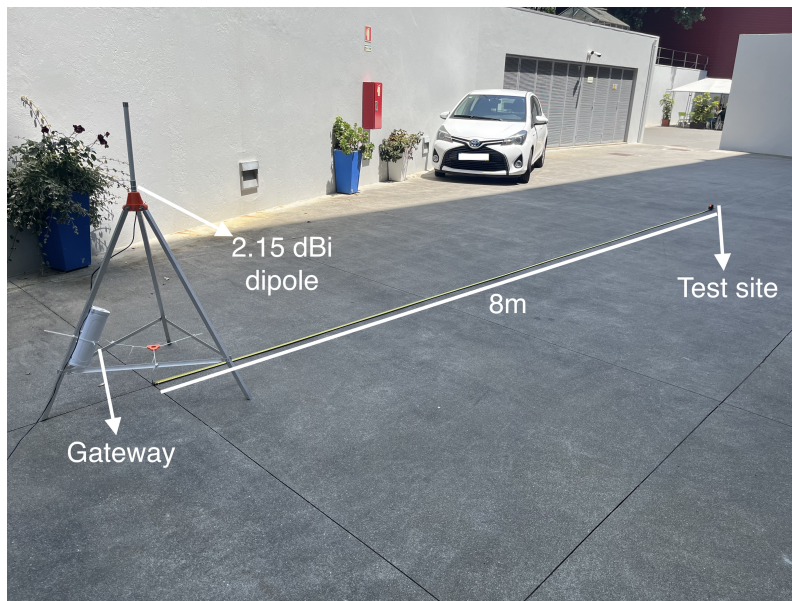


Figure 6.9: Gross gain test setup.

6.1.3.2 Results

The average RSSI for $\phi = -60^\circ$ was -31 dBm and -32 dBm for $\phi = 120^\circ$. The results of the test are shown in Equations 6.3, where G_{PIFA} and G_{dipole} represent the gain of the PIFA and of the previously mentioned dipole, respectively. L_{cable} and FSL represent the cable and free space losses, respectively, and P_{rx} and P_{tx} are the received and transmitted power, respectively. It is important to

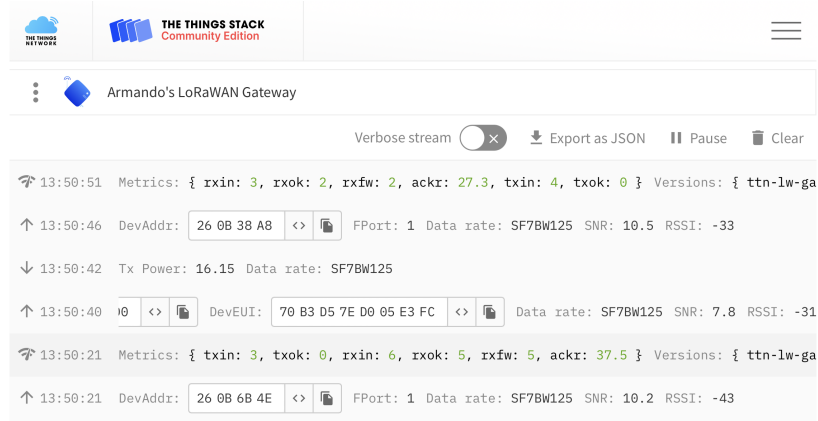


Figure 6.10: Gateway RSSI measurements.

note that the gateway measured RSSI with a precision of 1 dBm, which does not allow for a very fine measurement of realized gain.

These results do show a front-to-back ratio of 0.85 dB a realized gain close to the simulated 2 dB, validating the antenna design in agreement to previous simulations.

$$P_{TX} = P_{TX} - L_{cable} + G_{dipole} - FSL + G_{PIFA} \Leftrightarrow \quad (6.1)$$

$$P_{TX} = 14 - 0.2351 + 2.15 - 49.27 + G_{PIFA} \Leftrightarrow \quad (6.2)$$

$$-32 \geq P_{TX} \leq -31 \Rightarrow 1.51 \geq G_{PIFA} \leq 2.36 \quad [\text{dBi}] \quad (6.3)$$

6.2 Device Tests

Due to being fabricated much later in the project, the Node2 board was not used for device tests. However, the energy consumption tests described Subsection 6.2.2 are valid for both boards since the power system is exactly the same for both.

6.2.1 Long-Range Tests

Long-Range real-world tests play a crucial role in the validation of LoRaWAN devices. Even after fully characterizing an antenna in a controlled laboratory setting, there are certain aspects of radio links that are essential to assess but prove exceedingly difficult to test in such environments. For instance, a circularly polarized LoRa antenna with less gain might outperform an antenna with higher gain but with mostly linear polarization. In a real-world radio link, the received signal's polarization can be far from linear due to existing reflections and obstacle diffraction. Circularly polarized antennas, capable of receiving different polarization types, may outperform their linearly polarized counterparts with higher gain. This is one example of the multitude of factors important to LoRaWAN devices that cannot be simulated on a laboratory environment, highlighting the importance of real-world tests.

Two long-range tests were performed: one in a rural environment and another in a city. These two settings represent very common LoRaWAN applications, such as smart agriculture and smart cities. The rural test was conducted in Rio Caldo, a small village located just on the edge of Peneda-Gerês National Park in Portugal. The urban test was conducted in Aveiro, a Portuguese coastal city in Centro Region. Figure 6.11 shows the gateway placement for both tests.

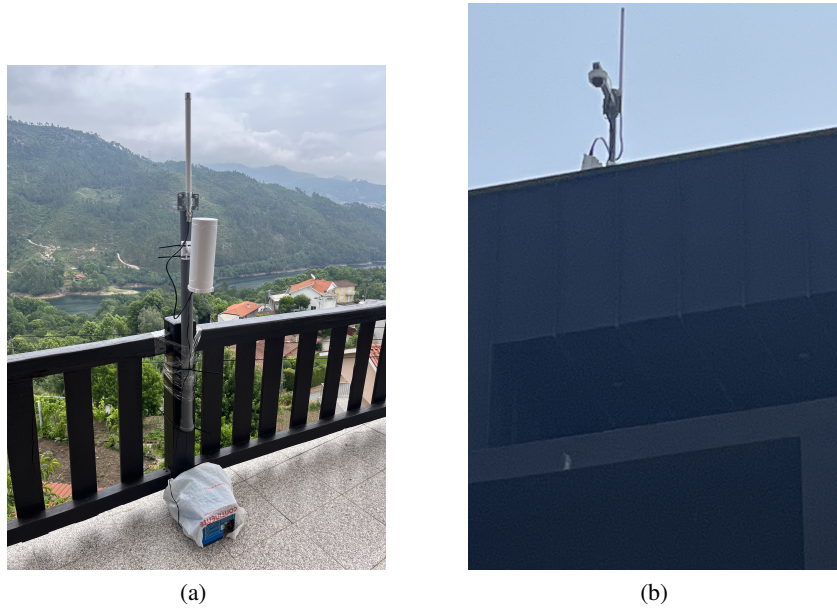
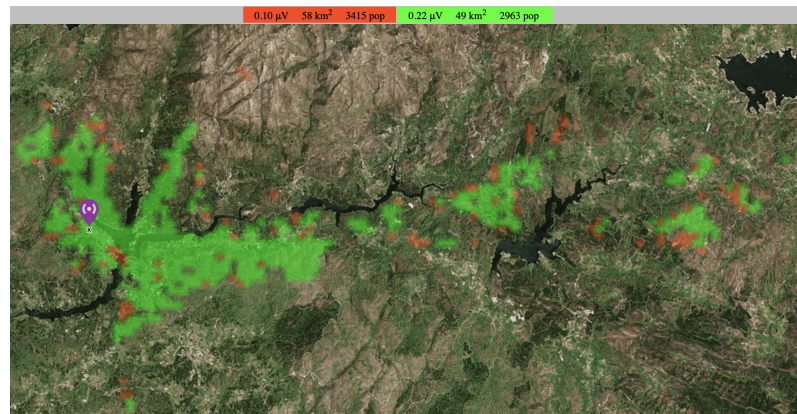


Figure 6.11: (a) *DLOS8* gateway used for the rural long range tests in Rio Caldo and (b) the *LRWCC3-MPCI* [62] gateway used for the urban long-range test in Aveiro.

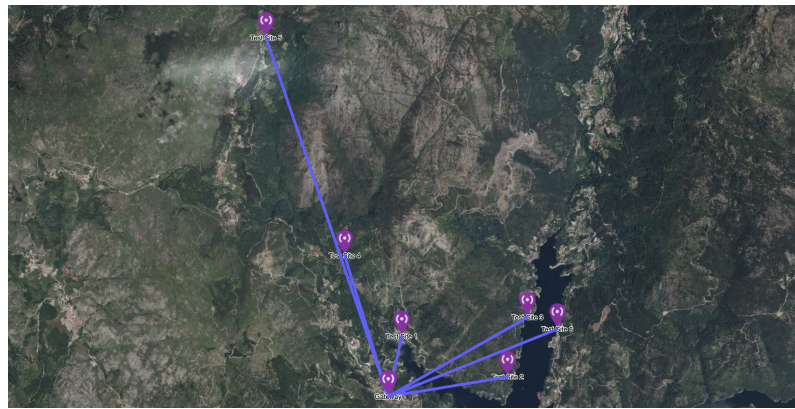
Based on the height above ground of each gateway, an RF propagation software, *Radio Mobile*, was used to simulate the estimated radio coverage of each gateway. Figures 6.12 and 6.13 depict the expected coverage and the sites used for each test. The locations of the gateways and of each test site can be found on Tables 6.2 and 6.3. For each test there was a device under test and a reference device, which are shown in Table 6.4.

Site Name	Coordinates
	(Lat.(°), Lon.(°), Elevation(m), Height(m))
Gateway	41.68437500, -8.19797000, 254.9, 2
Test Site 1	41.69119500, -8.19590000, 165.1, 2
Test Site 2	41.68660100, -8.17983400, 171.0, 2
Test Site 3	41.69335300, -8.17683000, 157.8, 2
Test Site 4	41.70036100, -8.20457700, 244.4, 2
Test Site 5	41.72504000, -8.21650000, 539.7, 2
Test Site 6	41.69201500, -8.17231900, 163.2, 2

Table 6.2: Gateway and site locations for the first long-range test (Rio Caldo).



(a)



(b)

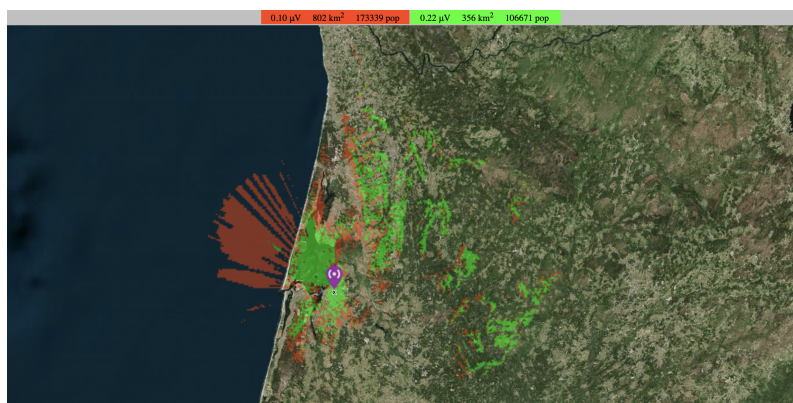
Figure 6.12: (a) Estimated coverage and (b) test sites for the first long-range test (Rio Caldo).

Site Name	Coordinates (Lat.(°), Lon.(°), Elevation, Height
Gateway	40.64210200, -8.63197800, 23.1, 11
Aveiro Site 1	40.65138400, -8.62111800, 21.9, 1.5
Aveiro Site 2	40.64789300, -8.59521400, 43.0, 1.5
Aveiro Site 3	40.65743500, -8.63603600, 5.8, 1.5
Aveiro Site 4	40.63903700, -8.64375600, 8.2, 1.5

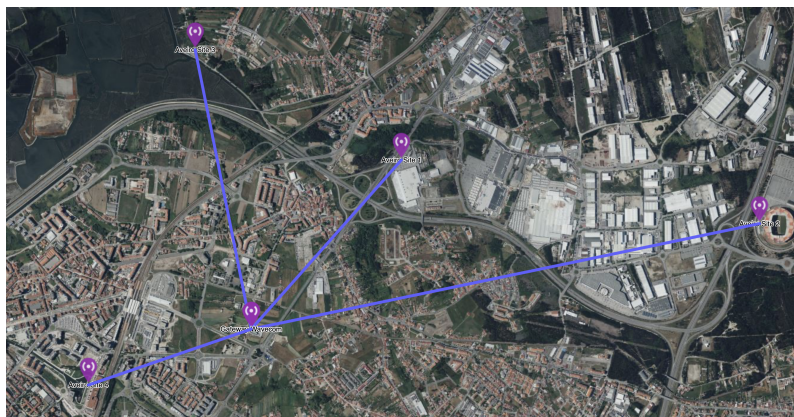
Table 6.3: Gateway and test site locations for the second long-range test.

Test Location	DUT	External Antenna	Reference	External Antenna
Rio Caldo	<i>TTGO T-Beam</i>	SMA1 Board	<i>TTGO T-Beam</i>	2 dBi rubber ducky antenna
Aveiro	Node1 board	N/A	<i>RAK10701-P Field Tester</i>	2.12 dBi antenna

Table 6.4: DUT and reference devices for each long-range test.



(a)



(b)

Figure 6.13: (a) Estimated coverage and (b) test sites for the second long-range test (Aveiro).

6.2.1.1 Results

Tables 6.6 and 6.5 present the results of both long range tests.

Site Name	RSSI (dBm)		SNR (dB)		SF	BW (kHz)	TX Power (dBm)
	DUT	Reference	DUT	Reference			
Test Site 1	-73	N/A	9.2	N/A	7	125	14
Test Site 2	-113	N/A	6	N/A	7		
Test Site 3	-108	N/A	6	N/A	8		
Test Site 4	-90	-93	10	9.8	7		
Test Site 5	-113	-106	4.2	3.8	7		
Test Site 6	-112	-110	5	4	7		

Table 6.5: Results of the first long-range test (Rio Caldo).

Site Name	RSSI		SNR		SF	BW	TX Power
	DUT	Reference	DUT	Reference			
Aveiro Site 1	-100	-109	8	6.5	7	125	7
Aveiro Site 2	-114	-116	0.8	-7			
Aveiro Site 3	-109	-117	5.2	-4.5			
Aveiro Site 4	-112	-117	0.2	-3.5			

Table 6.6: Results of the second long-range test (Aveiro).

The results of the tests conducted in Aveiro, using the Node1 board (board with chip-fed antenna), were highly promising, as the end node exhibited superior performance compared to the reference device. Together with the gain measurement test of Section 6.1.3, these results constitute a growing amount of evidence that supports the fact the PIFA developed in this project likely has a gain slightly higher than 2 dBi. On the other hand, the tests conducted with the SMA1 board, in Rio Caldo, showed comparatively poorer performance. This supports previous findings that the SMA connector likely had a significant impact on the antenna's performance in terms of the radiation pattern.

6.2.2 Energy Consumption Tests

6.2.2.1 Setup

Figure 6.14 depicts a scheme of the setup used for power consumption tests. The FTDI programmer flashes the MCU with firmware for different tasks, such as joining a LoRaWAN network, creating a Wi-Fi access point or entering deep sleep. The firmware also uses the power management system described in Section 5.2.4 to enable/disable different parts of the board. This, effectively allows the measurement of current draw for different realistic loads. A power supply is connected to the battery terminal, which also measures the device's power consumption. Finally, the test pins connected to the MCU's power pins measure its power consumption.

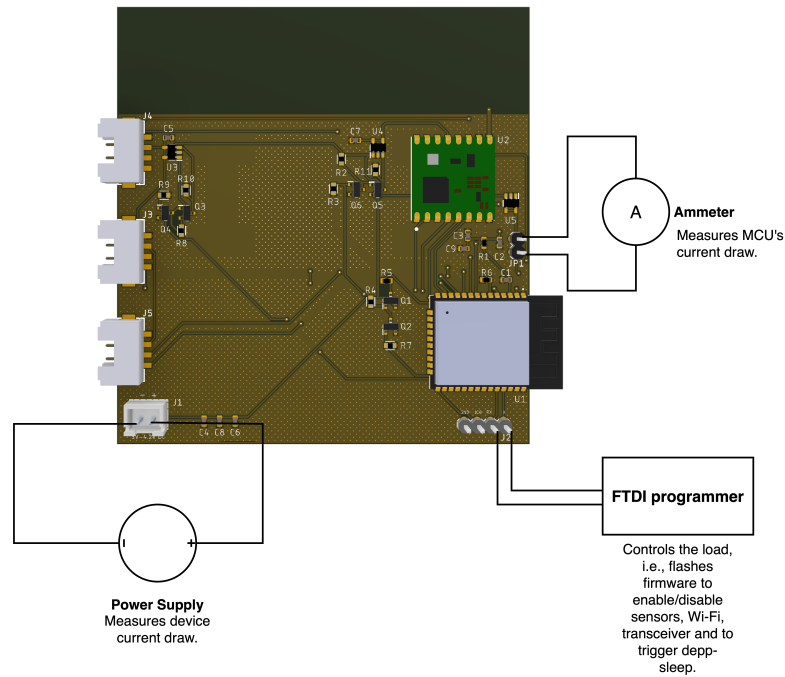


Figure 6.14: Illustration of the power consumption test setup.

The main objective of the test was to measure the power consumption of the device, and of different systems, for common tasks for a device of this kind, such as reading sensors, sending data and sleeping.

6.2.2.2 Results

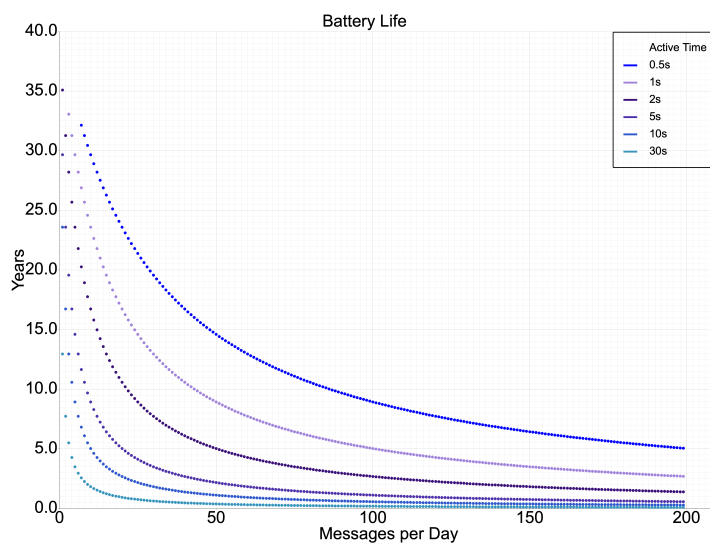
Table 6.7 presents the results obtained during the power consumption tests. All tested use-cases are layout, as well as every part of the device that is used for each use-case and the maximum and average current draw of both the device and just the MCU.

These tests highlight the low-power capabilities of the device, which effectively means that small primary LiSOC12 batteries can be used to power the end node, such as SAFT's LS17500 battery, mentioned in Subsection 5.2.4. This is desirable, as, this way, the total thickness of the board is 1.793 cm. This equates to a device thinner than the typical 3 cm helical whip antenna used in many, if not most, LoRaWAN devices. Using the Wi-Fi capabilities of the device does bring the battery close to its operating limits, but it has been shown in the previous chapter that this can be solved using another two batteries or adding one 2 μ F capacitor. There is enough space on the board for either solution without increasing the thickness of the device.

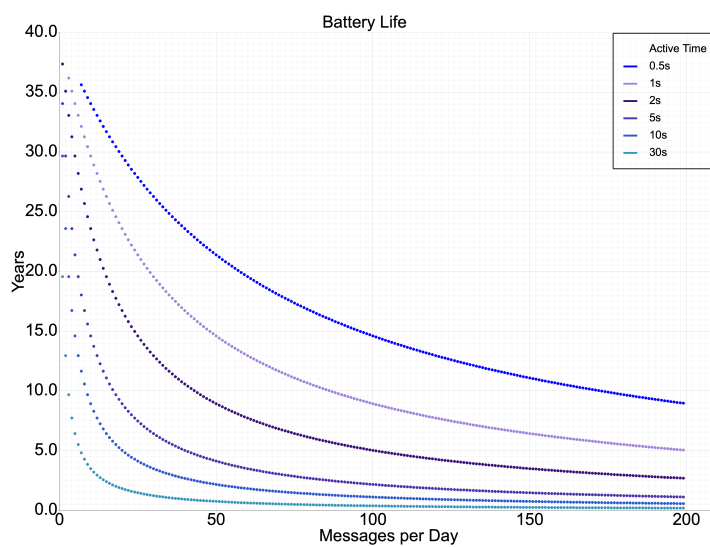
Considering the findings of this test, the battery life estimations presented in the last chapter can be updated to the much more realistic plots of Figure 6.15.

Use-Case	Configuration				Current Draw (mA)				
	Temp. Sensor/ Power Monitor	LoRa Modem	Wi-Fi Modem	Deep Sleep	CPU Freq. (MHz)	MCU Max.	MCU Avg.	Total Max.	Total Avg.
Data processing.	✗	✗	✗	✗	240	52	52	56	55
Reading sensor data.	✓	✗	✗	✗	80	29	29	30	30
					240	51	50	57	56
					80	29	29	31	31
Joining a network.	✗	✓	✗	✗	240	56	55	112	57
					80	30	30	49	30
Device configuration.	✗	✗	✓	✗	240	240	136	240	137
					80	148	110	149	111
					240	56	55	115	57
Transmitting sensor data.	✓	✓	✗	✗	80	30	30	95	31
Deep sleep period in-between transmissions.	✗	✗	✗	✓	N/A	0.0047	0.0046	0.0047	0.0046
Sensor warm-up.	✓	✗	✗	✓	N/A	500	500	0.906	0.906

Table 6.7: Results of the power consumption tests.



(a)



(b)

Figure 6.15: Estimated battery life as a function of messages per day and for different active times. (a) refers to a CPU frequency of 240 MHz and (b) 80 MHz.

Chapter 7

Conclusions and Future Work

7.1 Conclusions

This dissertation covered the successful development of a very thin, compact and low-power Lo-RaWAN end node. This was made possible by using a printed inverted-F antenna design and placing the device's electronics in the antenna's densely via stitched ground planes (technically, ground block). The proposed antenna has a total area of 67.11 cm^2 (about the size of a palm), 60 MHz bandwidth, an efficiency of 96.43% and a simulated realized gain of around 2 dBi. The end node has an estimated battery life of 10 years when spending around 80 seconds awake daily. The device has an average current draw of around 30 mA when active and of $5 \mu\text{A}$ when asleep. Additionally, it provides a battery voltage monitoring circuit. The power management system ensures sensors, communications and the MCU are independently powered and can be selectively enabled/disabled by the MCU. The end node also supports up to three external analogue or digital sensors and actuators, over the air programming and optional Wi-Fi and Bluetooth connectivity.

The research described in Chapter 4 indicates that dumbbell-shaped defected ground structures can improve the gain of PIFAs with single-layer ground planes operating on the EU863-870 band by around 0.5 dB. It was also discovered that using a ground block instead of a ground plane can be used to enhance gain by the same amount, if the antenna is bottom-fed. Realistic simulation models and real world prototypes showed that this ground block and its effects on antenna performance can be approximated by densely via stitching together the top and bottom ground planes of the board. Designs smaller than the one used in the end node were also proposed in this chapter. For instance, a PIFA with a smaller radiator-ground spacing achieved around 7% smaller area at the cost of a 0.3 dB decrease in realized gain and a 30 MHz decrease in bandwidth.

The antenna characterization presented in Chapter 6 validated the simulated design. Furthermore, long-range and power consumption tests described in the same chapter proved the low-power capabilities of the device and showed it to perform better than a reference device: a RAK10701 field tester. These tests validate the commercial viability of the device and highlight that the end node does differentiate itself from others in the market by providing long range and low power consumption, while still being a very compact device.

This work was not without some setbacks, though. Firstly, the gain-enhancing effects of DSDGSs on PIFAs with single-layer ground planes could not be replicated on PIFAs with ground blocks. Some alternative techniques described in Section 4.3.6 were implemented in an effort to circumvent this, but were not successful. It does seem that, for this frequency, this approach is likely only viable for smaller ground planes. Also, due to the lower electric field magnitude on the ground planes of PIFAs compared to Planar IFAs, where the ground plane sits directly below the radiating element, this DGSs end up having less impact on PIFAs than on Planar IFAs. Finally, the anechoic chamber characterization of the antenna did not yield precise realized gain measurements due to a faulty cable. The results were still useful to check for deformities on the radiation pattern and for shape comparison. Besides, other less precise tests, presented in 6.1.3, were able to successfully determine and validate realized gain.

7.2 Future Work

7.2.1 Production Release

The end node boards described in Chapter 5 are actually pre-release versions. There are a few changes that should be implemented for the final version of the product, such as removing development-only features (test pin, for instance) and selecting components that are mass-production-suitable in terms of logistic and the current state of the electronics market. Additionally, the board's *Grove* connectors could also be placed fully inside the board (in current versions they protrude slightly beyond the board outline) as it was confirmed during testing that cables can be attached without the need of protruding connectors. Designing the outside encapsulation of the device and compensating the antenna accordingly would also be necessary. Finally, device thickness is mainly limited by the battery that was used. As a result, further research into solutions that would provide similar performance with significantly thinner batteries could be beneficial.

7.2.2 Exploring Other Antenna Designs

This work explored most aspects of PIFAs and how to optimize them for a LoRa antenna with a great performance/size ratio. Nevertheless, there are still hundreds of different miniature antenna designs that could and should be explored.

It would be of great interest to ascertain whether sub-gigahertz patch-based designs are compatible with LoRa. Their typical external placement outside the main board often leads to increased device sizes. To address this, current material-based techniques are employed to drastically reduce the size of such patch-based antennas, compensating for their external positioning and keeping device size to a minimum. Nevertheless, these traditional material-based approaches might not be viable due to being too expensive, considering the larger size of antennas for the frequency bands LoRa operates on and the high cost of high-permeability substrates. In other words, low-cost material-based techniques, as typically employed nowadays, are only viable for higher frequency applications. That is why it would be very worthwhile to investigate if DGSs, having a much

bigger effect on planar IFAs and patches (due to increased electric field magnitude on the grounds of such antennas), could actually serve as topology-based techniques that presented such a size reduction that the antenna could be placed outside the main board without representing a significant compromise in terms of device size. In simpler terms, it could be that a hybrid approach between material-based techniques and DGSs could actually miniaturize the antenna enough to be used outside the main board.

Moreover, it would be valuable to understand if, at such low frequencies, integration of electronics directly into the radiating elements and ground planes of these antennas is actually feasible and if a departure from the current approach of having patch-based antennas separated from the main board could actually work for LoRa devices.

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