FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO

Integrated-Circuit Design of Power Management Circuit for TENG Energy Harvesting System

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Abstract

The demand for energy sustainable electronics is an ever growing trend. With the recent push of awareness towards electronic waste and energy saving, society has been looking into ways of decreasing energy and materials consumption. The semiconductor industry is no different, and this recent trend has pushed it into finding new solutions. One of the most commonly pushed solutions to fight this energy crisis is the development of power management circuits that are able to work autonomously solely relying on energy scavenged from the surrounding area, typically through the use of energy harvesting technologies.

In this work a power management integrated circuit is developed for a new energy harvesting technology known as Triboelectric Nanogenerator (TENG), a technology first proposed in 2012. A short study regarding this technology is conducted and an electrical model is developed inside the simulation environment to allow for realistic simulation results.

The developed power management circuit achieves autonomous operation relying solely on the harvested energy and provides best-effort power, based on energy availability. It operates on a low frequency of 50Hz to match the energy harvesting technology used and accepts an input voltage up to 4V. It delivers a stable output voltage of 2.7V and features a maximum efficiency of 57%. The circuit design is based on the CMOS 0.18um technology and was developed and simulated using Cadence Simulation Tools software.

Keywords: TENG, Integrated Circuit, CMOS

Resumo

A demanda por componentes eletrónicos sustentáveis em termos de energia é uma tendência cada vez maior. Com o recente impulso na consciencialização do lixo e resíduos eletrónicos e na economia de energia, a sociedade tem procurado maneiras de diminuir o consumo de energia e materiais. A indústria de semicondutores não é diferente, e essa tendência recente levou-a a encontrar novas soluções. Uma das soluções mais comuns para combater esta crise energética é o desenvolvimento de circuitos de gestão de energia que são capazes de funcionar de forma autónoma, contando apenas com a energia captada no meio ambiente que a rodeia, normalmente através do uso de tecnologias de colheita de energia.

Neste trabalho é desenvolvido um circuito integrado de gestão de energia para uma nova tecnologia de colheita de energia conhecida como Nanogerador Triboelétrico (TENG), uma tecnologia proposta pela primeira vez em 2012. Um pequeno estudo sobre essa tecnologia é realizado e um modelo equivalente elétrico é desenvolvido dentro do ambiente de simulação para que possam ser realizadas simulação com resultados minimamente realistas.

O circuito de gestão de energia desenvolvido alcança uma operação autónoma contando apenas com a energia recolhida e fornece potência com base na disponibilidade de energia. Ele opera em uma baixa frequência de 50Hz para combinar com a tecnologia de captação de energia usada e aceita uma tensão de entrada de até 4V. Oferece uma tensão de saída estável de 2,7V e apresenta uma eficiência máxima de 57%. O projeto do circuito é baseado na tecnologia CMOS 0.18μm e foi desenvolvido e simulado usando o software Cadence Simulation Tools.

Keywords: TENG, Circuito Integrado, CMOS

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Tiago Guedes

“Develop success from failures.
Discouragement and failure are two of the surest stepping stones to success.”

Dale Carnegie

Contents

Abbreviations

AC	Alternating-Current
CMEO	Cycle for maximized energy output
CMOS	Complementary Metal Oxide Semiconductor
CS	Contact-Separation
DC	Direct-Current
EHS	Energy Harvesting System
FS	Freestanding
IC	Integrated-circuit
LIB	Lithium-ion battery
MOSFET	Metal-oxide-semiconductor field effect transistor
NMOS	N-channel metal-oxide-semiconductor
LDO	Low-dropout Regulator
LIB	Lithium-ion battery
OC	Open circuit
PM	Power Management
PMOS	P-channel metal-oxide-semiconductor
PTFE	Polytetrafluoroethylene
RS	Relative-Sliding
SE	Single-electrode
SC	Short circuit
SC	Supercapacitor
SCPU	Self-charging power unit
TEG	Thermoelectric Nanogenerator
TENG	Triboelectric Nanogenerator
UVLO	Undervoltage Lockout
WEEE	Waste Electrical and Electronic Equipment

Chapter 1

Introduction

The wide advancements in technology have propelled the use of portable electronic devices into multiple areas such as personal wearable electronics [1, 2], wireless sensor networks [3] and healthcare [4]. The portability featured in these devices is extremely advantageous for diverse applications where a connection to a power grid cannot be established but it also represents the main disadvantage, as the portability comes at the cost of needing to have a supply through some kind of storage unit, which can only offer a limited range of energy.

For a long time, batteries have been the primary option to feed these systems due to their high energy density and portability, but their limited capacity and need of regular replacement does not allow for continuous supply without human intervention. When placed in remote or harsh environments batteries are not an option since maintenance becomes very costly or not possible at all. Moreover, due to the limited lifespan referred before, wasted batteries represent a considerable by-product of Waste Electrical and Electronic Equipment (WEEE), a directive that was created by the European Commission to manage the rapid growth of the waste stream created by electrical and electronic equipment. Another problem that derives from the crescent consumerism of portable electronics is the rise on energy consumption. Although these kind of electronics are generally considered low-power, the large scale in which they are being used also plays a part in the energy crisis the world is currently facing.

Therefore, to ease the growth of electronic waste caused by batteries and also support the trend of ever-growing power consumption researchers have pushed their focus towards environmentally friendly and sustainable electronics, commonly known as "green" electronics. Naturally, this demand for energy sustainable electronics is driving the semiconductor industry looking into new solutions to power the devices, or at least help charging the batteries of such devices by actively researching approaches that make use of clean energy sources.

With this in mind, energy harvesting emerged as a solution to face this energy demand in a sustainable way by scavenging energy from the surrounding environment and converting it into electrical energy. Multiple harvesting technologies have been developed to make use of the multitude of renewable energy sources that can be gathered such as mechanical, thermal or solar. It is important to note that this approach does not aim to produce power at a large scale but instead scavenge as much energy as possible during the peak times of energy availability [5]. Generally, the excess harvested energy is stored and used when the harvester fails to deliver enough power due to scarce energy availability. This method of operation is extremely promising for the portable electronics industry since it theoretically allows for infinite autonomous operation of the devices whilst enabling sustainable development, contributing to help the environment by decreasing the current reliance on batteries and making use of clean energy sources.

In order to make a viable energy harvesting system efficiency is key, since portable electronic devices usually work with energy around the mJ order. As a result, the biggest hurdle in the energy harvesting area derives from the lack of efficiency, although considerable advancements have been made. Therefore, a power management circuit is crucial to develop efficient energy harvesting systems (EHS). Due to the small nature of low power electronics, integrated circuits (IC) are often used to provide a better integration with the target system. In an effort to reduce costs, CMOS is usually the preferred technology since it features low energy consumption and inexpensive fabrication costs.

1.1 Motivation

Nowadays, renewable energy sources are being pursued more than ever before due to the acknowledged risks of an energy economy around fossil fuels (REF). Solar panel farms and wind turbines are, among other technologies, widely used for large scale energy generation and represent the upcoming energy revolution, poised to happen in the next decade.

To complement this shift towards renewable sources, powering alternatives for portable electronics are also being broadly researched to help extend battery performance or accomplish the utopical limitless autonomy, solely based on energy harvesters, since they match the low power requirements of portable devices.

Photovoltaic harvesters are among the most mature technologies since they were one of the first to appear in this area. Through the use of photovoltaic cells they are able to convert sunlight or artificial light into electrical energy but despite many advancements they still suffer from limited efficiency and are highly dependent on weather conditions [5]. Piezoelectric harvesters are another well established technology which generate electricity by gathering the vibrational energy found in the environment. They feature high output voltages and capacitances but one downside of this technology is the high cost of fabrication due to expensive materials [5].

In 2012, a technology with roots in piezoelectric harvesters was discovered and it was named triboelectric nanogenerators (TENG) [6]. TENGs use contact electrification and subsequent electrostatic induction to generate electrical energy but, in contrast to piezoelectric harvesters, it can be fabricated using cheap materials making them more accessible. This technology has been subject to intense research since its release and has proven to be very versatile so much so that in 2017 a study concluded that it was suitable for Mars exploration missions [7], achieving maximum performance in dust storms, which represent periods of high density of mechanical energy.

As stated before, power management is crucial in every harvesting technology and TENGs are no exception. Therefore, developing integrated circuits capable of extracting the maximum amount of energy of TENGs are compulsory to evolve this technology into market usable levels, with the final goal being the integration in portable electronics, making them more environmentally friendly.

1.2 Problem Characterization

Meeting the needs of low-power electronics through the means of renewable energy sources such as solar, thermal or mechanical energy is a complex task. The power management circuit for this kind of systems requires high efficiency in order to autonomously feed their applications, as the harvester is generally only able to gather low amounts of energy. This problem has been around for a long time and features a long research, but due to the rise of personal and portable electronics it has recently gained more attention.

One important aspect regarding the power management circuit is that it should suit the system's size, therefore in applications such as wireless sensor networks, it should be small to be integrated into the sensor. With this in mind, an integrated circuit (IC) solution is the ideal approach to suit every application's size requirements. Nowadays the most commonly used technology is CMOS due to low energy consumption and low cost of fabrication.

The common strategy to design a scavenging IC is to divide the problem in different parts. In the core power management unit, two circuits are essential: the AC/DC rectifier and the DC/DC converter. Apart from these, the storage unit also plays an important role in the design despite not being integrated in the power management IC since the design needs to be adapted according to the characteristics of the storage unit to be efficient. A diagram of the typical TENG energy harvesting system can be seen in Fig. 1.1.

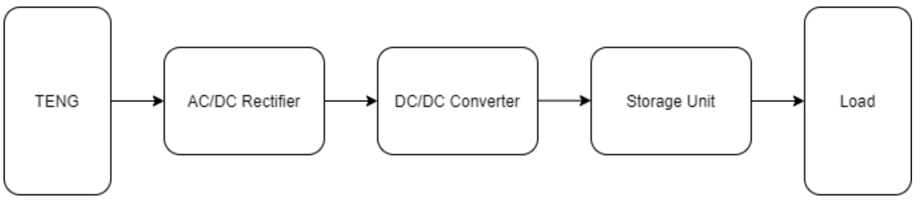


Figure 1.1: Overview of the TENG harvesting system.

1.2.1 Objectives

The present work aims to design an integrated circuit to efficiently scavenge and store energy from a chosen type of harvesting technology. The designed circuit will be used to power electronics with low-power requirements which may partly or fully subsist from the power delivered by the power management circuit. This process will involve the CMOS design of all developed circuits, validated by means of simulation. The work developed in this dissertation can be divided in the following steps.

- Literature review.
- Architecture and schematic design.
  - Rectifier sub-circuit.
  - Overvoltage protection sub-circuit
  - Regulator sub-circuit.
- Circuit simulation.
- Testing and performance review of the designed circuit through means of simulation.

Chapter 2

Literature Review

2.1 Energy Harvesting Technologies

In order to get a better overview of the state of the energy harvesting area, triboelectric nanogenerators as well as some other harvesting technologies were studied to complement and broaden the focus besides TENGs. Apart from further studying TENGs in a more complete manner, this step also helped understand how previous researchers approached this problem and what methodologies were applied in other technologies that may be useful to the development process of TENGs. It was also invaluable to understand how the energy harvesting area evolved and adapted throughout the years.
Nowadays there are multiple energy harvesting technologies available with a considerable amount of research backing them and [8] and [9] present their evolution throughout the years. Aside from TENG, the following section will present photovoltaic and piezoelectric technologies since they are two of the most popular technologies at the moment. Besides, piezoelectric were partly responsible for the appearance of TENGs, therefore it makes sense to delve further into this particular technology.

2.1.1 Photovoltaic

The photovaltic harvester was the first technology to be further studied since it is probably the most iconic regarding energy harvesting systems. Photovoltaic harvesters convert sunlight or artificial light into electrical power through the means of photovoltaic cells. This technology benefits from an energy source which can be found almost everywhere around the globe although at the same time its efficiency is largely dependant on the periods of sunlight. As stated in [5], when considering the deployment of photovoltaic EHS there are some factors that should be taken into consideration such as the period of light of the location and the weather conditions since these will affect the efficiency of the system. It also presents the various solar cell types, showing a rather low maximum efficiency of 30%. One implementation using this technology is shown in [10] where an indoor energy harvester provides a stable voltage output of around 0.40 V to 0.55 V in

the tested conditions. Another application of this technology that exemplifies how harvesting systems can be used in clothing is presented in [11] with a wearable jacket that harvests solar and thermal energy.
Although this technology has proven to be suitable for a variety of applications, it is the technology with the widest amount of research which makes it harder to find significant improvements.

2.1.2 Piezoelectric

The second technology that was examined in more detail was the piezoelectric harvesting technology where mechanical energy is converted into electricity when mechanical forces are applied on them. Their ability to detect vibrations have also made them viable for scavenging purposes [9]. Piezoelectric devices provide high output voltages and capacitances but are normally designed with expensive materials and the coupling coefficients are linked to the material properties. This technology is viable for multiple different applications such as wearable devices, where extense research has been developed. One example of this is [2] where a shoe with an embedded piezoelectric harvester is used to generate electrical power from human motion. Another interesting application of this kind of harvester is presented in [12], where this harvesting mechanism is evaluated for potential use in environments where there is significant road traffic.

2.1.3 Triboelectric Nanogenerators

Triboelectric nanogenerators or TENG convert mechanical energy into electrical energy through friction or periodic contact between different triboelectric materials and its operation is based on the conjugation of contact electrification and electrostatic induction. This is a novel technology that emerged recently, being first proposed in 2012 by Fan *et al.* [6] and has seen a growing interest in terms of research due to its potential. The following article [13] provides great insight on the current state of this technology and reviews its evolution. As stated in [14] TENG are capable of generating high output power, feature high conversion efficiency and have a low cost of fabrication.

Different studies have also been pursued to understand how TENG performance varies according to the materials that are used [13, 15], and it was shown that cost effective materials could still deliver considerable power outputs. This contrasts with piezoelectric harvesters which need expensive materials to be able to generate decent power outputs. Although this technology highlights numerous advantages, it also deals with problems such as the high voltage and low current output which represents a mismatch to the power needs of small power electronics. It also has a high matching impedance that proves incompatible with most common storage units such as capacitors or batteries.

One application of this technology is shown in [16] where TENG are seen as a promising technology for water wave energy harvesting, more commonly known as blue energy, since in contrast to electromagnetic generators they are able to work under low frequency fluctuations and stabilize its output under the condition of slow flow and random direction wave current. Another very interesting application is shown in [7] where TENGs are studied for potential deployment in Mars exploration missions since Mars features an abundance of mechanical energy and the lightweight nature of TENGs is very advantageous.

2.2 TENG Theoretical Analysis

Understanding the underlying mechanisms behind triboelectric nanogenerators is essential to design a proper scavenging IC. This technology has been previously explored and studied resulting in multiple theoretical reviews. These reviews present different TENG theoretical models which differ depending on which assumptions were made at the time of writing the electrical equations. These models provide a solid basis through which TENGs can be modelled using different equations. The TENG model presented below will be used as a theoretical point of comparison when evaluating the proposed solution practical results.

2.2.1 TENG Theoretical Model

The model used in this work as the theoretical reference relies on the assumption that the two electrodes (CS-TENG) can be seen as being infinitely larger when compared to the separating distance between them since, usually, the area of these metals is multiple orders of magnitude greater relative to their separating distance [17]. By making this assumption, the electric field in every one of the regions, being these the triboelectric layers and the air gap between them, are formulated as follows [18].

- **Air gap**

$$E_z = \frac{\sigma_I(z,t) - \sigma_c}{\varepsilon_0} \tag{2.1}$$

- **Dielectric 1**

$$E_z = \frac{\sigma_I(z,t)}{\varepsilon_1} \tag{2.2}$$

- **Dielectric 2**

$$E_z = \frac{\sigma_I(z,t)}{\varepsilon_2} \tag{2.3}$$

where E_z represents the electric field, $\sigma_I(z,t)$ stands for the density of free electrons on the surface of the electrodes which varies with respect to the gap distance $z(t)$ between the films, σ_c represents the triboelectric introduced surface charge density and ε_0, ε_1 and ε_2 represent the respective dielectric permitivities of each region.

Applying the previous equations enables the electric potential for the TENG to be devised as the following expression [18].

$$V = \sigma_I(z,t)[\frac{d_1}{\varepsilon_1} + \frac{d_2}{\varepsilon_2}] + \frac{z[\sigma_I(z,t) - \sigma_c]}{\varepsilon_0} \tag{2.4}$$

where d_1 and d_2 are the dielectric thicknesses.

When working under short-circuit condition (V=0), σ_I can be represented as

$$\sigma_{\mathrm{I}}(z,t) = \frac{z\sigma_{\mathrm{c}}}{d_1\frac{\varepsilon_0}{\varepsilon_1} + d_2\frac{\varepsilon_0}{\varepsilon_2} + z} \tag{2.5}$$

This leads the displacement current to be modelled as

$$J_{\mathrm{D}} = \frac{\partial D_z}{\partial t} = \sigma_{\mathrm{c}}\frac{\partial z}{\partial t}\frac{\frac{d_1\varepsilon_0}{\varepsilon_1} + \frac{d_2\varepsilon_0}{\varepsilon_2}}{[\frac{d_1\varepsilon_0}{\varepsilon_1} + \frac{d_2\varepsilon_0}{\varepsilon_2} + z]^2} + \frac{\partial \sigma_{\mathrm{c}}}{\partial t}\frac{z}{\frac{d_1\varepsilon_0}{\varepsilon_1} + \frac{d_2\varepsilon_0}{\varepsilon_2} + z} \tag{2.6}$$

The above equation is composed of two terms, where the first term states that the displacement current depends on the speed at which the two films make contact. The second term relates to the rate at which the surface charge density builds up and generally, after contacting for around 10 times it reaches saturation, and therefore this term vanishes [18].

When an external load is connected the transport equation is as shown in Eq. 2.7 [18].

$$\sigma_{\mathrm{I}}(z,t) = \frac{z\sigma_{\mathrm{c}}}{d_1\frac{\varepsilon_0}{\varepsilon_1} + d_2\frac{\varepsilon_0}{\varepsilon_2} + z} \tag{2.7}$$

2.2.2 Operation Modes

It is important to stress that the TENG model introduced in the previous section was based on the Contact-separation operating mode but it is not the only mode TENG systems are based on. Typically TENG support four basic operating modes based on the electrodes configuration and direction of polarization and these modes enable the possibility to design different structures and consequently develop diverse EHS for applications with the need for distinct requirements.

2.2.2.1 Contact-separation Mode

The vertical contact-separation mode consists of two films with opposite polarities facing each other in a stacked configuration. When an external force is applied to the triboelectric layers, they touch, and as a result, generate oppositely charged surfaces. Upon release, both surfaces are separated by a small distance which creates a voltage drop across the two electrodes [19]. The CS mode structure is shown below in Fig. 2.1. This mode can generate high-voltage pulse outputs while featuring simple geometries [20].

2.2.2.2 Relative-Sliding Mode

The Relative-sliding or RS mode works in a similar conversion fashion as the contact-separation mode but in the horizontal direction. Although this option may seem very attractive due to being suitable for high frequency applications, it bolsters concerns on long-term operation since the constant friction is destined to cause damage on the surfaces of the triboelectric materials [19]. Fig. 2.2 shows how this mode is structured.

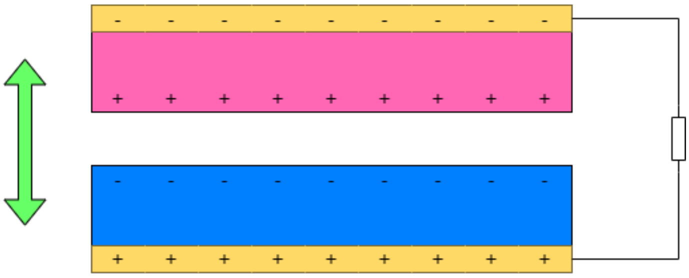


Figure 2.1: The Contact-separation mode generates power through periodic separation between the dielectric films (adapted from [21]).

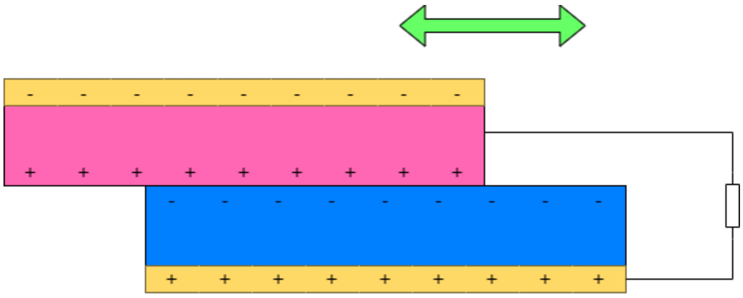


Figure 2.2: The Relative-sliding mode generates power through periodic sliding in and out of the dielectric films (adapted from [21]).

2.2.2.3 Single-electrode Mode

The single-electrode or SE mode, in contrast to the last two presented modes, works with a single electrode directly interacting with the moving triboelectric layer. This is very helpful when there are spatial constraints and simpler designs are necessary but it suffers from the electrostatic screening effect which decreases the efficiency of this mode [19]. The typical structure of this mode is shown in Fig. 2.3.

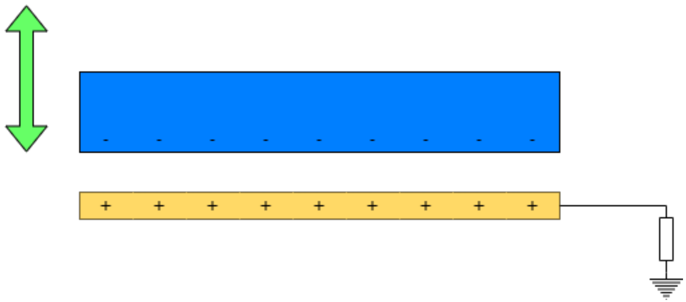


Figure 2.3: The Single-electron mode generates power through the periodic separation or sliding of the moving dielectric film (blue) on the grounded film (adapted from [21]).

2.2.2.4 Freestanding Mode

The last operation mode is called the freestanding or FS mode and resembles the RS mode but features a continuously moving triboelectric layer that alternatively approaches one of the two electrodes which causes an AC output to be generated. This operation mode is considerably more efficient than the SE mode since it does not suffer from electrostatic screening [20]. The following Fig. 2.4 shows the typical configuration of this mode.

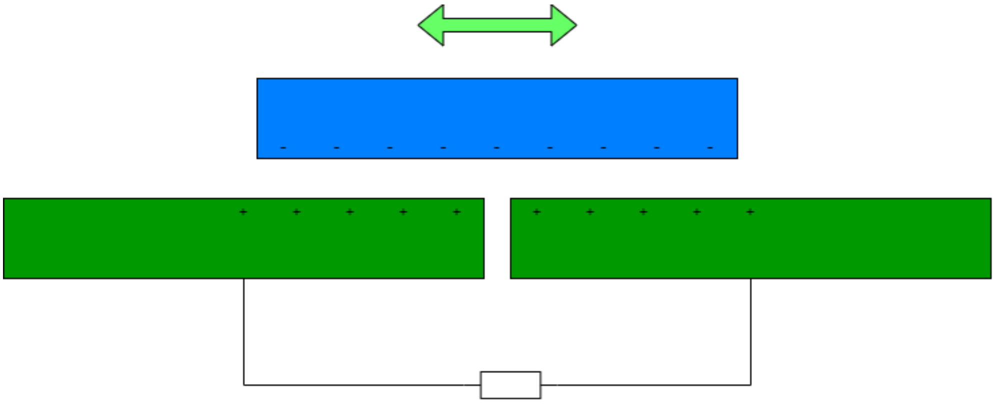


Figure 2.4: The Freestanding mode generates power through the periodic sliding of the freestanding dielectric film (blue) on the other two fixed films (adapted from [21]).

The different operation modes presented above lead to very different TENG structures and pulse outputs, therefore they are important to take into account when devising a scavenging or power management circuit.
After reviewing the different operation modes, the next step naturally came as a theoretical review of TENG output parameters to understand how they are modelled and compared through the basic output parameters. The following review helped define important output parameters that will be crucial when comparing different power management options through means of simulations.

2.2.3 Output Parameters

One final theoretical approach is needed to model the output characteristics of the TENG which consists on defining basic variables that are essential to understand what is the overall system performance and how it may be improved.
Since their first appearance in 2012 [6], TENG have seen increased interest from researchers, leading to a growth of EHS developed with this technology. This has led to further studies in the theory behind TENG and how it may be optimized for efficient energy generation [17, 22], [23]. According to [24], the following variables are generally adopted to compare different TENG performances.

- Q_{SC} **– Short-circuit charge**: output charge of the TENG in half cycle under short-circuit condition. Through this parameter we can derive the charge density σ through the following equation,

$$\sigma = \frac{Q_{SC}}{S} \tag{2.8}$$

  where **S** represents the area of the electrode.

- I_{SC} **– Short-circuit current**: charge quantity that passes through any cross section of a conductor per unit of time and it can defined through the following equation.

$$I_{SC} = \frac{dQ_t}{dt} \tag{2.9}$$

  where Q_t represents the charge transfer in the loop.

- V_{OC} **– Open-circuit voltage**: output voltage of the TENG under open-circuit condition. With this parameter in mind we can define the first governing equation that defines the total voltage difference **V** between two electrodes in any TENG, which is commonly referred as the V–Q–x relationship presented in the following equation [17].

$$V = -\frac{Q_t}{C_{TENG}(x)} + V_{OC}(x) \tag{2.10}$$

  As we can see by the above equation, this voltage difference is defined by two distinct parts. The first part, $-\frac{1}{C(x)}Q$ derives from the typical capacitor behavior where Q_t represents the already transferred charges and C_{TENG} the capacitance between the two electrodes which depends on the distance between the tribo-pair x [17]. The second part of the equation, $V_{OC}(x)$, corresponds to the open-circuit voltage presented before and relates to the polarized triboelectric charges [17].

From this equation we can easily derive the equivalent circuit which consists of an ideal voltage source and a capacitor in series, show in Fig. 2.5.

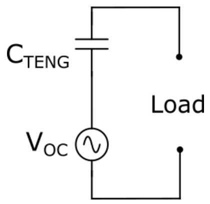


Figure 2.5: TENG equivalent circuit (adapted from [25]).

In the next subsections the resistive and capacitive load characteristics of TENGs will be presented as they are crucial to understand why a power management circuit is of significant importance to the conversion efficiency of a TENG system.

2.2.4 Resistive Load Characteristics

When TENGs are connected with a resistive load, we get the equivalent circuit already seen in Fig. 2.5, where the load circuit is a resistive load, and using Kirchhoff's law we obtain the following equation.

$$R\frac{dQ}{dT} = -\frac{1}{C}Q + V_{OC} \tag{2.11}$$

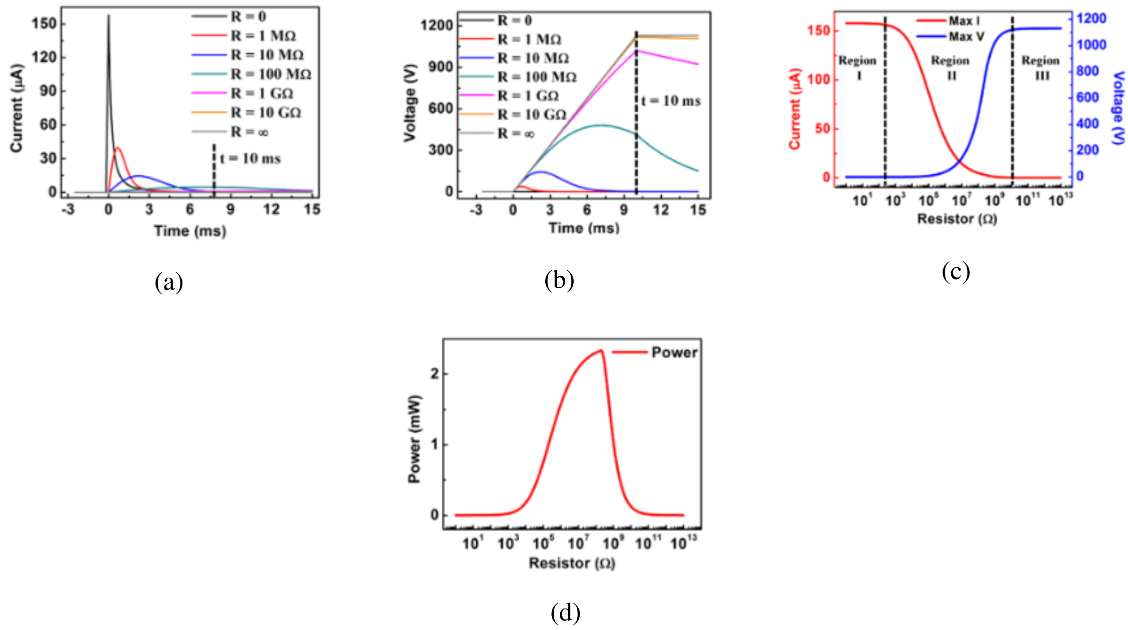


Figure 2.6: TENG resistive output characteristics. (a) Real-time current–time relationship at different load resistances. (b) Real-time voltage–time relationship at different load resistances. (c) The influence of the load resistance on the magnitude of the output current and voltage. (d) The influence of the load resistance on the instantaneous power output (reproduced from [17]).

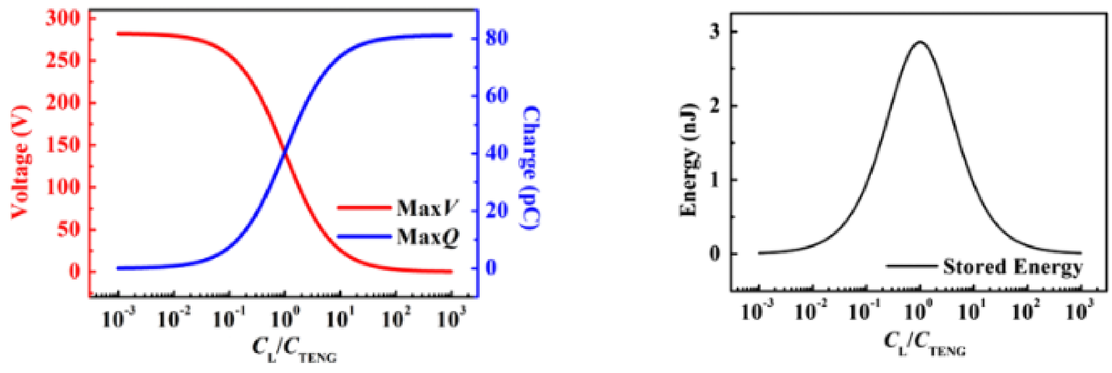
This is obtained through a first order derivative and will help to define the working regions presented here. According to [22] TENGs can be divided into three working regions defined according to their respective resistance values. How each region affects the respective voltage and current can be seen more explicitly in Fig. 2.6. The three working regions are defined in more detail below.

1. The first region is characterized by small load resistance values ranging from 1 – 1000 Ω where the peak current has a little drop compared to the SC (short-circuit) condition, and the maximum voltage is approximately proportional to the external resistance [17].

2. The second region is characterized by load resistance values ranging from 1000 Ω – 1 GΩ where the maximum current suffers a huge drop but the maximum voltage increases at a reverse trend [17].

3. The third region is characterized by load resistance values higher than 1 GΩ and the output characteristics in this region are close to the OC (open-circuit) condition in which the maximum voltage saturates at V_{OC} [17].

The optimum resistance value for maximum instantaneous power is key to maximize the effective efficiency of the TENG system. This value needs to be studied in a continuous way since it varies with the TENG structure and its operational conditions [17].



(a) (b)

Figure 2.7: TENG charging characteristics under unidirectional mechanical motion. (a) The influence of the load capacitance on the final voltage and charge stored in the load capacitor. (b) Final stored energy profile with load capacitance (reproduced from [17]).

2.2.5 Capacitive Load Characteristics

In this section the capacitive load characteristics are seen in more detail. The equivalent circuit consists of the TENG in series with a capacitive load. If we define x as the distance between the tribo-pair, $\mathrm{Q_O}$ as the transferred charges between the electrodes, $\mathrm{Q_C}$ as the charges on the top plate of the load capacitor and $\mathrm{C_L}$ and $\mathrm{C_T}$ as the load capacitance and inherent capacitance of the TENG, we can define the following equations [26].

$$\mathrm{V}(x = \mathrm{x_{max}}) = \frac{\mathrm{C_T V_{OC,max}}}{\mathrm{C_L + C_T}} = \frac{\mathrm{Q_{SC,max}}}{\mathrm{C_L + C_T}} \tag{2.12}$$

$$\mathrm{Q_C}(x = \mathrm{x_{max}}) = \frac{\mathrm{C_L Q_{SC,max}}}{\mathrm{C_L + C_T}} \tag{2.13}$$

Equation 2.12 and 2.13 represent the final voltage and the final charge on the capacitor, respectively, when the maximum distance $\mathrm{x_{max}}$ between the layers is reached where $Q_{SC,max}$ stands for short circuit transferred charges and $\mathrm{V_{OC,max}}$ for open circuit voltage. From [17] the total energy stored in the capacitor $\mathrm{E^C}$ is given as

$$\mathrm{E_C} = \frac{1}{2}\mathrm{C_L}[\mathrm{V}(x = \mathrm{x_{max}})]^2 = \frac{\mathrm{C_L}[\mathrm{Q_{SC}}(x = \mathrm{x_{max}})]^2}{2(\mathrm{C_L + C_T})^2} \tag{2.14}$$

In Fig. 2.7, the relation between the load capacitance and the final voltage and charge stored in the load capacitor can be observed in (a) and the final energy stored in (b).

It is important to note that the equations obtained above are simplified since they only stand for unidirectional motion, which is certainly not true for pratical applications of TENGs, who generate AC currents due to their back and forth movement, although they help understand how the capacitive characteristics influence the output voltage and current. Therefore a rectifier is needed to stop the charge leaking back from C_L to the TENG. Also, the inherent capacitance of TENGs is normally time-variant [17].

2.3 TENG Power Management

In the previous section the basic output characteristics of the TENG were defined with the intent of being able to quantitatively compare the different alternatives in the power management circuit and the capacitive and resistive characteristics helped understanding how the system performs under certain loads. Although TENG are seen as a promising technology in the energy harvesting area, boasting multiple advantages such as large power density, simple structures and a wide range of inexpensive fabrication materials [6], they still face serious challenges such as high matched impedance and high voltage output to be considered viable. With this in mind came the need to design a power management circuit to help maximize the TENG conversion efficiency and the delivered power to the external circuitry.

In this section the power management circuit was dissected into two parts: the rectifier and the DC/DC converter. Despite not being part of the power management IC, the storage unit is also highly influential on the design, therefore it was important to explore it alongside the rest of the power management parts. The block diagram in Fig. 2.8 represents the interaction between the TENG, power management circuit and the load. The integration of these three circuits shape the energy harvesting system, so in order to maximize the circuit efficiency, several simulations will need to be executed along the way to find the ideal design.

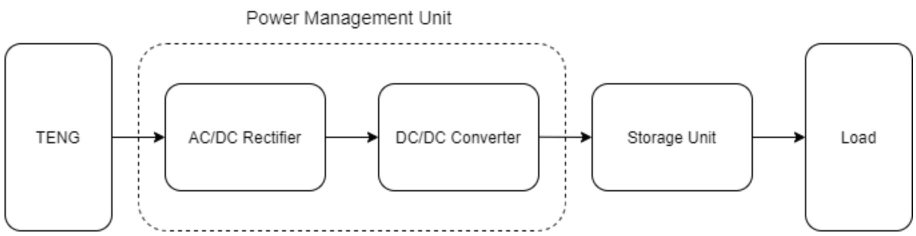


Figure 2.8: Block diagram of the complete EHS.

Due to the randomness of mechanical forces and their intrinsic capacitive behavior, TENG outputs are pulsed AC signals with variable frequency [17]. This is a common problem among various energy harvesting technologies but unlike other technologies TENG are able to reach high efficiencies at low frequencies. The first sub-circuit to be reviewed is the AC/DC rectifier.

2.3.1 AC/DC Rectifier

In order to convert the AC current coming from the TENG to DC, deciding upon which rectifier circuit to use is the first step required for the IC design process. Most power management circuits developed for pratical application of TENGs rely on full wave rectifiers since they are a simple solution. These kind of rectifiers rely on 4 diodes in a closed loop configuration as we can see in Fig. 2.9, which take turns in pairs to rectify the AC input coming from the TENG.

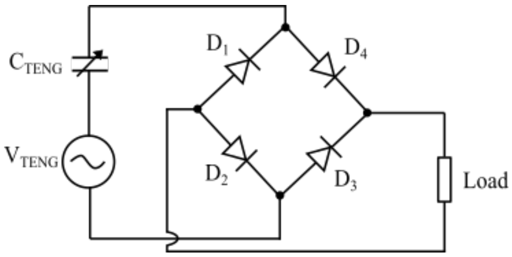


Figure 2.9: Full wave bridge rectifier schematic.

Although this solution works for simple systems who do not care much for efficiency, it is not ideal for high performance systems who need to save as much energy as possible. This happens because there is an impedance mismatch between the TENG and the rectifier bridge which causes considerable energy to be lost during the rectification process [27].
Another rectifier circuit is the half wave bridge rectifier. Contrary to common knowledge, this rectifier circuit actually delivers a higher amount of energy per cycle to a capacitive load compared to the full wave rectifier. This was shown by [28], where they tested and compared both circuits measuring 62 nJ of energy in the 101^{st} cycle to 21 nJ of the full wave rectifier. It should be noted this only applies to TENG operation modes that feature variable capacitance such as CS and RS mode.

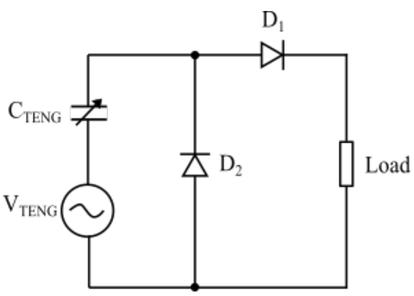


Figure 2.10: Half wave bridge rectifier schematic.

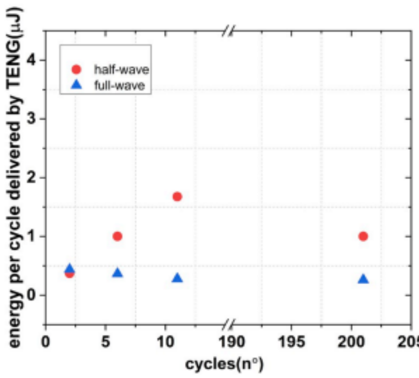


Figure 2.11: Comparison of calculated energy per cycle delivered by the TENG for the 2^{nd}, 6^{th}, 11^{th} and 201^{st} cycles of operation (reproduced from [28]).

Lastly, a novel rectifier circuit is presented in [29] which is called the Bennet doubler. In figure 2.13 the comparison between the half wave rectifier and the Bennet doubler is shown in terms of harvested power and it is clear that Bennet doubler is superior in orders of magnitude since it extracts approximately 23 µW to the 138 nW of the half wave rectifier, in the point where the maximum power is converted. This increase happens due to the self-increase of the triboelectric charge generated at each contact [29].

Generally TENG are characterized by their high output voltages in the hundreds of volts and

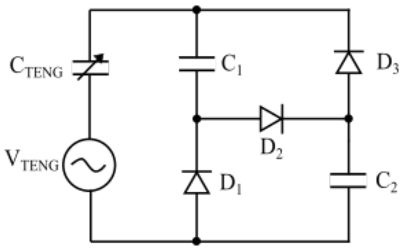


Figure 2.12: Bennet doubler schematic (adapted from [29]).

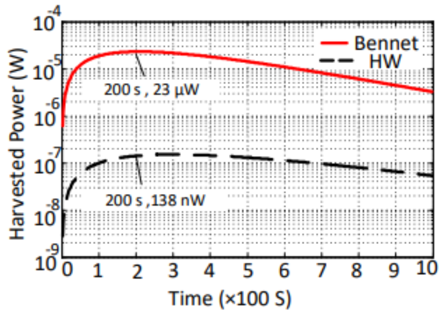


Figure 2.13: Comparison of the harvested power between the half-wave and the Bennet rectifier (reproduced from [29]).

low output current in the order of µA, which is incompatible with the current day electronic standards. Therefore, after rectifying the AC pulses generated by the TENG surges the need to design a buck converter circuit that lowers the voltage and increases the current.

2.3.2 DC/DC Converter

Although we could directly store the harvested energy by the TENG after the rectification process, this approach has shown poor results due to the impedance mismatch between the TENG, which have high impedances, and the respective storage elements such as capacitors or batteries, which are characterized by their low impedances [30]. Therefore a regulator circuit is essential to achieve high efficiencies. Three different approaches will be presented: inductive transformers, capacitive transformers and conversion based on active switches.

2.3.2.1 Inductive Transformers

Inductive transformers are a very common option to lower the output voltage of TENG and feature in several previous works [31, 32]. In 2014, Zhu *et al.* proposed a circuit composed of a inductive transformer, rectifier, voltage regulator and capacitors. They reported that this power management circuit enabled the system to output a constant DC voltage of 5 V in less than 0.5 s after the TENG started working. Fig. 2.14 represents the proposed circuit. It is important to refer that the circuits that will be presented in this chapter are not in CMOS technology since power management for TENG systems is still underdeveloped in IC technology.

The transformer shown in Fig. 2.14 boosts the output current at the expense of lowering the output voltage, which is helpful due to the general high voltages of TENGs, and substantially reduces the output impedance of the TENG [31]. The authors revealed that this power management system is able to serve two purposes: either provide a constant DC voltage to drive commercial electronics or serve as a charging source for recharging batteries. Another effective usage of this transformer consists in using it to lower the large impedance of TENG by changing the coil ratio [32]. When using the inductive transformer as a voltage and current regulator it lowers the voltage and boosts the current while also lowering the matched impedance. Although this

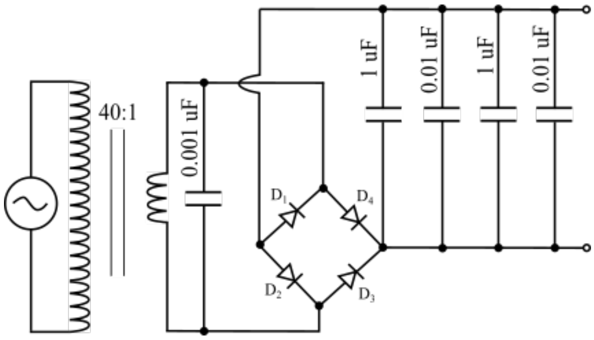


Figure 2.14: Circuit diagram of the complete power-supplying system that consists of a triboelectric generator and a power management circuit (adapted from [31]).

transformer features many advantages it is only efficient when applied to rotary-shaped TENG due to their frequency needs.

2.3.2.2 Capacitive Transformers

Differently from the inductive transformers, capacitive transformers can be used at variable frequencies. A circuit that employed this kind of transformer is shown in [26] with an array of self-connection-switching capacitors.

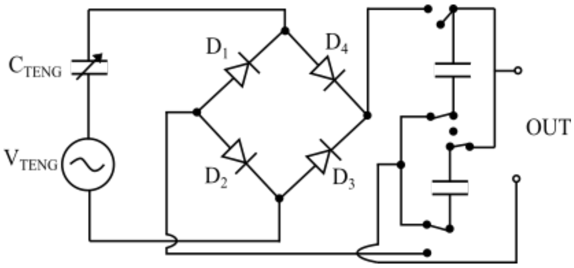


Figure 2.15: Equivalent circuit diagram (adapted from [26]).

By integrating a CS mode TENG with an array of self-connection-switching capacitors that are connected in series when being charged and in parallel when discharging, they built a system capable of rectifying and transforming the output from the TENG. It is also possible to tune the output voltage and the output current and charges can be increased per applied load [26]. They devised the following equations for the output charges and voltage,

$$Q_{out} = NQ_0 \tag{2.15}$$

$$V_{out} = \frac{V_0}{N} \tag{2.16}$$

where Q_0 and V_0 represent the total generated charge voltage and charges in the serial capacitors while N is defined as the number of capacitors in the circuit.

2.3.3 Power conversion based on active switches

In order to improve the universality of the power management circuits Niu *et al.* proposed the following charging strategy for maximized energy efficiency [33].

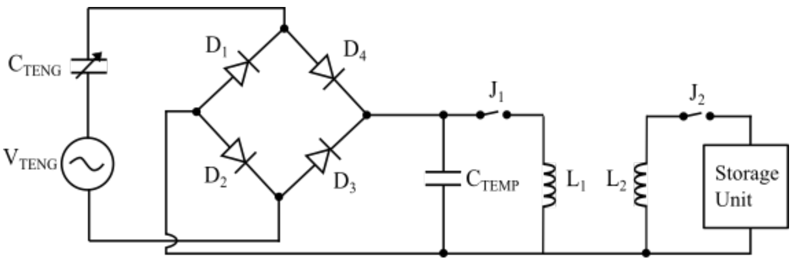


Figure 2.16: Equivalent circuit diagram (adapted from [26]).

This circuit worked in two stages. At first it charges a temporary capacitor C_{TEMP} through a full wave bridge rectifier and in the second stage it transfers the same energy from the temporary capacitor to the final energy storage unit. The circuit starts with both switches off to minimize the interference with the charging of the temporary capacitor. After C_{TEMP} reaches its max value, switch J_1 closes and the process of transferring the energy from the capacitor to L_1 starts. When this process is finished J_1 opens and J_2 closes which ignites the transferal of energy from L_1 to L_2 and finally to the storage unit. To minimize the energy loss in the transferal from the capacitor to the final storage unit, two switches and a coupled inductor are used in the second stage [33]. This work registered a total efficiency of 59.8%.

A simplified method was proposed where a different two step strategy is adopted with the focus being on the efficiency of each step. The steps consist in (1) maximize the output energy of a TENG by using built-up voltage V–Q plot and (2) maximize the transferred energy from TENG to the final storage unit by employing a LC oscillation model.

All three studied approaches that are currently the most employed in TENG for DC/DC conversion have been presented and Table 2.1 summarizes and compares each method through their advantages and disadvantages as well as their efficiency levels.

Method	Efficiency (%)	Advantages	Disadvantages
Inductive Transformer	1.2 - 72.4	Without switches Simple structure	Not suited for pulse output
Capacitive Tranformer	25	Suitable for pulse output	Increased complexity with voltage drop ratio
Active Switch	59.8 - 75.5	Suitable for pulse and uniform output High efficiency	Active switch controlled by external logic circuit

Table 2.1: Summary of DC/DC conversion methods ([33], [26]).

2.3.3.1 Energy Storage

The power management design is dependent on the type of energy storage since using supercapacitors or lithium-ion batteries imply different design approaches due to their intrinsic characteristics. The last step in designing an energy harvesting system consists in saving the generated energy with minimal losses. This is a really important step since the system needs to be able to store that energy in case the application is not needing it or there is surplus energy. Obviously this feature is invaluable to a system that is to be considered everlasting since this storage unit provides energy for periods of time where the TENG is not under mechanical motion therefore not being able to generate energy. This section presents the current options for energy storage which are batteries, through constant recharging, and supercapacitors.

2.3.3.2 Batteries

The first option that was further explored were batteries since they are currently the most used storage unit for portable electronics worldwide. This approach focuses on recharging batteries autonomously extending their lifetime. One of the first integrations of batteries with TENG resulted in a SCPU (self-charging power unit) in [34] where a TENG EHS is developed with a Li-ion battery (LIB) as storage unit. In this work, the TENG harvests the mechanical motions and after rectification charges the LIB which simultaneously driving the external load. They called this "sustainable mode". In this case the battery could be fully charged in 11h and provided a continuous and stable DC current of 11 µA and 1.55 V with continuous mechanical motions. This makes the battery work not only as a storage unit but also as a power regulator. This approach does not resolve the rising need of batteries but helps slowing down the time between batteries replacement.

2.3.3.3 Supercapacitor

Another very common option to store energy is the supercapacitor. This method of storing energy needs to be carefully planned since its integration with TENG EHS needs careful attention. A good example where supercapacitors fit well into systems is in wearable electronics since fabric, which people use every day, can be used in this approach. Supercapacitors require the substrate to be lightweight and flexible. In [35] an ultralight cut-paper based self-charging power unit that is capable of simultaneously harvesting and storing energy by combining cut-paper based TENG and a paper-based SC. By using a suitable capacitance of approximately 1 µF the supercapacitor took 250 s to be fully charged.

2.3.4 Power Management Review

After reviewing the multiple phases involved in the design of a power management circuit, it was easy to understand why the power management module is essential to any viable EHS that is to be deployed in a continuous and autonomous way. The different sub-circuits provide invaluable enhancements that boost the overall system efficiency and allow the connected load to be supplied with a stable output (that still depends on energy availability).

Chapter 3

TENG Electrical Model

The theory studied in the previous section was very important to get a general overview of how TENGs work and how their performance can be enhanced. To be able to progress in the harvesting system design the next crucial step came as the electrical modelling of a contact-separation TENG to allow for a realistic performance assessment of the harvesting system inside the simulation environment.

To design a TENG model with a realistic behaviour, relying solely on theoretical results is not advisable. Therefore, two different TENG prototypes were tested to get practical results and complement the results obtained in the theoretical analysis. These TENG prototypes were already fabricated and developed by colleagues in FCUP (Faculdade de Ciências da Universidade do Porto) but the results were obtained together within their testing facilities. Both TENGs are contact-separation TENGs and are PTFE-based since it is one of the most commonly used materials for the electron withdrawing part of the TENGs.

The goal is to develop a simplified electrical model that can replace the physical model and does not present any convergence issues when running in the simulation environment. This model should capture both the same power profile as well as the load performance of the physical TENG, i.e., have the same optimal load value and identical voltage and current waveforms.

3.1 TENG Prototypes

The first TENG was fabricated using a PTFE (Polytetrafluoroethylene) film as the negative triboelectric material and Nylon66 as the positive triboelectric material while the second prototype kept the PTFE film and used FEP (fluorinated ethylene propylene) as the tribopositive material. As shown in Fig. 3.1, the structure of these TENGs is kept simple and is composed of two cover slips that support the respective materials, two electrodes based on thin copper films and the PTFE and Nylon/FEP films.

The materials used in this TENG prototype were commercially obtained according to their triboelectric properties and therefore they have inherent physical properties detailed in their respective datasheets. A summary of the physical properties that hold the most weight when designing

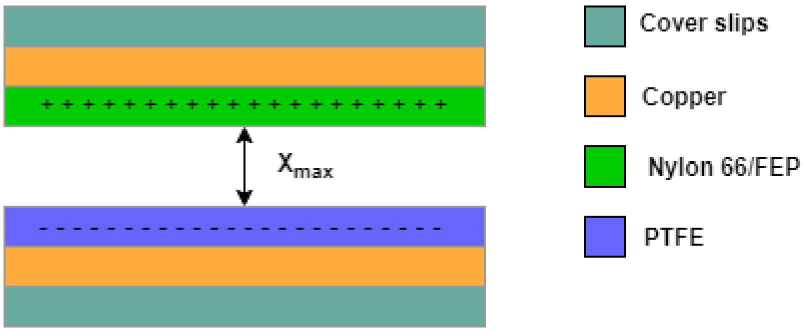


Figure 3.1: Structure of the PTFE/Nylon 66 TENG.

these TENGs are displayed in the following Tables.

Parameter	Value	
Dielectric Width (w)	0.05 m	
Dielectric Length (l)	0.1 m	
Maximum Separation Distance (x_{max})	0.003 m	
	PTFE	Nylon 66
Relative Permittivity (ε_r)	2.1	3.4
Dielectric Thickness (d)	0.05 mm	0.017 mm
Effective Dielectric Thickness (d_0)	28.8 μm	

Table 3.1: Parameters of the PTFE/Nylon 66 TENG prototype.

Parameter	Value	
Dielectric Width (w)	0.025 m	
Dielectric Length (l)	0.025 m	
Maximum Separation Distance (x_{max})	0.026 m	
	PTFE	FEP
Relative Permittivity (ε_r)	2.1	2.1
Dielectric Thickness (d)	0.05 mm	0.05 mm
Effective Dielectric Thickness (d_0)	47.6 μm	

Table 3.2: Parameters of the PTFE/FEP TENG prototype.

3.1.1 Test Setup

To simulate the movement applied to the TENG, a pneumatic linear motor was used to change the separation distance between the films. The motor described a simple harmonic motion and was connected to the electronegative layer (PTFE) while the other layer remained fixed. An electrometer was connected to the TENG and the values were obtained using a computer which was in turn connected to the electrometer. The experimental setup is displayed in Fig. 3.2 and a block diagram of this setup is shown subsequently.

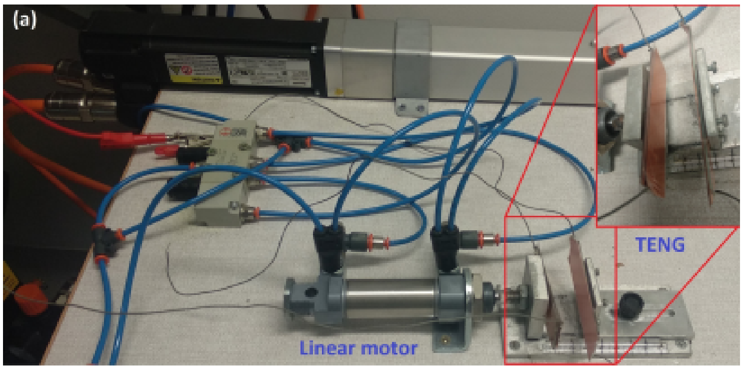


Figure 3.2: Photograph of the experimental setup.

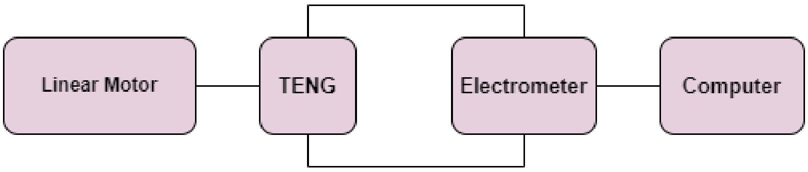


Figure 3.3: Block diagram of the experimental setup.

The electrometer is suitable for these kind of measurements as it can read voltages of up to 200 V and bolsters a very high input impedance (~$10^{14}\Omega$). Due to the very high value of input impedance of the electrometer, the circuit can be considered to be in open-circuit. Moreover, the electrometer also allows charge and current measurement by mimicking a short-circuit configuration.

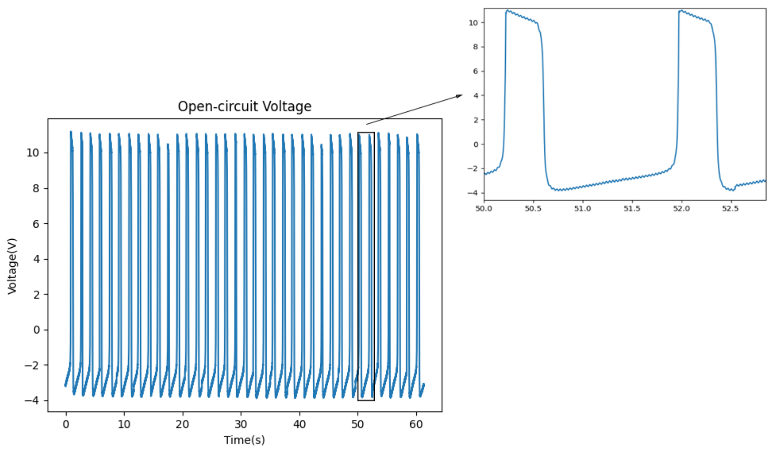
To obtain results on voltage and charge values different circuit configurations needed to be used. The configuration for open-circuit voltage is as shown in Fig. 3.4a, while the configuration for charge measurement is as shown in Fig. 3.4b. The only difference between the schematics below and the real setups reside in the absence of a load (the electrometer is seen as the load).

(a) (b)

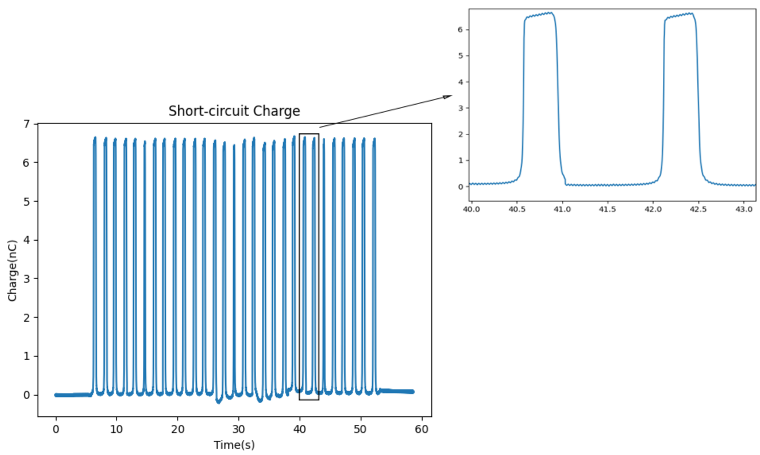
Figure 3.4: Circuit configuration for: (a) voltage laboratory measurement (b) current laboratory measurement.

3.1.2 Test Results

The first metrics obtained were the open-circuit voltage and short-circuit charge which are normally among the first metrics to be described when characterizing the output of a TENG. The data for each test was captured within a timespace of 1 minute. The pneumatic motor frequency was approximately 1Hz and the pressure took a value of 40 psi. The resulting plots can be observed in Fig. 3.5. To avoid cluttering too much plots and since the results were fairly similar between the two TENGs, only the results for the PTFE/FEP will be displayed for each test.



(a) Open-circuit voltage.



(b) Short-circuit charge.

Figure 3.5: Output characterization of the PTFE/FEP TENG: (a) Open-circuit voltage (b) Short-circuit charge.

The resulting waveform is asymmetrical which is common among TENGs and the wave shape comes down to the nature of the movement applied by the linear motor.

Afterwards, to get a general grasp of the voltage dependence on the load resistance, different load values were tested while maintaining the previous test conditions. As expected, by increasing the load resistance the only change was the increase of the peak voltage. The reverse behaviour was observed for the charge (and current). The resulting waveforms for the PTFE/FEP TENG prototype can be seen in Fig. 3.7.

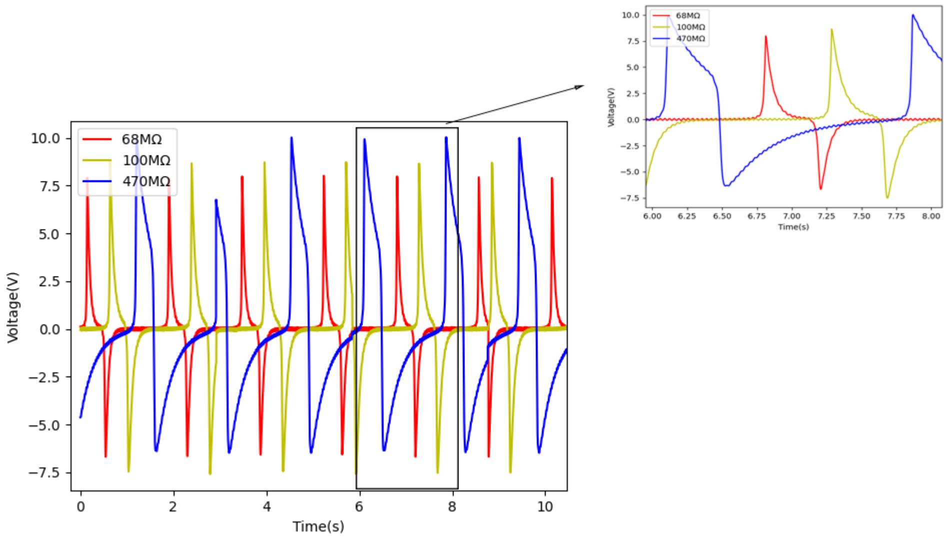


Figure 3.6: Output voltage for different load resistance values.

As expected, increasing load resistance values increases the voltage peaks but obviously has the reverse effect on the output current.

To finish the characterization of the TENGs, a load resistance sweep was performed to understand what load value maximizes output power since this is the major point of interest for the design of the energy harvesting system. The peak output voltage, peak current and power are summarized in the following plot.

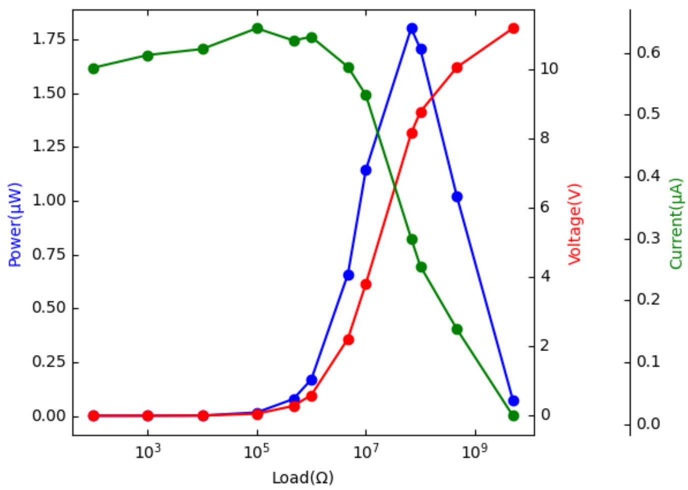


Figure 3.7: Output characteristics of the PTFE/FEP TENG.

For the PTFE/FEP prototype the maximum output power is ~1.75 µW obtained for a load value of approximately $10^8\Omega$. If the power management circuit were to be designed for this specific TENG, the load should be kept at this load value at all times to improve the overall efficiency of the system.

3.2 TENG Model Cell

After finishing collecting data on the fabricated TENG prototypes, it was time to move on to the simulation environment where the energy harvesting system will be built and evaluated. The data displayed in the previous section regarding the open-circuit voltage and short-circuit current is of significant importance since it gives a point of comparison when designing the TENG cell inside the simulation environment. Having a TENG model cell that matches (as much as possible) the voltage and current waves of the real TENGs obviously improves the accuracy when doing the performance assessment of the energy harvesting system. The first TENG model cell was written in Verilog-A to try and reflect the equations explored in the theory presented before. Listing 3.1 exhibits the Verilog-A code for this model.

```
// VerilogA for RESEARCH, teng_csmode_model_cell, veriloga

`include "constants.vams"
`include "disciplines.vams"

module teng_csmode_model_cell(VA, VB, x);

output VA, VB; input x;
electrical VA, VB, x;

// Capacitive Model (V-Q-x)
parameter real width=0.025 from (0:inf);      // width (m)
parameter real length=0.040 from (0:inf);   // length (m)
parameter sigma_s=5u from (0:inf);             // surface charge density (C/m^2)
parameter er1=2.75 from (0:inf);              // relative electric permittivity 1
parameter er2=4 from (0:inf);                    // relative electric permittivity 2
parameter d1=100u from (0:inf);             // thickness 1  //100u
parameter d2=100u from (-inf:inf);        // thickness 2   //100u
parameter real Q0=0 from (-inf:inf);        // initial charge on the capacitor

real VOC; // open-circuit voltage
real C;   // capacitance
real d0; // effective dielectric
real area; // area of each contact plate

analog begin
  d0 = (d1/er1)+ (d2/er2);
  area = width*length;
```

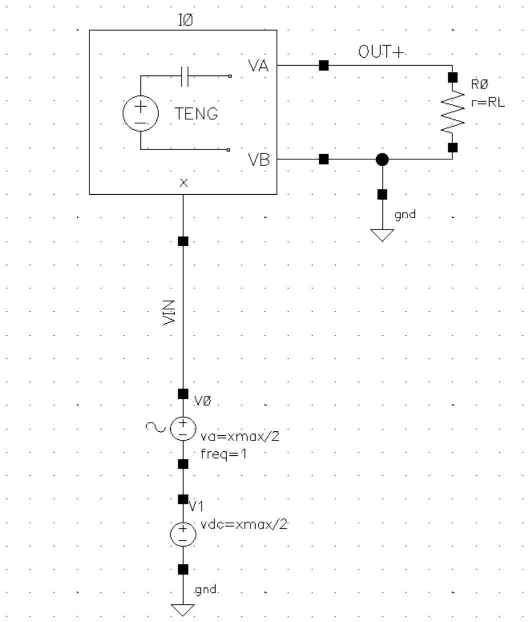
```
  VOC = sigma_s*V(x)/(`P_EPS0);
  C = (`P_EPS0)*area/(d0 + V(x));
  // output voltage:
  if (analysis("ic"))
    V(VA,VB) <+ Q0*C; // superposition
  else
    V(VA,VB) <+ idt(I(VA,VB),0)/C;
  V(VA,VB) <+ VOC; // superposition
end

endmodule
```

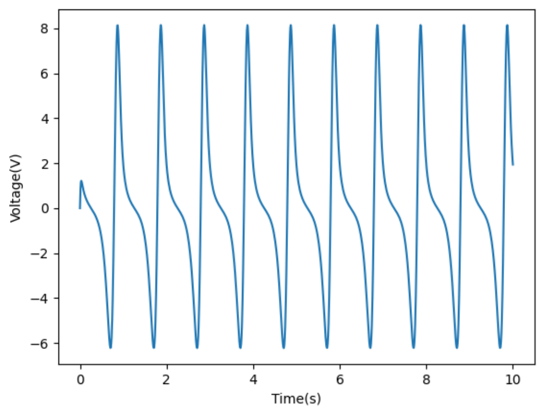
Listing 3.1: TENG model cell written in Verilog-A.

This cell, just like a real TENG, needs a movement stimulus to generate energy. This is accomplished through an input which takes the separation distance at any time. This cell also needs to be adjusted according to the kind of TENG that the user wants to mimic during simulation. To achieve this, a set of input parameters, just like the ones shown before when describing the fabricated TENGs (Tables 3.1 and 3.2), can be tweaked to try and match the practical results when instantiating the cell.

To test the output characteristics of the TENG model, an harmonic type of movement was applied to the TENG and a load resistance of 1G was connected to the output of the cell. The figures 3.8a and 3.8b show the circuit configuration and the transient output voltage for this harmonic input, respectively.



(a)



(b)

Figure 3.8: (a) Circuit configuration (b) Transient voltage plot.

Despite not sharing much similarities with the waves shown in the practical tests, this plot is similar to the ones shown in previous theoretical analysis, i.e., obtained using theoretical equations, which makes sense since this model was built using these same equations. Another reason for this discrepancy comes down to the movement exerted on the TENG. The movement made by the linear motor is not easily replicated inside the simulation environment, and this has a huge impact on the shape of the output voltage. Finally, the lab environment conditions also helped increase this mismatch since it is impossible to replicate these type of conditions inside the simulator.

As described before the shape of the wave highly depends on the type of movement that is being applied. To put this hypothesis to test, the type of movement was changed from an harmonic to a step wave, with and without rising and falling times to further increase the differences between waves, to see how this would affect the output characteristics of the TENG.

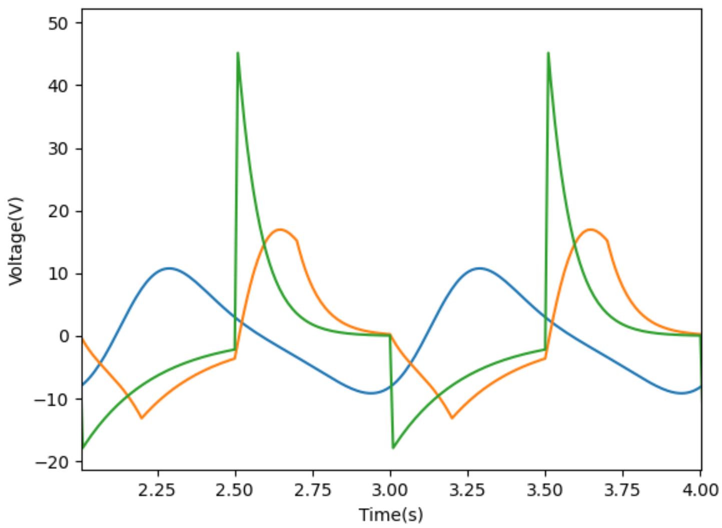


Figure 3.9: Effect of the input movement on the output voltage of the TENG cell.

The figure above confirms the hypothesis. The blue line represents the output for an harmonic input (the same plot as the one in Fig. 3.8b) while the other two lines were obtained by using a step input. The orange line resulted of an ideal step wave (rising and falling time equal to zero) while the green line happened after changing the step wave to have a rise and fall time of 0.2s. By exerting different movements on the TENG cell, the output voltage waveform changed accordingly since the TENG output voltage depends on the separation distance.

After confirming this, the input movement was explored with the objective of matching the real TENG voltage waveform. By using a step input with a period of 1.65s, which is roughly the average period obtained on the real TENG, and a pulse width of 400m the output voltage of the model cell had a good match with the real TENG voltage waveform as seen in the following figure.

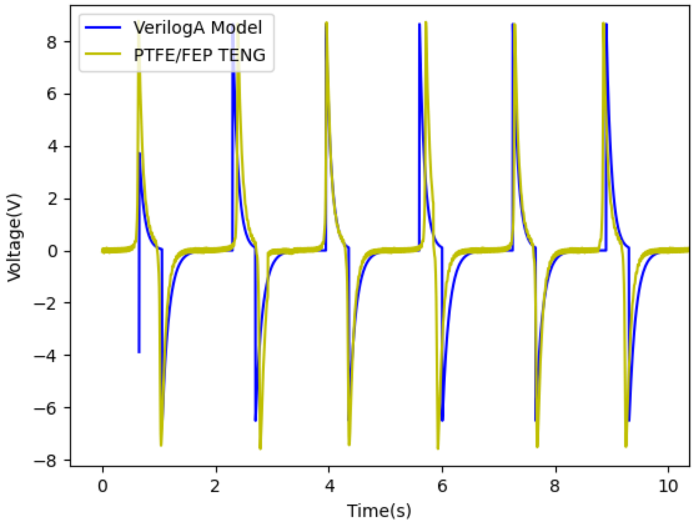


Figure 3.10: Output voltage comparison between the Verilog-A model and the PTFE/FEP TENG.

After matching the voltage waveforms, the current waveform for the Verilog-A model was obtained. Due to discrepancies between the setup in the TENG laboratory and the setup of the Verilog-A model inside the simulation environment, inconsistent values between the two were obtained and therefore render useless a subsequent analysis to the power profile of the Verilog-A model.

3.3 Equivalent Model

The Verilog-A model shown before was useful to understand that TENG electrical properties may be replicated to an extent inside the simulation environment, but since it is written in Verilog-A it caused convergence issues when doing more complex simulations.

To address this problem, a simpler model based on the equivalent TENG circuit was developed.

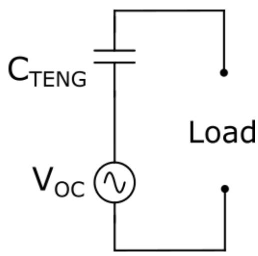
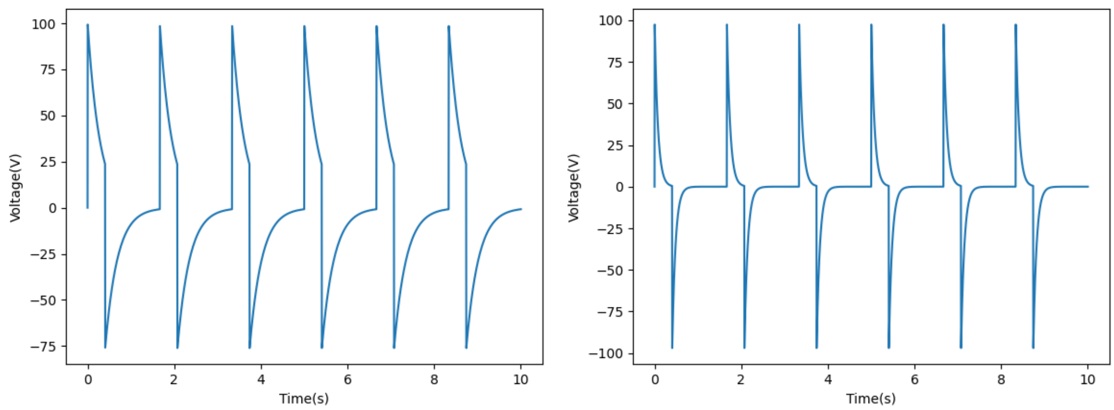


Figure 3.11: Equivalent electrical model of the TENG.

This model was developed with a generic TENG in mind, so matching this new model with the practical results was not the main objective but rather have a model that can produce a realistic TENG output characteristics. This equivalent model consisted of a voltage source with a capacitor in series. To replicate the shape of the voltage waveforms explored before, the voltage source in the model consisted of a pulse input with a frequency of 600mHz and a pulse width of 400ms. The peak voltage was defined as 100V. After varying the shape of the voltage source and the capacitor value, the voltage waveforms shown in Fig. 3.12 were obtained using a 5n series capacitor.



(a) (b)

Figure 3.12: Output voltage waveform for: (a) Maximum power point (56MΩ) (b) 15MΩ.

The plot shown in Fig. 3.12a was obtained using a 56MΩ load resistance, which is the value that corresponds to the maximum power point as will be shown shortly. Despite having created this model with the intent of replicating a generic TENG, the plot in Fig 3.12b intends to show that this model is also able to mimic the shape of the waveform of the PTFE/FEP TENG which may be beneficial in future comparisons for performance assessments.

Having obtained the desired TENG output voltage, the power profile was plotted to recognize where the maximum power point was achieved and what its value was, as well as understand how the power varied with the load resistance.

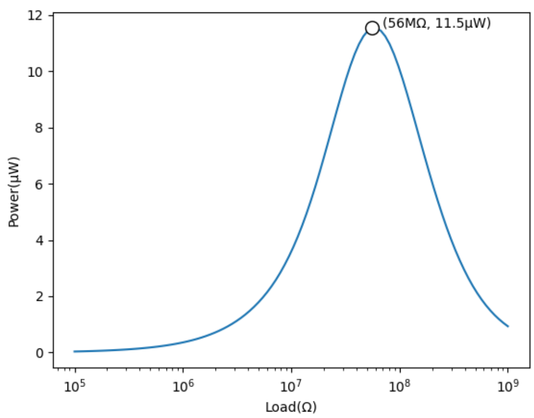


Figure 3.13: Power profile of the TENG equivalent model.

The maximum power achieved by this model was approximately 11.5 µW for a load of resistance of 56 MΩ. After having characterized this model and proven that it can replicate to a good extent the output characteristics of a real TENG, the foundation for realistic testing inside the simulation environment was finally achieved.

Chapter 4

Power Management Circuit

After modelling the TENG inside the simulation environment, the setup to test the power management circuit was finally set. With this important milestone done, it was time to start developing and designing the power management circuit.

The first step in the design process consisted in developing an architecture of the power management circuit that addresses the basic needs of the circuit. In total, the architecture can be divided in three main blocks:

- Rectification and Overvoltage Protection: this block addresses two major needs of the PM circuit. As the name of the block indicates it introduces rectification to the circuit as TENG harvesters mainly output AC waves. Without a rectifier the circuit would be rendered useless. The second point addressed by this block consists of an overvoltage protection circuit that protects the circuit from short-term exposure to high voltage peaks, something that may happen using triboelectric nanogenerators during extremely high power peaks.

- Undervoltage Protection: this block addresses the intention of the power management circuit to only turn on the circuit operating once a certain rectified voltage threshold is met. This is important since it enables the PM circuit to have minimal losses while it is trying to charge up to an operating voltage.

- Regulation: this block addresses one of the most fundamental needs of every power management circuit, regulation. Since the harvested energy by the TENG harvester is subject to constant variations, this becomes a problem if the output is unregulated. By introducing regulation the PM circuit is able to supply a stable output voltage to the load despite possible load or supply voltage variations.

Although the block diagram is important to get a good grasp of how the power management circuit is built, it does not delve into the sub-circuits that comprise the PM circuit and therefore limits the vision to only top-level.

To have a complete overview over the circuits that will be needed for the PM circuit and how they are interconnected, the complete circuit schematic is shown in Fig. 4.1.

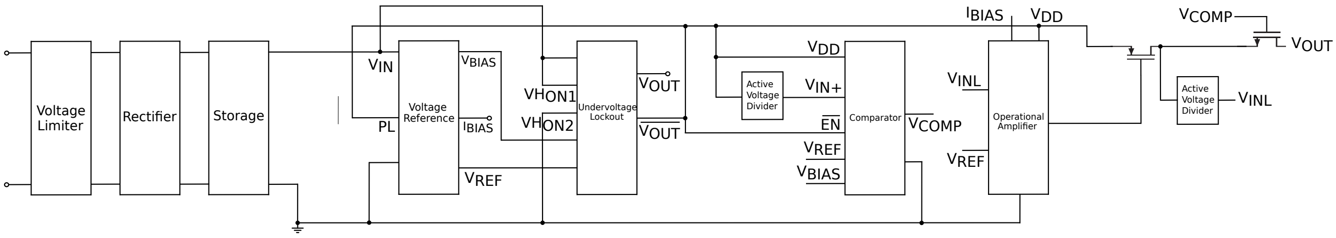


Figure 4.1: Power Management circuit schematic.

With an overview of the circuit components that need to be designed, the next sections will delve further into how each block of the power management circuit was designed to meet the circuit requirements.

4.1 Rectification and Overvoltage Protection

After modelling the TENG inside the simulation environment, the setup to test the power management circuit was finally set. With this important milestone done, it was time to start developing and designing the power management circuit. The first part of the circuit to be designed addressed rectification and protection from high voltages as these are the first main points of contact with the triboelectric nanogenerator harvester.

Energy harvesters scavenge ambient energy from the surrounding environment and convert it to electrical energy, generating an AC or DC output, depending on the type of harvester. Triboelectric nanogenerators, unlike solar cells and TEGs (Thermoeletric generator) who generate a DC output, generate an AC output. Therefore, to use the power harvested by the TENG in common electronics, AC to DC conversion is needed. To tackle this problem, a rectifier circuit was developed.

Apart from needing to transform the AC output into DC, TENG also have the particularity of having a very high output voltage. This represents a problem since not only the technology being used can only support up to 4V but most low-power electronics are charged with low voltages. To address this issue an overvoltage protection circuit was designed, which limits the input voltage of the power management circuit to about 4V.

4.1.1 Architecture

The overvoltage protection circuit and the rectifier together with a storage element form the first sub-circuit of the power management circuit. The top-level architecture is shown in the following figure.

The overvoltage protection circuit makes the first contact with the output from the triboelectric nanogenerator, effectively shorting the circuit when that voltage exceeds the 4V threshold. If the input voltage is less than the 4V threshold limit defined by the protection circuit, the rectifier converts the input AC wave into a DC output. Afterwards this energy is stored in the intermediate storage element of the sub-circuit.

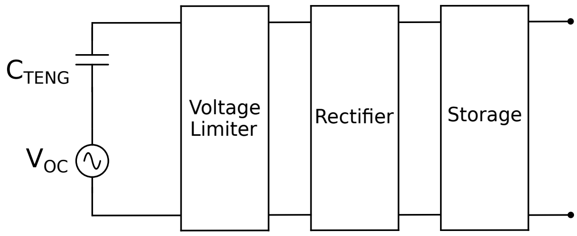


Figure 4.2: Rectification and Overvoltage protection sub-circuit block diagram.

4.1.2 Overvoltage Protection Circuit

As introduced before, this overvoltage protection circuit serves the purpose of protecting the power management circuit from possible damage due to high voltages. This circuit is designed to withstand high voltage spikes for only brief periods of time, as long exposure to high voltages will definitely render this protection useless. Naturally, this should be taken into account when deciding which kind of TENG harvester should be used as input. The schematic for this circuit is shown in Fig. 4.3.

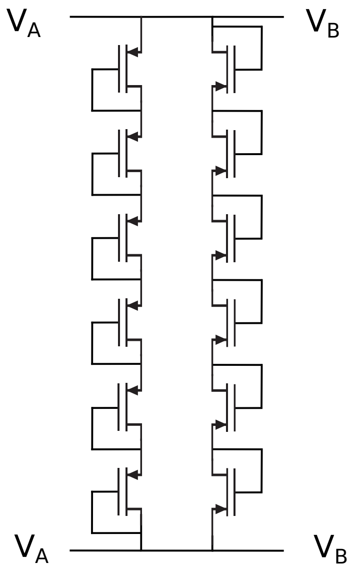


Figure 4.3: Overvoltage protection circuit schematic.

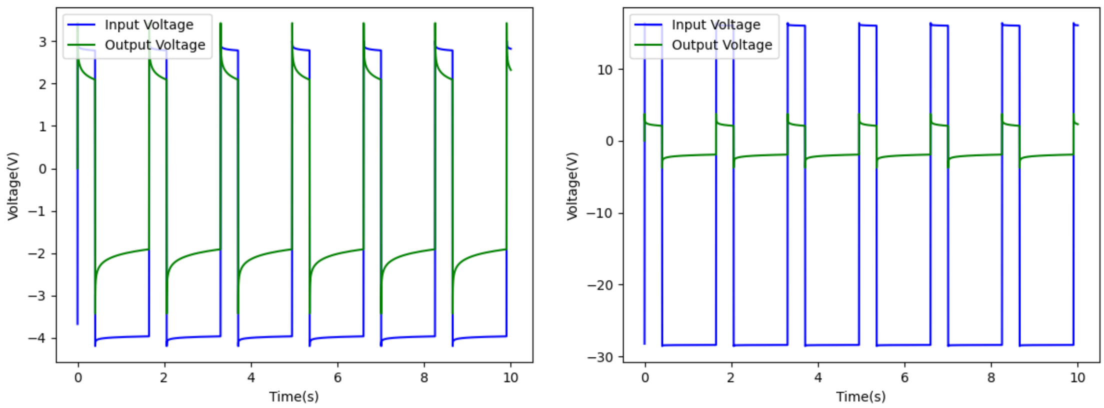
This protection circuit features a simple architecture comprised of two transistor paths with 6 diode-connected PMOS in series. The behaviour of this circuit is very simple. As the input voltage grows and the voltage threshold of each MOSFET transistor is met, one by one the transistors get turned on and enter saturation. When the input voltage reaches a point where all transistors are turned on, the path formed by those transistors creates a low resistance path, effectively shorting the circuit. During the time the circuit is active, the path created by these diode-connected transistors forces the voltage to a desired value. There are two paths to ensure both the positive and negative side of the input waves are covered by this protection.

Naturally, during the time one of these transistor paths is fully operating, no power is delivered to the output. This circuit was designed to limit the voltage to a value between 3.6 and 4V depending on the magnitude of the input voltage.

4.1.2.1 Operation

To test how this circuit performs under practical conditions, the TENG model was connected to its input. The circuit was tested under two different conditions to exemplify its behaviour:

- with a TENG output under 4V, where the circuit is yet to be turned on;
- With a TENG output of up to 30V, where the circuit should be turned on and force the output voltage to a value up to 4V.



(a) (b)

Figure 4.4: (a) Circuit turned off. Input voltage under 4V. (b) Circuit turned on. Input voltage over 4V.

As shown in Figure 4.4a, when the TENG output has not yet reached a voltage value that triggers the overvoltage limiter, the output of this circuit follows the input.

When the TENG output voltage exceeds the maximum voltage value accepted by the power management circuit, the overvoltage limiter acts (as in the previous situation) as a safety mechanism and the voltage presented in the output is guarded to a value of approximately 3.7V, as can be seen in Figure 4.4b.

The two previous situations cover the possible scenarios regarding the overvoltage limiter circuit and also serve to exhibit how the circuit limits the voltage within an acceptable range for the MOSFET technology.

4.1.2.2 Power Consumption

As pointed out in the last section, this circuit causes a short-circuit when the input voltage reaches the 4V threshold. While this circuit is turned on, no power is transferred to the rest of the circuit, effectively being lost. Therefore when the circuit is active, power consumption is not important.

When the circuit is not operating due to an acceptable input voltage range from the TENG, the circuit should ideally not consume any power. In practice, this is not possible but this circuit should aim to consume as little power as possible so as to not affect the overall efficiency of the power management circuit. This consumption will be further explored in the results section when the efficiency of the complete PM circuit is analysed.

4.1.3 Rectifier

Rectification is essential for any power management circuit that needs to deal with energy sources with AC outputs, as is the case with Triboelectric Nanogenerators. Rectifiers are commonly divided into two types: passive and active rectifiers. Passive rectification commonly refers to circuits built around p-n junction diodes, where there is no additional circuitry, having an emphasis on simplicity. On the other hand active rectification is generally used to improve efficiency by employing control circuitry. One such example is the use of comparators to control diode-connected mosfets, with the intent of minimizing conduction losses and reverse leakage currents. As expected, active rectification comes at a cost of increased complexity. In this work the focus was on passive rectifiers.

4.1.3.1 Full-wave Bridge Rectifier

The most commonly used topology among general purpose rectifiers is the full-wave bridge rectifier. This topology was already presented in the last chapter, where it used four diodes to perform full-wave rectification (see Fig. 2.9). This same topology can be achieved using CMOS technology by simply replacing the diodes with diode-connected MOSFETs, where the gates of each transistor are connected to their drain terminals therefore keeping the transistors in the saturation region. This simple replacement is already an improvement over using pn-junction diodes since the voltage threshold of MOS transistors is generally lower than the voltage threshold of said diodes.

As pointed out before, this topology shines for its simplicity but is generally lacking in terms of performance due to the two voltage drops in each rectifying path and the voltage thresholds the system is required to overcome.

4.1.3.2 Fully Differential Gate Cross-coupled Rectifier

To further enhance the full wave bridge rectifier topology without increasing complexity, the fully differential gate cross-coupled rectifier was chosen as the architecture to be used in this work. This topology increases the PCE (power conversion efficiency) of the previously shown full wave bridge architecture by connecting the gates of the 4 MOS transistors in a cross-coupled configuration as shown below.

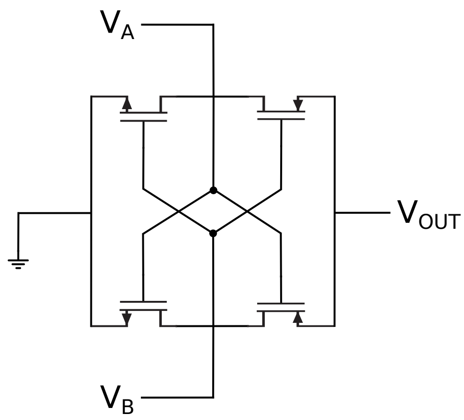


Figure 4.5: Fully Differential Gate Cross-coupled Rectifier circuit schematic.

This circuit works just like a typical bridge rectifier, i.e., whenever there is an high enough input voltage one of the two transistor pairs is turned on, depending on the voltage polarity, and makes up the rectifying path.

By using this configuration, the voltage threshold of both the transistors in each path is replaced by the effective voltage drop. The only drawback regarding this configuration is that it suffers from reverse conduction when the input voltage is lower than the output voltage. To reduce the losses regarding this reverse current, a pass transistor was connected to the output rectifier.

The next section will provide the results obtained with this fully differential gate cross-coupled configuration.

4.1.3.3 Operation

To understand if this rectifier was a good fit for the PM circuit in development, the TENG model developed earlier was once again used as the input source. The frequency used was 50Hz with a 10 MΩ load resistance along with a 30 nF smoothing capacitor to achieve an output wave with minimal ripple.

The input of the rectifier reaches an approximate peak voltage of 3.75V for which the rectifier achieves an output voltage between 3.05 and 3.1, therefore having a ripple of around 50 mV.

The output current can be seen in Fig. 4.7.

The output current for the rectifier circuit reaches a value between 305nA and 310nA, which gives a ripple of approximately 5nA.

4.1.3.4 Power Consumption

After confirming a correct and satisfying operation out of the rectifier circuit, it was time to understand how well it performed in terms of efficiency. To compute the efficiency of the rectifier circuit, the same setup used before with the TENG model cell to validate its operation was kept,

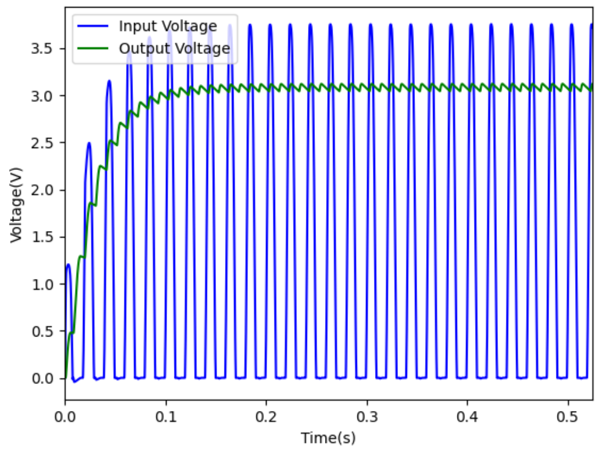


Figure 4.6: Transient simulation showing the output voltage versus the input voltage.

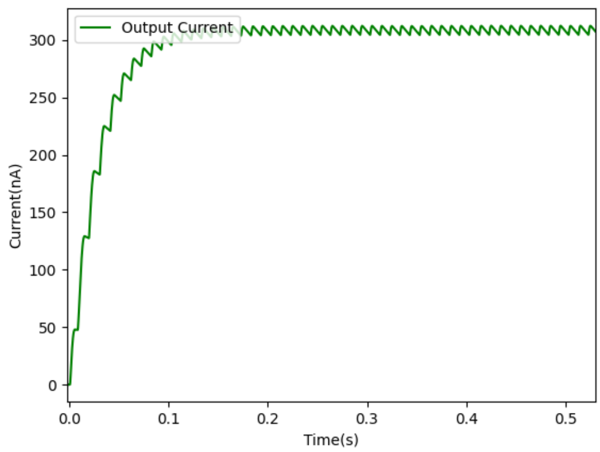


Figure 4.7: Transient simulation showing the output current.

to have an efficiency value closer to what is expected when the system is deployed. The efficiency was computed through means of a Periodic Steady State simulation with a load value of 10M. The efficiency is given by Equation 4.1.

$$\eta = \frac{P_{OUT}}{P_{IN}} \times 100 = \frac{0.947u}{1.149u} \times 100 = 82.44\% \tag{4.1}$$

4.2 Undervoltage Protection

After designing the overvoltage protection and rectification circuits, the next step in the design process consisted in developing an undervoltage lockout circuit to avoid operating when the input voltage drops below what is considered the operational level. This circuit prevents the IC from malfunctioning due to a voltage below the expected operating voltage and prevents the power management circuit from delivering any power to the load, as the aim of the PM circuit is to deliver a voltage of at least 2.7V.

4.2.1 Architecture

The designed Undervoltage Lockout (UVLO) circuit works by comparing the rectified input voltage value with an internally generated threshold voltage that determines when the subsequent circuitry should start operating. At the output, two complemented signals are provided as both may be useful depending on the logic that follows the UVLO. For this specific case, the inverted output will be the one providing the desired logic value.

This circuit is also dependant on a voltage reference to generate a stable operating voltage and a bias voltage, therefore an additional voltage reference circuit was designed to operate the undervoltage lockout circuit. The top-level architecture for the undervoltage protection sub-component of the power management circuit is shown in Fig. 4.8.

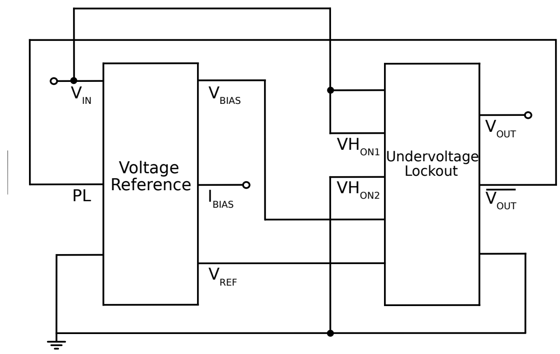


Figure 4.8: Undervoltage Lockout circuit top-level architecture.

4.2.2 Voltage Reference

As mentioned earlier the undervoltage lockout circuit requires not only a stable voltage to operate but also a bias voltage. The voltage reference generates both the bias voltage and the voltage reference and introduces a preload (denoted by the PL pin in the top-level architecture) that enables the voltage reference to start-up more rapidly as the energy previously stored before being powered off is kept. The schematic for this circuit is shown in Fig. 4.9.

Transistors M1 – M3 are used to startup the circuit. The PMOS transistors M4 – M7 are in charge of generating the bias voltage that feeds both the undervoltage lockout and the comparator circuit. The voltage reference generator, M8 – M11, generates a stable voltage reference given by the gate voltages of M8 and M10. Making use of the bias voltage, transistors M16 and M17 generate a bias current that feeds the Low-drop Regulator circuit. Finally, transistors M12 and M13 are tasked with the Preload. When the PL signal changes from a low value to a high value (turning off M13), M12 acts as a capacitor to avoid losing the voltage that was previously seen and with this, when the PL signal goes to a logic low again, the circuit will be started in a faster manner.

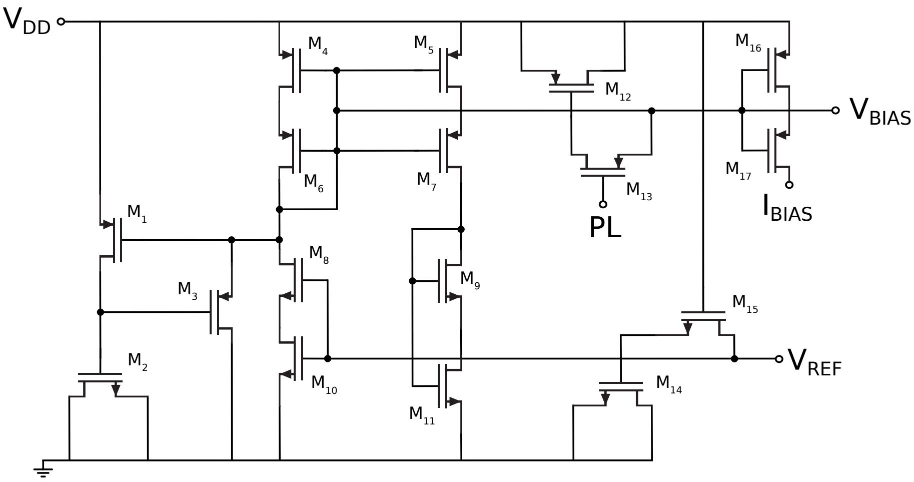


Figure 4.9: Voltage Reference circuit schematic.

4.2.2.1 Operation

This circuit was tested under two conditions to verify its operation. First, this circuit was tested using an ideal DC source as the input to understand if the circuit was able to provide the expected voltage reference for a wide input DC range. Afterwards, when the voltage reference has been successfully tested, the TENG input along with the rectifier were connected to the circuit input to understand if it would work under the rectified TENG wave.

As the name itself indicates, a voltage reference is supposed to provide a stable output voltage over a DC input range. For this specific design, the expected voltage level is around 240 mV. To test this a DC sweep was performed between the value of 0 and 3.3V to see how the output voltage reacts. The result can be seen in Fig. 4.10.

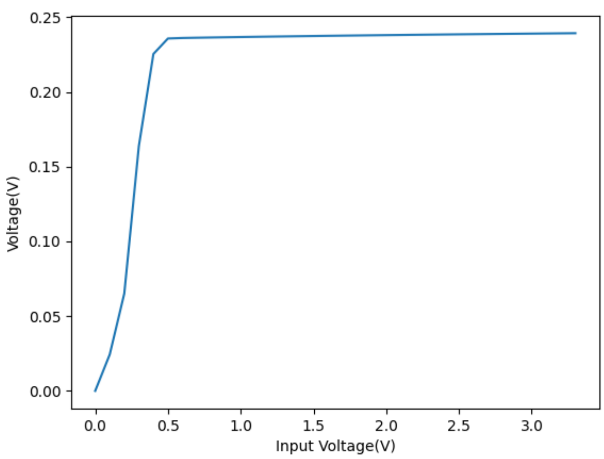


Figure 4.10: DC Sweep of the input voltage.

The voltage reference is able to produce a stable output voltage of approximately 238 mV between the input supply values of 0.5V up to 3.3V. When the input voltage is 0.5V the circuit outputs a 235 mV voltage and when the input reaches the 3.3V mark the output is 238mV. This indicates that the voltage reference suffers a small variation of 3 mV over its operation range, which is acceptable.

Having tested the basic operating mechanism of the voltage reference, a simple test was performed to see if the designed voltage reference worked under pratical conditions, i. e., when the circuit is connected to the TENG model. The result can be seen in Fig. 4.11.

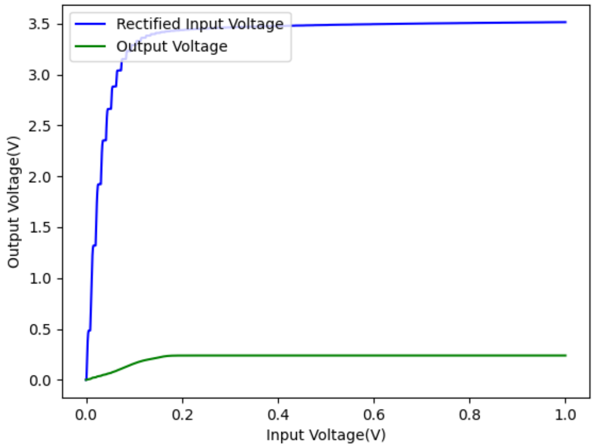


Figure 4.11: DC Sweep of the input voltage.

4.2.3 Undervoltage Lockout

The undervoltage lockout circuit, as described before, compares the input voltage with an internally defined threshold voltage. If the input voltage is lower than the threshold the UVLO inverted output follows the input voltage, and when the threshold is crossed the output drops to zero. This output is connected to the voltage reference Preload (PL) input as shown in the architecture in Fig. 4.8, which is in charge of starting up the voltage reference. This inverted output is also connected to a comparator (as will be seen in the next chapter) which will only start operating when the voltage threshold is met, effectively disabling power delivery to the load until the input rises. The schematic for this circuit is displayed in Fig. 4.12.

Transistors M1 – M6 are used to generate the undervoltage lockout logic output by using the VH_{ON1} and VH_{ON2} and the voltage reference inputs. Transistor pairs M8 – M9 and M11 – M12 form the typical inverter structure and are used to deliver complemented signal values at the output.

4.2.3.1 Operation

Just like the voltage reference, this circuit was also tested under two different situations. In both scenarios the circuit setup is as shown in Fig. 4.8, with the difference being the type of input is connected to V_{IN}. To understand if the circuit was behaving as intended, a pulse wave with a rising and falling time was connected to its input with a peak voltage of 3.3V. Since the applied input

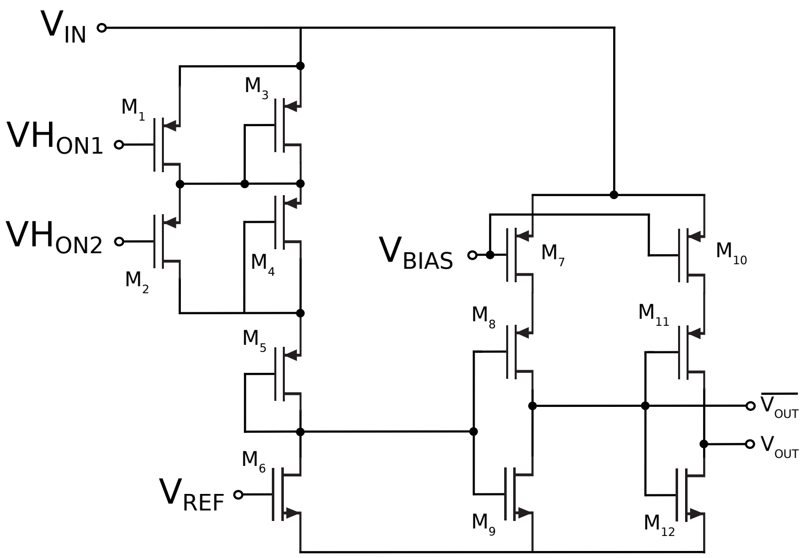


Figure 4.12: Undervoltage Lockout circuit schematic.

starts low, the inverted output should follow the wave as it rises and when the threshold is crossed, the output should drop to zero. The result of this simulation can be seen in Fig. 4.13.

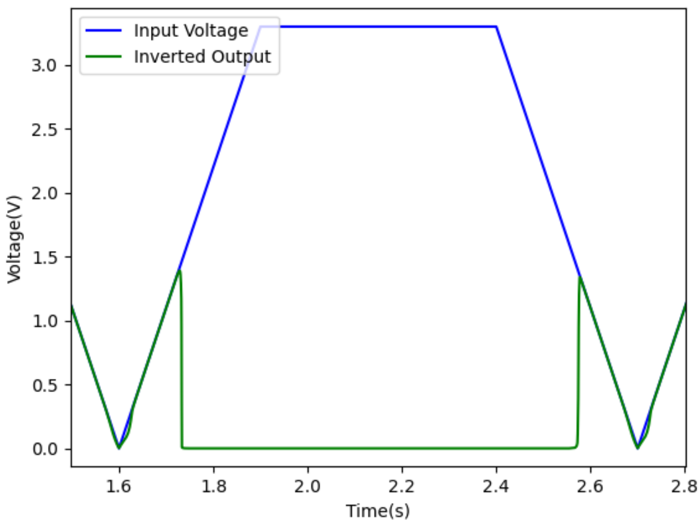


Figure 4.13: Transient simulation with a pulse wave input.

As expected, when the input voltage reaches the 1.45V threshold, the inverted output goes down and signals the voltage reference and the comparator that the input voltage is within the operating range.

In a second scenario the architecture presented in the beginning of this chapter is connected to the designed input rectifier and the input source is changed to the TENG model cell to obtain a pratical result. A transient simulation was performed with the TENG model cell delivering a voltage within the operating range, therefore the undervoltage lockout inverted output should stay low during the simulation to indicate a valid input. The result of this simulation can be seen in Fig. 4.14 below.

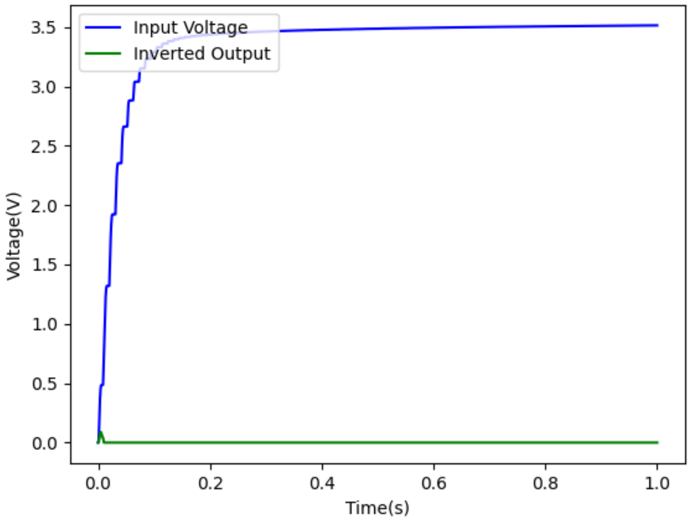


Figure 4.14: Transient simulation with a pulse wave input.

In this scenario, the input voltage rises quickly and the UVLO does not follow the input voltage before the threshold is crossed, which is shown as a little bump in the beginning of the simulation. The UVLO then detects that the threshold was crossed, drops the voltage to indicate a logic zero and maintains the inverted output low for the remainder of the simulation.

4.3 Comparator

In the last subsection the undervoltage lockout circuit was designed to shut down the power management circuitry when the input voltage was under the stipulated operating level. One of the circuits that is affected and directly controlled by the UVLO circuit is the comparator. The comparator was added to the power management circuit as a means of enabling the output pass transistor to deliver a stable output through the LDO.

The comparator is a very commonly used circuit for a variety of reasons. In this specific case it is useful to make a comparison between the harvested voltage that reaches the comparator input and a set voltage reference. For the present design the goal was to enable the output pass transistor to present a stable output voltage only when the rectified input wave was at least 3V. By employing this circuit, the power management circuit avoids feeding a low voltage value that may damage or cause an operating malfunction to the connected devices at the load.

The comparator circuit schematic can be seen in Fig. 4.15.

The presented amplifier is a differential to single-ended amplifier. As referred before, transistor M1, M6 and M15, to which the gate is connected to the negated input pin EN serve the purpose of enabling and disabling the circuit operation. Transistors M4 and M5 generate a current through

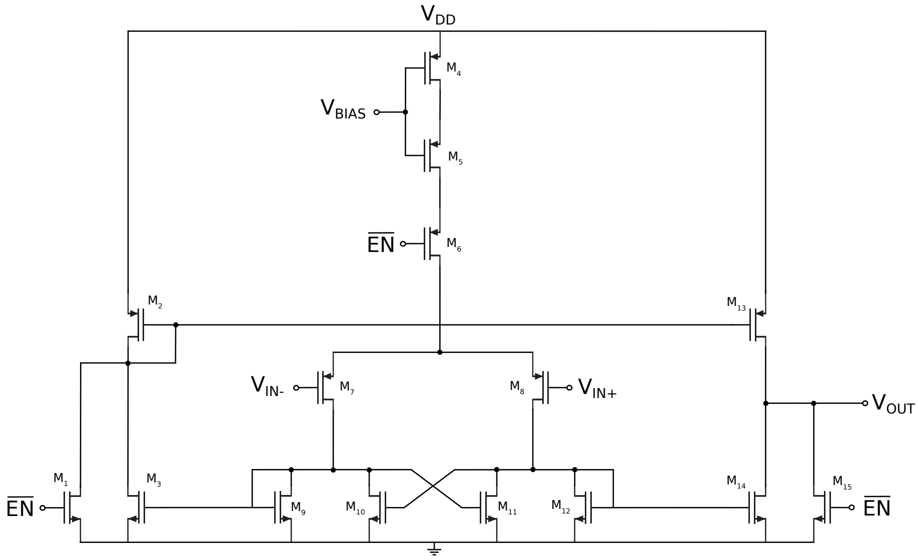


Figure 4.15: Comparator circuit schematic.

the VBIAS input voltage. Transistors M7 and M8 form a typical differential input pair. Transistors M9 – M12 form a positive feedback path that is used to generate the hysteresis.

A second circuit had to be designed to allow the use of the low voltage value that is generated by the voltage reference. In order to compare the voltage reference to the VDD, a voltage divider needs to be used. A simple purely resistive voltage divider could be used but it would consume too much power, which would increase the total power consumption of the circuit and decrease the overall PM circuit efficiency. Therefore, an active voltage divider was devised by using MOSFETS in series. This circuit schematic can be seen in Fig. 4.16.

Depending on the number of transistors used in the upper part of the design, the voltage division can be further tweaked. In this case, the active voltage divider for the comparator was designed to have a voltage of 260mV when the VDD reaches 3V.

4.3.1 Operation

The comparator is a decision circuit that either outputs a low or high input depending on the comparison result. For the designed comparator, when the voltage at the VIN+ input is higher than the reference voltage, the VOUT pin will output a voltage equal to the one fed on VDD. If the input is lower than the reference voltage, the output drops to zero. To test this behaviour, the comparator was simulated using an AC source with a voltage peak of 2.5V as the non-inverting input and a DC source of 1.8V as the inverting input.

To obtain results for the comparator behaviour a simple transient simulation was performed. The results are displayed in Fig. 4.17.

As expected, as the input voltage at VIN+ crosses the reference voltage fed at VIN-, which in this case is set to 1.8, the comparator output jumps to the value at VDD rail and when the input voltage drops below that reference voltage the voltage plummets to zero. One important

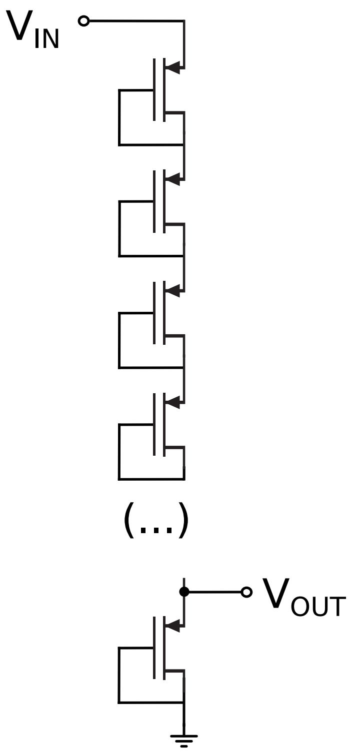


Figure 4.16: Active voltage divider circuit schematic.

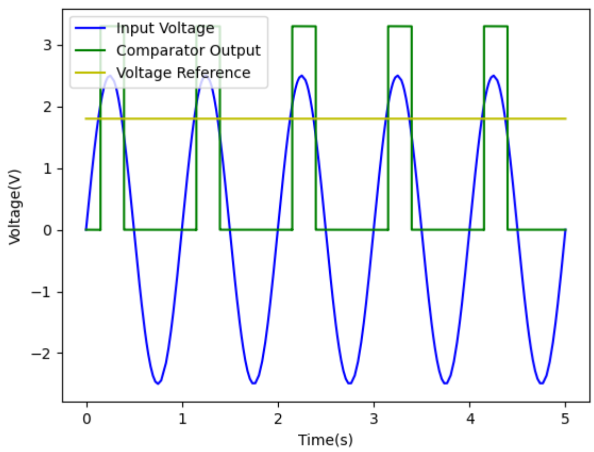


Figure 4.17: Transient simulation of the comparator.

characteristic of this comparator is in the use of hysteresis. Although the comparator changes its logic value when VREF is crossed, either by being higher or lower, the change at the comparator output is slightly delayed as seen in Fig. 4.17. This happens because instead of having a single threshold, one upper and one lower threshold are used. This feature is crucial to avoid multiple transitions due to noise, or in this case, due to variations in the TENG supplied voltage.

4.4 Low-Dropout Regulator

In Chapter 2 a comparator circuit was presented and the main goal of said comparator was to enable the Low-Dropout Regulator output to be delivered to the load.

In this chapter the LDO is presented and it represents the last component in the PM circuit design. This circuit is fundamental in any power management circuit as it is capable of delivering a stable voltage over a certain operating range without being affected by load changes. Therefore it comes as no surprise that this circuit also needs to be designed for the present power management circuit. In this case, the LDO was designed with the intent of maintaining a 2.7V stable output to avoid output voltage fluctuations due to variations in the energy harvested by the TENG.

For this specific circuit, an operational amplifier was used to build the LDO. The typical LDO configuration was used in which the inverted input of the operation amplifier is connected to a voltage reference and the non inverted input is connected to the targeted input power supply voltage. The output of the operational amplifier is then connected to a pass transistor that makes the bridge between the input power supply and the delivered power supply. For this specific design the voltage reference is the same as the one presented before, which is approximately 240mV. Therefore the non-inverted input voltage is connected to an active voltage divider similar to the one shown before for the comparator. The circuit configuration is shown in Fig. 4.18.

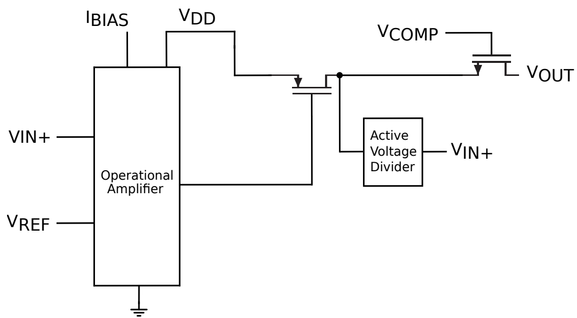


Figure 4.18: Low-Dropout Regulator circuit configuration.

The schematic for the operational amplifier circuit is shown in Fig. 4.19.

This is a typical two-stage operational amplifier with a third bias stage, formed by transistors M9, M10, M12 and M13. The bias current is delivered by the voltage reference. The first stage corresponds to the differential input stage, where the gates of transistors M6 and M7 receive the inputs to be compared. The second stage formed by M5 and M8 makes up the common-source stage.

4.4.1 Operation

To test the designed Low-Dropout Regulator to see if it was able to output a stable 2.7V voltage over a decent operating range, a DC sweep on the VDD pin was performed to understand how the LDO reacts. Since the objective of the LDO is to deliver a stable supply voltage to the load once the voltage supply at the input reaches the 3V mark, its important run a DC sweep to understand

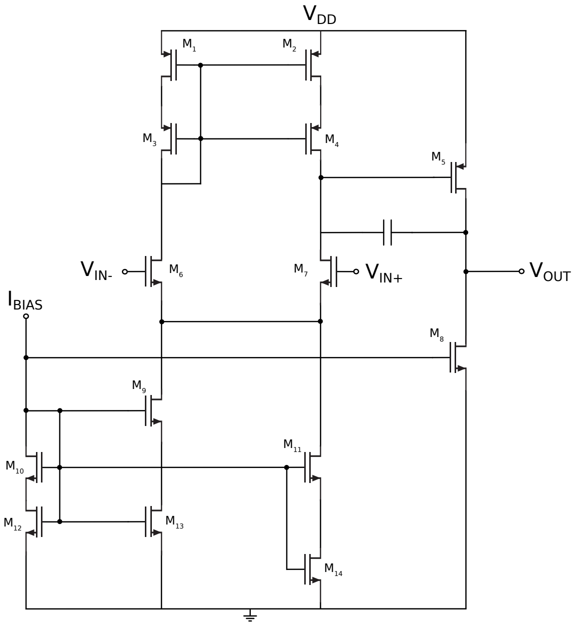


Figure 4.19: Operational Amplifier circuit schematic.

if circuit components such as the active voltage divider were well dimensioned such that the delivered output is at least 2.7V. For this simulation the VDD was set to 3V, the VREF was set to 240mV and the bias current IBP was set to 100n. The results for the DC sweep simulation are shown in Fig. 4.20.

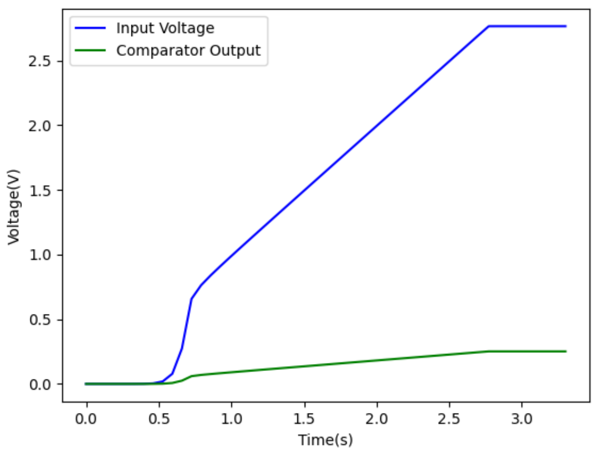


Figure 4.20: Transient simulation of the Low-Dropout Regulator circuit.

The LDO is able to provide a stable voltage of approximately 2.76V when the circuit supply VDD is within the 2.8V and 4V voltage range.

4.4.2 Power Consumption

Another important aspect regarding the LDO, as with every single component that comprises the power management circuit, is the circuit efficiency. One of the reasons the circuit configuration shown in Fig. 4.18 features an active voltage divider made up of MOSFETS connected in diode is to avoid using the typical resistors that consume a lot of power.

To test the efficiency of this circuit, a resistance load was connected in parallel with the active voltage divider. The obtained efficiency is described in Equation 4.2.

$$\eta = \frac{P_{OUT}}{P_{IN}} \times 100 = \frac{76.45u}{86.48u} \times 100 = 88.4\% \tag{4.2}$$

Chapter 5

Results

After verifying every single component that makes up the power management circuit, it was finally time to test the circuit as a whole to understand if the power management circuit behaves as expected and what is its performance level in terms of efficiency.

In the last chapter every circuit component that makes up the power management circuit was tested and validated individually. When the power management circuit is build and every component is integrated it is important to understand if any integration issues arise.

To test this, the power management circuit was connected to the TENG model cell to assert its behaviour under realistic conditions. To validate the circuit operation two different scenarios need to be tested. One where the TENG model cell is programmed to output a voltage lower than 3V, meaning the comparator output in the regulation block should disallow any output to the load. A second scenario where the TENG model cell outputs a voltage of around 3V to which the PM circuit should output a stable output voltage to the load.

Afterwards, when the circuit operation is validated, a performance test regarding the circuit efficiency will be presented.

5.1 Circuit Operation

To test the two operation scenarios presented earlier, the power management circuit architecture previously shown in the introduction (Fig. 4.1) was connected to the TENG model cell at the input and a capacitor was also added to the load to act as a storage device.

For the first scenario, the TENG model cell was programmed to have a peak voltage of 3.9V and a frequency of 50 Hz. The capacitor connected to the load was sized to be 1 µF. The results were obtained through the means of a transient simulation. To avoid cluttering the plots the input TENG voltage and corresponding rectifier output are shown in Fig. 5.1 and the same rectified along with the most important logic signals and the output voltage are shown in Fig. 5.2.

As expected, as the voltage rises quickly, the UVLO also quickly drops its non-inverted output to zero and maintains it throughout the rest of the simulation. This enables the comparator to start operating and instantly the comparator notices that the 3V threshold has been crossed and rises its

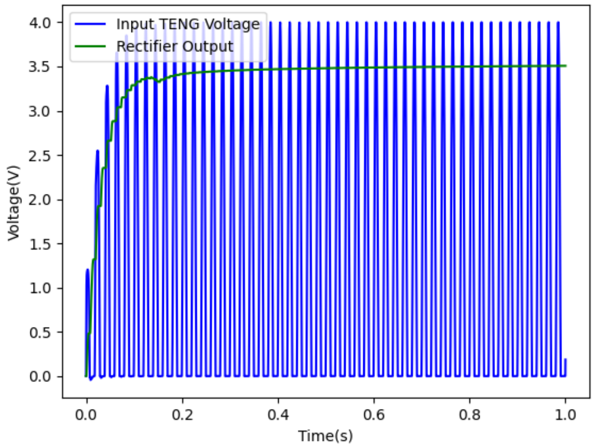


Figure 5.1: Output voltage for the rectifier of the PM circuit for a transient simulation.

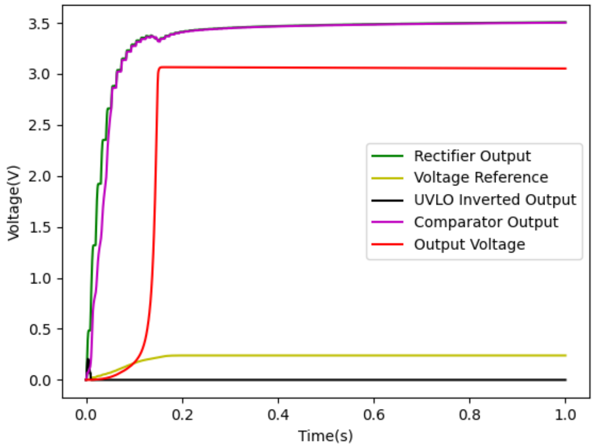


Figure 5.2: Intermediate logic signals and output voltage of the PM circuit for a transient simulation.

output signal to the VDD rail. In turn, this enables the output pass transistor to start delivering a stable voltage of approximately 3V given by the Low-Dropout Regulator.

In a second scenario, the only difference resides in the TENG input voltage level, which is toned down to 2V. With this voltage level the comparator is supposed to be enabled, but making the decision to the output pass transistor that the voltage level is below the operating range. The results were once more divided between two figures to avoid cluttering. These are displayed below.

Through Fig. 5.3 it is clear that the rectified voltage is 1.5V, which is enough to turn on the comparator. In the beginning of the simulation there is a slight misbehaviour by the PM circuit since the comparator output goes high when the rectified voltage is under 3V. This happens due to the delay in the voltage reference circuit to generate the 240mV voltage that is compared in the comparator. When the voltage reference finally establishes itself, the comparator goes down (not

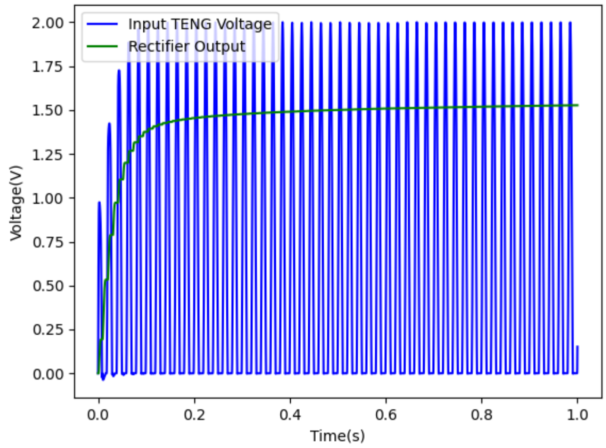


Figure 5.3: Output voltage for the rectifier of the PM circuit for a transient simulation.

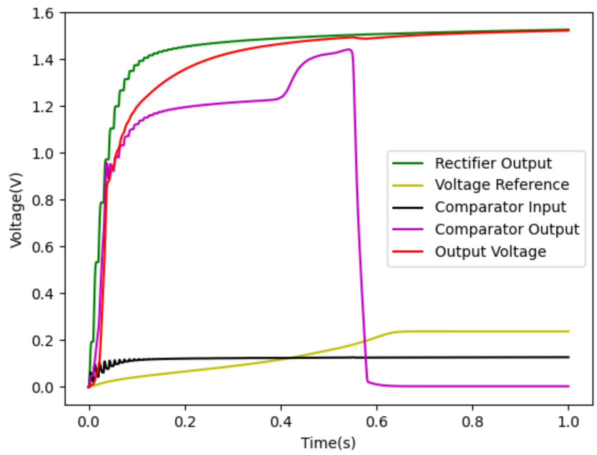


Figure 5.4: Intermediate logic signals and output voltage of the PM circuit for a transient simulation.

immediately after crossing the 240mV due to hysteresis). In the space of time that the comparator is active the output pass transistor transfers power to the load which can be see in the output voltage. After the comparator goes down, the load voltage should have gone down but since the circuit setup does not have any resistive load connected, the capacitor and the parasitic capacitance of the pass transistor hold the voltage. Naturally, if any kind of load was connected the output voltage would have plummeted.

5.2 Efficiency

The last step in characterizing the power management circuit comes down to its efficiency. To compute the efficiency of the PM circuit the power at the input and output terminals of the circuit were determined. To discover the total input power delivered to the circuit, the TENG model terminals were probed. To find the output power that the PM circuit supplies to the load, a resistance load was connected to the circuit in parallel with the output capacitor.

The efficiency of the circuit is dependant on the load resistance value that is connected to its output. Therefore, to find the maximum efficiency point of the PM circuit, a load sweep was performed. In the beginning the load sweep was performed over a large range of resistance values, but after the first simulation it was narrowed down to values between 1M and 5M. The result of this simulation can be seen in Fig.5.5.

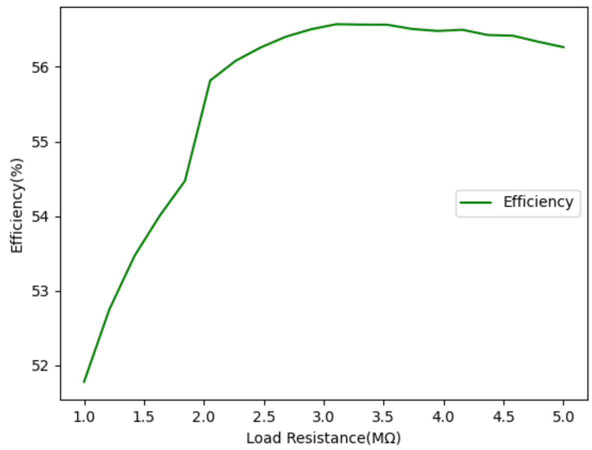


Figure 5.5: Load resistance sweep for PM circuit efficiency.

As seen in the above plot, the maximum efficiency is achieved for a load value of 3.3M, for which the efficiency reaches a value of 56.5%. Outside the displayed range of values the efficiency goes down abruptly, therefore, if possible, the load should be kept between the values of 1M and 5M to get the most power out of the circuit.

5.3 Discussion

The outcome of this research has certainly validated the proposed work since the circuit relied only on the input power to power itself, achieving full autonomy. Despite achieving perfect autonomy, the circuit failed to reach an high efficiency, therefore having the limitation of only, and in the best case scenario, delivering about half of what can be extracted at any time by the energy harvester. Due to the lack of power management IC studies done on TENG, it is hard to make a performance assessment of this architecture in relation to other architectures. Despite this efficiency limitation, the circuit implemented a novel way of limiting power waste by using a comparator that makes the decision to only deliver power until the input voltage is high enough to supply common electronics. Another important characteristic validated by simulation was the robustness of the circuit. Due to the overvoltage protection and undervoltage lockout circuitry the circuit is able to withstand peaks of power for short periods of time and avoid any malfunctions related to low voltage.

Chapter 6

Conclusions

Effective power management circuit designs are essential to make advancements in the area of green electronics. The circuit implemented in this work, despite complying with what was proposed, still lacked in efficiency which means that there is still a lot of room for improvement. This lack of efficiency can be directly correlated with the state of the harvesting technology. There were already some studies published regarding power management circuits for TENGs, but these are still very scarce for integrated-circuit solutions. Therefore this makes designing a power management circuit for TENGs harder than for a developed technology like Photovoltaic harvesters.

Nevertheless and despite the lacking efficiency, developing this work brought a new functional architecture into the IC PM circuitry literature directed at TENG, and therefore is making its part in helping the growth of the technology.

6.1 Future work

Although the main goal of the work was accomplished, the designed power management circuit could certainly be improved in certain areas.

One of the key aspects of this circuit, the efficiency, could be improved in different ways. One of the easiest ways without having to make significant changes to circuit comes by making a detailed analysis on each sub-circuit consumption to understand where the design is wasting more power. By employing different techniques like making new transistor sizings, or introducing some minor architectural changes on some sub-circuit schematics, the efficiency of the circuit could definitely be improved upwards of the current value of 57%.

Another important change that could highly benefit the PM circuit in terms of power extracted would be the introduction of Maximum Power Point Tracking (MPPT). The main point of MPPT is to extract the maximum available power by making the circuit operate at the most efficient voltage. This technique would be a great benefit to have as the current PM circuit suffers from a large efficiency fluctuation.

Finally, improvements can also be achieved without changing the PM circuitry. It is important to take a different perspective and understand that this circuit will be integrated with a certain energy harvester. In this work, the circuit was conceived to extract power from a triboelectric nanogenerator and although some research was made to understand how TENGs work, if a more extensive research is conducted, the user can increase the efficiency by simply choosing specific triboelectric materials, or by employing certain TENG configurations that will have a higher level of affinity with the designed PM circuitry and therefore increase the extracted power and efficiency.

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