FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO

DAB DC-DC Converter for use in an AC Power Bank

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Resumo

Nos últimos tempos as soluções de armazenamento de energia, principalmente em bateria, têm vindo a ver um crescimento quer de mercado quer em inovação. Isto em conjunto com o aumento das pressões sociais e políticas em prol de uma busca pela utilização de energias renováveis, e praticas de utilização das mesmas cada vez mais sustentáveis. Cria um espaço comercial para os chamados *Power Banks* .

Esta dissertação incide sobre o *design* e simulação, em *Matlab/Simulink* , de um conversor da topologia *Dual Active Bridge* capaz de integrar um dispositivo *Power Bank* ; o objetivo deste dispositivo seria a alimentação de cargas quer AC quer DC para situações em que o acesso à rede elétrica é ou impossível ou incomodativo, servindo de substituto aos geradores a combustíveis fosseis. O conversor será desenhado e simulado para fazer a interligação entre a bateria e qualquer carga DC que se ligue ao *Power Bank* até um máximo de $120W$. E deverá ser capaz de trânsitos de potência bidirecionais que permitam carregar a bateria.

Dois adicionais níveis de liberdade foram levados a cabo, nomeadamente o desenho e caracterização da bateria que o dispositivo *Power Bank* teria, e a exploração de dois tipos de modulação. Assim, as modulações em *Quasi-Square-Wave* e *Square-wave* são introduzidas e simuladas, tendo em vista a escolha da que se melhor adequa aos objetivos pretendidos.

Por fim, propostas de trabalho futuro são recomendadas para eventuais iterações e ou inspirações no trabalho possam ser realizadas com mais e ainda melhores resultados.

Abstract

As of late the energy storage solutions, mainly batteries, have been having a growth in both market and innovation. This is in conjunction with a rise in social and political pressures for the utilization of renewable energies, and increasingly sustainable practices of utilization. Creates a commercial space for the so-called *Power Banks*.

This dissertation focuses on the design and simulation, using *Matlab/Simulink*, of a *Dual Active Bridge* converter capable of integrating a *Power Bank* device; the objective of this device would be the supply of electrical energy to power up both AC and DC loads in situations where the access to the electrical grid is either unavailable or a nuisance, serving a substitute for the common fossil fuel generator. The converter will be designed and simulated to make the interconnection between the battery and any DC load that is connected to the *Power Bank* less or equal to $120W$. Bidirectional power flow must be arranged so as to allow for the charging of the battery.

Two additional freedom degrees were carried out, namely the design and characterization of the battery that the *Power bank* device would have, and the exploration of two different kinds of modulation. Thus, the *Quasi-Square-Wave* and *Square-wave* modulations were introduced and simulated, with the idea of comparing them and finding the one who would better suit the wanted objectives.

At last, future work proposals are recommended so that eventual iterations and or inspirations on the realized work can attain more and even better results.

Key Words: *Dual active bridge converter, Energy storage applications, Quasi-Square-Wave modulation.*

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A todos vocês um encarecido obrigado, pois é sem dúvida a vocês que devo o culminar da minha formação, quer enquanto pessoa como enquanto Engenheiro.

Nuno Miguel Fernandes Pacheco

"Enquanto houver estrada para andar,
a gente vai continuar."

Jorge Palma

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Abbreviations and symbols

C	Electrochemical Cell Capacity
C_{iss}	MOSFET input capacitance
C_{oss}	MOSFET output capacitance
C_{rss}	MOSFET reverse transfer capacitance
DAB	Dual active bridge
E	Energy
EM	Electrochemical model
ECM	Equivalent circuit model
f_c	Cutoff frequency
LUT	Lookup Table
PSM	Phase Shift Modulation
SQW	Square-wave
QSW	Quasi-Square-Wave
Q	Quality factor
R_{DSon}	MOSFET drain-source on-state resistance
SoC	State of Charge
SoH	State of health
SQW	Square-Wave
V_n	Cell Nominal Voltage
$V_{Fully\,Charged}$	End Of Charge Cell Voltage
V_{fw}	MOSFET body diode source-drain voltage
$V_{cut-off}$	Cell Cut-off Voltage
V_{th}	MOSFET gate-source threshold voltage
V_{gp}	MOSFET gate-source plateau voltage
ζ	Damping factor

Chapter 1

Introduction

The aim of this dissertation will be the specification, design and validation of the bidirectional dual active bridge DC/DC converter. This first chapter will lay a foundation for the document, introducing the topic at hand by indicating the motivation behind it and its goals.

The structure of this document will also be indicated in this chapter.

1.1 Context and Motivation

The increasing electrification, that has been happening in the last decades, has led to an escalation in electrical energy dependence. The amount of devices that exist on the market today, which rely on electrical energy to function, is plentiful and their applications are diversified. Since the impact of electrical devices on the daily lives of the common person is undeniable and their industrial use is irrefutable, it is the task of the engineer to bring innovation, safety, and efficiency to the table.

Where there is a device that functions on electrical energy, there is a need for supply. While access to electricity has become increasingly facilitated and widespread there are still many applications, in which, it is not guaranteed. Powering small fridges while camping, charging a vehicle's battery, or powering an electrical water pump outside urban areas, for example, can require an autonomous power source. Traditionally this is handled by diesel/gasoline generators that are dependent on fossil fuels; factors such as growing environmental concerns, the non-renewable nature of its fuel, and the crescent viability of electrical energy storage solutions through batteries, make the so-called *Power Bank* a reliable substitute.

The main dissertation topic, from which this dissertation resulted, was to create a device that could store electrical energy and had the means to supply it through both AC and DC outputs. The objective in mind would be to provide a substitute for fossil fuel generators. Upon further consideration, in conjunction with the supervisor, it was decided to focus on the DC output part of the device and that will, therefore, be the topic of this dissertation.

The work at hand will approach both energy storage and electrical conversion, individually each topic proves to be the object of wide research and innovation due to its fundamental importance to today's society. Together they are a plentiful complement to what was my academic path

and a wonderful reflection of my interests as a student.

1.2 Goals

The main objective of this dissertation will be the development of the DAB DC/DC converter to be incorporated into a larger *Power Bank* device; an overview of the larger *Power Bank* device is presented in figure 1.1 in form of a diagram, the modules addressed in this dissertation are emphasized through red squares with thicker lines.

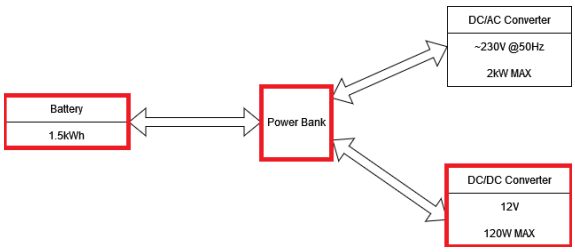

Figure 1.1: Diagram of the power Bank device.

Regarding the battery pack, should be sized with the $1.5kWh$ autonomy in mind; as such, a reliable battery pack or electrochemical cell must be found on the market with which the battery pack should be built. Attention to the variation of voltage with the evolution of the battery's state of charge should be considered and its impact on the converter functioning must be studied.

Regarding the DC/DC converter, it should be capable of bidirectional power flow allowing for the possibility of charging and discharging the *Power Bank* from the same port. Such a decision makes the device not only more robust to the multiple applications it can find but also simplifies the overall device design; making it more intuitive to use, cheaper to build since it no longer requires other ports/converters dedicated for charging the battery.

It is important that the output voltage of the converter is kept at $12V \pm 5\%$, this should be true regardless of the load changes verified throughout the converter's operation. Also, the voltage ripple at the converter's output during steady state operation must be limited to 1% of $12V$ ($0.12V$). Furthermore, the output, should also, be capable of supplying current ranging from $0A$ to $10A$, across its operation. Focus should also be given in maximizing the efficiency of the converter, due to the nature of the device in which it shall be incorporated.

1.3 Document Structure

This dissertation is organized into the following chapters:

Chapter 1 introduces the document, laying the basis for the work that is going to be made. The motivation for the choice of this dissertation is described and the topic is contextualized. The dissertation goals are subsequently listed and the document structure is characterized.

Chapter 2 provides a literature review of the necessary fields of study for the work. Since the main topic from which this dissertation emerged was the *Power Bank* device previously mentioned

and represented in figure 1.1. This chapter will analyze both DC to DC as well as AC to DC electrical conversion. An introduction of the different topology families will be carried out, and a direct study of the relevant ones will be performed. Beforehand, the chapter will start with an investigation of the energy storage unit, taking time to understand its parameters, and how to safely handle it, charge and discharge it.

Chapter 3 presents a theoretical characterization of the DAB converter as well as its operating principle. Different modulation strategies are studied, the converter is designed and its *open loop* functioning is validated through simulation.

Chapter 4 covers the control circuit responsible for the close loop operability of the converter, the modulation techniques are explored and its performance is evaluated. The converter's simulated operation is checked against the goals set to it.

Chapter 5 closures the dissertation contemplating the work realized and suggesting directions for future work.

Chapter 2

State of the art

From the notion of an *AC power bank* and the description of this thesis three main topics of research were identified as being relevant, these are the energy storage device, the DC-DC electric converter, and its AC-DC counterpart. As such, section 2.1 describes the principles of energy storage focusing on batteries, section 2.2 introduces electric converters dividing them between DC-DC and AC-DC conversion on sections 2.2.1 and 2.2.2 respectively. The primary objective of this chapter is to provide an overview of the main technologies/topologies used, since the objective is to select an appropriate design for the power bank, a focus will be given on detailing the advantages/disadvantages of each technology as well as their most common implementations/use cases according to the relevant literature.

2.1 Energy Storage

The worldwide net consumption of energy, has been steadily increasing since 1980, started to see a more pronounced growth from the year 2000 onwards [15]. This in conjunction with factors like: the already high production of battery-powered devices such as smartphones and laptop computers, the recent increase in the electric vehicle market demand, and the rising interest in energy storage technology to meet the electrical grid's peak power demand imply a growing necessity for energy storage. Factors such as battery energy density, specific energy and life time play an important role in the sustainability and viability of today's world.

In this section the electrochemical battery is explored as the primary method of storing energy used on this thesis. The following subsections present the necessary bibliography associated with the structure, functioning, charging methods and modeling of a battery. The battery management system is also approached in this bibliography.

2.1.1 Battery

The electrical battery is composed by one or more electrochemical cells which, through chemical reactions, are capable of producing or consuming electrical energy.

If the electrochemical cell produces energy as a by-product of the reactions that occur inside of it, it is possible to designate them as "Galvanic cells" (also called voltaic cells). If, in contrast, the cell consumes electrical energy to perform chemical reactions they are called "Electrolytic" cells.

The electrochemical cells are, in its turn, composed of two half-cells. An half-cell is where the chemical reactions, that produce or consume power, happen. Half-cells are composed by an electrode and an electrolyte. To produce an electrochemical cell one of the half-cells is a cathode and the other is an anode. The electrolyte of each cell must be connected by a salt bridge or semi-permeable membrane to let the ions of each electrolyte be replenished without letting both solutions mix.

Figure 2.1 presents a *"flow battery"* consisting of a basic electrochemical cell where its structure can clearly be seen.

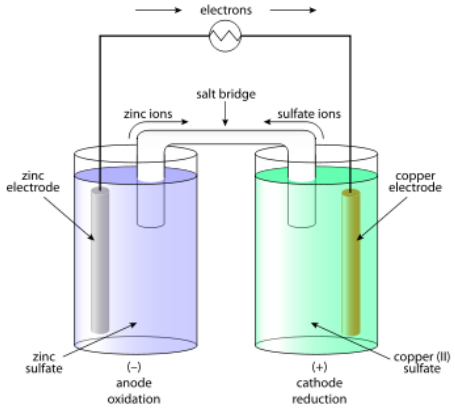

Figure 2.1: Structure of an electrochemical cell [1].

To produce current in an electrochemical cell, the half cells, ought to have a potential difference between them. This potential difference between them creates a electromotive force that tries to drive the circuit into equilibrium. The moment a close loop is established between them with an electric conductor, the electrons produced by the chemical reactions on the anode can flow from it to the cathode. Ultimately, this is what powers the devices/circuits connected to the cell. An electrochemical cell can be divided in many types, the most important ones being:

1. Primary cell - Only produces electrical energy. It is used until it runs out of energy, it can not be recharged. Galvanic cells are primary cells.

2. Secondary cell - This type of cell can, both, produce electrical energy from chemical reactions and uses electrical energy to produce chemical reactions. It is a junction of the galvanic and electrolytic cell concepts. Because of this, it can be used (discharged) and recharged.

3. Fuel cell - Produces electricity from the chemical energy of fuel. They differ from the other types because they require a continuous flow of fuel whereas, in the other types the chemicals are always present inside the cell.

2.1.2 Parameters of an electrochemical cell

Having specified the major types of an electrochemical cell. The main parameters that, allow for their distinction in terms of performance are as follows:

1. Capacity - is defined as the total amount of electricity generated due to electrochemical reactions in the battery and is expressed in ampere hours [16]. The S.I unity for capacity is A.h and it expresses the amount of hours a battery can supply a given amount of current without dipping bellow a certain terminal voltage per cell.

2. Cut-off voltage - consists of the voltage at which the cell is considered to be fully discharged. Discharging the cell further might result in harmful consequences for it.

3. State of charge (SoC) - is equivalent to the percentage of capacity that remains currently available in the cell. If the SOC is 100%, than the cell is said to be fully charged, whereas a SOC of 0% indicates that the cell is completely discharged [17].

2.1.3 Battery Model

The electrochemical battery is a nonlinear system dependant of many factors, some internal (for example SoC and state of health (SoH)) other external (like temperature and rate of discharge). There has been a great effort to model the batteries' behaviour which culminated in two big families of models, the Electrochemical model (EM) and the Equivalent circuit model (ECM) [18].

The EM is based on mathematical formulas that represent the electrochemical reactions that happen inside a battery and their consequent energy production [19]. This model can describe the macroscopic (e.g., cell voltage and current) and microscopic (e.g., potential, temperature and local distribution of chemical concentration) characteristics of the battery with great detail, however, its development is very complex and its implementation is difficult due to its high hardware resource usage which also increases cost [20]. This model is used primarily to optimize battery design and to identify its limitations, nonetheless, simulating the dynamic performance of the battery is a weak point on this method.

The ECM, contrary to the EM, is based on the dynamic characteristics of the battery. Utilizing electrical circuits such as capacitors, voltage sources and resistors, the model forms a circuit that behaves approximately like the battery that is modeled. Different models (that utilise different circuits) exist, the most simple being a ideal voltage source with a series resistor, however this model neglects the charge-voltage relation inside the battery and the non-linear phenomena that arise in the cell.

The two time constant model, presented in figure 2.2, presents an improved approximation of the short and long transient behaviour of the battery. An even more complex model proposed in [3] and represented in figure 2.3 implements further approximation and accounts for nonlinear open-circuit voltage, current, temperature, cycle number, and for storage time-dependent capacity of the battery.

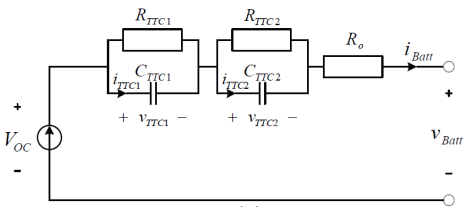

Figure 2.2

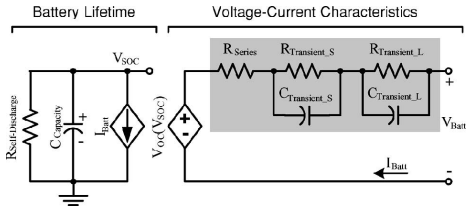

Figure 2.3

Figure 2.4: Equivalent-circuit models of an electrochemical cell: two time constant model according to ref.[2] (figure 2.2) and model proposed in ref.[3] (figure 2.3).

2.1.4 Charging Modes

The charging of a battery is dependent on the system it is implemented into. Factors like the charging time and/or performance, the charging method simplicity, cost of implementation, and its effect on the battery life cycle should be taken into account.

Several methods have been developed to answer these needs. In figure 2.5 an overview of them is presented, and a brief explanation of the main ones follows.

As it can be seen, the charging methods divide themselves between three major groups [4]. The simple charging methods are characterized by their relative inefficiency, long charging time and a tendency to shorten the service life of the battery. Their biggest advantage is simplicity and low cost of production.

1. Constant-current (CC): Accomplished by maintaining a constant current during the charging process. Its advantages are that it is relatively easy to the determine charging current, which depends only upon battery capacity and charging time. However, cumulative errors in SOC estimation algorithms may lead to problems with overcharging or undercharging [4].

2. Constant-voltage (CV): Achieved by maintaining a constant voltage while charging. Solves the overcharging/undercharging problem because the cell's voltage rises gradually through the process (decreasing current), also extends the service life of the battery when compared to the CC method. Nonetheless, it opens up the possibility for high initial charging currents that can damage the battery (especially when the initial SOC is low).

To meet more demanding charging criteria multiple optimized methods were invented. There are those who are based on waveform variation and try to combine the singular advantages of the CC and CV methods. These are:

1. Constant current-constant voltage (CC-CV): It is characterized by mixing the CC and the CV methods. First the charging occurs in CC until the voltage of the battery arrives at a certain preset level. After the method switches to CV. As the voltage of the battery evolves the current flows naturally and when it reduces to a certain value (cut-off current) the charging is complete [21]. Although being a significant improve when compared to the CC and CV methods, the last stage (CV) ends up being a very time-consuming process, it is also

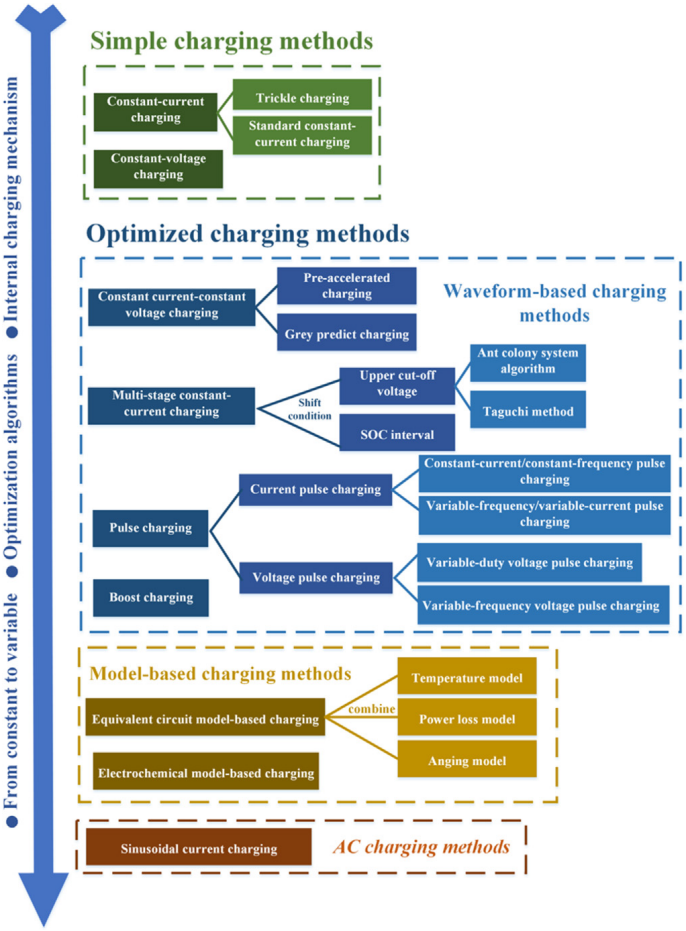

Figure 2.5: Summary of charging methods [4].

independent of battery models not distinguishing between individual cells and neglecting the internal resistance of the battery. This may lead to a surge in battery temperature and a drop in the charging efficiency.

2. Multi-step current control (MSCC): This method tries to fix the long charging times of CC-CV method, it is implemented as CC charging with multiple levels. When the first preset current is applied to charge a battery until the battery voltage reaches to the upper limit of cut-off voltage, the charging process shifts to the following preset current and repeats the previous charging process until all the preset levels of charging current are used [4]. The condition to trigger the shift in current level can also be based on SOC intervals or based on pulses off current.

3. Pulse charging: It is a technique that relies on frequent pulses of DC constant current to realise the charge of a battery. It can be implemented with fixed or variable duty-cycles and or charging current. The premise behind it is that, during the off time interval of each duty cycle, the battery can rest (balance ion concentration) effectively lowering (or even neutralizing) polarization voltage. This in turn, leads to lower charging times, as the average

charging current can be much greater than in the previous charging methods. The cost of this method is that it tends to generate more heat (when compared with CC-CV charging) and therefore, tends to decrease the useful life of a battery [22].

4. Boost charging: Combines the advantages of CV charging (it's low charging time) with the CC-CV method. The latter is used counteract the battery degradation provoked by the very high currents associated with CV charging. The implementation is based on the use of high charging current (during a short period of time) for low SoC batteries and then switch to normal CC-CV charging [23].

Other types of optimized charging are the model-based methods. These lean on the equivalent circuit model (ECM) or on the electrochemical model (EM) of the battery to control the voltage/current supplied to the battery.

1. ECM based charging: This method relies on the ECM model of the battery to decide the charging current employed (and its waveform). After having modeled the battery an optimization algorithm is generated with constraints such as: targeted SoC, battery temperature, efficiency of charge and total energy loss, maximum charging current and aging effects. According to the constraints used, or the weigh they possess on the function, the charging method assumes different names (Electrical-thermal-aging model, Equivalent circuit/power loss model, Equivalent circuit/temperature model) [24, 25, 26].

2. EM charging: Is based on the EM model of the battery, and uses it to maximize charging current while restraining unwanted reactions inside of the battery [27]. It can store more charge in a cell than in the CC-CV method, using the same charging rate [4].

At last the AC charging method, explicitly the sinusoidal-ripple-current (SRC) method, is implemented with a sinusoidal current to which a DC offset is added. The objective is to charge the batteries at a frequency that reduces the frequency dependant impedance present in the battery. Although the recent interest in this method, there is not a consensus in whether or not SRC presents improvements when compared to other methods, with some studies claiming there is no obvious advantages to using this method compared to the CC-CV [4, 28, 29, 30].

2.1.5 Battery Management System

As previously discussed in the section 2.1.1, a battery can be composed by the association of multiple electrochemical cells. Regardless if they are connected in parallel, series or a mix of both, the connection of multiple cells demands certain precautions.

These precautions are tied to a myriad of factors such as individual differences between cells in terms of ageing rate, variances in parameters and uneven temperature distribution during operation. In fact even cells from the same model and manufacturer, recently made, produced in the same batch and never used have slightly different parameters [31]. Also, every connection between cells is unique, and therefore different capacitance and resistance at the welding points and wires are to

be expected. Adding these effects all together culminates in different performance of each cell in a battery. This could lead to differences of voltage between cells (danger of short circuits and/or irregular temperature increase) and depletion of certain cell's SoC first than others. It is, therefore, important to balance the cells between each other and manage their thermal variation within the pack (as this can exacerbate the inconsistencies and lead to problems).

Other danger of cell association is that one might fail, and in doing so, lead to the failure of other cells or even to hazardous situations (short circuits and fire, among others). Means of diagnosing faults and safely disconnecting cells are thus, a necessity.

The unit responsible to perform all the upwards mentioned functions (cell balancing, thermal management and fault diagnosis) is the battery management system (BMS). Apart from this, the BMS should also be responsible for the estimation of the battery SoC.

2.1.5.1 Methods of SoC estimation

SoC estimation is a necessary attribute of the BMS, a good estimation method can prevent over-charging, protect the battery and the device that is being supplied. A good SoC estimation method can also provide information for the BMS, opening up the possibility for battery control strategies, saving energy. SoC estimation is complex and difficult because there is no direct way of measuring it, it is estimated using the measurable parameters of the battery (such as voltage and current) and sometimes a battery model. Figure 2.1 represents a summary of the different SoC estimation methods.

Table 2.1: Classification of SoC estimating mathematical methods [14].

Categories	Mathematical methods
Direct measurement	(i) Open circuit voltage method (ii) Terminal voltage method (iii) Impedance method (iv) Impedance spectroscopy method
Book-keeping estimation	(i) Coulomb counting method (ii) Modified Coulomb counting method
Adaptive systems	(i) BP neural network (ii) RBF neural network (iii) Support vector machine (iv) Fuzzy neural network (v) Kalman filter
Hybrid methods	(i) Coulomb counting and EMF combination (ii) Coulomb counting and Kalman filter combination (iii) Per-unit system and EKF combination

When multiple electrochemical cells are connected to form a battery, the SoC of each cell might not be the same. To estimate each cell SoC is a task that has complexity and computational/hardware cost proportional to the quantity of cells, as such, it is often impractical.

In order to overcome this difficulties it is possible to [31]:

1. Assume all the cells to have the same SoC and apply the estimation method to the all pack. This is only possible if cells have very similar characteristics.

2. Chose one or more reference cells in the battery and measure their SoC. This method assumes that this cells are representative of the whole pack or of a portion of him.

3. Use a mean of all cell's voltage and temperature to estimate a mean SoC of the battery. This is done using an algorithm with high bandwidth, then with a lower bandwidth algorithm the difference between the SoC of each cell and the mean is calculated.

2.1.5.2 Methods of Cell Balancing

Cell balancing can be achieved through dissipative or non-dissipative methods. Dissipative methods are typically less expensive, more simple and reliable than the non-dissipative methods. This method implies the use of a resistor in connection with the cell that needs balancing, switched shunt resistors are the most common technique [31]. In spite of the advantages mentioned, dissipative methods are slow (compared to non-dissipative ones), promote energy loss and heat generation.

Non-dissipative methods are without a doubt more energy efficient than their counterpart utilizing inductors, capacitors, power converters and/or transformers to transfer energy between cells. They achieve energy transfer from cells with greater SoC to more discharged cells extending the life of each battery cycle, however the complexity and cost of this designs greatly surpasses that of the dissipative methods.

2.2 Electric converters

For some decades now, electric converters have been used and developed across a wide range of applications. From a more industrial utilization like electrical machine drives, Vehicle-to-Grid (V2G) and microgrid technologies to common household appliances such as telephone chargers and television power supplies.

The electric converter is by definition a device that, through internal action, changes the original properties of the electrical energy he is supplied with. Its classification is dependant of this change, and as such, makes them divisible in dc-dc, dc-ac, ac-dc and ac-ac converters.

2.2.1 DC-DC Converters

The DC-DC converters receive direct current at its input, and output also, direct current. Depending on the voltage gain between the input and output they can be characterized as being step-up (output voltage is greater then input) or step-down converters (when the contrary happens).

For a DC-DC converter there are three major modes of operation, these are linear mode, hard switching mode and soft switching mode [32]. Figure 2.6 provides an illustration of the these three major types and subsequent classifications.

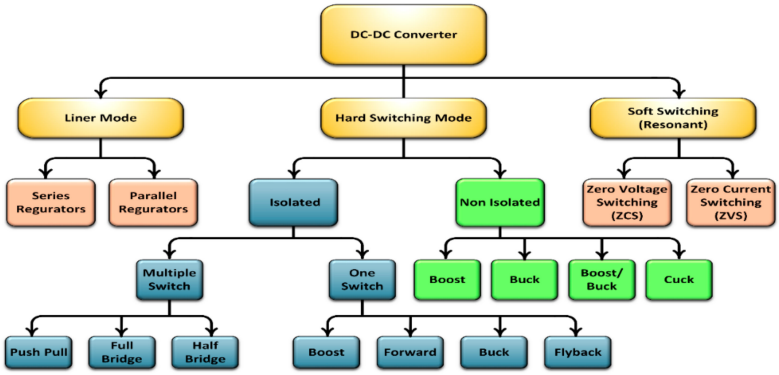

Figure 2.6: Classification of DC-DC converters [5]

The DC-DC converters said to be of linear mode type are without a doubt the most simple ones, although they present useful attributes such as low noise and good regulation, they are very inefficient and their zone of operation is very limited (commonly restricted to low power applications) . Therefore, they will not be further discussed on this work.

Hard switching-mode converters (like the push pull, full bridge and the flyback) present better efficiency and greater complexity than the linear mode ones. They are inherently switching mode converters, which means that they utilize transistors that switch between their off and saturated state, minimizing the dissipated power to switching losses and lower conduction losses (than the linear mode converters) associated with the saturated state of the transistor. However due to the switching activity EMI emissions increase and output filters may be required to lower current ripple [33]. The hard switching classification refers to the fact that the transistors switch between states with non-zero current and or voltage. This is a disadvantage since it potentiates switching losses, device stress and EMIs, since dissipated power associated with commutation losses is proportional with switching frequency this determines that the maximum frequency of operation is conditioned and should tend to be lowered. This leads to bigger inductors, to compensate, and increases the overall size and weight of the converter [34].

Soft switching converters overcome the difficulties associated with the commutation losses of the Hard switching converters by controlling the current or voltage at the transistors to be zero during the commutation. Therefore, they can be classified as zero current switching (ZCS) or zero voltage switching (ZVS). This techniques lead to a greater efficiency, less stress on the semiconductors during commutation, lower overall EMI, capability of working at higher frequencies,

wider range of DC input voltages and can be built with smaller transformers and inductors (which in turn imply less weight) [32].

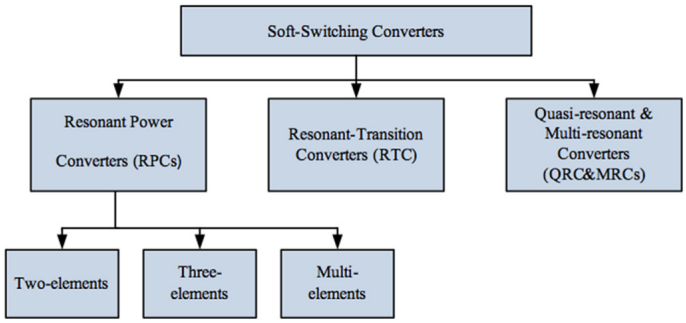

Figure 2.7: Soft switching converters family [5].

Due to their suitable applicability in this work section 2.2.1.1 presents further detail on soft switching converters.

2.2.1.1 Soft Switching converters

Regardless if soft switching converters operate in ZVS or ZCS, the principles behind their operation allow us to classify them into three different families: Resonant power converters (RPCs), resonant transition converters (RTCs), quasi-resonant converters (QRCs) and multi-resonant converters (MRCs) [5].

QRCs are types of converters that utilize an LC resonant element to achieve ZVS or ZCS in one semiconductor. If ZVS is desired, the inductor should be placed in series with the switch and the capacitor in parallel or vice versa for ZCS. The drawbacks associated with them are that they can only achieve ZVS or ZCS for either the switch or the rectifying semiconductor and as such the power losses at high frequency have to be considered. MRCs have been proposed to overcome these disadvantages, they build on QRCs adding another resonant component (inductor or capacitor) and connecting them in series or parallel with the rectifying semiconductor, effectively incorporating them in the resonant network and allowing ZVS or ZCS on both semiconductors.

RTCs utilize four auxiliary devices to achieve soft switching. Two are used as reactive elements the other two as switches. Depending on the arrangement of the elements the switches can exhibit zero-voltage transition (ZVT) or zero-current transition (ZCT) [35].

RPCs have three stages: the control switch network (CSN), the resonant tank network (RTN), and the diode rectifier with a low pass filter (DR-LPF) (as can be seen in figure 2.8). The High frequency (HF) transformer is not required, but when employed provides galvanic isolation between stages. The CSN stage is composed of a switching network (normally, either full bridge or half bridge design [5]) that will invert the voltage of the input DC power supply creating a square voltage wave with the same frequency as the commutation of the switches. This square wave is carried on to the RTN stage where the resonant components are present (inductor and capacitor), depending on the way the components are connected (series, parallel, series-parallel) and on the

number of components the behavior will also change. The last stage (DR-LPF), should be conformant with the behavior of the RTN stage to produce the output DC waveform. This stage presents an effective load resistance equal to the ratio between the voltage and the current waveforms at the output of the RTN stage.

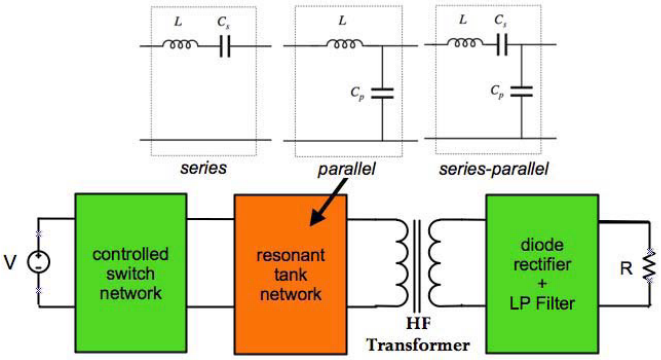

Figure 2.8: Structure of the resonant power converter [6].

2.2.1.2 Dual active bridge (DAB) IBDC

The dual active bridge (DAB) isolated bidirectional dc-dc converter (IBDC) is a *proven technology* for medium power applications [7, 36]. This design is shown on figure 2.9 and is commonly used in energy storage applications since it can continue to operate even when the voltage of the energy storage device changes due to charging and discharging.

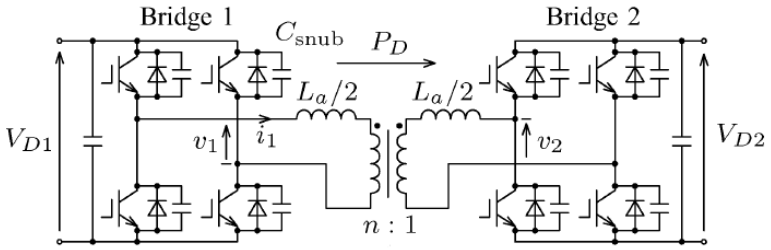

Figure 2.9: Dual active bridge isolated dc-dc converter [7].

The use of the transformer in between both full bridges ensures galvanic isolation and/or voltage matching [7]. The control is usually achieved through phase shift modulation, actuating on each full bridge and producing a square voltage wave at the terminals of the transformer. Depending which voltage wave (v_1 or v_2) leads, the power flow will be changed securing the bidirectional energy flow. Despite needing snubbers (in this case capacitors) parallel to the transistors to reduce switching losses and damp out overvoltage, it is possible to achieve ZVS commutation under certain conditions.

2.2.1.3 Bidirectional CLLC resonant converter

The CLLC resonant converter can be seen on figure 2.10, this type of converter falls into the RPC classification. In spite of being completely snuberless the switching losses are minimized because the converter can operate under soft switching conditions for both the primary inverting switches and the secondary rectifiers [37]. In fact, the primary inverters switch with ZVS and the rectifiers with ZCS, this happens for both directions of power flow (due to the symmetric resonant tank) and is optimal for minimizing switching losses in MOSFET equipped bidirectional converters (BDC) [38].

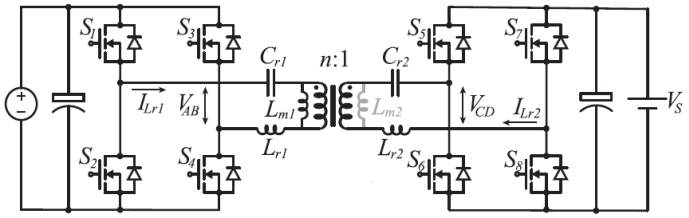

Figure 2.10: Topology of CLLC resonant converter [8].

The symmetrical resonant tank also guarantees that the switch control algorithm can be applied to the converter without reference to power flow direction. Traditionally the control is done in three parts: power flow direction control done with a dead band control, switching control done with pulse frequency modulation (PFM) conjugated with a PI controller and soft-start control [37, 39].

Even though the converter is able to operate with a wide voltage range at the input, the different gain requirements during the charging and discharging of a battery often lead to an undesirably large switching frequency range and, as such, some implementations with asymmetric resonant tanks or different control methods to improve performance are proposed in works like [39, 8].

2.2.2 AC-DC Converters

Due to the ever growing need of AC-DC converters for applications such as microgrids, V2G technologies and EV production several topologies have been proposed, with variable performance, cost and complexity, in order to answer to different problems in the best possible way.

In figure 2.11 a general classification of the AC-DC converters can be seen, a brief description of every family will be given and after two relevant AC-DC converter topologies will be presented and further explained in detail.

Of the four families the most basic [9] is the voltage source bridge converter (VSC). The full bridge configuration uses more control inputs being more complex and expensive than the half bridge, however it generates less harmonic distortion (and as such requires a smaller filter), the voltage stress at the switches is also lower which enables the use of lower rated switches (reduced cost). VSC operates in buck mode while used as an inverter and as boost mode in rectifier operation, this topology is commonly used for low voltage (less than 500V) grids.

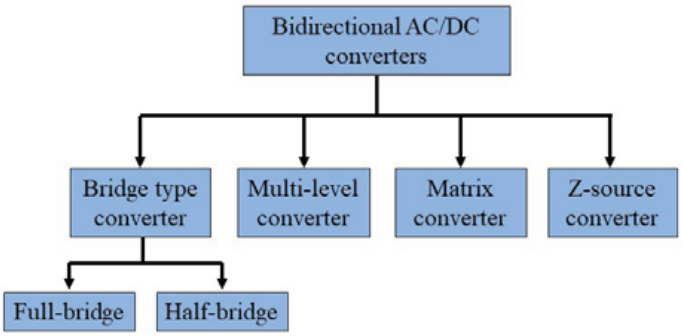

Figure 2.11: Classification of AC-DC Converters [9].

The multi-level converter is the name given to the VSC converters with three or more levels of rectification. They are more complex than the simple VSC and provide less harmonic distortion, acoustic noise, electromagnetic interference (EMI) and lower voltage stress on components. They can be further classified into diode-clamped, flying capacitor and cascaded H-bridge converters depending on their method to shift DC voltage levels.

The matrix converter is ideal for applications with hugely varying DC voltage and are commonly used in medium voltage applications [9]. This type of converter has a topology very similar to the VSC, except that it utilizes switch devices arranged to be bidirectional, this feature provides them with better controlled rectification than the VSC.

The impedance source (or Z-source) converter has the ability to vary the AC voltage independently of the of the DC voltage magnitude creating a converter with improved buck-boost capability. This converter employs an impedance network between the switch network and the power source.

2.2.2.1 Voltage Source Converter (VSC)

The voltage source converter is commonly implemented as single-stage seen on figure 2.12, or on its dual-stage form. The dual stage form employs a separate DAB for dc-dc conversion connected in parallel with the capacitor, frequently employing a high frequency transformer to provide galvanic isolation, this form is often preferred for energy storage applications due to its easier control design, better line-disturbance rejection [40]. This topology is capable of bidirectional power flow and power factor correction (PFC) and can be implemented with resonant tanks to achieve soft-switching conditions.

The control of the first stage is usually realized with vector control strategy (VCS) [40].

2.2.2.2 Z-source converter

The Z-source converter can be seen on figure 2.13 in a three phase topology. This type of converter is very advantageous for grid interfacing applications due to its ability to secure bidirectional power flow for different levels of voltage [9]. The impedance network varies with different use

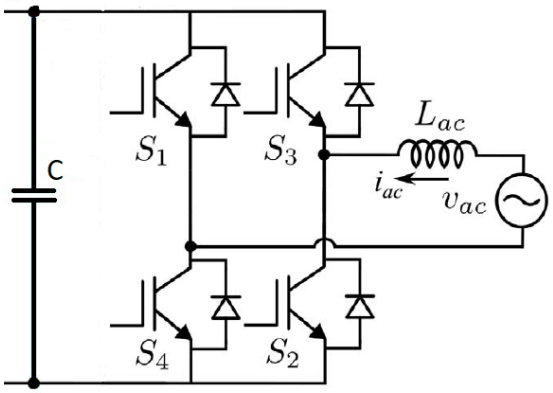

Figure 2.12: Bidirectional single stage voltage source converter [10].

cases, normally with energy storage applications using batteries a quasi-resonant impedance network is used to provide continuous input current. This comes with the added benefit of providing soft switching conditions and therefore power loss reduction. Compared to the use of the VSC for energy storage applications, this converter has the advantage of being buck-boost for both power flow directions.

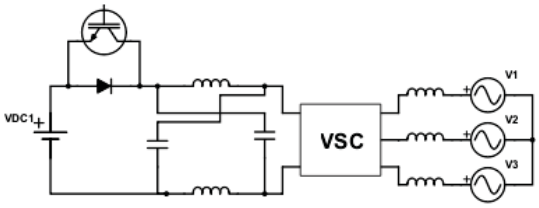

Figure 2.13: Bidirectional Z-source converter [9].

2.2.3 Galvanic isolation

Galvanic isolation happens when there is no direct electrical path, for energy to flow, between two individual parts of the circuit. This allows each part of the circuit to have grounds with different potentials preventing ground loops. Multiple methods are employed to achieve galvanic isolation, the use of transformers and capacitors (in series) and opto-isolators are well established. However, for the purpose of this thesis, only the transformer will be analysed due to its predominance in electrical converters.

In an electrical transformer the energy is exchanged between the primary and secondary through magnetic induction, and as such DC values don't conduct between both. Since most transformers employ an electrostatic shield (Faraday shield) between both windings common-mode noise and transients are reduced [11].

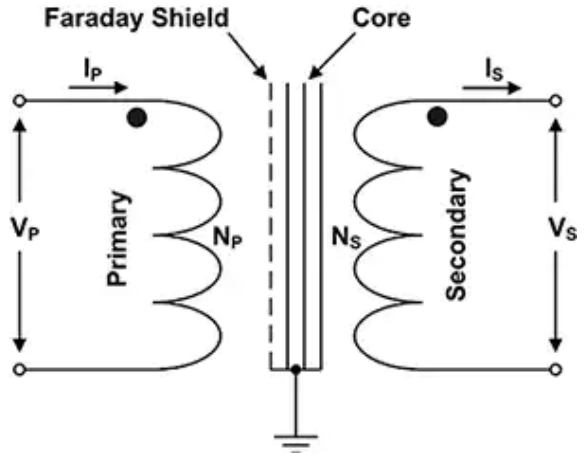

Figure 2.14: Schematic of a simple transformer [11].

2.2.4 Semiconductor devices

If we were to classify semiconductors in terms of build material, three major options could be found available on the market, this are: *Silicon (Si)*, *Silicon Carbide (SiC)* and *Gallium nitride (GaN)*.

Due to many decades of development, fabrication, and optimization of a large variety of Si devices and a large material abundance, high manufacturing capability, and extremely low cost, Si is still the most used element for the production of power semiconductor devices [41]. However, *SiC* and *GaN* semiconductors have been seeing significant improvements in both material growth and reliability as of late; they have been and are expected to replace the common *Si* semiconductor in many applications for their promising high-power, high-temperature, and high-frequency capabilities [41].

Analyzing the *Si* based transistors, it is possible to find three major types: the BJTs, MOSFETs, and the IGBTs.

The BJTs are not commonly utilized presently due to their low switching frequencies, they are controlled by current and they possess relatively low on-state resistance.

The IGBTs are largely utilized for high power applications, they are characterized by having a generally low on-state resistance, and being able to operate at high frequencies with low conduction losses. If current flow should flow through an IGBT in both directions, an antiparallel diode is needed.

The MOSFETs can operate at even higher switching frequencies than the IGBTs, they have an intrinsic antiparallel diode that ensures both current flow directions. The trade-off is their higher on-state resistance which makes it not applicable for high power applications.

Chapter 3

DAB converter

The dual active bridge (DAB) dc-dc converter, is a proven technology and a popular choice for applications that require bidirectional power flow [42], numerous advantages inherent to this topology can be listed. Its decrease number of devices, capability for soft-switching commutation, low cost, high efficiency, to name a few, make it attractive to applications where power density, cost, weight and reliability are considered to be critical factors [43]. Such objectives, greatly align with the focus of this dissertation.

In this chapter, a study of the converter's operation in steady state will be presented and common modulation techniques will be explored. The mathematics behind the converter functioning will serve as the backbone of the chapter and, therefor, will be used for component design.

3.1 Steady state analysis

The DAB converter, shown in figure 3.1, consists of two full bridge voltage sources connected through a high frequency transformer, that provides galvanic isolation, a coupling inductor L and capacitors C_a and C_b which provide current filtering for the corresponding voltage sources.

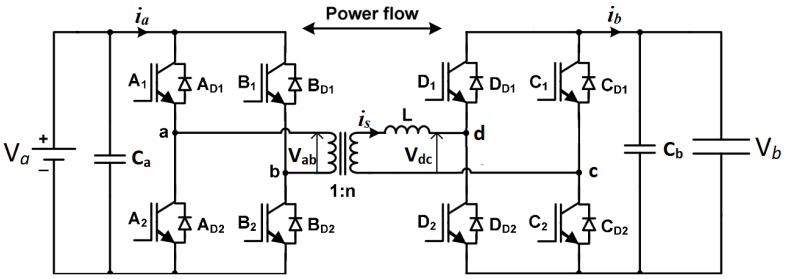

Figure 3.1: Schematic of the DAB DC-DC converter [12].

In order to simplify the analysis of the converter functioning:

1. all loses will be neglected,

2. the transformer is assumed as being ideal (no magnetizing induction or parasitic capacitance),

3. supply voltages are considered to be constant [44].

According to this simplifications the schematic can be further simplified into the following one represented on figure 3.2.

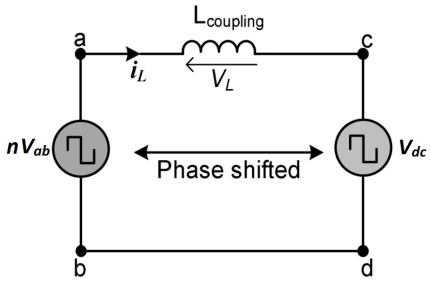

Figure 3.2: Simplified equivalent circuit [12].

The possible states for V_{ab} are,

$$V_{ab} = \begin{cases} +V_a & A_1, B_2 \text{ on}, A_2, B_1, \text{off}. \\ 0 & A_1, B_1 \text{ on}, A_2, B_2, \text{off}. \\ 0 & A_2, B_2 \text{ on}, A_1, B_1, \text{off}. \\ -V_a & A_2, B_1 \text{ on}, A_1, B_2, \text{off}. \end{cases} \tag{3.1}$$

In the same manner, the result of the switching states of C and D transistors is $+V_b$, 0 , $-V_b$.

As such, the voltage V_L across the inductor will be dictated as

$$V_L(t) = n \cdot V_{ab}(t) - V_{dc}(t) \tag{3.2}$$

generating a current

$$i_L(t_1) = i_L(t_0) + \frac{1}{L}\int_{t_0}^{t_1} V_L(t)\,dt \quad \forall\, t_0 < t_1 \tag{3.3}$$

at the time instant t_1, when t_0 is the initial instant with $i_L(t_0)$ as initial condition.

Therefor, instantaneous power consumed/generated by the voltage sources is

$$p_1(t) = n \cdot v_{ab}(t) \cdot i_L(t) \tag{3.4}$$

$$p_2(t) = v_{dc}(t) \cdot i_L(t) \tag{3.5}$$

The average power over one switching cycle, T_s, is given by,

$$P_1 = \int_{t_0}^{t_0+T_s} p_1(t)dt \tag{3.6}$$

$$P_2 = \int_{t_0}^{t_0+T_s} p_2(t)dt \tag{3.7}$$

Maintaining the assumption of a lossless converter,

$$P_1 = P_2 \tag{3.8}$$

Thus, the power level of the DAB converter is typically adjusted using the following parameters [44]:

- phase shift Φ, between V_{ab} and V_{dc} with $-\pi < \Phi < \pi$
- duty cycle, D_1 and D_2 from V_{ab} and V_{dc}, respectively, between 0 and $\frac{1}{2}$
- switching frequency f_s

3.1.1 Modulation methods

3.1.1.1 Phase shift Modulation

In typical phase shift modulation (PSM), also called square-wave modulation [12], each bridge is controlled in order to produce a fixed frequency square wave with a 50% duty cycle at the corresponding *ab* or *cd* terminals.

The two square-waves are then phase shifted with respect to each other. Changing the phase shift angle will subject the inductor to different voltage conditions allowing for the control of both power flow direction and its magnitude. Power flows direction is from the leading bridge to the other. The idealised waveforms for the converter, having power flowing from the power supply V_a to V_b, are represented on figure 3.3.

The voltages generated by the full bridges v_{ab}, v_{dc} are square waves shifted by an angle denoted as Φ and a time interval of $\frac{d*T_s}{2}$, where T_s is the switching period and d is the controlled duty ratio.

Focusing on the figure, the various time instants are as follows:

- $t_0 \rightarrow t_1$: At t_o transistors A_1 and B_2 are turned on while their anti-parallel diodes are conducting, which develops voltage equal to V_a on the primary. Transistors C_1 and D_2 are conducting and, therefor, at the secondary voltage equals $-V_b$. The current across the inductor is forced to increase due to the voltage difference.
- $t_1 \rightarrow t_2$: At t_1 transistors A_1 and B_2 continue on while C_1 and D_2 are switched off with ZVS. Since current at turn-off is high, to benefit from soft-switching, a turn-off snubber is generally advised. The current from transistor C_1 is transferred to diode C_{D2}. Similarly, transistor D_2 current is transferred to D_{D1} under ZVS. The voltage across the secondary changes to V_b and i_L continues to increase until it reaches peak value at t_2.

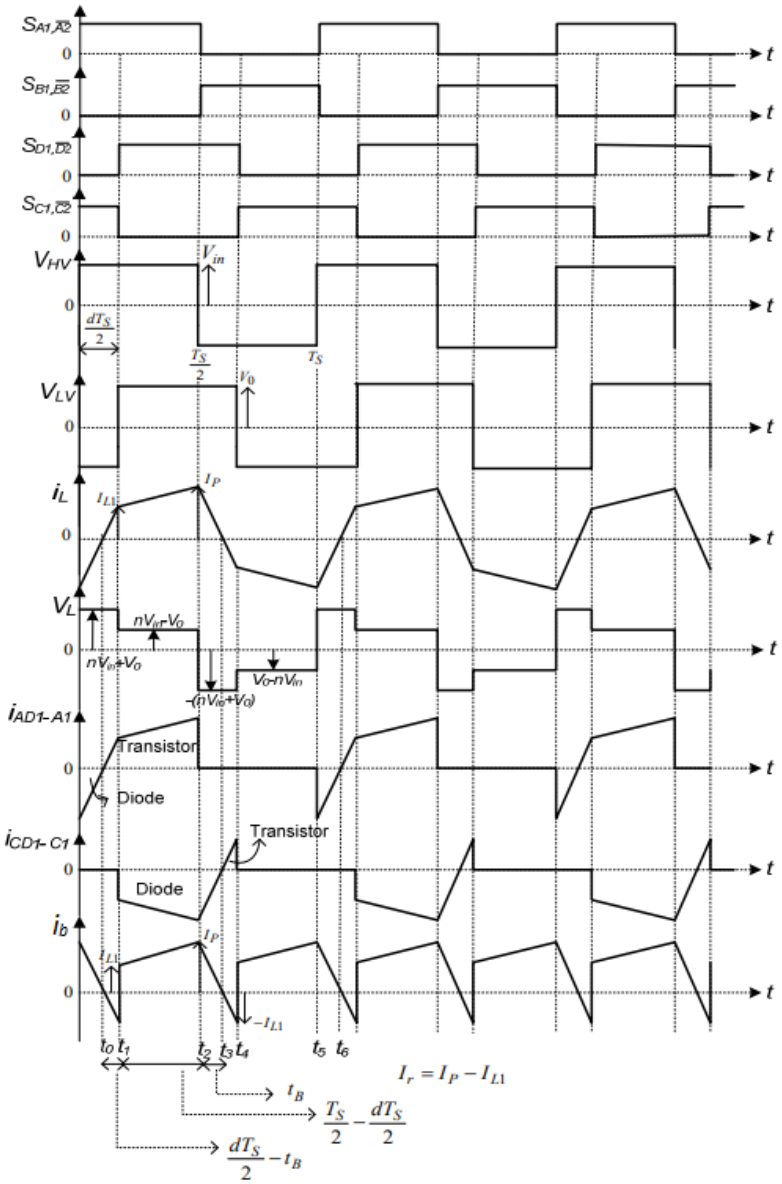

Figure 3.3: Idealised waveforms of the DAB converter [12].

- $t_2 \rightarrow t_3$: At t_2 transistors A_1 and B_2 turn off under ZVS, their current transfers for the diodes A_{D2} and B_{D1} making them conduce. The primary voltage is clamped to $-V_a$. On the secondary side, diodes D_{D2} and C_{D1} continue conducting, this results in a decrease in inductor current until it hits zero and starts to charge in the opposite direction. At t_3, the aforementioned cycle is repeated from t_3 to t_6, with the opposite set of bridge transistors and diodes.

If the power flow were to be inverted, than V_{dc} would lead V_{ab}, and the current i_L and i_0 would be mirrored across the time axis.

Based on figure 3.3 and especially the V_L waveform, the following equation can be derived:

$$I_P = \frac{T_s}{4L} \cdot [V_b(2d-1) + nV_a] \tag{3.9}$$

$$I_{L1} = \frac{nV_a + V_b}{L} \cdot \frac{dT_s}{2} - I_P = \frac{T_s}{4L} \cdot [nVa(2d-1) + V_b] \tag{3.10}$$

$$I_b = \frac{T_s nV_a}{2L}(d - d^2) \tag{3.11}$$

From equation 3.11, the following relation between I_b (here denominated as output current I_o for simplicity) and duty ratio d:

Figure 3.4: Normalised average output current vs Duty ratio [12].

3.1.1.1.1 ZVS condition

For the converter to achieve low to virtually loss-less switching characteristics, the following conditions must be met [12]:

- Anti-parallel diode is conducting at device's turn-on.
- Minimum current flow through the device is positive at turn-off.

Furthermore, in practice for ZVS to occur the inductor current must always be large enough to charge/discharge the device output capacitance's at the switching instants [12]. As such, depending on the physical properties of the transistor and the operation of the converter, there might be conditions in which the ZVS will be imperfect. For such situations, the use of a snubber to further minimize losses should be studied.

Assuming power flowing from the primary to the secondary, the current at both sides during the switching instant must be greater than zero to achieve ZVS. Inspired by figure's 3.3 waveforms

and using equations 3.9 and 3.10,

$$I_P = \frac{T_s}{4L} \cdot [V_b(2d-1) + nV_a] \geq 0 \tag{3.12}$$

$$I_{L1} = \frac{T_s}{4L} \cdot [nVa(2d-1) + V_b] \geq 0 \tag{3.13}$$

having $V_b' = \frac{V_b}{nV_a}$, where V_b' represents the normalised voltage conversion ratio. For this case, equation 3.12 is met [12] if the following limiting condition is met:

$$I_{L1} \geq 0 \tag{3.14}$$

Keeping in mind that the ideal waveforms and equations used represent the case where $V_b' < 1$ (buck mode), than ZVS conditions must also be derived for $V_b' > 1$ (boost mode). In practice, this will translate to an interchangement of the expressions for the currents at the primary and secondary switching instants [12].

Therefor, the limiting condition will now be:

$$I_P \geq 0 \tag{3.15}$$

At last, developing equations 3.14 and 3.15

$$\begin{cases} d \geq 0.5 - \frac{V_b'}{2}, V_b' < 1 \\ d \geq 0.5 - \frac{1}{2V_b'}, V_b' > 1 \end{cases} \tag{3.16}$$

3.1.1.2 Quasi-Square-Wave modulation

Although the various advantages of phase shift modulation, previously discussed in chapter 3.1.1.1, under light loads the inductor might not be sufficient to discharge the devices snubbers and/or output capacitance, leaving the transistors subject to hard switching [12]. The Quasi-square-wave (QSW) modulation, appears as a way to improve the soft-switching region of the transistor.

A great similarity between the PSM and QSW techniques can be noted, in fact, QSW modulation builds on PSM adding a short dead-time on the voltage waveform of the *ab* or *cd* terminals.

The dead-time can be applied on either side of the transformer or on both, and is achieved through phase shifting the waveforms that drive the gates of the bridge's diagonal transistors. In this mode only one transistor will turn of at any one time [12]. This phase shift is represented as δ_x where x is either a or b depending on the corresponding bridge.

Figure 3.5 represents the idealized waveforms for the converter when quasi-square-wave operation is present on both active bridges.

Analysing the waveforms and comparing them with the ones from the PSM method, the adding of 4 time intervals, marked in green, are detected.

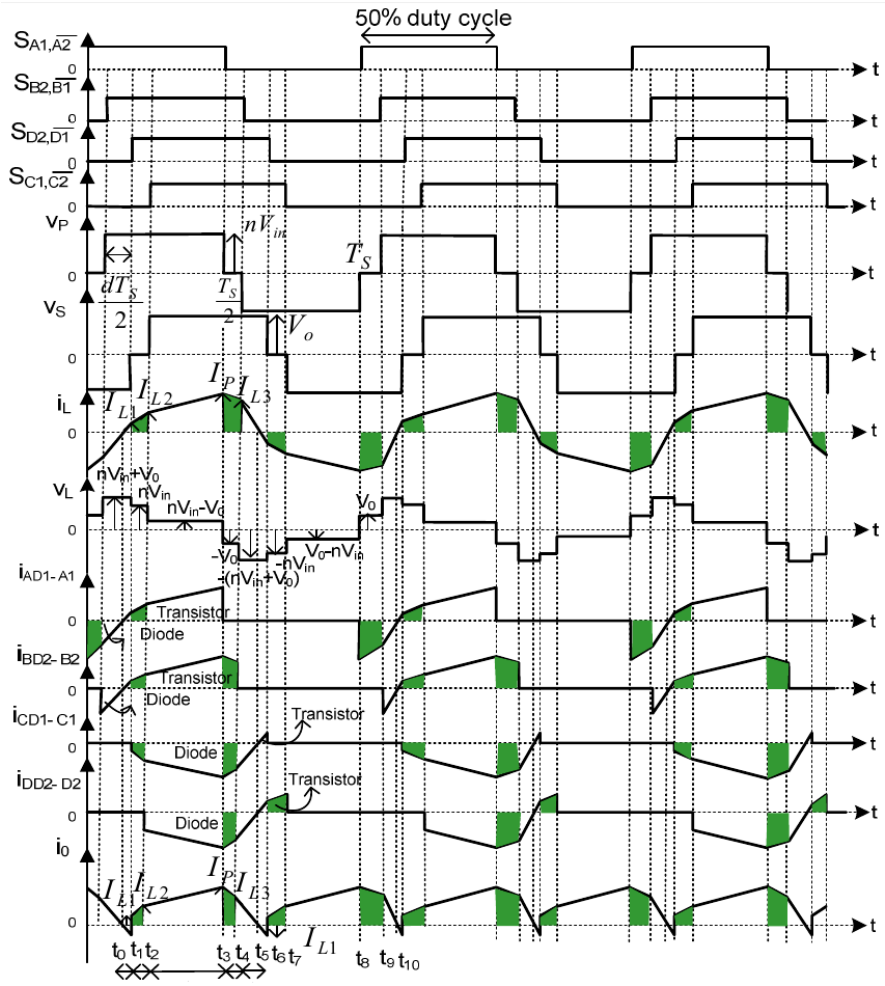

Figure 3.5: Ideal waveforms for quasi-square-wave applied on transformer primary and secondary [12].

- $t_1 \rightarrow t_2$: at t_1 transistor D_2 is switched off under ZVS and its current is transferred to D_{D1} under ZVS. Current freewheels through D_{D1} and C_1. On the primary, A_1 and B_2 continue to conduct, voltage is clamped to V_a and current increases to a peak of I_{L2}.

- $t_3 \rightarrow t_4$: at t_3 transistor A_1 is turned off under ZVS and its current transfers to A_{D2} under ZVS. The current, now, freewheels through B_2 and A_{D2}. On the secondary, D_{D2} and C_{D1} continue to conduct and the voltage is maintained at V_b, current i_L falls to a peak of I_{L3}.

Time intervals $t_6 \rightarrow t_7$ and $t_8 \rightarrow t_9$ are similar to $t_1 \rightarrow t_2$ and $t_3 \rightarrow t_4$, except that the diodes or transistors are switched, inside the corresponding leg.

The dead-time increases the average output current of the converter, improving its efficiency and ZVS operation at the expense of increase conduction losses [12].

Similarly to section 3.1.1.1, the following equations can be derived from the waveforms seen on figure 3.5:

$$I_{L1} = \frac{T_s}{4L} \cdot [nV_a(2d - \delta_a - 1) + V_b(1 - \delta_b)] \tag{3.17}$$

$$I_{L2} = \frac{T_s}{4L} \cdot [nV_a(2d + \delta_a + 2\delta_b - 1) + V_b(1 - \delta_b)] \tag{3.18}$$

$$I_{L3} = \frac{T_s}{4L} \cdot [nV_a(1 - \delta_a) + V_b(2d + \delta_b - 1)] \tag{3.19}$$

$$I_b = \frac{nV_aT_s}{2L} \cdot (d - d^2 - d\delta_a - d\delta_b + \frac{\delta_a + \delta_b}{2} - \frac{\delta_a^2 + \delta_b^2}{2} - \frac{\delta_a\delta_b}{2}) \tag{3.20}$$

3.1.1.2.1 Effect on ZVS

Due to the relatable nature between the QSW and SQW modulation techniques, in which SQW presents itself as an explicit case of QSW modulation with $\delta_a = \delta_b = 0$. Conditions analogous for soft switching occurrence can be derived, namely,

$$\begin{cases} I_{L1} \geq 0 \ , V_b' < 1 \\ I_{L3} \geq 0 \ , V_b' > 1 \end{cases} \Leftrightarrow \begin{cases} d \geq 0.5 - \frac{\delta_a}{2} - \frac{V_b'}{2}(1 - \delta_b) \ , V_b' < 1 \\ d \geq 0.5 - \frac{\delta_b}{2} - \frac{1}{2V_b'}(1 - \delta_a) \ , V_b' > 1 \end{cases} \tag{3.21}$$

From the aforementioned conditions, the following plots can be charted to translate the improvement in soft switching capability of the converter with respect to $\delta = \delta_a = \delta_b$, duty ratio d and conversion ratio V_b'.

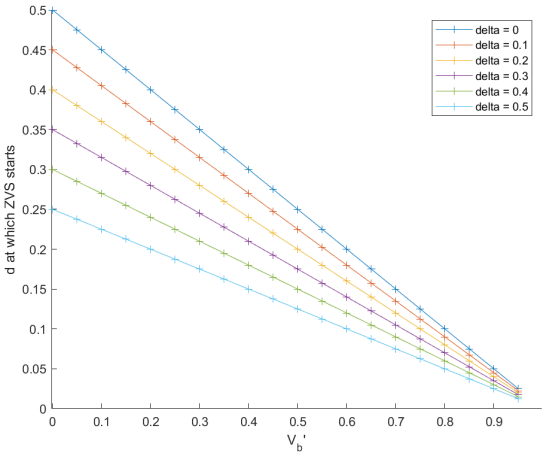

Figure 3.6: (a)

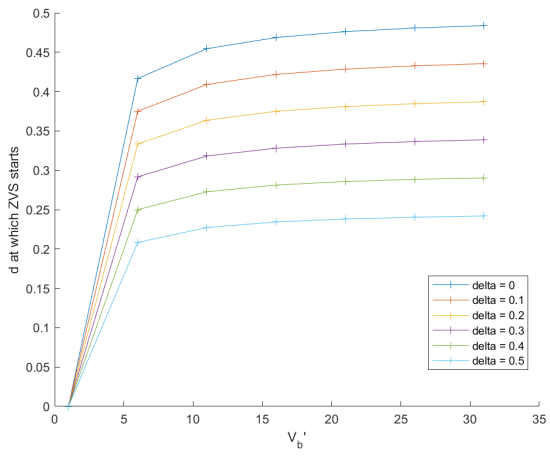

Figure 3.7: (b)

Figure 3.8: Duty ratio d above which ZVS starts to occur under buck 3.6 or boost 3.7 mode.

From figure 3.8, it is easy to notice that increasing δ_a, δ_b improves soft switching capabilities of the converter. Further more, using equation 3.20 in a normalised form, figure 3.9 can be charted implying a clear relation between the increase of δ_x and the shift of the peak output current to lower duty ratios d.

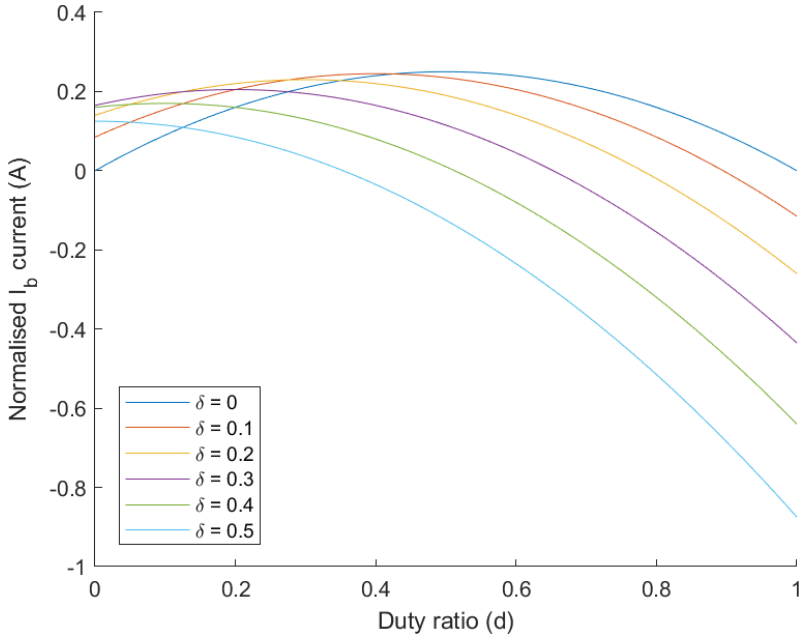

Figure 3.9: Normalised average output current as a function of duty ratio for different values of δ [12].

Summing up, QSW modulation extends the soft switching region of the converter through δ_x. An increase in δ_x will translate in a bigger soft switching region of operation; however it also performs a shift of the converter's power curve, since I_b current is independent of output voltage. In general, with a higher δ_x a higher power transfer can be achieved under light-loads, increasing efficiency [12]. Nonetheless, according to reference [12], increasing δ_x also increases peak and RMS current that circulate through the inductor; therefor, a trade-off between conduction and switching losses must be considered.

3.2 Requirements

In order to size the components necessary for the converter to function, it is first necessary to understand the operating conditions it will be subject to. Section 1.2 started the work leaving some objectives that must be accomplished by the converter. As such, they are considered as requirements.

The INR21700-40T is a lithium-ion rechargeable cell available on the market that was found to have good capacity and energy density. Its main characteristics are:

- Standard capacity = 4000 mAh
- Nominal Voltage = 3.6V
- Charged Voltage = 4.2V
- Discharge cut-off voltage = 2.5V

- Diameter = 21.22 mm

- Height = 70.30 mm

Since the battery pack must have autonomy of $1.5kWh$. Using the individual cell characteristics, aforementioned,

$$E_{cell} = C_{cell} \cdot V_{nominal} = 4000e^{-3} \cdot 3.6 = 14.4Wh \tag{3.22}$$

and the number of cells necessary at the battery pack to achieve the desired autonomy is given by:

$$\text{Number Cells} = \frac{1.5 \cdot 10^3}{14.4} \approx 105cells \tag{3.23}$$

Upon consideration it was decided, that increasing the cell count to 110 in order to make a $10x11$ cell battery pack, would both meet the desired requirements while allowing for a package with commercially viable sizes at approximately $21.3cm\ x23.4cm\ x7cm$.

The voltage source referred to in figure 3.1 as V_a corresponds to the designed battery pack, and therefore, possesses the following characteristics:

- $V_{fully\ charged} = 42V$

- $V_{nominal} = 36V$

- $V_{cut-off} = 25V$

The voltage source referred to as V_b corresponds to the output port of the converter to which a constant voltage of $12V$ shall be applied. This voltage should not exceed a deviation of more than 5% ($0.6V$) from the $12V$ value under steady-state operation. Considering that this condition must hold true even under possible load changes, a decision was made to limit voltage ripple for constant load in steady state to 1% of $12V$ ($0.12V$).

The output, should also, be capable of supplying current ranging from $0A$ to $10A$, for values of battery voltage superior to $V_{cut-off}$. Since, $V_{cut-off}$ is the battery cut-off voltage, draining the battery further can result in damage to the equipment and thus a practical implementation of the upcoming work should shut down the converter. Throughout this dissertation, $V_{cut-off}$ may be considered the worst-case scenario for sizing components and proving results, however, its practical inoperability must be kept in mind. As such, considering the commonly steep, descent curve of voltage at the battery's end of charge, before and into the cut-off voltage. A decision was made to place the minimum voltage of the battery at $27.5V$ which will be referred to as $V_{discharged}$ hereinafter.

3.3 Component Design

Having proved, in sections 3.1.1.1 and 3.1.1.2 PSM to be a simplified case of QSW, with lower range of ZVS operation. A decision was made to design the converter according to that modulation method.

3.3.1 Transformer ratio design

From equations 3.9 and 3.10 it is possible to deduce that both local maximums for the inductor current are dependant on the transformer ratio n. As such, in order to reduce conduction losses the transformer turns ratio n was designed in such a way that, when the power supply V_a (battery) is operating at nominal voltage ($36V$) the peak current across the inductor is minimized.

For that to happen, the following condition must be met:

$$\frac{I_P}{I_{L1}} = \frac{\frac{T_s}{4L}[V_b(2d-1)+nV_a]}{\frac{T_s}{4L}[nV_a(2d-1)+V_b]} = 1 \Leftrightarrow V_b(2d-2) = nV_a(2d-2) \Leftrightarrow n = \frac{V_b}{V_a} \tag{3.24}$$

From it, follows

$$n = \frac{12}{36} = \frac{1}{3} \tag{3.25}$$

3.3.2 Inductor design

The converter must be able to supply $10A$ of current to the load up until the point when the supply battery is discharged, sizing for the cut-off voltage ($25V$) will give a safe margin for the absolute worst case scenario. Apart from it, it is desirable that the phase shift ratio that provides the said current is chosen to be a bit less than 0.5 (maximum value), both for accounting non-idealities/losses that the converter might and also because of the inversion of growth to decrease of average output current as duty ratio crosses over 0.5. As such, defining $d = 0.45$ and $I_{o_{max}} = 10A$, from equation 3.11

$$I_{o_{max}} = 10A = \frac{\frac{1}{3}\cdot 25 \cdot \frac{1}{25\cdot 10^3}}{2\cdot L}(0.45 - 0.45^2) \Leftrightarrow L_{max} \approx 4.12\mu H \tag{3.26}$$

3.3.3 Output capacitor design

The capacitor present on the b side (here referred as output side for simplicity), must be able to absorb the current changes and provide an allowable steady state voltage ripple [45].

Since,

$$C_b = \frac{\Delta Q}{\Delta V} \tag{3.27}$$

it is now, necessary to calculate the amount of charge received or supplied by the capacitor in steady state. In figure 3.10, the current across the inductor is presented in detail

Recalling figure 3.3,

$$t_b = \frac{\mathrm{T_s}\,(n\,\mathrm{V_a} + \mathrm{V_b}\,(2\,d-1))}{4\,\mathrm{V_b} + 4\,n\,\mathrm{V_a}} \tag{3.28}$$

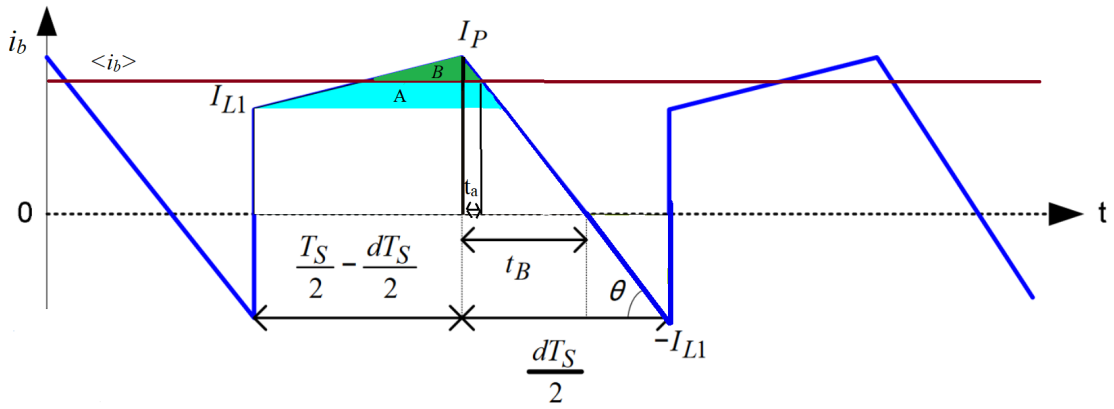

Figure 3.10: Current waveform of output in steady state [12].

$$I_P - I_{L1} = \frac{1}{L} \cdot -(nV_a + V_b) \cdot t_a + I_P \Leftrightarrow t_a = \frac{-I_{L1}}{\frac{1}{L} \cdot -(nV_a + V_b)} \tag{3.29}$$

considering the previously determined values as:

$$\begin{cases} L = 4.12uF \\ T_s = \frac{1}{25 \cdot 10^3} \\ n = \frac{1}{3} \end{cases} \tag{3.30}$$

Assuming $V_a = 42V$ which amounts for the worst case, in which the voltage ripple is greater. In order to limit the output voltage ripple to a maximum ripple of 1% it is necessary to determine d for maximum output current of $10A$ under this conditions. As such, remembering equation 3.11,

$$I_o = 10A = \frac{\frac{1}{3} \cdot 42 \cdot \frac{1}{25 \cdot 10^3}}{2 \cdot 4.12 \cdot 10^{-6}} \cdot (d - d^2) \Leftrightarrow d \approx 0.1791 \vee d \approx 0.8209 \tag{3.31}$$

from this, the possible value is $d = 0.1791$ and from equations 3.10 and 3.9

$$I_P \approx 39.81A \tag{3.32}$$

$$I_{L1} \approx 7.318A \tag{3.33}$$

$$\tag{3.34}$$

Leaving,

$$t_a \approx 1.160\mu s \tag{3.35}$$

$$A_{A+B} = \frac{\frac{T_s}{2} - \frac{dT_s}{2} + t_a}{2} \cdot (I_P - I_{L1}) \approx 2.856 \cdot 10^{-4} C \tag{3.36}$$

$$A_B = A_{A+B} \cdot (\frac{I_P - I_{oavg}}{I_P - I_{L1}})^2 \approx 2.404 \cdot 10^{-4} C \tag{3.37}$$

$$C_b = \frac{\Delta Q}{\Delta V} = \frac{A_B}{2 \cdot V_b \cdot 1\%} \approx 1001\mu F \tag{3.38}$$

where A_{A+B} is the sum area of shapes A and B and A_B is the area of shape B.

Considering the value to be very specific and difficult if not impossible to find on market, it was decided to employ

$$C_b = 1.5mF \tag{3.39}$$

which is a common market value and also allows provide a even lower output voltage ripple. Also, parasitic resistances at the wires and components, drive the voltage seen by the transformer's primary to be even greater which in turn demands a greater capacitor for the same output ripple. Such an over sizing of the capacitor implies that the output characteristics are still met.

3.4 Open Loop simulation

Following the studying of the theoretical functioning of the converter achieved on chapter 3, the implementation of it on a simulation environment, under an open loop regime surges as a next logical step.

It will allow for the validation of the calculated parameters in section 3.3 alongside the used waveform equations.

Simulation will be divided into three major sections, the simulated electrical circuit whose explanation will be approached on upcoming section 3.4.1, the transistor control (section 3.4.2) that approaches the circuit responsible to drive on or off the gates of the multiple transistors, also referred as "gate driver" circuit. Lastly, since the open loop character of the aforementioned sections, chapter 4 will approach the circuitry responsible to control the circuit in close loop.

In Simulink, the DAB converter power circuitry and modulation block were implemented from scratch. Its simulation results are then analysed in section 3.4.3.

3.4.1 DAB implementation

In figure 3.11, an overview of the simulated model of the electrical DAB converter can be seen.

Due to the inherent reverse conducting diode present in the body of the MOSFET semiconductors, their faster switching times and the relative low power of the converter, MOSFETs were preferred to IGBTS.

The converter's implementation is based on the ideal DAB previously presented on figure 3.1, however, both R_t and L_m are added.

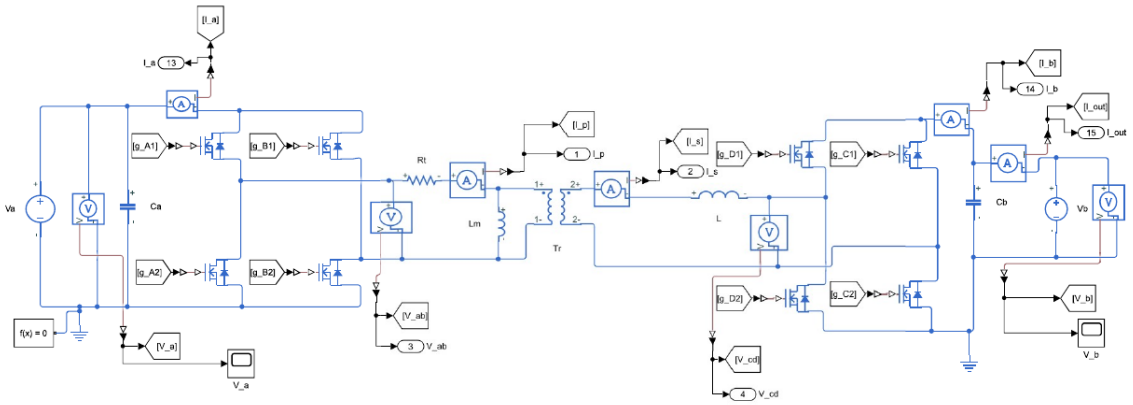

Figure 3.11: Implemented DAB overview.

R_t serves to simulate resistance parasitic through the transformer, across the wires, switches, inductor, capacitor or possibly even a resistance implemented in the circuit itself, all lumped together. As these will effect the transient response of the circuit.

Inductance L_m implements the magnetizing inductance of the transformer T_r, in an ideal transformer its value should be close to infinity and have a negligible effect on the circuit. However, outside an ideal simulation environment, this is never the case and its impact to transient behaviour should be considered.

It is important to point out that all the symbolic terminology shown on figure 3.11 will be recurrently used throughout this dissertation, they should therefor be presented on forthcoming chapters without the need of further description.

3.4.2 Transistor control

To control the functioning of the converter, a circuit responsible for implementing the modulation technique and driving the gates of the converter transistors accordingly was devised. In light of previous chapters, such a circuit block must be capable of QSW modulation.

The full circuit is represented at annex A.2, but due to its sheer dimension, explanation of the working principle will be focused on the logic behind the driving of MOSFETs' gate $A1$ and $A2$. Nevertheless, the logic behind each transistors gate will be explained through equations and its implementation will share a similar model to the ones of gate $A1$ and $A2$.

Branding the $Phase_1$ and $Phase_2$ as the phases of V_{ab} and V_{dc} waveforms, correspondingly $PhaseShift$ the phase between them in radians and $Delta_P$, $Delta_S$ the QSW dead-time duty ratio of the primary (V_{ab}) and secondary (V_{dc}) waveforms. Follows,

$$Phase_1 = \begin{cases} wt - \frac{Delta_P T_s}{2} & \text{, A leg} \\ wt + \frac{Delta_P T_s}{2} + \pi & \text{, B leg} \end{cases} \tag{3.40}$$

$$Phase_2 = \begin{cases} Phase_1 + PhaseShift - \frac{Delta_S T_s}{2} & \text{, D leg} \\ Phase_1 + PhaseShift + \frac{Delta_S T_s}{2} + \pi & \text{, C leg} \end{cases} \tag{3.41}$$

where,

$$Phase_1, Phase_2 \in [0,\ 2\pi] \tag{3.42}$$

As seen in figure 3.12, firstly the switching frequency F_s is multiplied by 2π and integrated in time to form the phase angle wt which must be wrapped between 0 and 2π radians. Generating a sawtooth waveform that at every instant gives the phase of the corresponding bridge output voltage.

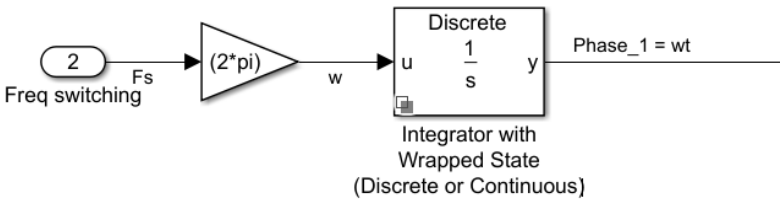

Figure 3.12: Phase generator.

The instantaneous phase is later added or subtracted the value of the corresponding QSW dead-time duty ratio in radians.

To wrap the resulting waveform between 0 and 2π the following equation was implemented:

$$Wrapper(\alpha) = (\alpha - \alpha_{min}) \bmod (\alpha_{max} - \alpha_{min}) \tag{3.43}$$

Figure 3.13 represents the aforementioned description, where Lower Limit $= \alpha_{min}$ and Upper Limit $= \alpha_{max}$.

Since switches of the same leg cannot be simultaneously on, due to the danger of short circuiting the supply voltage source, a dead time between them should be added. Figure 3.14 shows the implementation of the dead time between same leg transistors, in this case A_1 and A_2.

Other MOSFETs' are driven with a similar logic conjugated, of course, with equations 3.40 and 3.41. As such, $Phase_2$ will added a $PhaseShift$ value corresponding to d which will determine the direction and magnitude of the power flow between bridges.

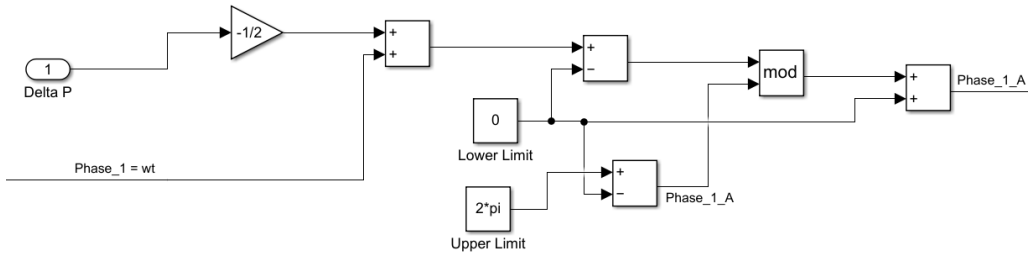

Figure 3.13: Delta adding and phase normalizing.

It is important to note once again that this design is prepared for both SQW and QSW modulation, which will be important for both, validating chapter 3 results, and to control the converter at later stages of this dissertation.

3.4.3 Results

A simulation in open loop was carried out taking into account the modeled circuits of sections' 3.4.1 and 3.4.2. Throughout this simulation, the following conditions were implemented:

- Switches were considered to be ideal.
- Transformer was considered ideal and its magnetizing inductance L_m is, therefor, infinite and can be neglected.
- Voltage sources were modelled to be ideal.
- Wire resistance is neglected.
- Components were sized according to section 3.3.

As previously explained, the case which will cause the most ripple at the output is when $V_a = 42V$ and the output is being supplied with $10A$.

Using equation 3.11,

$$I_b = 10A = \frac{\frac{1}{3} \cdot 42 \cdot \frac{1}{25 \cdot 10^3}}{2 \cdot 4.12 \cdot 10^{-6}} (d - d^2) \Leftrightarrow d \approx 0.1791 \tag{3.44}$$

which gives the duty ratio d, forcing the power flow's direction to be from the primary to the secondary, means having V_{ab} lead V_{dc}. According to the design implemented for the MOSFET gate driver A.2, leaves

$$\text{phase\_shift\_Open\_Loop} = -0.1791\pi \tag{3.45}$$

Replacing V_b voltage source with a resistance to of $R_{Load} = \frac{12V}{10A} = 1.2\Omega$ to model a resistive load, voltage ripple at V_b can be simulated. Figures 3.15, 3.16 and 3.17 yield the results of the simulation.

Results were deemed in accordance to what was theoretically expected in section 3.3. Output voltage was centered at $12V$ and ripple was within the stipulated 1% of V_b for a average $10A$

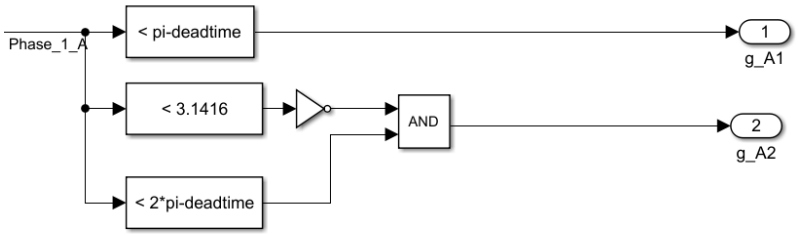

Figure 3.14: Dead time generator.

current. The phase shift between active bridges was confirmed and currents instantaneous I_b and I_p met its the theoretical shape.

The average value of I_p, however, was different from zero which might have unwanted intentions such as saturate the transformer causing the function of the converter to degrade in a less idealised simulation model. This further implies the importance of R_t which will "discharge" the average value of the current through the coil L driving it to zero.

3.5 Summary

To summarise, the DAB converter was approached due to its wide input range capabilities. Bidirectional power flow was studied alongside the converter steady state functioning, the soft switching characteristics were identified as being ZVS turn on/off for all transistors. However, soft switching can only be achieved on a limited range of operation. Two main modulation techniques were identified as being SQW and QSW, the last being capable of extending the converter's soft switching range at the cost of added complexity. Waveforms and steady state equations were derived for both modulation techniques.

At last, the main requirements for the converter functioning were identified, having the converter's components been sized properly according to it.

An open Loop simulation of the DAB converter was carried out using the Simulink simulation environment. Firstly a description of the implemented blocks was presented with due explaining of its functioning.

The open loop simulation was set with ideal components verifying previous requirements imposed to it previously on this dissertation. Overall response of the converter met satisfactorily theoretical assumption made to it.

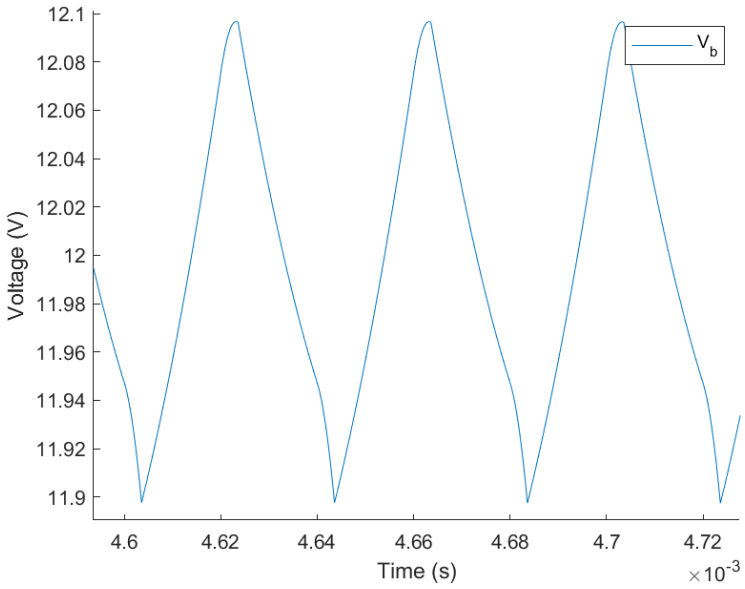

Figure 3.15: Voltage ripple at the output.

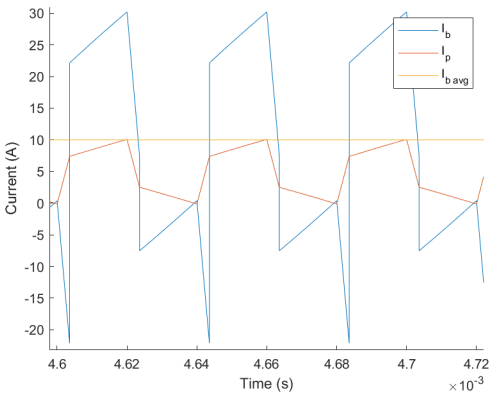

Figure 3.16

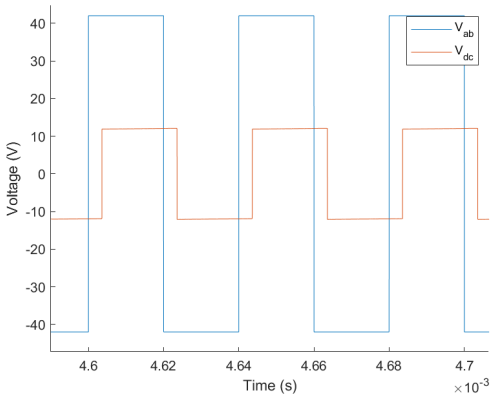

Figure 3.17

Figure 3.18: Current waveforms at the output, primary and average current at the output 3.16; Voltage at each active bridge terminals 3.17.

Chapter 4

Closed Loop Analysis

After having the performance of the converter validated in open loop, all the conditions are united to move for a closed loop regulation of the controller. Such as step is necessary in order to maintain desired output characteristics independent of variable operating conditions. Bidirectional power flow must also be considered in the control design.

The controller must be able to maintain output voltage V_b within the required 5% of variation despite load changes.

In the appendix A.1 an overview of the converter simulated is presented with the respective transistor control logic circuit on A.2.

4.1 Closed Loop Controller

The simulated controller was heavily based on reference [42], its objective is to drive the converter's controllable variable, $PhaseShift$ between bridges, to maintain the output state V_b within bounds. Figure 4.1 presents the modeled circuit scheme.

The PI controller possess an infinite DC gain, thereby ensuring zero steady-state error, resulting in good reference tracking [46]. Additionally, any noises at the tracked signals that a physical implementation of the controller could pick up would not be translated into the performance of the converter as much as with a PID. Output voltage (V_b) is sampled and filtered into its DC value ($V_{b\,filt}$), and the error between it and the voltage reference V_{ref} enters a PI controller which tracks the required current I_b. Therefore, the output of the first PI (from left to right) will increase or decrease according to the need for current to maintain the set, capacitor C_b plus output load, at V_{ref} voltage value.

The second PI controller outputs the required $PhaseShift$ value with which, the gate pulses will be activated. The input of the controller is computed as the error between the current reference $I_{b\,ref}$ and its filtered DC value $I_{b\,filt}$.

In a traditional FeedBack Based control, reference $I_{b\,ref}$ for the second PI, would be generated as the output of the first PI. This is enough to achieve zero steady-state error between $V_{b\,filt}$ and

V_{ref}; however, response time is typically poor [42]. In a system like the proposed in this dissertation, the slow response of the simple feedback-based controller would mean that the $\pm 5\%$ bound from V_{ref} could not be met given a fast enough load variation.

The feedforward controller can improve response time and overshot control of the output voltage [42], the load current I_{out} was filtered, to get its DC value ($I_{out\ filt}$), which was used to supplement the generated PI based current reference. As such, two feedforward components were added to the reference, one directly proportional to $I_{out\ filt}$, other to the derivative of $I_{out\ filt}$.

Since a load change translates into a variation of load current I_{out}, having it being directly fed to the reference of current allows for a faster adjustment of the $PhaseShift$ value decreasing overall V_b overshoot without altering PI values. Having the derivative of I_{out} being fed as well to the current reference adds to the overall response of the converter, allowing to minimize delays associated with filter response.

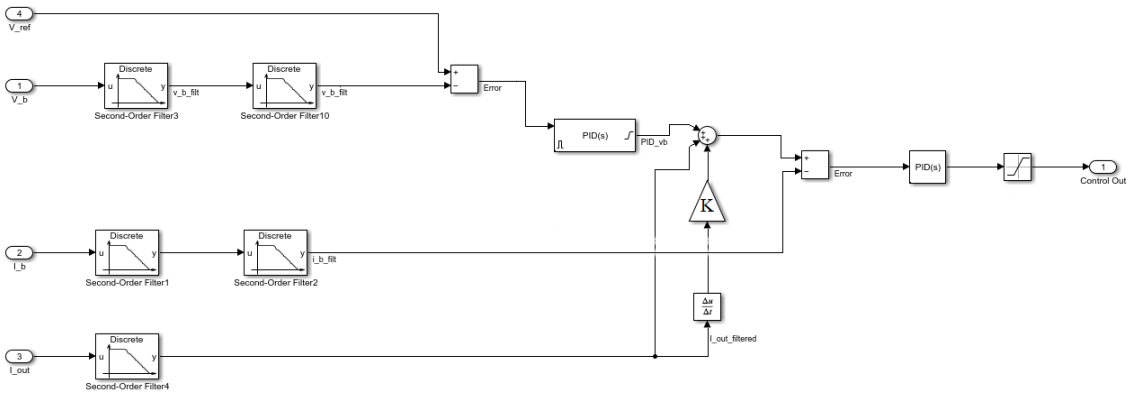

Figure 4.1: Closed loop controller

Note that the derivative feed forward component is affected by a certain gain. The gain was calculated considering that the maximum output current of the converter is $10A$ which deems the maximum load change to of $20A$ (from $10A$ to $-10A$), applying such a load change to the converter will make of I_{out} a square wave, but $I_{out\ filt}$ will not transition instantaneously between current levels due to the response delay across the filter. The falling time was measured as $80\mu s$ from the simulated model. Therefor, the average derivative for such a load change would be:

$$\frac{di_{out}}{dt}_{avg} = \frac{20}{80 \cdot 10^{-6}} \tag{4.1}$$

In order, to limit the derivative component feed to the controller, a decision was made that the average derivative, for the maximum load change, should effect the reference in a value three times superior to the load change. Having found, through trial and error, this value to work well for the controller tuned in section 4.1.2. Letting:

$$\frac{di_{out}}{dt}_{avg} \cdot K = 20 \cdot 3 \Leftrightarrow K = 240 \cdot 10^{-6} \tag{4.2}$$

where K represents the gain applied to the derivative block.

4.1.1 Filters

The simulated controller, discussed previously, is dependant on the tracking of the DC value of V_b, I_b and I_{out} waveforms.

Voltage V_b 's waveform is, ideally, purely DC and constant. However, as previously explained it is subject to voltage ripple, moreover, a changing load current should effect a transient behaviour in which the DC value will briefly change.

Current I_b will assume a shape alike the one illustrated on chapter 3.1.1.1 figure 3.3, completing a period twice every switching cycle.

Current I_{out} will depend greatly on the load applied to the converter, and as such cannot be predicted. Due to the feed forward nature of I_{out} mixed with its unpredictability, a generally quicker response will be needed from it compared to the filtering of I_b and V_b.

The higher the filter's order, the faster its rolloff rate will be, however it comes with a cost of increased phase lag. Keeping in mind this trade-off, signals V_b and I_b are filtered with two second order filters cascaded, effectively creating a fourth order filter.

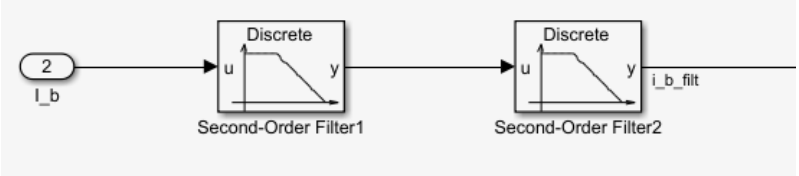

Figure 4.2: Simulated filters.

Each "Second-order Filter" block implements the following Laplace transfer function:

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{4.3}$$

corresponding to a Low-pass second order filter where ω_n is the filter natural angular frequency, and ζ equals to the damping ratio. The damping ratio was fixed at 1 so as to achieve an "over-damped" response, iteratively the natural frequency of the filter was than lowered until a good response was achieved. Such amounted to the following parameters:

$$\begin{cases} Natural\ frequency = f_n = 15kHz \\ Damping\ factor = \zeta = 1 \end{cases} \tag{4.4}$$

The cascaded second order filter's transfer function can be achieved according to the following

$$\begin{aligned} H_{cascaded}(s) = H(s) \cdot H(s) = \left(\frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}\right)^2 = \\ = \frac{{w_n}^4}{s^4 + 4s^3 w_n \zeta + 4s^2 {w_n}^2 \zeta^2 + 2s^2 {w_n}^2 + 4s {w_n}^3 \zeta + {w_n}^4} \end{aligned} \tag{4.5}$$

Figure 4.3, shows the frequency response of the specified filters. The cut-off frequencies of the second and fourth order filters are, $9.654kHz$ and $6.206kHz$ respectively.

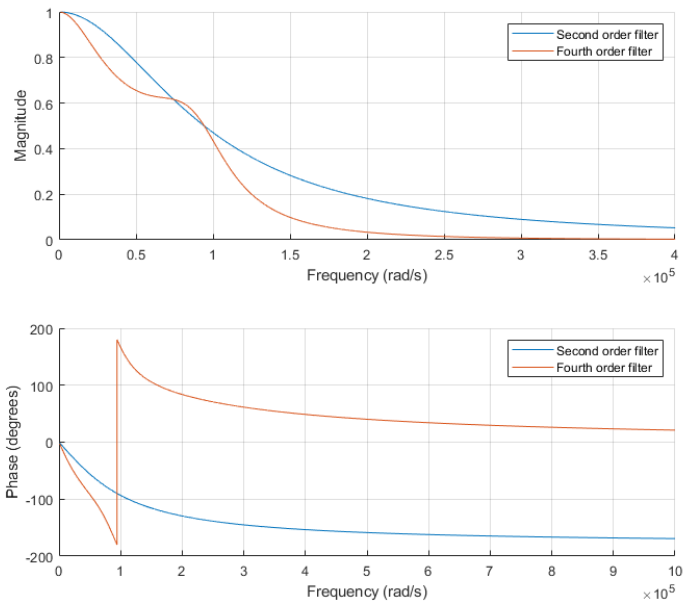

Figure 4.3: Frequency response of the second order filter.

4.1.2 PI tuning

In order to tune the PI controllers, the Ziegler and Nichols iterative method was used. For the first PI controller the critical gain K_u and the oscillation period T_u, have been determined as:

$$K_{u1} = 0.7 \quad T_{u1} = 178\mu s \tag{4.6}$$

However, due to the known *aggressive behaviour* characteristic to the response of the controller tuned with the Ziegler and Nichols method, this should only serve as a starting point. In fact, any overshoot of voltage V_b resulting from this method should not be accepted, than the response shall be adjusted to be slower without overshoot. Iteratively, it was possible to arrive at the following values:

$$\begin{cases} K_{p1} = 0.45 \cdot K_{u1} \cdot 4 \\ K_{i1} = 0.54 \cdot \frac{K_{u1}}{T_{u1}} \cdot \frac{2}{5} \\ k_{d1} = 0 \end{cases} \Leftrightarrow \begin{cases} K_{p1} = 0.6300 \\ K_{i1} \approx 849.4 \\ k_{d1} = 0 \end{cases} \tag{4.7}$$

The second PI controller, nonetheless, does not need to be constricted to have no overshoot; in fact it should have a significantly faster response than the first one, to be able to respond to load changes in an effective way. The standard Ziegler and Nichols method was found to work well, and therefor the following was simulated:

$$K_{u2} = -0.16 \quad T_{u2} = 70\mu s \tag{4.8}$$

$$\begin{cases} K_{p2} = 0.45 \cdot K_{u2} \\ K_{i2} = 0.54 \cdot \frac{K_{u2}}{T_{u2}} \\ k_{d2} = 0 \end{cases} \Leftrightarrow \begin{cases} K_{p2} = -0.07200 \\ K_{i2} \approx -1.234 \cdot 10^3 \\ k_{d2} = 0 \end{cases} \tag{4.9}$$

In order to confirm the validity of the converters response, a "*stress test*" in which the output load is forced to vary between $10A$ and $-10A$ in square wave at time intervals $t = 1ms$ and $t = 2ms$. Since the maximum output current for which the converter is prepared is of $10A$, and setting V_a equal to $25V$ ($V_{cut-off}$), than the worst scenario response can be achieved.

Figure 4.4 and 4.5 illustrate this test.

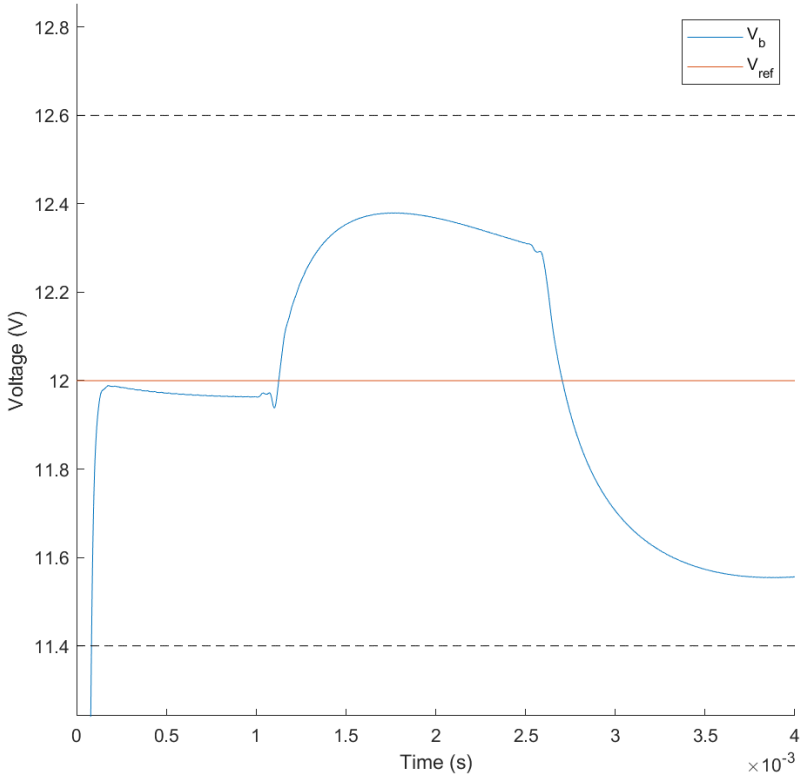

Figure 4.4: Output voltage response to stress test.

Note that due to the feed forward derivative converter peaks appear at the reference when there is a transition between load current.

Analysing the aforementioned figures, it was possible to confirm that the voltage did held inside the established limits having peaked maximally at $12.38V$ and minimally at $11.56V$. A good current tracking was registered at figure 4.5; settling times, after reference transition, were measured at $t = 0.7242ms$, $t = 0.6141ms$ and $t = 0.6213ms$ at time instants $t = 0.7242ms$, $t = 1.6141ms$ and $t = 3.121ms$, respectively.

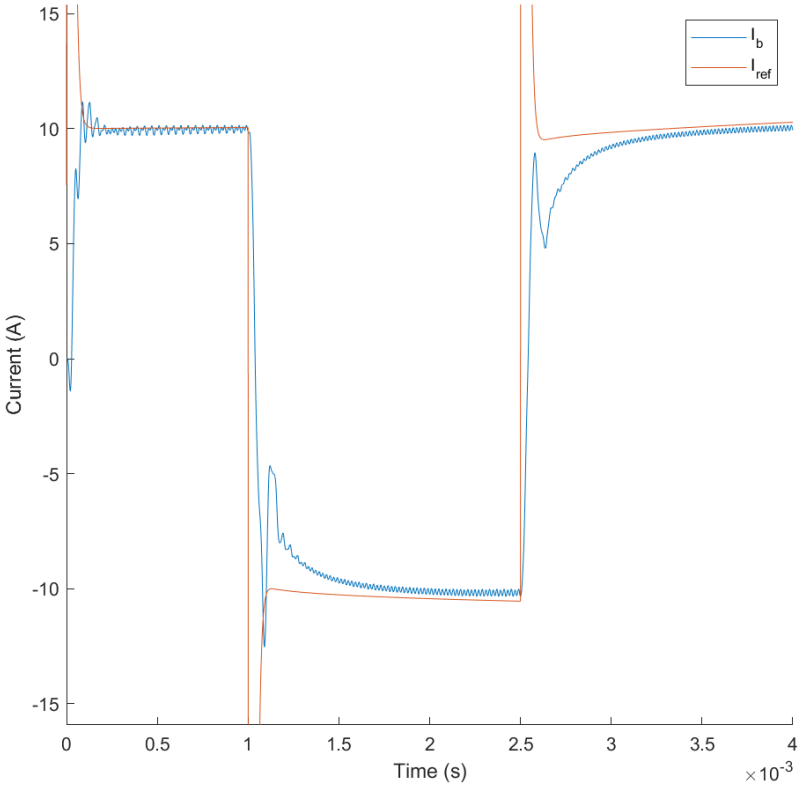

Figure 4.5: Current supplied to C_b under stress test.

In practice, $V_a = 25V$ is a case which the converter shall never operate because, it corresponds to the cut-off voltage of the battery, for which the battery is considered to be cut-off.

4.2 Quasi-Square-Wave Controller

Having established operation of the converter under SQW modulation, QSW modulation was also simulated. Such was done with the objective to compare both modulation methods and draw conclusions for performance, power losses and ZVS range.

In order to generate the δ_x values, necessary to feed the transistor's command signal with, a method was devised using a Lookup table (LUT). Based on equation 3.20, replicated bellow for convenience; a relation between I_b, δ_a and δ_b can be drawn as:

$$I_b = \frac{nV_aT_s}{2L}(-d^2 - d\,\delta_a - d\,\delta_b + d - \frac{{\delta_a}^2}{2} - \frac{\delta_a\,\delta_b}{2} + \frac{\delta_a}{2} - \frac{{\delta_b}^2}{2} + \frac{\delta_b}{2}) \tag{4.10}$$

Applying the following assumptions,

$$\begin{cases} \delta_a = \delta_b = \delta_x \\ a = \frac{I_b}{nV_a}\frac{2L}{T_s} \end{cases} \tag{4.11}$$

Through algebraic manipulation, an expression for "a" can be achieved as shown on 4.12.

$$a = -d^2 - 2d\,\delta_x + d - \frac{3\,{\delta_x}^2}{2} + \delta_x \Leftrightarrow \delta_x = \begin{cases} \frac{1}{3} - \frac{\sqrt{-2d^2+2d-6a+1}}{3} - \frac{2d}{3} \\ \frac{\sqrt{-2d^2+2d-6a+1}}{3} - \frac{2d}{3} + \frac{1}{3} \end{cases} \tag{4.12}$$

Plotting *"a"* according to duty cycle and δ_x, figure 4.6 can be obtained. The idea is to use the plotted curves to analyse $I_b(d)$ that translates the maximum power transfer per duty ratio possible with respect to δ_x.

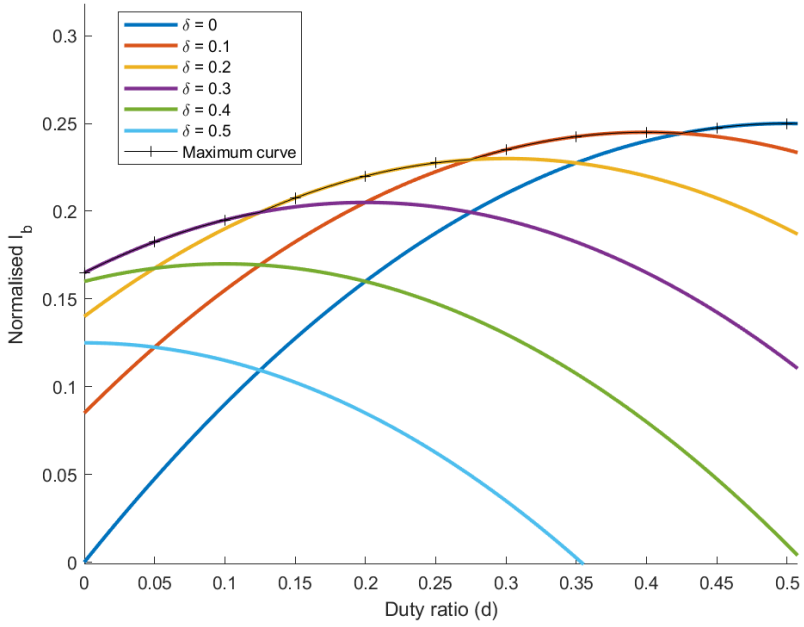

Figure 4.6: Maximum curve for normalised average output current as a function of duty ratio for different values of δ_x.

Since in its essence, 4.12 consists of a function that generates the δ_x values according to I_b current and duty ratio d. It can be used to plot the δ_x that translates the maximum *"a"* (normalised I_b current) in function of duty ratio d, represented on figure 4.7.

Using a LUT to implement the function, δ can be generated according to d retrieved from the controller's circuit.

Figure 4.8 presents the modulation method previously described. Note the use of a switch that allows for a simple change between simulating QSW or purely SQW modulation.

4.2.1 ZVS Evaluation

Through equations 3.21, replicated bellow for convenience, it is possible to evaluate if the converter is instantaneously operating under ZVS or not.

$$\begin{cases} d \geq 0.5 - \frac{\delta_a}{2} - \frac{V_b'}{2}(1-\delta_b) & ,V_b' < 1 \\ d \geq 0.5 - \frac{\delta_b}{2} - \frac{1}{2V_b'}(1-\delta_a) & ,V_b' > 1 \end{cases} \tag{4.13}$$

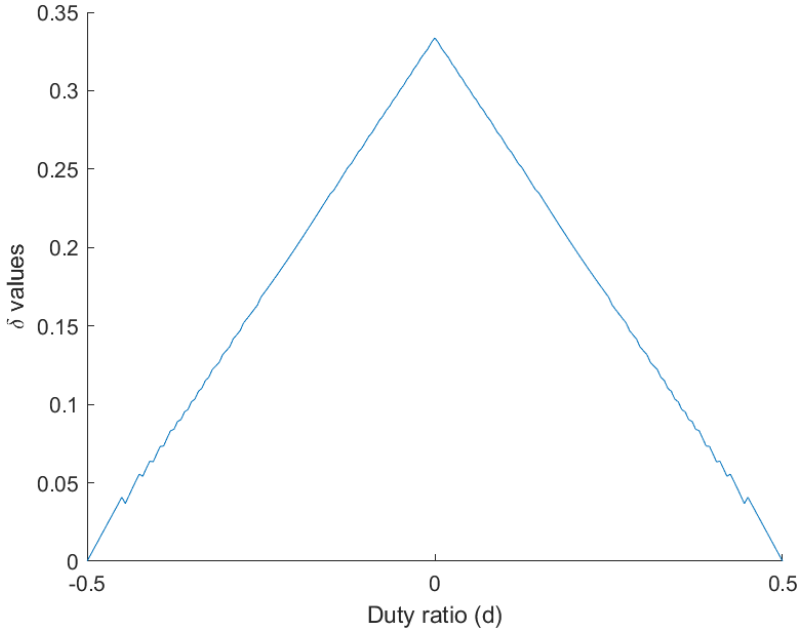

Figure 4.7: δ_x for maximum normalised average current as function of duty ratio.

Where V_b' is the normalised V_b voltage, and as such:

$$V_b' = \frac{V_b}{nV_a} \tag{4.14}$$

Utilizing the aforementioned equations, the block represented on figure 4.9 was created, its objective is to instantaneously determine if the converter is operating under ZVS. If the ZVS conditions are met, a *"flag"* is raised with the value of 1 else the *"flag"* remains with a value of 0. Such allows a easier interpretation of the simulation results, the code employed on the function block can be seen on annex A.3.

4.3 Simulation

To compare the response of the system under different modulation techniques, the converter was simulated using non ideal MOSFETS modeled after the PXN012-60QL. It is important to note that, due to the adopted transformer ratio design, when power is flowing from V_a to V_b three situations are possible.

- The converter operates as buck for V_a above nominal battery voltage ($V_b' < 1$).
- The converter operates as boost for V_a below nominal battery voltage ($V_b' > 1$).
- The converter in between buck mode and boost mode for nominal battery voltage.

As such, to determine the impact of QSW modulation on the ZVS duty ratio, a ideal current source was connected in parallel with the C_b capacitor. This ideal current source will simulate

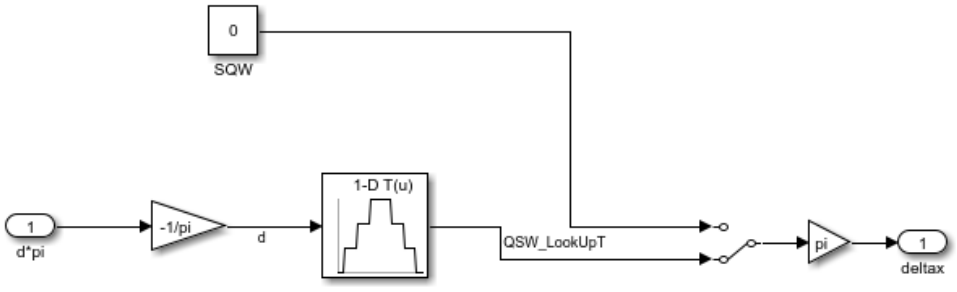

Figure 4.8: Block responsible to calculate δ_a, δ_b.

the presence of a load connected to the output terminals of the converter, its objective in this test is to determine the I_b current and duty ratio d for which ZVS starts to occur in both modulation techniques.

Regarding the ideal load current source, a slow linearly ascending current was chosen not to upset the feed forward derivative component on the closed loop controller. Having a too steep current increase would reflect on the current reference, causing unwanted surges of current at the inflection points.

4.3.1 Non-Ideal Components

In order to properly realize simulations of power losses and performance, a decision was made to use models of non-ideal components. As such:

- $L_m = 14\mu F$
- $R_t = 0.02\Omega$
- MOSFETs were modeled after the commercial device PXN012-60QL.

Using the PXN012-60QL MOSFET datasheet the following values were gathered:

$$\begin{cases} V_{th} = 2.5V \\ V_{fw} = 0.82V \\ V_{gp} = 3.1V \\ R_{DSon} = 9.8m\Omega \\ C_{iss} = 957pF \\ C_{oss} = 386pF \\ C_{rss} = 31pF \end{cases} \tag{4.15}$$

Despite their susceptibility to change in function of the device's operating conditions, for the objective of the simulation they will suffice. Furthermore, attention will be taken in order to mimic the datasheet conditions as much as possible. Namely, V_{GS} will be $10V$ ON and $0V$ OFF.

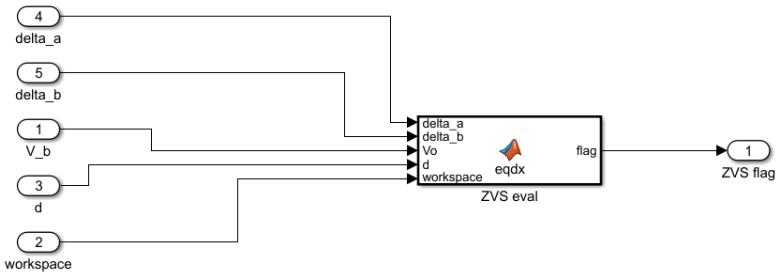

Figure 4.9: Block responsible to evaluate the ZVS condition.

Figure 4.10 shows the used non ideal MOSFET block, and respective MOSFET driver.

As shown, a MOSFET driver will be needed to effectively turn on or off the MOSFET. Since this is a non ideal model, the device's switching times should be kept in mind; as so, the switching temporal performance will be subject to a panoply of different factors, some of which (operating temperature, for example) will not be considered. For this work, the MOSFET device shall be considered as presented on figure 4.11.

The switching times will therefor be influenced by the amount of current that flows to the gate, making the sizing of the gate resistance an important part of the simulation test. Considering that the *deadtime* between same leg transistors is of $150ns$, the gate resistance should be such that:

1. The device switches totally OFF before the next *"in series"* MOSFET is turned ON, or vice versa, in order to avoid a short circuit.

2. Spikes at the Drain-source voltage, caused by command signal leakages through the *gate-to-drain* capacitance, are minimized. I.e., the gate current should be minimized.

Figures 4.13 and 4.14, describe the switching behaviour of the MOSFET, from which equations 4.16 to 4.21 are drawn.

$$t_1 = R_G C_{iss} \cdot \ln \frac{1}{1 - \frac{V_{th}}{V_{GS}}} \tag{4.16}$$

$$t_2 = R_G C_{iss} \cdot \ln \frac{1}{1 - \frac{V_{gp}}{V_{GS}}} \tag{4.17}$$

$$t_3 = R_G C_{rss} \cdot \frac{V_{DS}}{V_{GS} - V_{gp}} \tag{4.18}$$

$$t_4 = R_G C_{iss} \cdot \ln \frac{V_{GS}}{V_{gp}} \tag{4.19}$$

$$t_5 = R_G C_{rss} \cdot \frac{V_{DS}}{V_{gp}} \tag{4.20}$$

$$t_6 = R_G C_{iss} \cdot \ln \frac{V_{gp}}{V_{th}} \tag{4.21}$$

Considering the deadtime, and the worst case in which $V_{DS} = 42V$ for the High-side MOSFETs and $12V$ for the Low-side.

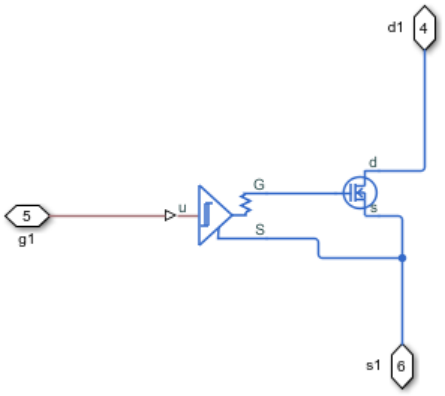

Figure 4.10

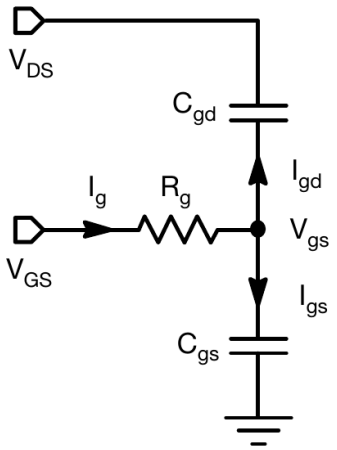

Figure 4.11

Figure 4.12: Simulated MOSFET block (4.10) and MOSFET's equivalent circuit (4.11).

$$\begin{cases} T_{total\ on} = t_1 + t_2 + t_3 \leq 100ns \\ T_{total\ off} = t_4 + t_5 + t_6 \leq 100ns \end{cases} \Leftrightarrow R_G \leq \begin{cases} 183.4\Omega, \text{ Turn On High Side} \\ 57.25\Omega, \text{ Turn Off High Side} \\ 244.5\Omega, \text{ Turn On Low Side} \\ 69.12\Omega, \text{ Turn Off Low Side} \end{cases}$$
$$R_G \approx \begin{cases} 180\Omega, \text{ Turn On High Side} \\ 50\Omega, \text{ Turn Off High Side} \\ 240\Omega, \text{ Turn On Low Side} \\ 60\Omega, \text{ Turn Off Low Side} \end{cases} \tag{4.22}$$

4.3.2 Simulation Results

Using the aforementioned circuit blocks, the converter was simulated on Simulink. As discussed, the converter that has been sized throughout this dissertation will be subjected to operate from boost to buck mode in function of V_a (battery) charge. Three situations are of particular interest the V_{ch} and V_{dch} situations which mark out the operating range and V_{nom}. The nominal case is interesting since, recalling figure 3.6, ideally the duty ratio at which ZVS starts, tends to 0 when $V_b' = 1$ with traditional SQW modulation. The cut-off voltage case will also be simulated to further compare both modulation methods.

Due to the sheer amount of simulation data, all simulation plots will be kept in the appendix, being replicated *"on the spot"* whenever needed. Appendixes A.4.1 to A.4.4 hold the mentioned data.

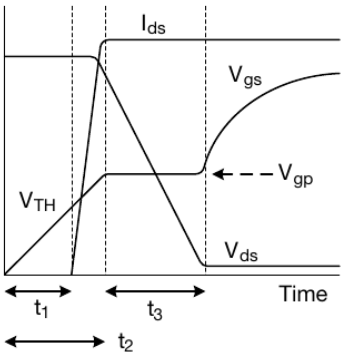

Figure 4.13

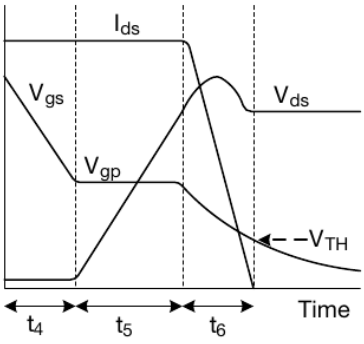

Figure 4.14

Figure 4.15: Turn-on (4.13) and Turn-off (4.14) transient of the MOSFET [13].

4.3.2.1 Comparing modulation techniques: current per duty ratio performance

Analysing the simulation corresponding to the fully charged battery state, figures 4.16 and A.6 translate the differences between modulation techniques in current, duty ratio and transistor dissipated power, respectively.

From the analysis of figure 4.16, it is possible to notice that the overall I_b current performance is practically unchanged, characterized only by having slightly less QSW I_b DC ripple at really fast transients (observed at start up). This is due to the explained increase in RMS current with the increase in δ_x, this is maintained throughout all simulations. A decrease in *current per duty ratio* was also verified. Analysing, however the cut-off voltage case at figure A.9 in the appendice, it is possible to notice that the this ratio increases and decreases with the δ_x evolution. Nevertheless, the overall maximum current that the converter is capable of supplying is independent of δ_x and will always correspond to $d = 0.5$ and $\delta_x = 0$ conditions; this is supported by figure 4.7.

It is important to point out, that in the cut-off state the converter is enable to reach the $10A$ of maximum current for the modelled MOSFETs, barelly missing the mark at a maximum of $9.73A$. However, since the converter only needs to operate between discharged and charged states, the requirements are still met.

Moving out to a comparison of the QSW impact over the different battery charge instants. Although not represented at pictures 4.16, A.3, A.7 and A.9 as not to "saturate" them with information; the *"ZVS flag"* previously implemented on section 4.2.1 was used to register the point at which the device entered ZVS operating range throughout the load ascending current test. Table 4.1 holds that information, discerning them across all four individually studied battery states.

Analysing the table, the nominal case was found to be the one which less benefited from the QSW modulation, proving the expected in section 3.1.1.2.1. The further the battery voltage is from the nominal conditions the greater is the improvement in performance in case of QSW modulation.

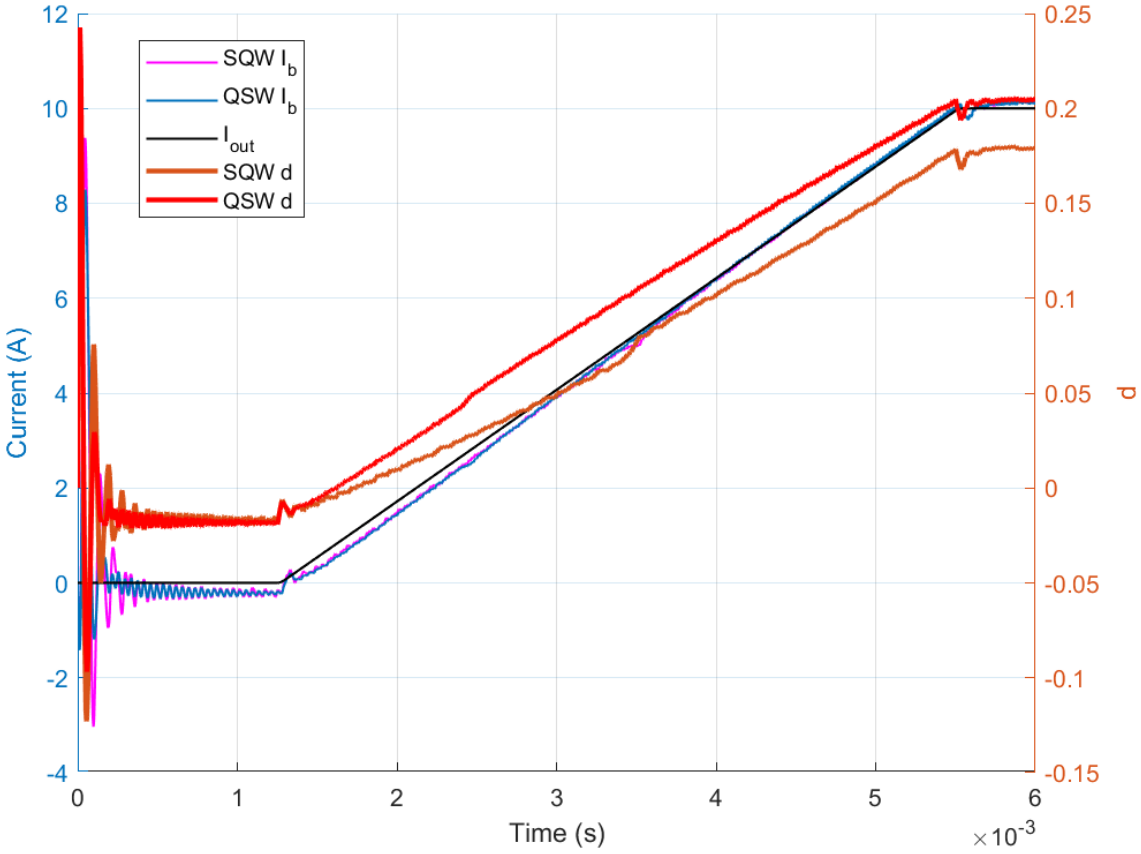

Figure 4.16: Current I_b and duty ratio d compared between both modulations techniques with charged V_a.

4.3.2.2 Comparing modulation techniques: effect on power losses

Regarding the dissipated power at the MOSFETs, figure 4.17 translates the total average dissipated power of all eight MOSFTEs for both modulation techniques. The first noticeable thing is the decrease in overall dissipated power from SQW to QSW modulation. However, spikes at the average dissipated power could also be acknowledged; this are synchronous with the transistors switching and they are a product of imperfect soft-switching of the transistors. If section 3.1.1.1.1 is recalled, perfect ZVS is dependent on the inductor current being able to completely charge/discharge the output capacitance of the transistors during the switching instants, in fact analysing figure 4.18 it is possible to see the *drain to source* voltage and current of transistors A1 and C1 across one switching cycle with the switching instants zoomed in.

From the figure it was possible to understand that both transistors turn on with negative *drain to source* current and turn off with positive current; ideally this would translate in ZVS commutation, however for the MOSFET A1, the turn-off is not perfect creating a spike in the average dissipated power of the MOSFET, this was found to be true for all the high side transistor. Low side MOSFETs, like C1, also share the same problem, however due to their more near zero current waveform at the turn off instant, the problem is minimized.

Note that due to the very fast switch transitions (in the nanoseconds range) the simulator

Table 4.1: Simulation ZVS start results.

	SQW		QSW		Improvement
	d	$I_b\ (A)$	d	$I_b\ (A)$	ZVS Range
$V_{cut-off}$	$1.501e^{-1}$	3.411	$1.108e^{-1}$	2.875	7.86%
V_{dch}	$1.143e^{-1}$	4.382	$8.336e^{-2}$	2.415	6.19%
V_{nom}	$3.020e^{-3}$	$3.284e^{-1}$	$2.141e^{-3}$	$2.457e^{-1}$	0.17%
V_{ch}	$7.373e^{-2}$	4.925	$5.120e^{-2}$	2.713	4.51%

presents relatively low resolution during them. The shown simulation was made with constant $100MHz$ step frequency, increasing the step-size to get significantly more resolution resulted in impracticably long simulation times and a variable step size proved to get results similar to the ones shown on figure 4.18. As such, and since the results go into what was theorized by the relevant literature, it was found that the low resolution was not impeditive to the conclusion drawn above. When in the QSW modulation technique this surges in dissipated power continue to appear, nonetheless since in QSW only one transistor turns off at a time the spike instants will be doubled.

The efficiency of the converter can be calculated as the ratio between the output and input power, if power is flowing from V_a to the load, then equation 4.23 translates the converter's efficiency in percentage.

$$Eff = \frac{P_{Load}}{P_a} \cdot 100 \tag{4.23}$$

Using the "average" block and some arithmetic expressions in symulink, the average input and output power was computed as the product of each side voltage and current. Setting a continuous load current the steady state average efficiency was computed and noted on tables 4.2 and 4.3, that correspond to the SQW and QSW modulation techniques respectively. This test was carried out, once again, across all individual battery states and plotted on figure 4.21. A polynomial fit was carried out to allow a more effortless comparison of the results, having arrived at the conclusion that, once more the QSW modulation demonstrated superior efficiency.

Overall the converter showed reasonable efficiency with high deterioration for light loads. In fact, above $6A$ both modulation techniques showed good results with efficiencies above 84.75%. The results are affected inversely by the battery voltage, this is due to the imperfect soft-switching of the MOSFETs that cause losses to rise up with the increase of *drain to source* voltage that happens on the high side when battery voltage increases.

Table 4.2: Efficiency in percentage, of the converter for output current range in SQW modulation.

V_a \ I_{out} (A)	2	4	6	8	10
V_{dch}	84.68	90.69	92.64	93.21	92.76
V_{nom}	76.09	84.97	88.50	90.54	91.69
V_{ch}	68.40	79.80	84.75	87.54	89.44

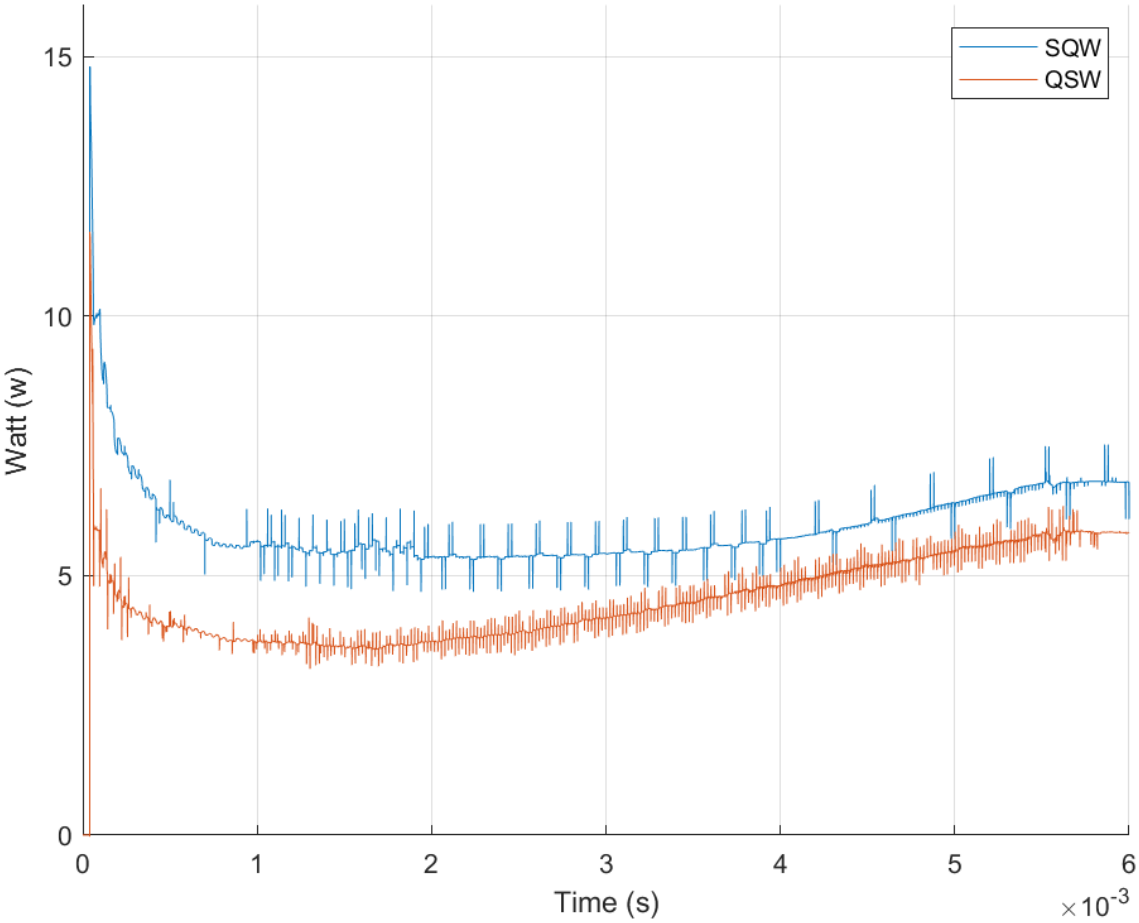

Figure 4.17: Power dissipated at the MOSFETs compared between both modulations techniques with charged V_a.

4.3.2.3 Results for bidirectional Power flow

Having proven that the QSW modulation is the most suited for the requirements the converter was proposed to fulfill. As such, a variable load was imposed on the converter like it is represented on figure 4.23; the converter was given enough time to reach steady state for each load change and so, a $0A$ to $10A$ to $-10A$ regime was tested under the battery discharged condition.

This load characteristics where chosen since they would effectively push the converter to its operation limits, provoking the biggest voltage change with each transition. Joining in the fact that the test was performed under the battery discharged case, in which the controller has to cover the biggest duty ratio range possible; and also effects the least current change per duty ratio change. Contributes to the fact that the controller is working under the worst possible conditions. The same test was simulated with the battery charged state, and the results are present on appendix A.4.5.

Figure 4.22 represents the voltage V_b variation throughout the test, the QSW operation was also shown on figure 4.24 where it is possible to see both V_{ab}, V_{dc} and the inductor current I_s at the reverse power flow steady state.

From the analysis of the figures, and overall satisfactory response was detected. The voltage

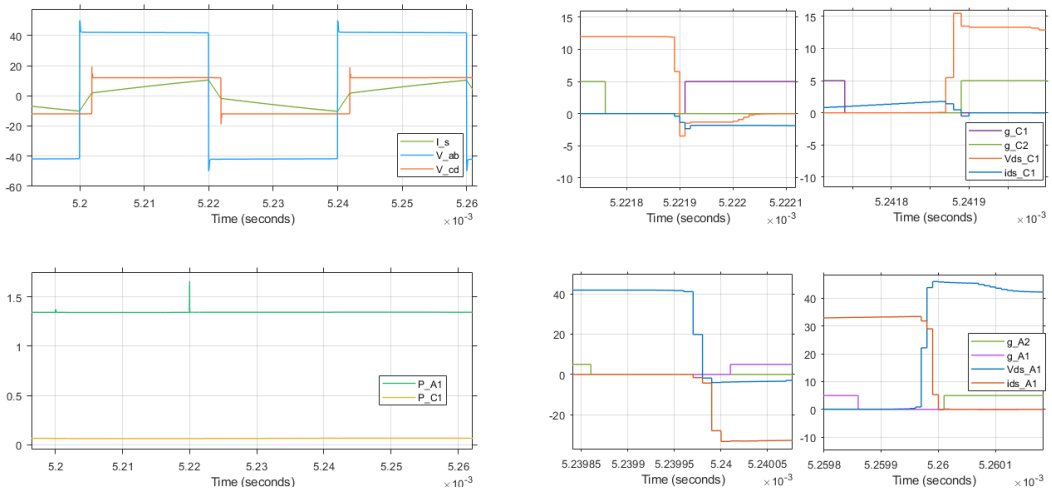

Figure 4.18: Analysis of MOSFETs A1 and C1 across a switching cycle.

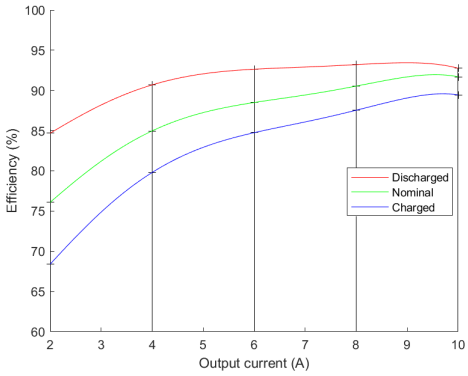

Figure 4.19

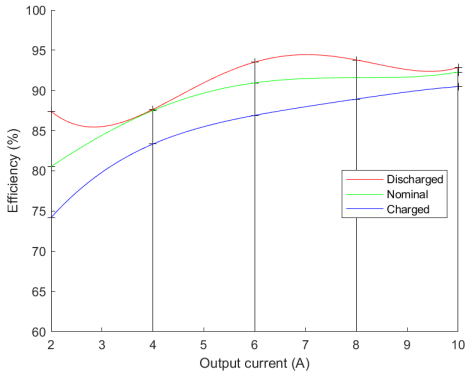

Figure 4.20

Figure 4.21: Plotted efficiency of the converter in SQW (4.19) and QSW modulation 4.20.

V_b stayed under the desired range, and the current I_b followed the load changes with fast response and low overshoot. Bidirectional power flow capabilities were shown and its functioning proved to be satisfactory.

4.4 Summary

This chapter, could majorly be divided in three parts, each corresponding to its section.

First section described the closed loop controller adopted, it sizing was exhibited as well as the reasoning behind it. Additional attention was given to the filters and *PIs* due to their nature. Still in this subsection, a test in which the converter was tested for the positive and negative load limits in order to validate both the *PIs* and the SQW operability of the converter within the imposed requirements.

Second section built upon the last, taking advantage of the functional SQW converter, a controller was established to supply the appropriate δ_x values responsible to translate an SQW mod-

Table 4.3: Efficiency in percentage, of the converter for output current range in QSW modulation.

V_a \ I_{out} (A)	2	4	6	8	10
V_{dch}	87.40	87.64	93.52	93.79	92.86
V_{nom}	80.52	87.50	90.94	91.58	92.29
V_{ch}	74.19	83.33	86.90	88.93	90.48

ulation into a QSW. Consideration was taken to maximize efficiency by forcing δ_x to be such that the converter power transfer is maximal across its duty ratio. An extra block was devised to evaluate when the converter entered its theoretical ZVS range of operation.

The third section focused on simulation, test where carried out in order to compare both modulation techniques against each other. In order to properly appraise the difference between modulation techniques, whose main difference was in the way the MOSFETs commutation was carried out, non ideal MOSFETs were modeled from an available market device. Across the tests QSW modulation technique proved its superiority with better efficiency and transient response. This was, though at the cost of more complexity.

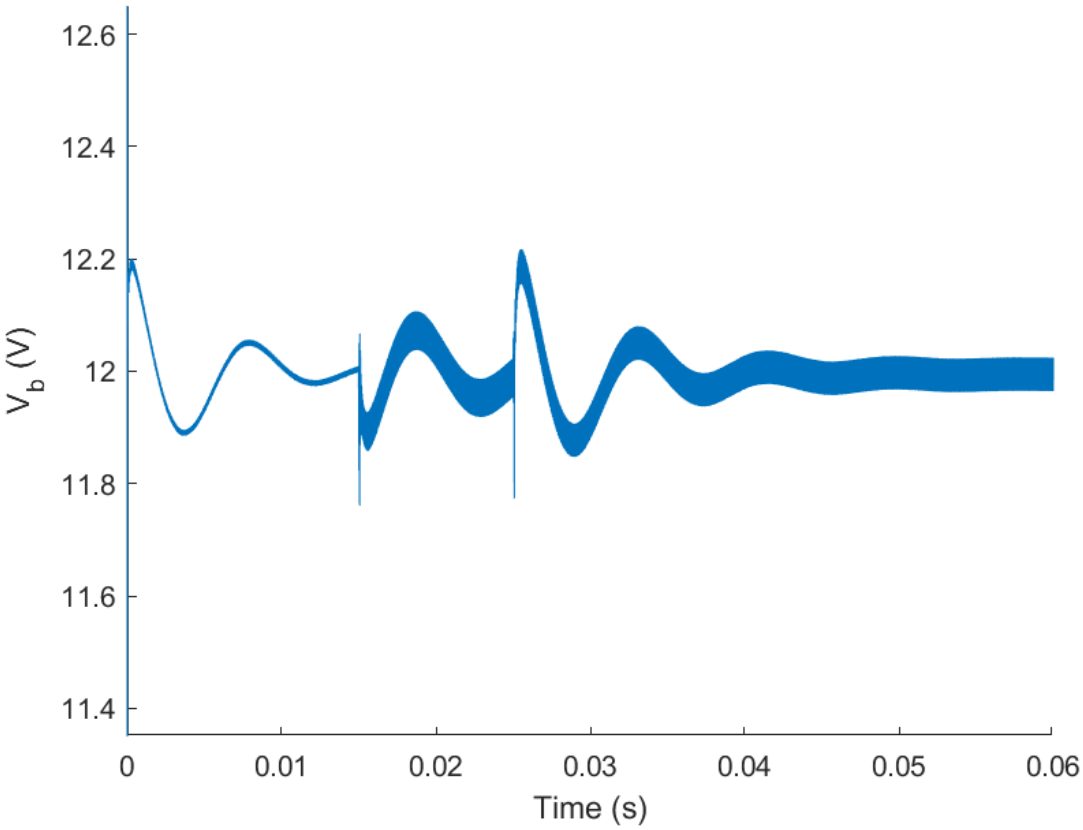

Figure 4.22: Bidirectional power flow test of the converter.

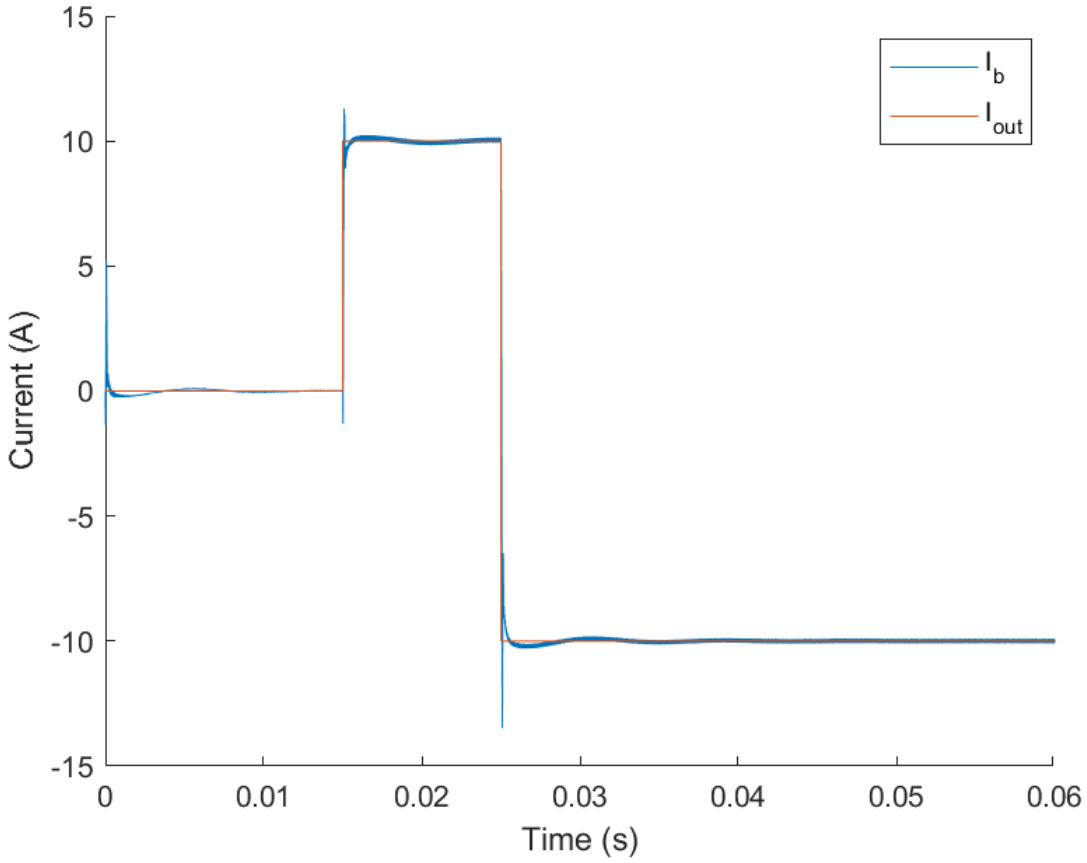

Figure 4.23: Bidirectional power flow test of the converter.

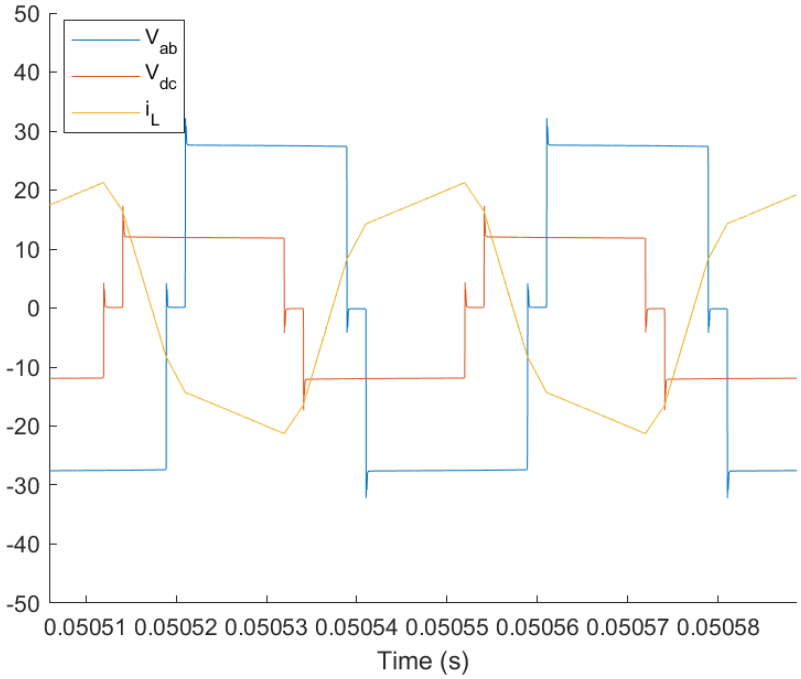

Figure 4.24: Voltage at the active bridges terminals, and inductor current during reverse power flow.

Chapter 5

Conclusions and Future Work

In this chapter the degree of satisfaction with which the work reached its goals will be indicated. Additionally, directions will be suggested to further improve the work built on this dissertation.

5.1 Objective completion

Overall, the goals set for this dissertation were met with success.

The DAB converter was properly described along with two major modulation strategies, the SQW and QSW modulation. The closed loop functioning was implemented through a devised controller, having been tuned by the Ziegler-Nichols method and validated by means of computational simulation using *Matlab/Simulink*. Under this controller, the requirements of voltage and current range set on the start where fulfilled. Bidirectional power flow was simulated and proven.

Both modulation techniques where simulated and compared against each other, having determined the QSW modulation to be superior for the use case at hand. The converter was also simulated using models of non-ideal components and its efficiency was evaluated, having found the results to be overall positive.

5.2 Future work

Although the prime goals of this dissertation have been achieved, there remains space for future work in the development of this converter.

5.2.1 Adding a snubber

As seen in section 4.3.2.2, the turn-off of the MOSFETs happens with imperfect ZVS, although soft switching was achieved. The addition of a snubber could help to lower the losses on the semiconductors. According to ref. [12], adding a capacitor in parallel with the semiconductor would slow down the rate of voltage rise across the transistor, during turn-off, so that a lower voltage appears during the current decay time.

This would theoretically improve the efficiency of the converter by limiting switching transients, reducing current/voltage spikes and minimising electromagnetic compatibility (EMC) problems associated with high *dv/dt* [12]. However its impacts on the turn-on should be studied and taken into consideration in the snubber sizing, and its necessity on the low side should be contested.

5.2.2 Discretization and signal delay repercussion

Throughout this work, the control of the converter functioned on the continuous time domain, in a possible iteration the controlling circuit should be passed onto the discrete time domain. In a practical implementation of this work, the control would most likely be handled by a microcontroller and as such the amount of time required to sample and process the signals would be finite. Such delays should be considered also since they affect the overall controller performance. This would lay a solid ground with which a physical implementation of the work could be performed.

5.2.3 Battery implementation and protection

Having already made the basic steps in sizing the battery the next step to a physical implementation of the converter would be to test it connected to a physical implementation of the designed battery pack. For such to happen, the battery management system should be designed.

Its main functions would be to estimate SoC, balance cell's charge within the pack, prevent over and undercharging of the battery, to detect and safely disconnect damaged cells from the pack.

Appendix A

DAB implementation

A.1 DAB converter Simulink Implementation

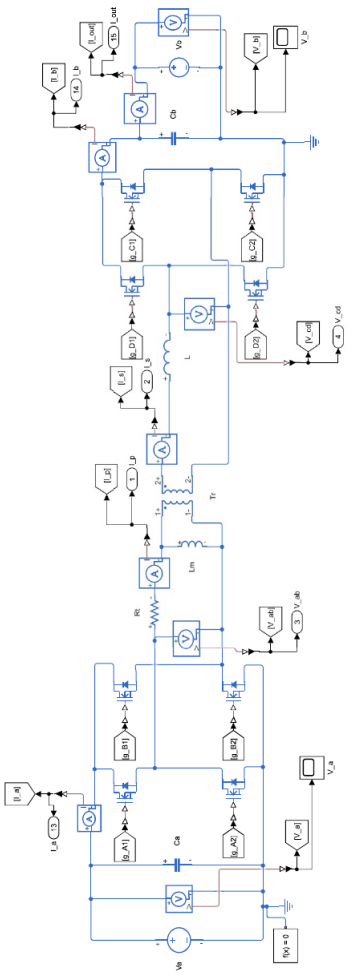

Figure A.1: Implementation of the DAB converter on simulink.

A.2 Gate Signal Generator

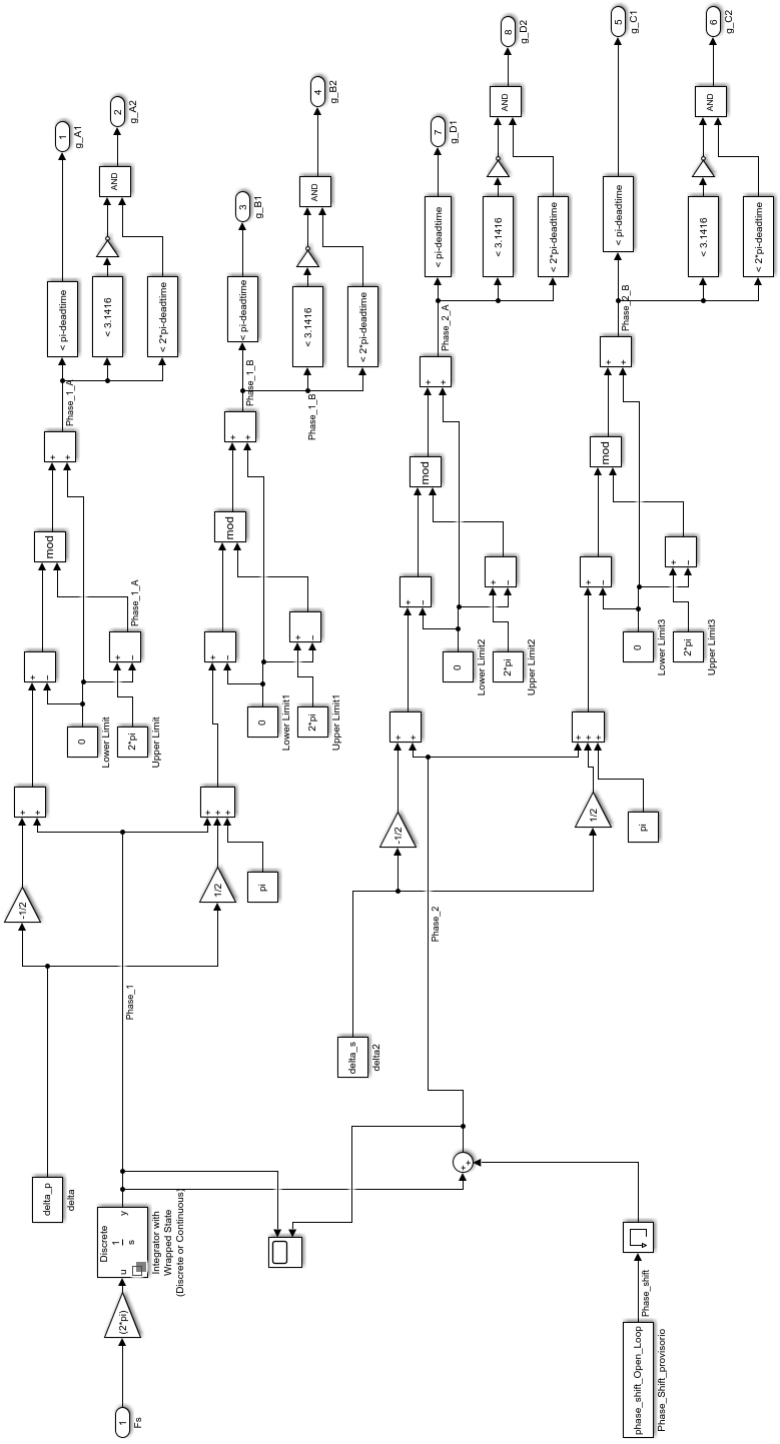

Figure A.2: Gate driver logic

A.3 ZVS Evaluation Block

```
function flag = eqdx(delta_a, delta_b, Vo, d, workspace )

zvs_buck = 0;
zvs_boost = 0;

vo_norm = Vo/(workspace(4)*workspace(3));

d_buck = 0.5 - delta_a/2 - vo_norm/2 *(1-delta_b);

d_boost = 0.5 - delta_b/2 -1/(2*vo_norm) *(1-delta_a);

flag = ( (d >= d_buck) && ( vo_norm <= 1) ) || ( (d >= d_boost) && (vo_norm > 1) );
```

A.4 Simulations

A.4.1 Nominal battery voltage case

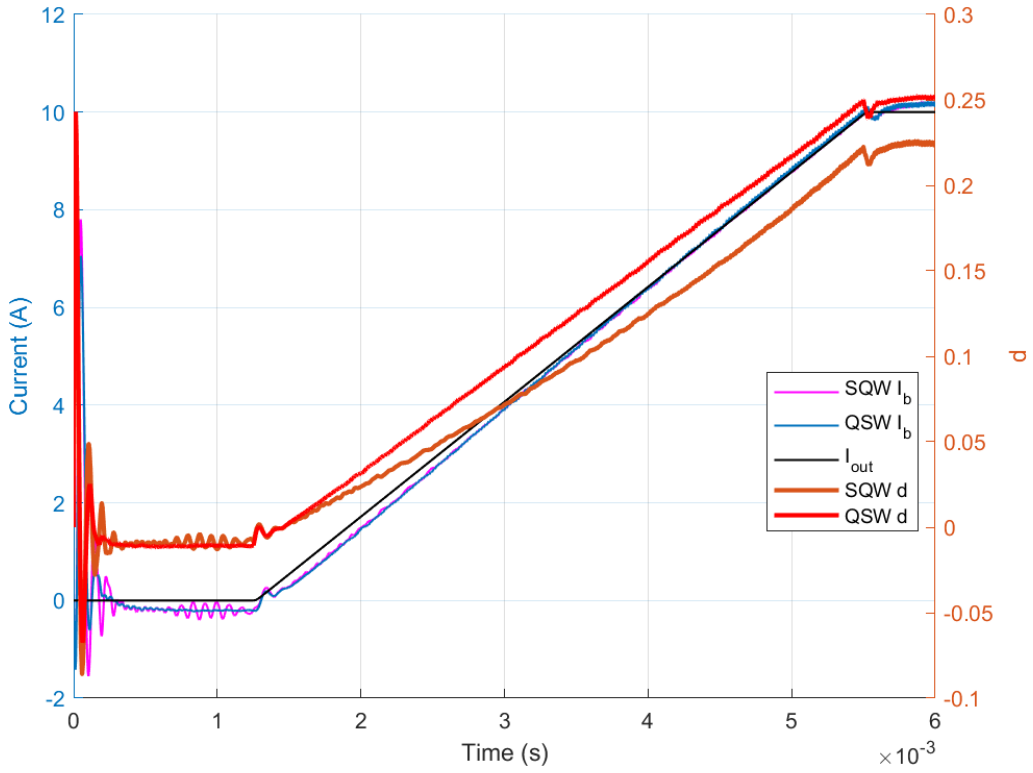

Figure A.3: Current I_b and duty ratio d compared between both modulations techniques with nominal V_a.

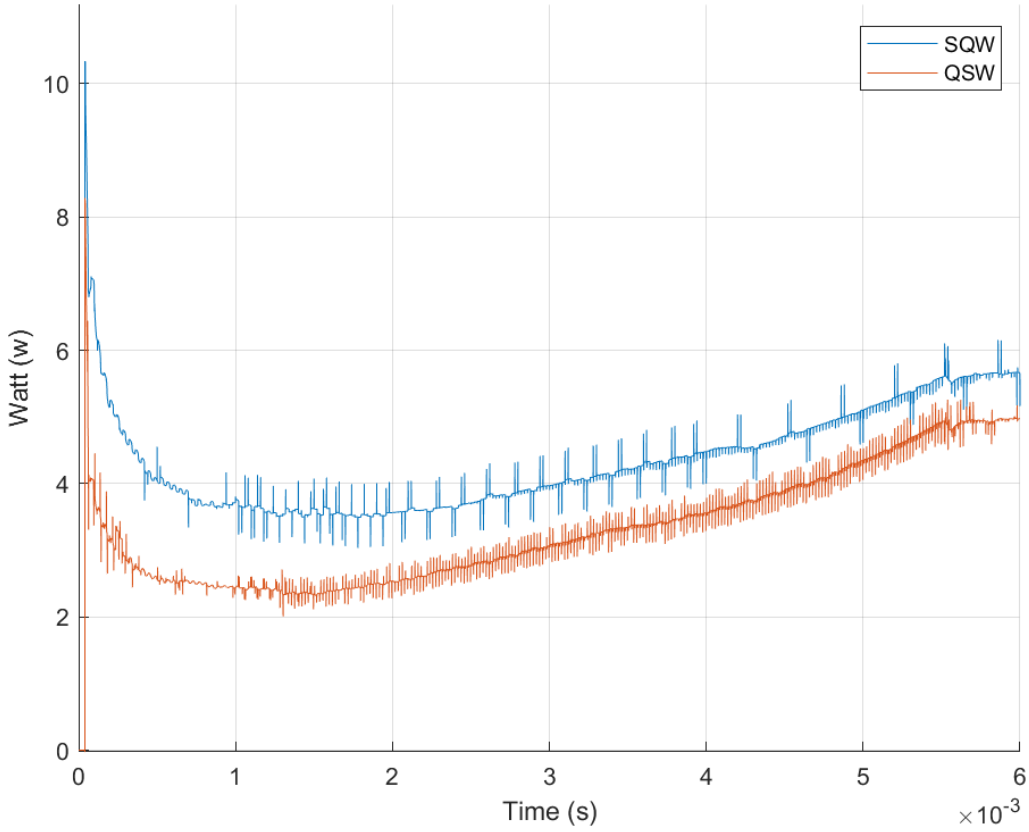

Figure A.4: Power dissipated at the MOSFETs compared between both modulations techniques with nominal V_a.

A.4.2 Charged battery voltage case

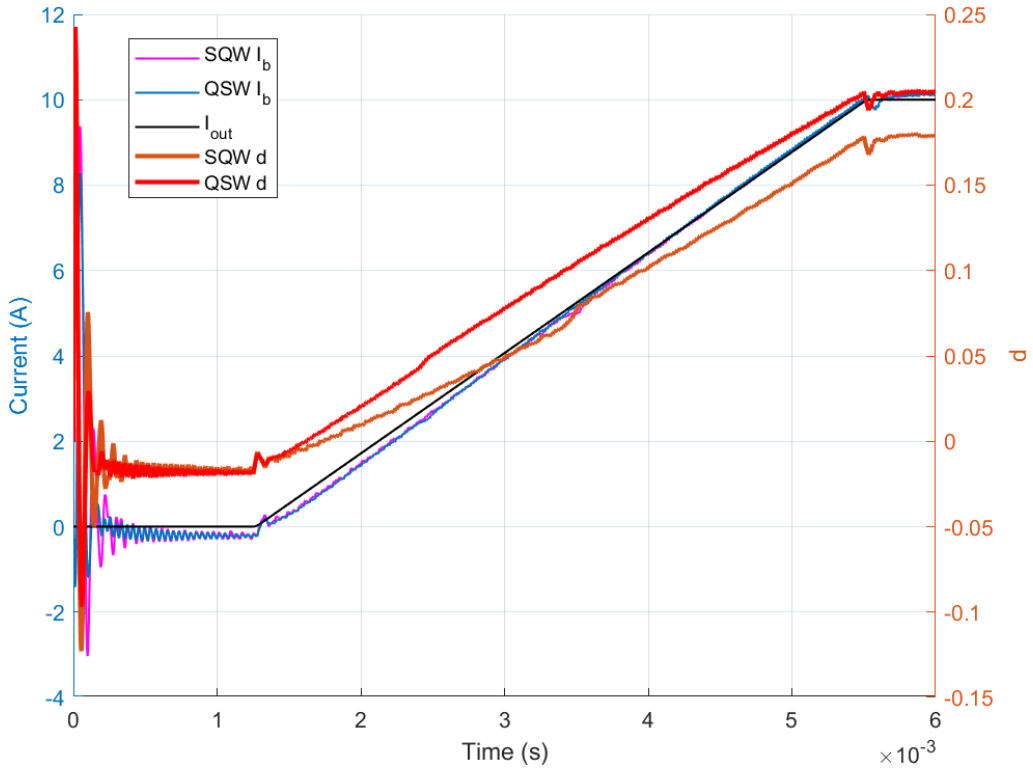

Figure A.5: Current I_b and duty ratio d compared between both modulations techniques with charged V_a.

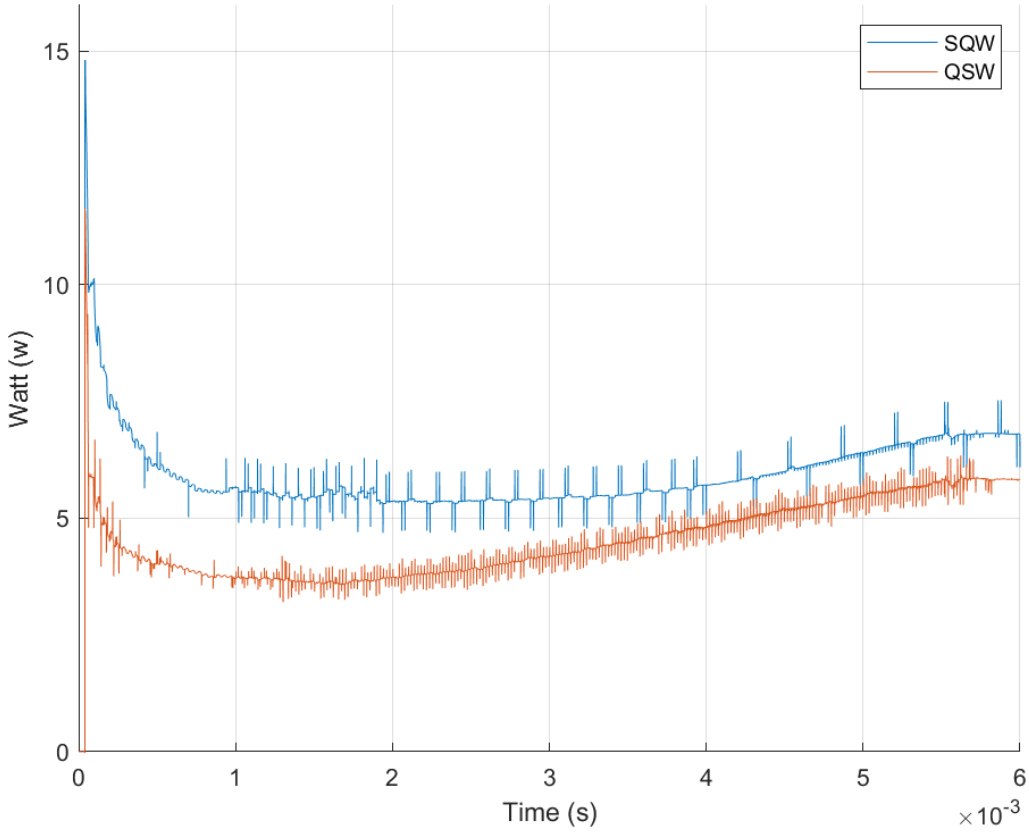

Figure A.6: Power dissipated at the MOSFETs compared between both modulations techniques with charged V_a.

A.4.3 Discharged battery voltage case

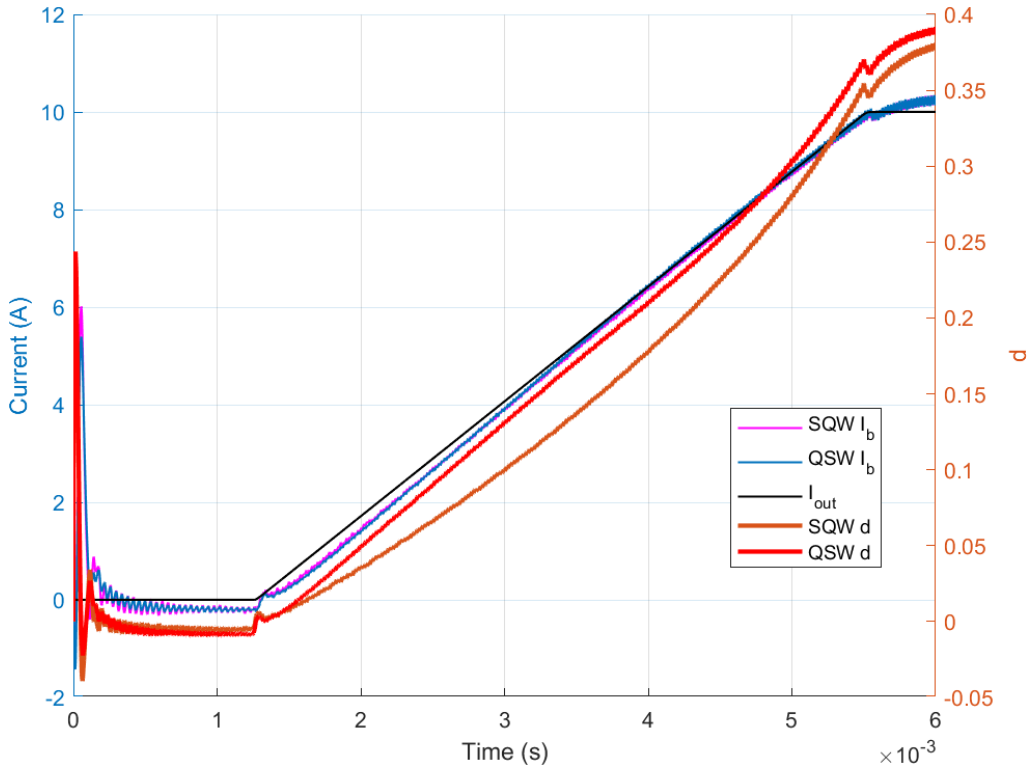

Figure A.7: Current I_b and duty ratio d compared between both modulations techniques with discharged V_a.

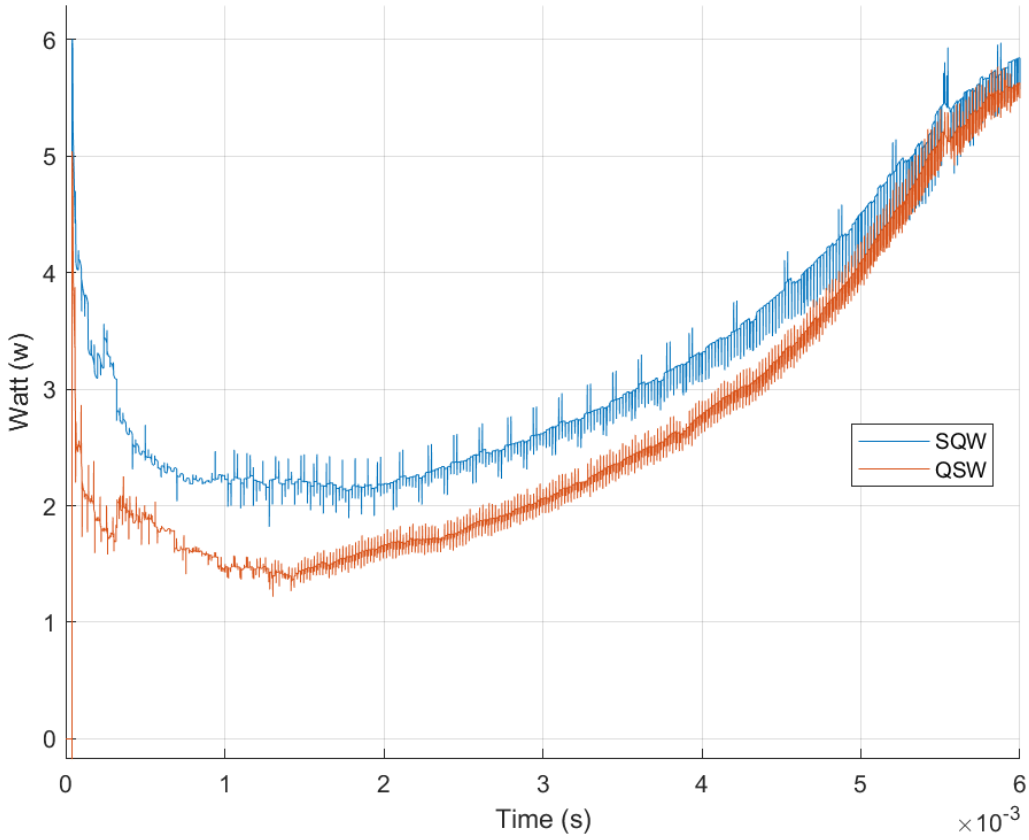

Figure A.8: Power dissipated at the MOSFETs compared between both modulations techniques with discharged V_a.

A.4.4 Cut-off battery voltage case

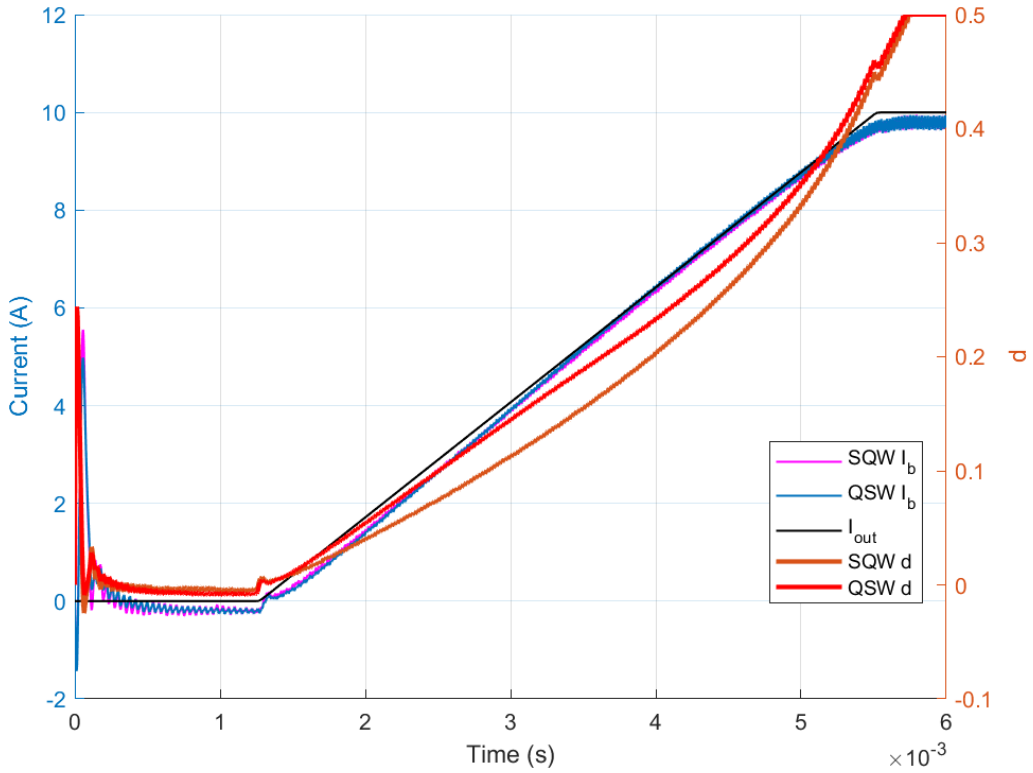

Figure A.9: Current I_b and duty ratio d compared between both modulations techniques with cut-off V_a.

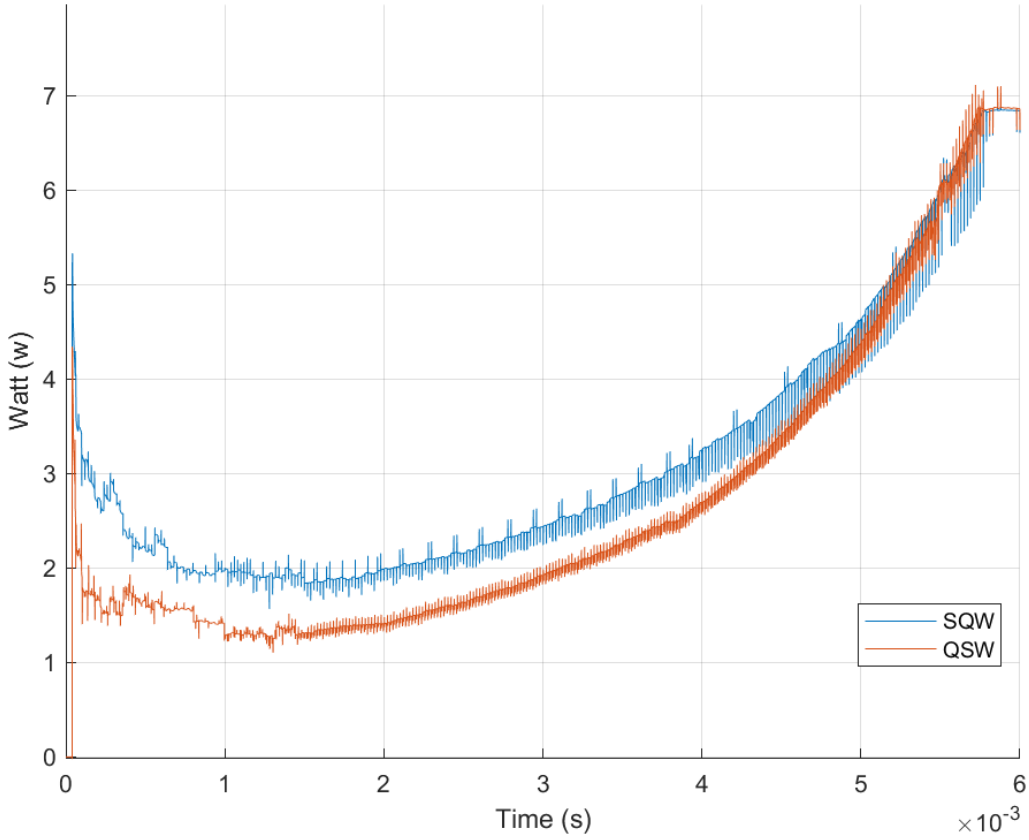

Figure A.10: Power dissipated at the MOSFETs compared between both modulations techniques with cut-off V_a.

A.4.5 Bidirectional Power Flow test

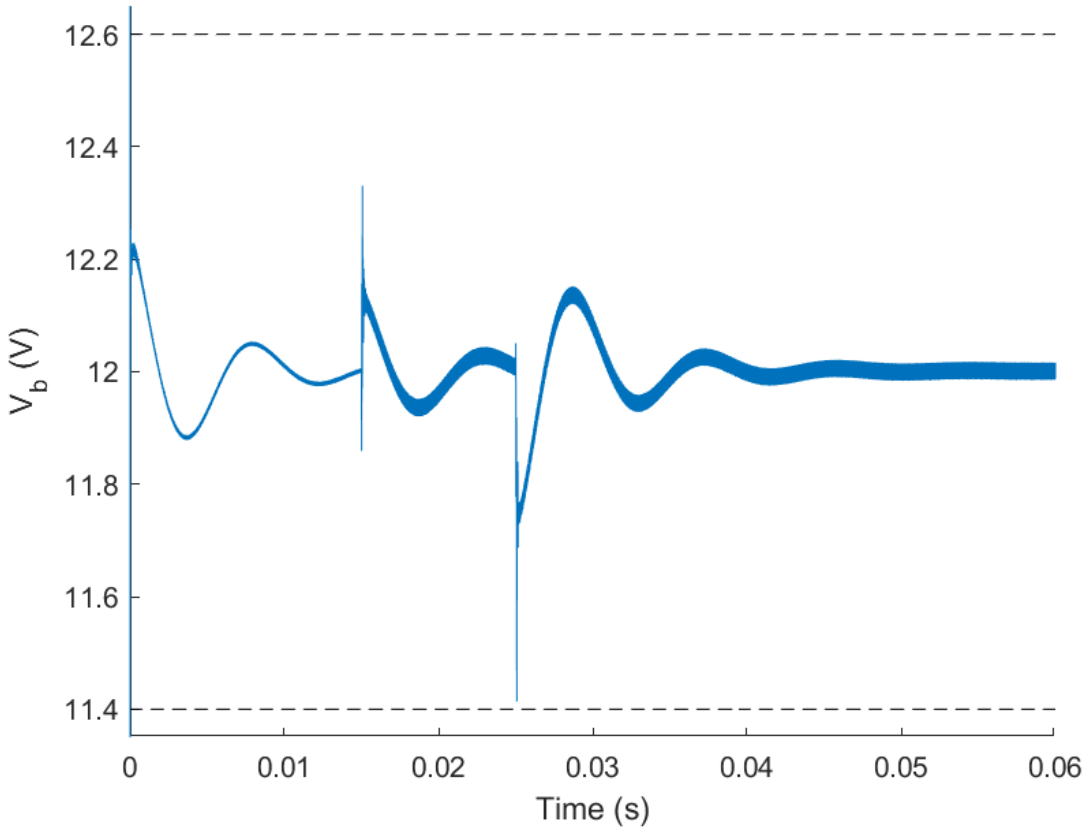

Figure A.11: Bidirectional power flow test of the converter with battery in charged state.

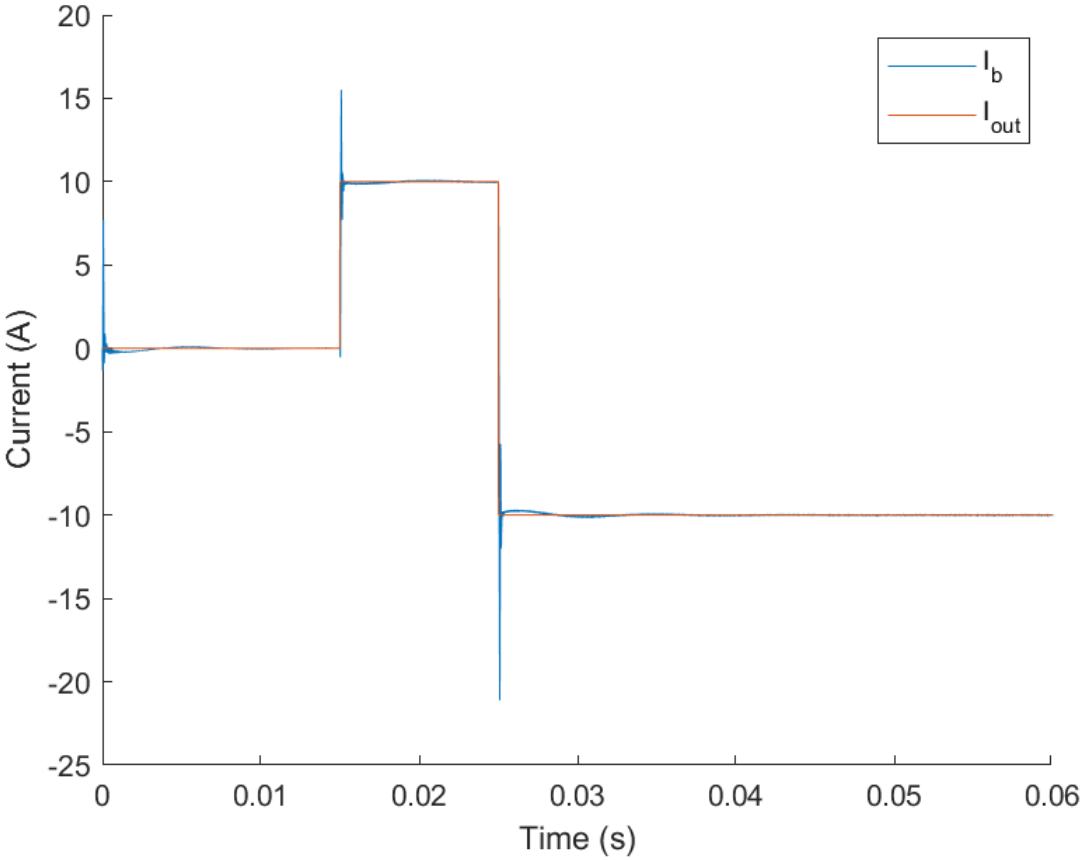

Figure A.12: Bidirectional power flow test of the converter with battery in charged state.

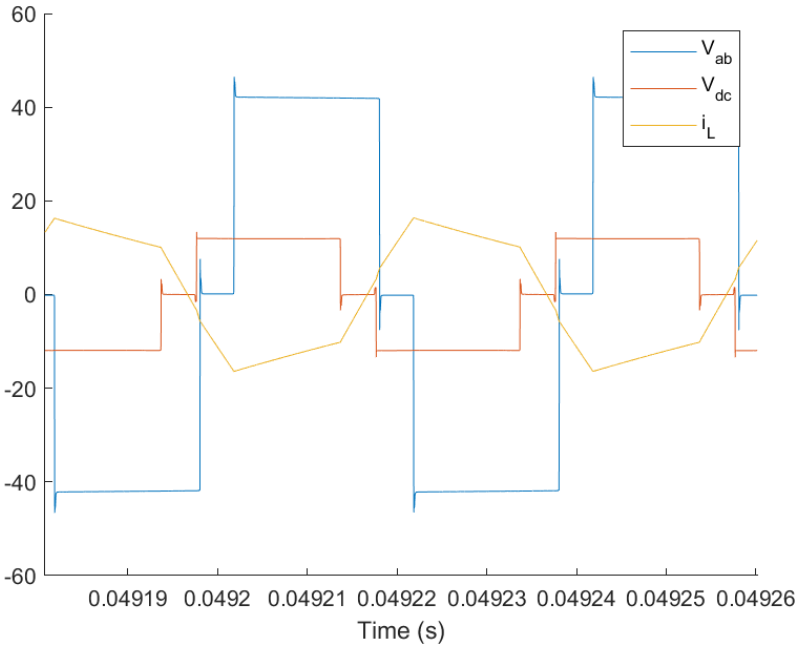

Figure A.13: Voltage at the active bridges terminals, and inductor current during reverse power flow with battery in charged state.

References

[1] Electrochemical Cells | Boundless Chemistry. URL: https://courses.lumenlearning.com/boundless-chemistry/chapter/electrochemical-cells/.

[2] A. Rahmoun and H. Biechl. Modelling of Li-ion batteries using equivalent circuit diagrams. *Przeglad Elektrotechniczny*, 88(7 B):152–156, 2012.

[3] Min Chen and G.A. Rincon-Mora. Accurate electrical battery model capable of predicting runtime and I-V performance. *IEEE Transactions on Energy Conversion*, 21(2):504–511, June 2006. Conference Name: IEEE Transactions on Energy Conversion. doi:10.1109/TEC.2006.874229.

[4] Towards a smarter battery management system: A critical review on optimal charging methods of lithium ion batteries | Elsevier Enhanced Reader. URL: https://reader.elsevier.com/reader/sd/pii/S0360544219312605?token=EA2FC6320A7C3C8EDDC0B34E53FC66AD4A01182F601EB19C6B3387A2424CA9ED218FCC9404868DDE18340B1A0D457FCF&originRegion=eu-west-1&originCreation=20220116135109, doi:10.1016/j.energy.2019.06.128.

[5] Mohamed Salem, Awang Jusoh, N. Rumzi N. Idris, Himadry Shekhar Das, and Ibrahim Alhamrouni. Resonant power converters with respect to passive storage (LC) elements and control techniques – An overview. *Renewable and Sustainable Energy Reviews*, 91:504–520, August 2018. URL: https://linkinghub.elsevier.com/retrieve/pii/S1364032118302302, doi:10.1016/j.rser.2018.04.020.

[6] Maria Teresa Outeiro, Giuseppe Buja, and Adriano Carvalho. Resonant converters for electric equipment power supply. *IECON Proceedings (Industrial Electronics Conference)*, pages 5065–5071, February 2014. Publisher: Institute of Electrical and Electronics Engineers Inc. doi:10.1109/IECON.2014.7049270.

[7] Shigenori Inoue and Hirofumi Akagi. A Bidirectional DC–DC Converter for an Energy Storage System With Galvanic Isolation. *IEEE Transactions on Power Electronics*, 22(6):2299–2306, November 2007. Conference Name: IEEE Transactions on Power Electronics. doi:10.1109/TPEL.2007.909248.

[8] Jun Min and Martin Ordonez. Bidirectional Resonant CLLC Charger for Wide Battery Voltage Range: Asymmetric Parameters Methodology. *IEEE Transactions on Power Electronics*, 36(6):6662–6673, June 2021. Conference Name: IEEE Transactions on Power Electronics. doi:10.1109/TPEL.2020.3033982.

[9] Shamini Dharmasena, Temitayo O. Olowu, and Arif I. Sarwat. Bidirectional AC/DC Converter Topologies: A Review. In *2019 SoutheastCon*, pages 1–5, April 2019. ISSN: 1558-058X. doi:10.1109/SoutheastCon42311.2019.9020287.

[10] Anwesha Mukhopadhyay and Vinod John. Constraints Based Design of DC side LC Filter for Single-Phase Voltage Source Converter. In *2020 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, pages 1–6, December 2020. doi:10.1109/PEDES49360.2020.9379380.

[11] Arthur Pini. The Basics of Isolation Transformers and How to Select and Use Them. URL: https://www.digikey.com/en/articles/the-basics-of-isolation-transformers-and-how-to-select-and-use-them.

[12] A.J. Forsyth and R.T. Naayagi. Bidirectional DC-DC converter for aircraft electric energy storage systems. In *5th IET International Conference on Power Electronics, Machines and Drives (PEMD 2010)*, pages 223–223, Brighton, UK, 2010. Institution of Engineering and Technology. URL: https://digital-library.theiet.org/content/conferences/10.1049/cp.2010.0184, doi:10.1049/cp.2010.0184.

[13] 2016. URL: https://www.vishay.com/docs/73217/an608a.pdf.

[14] Wen-Yeau Chang. The State of Charge Estimating Methods for Battery: A Review. *ISRN Applied Mathematics*, 2013:e953792, July 2013. Publisher: Hindawi. URL: https://www.hindawi.com/journals/isrn/2013/953792/, doi:10.1155/2013/953792.

[15] World electricity consumption. URL: https://www.statista.com/statistics/280704/world-power-consumption/.

[16] Ahmet Aktaş and Yağmur Kirçiçek. Chapter 5 - Solar Hybrid Systems and Energy Storage Systems. In Ahmet Aktaş and Yağmur Kirçiçek, editors, *Solar Hybrid Systems*, pages 87–125. Academic Press, 2021. URL: https://www.sciencedirect.com/science/article/pii/B9780323884990000057, doi:https://doi.org/10.1016/B978-0-323-88499-0.00005-7.

[17] Hamdi Abdi, Behnam Mohammadi-ivatloo, Saeid Javadi, Amir Reza Khodaei, and Ehsan Dehnavi. Chapter 7 - Energy Storage Systems. In G. B. Gharehpetian and S. Mohammad Mousavi Agah, editors, *Distributed Generation Systems*, pages 333–368. Butterworth-Heinemann, 2017. URL: https://www.sciencedirect.com/science/article/pii/B9780128042083000078, doi:https://doi.org/10.1016/B978-0-12-804208-3.00007-8.

[18] Rui Xiong, Hongwen He, Hongqiang Guo, and Yin Ding. Modeling for Lithium-Ion Battery used in Electric Vehicles. *Procedia Engineering*, 15:2869–2874, 2011. URL: https://linkinghub.elsevier.com/retrieve/pii/S1877705811020418, doi:10.1016/j.proeng.2011.08.540.

[19] D. Di Domenico, A. Stefanopoulou, and G. Fiengo. Lithium-ion battery state of charge and critical surface charge estimation using an electrochemical model-based extended Kalman filter. *Journal of Dynamic Systems, Measurement and Control, Transactions of the ASME*, 132(6), 2010. doi:10.1115/1.4002475.

[20] Claudio Ricardo Vergara Ramírez. Representing Battery Energy Storage in Electric Power System Studies. February 2015. Accepted: 2019-02-01T05:14:00Z. URL: https://repositorio-aberto.up.pt/handle/10216/78353.

[21] J. Xu. Design of constant current-constant voltage mode regulation in Li-ion battery charger. *Semicond Technol*, 36(4):291–295, 2011.

[22] Sheng Shui Zhang. The effect of the charging protocol on the cycle life of a Li-ion battery. *Journal of Power Sources*, 161(2):1385–1391, October 2006. URL: https://www.sciencedirect.com/science/article/pii/S0378775306011839, doi:10.1016/j.jpowsour.2006.06.040.

[23] P. H. L. Notten, J. H. G. Op het Veld, and J. R. G. van Beek. Boostcharging Li-ion batteries: A challenging new charging concept. *Journal of Power Sources*, 145(1):89–94, July 2005. URL: https://www.sciencedirect.com/science/article/pii/S0378775305000728, doi:10.1016/j.jpowsour.2004.12.038.

[24] Min Ye, Haoran Gong, Rui Xiong, and Hao Mu. Research on the Battery Charging Strategy With Charging and Temperature Rising Control Awareness. *IEEE Access*, 6:64193–64201, 2018. Conference Name: IEEE Access. doi:10.1109/ACCESS.2018.2876359.

[25] Ernesto Inoa and Jin Wang. PHEV Charging Strategies for Maximized Energy Saving. *IEEE Transactions on Vehicular Technology*, 60(7):2978–2986, September 2011. Conference Name: IEEE Transactions on Vehicular Technology. doi:10.1109/TVT.2011.2162085.

[26] Hector Eduardo Perez, Xiaosong Hu, Satadru Dey, and Scott J. Moura. Optimal Charging of Li-Ion Batteries With Coupled Electro-Thermal-Aging Dynamics. *IEEE Transactions on Vehicular Technology*, 66(9):7761–7770, September 2017. Conference Name: IEEE Transactions on Vehicular Technology. doi:10.1109/TVT.2017.2676044.

[27] Meng Xu, Rui Wang, Peng Zhao, and Xia Wang. Fast charging optimization for lithium-ion batteries based on dynamic programming algorithm and electrochemical-thermal-capacity fade coupled model. *Journal of Power Sources*, 438:227015, October 2019. URL: https://www.sciencedirect.com/science/article/pii/S0378775319310080, doi:10.1016/j.jpowsour.2019.227015.

[28] Alexander Bessman, Rudi Soares, Sunilkumar Vadivelu, Oskar Wallmark, Pontus Svens, Henrik Ekström, and Göran Lindbergh. Challenging Sinusoidal Ripple-Current Charging of Lithium-Ion Batteries. *IEEE Transactions on Industrial Electronics*, 65(6):4750–4757, June 2018. Conference Name: IEEE Transactions on Industrial Electronics. doi:10.1109/TIE.2017.2772160.

[29] Shin-Young Cho, Il-Oun Lee, Jae-Il Baek, and Gun-Woo Moon. Battery Impedance Analysis Considering DC Component in Sinusoidal Ripple-Current Charging. *IEEE Transactions on Industrial Electronics*, 63(3):1561–1573, March 2016. Conference Name: IEEE Transactions on Industrial Electronics. doi:10.1109/TIE.2015.2497661.

[30] Sunilkumar Vadivelu. *Investigation of sinusoidal ripple current charging techniques for Li-ion cells*. 2016. URL: http://urn.kb.se/resolve?urn=urn:nbn:se:kth:diva-195169.

[31] Mina Naguib, Phillip Kollmeyer, and Ali Emadi. Lithium-Ion Battery Pack Robust State of Charge Estimation, Cell Inconsistency, and Balancing: Review. *IEEE Access*, 9:50570–50582, 2021. Conference Name: IEEE Access. doi:10.1109/ACCESS.2021.3068776.

[32] Salah Alatai, Mohamed Salem, Dahaman Ishak, Himadry Shekhar Das, Mohammad Alhuyi Nazari, Ali Bughneda, and Mohamad Kamarol. A Review on State-of-the-Art Power Converters: Bidirectional, Resonant, Multilevel Converters and Their Derivatives. *Applied*

Sciences, 11(21):10172, October 2021. URL: https://www.mdpi.com/2076-3417/11/21/10172, doi:10.3390/app112110172.

[33] P Barrade. Switched-mode converters (one quadrant). page 24.

[34] Sajib Chakraborty, Hai-Nam Vu, Mohammed Mahedi Hasan, Dai-Duong Tran, Mohamed El Baghdadi, and Omar Hegazy. DC-DC Converter Topologies for Electric Vehicles, Plug-in Hybrid Electric Vehicles and Fast Charging Stations: State of the Art and Future Trends. *Energies*, 12(8):1569, April 2019. URL: https://www.mdpi.com/1996-1073/12/8/1569, doi:10.3390/en12081569.

[35] Maria Teresa Outeiro, Giuseppe Buja, and Dariusz Czarkowski. Resonant Power Converters: An Overview with Multiple Elements in the Resonant Tank Network. *IEEE Industrial Electronics Magazine*, 10(2):21–45, June 2016. Conference Name: IEEE Industrial Electronics Magazine. doi:10.1109/MIE.2016.2549981.

[36] Yu Du, Xiaohu Zhou, Sanzhong Bai, Srdjan Lukic, and Alex Huang. Review of non-isolated bi-directional DC-DC converters for plug-in hybrid electric vehicle charge station application at municipal parking decks. In *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 1145–1151, February 2010. ISSN: 1048-2334. doi:10.1109/APEC.2010.5433359.

[37] Jee-Hoon Jung, Ho-Sung Kim, Myung-Hyo Ryu, and Ju-Won Baek. Design Methodology of Bidirectional CLLC Resonant Converter for High-Frequency Isolation of DC Distribution Systems. *IEEE Transactions on Power Electronics*, 28(4):1741–1755, April 2013. Conference Name: IEEE Transactions on Power Electronics. doi:10.1109/TPEL.2012.2213346.

[38] Wei Chen, Ping Rong, and Zhengyu Lu. Snubberless Bidirectional DC–DC Converter With New CLLC Resonant Tank Featuring Minimized Switching Loss. *IEEE Transactions on Industrial Electronics*, 57(9):3075–3086, September 2010. Conference Name: IEEE Transactions on Industrial Electronics. doi:10.1109/TIE.2009.2037099.

[39] Huan Chen, Kai Sun, Languang Lu, Shuoqi Wang, and Minggao Ouyang. A Constant Current Control Method With Improved Dynamic Performance for CLLC Converters. *IEEE Transactions on Power Electronics*, 37(2):1509–1523, February 2022. Conference Name: IEEE Transactions on Power Electronics. doi:10.1109/TPEL.2021.3108631.

[40] Vishnu Mahadeva Iyer, Srinivas Gulur, and Subhashish Bhattacharya. Small-Signal Stability Assessment and Active Stabilization of a Bidirectional Battery Charger. *IEEE Transactions on Industry Applications*, 55(1):563–574, January 2019. Conference Name: IEEE Transactions on Industry Applications. doi:10.1109/TIA.2018.2871101.

[41] Tanya K. Gachovska and Jerry L. Hudgins. SiC and GaN Power Semiconductor Devices. In *Power Electronics Handbook*, pages 95–155. Elsevier, 2018. URL: https://linkinghub.elsevier.com/retrieve/pii/B9780128114070000052, doi:10.1016/B978-0-12-811407-0.00005-2.

[42] Amit Bhattacharjee and Issa Batarseh. Improved Response of Closed Loop Dual Active Bridge Converter Using Combined Feedback and Feed-forward Control. In *2019 IEEE Conference on Power Electronics and Renewable Energy (CPERE)*, pages 425–430, October 2019. doi:10.1109/CPERE45374.2019.8980044.

[43] Alberto Rodriguez Alonso, Javier Sebastian, Diego G. Lamar, Marta M. Hernando, and Aitor Vazquez. An overall study of a Dual Active Bridge for bidirectional DC/DC conversion. In *2010 IEEE Energy Conversion Congress and Exposition*, pages 1129–1135, Atlanta, GA, September 2010. IEEE. URL: https://ieeexplore.ieee.org/document/5617847/, doi:10.1109/ECCE.2010.5617847.

[44] Krismer Florian. *Modeling and optimization of bidirectional dual active bridge DC-DC converter topologies*. PhD thesis, ETH Zurich, 2010. Artwork Size: 1 Band Medium: application/pdf Pages: 1 Band. URL: http://hdl.handle.net/20.500.11850/152569, doi:10.3929/ETHZ-A-006395373.

[45] Amr Amin. A Transformerless Dual Active Bridge DC-DC Converter for Point-of-Load Power Supplies. page 86.

[46] Nuno Alves. High-Performance Isolated Bidirectional DC-DC Converter. Master's thesis, FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO, July 2017.