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Low-Power References for Subthreshold Circuits

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Abstract

Now more than ever the electronics area is in exponential growth, and one of the main topics the market demands for new developments is devices of low supply voltage and ultra-low power consumption, leading to a more responsible consumption in an ecological point of view. Thus, reducing those power levels has been a challenge throughout the years, having already been reduced mainly from the milliwatt to the dozens of nanowatt range, and in some cases, even reached the picowatt limit, by operating in the subthreshold region. Most of the electronic devices use references, either of voltage or current, which function is to provide a constant voltage or current, respectively, as well as an indispensable stability for the efficient operation of the sub-circuits of the device. Therefore, by reducing the power consumption, as well as the supply voltage of these building blocks, a giant leap forward a reduction of the overall consumption of the device is being taken.

In this dissertation is then done an extensive study of the state-of-the-art voltage references, which were organized in four typologies: bandgap voltage reference, voltage reference based on ΔV_{GS} (Gate-Source Voltage), voltage reference based on ZTC (Zero Temperature Coefficient) and voltage reference based on V_{TH} (Threshold Voltage). For each typology and respective circuits it is described their architecture, evaluated their performance and defined the main advantages and drawbacks. Subsequently, is proposed a voltage reference that achieves an output voltage of 536 mV, powered by a minimum supply voltage of 0.6 V, consuming 3.26 nW and with remarkably good performance to process, voltage and temperature (PVT) variations.

Regarding the current reference building block, a stability study of some state-of-the-art circuits is done with the purpose to demonstrate the differences between self-biased current references and the proposed one, which aims to solve the instability created by the feedback technique used for self-biasing, and, consequently, the design constrains that derive from ensuring that the circuit is stable and has a good performance. A point to highlight is that the proposed current reference uses the proposed voltage reference embedded. Additionally, a trimming circuit is created to improve the process instability resulting from the process corners. To conclude this topic, the proposed current reference achieves an output current of 1.05 nA, powered by a minimum supply voltage of 0.65 V and with a temperature coefficient performance of 71.86 $ppm/^{\circ}$C.

Last of all, a final solution is proposed which integrates the previous developed building blocks, the voltage reference and the current reference, along with an operational amplifier designed to work as a buffer in the subthreshold region. This structure achieves an output voltage reference of 536 mV and a power consumption of 128 nW, using a minimum supply voltage of 0.8 V. Regarding the performance parameters, the circuit obtains a temperature coefficient value of 18.5 $ppm/^{\circ}$C, in a temperature range from 0°C to 80°C, and a line sensitivity of -0.386 $\%/V$.

Keywords: CMOS, voltage reference, current reference, subthreshold, low voltage, ultra low power, trimming

Resumo

Atualmente, tem vindo a registrar-se um crescimento exponencial na área da eletrónica, sendo a procura de novos desenvolvimentos no mercado por dispositivos de baixo consumo de potência um dos tópicos mais em voga, pelo facto de levarem a um consumo mais responsável do ponto de vista ecológico. Reduzir estes níveis de potência representa um dos grandes desafios dos últimos anos, sendo que a maioria das reduções já alcançadas foram na ordem dos milliwatt para a ordem das dezenas de nanowatt e, em alguns casos, foi alcançado o limite de picowatt, quando a operar na região de *subthreshold*. A maioria dos aparelhos eletrónicos tem recurso a referências, de tensão ou de corrente, cuja função é fornecer, respetivamente, uma tensão ou corrente constante, assim como estabilidade, sendo esta indispensável para um funcionamento eficiente dos vários sub-circuitos do dispositivo. Assim, a redução do consumo de potência e da tensão de alimentação destas estruturas, é um enorme avanço na redução do consumo total do aparelho.

Ao longo desta dissertação é apresentado um estudo extenso do estado de arte das referências de tensão. Este estudo foi dividido em quatro tipologias distintas, sendo elas: a referência de tensão *bandgap*, a referência de tensão baseada em ΔV_{GS} (tensão gate-source), a referência de tensão baseada em ZTC (zero coeficiente de temperatura) e a referência de tensão baseada em V_{TH} (tensão de threshold). Para cada tipologia e respetivos circuitos é realizada uma descrição da arquitetura, avaliação da performance e ainda definidas as suas principais vantagens e desvantagens. De seguida, é proposta uma referência de tensão, que consegue atingir uma tensão de saída de 536 mV, com uma tensão mínima de alimentação de 0.6 V, consumindo 3.26 nW, com uma notável performance relativamente a variações de processo, tensão e temperatura (PVT).

Adicionalmente, tendo em consideração a estrutura da referência da corrente, procedeu-se a um estudo da estabilidade de alguns circuitos do estado de arte. Este estudo tem como objetivo demonstrar as diferenças entre as referências de corrente auto-polarizadas e a referência de corrente proposta nesta dissertação, com o intuito de resolver a instabilidade criada pela técnica de *feedback* frequentemente utilizada para auto-polarização e consequentes restrições de *design* que derivam da tentativa de assegurar a estabilidade e, ao mesmo tempo, a boa performance do circuito. É de relevar que a referência de corrente proposta integra a referência de tensão anteriormente desenvolvida. Adicionalmente, é apresentado um circuito *trimming* com o objetivo de melhorar a instabilidade de processo resultante dos corners avaliados. Para concluir, a referência de corrente proposta atinge uma corrente de saída de 1.05 nA, com uma tensão mínima de alimentação de 0.65 V e um coeficiente de temperatura de 71.86 $ppm/^{\circ}$C.

Por último, é proposta uma solução final que integra os blocos desenvolvidos anteriormente, a referência de tensão e a referência de corrente, em conjunto com um amplificador operacional dimensionado para trabalhar como um buffer e em *subthreshold*. Esta estrutura permitiu alcançar uma tensão de referência de 536 mV e um consumo de potência de 128 nW, utilizando uma tensão de alimentação mínima de 0.8 V. Relativamente aos parâmetros de performance, o circuito obtém um coeficiente de temperatura de 18.5 $ppm/^{\circ}$C, numa gama de temperatura entre 0°C e 80°C, e

uma regulação de -0.386 $\%/V$.

Palavras-chave: CMOS, referência de tensão, referência de corrente, *subthreshold*, baixa tensão de alimentação, ultrabaixa potência, *trimming*

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"Sé el cambio que deseas ver en el mundo."

Mahatma Gandhi

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Abbreviations and Acronyms

V_{GB}	Bandgap Voltage
V_{BE}	Base-Emitter Voltage
I_B	Bias Current
BJT	Bipolar Junction Transistor
k_B	Boltzmann Constant
C	Capacitor
L	Channel Length
W	Channel Width
CMOS	Complementary metal–oxide–semiconductor
CMRR	Common-Mode Rejection Ratio
CTAT	Complementary to Absolute Temperature
IREF	Currente Reference
I_D	Drain Current
DIBL	Drain Induced Barrier Lowering
Q	Electron Charge
C_{ox}	Gate Oxide Capacitor
V_{GS}	Gate-Source Voltage
IC	Integrated Circuit
LS	Line Sensitivity
I_{LOAD}	Load Current
LR	Load Regulation
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
μ	Mobility Parameter
NMOS	N-channel metal-oxide-semiconductor
OPAMP	Operational Amplifier
r_o	Output Resistance
PM	Phase Margin

PMOS	P-channel metal-oxide-semiconductor
P_{cons}	Power Consumption
PSRR	Power Supply Rejection Ratio
PTAT	Proportional to Absolute Temperature
PVT	Process, Voltage, Temperature
R	Resistor
η	Subthreshold Slope Factor
I_{DD}	Supply Current
V_{DD}	Supply Voltage
T	Temperature
TC	Temperature Coefficient
V_T	Thermal Voltage
V_{TH}	Threshold Voltage
gm	Transconductance
V_{REF}	Voltage Reference
VTP	Voltage Temperature Parameter
ZTC	Zero Temperature Coefficient
ZVT	Zero Threshold Voltage

Chapter 1

Introduction

The world is in need of more ecological technologies and the first step towards the improvement is to have more responsibility with energy consumption. The utilisation of electronic devices is in exponential increase and that leads to an electronic component consumption higher than ever. In order to decrease unnecessary consumption and avoid waste, it is essential that the lifetime of the equipment is reasonably long. This way, the development of analog circuits of low supply voltage and ultra low power consumption is of extreme importance due to the requirements of the different technological equipment, such as, mobile devices, implantable medical devices, monitoring systems, intelligent sensor networks, among others. These devices require an ultra low power consumption once one of their characteristics is to have a low duty cycle, therefore, managing the energy consumption, specially while the equipment is in IDLE mode, i.e. not operating while waiting to take some action, is proved to increase in a significant way their lifetime, in fact it can change from one month to five years, and hence more ecologic and economic devices can be manufactured.

The key building blocks for the development of circuits of ultra low power consumption are voltage and current references, which function is to provide, respectively, a constant output voltage and current, as well as a stability indispensable for the efficient operation of the sub-circuits of the device. This stability should not be affected by process, voltage or temperature variations. These references assists both digital and analog blocks, which include voltage regulators, AD/DA converters, radio frequency communication blocks, operational amplifiers, comparators, oscillators, PLLs, among others [1, 2].

Figure 1.1 is a logarithmic chart of the power consumption of several voltage references throughout the last two decades. All these voltage references, which will be analysed with more detail in chapter 2, are implemented in complementary metal–oxide–semiconductor (CMOS) technology, being most of them low voltage, i.e. powered by supply voltage lower than 1 V. The dotted line represents the commence of the picowatt power consumption. The voltage references which power consumption is in this order of magnitude are recent and few, however, the technology nowadays is evolving towards this path. Therefore, the optimization of voltage references is an essential aspect for a successful performance of ultra low power consumption circuits.

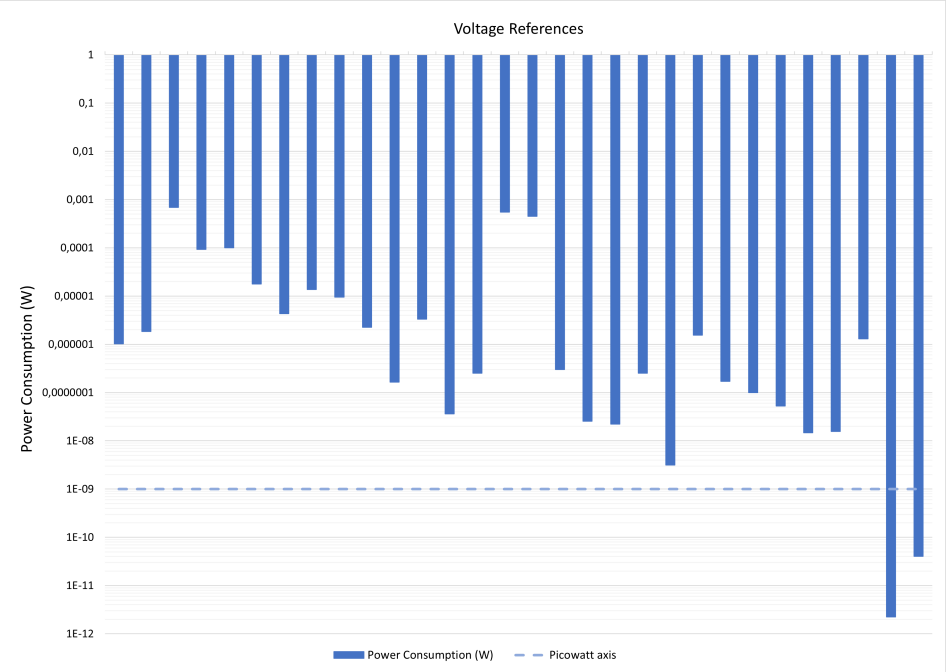


Figure 1.1: Power consumption comparison of voltage references (logarithmic scale)

1.1 Objectives

Bearing in mind the importance of low-power references for ecological and economic analog circuits, the following objectives were established:

- A study of the state-of-the-art voltage and current references.
- The development of a voltage reference, with the aim of achieving the lowest power dissipation possible along with good performance outcomes and low PVT sensibility.
- The development of a current reference that uses a different architecture from feedback for self-biasing.
- The development of a trimming circuit in order to improve the variations caused by the process.
- The layout development with a focus on minimum area.

At the end, it is proposed a final solution that integrates the voltage reference, the current reference and an operational amplifier designed to work has a buffer and on a subthreshold operation regime.

All the circuits are implemented in CMOS 0.18 μm technology, in order to more effectively comply with the necessary performance and design requirements, such as the weak-inversion operation regime, low supply voltage and area, among others. All the designs were created using Cadence Virtuoso Analog Design Environment and validated in simulation.

1.2 Organisation of this document

This document is composed by five chapters, besides the Introduction. Chapter 2 introduces the literature review of CMOS voltage references organised by typologies. In chapter 3 and 4 is presented the study and developed blocks of voltage reference and current reference, respectively. Chapter 5 describes the complete proposed solution, while chapter 6 concludes the dissertation with some final insights and suggestions for future work on this topic.

Chapter 2

CMOS Voltage References

In micro-electronics one of the most important building blocks is the voltage reference, regardless of the circuit system being analog, digital or mixed-signal, which purpose is to generate a constant output voltage for several other components of the circuit [2]. Theoretically, this output voltage does not depend on the supply voltage, load current or the passage of time and has to be insensitive to process, voltage and temperature variations [1]. There is a variety of circuits in which voltage references find applications, such as, analog to digital (A/D) and digital to analog (D/A) converters, power supplies, portable mobile devices, implantable medical devices, dynamic random-access memory (DRAM), flash memories, smart sensor networks, among others. Moreover, the exactness of the reference voltage determines the performance of coders and decoders and data converters [3].

Henceforth, these devices have to operate with low supply voltages and with ultra-low power consumption, the last one in the order of picowatts, once the usage of micro batteries and ecological energy sources is increasing and consequently, the circuits need to be able to get the necessary energy from this low energy sources [2], what makes energy consumption the main requirement for voltage references, along with size.

With regards to the performance of a voltage reference, the following parameters need to be measured [4]:

- Line Sensitivity (LS) that specifies the variation of the output voltage (V_{REF}) with respect to the input voltage variation (V_{DD}), at the nominal temperature (T):

$$LS(\%/V) = \left(\frac{V_{REF_{@V_{DDmax}}} - V_{REF_{@V_{DDmin}}}}{V_{REF_{@V_{DDnom}}}}\right)\left(\frac{1}{V_{DD_{max}} - V_{DD_{min}}}\right) \cdot 100 \tag{2.1}$$

- Temperature Coefficient (TC) that specifies the variation of the output voltage according to temperature, under the nominal V_{DD}:

$$TC(ppm/^{\circ}\mathrm{C}) = \left(\frac{V_{REF_{max}} - V_{REF_{min}}}{V_{REF_{@T_{nom}}}}\right)\left(\frac{1}{T_{max} - T_{min}}\right) \cdot 10^6 \tag{2.2}$$

The authors in [5] defined an alternative parameter for LS and TC, once these two parameters present some disadvantages, for instance, they are evaluated at the nominal supply voltage for LS or nominal temperature for TC, which limits the global information about the reference voltage variations, another aspect is that the output voltage dependence on temperature and supply voltage is not linear, therefore the values of these parameters are measured in a specific range, not enabling the analysis for a larger or smaller range. In order to solve these limitations, the authors present the Voltage Temperature Parameter (VTP):

$$VTP(\%) = \frac{V_{REF_{max}} - V_{REF_{min}}}{V_{REF_{mean}}} \cdot 100\% \tag{2.3}$$

- Power Supply Rejection Ratio (PSRR) that specifies the variation of the output voltage according with the noise of the input voltage:

$$PSRR(dB) = 20\log\left(\frac{\Delta V_{DD}}{\Delta V_{REF}}\right) \tag{2.4}$$

- Load Regulation (LR) that specifies the variation of the output voltage with respect to the load current variation:

$$LR(ppm/mA) = \left(\frac{V_{REF_{@I_{LOADmax}}} - V_{REF_{@I_{LOADmin}}}}{V_{REF_{@I_{LOADnom}}}}\right)\left(\frac{1}{I_{LOAD_{max}} - I_{LOAD_{min}}}\right) \cdot 10^6 \tag{2.5}$$

- Power consumption which is the main parameter to be optimized without jeopardising the values of the above mentioned parameters:

$$P_{cons}(W) = V_{DD} \cdot I_{DD} \tag{2.6}$$

The following subsections present the state of the art of the various voltage references organized in four typologies: bandgap voltage reference, voltage reference based on ΔV_{GS}, voltage reference based on zero temperature coefficient (ZTC) and voltage reference based on V_{TH}. The last section presents some ultra-low power voltage reference.

2.1 Bandgap Voltage Reference

The Bandgap Voltage Reference circuit concept was first published by David Hilbiber in 1964 [6], however, the first widely used bandgap voltage reference was designed in 1974 by Paul Brokaw whose creation result from an successful attempt of improving the voltage reference with base-emitter temperature compensation designed by Robert Widlar in 1971 [4]. The Brokaw bandgap voltage reference circuit [7], shown in figure 2.1, was implemented using bipolar junction transistors (BJT) and the main idea of the circuit typology is to combine two voltages with opposite temperature behaviours in order to achieve temperature independence. The process consists in

summing a voltage that increases with temperature, a PTAT (proportional to absolute temperature), to a voltage that decreases with temperature, a CTAT (complementary to absolute temperature), this way it is possible to produce a reference voltage with near-zero temperature dependence of 1.205 V, which is the bandgap voltage of silicon [8].

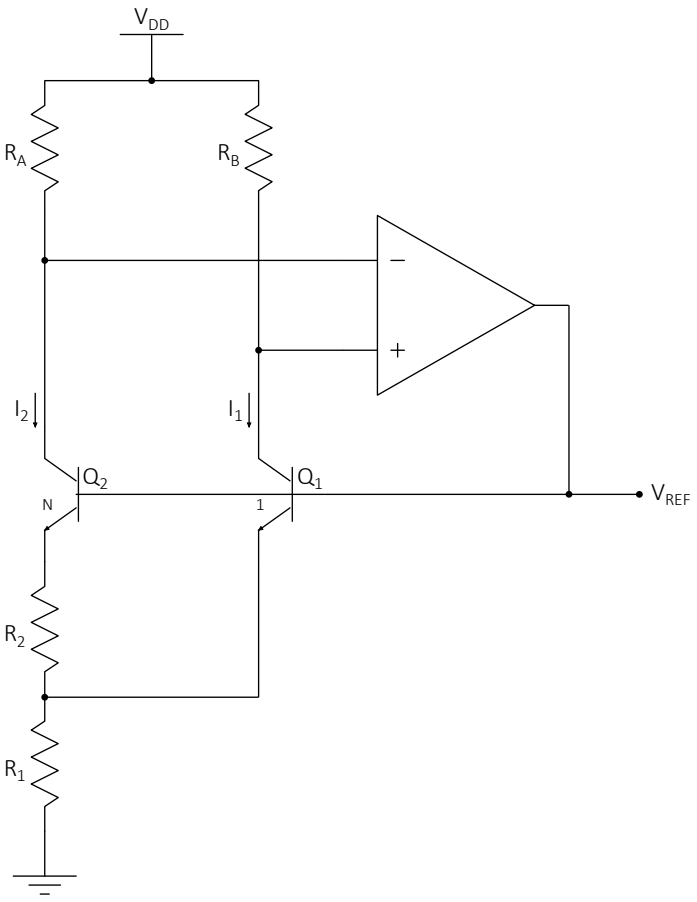


Figure 2.1: Brokaw voltage reference

In the late seventies, bandgap voltage references started to be implemented in CMOS technology, once subthreshold MOS transistors became available. This evolution in technology resulted in the development of the most commonly used CMOS bandgap voltage reference nowadays, a circuit design by Hironori Banba *et al.* in 1999 [9].

The voltage reference proposed by Banba *et al.*, shown in figure 2.2, solves a limitation present in Widlar voltage reference: the minimum supply voltage is 1.25 V, and so it is not able to provide output voltages lower than that value, which is a barrier in the evolution of integrated circuits (IC). Therefore, Banba *et al.* builds a low-power voltage reference capable of operating with a voltage supply lower than 1 V. It is implemented in 0.4 μm CMOS and the operating method, conversely to the sum of two voltages mentioned above, consists in the sum of two currents generated by only one feedback loop: one is proportional to V_{BE} and so it decreases with temperature, and the other is proportional to ΔV_{BE} then it increases with temperature. A second effect of this circuit is the first order cancellation of the thermal coefficient of the resistors. This effect is achieved due to

the existence of R_3 in the output voltage equation, as shown in (2.10), whose thermal coefficient cancels the ones of R_2 and R_0.

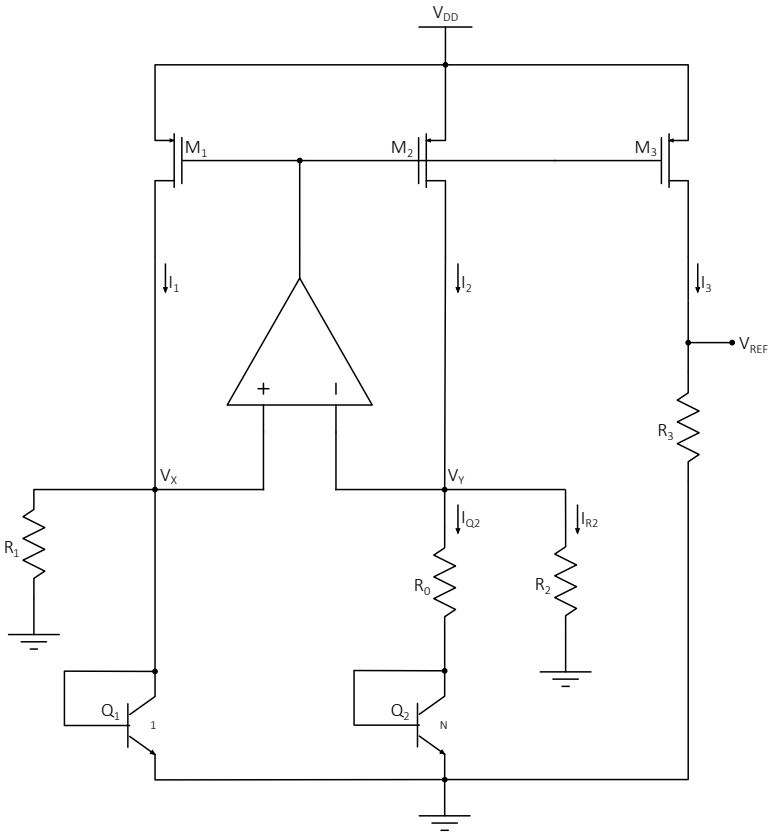


Figure 2.2: Banba voltage reference

The PMOS transistors M_1, M_2 and M_3 have the same dimensions, the resistors R_1 and R_2 are equal, therefore, the voltages V_X and V_Y are also equal and the currents I_1, I_2 and I_3 form a current mirror. The output voltage can be written as:

$$V_{REF} = R_3 \cdot I_3, \tag{2.7}$$

where I_3 corresponds to the sum of two currents: $I_{R2} + I_{Q2}$:

$$I_{R2} = \frac{V_Y}{R_2} = \frac{V_X}{R_2} = \frac{V_{BE_1}}{R_2}, \tag{2.8}$$

$$I_{Q2} = \frac{V_Y - V_{BE_2}}{R_0} = \frac{V_{BE_1} - V_{BE_2}}{R_0} = \frac{\Delta V_{BE}}{R_0} = \frac{V_T \cdot ln(N)}{R_0}, \tag{2.9}$$

where V_{BE} can be expressed as $V_{BE} = V_{BG} - \gamma \cdot T$, i.e. the sum of the bandgap voltage of the silicon with a negative dependence temperature coefficient, and $V_T = (k_B \cdot T)/Q$ is the thermal voltage which has a positive dependence on temperature (k_B is the Boltzmann constant, Q the electron charge and T the absolute temperature). Therefore, I_{R2} being proportional to V_{BE_1} forms a CTAT, and I_{Q2} being proportional to V_T forms a PTAT. Thus, the output voltage given by (2.7) can be

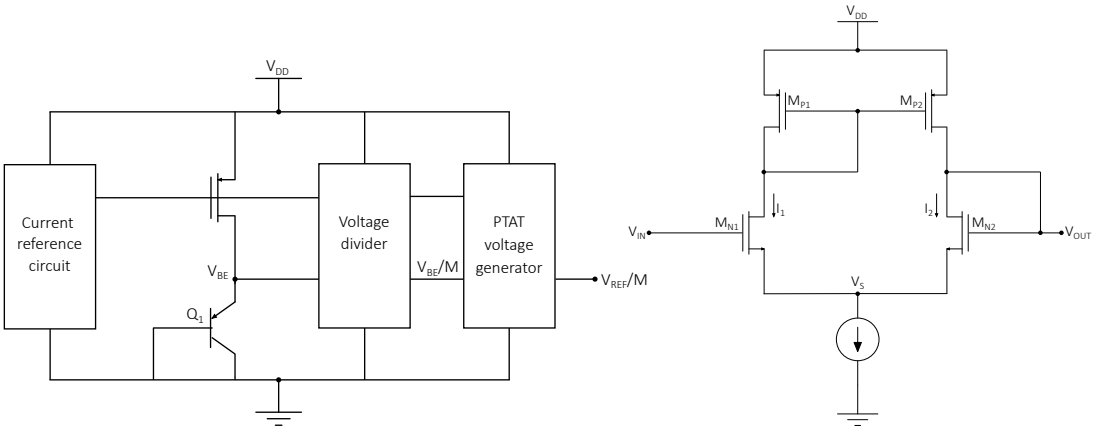
rewritten as:

$$V_{REF} = R_3 \cdot \left(\frac{V_{BE_1}}{R2} + \frac{\Delta V_{BE}}{R_0} \right). \tag{2.10}$$

and achieves an experimental minimum value of 518 mV using a supply voltage of 2.1 V, in a temperature range from 27°C to 125°C. Moreover, the simulated results show that the power consumption of the circuit is 1.85 μW with a minimum supply voltage of 0.84 V, in a total area of 0.1 mm^2. Note that there is a discrepancy between the supply voltage used for the experimental results and the one used for simulated results, which stem from the need to utilise native transistors once the transistors designed for the experiment were not suitable for the low-voltage operation of the 0.4 μm flash memory, which limited the experimental supply voltage to a high value [9].

Although the values presented above represent a big improvement for bandgap voltage references, at that time, in the low-power scope, this architecture presents some disadvantages, such as, the usage of an amplifier for error correction which provides insensitivity to variations of temperature and supply voltage at the expense of power consumption and minimum supply voltage limitations [1], also, the amplifier together with the need of resistors with a high resistance generate a significant area overhead [2].

More recently, in 2013, Yuji Osaki *et al.* [10] develops a resistor-less sub-bandgap voltage reference, based on a circuit of Tetsuya Hirose *et al.* [11], published in 2010, and achieves record outcomes for this typology. The Osaki *et al.* sub-bandgap voltage reference, which schematic is shown in figure 2.3a, is implemented in 0.18 μm CMOS and is composed by a nano-ampere current reference circuit, a bipolar transistor, a voltage divider and a PTAT voltage generator.



(a) Circuit schematic (b) PTAT voltage generator

Figure 2.3: Osaki voltage reference

The circuit has several particularities: one is the usage of a voltage divider, which function is to divide the base-emitter voltage of the bipolar transistor $\left(V_{BE/M}\right)$, this way it is possible to lower the value of both the supply voltage and the reference voltage. Another characteristic is the use of a PTAT voltage generator composed by several differential pairs in cascade and a current mirror, where one stage is shown in figure 2.3b, and which function is to generate a voltage that

has a positive dependence on temperature in order to cancel the negative dependence on temperature of V_{BE}. Once the usage of only one differential pair is not enough to nullify the negative temperature dependence above mentioned, there is the necessity of using a cascade of differential pairs, with different aspect ratios, composed by as many stages as needed until the cancellation effect is achieved. The third particularity is that the voltage divider and the PTAT voltage generator were design without resistors, and this is an advantage in the area, voltage supply and power consumption ambit, reaching values of power in the order of the nano-watts. Moreover, the voltage reference uses a current reference circuit which purpose is to generate a stable current that is independent of the supply voltage, in order to avoid variations of V_{BE}.

The reference voltage can be written as the sum of the output of the voltage divider with the voltage generated by the PTAT. The PTAT voltage generated, described in the second term of the equation (2.11), result from the subthreshold current equation once almost all the MOSFETs of the PTAT operate in the weak-inversion region:

$$V_{REF} = \frac{V_{BE}}{M} + \eta \cdot V_T \cdot ln\left(\prod_{i=1}^{N} \frac{(W/L)_{N_{2i-1}} \cdot (W/L)_{P_{2i}}}{(W/L)_{N_{2i}} \cdot (W/L)_{N_{2i-1}}}\right), \tag{2.11}$$

where $(W/L)_N$ and $(W/L)_P$ correspond to the aspect ratios of the differential pairs and their product come from the cascade of N stages. By expressing V_{BE} and V_T as above-mentioned, (2.11) can be rewritten as:

$$V_{REF} = \frac{V_{BG}}{M} + \left(-\frac{\gamma}{M} + \frac{\eta \cdot k_B}{Q} \cdot ln\left(\prod_{i=1}^{N} \frac{(W/L)_{N_{2i-1}} \cdot (W/L)_{P_{2i}}}{(W/L)_{N_{2i}} \cdot (W/L)_{N_{2i-1}}}\right)\right) \cdot T, \tag{2.12}$$

however, due to the role of the PTAT, the second term of the equation is canceled and a zero-temperature coefficient output voltage is obtained:

$$V_{REF} = \frac{V_{BG}}{M}. \tag{2.13}$$

achieving an experimental value of 548 mV using a $M = 2$. The power consumption of the circuit is 52.2 nW, powered by a supply voltage of 0.7 V in a total area of 0.025 mm^2. The values of the minimum supply voltage, power consumption and area of this architecture represent record values for bandgap voltage references.

Table 2.1 summarizes the performance characteristics of bandgap voltage references.

2.2 Voltage Reference based on ΔV_{GS}

The voltage reference based on ΔV_{GS} is a typology presented by Ka Nang Leung *et al.* [17] and Giuseppe De Vita *et al.* [18] and consists in achieving a reference voltage essentially through the difference between the gate–source voltages of two MOS transistors that have the same absolute values of threshold voltage.

Table 2.1: Comparison of Bandgap Voltage References

	[9]	[12]	[13]	[14]	[15]	[16]	[10]
Tech (CMOS)	0.4 μm	0.35 μm	0.8 μm	0.6 μm	0.5 μm	0.16 μm	0.18 μm
V_{DDmin} (V)	0.84	0.85	1	0.98	0.95	1.1	0.7
Power (μW)	1.848	1.02	92	17.64	9.5	1.54	0.0525
TC ($ppm/°C$)	116	57	19	15	17	30	114
Temp. range (°C)	[27,125]	[-20,100]	[0,80]	[0,100]	[-40,125]	[-45,135]	[-40,120]
LS ($\%/V$)	0.1	-	-	0.73	-	-	-
Area (mm^2)	0.1	0.063	0.25	0.24	1.0904	0.0025	0.246
PSRR (dB)							
@100Hz	-	-	-	-44	-	-	-56
@10MHz	-	-	-	-17	-	-	-
V_{REF} (mV)	518	650	536	6033	628	944	548

In 2003, Leung *et al.* implements the circuit shown in figure 2.4 using 0.6 μm CMOS technology, which is composed by a current generator and a core circuit formed a PTAT generator, two resistors and two transistors operating in saturation region, a PMOS and a NMOS.

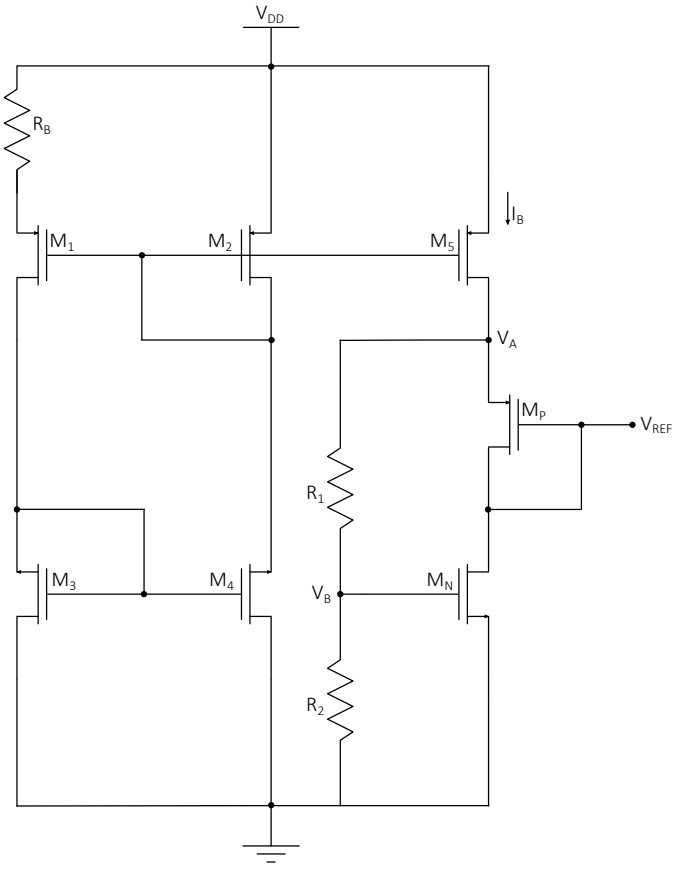


Figure 2.4: Leung voltage reference

To achieve the output voltage equation, we have to keep in mind that $V_A = V_{REF} + V_{GS_P}$, $V_B = V_{GS_N}$, being V_{GS_N} and V_{GS_P} the gate-source voltage of the NMOS and the PMOS respectively, and assume that the majority of the bias current (I_B) generated by the PTAT flows through the reference transistors, therefore:

$$\frac{V_{GS_N} - (V_{REF} + V_{GS_P})}{R_1} + \frac{V_{GS_N}}{R_2} = 0, \tag{2.14}$$

Reorganising the previous equation, the voltage reference can be written as:

$$V_{REF} = \left(1 + \frac{R_1}{R_2}\right) \cdot V_{GS_N} - |V_{GS_P}| \tag{2.15}$$

In the saturation region the current equation is given by:

$$I_{sat} = \frac{1}{2} \cdot K \cdot (V_{GS} - V_{TH})^2 \tag{2.16}$$

where $K = \mu \cdot C_{ox} \cdot (W/L)$, being μ the mobility parameter, C_{ox} the gate oxide capacitor, W/L the size ratio of the transistor and V_{TH} the threshold voltage. From (2.15) and (2.16), and knowing that the threshold voltages of both transistors are symmetric:

$$V_{REF} = \frac{R_1}{R_2} \cdot V_{TH} + \sqrt{2 \cdot I_B} \cdot \left[\left(1 + \frac{R_1}{R_2}\right) \cdot \sqrt{\frac{1}{K_N}} - \sqrt{\frac{1}{K_P}}\right] \tag{2.17}$$

As expressed in (2.17), the output voltage has a temperature dependence intrinsic of the threshold voltages, the mobility and the bias current. The temperature dependence is attenuated via two techniques: by sizing the resistors ratio so that the temperature dependence of the threshold voltage is compensated, and by dimensioning the transistors size as a mean of compensating the mobility temperature dependence at the reference temperature [19].

This architecture achieved a reference voltage of 309 mV and a power consumption of 13.58 μW using a minimum a supply voltage of 1.4 V, in a total area of 0.055 mm^2. Regarding the performance measures, the circuit reaches a TC of 36.9 $ppm/°C$ in a temperature range from 0°C to 100°C, and a LS value of 0.012 $\%/V$.

The main advantage of this voltage reference is being executed in a standard CMOS process, on the other hand, the design has a large area due to the dependence on the matching of the resistors [1, 20], and despite the implementation of some methods to achieve temperature independence, this dependency is not completely cancelled [17].

In 2006, Vita *et al.* implements a voltage reference using the same concept presented above but is able to solve numerous previous limitations, such as, the cancellation of second-order channel length modulation and body effects and achieves a complete suppression of the temperature dependence of mobility in the whole temperature range. The circuit, shown in figure 2.5, uses 0.35 μm CMOS technology, operates in saturation region and is composed by a current generator and a core circuit of four transistors. The advantages of this architecture are several. In relation to

the core circuit, an active voltage divider is used, formed by M_9 and M_{10}, instead of a passive resistive divider, which results, firstly, in a compensation of the channel-length modulation and body effects, and subsequently, the TC value decreases. Secondly and together with the resistor-less current generator, there is a significant reduction of the bias current required, which consequently improves the area and the power consumption. Lastly, the structure of the current generator is the key for obtaining mobility temperature independence.

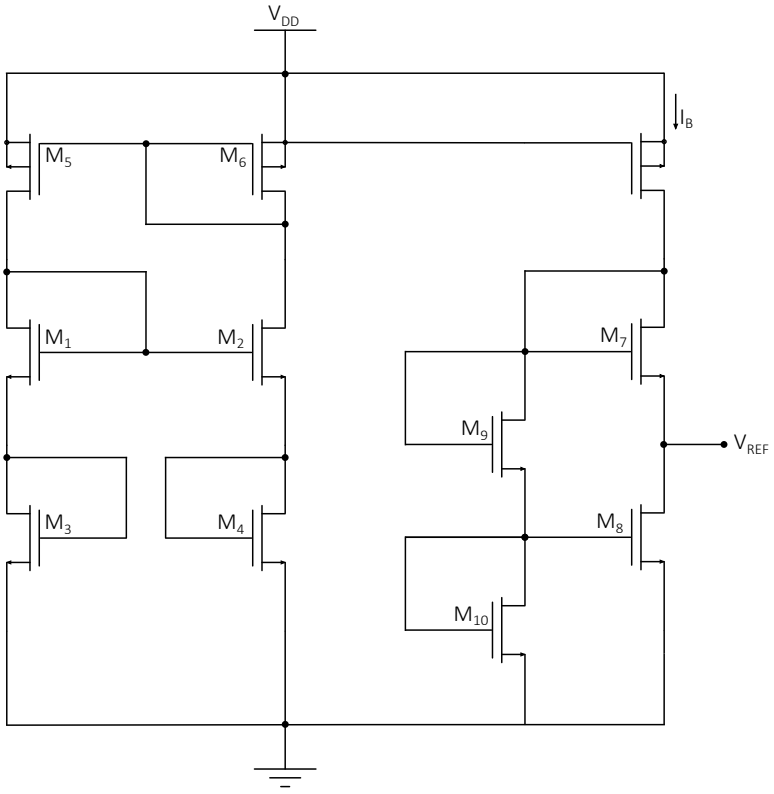


Figure 2.5: Vita voltage reference

Similarly to (2.17) and assuming that the majority of I_B flows through M_7 and M_8, the voltage reference can be written as:

$$V_{REF} = V_{TH} + \sqrt{2 \cdot I_B} \cdot \left[\left(1 + \sqrt{\frac{W_{10}/L_{10}}{W_9/L_9}} \right) \cdot \sqrt{\frac{1}{K_8}} - \sqrt{\frac{1}{K_7}} \right] \tag{2.18}$$

Analysing the equation (2.18) in temperature dependence scope, in the first term there is a negative dependence due to the threshold voltages, which forces the need of a positive dependence in the second term of the equation, simultaneously, there is a negative dependence due to the mobility parameter in K, which, again, forces the need of having a proportional compensation in that same second term of the equation. The solution is in the bias current: it has to be proportional to the temperature squared (T^2) in order to cancel the linear dependence of V_{TH}, and it has to be proportional to the mobility $(\mu(T))$ in order to cancel the dependence of K in the denominator [19].

Referring to figure 2.5, one can obtain:

$$V_{GS_1} + V_{GS_3} = V_{GS_2} + V_{GS_4} \tag{2.19}$$

The operation regime of M_1 and M_2 is in weak-inversion region, while M_3 and M_4 is in saturation region. The current equation for the saturation region is (2.16), and the current equation for the weak-inversion region is given by:

$$I_{sub-th} = K \cdot (\eta - 1) \cdot V_T^2 \cdot e^{\left(\frac{V_{GS} - V_{TH}}{\eta \cdot V_T}\right)} \tag{2.20}$$

where η is the subthreshold slope factor. Equating (2.20) and (2.16) at V_{GS}, respectively:

$$V_{GS_{1,2}} = V_{TH} + \eta \cdot V_T \cdot ln\left(\frac{I_B}{\mu \cdot C_{ox} \cdot (W/L) \cdot (\eta - 1) \cdot V_T^2}\right) \tag{2.21}$$

$$V_{GS_{3,4}} = V_{TH} + \sqrt{\frac{2 \cdot I_B}{\mu \cdot C_{ox} \cdot (W/L)}} \tag{2.22}$$

From (2.19), (2.21) and (2.22), equating at I_B, the parameters V_T^2 and K_4 are obtained, which match the idea previously explained:

$$I_B = \frac{\eta^2 \cdot V_T^2}{2} \cdot K_4 \cdot \left(\frac{N}{N-1}\right)^2 \cdot ln^2\left(\frac{(W/L)_2}{(W/L)_1}\right) \tag{2.23}$$

where $N = \sqrt{K_3/K_4}$.

This architecture achieved a output voltage of 891.1 mV and a power consumption of 165 nW using a minimum supply voltage of 1.5 V, in a total area of 0.015 mm^2. The TC reach the minimum value of 12 $ppm/^{\circ}$C in a temperature range from 0°C to 80°C and a LS of 0.46 $\%/V$.

A disadvantage of both these voltage references is that as the CMOS transistors have to operate in the saturation region, the minimum supply voltage is relatively high in order to prevent that the circuit starts operating in the triode region [20, 21], and, consequently, the power consumption is also high [2, 22].

Table 2.2 summarizes the performance characteristics of ΔV_{GS} voltage references.

2.3 Voltage Reference based on ZTC

The voltage reference based on ZTC, that stands for zero temperature coefficient, consists in developing a reference voltage operating in the strong-inversion region which output value is determined by biasing the transistor to a specific I_D that corresponds to a V_{GS} independent of temperature. Figure 2.6 illustrates the transconductance characteristic of a transistor using temperature as a parameter, i.e., the relation between the drain current and the gate-source voltage at different temperatures. The curves have a common interception point in which V_{GS} does not depend on

Table 2.2: Comparison of Voltage References based on ΔV_{GS}

	[17]	[19]	[18]
Tech (CMOS)	0.6 μm	0.35 μm	0.35 μm
V_{DDmin} (V)	1.4	1.5	1.5
Power (μW)	13.58	2.25	0.165
TC ($ppm/°C$)	36.9	25	12
Temp. range (°C)	[0,100]	[0,80]	[0,80]
LS ($\%/V$)	0.012	0.95	0.46
Area (mm^2)	0.055	0.08	0.015
PSRR (dB)			
@100Hz	-47	-65	-59
@10MHz	-20	-57	-52
V_{REF} (mV)	309	168	891.1

temperature, known as ZTC point, due to a mutual compensation of the mobility (μ) and threshold voltage (V_{TH}). This operating point varies according to the technology and geometry of the transistor.

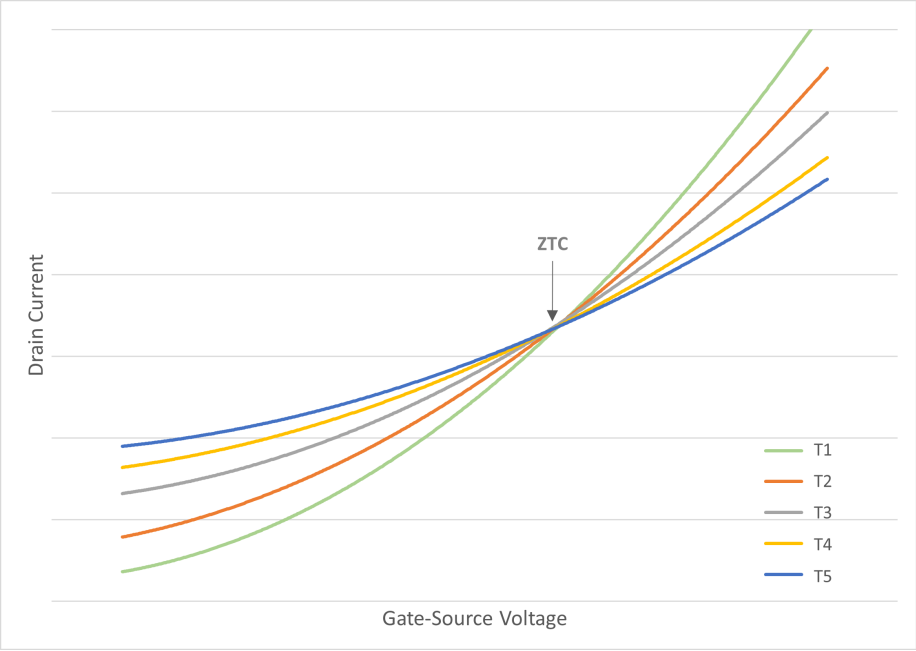


Figure 2.6: Transconductance characteristics of a transistor

There are two methods to implement this typology. Either the diode-connected MOSFET is biased exactly at the ZTC operating point, as implemented by Igor Filanovsky *et al.* [23], or the MOSFET can be biased in the proximity of the ZTC point using additionally a current generator, as implemented by Laleh Najafizadeh *et al.* [24]. When the transistor is biased outside the ZTC operating point, the gate-source voltage behaves as a CTAT or a PTAT. Thereby a current

generator that shows opposite temperature behaviour needs to be implemented in order to achieve temperature independence [25].

In 2001, Igor Filanovsky *et al.* implements the circuit shown in figure 2.7 using 0.35 μm CMOS technology, which is composed by an operational amplifier, three resistors and a NMOS operating in saturation.

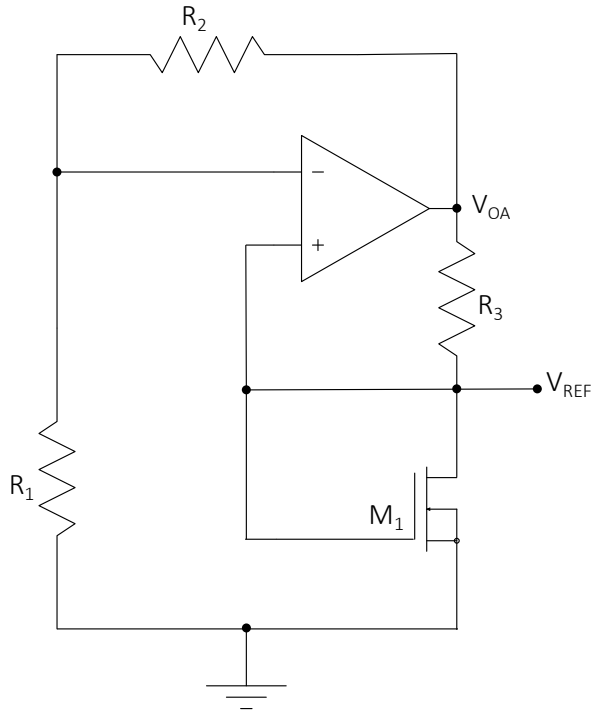


Figure 2.7: Filanovsky voltage reference

Keeping in mind that the input voltages of the OpAmp are equal to V_{REF}, which in turn is equal to V_{GS_1}, the output voltage of the OpAmp is given by:

$$V_{OA} = \left(1 + \frac{R_2}{R_1}\right) \cdot V_{REF} \tag{2.24}$$

Thus, the drain current equation of M_1 is given by:

$$I_{M1} = \frac{(1 + R_2/R_1) \cdot V_{REF} - V_{REF}}{R_3} = \frac{R_2}{R_1 \cdot R_3} \cdot V_{GS_1} \tag{2.25}$$

As explained above, the resistors need to be sized in order to achieve the I_{M1} and V_{GS_1} values that correspond to the ZTC point. In this circuit, with the experimental values of $I_{M1} = 230\ \mu V$ and $V_{GS_1} = 883\ mV$, the circuit achieves a voltage reference of 799 mV and a power consumption of 690 μV, using a minimum supply voltage of 3 V, in a total area of 0.02 mm^2. The TC reaches a value of 10 $ppm/°C$ in a temperature range from -20°C to 100°C.

In 2004, Laleh Najafizadeh *et al.* implements the circuit shown in figure 2.8 using 0.18 μm CMOS, which is composed by a PTAT current generator and a core circuit formed by four tran-

sistors and two resistors. The diode-connected NMOS M_7 and M_8 operate below the ZTC point, showing, therefore, a CTAT behaviour, which temperature dependence is nullified by the current generator.

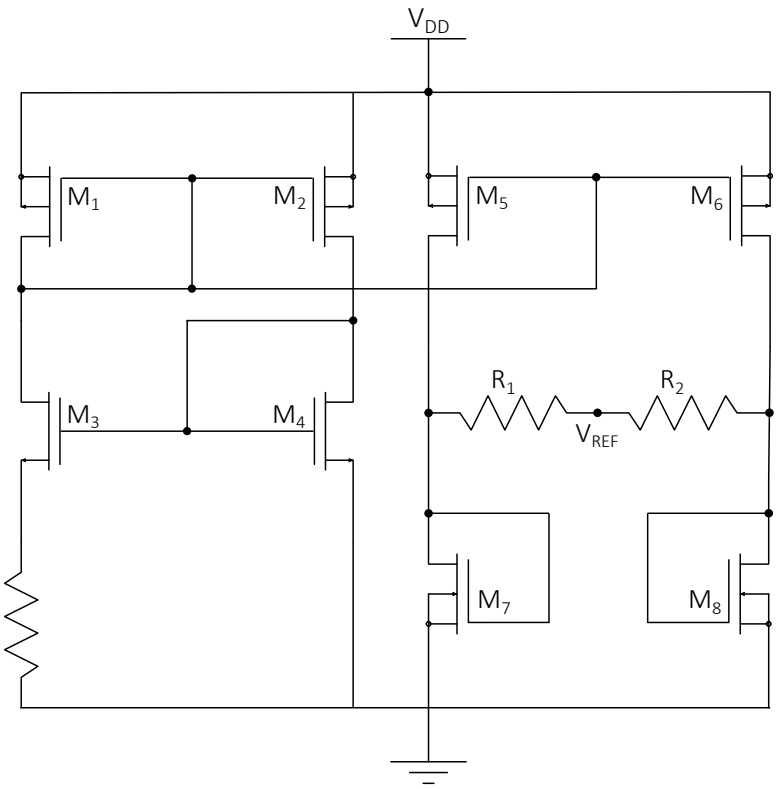


Figure 2.8: Najafizadeh voltage reference

The output voltage is given by:

$$V_{REF} = \frac{V_{GS_7}}{1+(R_1/R_2)} + \frac{V_{GS_8}}{1+(R_2/R_1)} \tag{2.26}$$

achieving a simulation value of 640 mV with a supply voltage of 1.8 V. However the reference voltage is able to operate with a voltage supply lower than 1 V. In comparison with the first presented ZTC method, the supply voltage achieved in this method is lower because the reference transistors are biased with CTAT behaviour [25]. The record TC value achieved is 4 $ppm/°$C in a temperature range from -50°C to 150°C. Note that this values result from simulation once the circuit was not fabricated.

This typology is the one that presents better values of temperature coefficient (TC) due to the efficient method of cancelling the temperature dependencies of both the threshold voltage and mobility, even though there is still residue resulting from the non-linear temperature dependencies [24]. However, it implies the usage of a certain supply current correspondent to the ZTC point (or in the vicinity), and the value of that current is relatively high compared to other typologies, which affects the power consumption of the voltage reference.

Table 2.3 summarizes the performance characteristics of ZTC voltage references.

Table 2.3: Comparison of Voltage References based on ZTC

	[23]	[24]	[25]
Tech (CMOS)	0.35 μm	0.188 μm	0.13 μm
V_{DDmin} (V)	3	<1	0.45
Power (μW)	690	-	1.3
TC ($ppm/°C$)	10	4	154
Temp. range (°C)	[-20,100]	[-50,150]	[-40,85]
LS ($\%/V$)	-	-	1.8
Area (mm^2)	0.0204	-	0.017
PSRR (dB)			
@100Hz	-	-	-41
@10MHz	-	-	-
V_{REF} (mV)	799	640	318

2.4 Voltage Reference based on V_{TH}

The voltage reference based on V_{TH} typology had one of the first implementations in 1978 by Robert Blauschild *et al.* and the initial concept consists in developing a reference voltage that operates in the strong-inversion region and which temperature independence is achieved by subtracting the gate-source voltages (V_{GS}) of two different types of MOSFET: enhancement-mode and depletion-mode. figure 2.9 demonstrates the transconductance characteristic at different temperatures for enhancement and depletion-mode of NMOS and PMOS transistors. As shown, the temperature dependencies either of enhancement-mode NMOS with enhancement-mode PMOS or depletion-mode NMOS with depletion-mode PMOS are complementary. This way, there are several combinations of transistors which are able to provide a temperature cancellation, such as, a reference voltage resulting of the V_{GS} subtraction of two different-type NMOS or two different-type PMOS, the latest as implemented by Blauschild *et al.* [26], or a reference voltage resulting of the V_{GS} summation of a NMOS with a PMOS of different types, first implemented in 2001 by Mamoru Ugajin *et al.* [27].

In the figure 2.10a is illustrated the conventional voltage reference proposed by Blauschild *et al.* which is composed by three depletion-mode PMOS, one enhancement-mode PMOS and a operational amplifier. The choice of using PMOS transistor is because using NMOS requires 3-transistor stacking, which is an inconvenient.

In the figure 2.10b is illustrated the voltage reference proposed by Ugajin *et al.*, implemented in fully depleted CMOS/SOI and composed by three depletion-mode PMOS, one of them undoped, one enhancement-mode NMOS and a operational amplifier. The usage of the operational amplifier in a negative feedback configuration enables that the output voltage is independent of the supply voltage once the I_D of M_3 and M_4 are equal. An undoped depletion-mode PMOS transistor (M_4) is used as one of the reference transistors given that its threshold voltage is smaller than doped transistors.

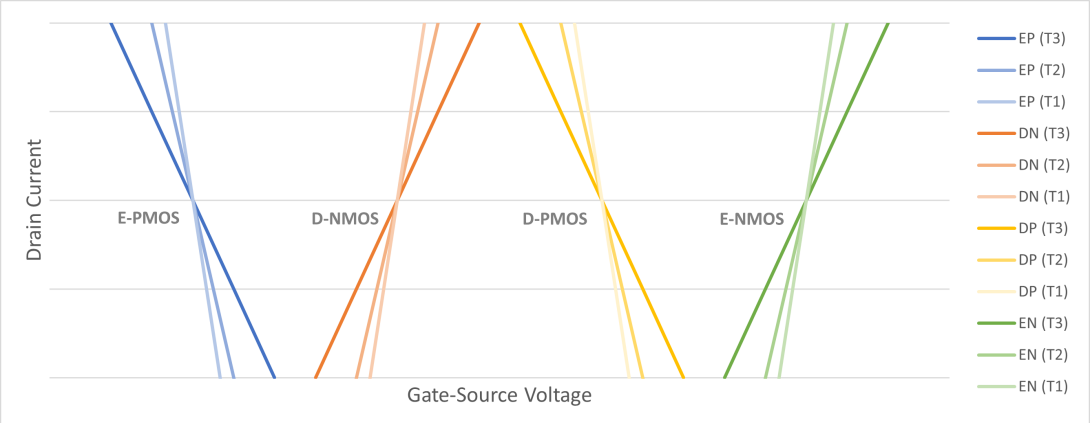
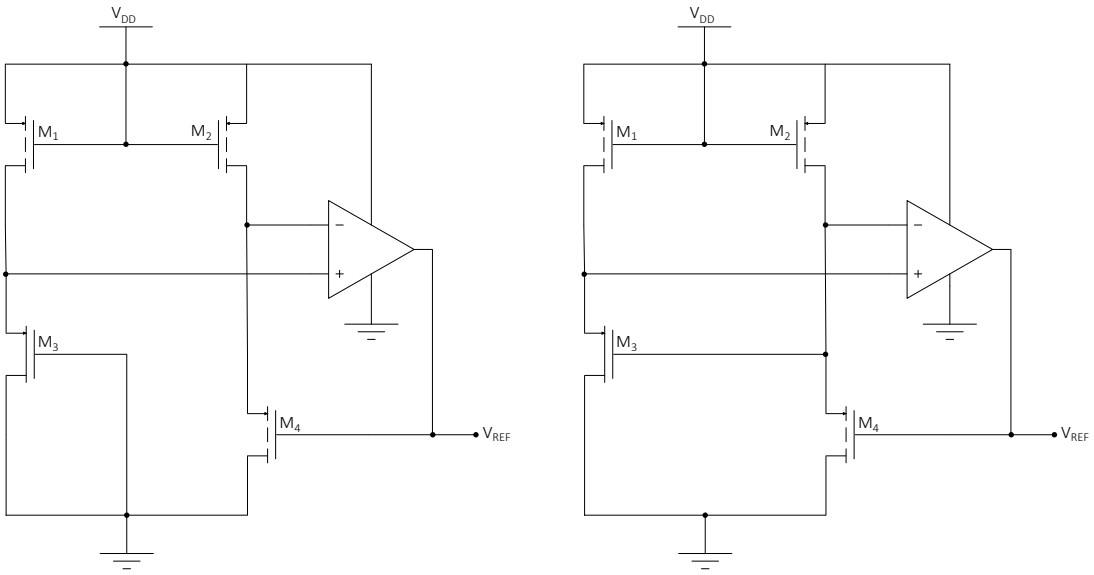


Figure 2.9: Transconductance characteristics of enhancement-mode (E) and depletion-mode (D) NMOS and PMOS transistors



(a) Blauschild voltage reference (b) Ugajin voltage reference

Figure 2.10: Blauschild and Ugajin voltage references

The equation of the drain current in the saturation region is given by (2.16). The reference voltage equation of Blauschild (V_{REF_a}) and Ugajin (V_{REF_b}) can be simply written, respectively, as:

$$V_{REF_a} = V_{GS_{DP}} - V_{GS_{EP}}, \tag{2.27}$$

$$V_{REF_b} = V_{GS_{DP}} + V_{GS_{EN}}, \tag{2.28}$$

where the indicators DP, EP and EN stand for depletion-mode PMOS, enhancement-mode PMOS and enhancement-mode NMOS, respectively. Thus, from (2.16), (2.27) and (2.28):

$$V_{REF_a} = V_{TH_{DP}} - V_{TH_{EP}} + \sqrt{\frac{2 \cdot I_D}{K_{DP}}} - \sqrt{\frac{2 \cdot I_D}{K_{EP}}} \tag{2.29}$$

$$V_{REF_b} = V_{TH_{EN}} + V_{TH_{DP}} + \sqrt{\frac{2 \cdot I_D}{K_{EN}}} - \sqrt{\frac{2 \cdot I_D}{K_{DP}}} \tag{2.30}$$

In order to nullify the mobility parameter (μ) and make the output independent of the supply voltage, the size ratio of the reference transistors are modified so that the transconductance (K) of the transistors are equal and cancel each other. The output voltages of both circuits can then be rewritten merely as the difference or the sum of multi-threshold voltages:

$$V_{REF_a} = V_{TH_{DP}} - V_{TH_{EP}} \tag{2.31}$$

$$V_{REF_b} = V_{TH_{EN}} + V_{TH_{DP}} \tag{2.32}$$

In relation to Ugajin *et al.* circuit, the reference voltage achieve a value of 530 mV, being able to operate with a minimum supply voltage of 0.6 V. The power consumption of the circuit is 100 μV, using a supply voltage of 1 V, and the total area is 0.06 mm^2.

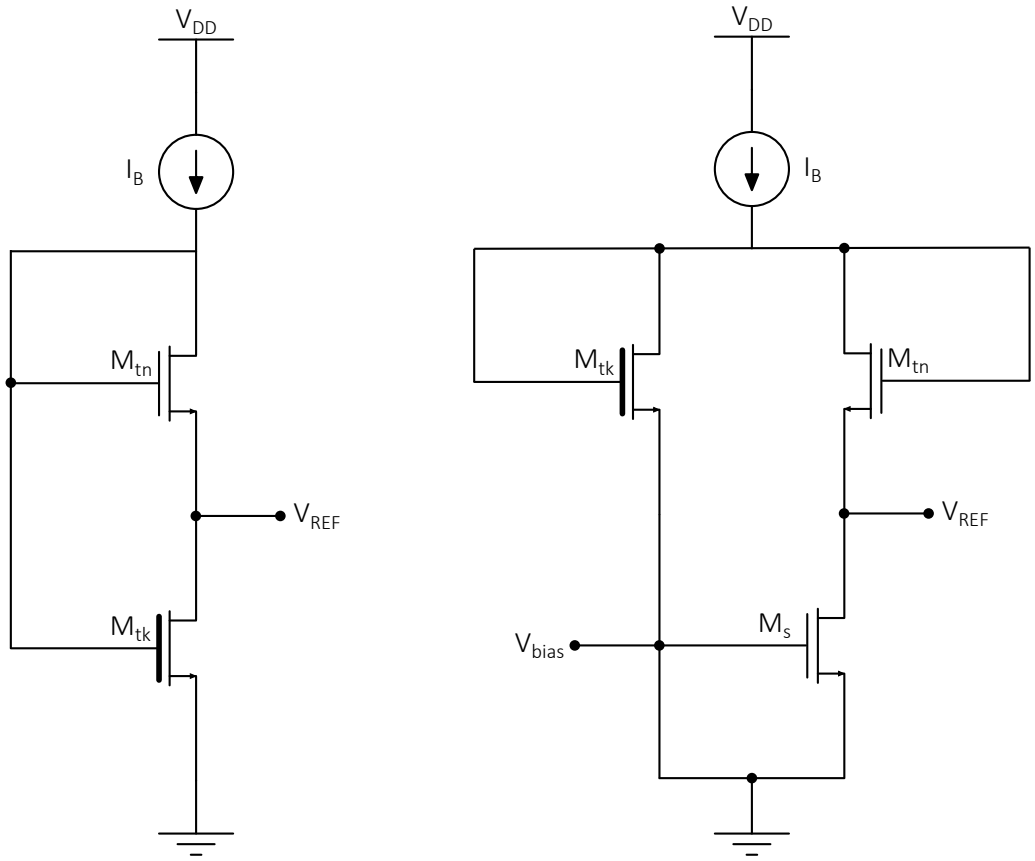
This more recent architecture benefits from the conventional one in some factors. One of the most significant changes is that the output voltage is no longer directly connected to the input offset of the feedback operational amplifier, turning the output voltage independent of this unstable voltage. In addition, the temperature insensitive is higher due to a smaller temperature coefficient and a smaller mobility temperature coefficient ratio. However, there are some drawbacks also, for instance, the usage of non-standard devices, like depletion-mode MOSFET, due to their rare availability or need of additional fabrication steps [28, 29], and the use of an operational amplifier which limits the values of area, power consumption and minimum supply voltage [1]. Moreover, the circuit requires a trimming technique in order to control the dispersion of the output voltage with process [27].

More recently, in 2009, W. Yan *et al.* [30] proposed a voltage reference with a similar principle of the one presented above: reaching temperature independence by gate-source voltages subtraction, however, in this case, the NMOS transistors have different gate oxide thickness (thick gate oxide and thin gate oxide) and operate in the weak-inversion region. In the figure 2.11 there are two equivalent versions of the architecture, implemented in 0.35 μm CMOS and composed mainly by two reference transistors, a thin gate oxide NMOS and a thick gate oxide NMOS, differing only in the circuit structure: in version (a) the transistors are stacked whereas in version (b) the transistors are connected in folded form.

The equation of the drain current in weak-inversion region is given by (2.20). Equating the equation at V_{GS}:

$$V_{GS} = V_{TH} + \eta \cdot V_T \cdot ln\left(\frac{I_D}{K \cdot (\eta - 1) \cdot V_T^2}\right), \tag{2.33}$$

Regarding the drain current passing through the reference transistors, it is clear that in version (a) the current is the same and in version (b) it is possible to set equal currents by matching the bias current for that purpose. Thereby, assuming that $I_{TK} = I_{TN}$, the output voltage equation of both



(a) Stacked form version (b) Folded form version

Figure 2.11: Yan voltage references

versions can be written as

$$V_{REF} = V_{GS_{TK}} - V_{GS_{TN}} = V_{TH_{TK}} - V_{TH_{TN}} + \eta \cdot V_T \cdot ln\left(\frac{K_{TN}}{K_{TK}}\right). \tag{2.34}$$

where the indicators TK and TN stand for thick gate oxide and thin gate oxide.

Using a minimum supply voltage of 1.1 V, the reference voltage values obtained are 96.6 mV and 108.9 mV and the power consumption of the circuits are 22 nW and 25.3 nW, for version (a) and (b) respectively, in a total area of approximately 0.019 mm^2 for both circuits. This architecture has the advantage of operating in the weak-inversion region which generates lower power consumption relating to operations in the strong-inversion region. The main performance difference between the two versions are the values of the temperature coefficient, which are 11.4 $ppm/°C$ and 9.2 $ppm/°C$ in a temperature range from -20°C to 80°C, and the values of the line sensitivity, being 0.09 $\%/V$ and 0.17 $\%/V$ for version (a) and version (b) respectively.

Table 2.4 summarizes the performance characteristics of V_{TH} voltage references.

Table 2.4: Comparison of Voltage References based on V_{TH}

	[27]	[30]	[30]
Tech (CMOS)	N/A	0.35 μm	0.35 μm
V_{DDmin} (V)	0.6	1.1	1.1
Power (μW)	100	0.022	0.0253
TC ($ppm/°C$)	-	11.4	9.2
Temp. range (°C)	[-25,100]	[-20,80]	[-20,80]
LS ($\%/V$)	-	0.09	0.17
Area (mm^2)	0.06	0.0189	0.0193
PSRR (dB)			
@100Hz	-	-60	-60
@10MHz	-	-40	-40
V_{REF} (mV)	530	96.6	108.9

2.5 Ultra-Low Power Voltage Reference

In this section two similar architectures based on ΔV_{TH} typology are presented. These voltage references operate in weak-inversion and achieve power consumption values down to the picowatt order of magnitude, being named after that as ultra-low power, using, as well, low supply voltage. Additionally, the performance of the circuits, such as TC, LS, PSRR and area values are comparable to other voltage references.

In the figure 2.12a is illustrated the voltage reference proposed by Mingoo Seok *et al.* [1] in 2012, implemented in 0.13 μm CMOS technology. The circuit is composed simply by two NMOS transistors of different threshold voltages, an I/O transistor and a native transistor, both of thick gate oxide.

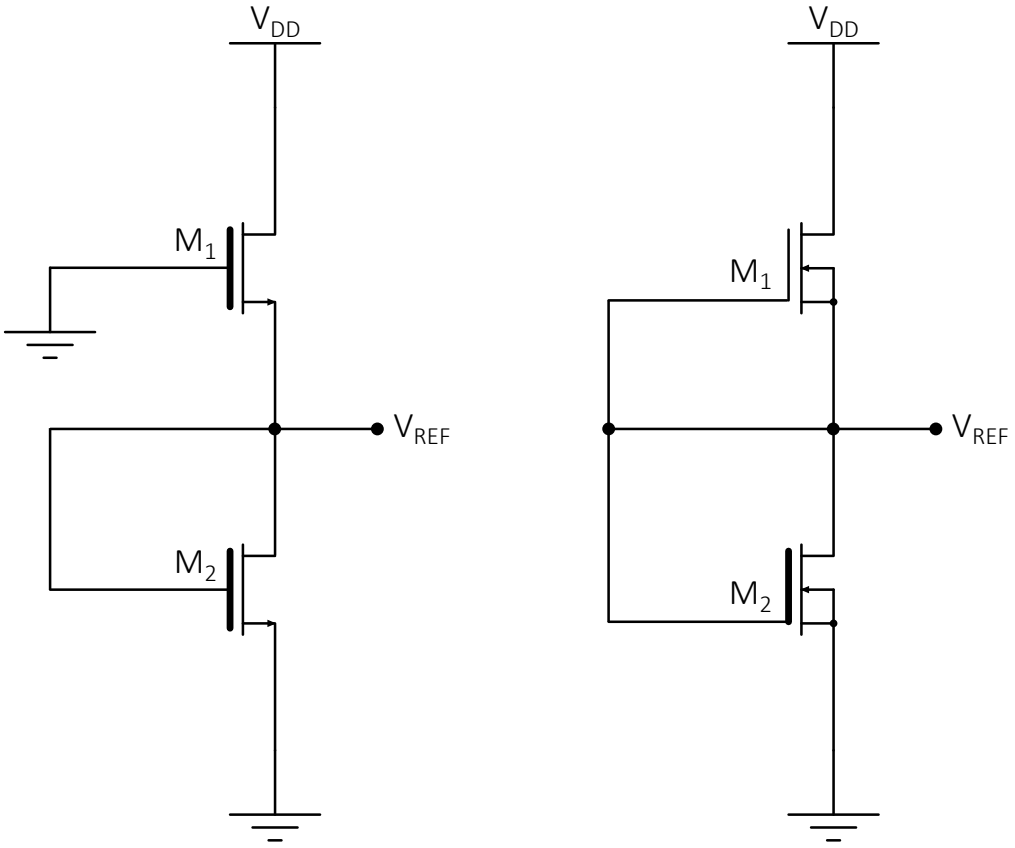
In the figure 2.12b is illustrated the voltage reference proposed by Domenico Albano *et al.* [5] in 2013, implemented in 0.18 μm CMOS technology. The circuit is also composed by only two NMOS transistors, however, in this case, one is a high-threshold voltage transistor and the other is a low-threshold voltage transistor, with threshold voltages of 600 mV and 320 mV respectively.

The equation of the drain current in weak-inversion region is given by (2.20). From analysing the circuit schematics, the difference between both configurations is in the body and gate connections of M_1. The current flowing through M_1 and M_2 is equal, therefore, the output voltage equation of Seok (V_{REF_a}) and Albano (V_{REF_b}) circuit can be written, respectively, as:

$$V_{REF_a} = \frac{\eta_1 \cdot \eta_2}{\eta_1 + \eta_2} \cdot (V_{TH_2} - V_{TH_1}) + \frac{\eta_1 \cdot \eta_2}{\eta_1 + \eta_2} \cdot V_T \cdot ln\left(\frac{\mu_1 \cdot C_{OX_1} \cdot (W_1/L_1)}{\mu_2 \cdot C_{OX_2} \cdot (W_2/L_2)}\right) \tag{2.35}$$

$$V_{REF_b} = V_{TH_2} - \frac{\eta_2}{\eta_1} \cdot V_{TH_1} + \eta_2 \cdot V_T \cdot ln\left(\frac{\mu_1 \cdot C_{OX_1} \cdot (W_1/L_1)}{\mu_2 \cdot C_{OX_2} \cdot (W_2/L_2)}\right) \tag{2.36}$$

The equations are constituted by a part that has a complementary temperature dependence due to V_{TH}, and another one that has a proportional temperature dependence on account of V_T. This last



(a) Seok voltage reference (b) Albano voltage reference

Figure 2.12: Ultra-low power voltage references

temperature dependence can be cancelled by properly sizing the transistors. Also, by considering that $\eta_1 = \eta_2$ and, in (2.37) $\eta = 1.5$, the output voltages equations are simplified:

$$V_{REF_a} = \frac{\eta^2}{2 \cdot \eta} \cdot (V_{TH_2} - V_{TH_1}) = 0.75 \cdot \Delta V_{TH} \tag{2.37}$$

$$V_{REF_b} = V_{TH_2} - V_{TH_1} = \Delta V_{TH} \tag{2.38}$$

The Seok *et al.* architecture achieves a reference voltage of 175 mV and a record power consumption of 2.22 pW using a minimum supply voltage of 0.5 V, in a total area of 1350 μm^2. Regarding the performance parameters, the circuit obtained a minimum TC value of 16.9 $ppm/^{\circ}$C, in a temperature range from -20°C to 80°C, and a LS of 0.033 $\%/V$.

In relation to Albano *et al.* circuit, the reference voltage achieve a value of 275.4 mV and a power consumption of 40 pW using a minimum supply voltage of 0.45 V, which is the lowest supply voltage reported, in a total area of 0.018 mm^2. The circuit obtained an average TC value of 105.4 $ppm/^{\circ}$C, in a temperature range from 0°C to 120°C, and an average LS of 0.46 $\%/V$.

Both architectures above-mentioned in this section present a major advantage in contrast with other voltage references, which is not using amplifiers, saturated devices, resistors, current generators and start-up circuits. By doing so, the values of power consumption, supply voltage and area

meet the required values for low-voltage and ultra-low power consumption. Moreover, the performance of the circuits, in particular the line-sensitivity and power supply rejection ratio values, are not affected by not using amplifiers because the output voltage is totally independent of the supply voltage. Additionally, since the power consumption is ultra-low, there is no need to implement duty-cycling techniques for economising energy. Lastly, due to the simplicity of the architectures, these can be easily used as intellectual property blocks [1].

Table 2.5 summarizes the performance characteristics these two ultra-low power voltage references.

Table 2.5: Comparison of Ultra-Low Power Voltage References

	[1]	[5]
Tech (CMOS)	0.13 μm	0.18 μm
V_{DDmin} (V)	0.5	0.45
Power (μW)	2.22 pW	40 pW
TC ($ppm/°C$)	62	105.4
Temp. range (°C)	[-20,80]	[0,120]
LS ($\%/V$)	0.033	0.46
Area (mm^2)	0.00135	0.018
PSRR (dB)		
@100Hz	-53	-48
@10MHz	-62	-29.2
V_{REF} (mV)	174.9	275.4

2.6 Problem Statement

In table 2.6 is compiled a detailed summary of the performance of some state-of-the-art voltage references, ordered by typology.

Table 2.6: Comparison table of Voltage References

Voltage Reference	Typology	Tech CMOS	V_{DDmin} (V)	Power (μW)	TC ($ppm/°C$)	Temperature range (°C)	LS ($\%/V$)	Area (mm^2)	V_{REF} (mV)
Banba [9]	Bandgap	0.4 μm	0.84	1.848	116	[27, 125]	0.1	0.1	518
Annema [12]	Bandgap	0.35 μm	0.85	1.02	57	[-20, 100]	-	0.063	650
Malcovati [13]	Bandgap	0.8 μm	1	92	19	[0, 80]	-	0.25	536
Leung [14]	Bandgap	0.6 μm	0.98	17.64	15	[0, 100]	0.73	0.24	603
Doyle [15]	Bandgap	0.5 μm	0.95	9.5	17	[-40, 125]	-	1.0904	628
Annema [16]	Bandgap	0.16 μm	1.1	1.54	30	[-45, 135]	-	0.0025	944
Osaki [10]	Bandgap	0.18 μm	0.7	0.0525	114	[-40, 120]	-	0.0246	548
Leung [17]	ΔV_{GS}	0.6 μm	1.4	13.58	36.9	[0, 100]	0.012	0.055	309
Vita [19]	ΔV_{GS}	0.35 μm	1.5	2.25	25	[0, 80]	0.95	0.08	168
Vita [18]	ΔV_{GS}	0.35 μm	1.5	0.165	12	[0, 80]	0.46	0.015	891.1
Filanovsky [23]	ZTC	0.35 μm	3	690	10	[-20, 100]	-	0.0204	799
Najafizadeh [24]	ZTC	0.18 μm	<1	-	4	[-50, 150]	-	-	640
Wenger [25]	ZTC	0.13 μm	0.45	1.3	154	[-40, 85]	1.8	0.017	318
Ugajin [27]	V_{TH}	N/A	0.6	100	-	[-25, 100]	-	0.06	530
Yan [30]	V_{TH}	0.35 μm	1.1	0.022	11.4	[-20, 80]	0.09	0.0189	96.6
Yan [30]	V_{TH}	0.35 μm	1.1	0.0253	9.2	[-20, 80]	0.17	0.0193	108.9
Seok [1]	Ultra-Low	0.13 μm	0.5	2.22 pW	62	[-20, 80]	0.033	0.00135	174.9
Albano [5]	Ultra-Low	0.18 μm	0.45	40 pW	105.4	[0, 120]	0.46	0.018	275.4
Giustolisi [31]	Alternative	1.2 μm	1.2	4.23	119	[-25, 125]	-	0.23	300
Huang [32]	Alternative	0.18 μm	0.85	3.3	194	[-20, 120]	0.905	0.0238	221
Vita [20]	Alternative	0.35 μm	0.9	0.036	10	[0, 80]	0.27	0.045	670
Kinget [33]	Alternative	0.09 μm	0.5	482	150	[5, 100]	20.7	0.07 μm^2	241
Ueno [2]	Alternative	0.35 μm	1.4	0.3	15	[-20, 80]	0.002	0.055	745
Magnelli [34]	Alternative	0.18 μm	0.45	0.00315	142	[0, 125]	0.44	0.043	263.5
Ivanov [35]	Alternative	0.13 μm	0.75	0.17	40	[-20,85]	0.005	0.07	256
Zhu [36]	Alternative	0.18 μm	0.45	0.0156	59.4	[-40, 85]	0.033	0.0132	118.41

All in all, each typology as their own strengths and drawbacks.

For bandgap voltage references, even though the typology presents great values for PVT insensitivity, the supply voltage, power consumption and area are affected due to the use of amplifiers and resistors. Also, the typology concept implies using a bipolar junction transistor or a diode, which makes the design more complex.

Regarding the ΔV_{GS} typology, it was possible to achieve a complete suppression of the temperature dependence of mobility and second-order channel length modulation and body effect, using standard CMOS technology, which results in good values of temperature coefficient. On the other hand, the operation regime is in saturation region which affects dramatically the supply voltage and consequently the power consumption values.

The ZTC typology concept has as main purpose achieving the lowest values of temperature coefficient, being able to obtain measures extremely near to zero. Although, that involves using the ZTC current whose values are relatively high, affecting, hence, the power consumption.

Concerning the V_{TH} typology, the main disadvantage is the usage of non-standard devices, because of their low availability and need of additional fabrication steps. However, that can be compensated once it was possible to design circuits without amplifiers, resistors, current generators and start-up circuits, and, in addition, the circuits operate in the weak-inversion region. Thereby, the voltage references are low-voltage, ultra-low power and have small area. Another inconvenient is that this architectures require trimming techniques due to the process instability.

For the purpose of this dissertation, the voltage reference has to meet the following demands: a low supply voltage, i.e. sub-1V, a small area, a stable output voltage against process, temperature and voltage variations and, the crucial factor is having the lowest power consumption possible.

2.7 Proposed Solution

After doing an analysis and comparison between the various voltage references in literature, the ones presented in Section 2.5 are the most suitable for the required parameters. Therefore, the proposed solution is based on the design of [1], which is implemented in CMOS, using only two transistors in the weak-inversion region, powered by a supply voltage of 0.5 V, all in the lower area reported. Also, the design does not include amplifiers, saturated devices, resistors, current generators nor start-up circuits. However, this architecture has more sensibility to process variations than others in literature, due to the usage of leakage currents to obtain the reference voltage. Thus, there is a need of developing a trimming circuit to improve the PVT values, maintaining the performance already achieved. The idea is to create a digital trimming circuit with a flow concept, so that it can be easily used when changing technology.

Chapter 3

Proposed Voltage Reference

Based on the voltages references presented in Section 2.5, it was developed and studied several circuit alternatives, using UMC 0.18 μm technology, which are presented in figure 3.1. The circuits 3.1a, 3.1b are composed by one NMOS and one PMOS, while 3.1c, 3.1d are composed by two NMOS. The circuits 3.1e, 3.1f, 3.1g, 3.1h are respectively identical to the previous ones however composed by two stages. According to [1], any combination of two devices with a considerable V_{TH} difference is suitable to be used in this voltage reference typology, and so, in all circuit versions, two different device are used: the transistors $M_{1,3}$ are native devices, also known as ZVT, and $M_{2,4}$ are standard devices. Besides, for each circuit it was also studied different possibilities of devices types: either all thick-gate oxide MOSFETs, or thick-gate oxide for $M_{1,3}$ along with thin-gate oxide for $M_{2,4}$. Keep in mind that in this technology the bulk of NMOS devices has to be connected to the lowest voltage level, which limited the number of circuit alternatives to be studied.

For circuit analysis it was used the Cadence Virtuoso Analog Design Environment, in this phase specifically the ADE Assembler, in which it was created a testbench with several performance tests. For each circuit and respective two device type possibilities, it was tested their line sensitivity, temperature coefficient, power supply rejection ratio, noise and power consumption, in which the values to be achieve were: LS $< 0.4\ \%/V$, TC = [-100, 100] $ppm/^{\circ}$C, $P_{cons} < 16.5\ nW$, and also, a minimum supply voltage of $V_{DD_{min}} < 0.65\ V$. Regarding the sizes of the transistors, it was initial set a length for all transistors to the highest available for this technology, i.e., $L_{1-4} = 50\ \mu m$, once, while working in weak-inversion and with leakage currents, the resistance of the transistor is more constant for higher length values, therefore a better insensitivity to supply voltage and a lower power consumption can be achieved. The width was set to several values in a range between the minimum and the maximum of the technology, i.e., $W_{1-4} = [min : step : max]$.

From the performance results of the first iteration of simulations of all the different circuits, 3.1a, 3.1b, 3.1c, 3.1d were excluded because they fail the established specifications for LS and/ or TC. Thereby, there was a motivation to develop the 2-stage circuit configuration, even though it means an increase of the minimum supply voltage.

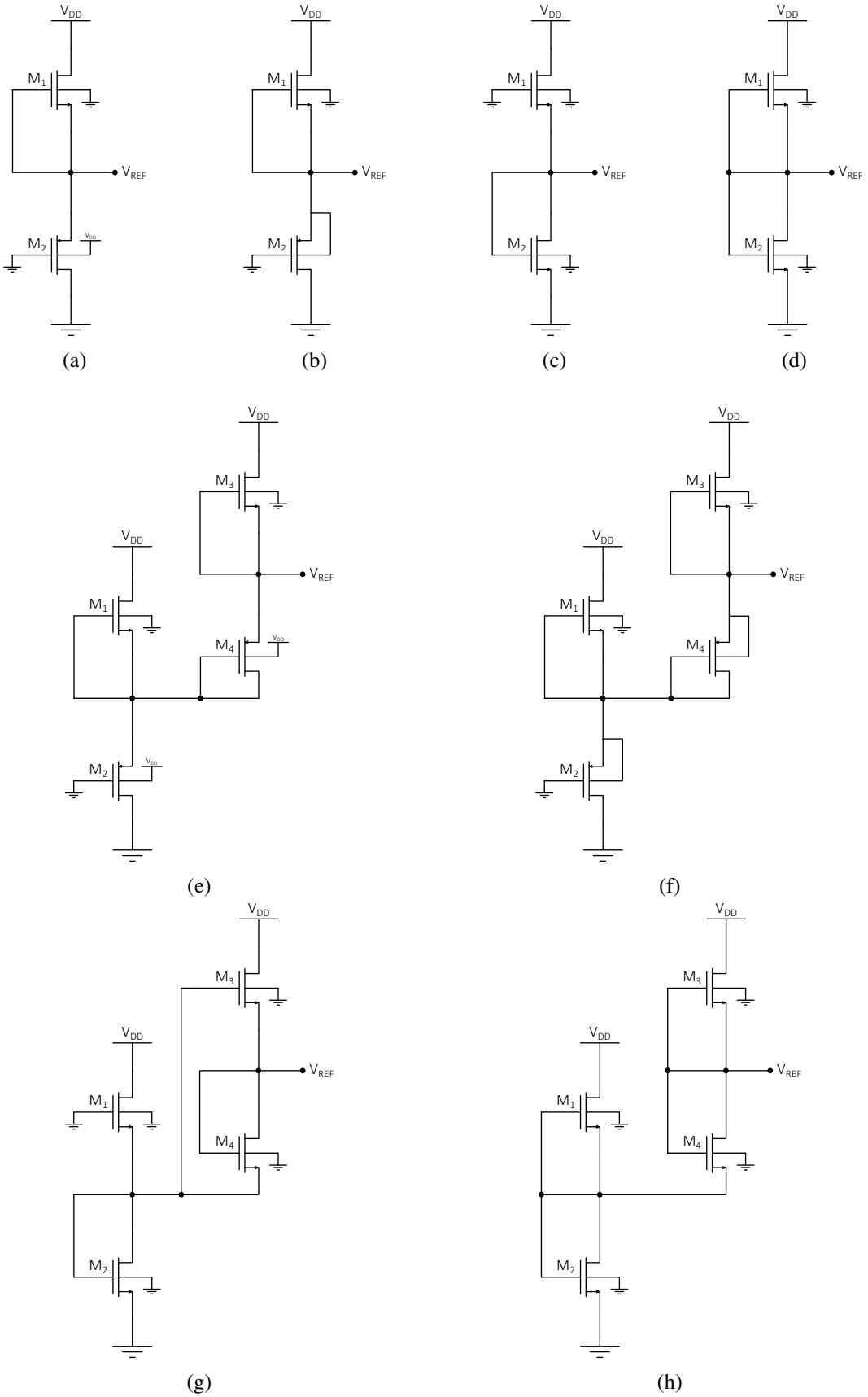


Figure 3.1: Several Voltage References

Analysing the performance results for the 2-stage circuits, 3.1g and 3.1h using both thick-gate and thin-gate oxide devices, were the only ones which qualify all the required specifications. However, the circuit 3.1h, also illustrated with more detail in figure 3.2, is the chosen circuit for this work due to a better performance in the corner analysis, specifically for the TC parameter, which will be presented further in this chapter. Note that the 2-stage circuits which fail the specifications, 3.1e and 3.1f, failed either due to the same reasons of the equivalent 1-stage circuit, or because it was not reached a balance between the improved LS and TC values, and the worsen minimum supply voltage values.

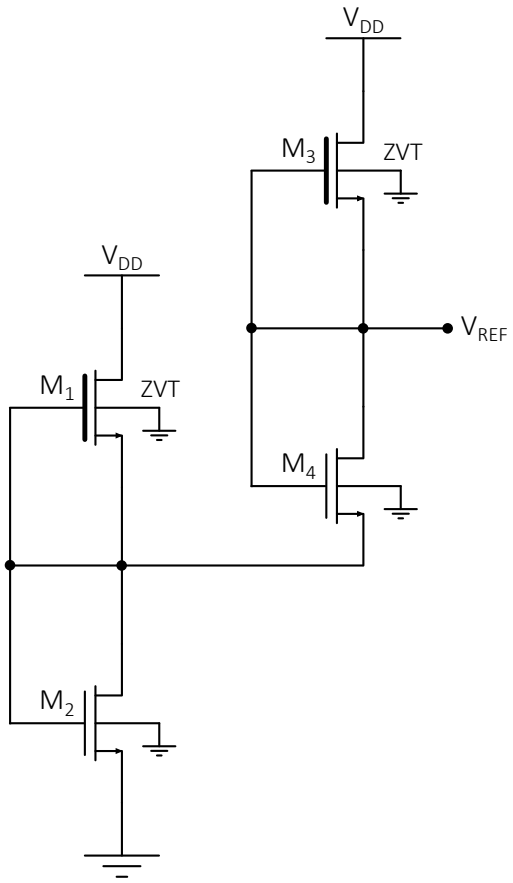


Figure 3.2: Proposed Voltage Reference

Out of this set of results it was possible to make some conclusions:

- The performance of a voltage reference is technology dependent.
- The minimum and maximum values of V_{DD} and V_{REF} are lower for the configuration using both thick-gate oxide and thin gate oxide MOSFETs, compared with the configuration using all thick-gate oxide MOSFETs. This is because the threshold voltage of thin-gate oxide transistors is lower.
- The minimum and maximum values of V_{DD} and V_{REF} are higher for the 2-stage circuit architecture compared with the 1-stage circuit architecture.

However the output reference voltage of the 2-stage design is higher, it is not necessarily a disadvantage because it prevents the circuit in which the voltage reference is used to be forced to work also in the subthreshold region. In the case that it is required for the external circuit to work in the subthreshold region, the 2-stage configuration offers the possibility to connect the output reference voltage to the source of M_1, in which the output value is lower.

Regarding to the sizing of the circuit of figure 3.2, the following methodology, which is graphically presented in figure 3.3, was followed, using the support of the optimiser of Cadence Virtuoso tool:

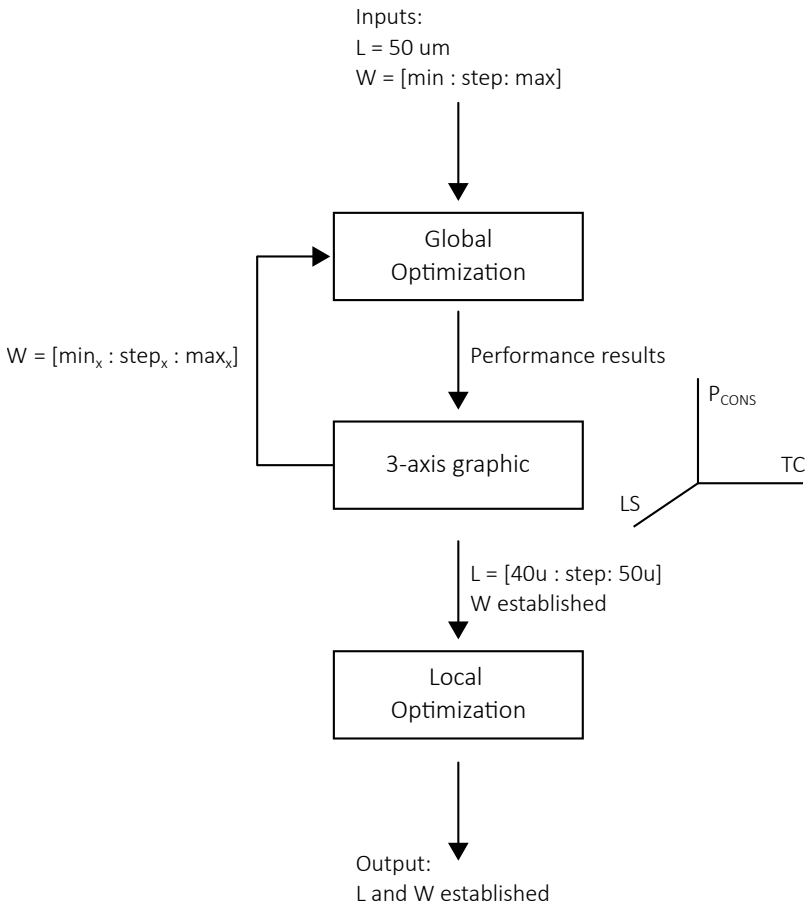


Figure 3.3: Sizing methodology

1. Run a Global Optimization setting a fixed length, e.g. $L = 50\ \mu m$, and a width range such as $W = [min : step : max]$, for all transistors.

   (a) Create a 3-axis graphic, in which each axis represents LS, $|TC|$ and P_{cons}, and plot the results of every design point.

   (b) Measure the distance of each design point to the center $(0,0,0)$ and filter the ones with a smaller distance. The design points with lower distance to the center are the ones with a better balanced performance.

(c) Replace the minimum and maximum values of the width range by values around the bests design points of the last iteration results, and reduce the range step, i.e. $W = [min_x : step_x : max_x]$

(d) Repeat the procedure 1. until an optimum width value is achieved.

2. Run a Local Optimization with the width previously established, and a length range such as $L = [40\mu m : step : 50\mu m]$. This adjustment can improve the TC values without compromising the need of a high length for low power consumption.

The chosen values for the transistor sizes are described in table 3.1.

Table 3.1: Parameter values of the Proposed Voltage Reference

	M_1	M_2	M_3	M_4
W (μm)	0.8	1.2	11.2	0.24
L (μm)	50	49	49.5	49.5

The IC fabrication process is non-optimal and so all the components in a wafer will suffer from parameters variations, creating transistors with different doping, which affect their resistance, threshold voltage, capacitance, among other factors. This causes operational differences between the designed circuit and the post-fabrication circuit. The transistors are categorized as fast, slow or typical, and there is five combinations of these states which are the process corners, namely TT (typical-typical), SS (slow-slow), FF (fast-fast), SF (slow-fast) and FS (fast-slow), in which the first character relates to the fabrication process of the NMOS and the second character to the PMOS. Thereby a corner analysis was done. The figures 3.4, 3.5, 3.6 and 3.7 show the results of the corner analysis for LS, TC, PSRR and Noise, respectively, and in the table 3.2 is summarise the outcomes of each performance test for each process corner.

A Monte Carlo analysis was not possible to do because there is no model files for ZVT devices.

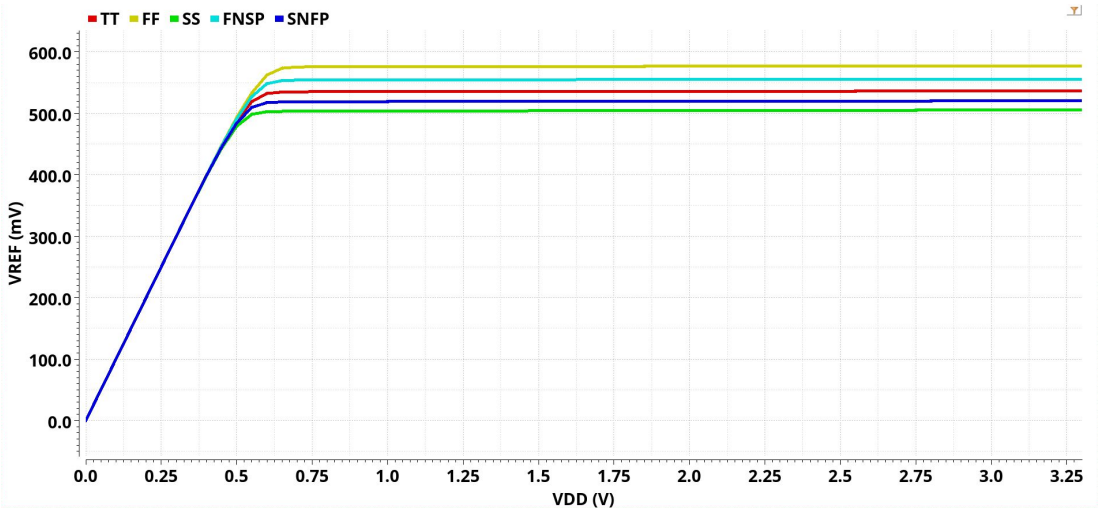


Figure 3.4: LS analysis for different process corners - Voltage Reference

As seen from these results, the circuit has a worst performance when using faster NMOS devices, in other words, for FF and FNSP corners, however the deviations are minimal. For TT process corner, the voltage reference achieves an output voltage of 536 mV, powered by a minimum supply voltage of 0.6 V and consuming 3.26 nW. Regarding the performance parameters, the circuit obtains a LS of 0.28 $\%/V$ and a TC of 17 $ppm/°C$, in a temperature range from 0°C to 80°C. In an overall performance point of view, the proposed voltage reference is a very stable circuit, nearly insensible to temperature and voltage variations, which makes it notably reliable.

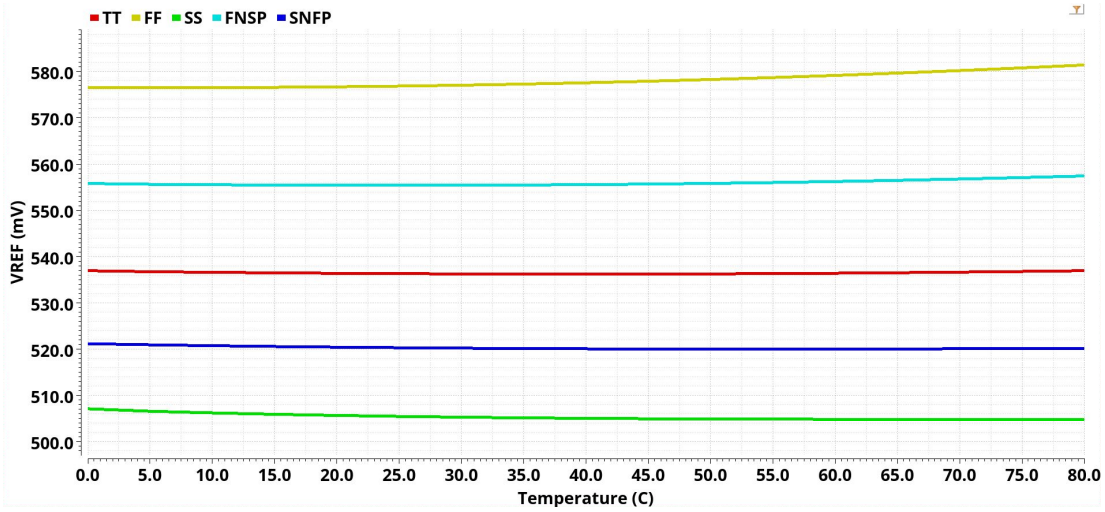


Figure 3.5: TC analysis for different process corners - Voltage Reference

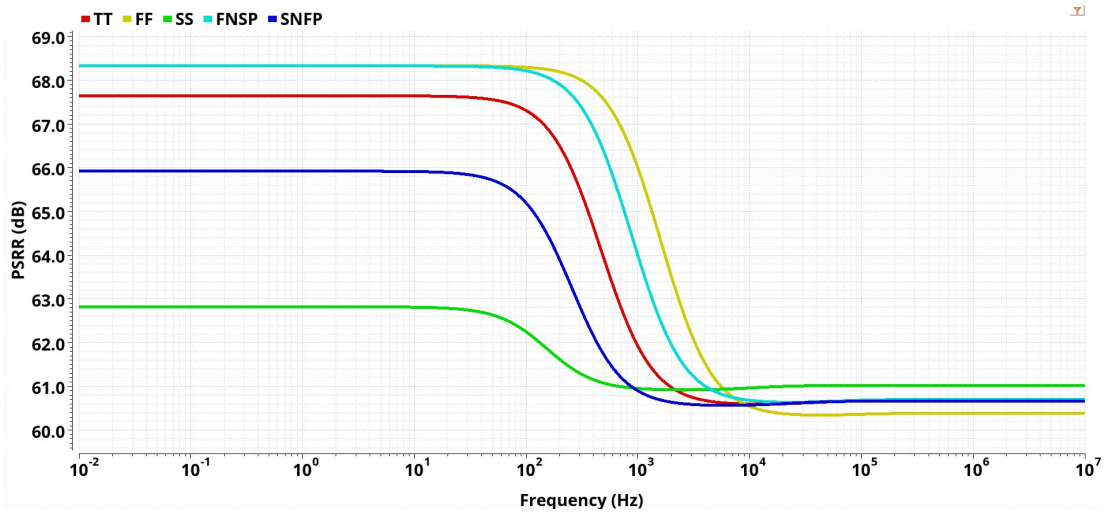


Figure 3.6: PSRR analysis for different process corners - Voltage Reference

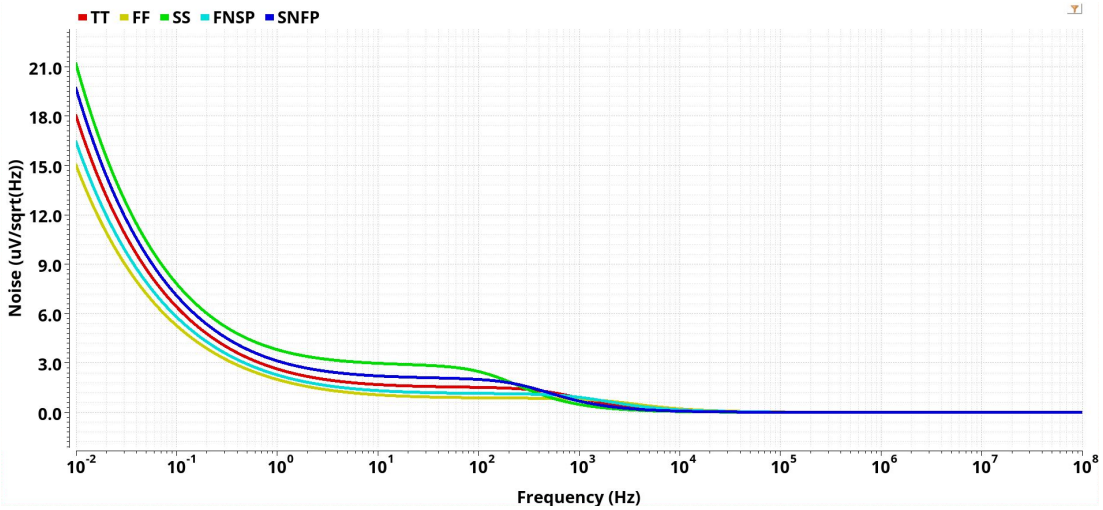


Figure 3.7: Noise analysis for different process corners - Voltage Reference

Table 3.2: Process corners performance - Voltage Reference

Process corners	TT	FF	SS	FNSP	SNFP
$V_{DDmin}(V)$	0.6	0.6	0.55	0.65	0.6
$V_{REF}(mV)$	536	576	504	555	520
Power (nW)	3.26	13.3	0.731	6.68	1.55
LS $(\%/V)$	0.28	0.234	0.509	0.154	0.213
TC $(ppm/°C)$ @T = [0, 80]°C	17	106	54.9	45.5	27.9
PSRR @100Hz (dB)	67.3	68.3	62.2	68.2	65.2
PSRR @10MHz (dB)	60.7	60.4	61	60.7	60.7
Noise @1Hz $(\mu V/\sqrt{Hz})$	2.63	2	3.81	2.27	3.13
Noise @1kHz $(\mu V/\sqrt{Hz})$	0.874	0.802	0.483	0.915	0.685

Chapter 4

CMOS Current References

A current reference is also a crucial building block in the micro-electronics area, which purpose is to generate a constant output current for other components of a device. As well as a voltage reference, a current reference has to ensure stability to variations of process, voltage and temperature, and so the performance can be established measuring the following parameters:

- Line Sensitivity (LS) that specifies the variation of the output current (I_{REF}) with respect to the input voltage variation (V_{DD}), at the nominal temperature (T):

$$LS(\%/V) = \left(\frac{I_{REF_{@V_{DDmax}}} - I_{REF_{@V_{DDmin}}}}{I_{REF_{@V_{DDnom}}}}\right)\left(\frac{1}{V_{DD_{max}} - V_{DD_{min}}}\right) \cdot 100 \tag{4.1}$$

- Temperature Coefficient (TC) that specifies the variation of the output current according to temperature, under the nominal V_{DD}:

$$TC(ppm/^{\circ}\mathrm{C}) = \left(\frac{I_{REF_{max}} - I_{REF_{min}}}{I_{REF_{@T_{nom}}}}\right)\left(\frac{1}{T_{max} - T_{min}}\right) \cdot 10^6 \tag{4.2}$$

In this chapter it is presented a stability study of some state-of-the-art current references with the purpose to demonstrate the differences between these self-biased current references and the proposed one. The feedback is a technique widely used in analog designs in order to make the circuits versatile and achieve a good performance over a wide range of supply voltage, however, this feedback can also cause instability due to the tendency of oscillation. Thus, to avoid this inconstancy, it is expected the open loop gain of the feedback circuit to be positive and lower than one.

4.1 Widlar Current Reference

In the figure 4.1 is illustrated a CMOS version of the well-known current reference of Robert Widlar [37]. The circuit is simply composed by two PMOS, two NMOS and a resistor.

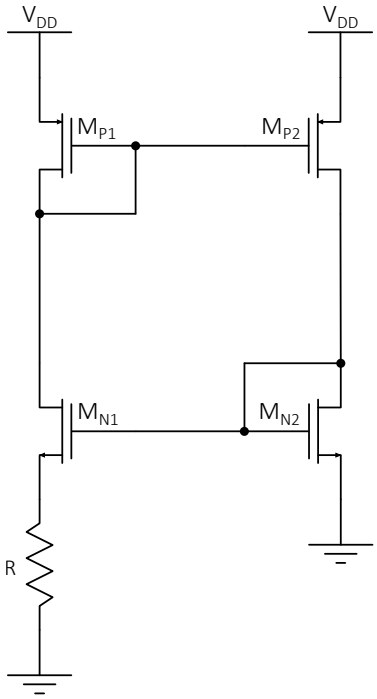


Figure 4.1: Widlar Current Reference

The stability analysis is done in an open loop, thus the loop is opened in the gates of the NMOS pair, in which the gate of M_{N1} is the input voltage and the gate of M_{N2} is the output voltage, once the output should be the diode-connected transistor. Having in mind the small signal MOSFET model, the output (vo) and input (vi) voltage equations, as well as the open loop gain (vo/vi) equation can be written, respectively, as:

$$vo = \frac{1}{gm_{N2}} \cdot (-gm_{P2} \cdot V_{GS_{P2}}) \tag{4.3}$$

$$vi = V_{GS_{N1}} + R \cdot gm_{N1} \cdot V_{GS_{N1}} \tag{4.4}$$

$$\frac{vo}{vi} = \frac{-gm_{P2} \cdot V_{GS_{P2}}}{gm_{N1} \cdot V_{GS_{N1}}} \cdot \frac{1}{(gm_{N2}/gm_{N1}) + gm_{N2} \cdot R} \tag{4.5}$$

where gm corresponds to the transconductance of a transistor. Assuming that $I_{P1} = I_{P2}$ for matching purposes, then $gm_{N1} \cdot V_{GS_{N1}} = -gm_{P2} \cdot V_{GS_{P2}}$, therefore:

$$\frac{vo}{vi} = \frac{gm_{N1}}{gm_{N2}} \cdot \frac{1}{1 + gm_{N1} \cdot R} \tag{4.6}$$

At this point, in order to have the required positive and lower than one open loop gain, it is necessary to garantee that $gm_{N1} < gm_{N2}$. However, the equation for the transconductance of a transistor, using the subthreshold current equation (2.20), is given by:

$$gm = \frac{\delta I_{sub-th}}{\delta V_{GS}} = \frac{I_{sub-th}}{\eta \cdot V_T} \tag{4.7}$$

Accordingly, $gm_{N1} = \frac{I_{P1}}{\eta \cdot V_T}$ and $gm_{N2} = \frac{I_{P2}}{\eta \cdot V_T}$. and as mentioned before $I_{P1} = I_{P2}$ so $gm_{N1} = gm_{N2}$. The open loop gain equation is then simplified as:

$$\frac{vo}{vi} = \frac{1}{1 + gm_{N1} \cdot R} \tag{4.8}$$

which results is always positive and lower than one, independently of the parameter values of the transistors, so the stability of this design is assured.

The values for the transistor sizes, presented in table 4.1, were chosen in order to achieve a good performance and also to have a output current reference of 1 nA, so that the performance values can be comparable to the results of the other current references present in this chapter.

Table 4.1: Parameter values of the Widlar current reference

	$M_{P1,2}$	M_{N1}	M_{N2}	R
W (μm)	80	1	67	88M Ω
L (μm)	48	0.5	16.5	

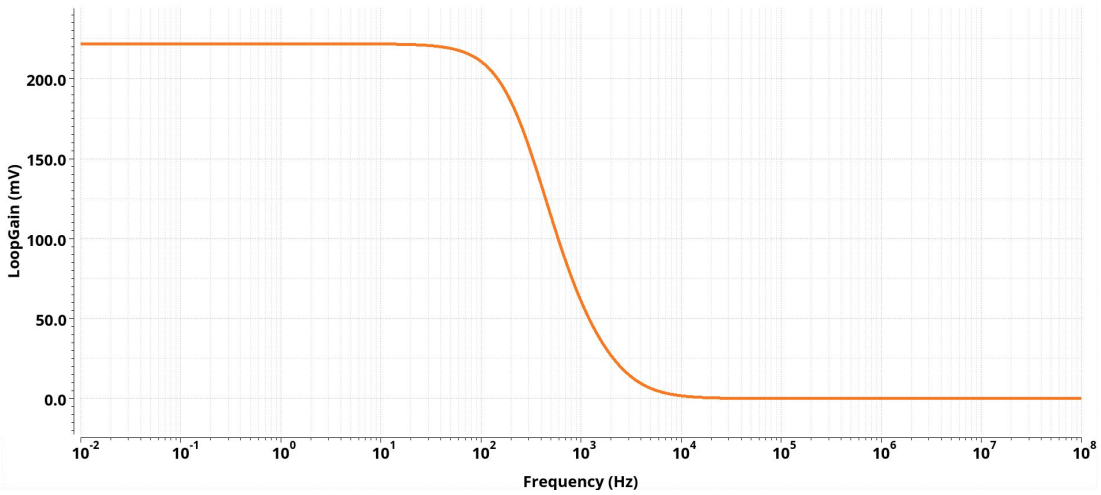


Figure 4.2: Stability analysis of Widlar Current Reference

In order to support the theoretical stability analysis, it was done a simulation in Cadence Virtuoso Analog Design Environment. From the simulation it is possible to get the operation points of the transistors and, for this circuit sizing, $gm_{N1} = 29.4\ nS$ and $gm_{N2} = 29.86\ nS$ which validates the conclusions taken from equation (4.7): $gm_{N1} = gm_{N2}$. Regarding the open loop gain result, by replacing the gm values in the equation (4.8): $vo/vi = 278\ mV/V$. In figure 4.2 is presented the simulated open loop gain response to different frequency values, and for low frequencies, $vo/vi = 222\ mV/V$, which again is very similar to the theoretical result. Note that the

values are slightly different because the output resistance parameter (r_o) of the transistors is being ignored.

Table 4.2 summarizes the performance characteristics of the Widlar current reference. The architecture dimensioned to have a reference current of 1 nA, is able to achieve a minimum supply voltage of 0.75 V, with a LS of 0.486 $\%/V$ and a TC value of 663.3 $ppm/^{\circ}$C, in a temperature range from 0°C to 80°C. Although the performance values of this design are very good, as well as the stability results, the need of a resistor, specially with such a high resistance, generate a significant area overhead, turning the circuit into a inconceivable proposal for IC.

Table 4.2: Performance of the Widlar Current Reference

	Widlar Current Reference
Tech (CMOS)	0.18 μm
V_{DDmin}	0.75 V
I_{REF}	1 nA
Power	6.668 nW
LS	0.486 $\%/V$
TC $(ppm/^{\circ}\text{C})$ @T = [0, 80] °C	663.3 $(ppm/^{\circ}\text{C})$

4.2 Oguey Current Reference

The Oguey *et al.* current reference [38], presented in figure 4.3, is based on the Widlar current reference but the resistor is replaced by a second close loop of transistors. This architecture is then constituted by two feedback, one composed by the transistors M_{P1-2} and M_{N1-2} which can be called by internal feedback, and the other formed by M_{N3-4} and M_{P3} which can be called by external feedback, being the first one influenced by the second.

Table 4.3 presents the chosen size values of the transistors, with the target of achieve a good performance and also to have a output current reference of 1 nA, so that the performance values can be comparable to the results of the other current references present in this chapter.

Table 4.3: Parameter values of the Oguey Current Reference

	$M_{P1,2}$	M_{N1}	M_{N2}	M_{N3}	M_{N4}	M_{P3}
W (μm)	1	6×100	5.5	64.5	36	42.5
L (μm)	4×13.5	50	45.5	0.5	18	4×41.5

Regarding the simulation of the stability analysis, it can be divided into two parts: the first related to the internal feedback and the second related to the external feedback. For the internal feedback, the open loop gain graphic is presented in figure 4.4, and for low frequencies $vo/vi = 47\ mV/V$, which is also positive and lower than one, guaranteeing the stability of the circuit for this loop. In relation to the external feedback, the loop can be opened in the gates of

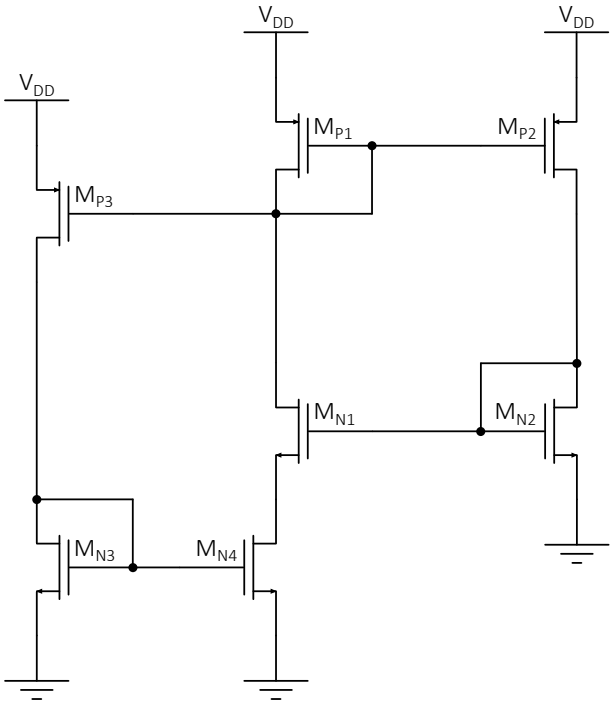


Figure 4.3: Oguey Current Reference

M_{N3-4}, being the gate of M_{N4} the input voltage and the gate of M_{N3} the output voltage, therefore the open loop gain equation can be deducted in this way:

$$V_{GS_{N3}} = \frac{1}{gm_{N3}} \cdot I_{N3} \tag{4.9}$$

$$I_{N3} = I_{N4} = gm_{N4} \cdot V_{GS_{N4}} \tag{4.10}$$

$$\frac{vo}{vi} = \frac{V_{GS_{N3}}}{V_{GS_{N4}}} = \frac{gm_{N4}}{gm_{N3}} \tag{4.11}$$

Thus, to avoid instability, it is critical to ensure that $gm_{N3} > gm_{N4}$. The simulated open loop gain graphic for the external feedback is illustrated in figure 4.5, and it shows that $vo/vi = 926\ mV/V$, so for this sizing the circuit is stable.

Contrasting the stability results for the internal feedback of the Oguey circuit with the results of the Widlar approach, the present outcome is significantly lower, which consequently means that the regulation of the Oguey current reference is worst, specifically LS $= 0.678\ \%/V$. Moreover, the circuit achieves a TC of 38 650 $ppm/°C$, in a temperature range from 0°C to 80°C, and starts working with a minimum supply voltage of 0.95 V. Table 4.4 summarizes the performance characteristics of the oguey current reference.

The main advantage of this architecture, compared to the previous one, is the area reduction once it does not use resistors, still the transistor dimensions are big. In addition, the circuit does not have a temperature compensation technique which results in such an enormous TC value, plus

the minimum supply voltage is almost 1 V, making the circuit hardly belonging to the low-power category, which is a considerable drawback for subthreshold blocks. Also, the circuit stability is dependent on the transistors parameters, which creates design constraints.

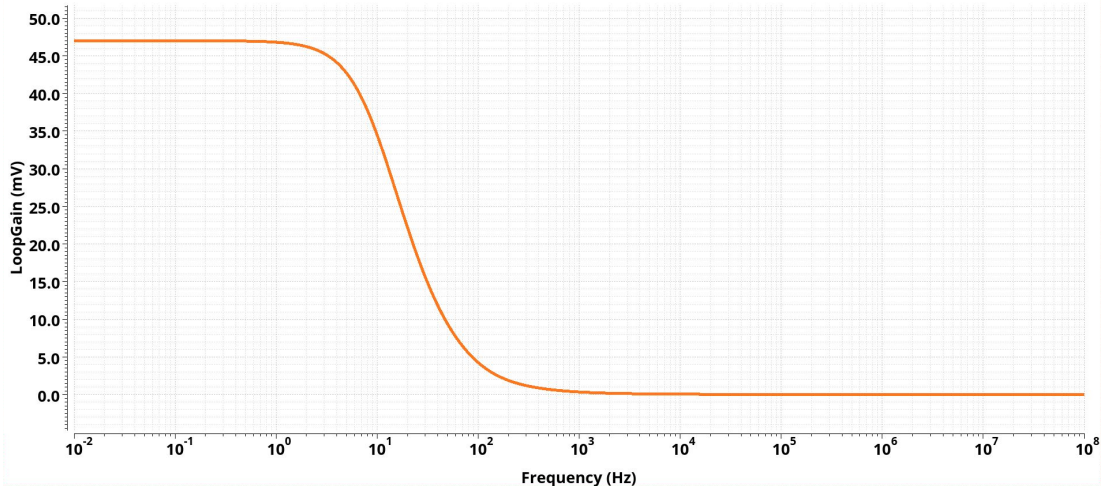


Figure 4.4: Stability analysis of the internal feedback of Oguey Current Reference

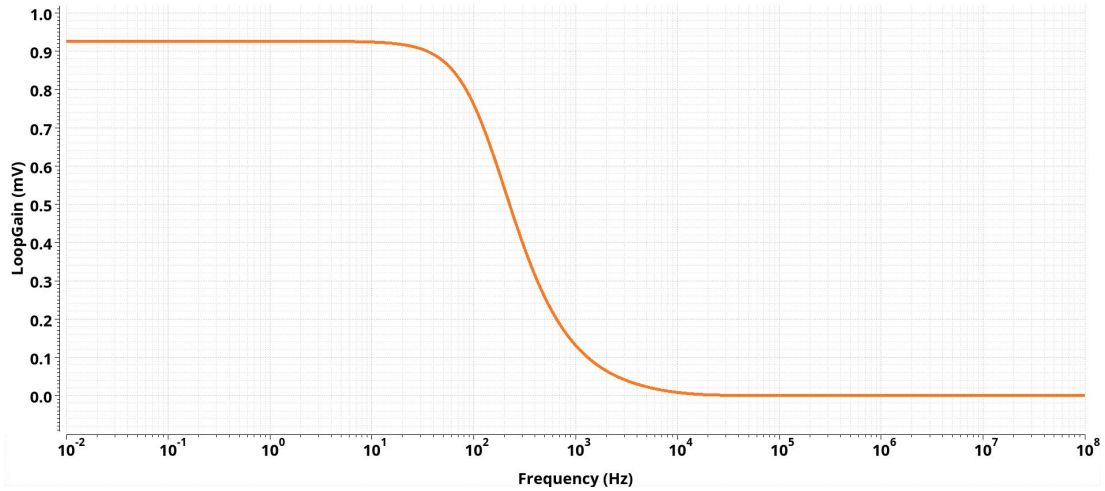


Figure 4.5: Stability analysis of the external feedback of Oguey Current Reference

Table 4.4: Performance of the Oguey Current Reference

	Oguey Current Reference
Tech (CMOS)	0.18 μm
V_{DDmin}	0.95 V
I_{REF}	1.07 nA
Power	70.28 nW
LS	0.678 $\%/V$
TC ($ppm/°C$) @T = [0, 80] °C	38 650 ($ppm/°C$)

4.3 Proposed Current Reference

In this dissertation a current reference is proposed, using CMOS 0.18 μm technology, with the purpose of solving the main problematic approached in the previous sections of this chapter: the instability created by the feedback technique used for self-biasing, and, consequently, the design constrains that derive from ensuring that the circuit is stable and has a good performance, such as, the need of high resistance, high minimum supply voltage or even unsatisfactory TC performance.

In figure 4.6 is illustrated the proposed current reference which design is also based on the Widlar architecture, however instead of using a resistor, or even creating a second closed loop of transistors like Oguey *et al.* suggested, in this proposal a voltage source is applied to generate the circuit current in a open loop structure. Additionally the current reference is also composed by a close loop of transistors formed by M_{P1-2} and M_{N1-2}, and this feedback has the purpose of maintaining the output current for a wide range of supply voltage.

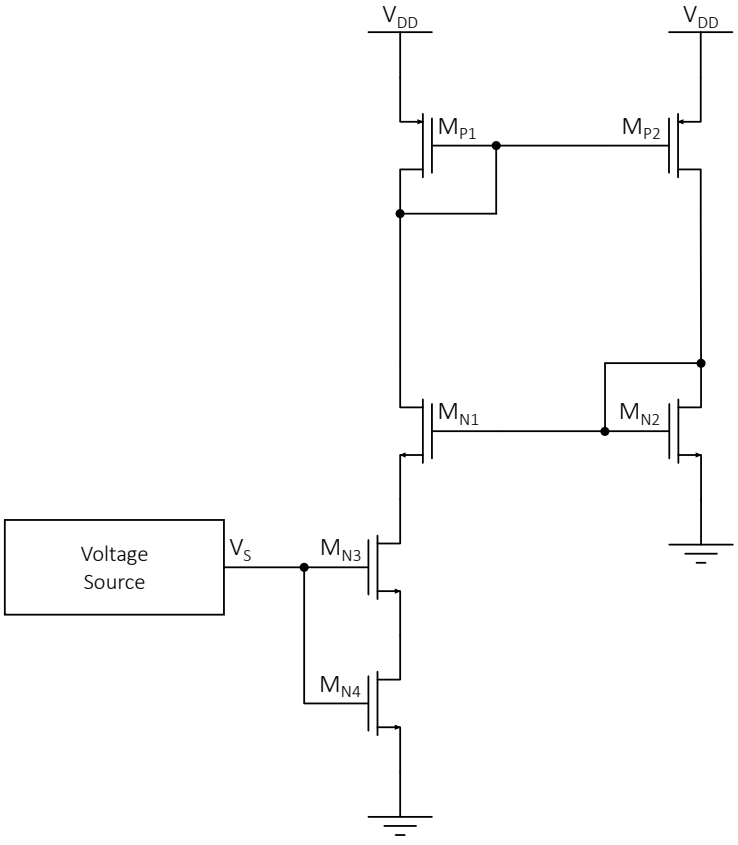


Figure 4.6: Proposed Current Reference

In figure 4.7 is presented the schematic of the voltage source used in the current reference, and it is composed by three parts. Firstly it uses the voltage reference proposed in this dissertation in chapter 3 since its performance comply with the needed specifications at every level. However, the current reference on its own has a first-degree negative TC characteristic which needs to be compensated, and for that purpose is used, secondly, the thermal compensation circuit, which is formed by the transistors M_{P1-2} and M_{N1-2}. The method used by the thermal compensation circuit

consists in creating a symmetric TC characteristic so that both parameters can cancel out. At this point the current reference is thermally balanced, but consequently the excellent LS performance at the output of the proposed voltage reference is now worsened at the output of the thermal compensation circuit, and for that matter a third part is implemented, a DIBL circuit, in another words, a drain-induced-barrier-lowering circuit [39]. This block is composed by the transistors M_{P3-4} and M_{N3-5} and the process consists in withdrawing some supply dependent current from the output branch, like this, the voltage that increases with the supply voltage at the output of the thermal compensation circuit is balanced with the voltage that decreases with the supply voltage generated by the DIBL effect, obtaining a near-zero LS reference voltage, in this case V_S.

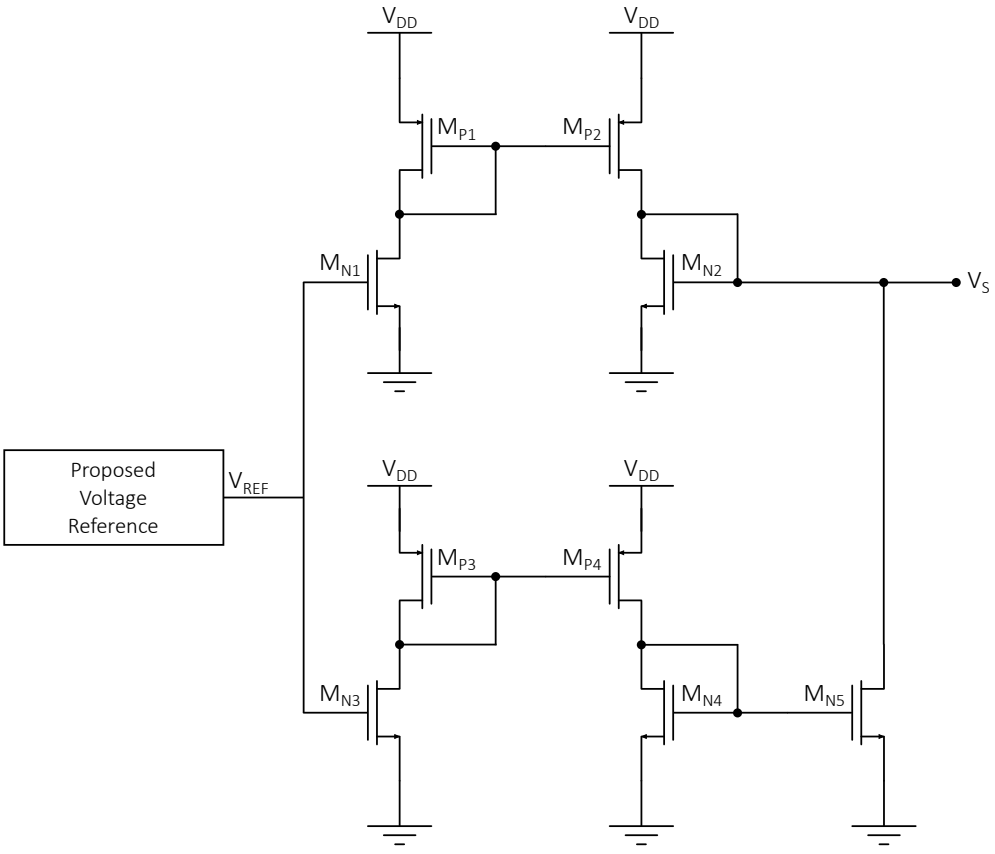


Figure 4.7: Voltage Source Circuit of the Proposed Current Reference

The values for the transistor sizes for both the current reference and its voltage source are presented in table 4.5 and table 4.6, and, again, the parameters were chosen in order to achieve and good performance along with an output current reference of 1 nA, so that the performance values can be comparable to the results of the current references mentioned above in this chapter.

Table 4.5: Parameter values of the Proposed Current Reference

	$M_{P1,2}$	M_{N1}	M_{N2}	M_{N3}	M_{N4}
W (μm)	91	56	11	76	96
L (μm)	26	15.5	2	3	2.5

Table 4.6: Parameter values of the Voltage Source Circuit

	$M_{P1,2}$	M_{N1}	M_{N2}	M_{P3}	M_{P4}	M_{N3}	M_{N4}	M_{N5}
W (μm)	81	11	31	0.5	100	1	31	81
L (μm)	11	41	1	0.5	50	11	21	31

Regarding the stability analysis of the feedback created by M_{P1-2} and M_{N1-2} of figure 4.6, the loop is opened in the gates of the NMOS pair, in which the gate of M_{N1} is the input voltage and the gate of M_{N2} is the output voltage, and their equations as well as the open loop gain equation can be written as:

$$vo = \frac{1}{gm_{N2}} \cdot (-gm_{P2} \cdot V_{GS_{P2}}) \tag{4.12}$$

$$vi = V_{GS_{N1}} + \frac{1}{gm_{P1}} \cdot gm_{N1} \cdot V_{GS_{N1}} \tag{4.13}$$

$$\frac{vo}{vi} = \frac{-gm_{P2} \cdot V_{GS_{P2}}}{gm_{N1} \cdot V_{GS_{N1}}} \cdot \frac{1/gm_{N2}}{1/gm_{N1} + 1/gm_{P1}} \tag{4.14}$$

Assuming that $I_{P1} = I_{P2}$ for matching purposes, then $-gm_{P2} \cdot V_{GS_{P2}} = gm_{N1} \cdot V_{GS_{N1}}$, and also, as explain in equation (4.7), $gm_{P1} = gm_{P2}$ and $gm_{N1} = gm_{N2}$, so the equation (4.14) can be simplified as:

$$\frac{vo}{vi} = \frac{1}{1 + gm_{N1}/gm_{P1}} \tag{4.15}$$

which result is also always positive and lower than one, assuring the stability of the circuit and completly eliminating the oscillation issues.

From the stability simulation it was taken the transconductance values of the transistors, presented in table 4.7, and the conclusions made in the equation (4.7) are, again, corroborated. Replacing this gm values in equation (4.15), $vo/vi = 451\ mV/V$, while from the simulation $vo/vi = 571\ mV/V$ as it is possible to see in figure 4.8 where is illustrated the simulated open loop gain characteristic. Noting that the values are slightly different because the parameter r_o of the transistors is being ignored, the open loop gain results are similar enough, reconfirming the theoretical analysis.

Table 4.7: Transconductance values of the Proposed Current Reference

gm_{P1}	gm_{P2}	gm_{N1}	gm_{N2}	gm_{N3}	gm_{N4}
25.63nS	25.78nS	31.23nS	31.81nS	31.79nS	31.71nS

The figures 4.9 and 4.10 show the results of the corner analysis for LS and TC, respectively, and the table 4.8 summarises the outcomes of each performance test for each process corner. As seen from these results, the circuit has a general worse performance at every corner, being the deviations quite significant. For SNFP transistors, the circuit seems to have a more reliable operation,

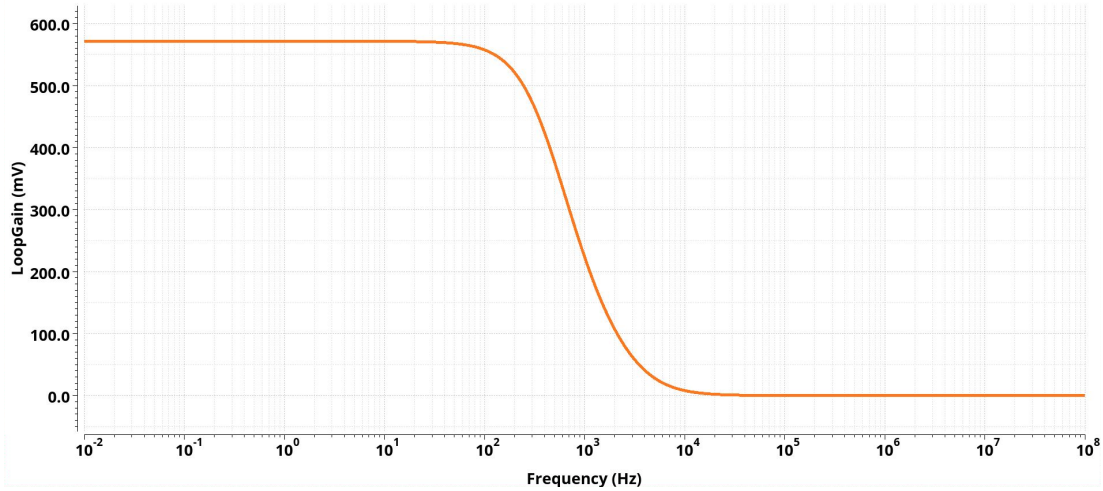


Figure 4.8: Stability analysis of the Proposed Current Reference

being the main divergence coming from the output current which value is half of the intended. For TT process corner, the current reference achieves an output current of 1.05 nA, powered by a minimum supply voltage of 0.65 V and consuming 106.3 nW. Regarding the performance parameters, the circuit obtains a LS of 1.714 $\%/V$ and a TC of 71.86 $ppm/°C$, in a temperature range from 0°C to 80°C.

A Monte Carlo analysis was not possible to do because there is no model files for ZVT devices.

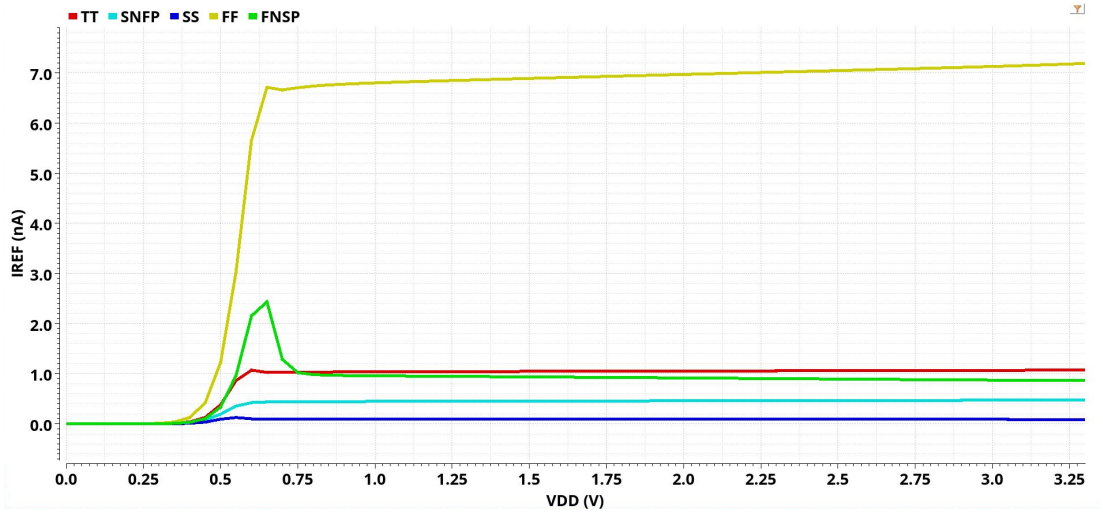


Figure 4.9: LS analysis for different process corners - Current Reference

4.4 Proposed Trimming Circuit

On account of the significant divergence of the output reference current values of each corner, a trimming circuit was developed in order to compensate those values to the reference of 1 nA. The process compensation is achieved with external control bits that activate and deactivate certain

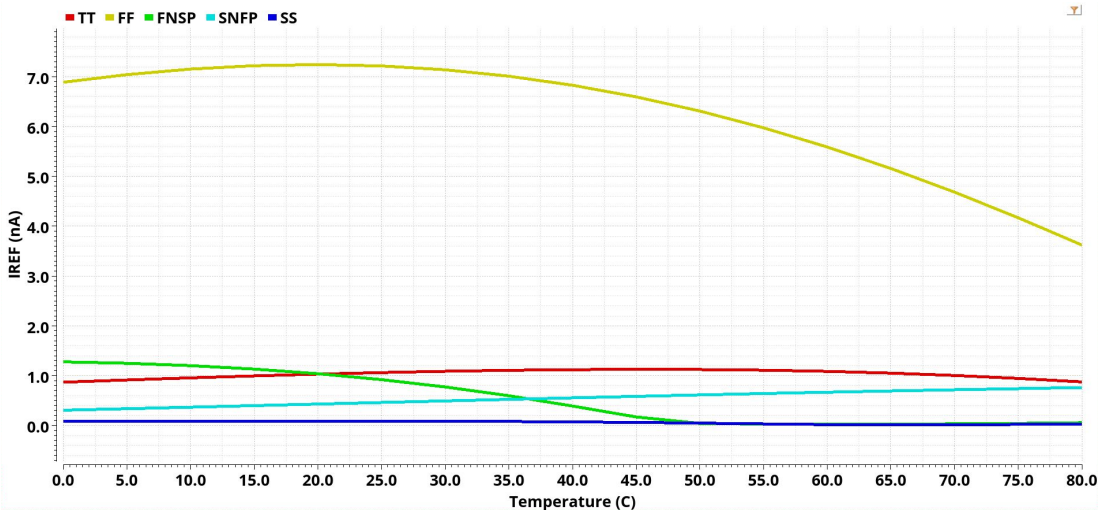


Figure 4.10: TC analysis for different process corners - Current Reference

Table 4.8: Process corners performance - Current Reference

Process corners	TT	FF	SS	FNSP	SNFP
V_{DDmin} (V)	0.65	0.7	0.65	0.75	0.65
I_{REF} (nA)	1.05	6.972	0.092	0.914	0.458
Power (nW)	106.3	719.6	14.92	291.4	29.78
LS $(\%/V)$	1.714	2.911	-3.103	-6.756	3.199
TC $(ppm/°C)$ @T = [0, 80] °C	71.86	5 683	6 830	17 720	12 020

transistors to lower or increase the intended current [40]. The circuit is presented in figure 4.11, and is composed by a set of seven pairs of PMOS transistors in parallel, which are connected to the gate of M_{P1} of the proposed current reference, illustrated in figure 4.6, being the input of the circuit seven control bits (b_{0-6}), and the output is the drain of the transistors M_{8-14}. This output node, as previously mentioned, varies accordingly to the transistors that are activated, so for different digital words there are different outputs, once the output current is the sum of the currents of the activated transistors.

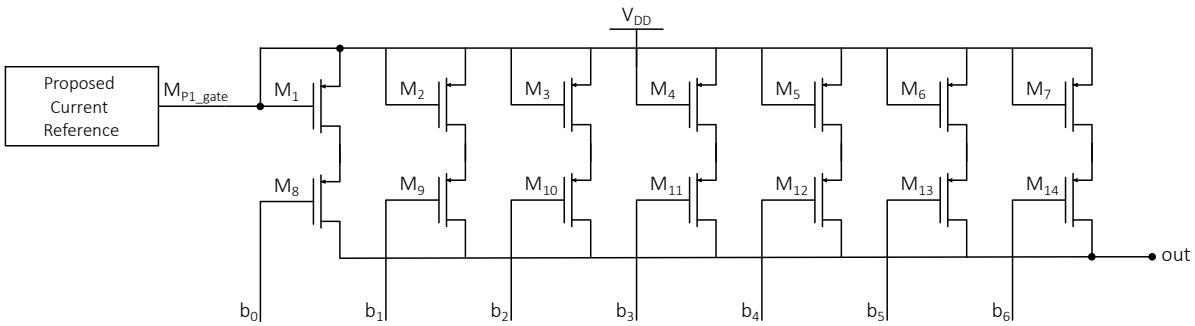


Figure 4.11: Proposed Trimming Circuit - Current Reference

The number of parallel devices was defined so that it compensates for a wide range of supply

voltage and for all process corners. The transistors sizes of the trimming circuit are shown in table 4.9, and there is a scaling of the width values for the transistors M_{1-7} which increases by the power of 2, creating a binary word with a minimum resolution defined by the size of the smallest PMOS (M_1).

Table 4.9: Parameter values of the Proposed Trimming Circuit

	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_{8-14}
W (μm)	0.55	0.55	0.55	0.55	0.55	0.55	0.55	0.24
L (μm)	26	26	26	26	26	26	26	0.34
multiplicity	16	32	64	128	256	512	1024	1

Therefore, with 7 bits it was possible to determinate a digital word for each process corner, which are presented in table 4.10. By applying the respective digital word to each corner, a trimmed output current is then achieved, as it is possible to see in figure 4.12, and so for every process deviation it is now feasible to adjust to the pretended point using the proposed trimming circuit.

Table 4.10: Digital word for the Proposed Trimming Circuit

Process corners	FF	SS	FNSP	SNFP
Digital Word	1111110	0001011	1110101	1101101

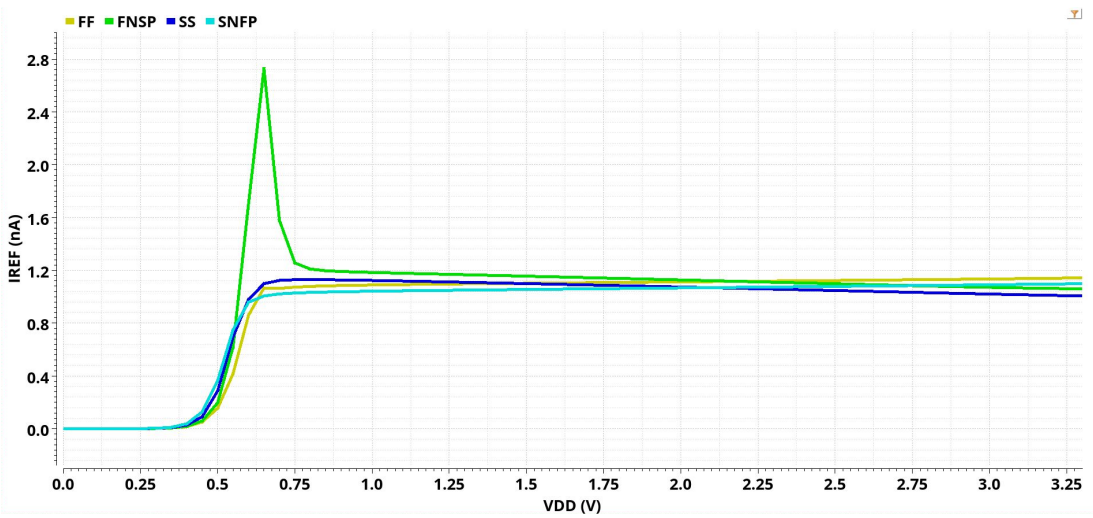


Figure 4.12: LS analysis for different process corners after Trimming - Current Reference

Table 4.11 summarises the performance outcomes of the current reference after trimming for each process corner and, as expected, it is noticeable the regulated values of I_{REF} to 1 nA. Comparing this results to the ones achieved before trimming, presented in table 4.8, it is possible to see that the minimum supply voltages as well as the line sensitivity do not suffer from big variations,

however, the TC performance has big improvements. On the other hand, the power consumption of the circuit, as predicted, increases.

Table 4.11: Process corners performance after trimming - Current Reference

Process corners	TT	FF	SS	FNSP	SNFP
V_{DDmin} (V)	0.65	0.65	0.65	0.75	0.60
I_{REF} (nA)	1.05	1.11	1.07	1.13	1.07
Power (nW)	106.3	735.7	18.5	735.7	33.68
LS $(\%/V)$	1.714	2.601	-3.26	2.601	4.888
TC $(ppm/°C)$ @T = [0, 80] °C	71.86	2 475	4 775	2 475	19 000

4.5 Conclusions

In the table 4.12 is compiled a summary of the performance of the current references approached in this chapter.

Table 4.12: Comparison table of Current References

	Widlar	Oguey	Proposed
Tech (CMOS)	0.18 μm	0.18 μm	0.18 μm
V_{DDmin} (V)	0.75	0.95	0.65
I_{REF} (nA)	1	1.07	1.05
Power (μW)	6.668	70.28	106.3
LS $(\%/V)$	0.486	0.678	1.714
TC $(ppm/°C)$ @T = [0, 80] °C	663.3	38 650	71.86
Open Loop Gain (mV/V)	222	47	571

The proposed current reference has several enhancements when compared to the state-of-the-art Widlar and Oguey. First of all its architecture is resistorless which implies that the area occupation is considerably lower than the Widlar's and for IC nowadays it is a critical specification. Secondly its minimum supply voltage is the lowest one, it is important that when a current reference is integrated in a major block its starting point as well as its range of operation is equally low and broad. Moreover, the performance related to the temperature compensation of the proposed reference is also the leading one.

On the other hand, both the power and line sensitivity of the circuit reveal to be unfavourable in the overall performance. However, the open loop gain results show that, not only all the circuits are stable, but also that the highest value belongs to the proposal in this dissertation, and the highest the outcome the better is its regulation. Therefore, the current reference on its own, independent of the voltage source, has a quality LS performance. In conclusion, it was identified that the inferior performance in power and LS comes from the thermal compensation circuit, specifically, it is responsible for 70% of the total power consumption.

Chapter 5

Integration

In this chapter is presented an integration of the previously developed building blocks. As seen in figure 5.1, this final solution is composed by three main blocks: the voltage reference mentioned in chapter 3, the current reference introduced in chapter 4, and an operational amplifier which purpose is to work as a buffer of the output voltage reference, and will be presented with more detail further in this chapter.

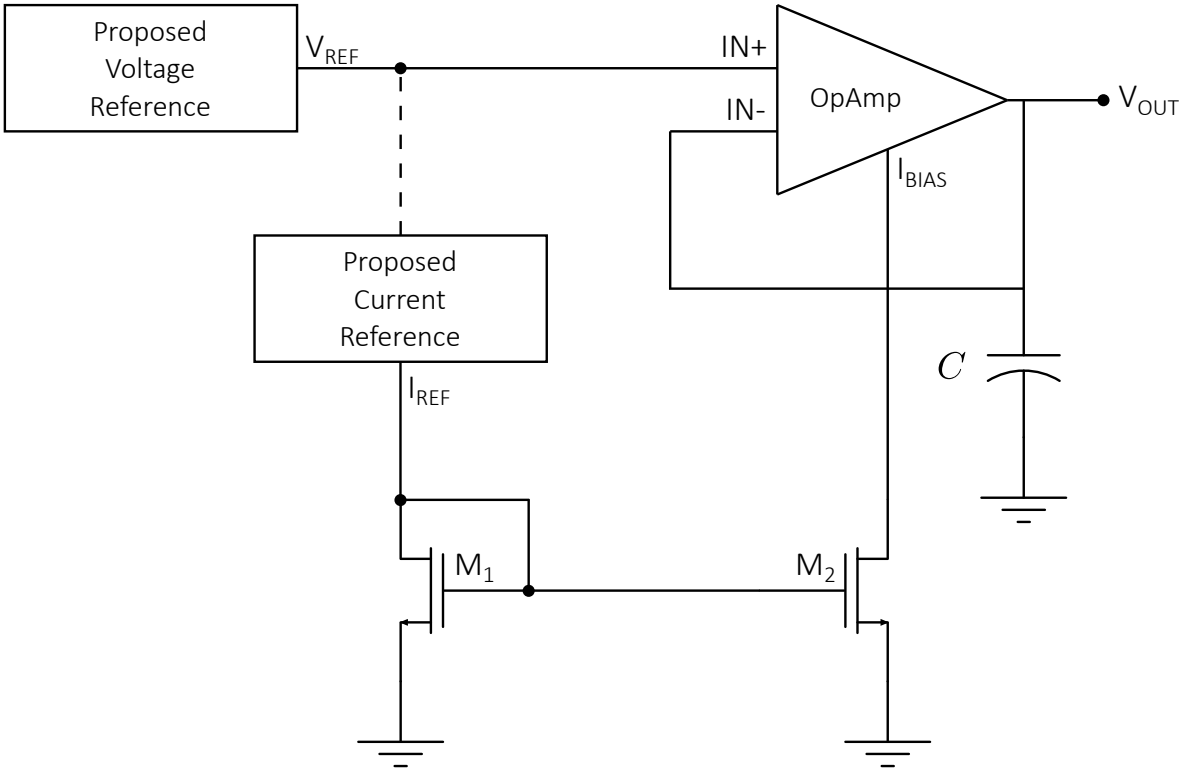


Figure 5.1: Proposed Solution

The flow between these blocks work as followed:

1. There is an output voltage coming from the respective voltage reference block (V_{REF}), and this voltage apart from being introduced in the OpAmp for subsequent buffering, it is also

used as an input of the current reference block.

2. Thereafter, an output current is generated by the current reference block (I_{REF}), which is used, along with the transistors M_{1-2}, to drive the operational amplifier.

3. Finally, the OpAmp by receiving as an input the voltage and current references, and note that is connected in feedback, it generates the output reference voltage of the all system (V_{OUT}).

5.1 Operational Amplifier

A unity gain operational amplifier is used as a voltage follower for V_{REF}, and its necessity stem from isolation requirements, preventing leakage currents from supplying other circuit components. For that the OpAmp, illustrated in figure 5.2, has to be connected in a closed-loop feedback, and once its gain is unitary, the magnitude value of the voltage reference is not impacted.

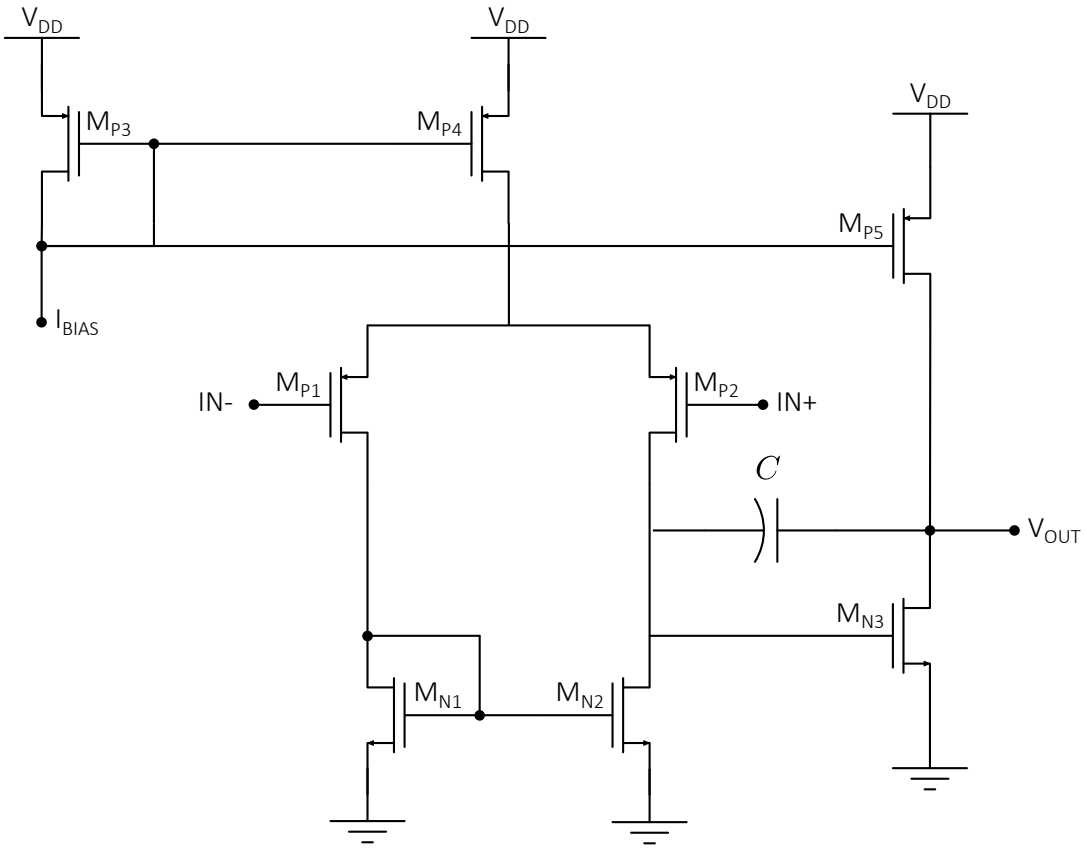


Figure 5.2: Operational Amplifier

The chosen values for the transistor sizes are described in table 5.1. It was defined a length value for all the transistors of 1 μm, in order to be high enough to guarantee immunity to process variations, and at the same time low once the operation regime is subthreshold. Regarding the initial specifications to be achieved, it was defined: a phase margin (PM) > 60°, in order to ensure

stability of the feedback loop, a common-mode rejection ratio (CMRR) > 40 dB and the lower power consumption possible.

Table 5.1: Parameter values of the Operational Amplifier

	$M_{P1,2}$	$M_{N1,2}$	$M_{P3,4}$	M_{P5}	M_{N3}	C
W (μm)	2.4	2.4	52	4×27	4×0.5	5pF
L (μm)	1	1	1	1	1	

After simulation it was verified that the operational amplifier is able to achieve a PM = 75.2°, CMRR = 55.8 dB and a power consumption of 14.3 nW. Moreover, it was measured its common-mode input range in which it can be seen that the output of the OpAmp in a unitary gain closed-loop follows its input, being its deviation of merely of 220 μV.

5.2 Proposed Solution

Resuming the development of the complete proposed solution, the parameters values presented in table 5.2 were the chosen ones. The transistor M_1 has half the width size of the transistor M_2, with the purpose of reducing the current flowing through that branch and consequently reducing its power consumption. Regarding the capacitor, it is needed a capacitance of 120 pF to achieve a PSRR performance close to 60 dB.

Table 5.2: Parameter values of the Proposed Solution

	M_1	M_2	C
W (μm)	45.5	91	120pF
L (μm)	26	26	

A process corner analysis for the performance measures LS, TC, PSRR and Noise was done, which results are shown in figure 5.3, 5.4, 5.5 and 5.6, respectively. The table 5.3 summarises the outcomes of each performance test for each process corner.

A Monte Carlo analysis was not possible to do because there is no model files for ZVT devices.

Similarly to the voltage reference, this final solution has a worst performance when using faster NMOS devices. For TT process corner, the circuit achieves an output voltage of 536 mV, powered by a minimum supply voltage of 0.8 V and consuming 128 nW. Regarding the performance parameters, the circuit obtains a LS of -0.386 $\%/V$ and a TC of 18.5 $ppm/°$C, in a temperature range from 0°C to 80°C.

Once it is intended that the output of the operational amplifier (V_{OUT}) is as similar as possible to the output of the voltage reference building block (V_{REF}), the performance results of both structures are compared:

- The minimum supply voltage increases 0.2 mV at the output of the OpAmp. This is due to the spike existing in the current reference block, specifically in its thermal compensation circuit.
- The power consumption of the final implementation is around 40$\times$ higher that the one consumed by the voltage reference. This increase is expected once the complete integration has to power not only the voltage reference, but also the current reference and the OpAmp. However approximately 80% of the consumption is spent in the thermal compensation circuit.
- In relation to the output voltage, line sensitivity and the temperature coefficient, the performance of both structures are very similar, not presenting significant variations.

All in all, the circuit integration achieves good outcomes, and the source of the main drawbacks is the thermal compensation circuit.

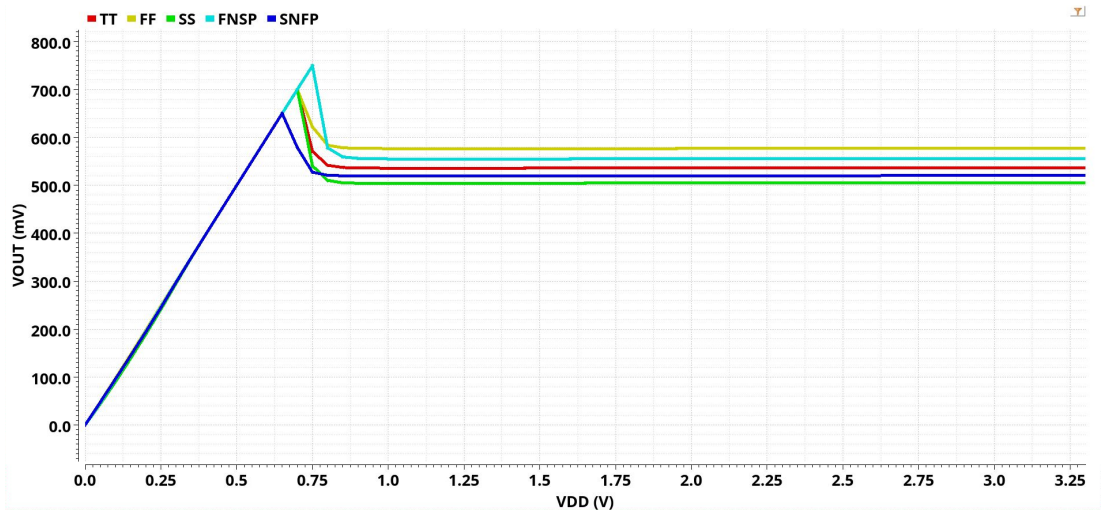


Figure 5.3: LS analysis for different process corners - Proposed Solution

Table 5.3: Process corners performance - Proposed Solution

Process corners	TT	FF	SS	FNSP	SNFP
$V_{DDmin}(V)$	0.8	0.8	0.8	0.85	0.75
$V_{REF}(mV)$	536	577	505	555	520
Power (nW)	128	851	17.3	314	39.3
LS $(\%/V)$	-0.386	-0.446	-0.368	-0.261	-0.519
TC $(ppm/°C)$ @T = [0, 80] °C	18.5	108	47.5	53.1	26.6
PSRR @100Hz (dB)	51.5	69.1	47.2	47.5	32.5
PSRR @10MHz (dB)	60	59.8	60.2	60	60
Noise @1Hz $(\mu V/\sqrt{Hz})$	96.1	87.9	96.8	97	95
Noise @1kHz $(\mu V/\sqrt{Hz})$	0.404	6.57	0.0393	0.31	0.164

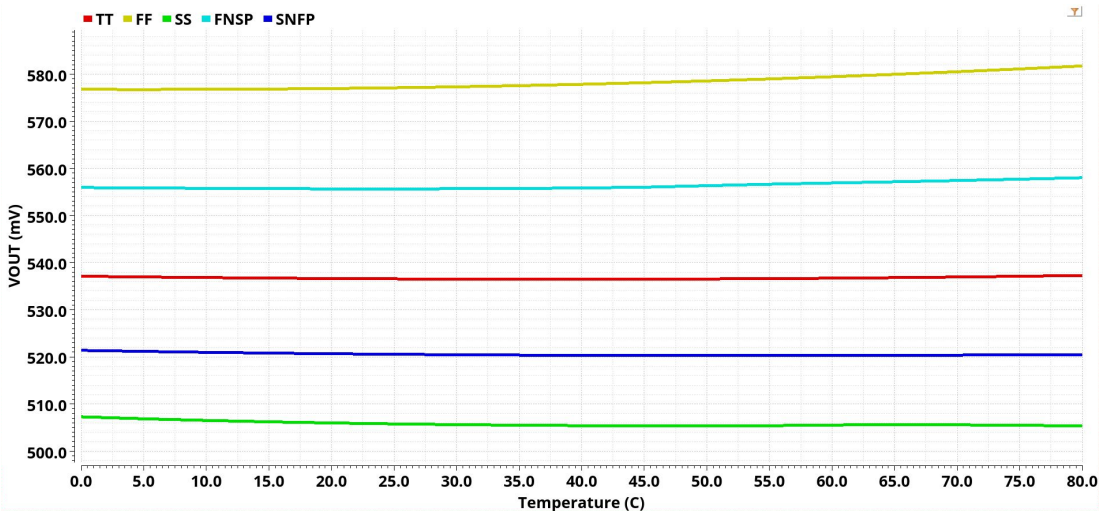


Figure 5.4: TC analysis for different process corners - Proposed Solution

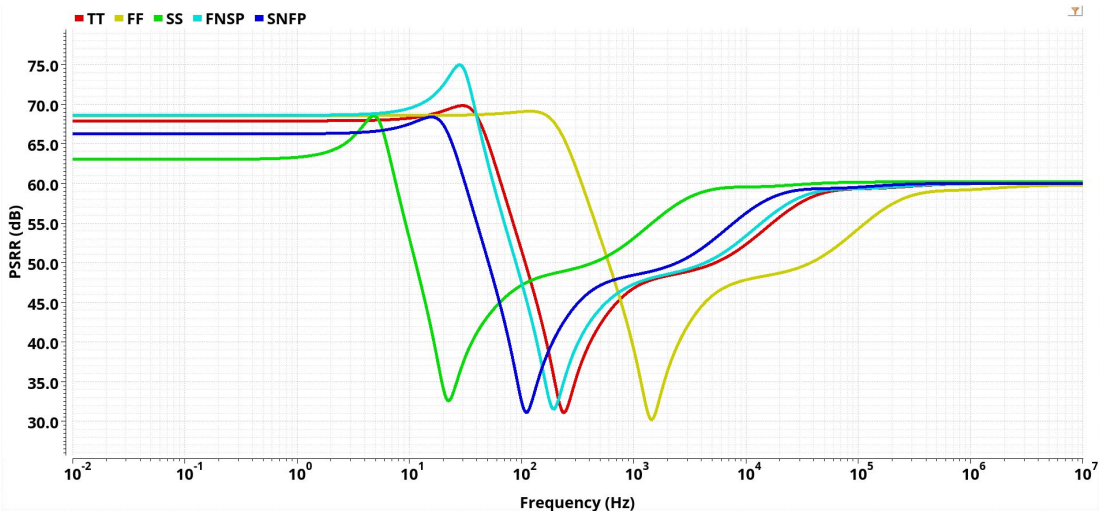


Figure 5.5: PSRR analysis for different process corners - Proposed Solution

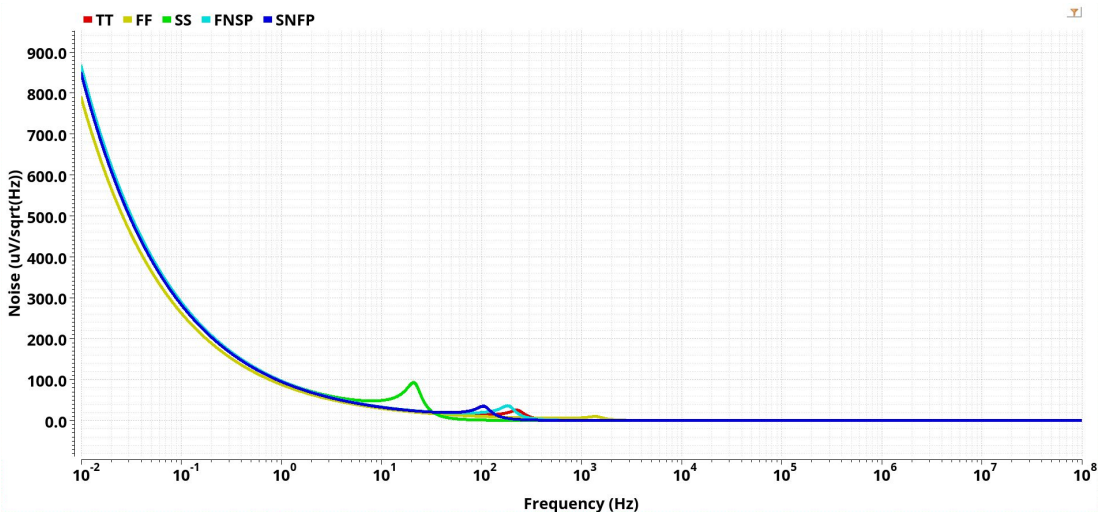


Figure 5.6: Noise analysis for different process corners - Proposed Solution

The layout of the proposed solution is presented in figure 5.7, achieving a total area of 0.147 mm^2. Note that the voltage reference represents 0.7% of the total area, the current reference represents 27.5% and the operational amplifier represents 6.25%. Even thought it was possible to overlap the capacitors once its metal composition is not used for routing, it represents the majority of the area consumption.

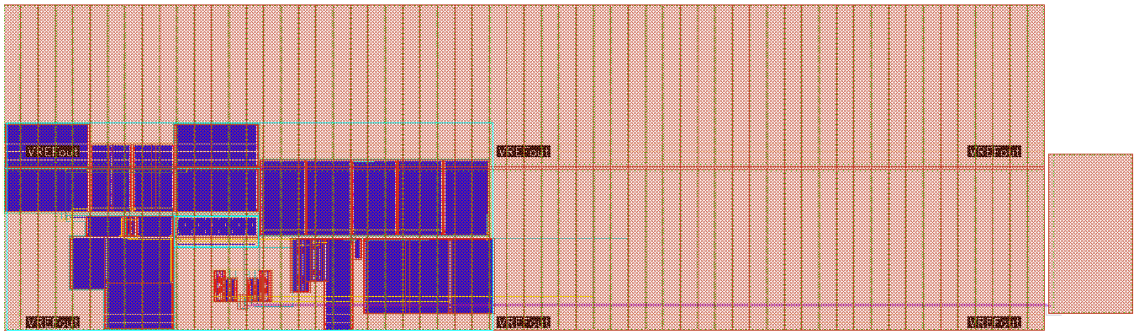


Figure 5.7: Layout - Proposed Solution

Chapter 6

Conclusion

The main contribution of this dissertation is the development of low-power references for subthreshold analog circuits, namely a voltage reference and a current reference. Furthermore, an integration of both of these blocks was done, along with an operational amplifier, being the final proposal a voltage reference as well complemented with a buffer.

The voltage reference achieves an output voltage of 536 mV, powered by a minimum supply voltage of 0.6 V and consuming 3.26 nW. Regarding the performance parameters, the circuit obtains a LS of 0.28 $\%/V$ and a TC of 17 $ppm/^{\circ}$C, in a temperature range from 0°C to 80°C.

The current reference achieves an output current of 1.05 nA, powered by a minimum supply voltage of 0.65 V and consuming 106.3 nW. Regarding the performance parameters, the circuit obtains a LS of 1.714 $\%/V$ and a TC of 71.86 $ppm/^{\circ}$C, in a temperature range from 0°C to 80°C. After implementing a trimming circuit at the output of the current reference in order to compensate the variations caused by the process, every process corner achieves an output current of 1 nA.

The final proposed circuit achieves an output voltage of 536 mV, powered by a minimum supply voltage of 0.8 V and consuming 128 nW. Regarding the performance parameters, the circuit obtains a LS of -0.386 $\%/V$ and a TC of 18.5 $ppm/^{\circ}$C, in a temperature range from 0°C to 80°C.

The structures, developed in CMOS 0.18 μm technology, comply with the requirements for subthreshold circuits: low supply voltage, low power consumption, stable voltage or current output, small size and good results for LS, TC, PSRR and Noise. Therefore, the proposals in this dissertation are suitable to be used in IC.

6.1 Future Work

The next steps into improvement and further development in this dissertation would be:

- Improve the thermal compensation circuit since it is responsible for around 80% of the total power consumption, and for an increase of the minimum supply voltage of the final implementation, and also for a lower LS performance of the current reference block.

- Perform post-layout simulations, followed by the implementation of the needed layout improvements.
- Develop a trimming circuit for the final structure in order to compensate the process, voltage and temperature variations resulting from the fabrication process.

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