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Review

Comparison of DSOGI-Based PLL for Phase Estimation in Three-Phase Weak Grids

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Abstract: The paper presents a summary of different double second-order generalized integrator (DSOGI)-based phase-locked loop (PLL) algorithms for synchronization with three-phase weak grids. The different methods are compared through simulation under a variety of grid conditions, such as unbalanced phase voltages, high low-order harmonics distortion, frequency steps, phase jumps, and voltage sags. Following the simulation results, the three methods that have shown the overall best results are compared through an experimental setup for further results validation under operation with a voltage-source converter. Based on the obtained results, a benchmark table is presented that allows ranking the performance of the tested methods for different expected grid conditions.

Keywords: synchronism; PLL; DSOGI; positive sequence; fundamental frequency; weak grids; frequency; phase

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1. Introduction

Microgrids are currently an extensive topic of discussion since such a concept presents a viable solution to allow the integration of distributed energy resources near loads without disturbing or contributing to the stability of the main grid. Those microgrids can operate either when connected to the main grid or disconnected (island mode). During island mode operation, the inertia provided from the main grid is no longer available, and the local grid becomes very sensitive to power changes (weak grid). To guarantee the adequate operation of the connected power converters, one of the key aspects is to ensure synchronization under the mentioned conditions.

The power converters control loop is normally fully or partially performed as in the synchronous reference frame (SRF), where voltage estimation becomes even more critical as the phase estimation errors are propagated to the synchronous voltage and current measurements through the Park transform. Additionally, methods such as droop control or the virtual synchronous generator demand stable frequency measurement/estimation to achieve robust and proper power-sharing. The phase-locked loop (PLL) is designed primarily to estimate the phase of the voltage fundamental frequency positive sequence, but it also allows to obtain a stable voltage amplitude and frequency as discussed in this paper. The importance of the phase angle estimation is addressed in [1], where it is studied the dynamic impact of phase jumps in synchronous generators and power converters, which may be caused by the estimation error during the connection with the grid.

There are currently several techniques to achieve grid synchronization, though it is not possible to point to a single synchronization algorithm that can simultaneously be the most accurate, fastest, most robust and lightest for every grid condition. Therefore, it is naturally necessary to establish a compromise between different goal objectives or grid conditions before choosing a particular synchronization algorithm.

In accordance with [2], there are two main methods to achieve grid synchronization: open-loop or closed-loop. In an open-loop approach, the phase angle is directly estimated

from a filtered signal. In the closed-loop, there may exist a filtering stage but angle estimation is obtained through a closed-loop structure.

An open-loop and simple technique for grid synchronization is zero cross-detection, which allows synchronizing with the grid at every instant that the grid voltage crosses a reference zero. The synchronization is achieved through the detection of the zero-cross events and the generation of a rectangular waveform, accordingly. The resulting waveform allows to estimate the phase and frequency but only during the zero-cross instants; for that reason, it presents phase tracking slow dynamics and it is susceptible to external interference, leading to phase tracking errors [3,4]. With such a technique, synchronization is achieved for a single-phase system, twice per cycle. Additionally, voltage harmonics or measurement noise may lead to undesired zero-crossing detection if no filters are added. Another open-loop approach is the use of filters in the $\alpha\beta$ frame and prior angle calculation through a trigonometric relationship. Some of those filters include the Butterworth low-pass filter, space vector filter, adaptive notch filter, *etc*. As an alternative to digital filters, there can be found methods that suggest the use of discrete Fourier transform, Kalman filters, least mean square [5], or sliding mode control [6].

Another method, and the most common synchronization technique in grid-tied power converters, is the closed-loop approach known as the synchronous reference frame phase-locked loop (SRF-PLL). The SRF-PLL presents fast dynamics with a very low steady-state error when no low order harmonics exist and balanced conditions are considered [7]. Such assumptions are unrealistic in most real cases, especially when considering weak grids. Hence, most of the advanced PLL algorithms consist of the application of techniques to extract the fundamental frequency positive sequence (FFPS) of the grid voltage and further phase tracking through the SRF-PLL [8–10].

To extract the FFPS, the authors in [11] suggest the application of a double synchronous reference frame: one rotating with the positive frequency and another in the opposite direction (negative sequence). A decoupling network is presented that allows the extraction of the positive sequence from the double SRF. Furthermore, a second-order low pass filter is applied at the output to reduce harmonics interference in the positive sequence synchronous voltage estimation.

Another method is based on the single-phase enhanced PLL (EPLL). In this method, it is applied a quadrature signal generator based on the second-order generalized integrator (SOGI-QSG) to obtain a lagging 90 degrees phase shift of the input signal, offering simultaneously a filtering capability at frequencies beyond the filter central frequency [12]. An extension of this method [13] consists of considering a double SOGI-QSG (DSOGI-QSG), i.e., two SOGI-QSG are used to obtain the direct and quadrature signals of the alpha and beta components, respectively, for further positive sequence calculation. This method allows obtaining the positive sequence with intrinsic filtering capability. Since the DSOGI-QSG central frequency is adjusted accordingly with the PLL frequency, the DSOGI is a frequency-adaptive filter. Additionally, in [10], it is shown that the DSOGI-PLL is equivalent to the DSRF-PLL under certain conditions; therefore, the analysis on this paper disregards the second. The DSOGI-QSG can be applied with phase tracking (PLL) or frequency tracking, becoming a frequency-locked loop (FLL).

In [10,14–18] different PLL methods, including the DSOGI-based PLL, are compared and qualified where the DSOGI is highlighted as one of the most performant. Though it does not discriminate the performance of different DSOGI-based methods and in most of the tests, it lacks numerical performance quantification.

The paper is separated into eight sections. In Section 2 it is introduced the basic principle of work of the closed-loop PLLs, based on the synchronous reference frame (SRF-PLL). The generation of the quadrature signal, its extension to form the double second-order generalized integrator, and the extraction of the positive and negative phases sequence are presented in Section 3. In Section 4, it is presented the complete structure of the PLLs for synchronization with the grid-positive sequence and in Section 5, synchronization through the frequency-locked loop (FLL). Section 6 presents the simulation and experimental

results and the respective discussion. Finally, in Section 7, it is discussed the main chapter conclusions and the PLL implementation chosen for the thesis is justified.

2. Synchronous Reference Frame Phase-Locked Loop

The SRF-PLL is based on the *dq0* frame, and it is illustrated in Figure 1. The principle of operation consists of orienting the voltage vector in the *dq0* frame to be aligned with a reference phase of the three-phase voltage system. To achieve this, the quadrature component of the voltage in the *dq0* frame is controlled to zero, typically through a proportional-integral (PI) controller. It is important to notice that in the synchronous frame (*dq0* frame), all vectors rotating at synchronous speed are represented in a steady state by a constant, direct and quadrature component. The output of the PI is further integrated to obtain the phase angle that is used as feedback for the calculation of the *dq0* transformation matrix. In the steady state, the PI output and the forward compensation represent the grid frequency ω'.

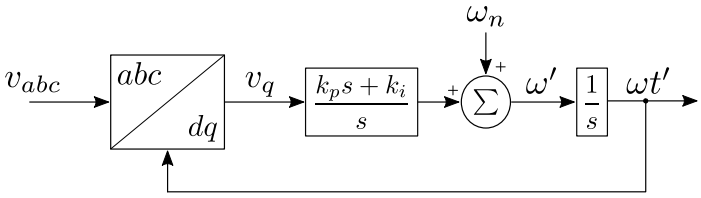


Figure 1. Block diagram of the SRF-PLL.

The Clarke and Park (1) transformation matrix, presented in Figure 1, are in the power invariant form and aligned with the cosine of phase v_a. Notably, the zero component is disregarded since it does not influence the synchronization loop. Additionally, the PI gains k_p and k_i are tuned in accordance with [3] and synthesized in Equation (2), where ω_c represents the filter natural (or controller) frequency, ζ the damping, and E_g the grid peak voltage amplitude.

$$T_{abc\to\alpha\beta} = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}, \quad T_{\alpha\beta\to dq} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix} \tag{1}$$

$$\begin{cases} k_p = \dfrac{2\omega_n \zeta}{E_g} \\ k_i = \dfrac{E_g}{4\zeta^2} \end{cases} \tag{2}$$

3. Fundamental Frequency Positive Sequence Extraction

This section reviews the principle of operation of the SOGI filter, its extension to the DSOGI, and the decoupling network that allows extracting the positive and negative grid phase sequence.

3.1. Second-Order Generalized Integrator-Quadrature Signal Generator

The SOGI-QSG is based on a band-pass filter tuned at a center frequency ω_0 and quality factor k $(= 1/Q)$. There are two main particularities on this filter: one is that it presents at the center frequency two outputs with unitary gain (the input signal with 0° and with 90° phase delay); the second is that allows to adapt the center frequency. Hence, at the center frequency, the SOGI-QSG generates the direct and quadrature signals of the input filtered signal. Such behavior can be further understood by analyzing the filter block diagram of Figure 2, the transfer functions (3) and the respective bode plots as illustrated in Figure 3.

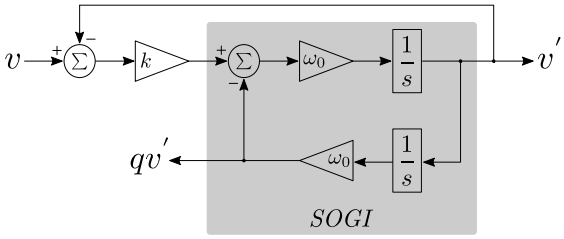


Figure 2. SOGI-QSG block diagram.

$$\begin{aligned} D(s) &= \frac{v'}{v}(s) = \frac{k\omega' s}{s^2 + k\omega' s + \omega'^2} \\ Q(s) &= \frac{qv'}{v}(s) = \frac{k\omega'^2}{s^2 + k\omega' s + \omega'^2} \end{aligned} \tag{3}$$

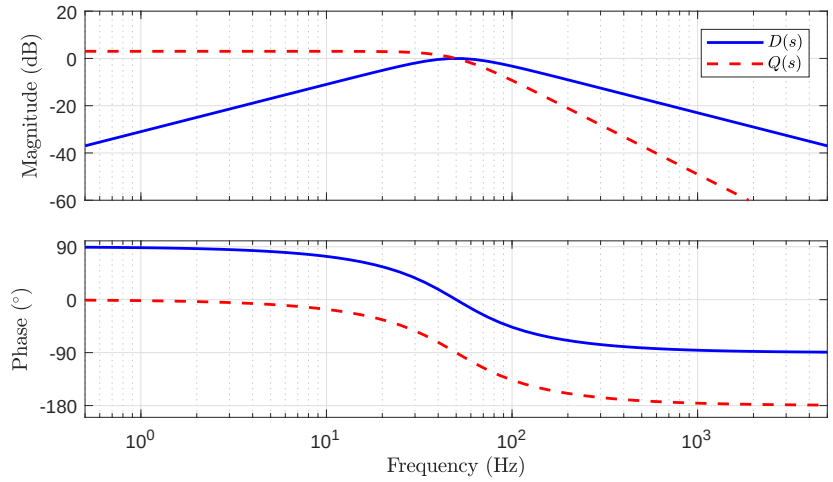


Figure 3. SOGI-QSG bode plot for a centre frequency of 50 Hz and a quality factor $k = \sqrt{2}$.

In Figure 3, it can be noticed that at the center frequency, the gain of both direct $D(s)$ and quadrature $Q(s)$ is unitary, while the phase of $Q(s)$ is lagging 90°. Another interesting feature of this filter, highlighted in [13], is the fact that, independent of the input signal frequency, the output qv' always lags 90° from v'; therefore, when the frequency of the input signal deviates from the center frequency, the filter output signals differ only in magnitude.

The SOGI-QSG, as shown before, allows to filter the input signal with an attenuation of 20 dB/dec and simultaneously generates the direct and quadrature component of the filtered signal. Additionally, it is possible to ensure unitary gain if the filter center frequency is properly adjusted.

3.2. Double SOGI-QSG and Positive Sequence Extraction

The SOGI-QSG can be extended to extract the fundamental frequency of an unbalanced phase system. To achieve it, we consider the symmetrical components method (4) to extract both positive and negative sequences of the unbalance three-phase system. As suggested in [12], the DSOGI consists of two SOGI-QSG (one for each component of the Clarke transform), which allows extracting the positive sequence of the three-phase voltage through the positive sequence calculator (PSC) (5), where qv_α and qv_β are obtained through two different SOGI-QSGs. In Figure 4, it is represented the DSOGI-QSG block diagram.

$$\begin{matrix} v^+_{abc} = T_p v_{abc} \\ v^-_{abc} = T_n v_{abc} \end{matrix}, \quad T_p = \frac{1}{3}\begin{bmatrix} 1 & a & a^2 \\ a^2 & 1 & a \\ a & a^2 & 1 \end{bmatrix}, \quad T_n = \frac{1}{3}\begin{bmatrix} 1 & a^2 & a \\ a & 1 & a^2 \\ a^2 & a & 1 \end{bmatrix}, \quad a = e^{j\frac{2\pi}{3}} \tag{4}$$

$$\begin{aligned} v^+_{\alpha\beta} = [T_{\alpha\beta}]v^+_{abc} = [T_{\alpha\beta}][T_p]v_{abc} = [T_{\alpha\beta}][T_p][T_{\alpha\beta}]^T v_{\alpha\beta} \Leftrightarrow \\ \Leftrightarrow v^+_{\alpha\beta} = \frac{1}{2}\begin{bmatrix} 1 & -q \\ q & 1 \end{bmatrix} v_{\alpha\beta}, \quad q = e^{-j\frac{\pi}{2}} \end{aligned} \tag{5}$$

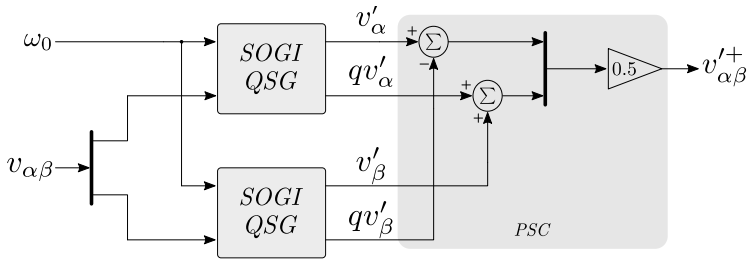


Figure 4. DSOGI-QSG block diagram.

As shown before, it is possible to extract the FFPS of the three-phase voltages represented in the static orthogonal frame (Clarke). Furthermore, the same procedure can be applied to obtain the negative sequence (6), despite its omission in Figure 4. It is worth noting that $v_{\alpha\beta}$ is obtained directly from the three-phase voltage measurement, while ω_0 must be set or estimated in accordance with the grid conditions.

$$v^-_{\alpha\beta} = \frac{1}{2}\begin{bmatrix} 1 & q \\ -q & 1 \end{bmatrix} v_{\alpha\beta} \tag{6}$$

4. DSOGI Based Phase-Locked Loop

In previous sections, it was presented the base of the DSOGI filter and it was shown how it can be used for extraction of the three-phase voltage FFPS.

In the current section, it is discussed two methods for the filter center frequency feedback: the DSOGI-PLL with a low pass filter in the frequency feedback (here simply called DSOGI-PLL) and the frequency-fixed DSOGI-PLL (FFDSOGI-PLL). Both algorithms consist of adding the SRF-PLL to the positive sequence obtained from the DSOGI-QSG, for frequency and phase estimation. The methods differ in how the DSOGI-QSG center frequency is adapted.

4.1. DSOGI-PLL

In the DSOGI-PLL, the estimated frequency of the SRF-PLL is added as a feedback path to the DSOGI filter center frequency. Furthermore, to smooth the frequency feedback from the PLL estimated frequency transients, it is proposed to add a low-pass filter to the frequency feedback path. The estimated frequency is provided by the SRF-PLL as a result of the PI controller keeping the phase angle error to zero. During voltage transients, such as phase jumps, the frequency estimation spikes to bring the phase error back to zero, independent of whether the actual grid frequency changed or not. The added LPF attenuates the interference of such transients as well the normal ripple produced by the PI controller. This scheme is represented in Figure 5, where the SRF-PLL estimated frequency ω'' is filtered by the LPF (ω') before being fed to the DSOGI-QSG. Hence, there are four tunable parameters: DSOGI damping (k), SRF-PLL gains (kp, k_i), and the LPF cut-off frequency (ω_c).

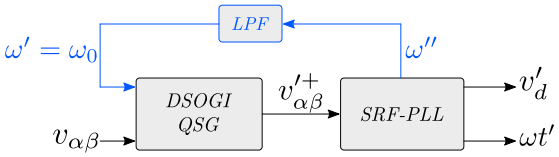


Figure 5. DSOGI-PLL with LPF block diagram.

4.2. FFDSOGI-PLL

A more recent approach, suggested in [19,20], considers a SOGI filter with a fixed center frequency ($\omega_0 = \omega_n$) for single-phase systems (FFSOGI). The method was further extended in [21] to a double SOGI, becoming an FFDSOGI. Contrary to the DSOGI, the FFDSOGI operates with a fixed frequency (there is no frequency feedback path to the SOGIs). Instead, any frequency deviance ($\omega' - \omega_0$) is further compensated in the filter output magnitude and phase. To achieve so, the authors present a linearized small-signal model of the DSOGI filter, considering small deviance $|\omega_0^2 - \omega'^2| << k\omega'\omega_0$. Under these circumstances, deviance can be compensated for by adding a gain correction to the quadrature signal of both $\alpha\beta$ component SOGIs and adding an angle correction to the estimated angle of the SRF-PLL (7). These changes result in the schematic of Figure 6, where grey areas highlight the amplitude and angle compensations. Comparing it with the previous method, the FFDSOGI-PLL has one less tunable parameter (the LPF time constant), as it is suggested to extract the frequency from the PI error integral [19]. Notably, in a steady-state, the error is zero and the frequency is given by the PI error integrative component. Furthermore, without frequency filtering, the estimated frequency oscillations are feed-forward to both frequency and angle compensations. In the paper, it is proposed to filter the estimated frequency as in the case of the DSOGI-PLL before feeding it to the compensation blocks, as shown in Figure 7. The option of adding the LPF, instead of using the PI error integral output, allows decoupling the synchronization dynamics (angle) from the frequency estimation. With this change, the FFSDOGI-PLL and DSOGI-PLL present the same number of tunable parameters, tuned with the same parameters for a fair comparison of both methods.

$$\begin{cases} qv' = \dfrac{\omega'}{\omega_0} qv' \\ \omega t' = \omega t' + \delta \\ \delta = \dfrac{\omega'^2 - \omega_0^2}{k\omega'\omega_0} \end{cases} \tag{7}$$

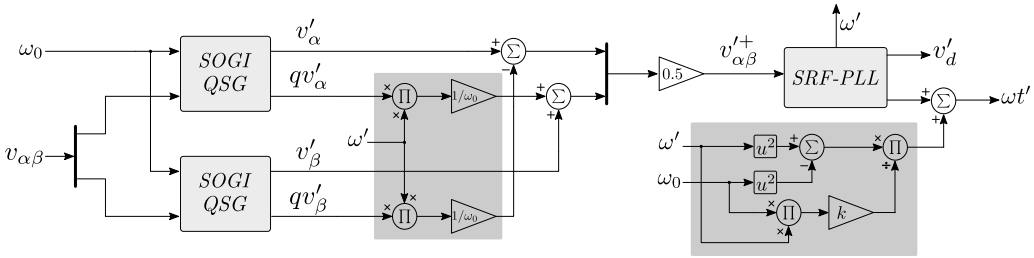


Figure 6. FFDSOGI-PLL block diagram.

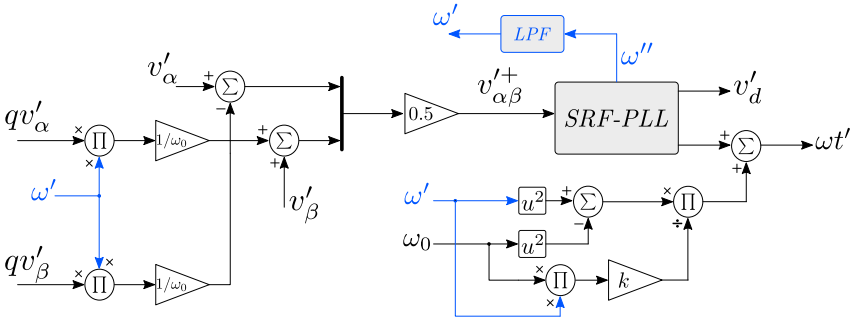


Figure 7. FFDSOGI with frequency LPF.

5. DSOGI Based Frequency-Locked Loop

Another approach to adapt the DSOGI-QSG center frequency ω_0, is proposed and well described in [22]. The author suggests an extension of the EPLL frequency adaptive structure to be applied in the SOGI-QSG. Such modifications result in the block diagram presented in Figure 8, where ω_N is the nominal grid frequency, and the grey area represents the gain normalization GN (9). The input error $\varepsilon_{\alpha\beta}$ is given by (8), considering the SOGI-QSG nomenclature shown in Figure 2). To highlight that the $\sum \varepsilon_{\alpha\beta}$ is negative for $\omega' < \omega$, zero for $\omega' = \omega$ and positive for $\omega' > \omega$. Hence, it is possible to obtain zero steady-state errors ($\omega' = \omega$) with an error integral and gain $-\Gamma$.

$$\begin{cases} \varepsilon_\alpha = (v_\alpha - v'_\alpha) q v_\alpha \\ \varepsilon_\beta = (v_\beta - v'_\beta) q v_\beta \end{cases} \tag{8}$$

$$GN = \frac{k\omega'}{(v'^{+}_\alpha)^2 + (v'^{+}_\beta)^2} \tag{9}$$

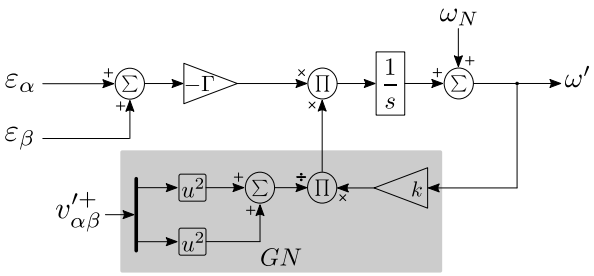


Figure 8. FLL block diagram.

Taking into account the FLL block diagram of Figure 8, it can be noticed that the FLL has only one tuning parameter, Γ, since k is the DSOGI-QSG filter quality factor and ω_N is a known constant. Furthermore, it is shown in [22] that with the gain normalization, the FLL presents a first-order transfer function (10), which allows tuning Γ in accordance with the desired system response settling time t_s.

$$\frac{\omega'}{\omega} = \frac{\Gamma}{s+\Gamma} \Rightarrow \Gamma \approx \frac{5}{t_s} \tag{10}$$

In [23], it is presented an improved frequency locked-loop (IFLL) that differs from the previous FLL, in a slight change on how the gain is normalized. Instead of considering only the positive sequence, the negative sequence is also considered (11). Such modification only improves the method, when the negative sequence becomes significant compared to the positive sequence (very high unbalancing). Another method variation is presented in [24], where a third-order generalized integrator (TOGI) is combined with an FLL for the elimination of the DC component. Such an approach is suited for single-phase systems, where the DC component is not eliminated by the Clarke transform. Additionally, any

SOGI referred on this work can be turned into a TOGI for further implementation in a single-phase system.

The DSOGI-FLL (or the DSOGI-IFLL) has only two tunable parameters: the DSOGI-QSG damping k and the FLL gain Γ.

$$GN = \frac{k\omega'}{(v'^{+}_{\alpha})^2 + (v'^{+}_{\beta})^2 + (v'^{-}_{\alpha})^2 + (v'^{-}_{\beta})^2} \tag{11}$$

To compare the synchronization of both PLL and FLL, it is suggested to add a phase estimation stage to the previously discussed FLL scheme. To achieve so, it is suggested to use the FFPS ($v'^{+}_{\alpha\beta}$) filtered by the DSOGI-FLL to estimate the phase angle. Three different approaches are considered: zero-cross detection, SRF-PLL, and the arc-tangent function. Notice that, contrary to the PLL schemes, in the FLL, both the frequency and phase are tracked independently, despite the phase tracking accuracy being dependent on the FLL performance.

5.1. DSOGI-FLL with Zero-Cross Detection

The zero-cross detection method employed here consists of integrating the frequency estimated by the FLL, but with an angle reset at every zero-cross detected, i.e., when v'^{+}_{α} or v'^{+}_{β} crosses zero, the frequency integral is reset to the known angle. This way, it is possible to correct the estimated phase four times per period. Every time a zero-cross occurs, a flag is triggered ($\delta_{tr,\alpha}$ or $\delta_{tr,\beta}$) and feeds into a lookup table (LUT) to obtain the respective reset angle value accordingly with Table 1. Though it only allows synchronizing during four instants per wave period, this method is simple with a low processing demand, though it may lead to significant phase deviations during transients. This method does not add tunable parameters to the DSOGI-FLL.

Table 1. Zero-cross detection: angle reset LUT.

	$v'^{+}_{\alpha} > v'^{+}_{\beta}$	$v'^{+}_{\alpha} < v'^{+}_{\beta}$
$\delta_{tr,\alpha} > 0$	$\frac{3\pi}{2}$	$\frac{\pi}{2}$
$\delta_{tr,\beta} > 0$	0	π

5.2. DSOGI-FLL with SRF-PLL

The SRF-PLL can be added to the DSOGI-FLL to further estimate the phase frequency. Different from the PLL methods, in the FLL, the PI dynamics of the SRF-PLL do not influence the positive sequence extraction since the center frequency feedback of the DSOGI-FLL does not depend on the PI but on the FLL block diagram instead.

This scheme is here called the DSOGI frequency and phase-locked loop (DSOGI-FPLL). The method adds two tunable parameters to the original DSOGI-FLL (kp and ki), resulting in a total of four tunable parameters.

5.3. DSOGI-FLL with Atan2

The last considered method consists of calculating the arc-tangent of $v'^{+}_{\alpha\beta}$ to obtain the respective angle at any time instant. To reduce the processing burden associated with the typical arc-tangent methods, the fast arc-tangent suggested in [25] is employed. The proposed function is implemented through a LUT (or array) with limited angle representation, i.e., $\omega t' = \arctan(u) \ \wedge u \in [0,1]$ or $\omega t' \in [0, \pi/4]$. To extend its operation for the four quadrants, the functional properties (12) and (13) are considered.

$$\begin{cases} \arctan(-u) = -\arctan(u) \\ \arctan(u) + \arctan\left(\frac{1}{u}\right) = \frac{\pi}{2}, \quad u > 0 \\ \arctan(u) + \arctan\left(\frac{1}{u}\right) = -\frac{\pi}{2}, \quad u < 0 \end{cases} \tag{12}$$

$$\text{atan2}(y,x) = \begin{cases} \arctan(\frac{y}{x}), & x > 0 \\ \pi + \arctan(\frac{y}{x}), & y \geq 0, x < 0 \\ -\pi + \arctan(\frac{y}{x}), & y < 0, x < 0 \\ \frac{\pi}{2}, & y > 0, x = 0 \\ -\frac{\pi}{2}, & y < 0, x = 0 \\ \text{NaN}, & y = 0, x = 0 \end{cases} \tag{13}$$

6. Results and Discussion

To compare the different SOGI-based PLL performance under severe grid conditions of a weak grid, several simulations are performed in Matlab/Simulink. Furthermore, all aforementioned methods were implemented in the discrete-time domain with a sampling rate of 10 kHz to emulate the micro-controller behavior. Discretization was performed considering the forward Euler integration method.

The performed tests are divided into three different subgroups: unbalancing and harmonics (test #1), frequency and phase jumps (test #2), and voltage sags (test #3). However, in the last two, harmonics and unbalancing are also considered but with a smaller impact. In Table 2, it is shown the harmonic content considered in the different tests as a percentage of the FFPS voltage.

The grid voltage is generated directly from pre-defined positive and negative sequences, while harmonics are posteriorly added. Hence, at any instant, it is possible to know the exact frequency, phase, and magnitude of the fundamental positive (and negative) sequence and the harmonics magnitude.

Additionally, it is considered that the PLL is locked when the estimated frequency reaches a steady state. Therefore, if both the FLL and PLL dynamic responses present the same frequency settling time, it is possible to carry a fair comparison between the methods. Hence, PI was tuned (2) considering $\omega_c = 314$ rad/s and $\zeta = 1/\sqrt{2}$, while the FLL gain was tuned (10) with $t_s = 0.1$ s. The SOGI damping, in all different methods, was set as $k = \sqrt{2}$. The tuned gains are summarized in Table 3.

Table 2. Harmonics magnitude (%V^+).

h	Highly Polluted [23] (Test #1)	Limits in EN 50160 [26] (Tests #2 and #3)
5th	20%	6%
7th	15%	5%
11th	10%	3.5%
13th	8%	3%

Table 3. Tuned gains.

k_p	k_i	ω_c	Γ	k
1.37	163	78.5	40	$\sqrt{2}$

6.1. Test #1—Unbalancing and Harmonics

This test considers balanced three phases (positive sequence only) at 50 Hz, with all the methods already in a steady state at the simulation start. Unbalancing is achieved by injecting a negative sequence component, followed by harmonics with an amplitude, as presented in Table 2. Moreover, for the phase estimation, the results in this test are first applied to the FLL (DSOGI-IFLL) and further compared with the PLL (DSOGI-PLL and FFDSOGI-PLL).

The analysis of the three-phase voltages are illustrated in Figure 9, where t_1 to t_4 are the time instants that mark the added changes to the subsequent conditions listed in

Table 4. The estimated frequency ω' and the respective errors ($\omega - \omega'$) are illustrated in Figures 10 and 11, respectively. In Figure 10, it can be noticed that all methods remain near the nominal frequency with the exception of the SRF-PLL. Its performance is significantly poor when facing unbalanced conditions and further deteriorates when high low-order harmonics are present in the three-phase voltage. For these reasons, the following analysis disregards the SRF-PLL and justifies the need for methods capable of extracting the FFPS.

Table 4. Introduced voltage unbalancing and harmonics during test #1.

$t = 0$	Positive sequence only with $v^{+}_{\alpha\beta} = [325\ 0]\ V$ (balanced three phases)
t_1	Negative sequence is added with $v^{-}_{\alpha\beta} = [25\ 12]\ V$
t_2	Injection of the 5th and 7th order harmonics (highly polluted)
t_3	Injection of the 11th and 13th order harmonics (highly polluted)
t_4	Negative sequence is changed to $v^{-}_{\alpha\beta} = [100\ 0]\ V$

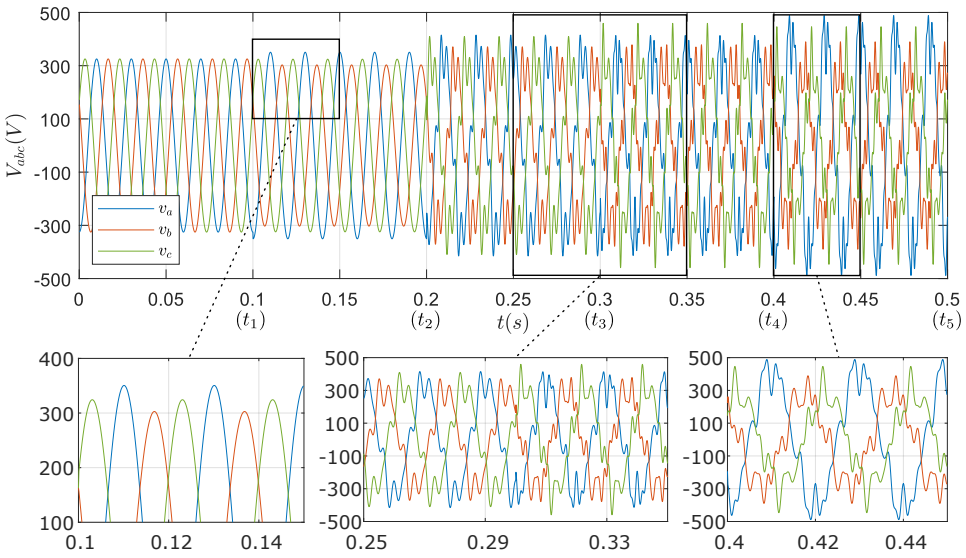


Figure 9. Three-phase voltage and the respective changes introduced during test #1.

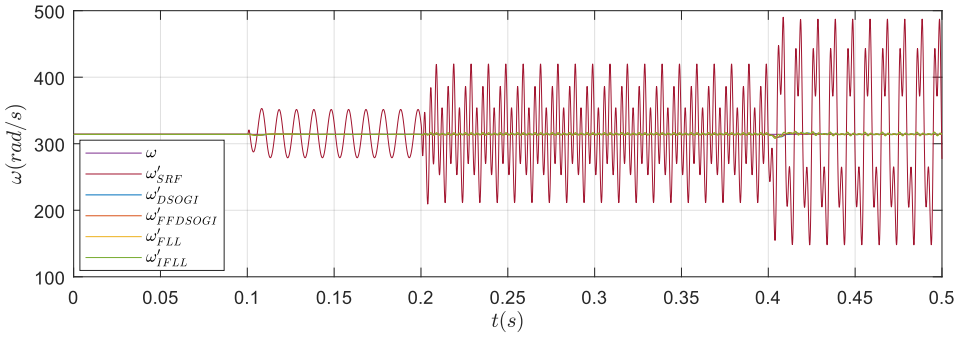


Figure 10. Estimated frequency for the different methods during test #1.

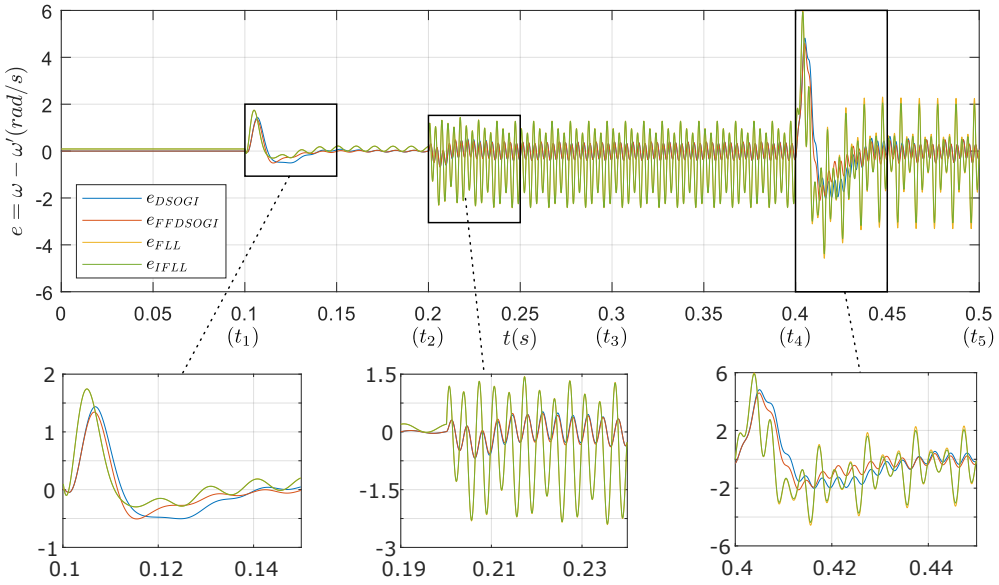


Figure 11. Estimated frequency errors for the different methods during test #1.

In Figure 11 it is noticeable that the DSOGI and FFDSOGI (PLL) presents similar behavior, both with lower estimated frequency steady-state oscillations when compared with the FLL methods. Furthermore, both FLL and IFLL perform very similarly, mostly until t_4, where the negative sequence is reduced. After t_4, unbalancing is more noticeable and the IFLL presents lower oscillations than the FLL, though such a difference may be neglected. To allow a quantification analysis of the results, in Table 5, it is presented the root mean square error (RMSE) as a measure of the error oscillations, and the mean error (ME) as its DC value during steady-state stages. In Table 5, $T_N = 0.02\ s$ and refers to the FFPS voltage waveform time period.

Table 5. Steady-state estimated frequency RMSE and ME obtained during test #1.

	SRF		**DSOGI**		**FFDSOGI**		**FLL**		**IFLL**	
	RMSE	**ME**	**RMSE**	**ME**	**RMSE**	**ME**	**RMSE**	**ME**	**RMSE**	**ME**
$t_1 - 2T_N \Rightarrow t_1$	8.3×10^{-13}	1.8×10^{-9}	1.1×10^{-10}	1.8×10^{-9}	1.2×10^{-10}	1.9×10^{-9}	4.9×10^{-14}	90×10^{-3}	5.2×10^{-14}	90×10^{-3}
$t_2 - 2T_N \Rightarrow t_2$	26	-54×10^{-3}	27×10^{-3}	6.1×10^{-4}	25×10^{-3}	-2.5×10^{-3}	78×10^{-3}	0.10	78×10^{-3}	0.10
$t_3 - 2T_N \Rightarrow t_3$	56	-2.5×10^{-3}	0.26	-7.2×10^{-3}	0.26	-6.5×10^{-3}	1.1	−0.56	1.1	−0.56
$t_4 - 2T_N \Rightarrow t_4$	56	-2.5×10^{-3}	0.26	-7.1×10^{-3}	0.26	-7.2×10^{-3}	1.1	−0.56	1.1	−0.56
$t_5 - 2T_N \Rightarrow t_5$	105	33×10^{-3}	0.27	-9.0×10^{-3}	0.27	-14×10^{-3}	1.3	−0.40	1.2	−0.40

Analyzing data from Table 5, it can be noticed that under ideal conditions $t = [0;\ t_1]$ the FLL and IFLL present a higher steady-state error (ME) when compared with the DSOGI-based PLL structures, though under such conditions, all methods perform very well. With the introduction of the three-phase unbalancing and harmonics, oscillations are more noticeable in the FLL methods than in the PLL. An interesting behavior of the FLL methods is in the change of the steady-state frequency ME with the changes in grid conditions. Observing the integral error of the FLL, it is concluded that the integral error gain is high enough to guarantee zero steady-state error, which indicates that the small ME is caused by the FLL structure, particularly in the way that the error $\varepsilon_{\alpha\beta}$ is generated for adapting the frequency.

Since both the FLL and IFLL performance are similar, only the IFLL is considered in the following performance evaluation.

In Figure 12, it is presented the errors obtained for the phase estimation $\omega t'$. Note that the different methods presented in Section 5 for phase estimation are applied to the IFLL

(FLL is not shown since it presents similar results). Furthermore, the RMSE and ME were obtained under steady-state conditions for the same intervals of Table 5 and are shown in Table 6.

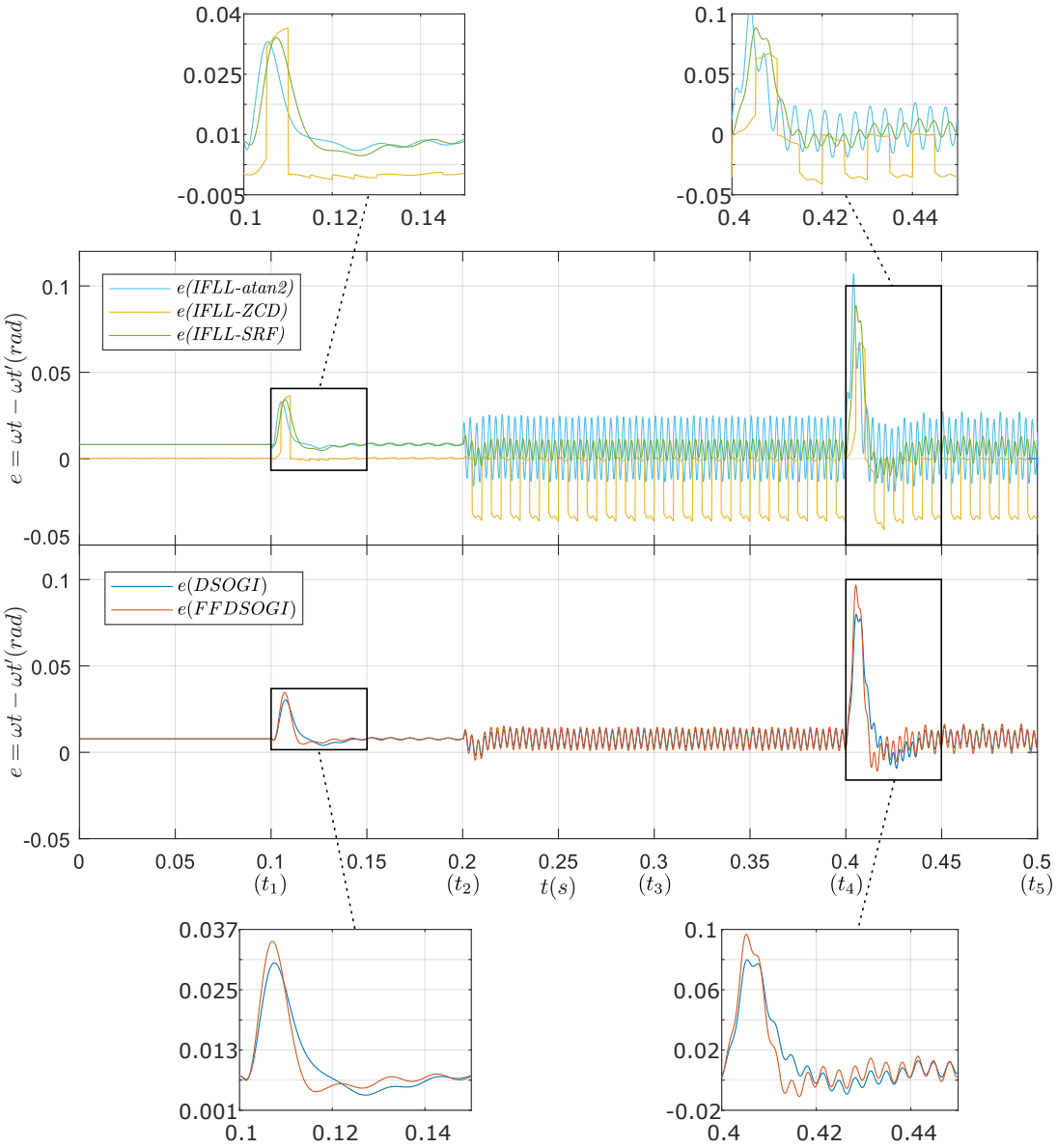


Figure 12. Estimated phase errors for the different methods during test #1. In the top figure, it is shown the different phase estimation methods applied to the IFLL, and in the bottom, the estimated phase by the PLL methods.

Table 6. Steady-state estimated phase angle RMSE and ME obtained during test #1.

	IFLL-Atan2		IFLL-ZCD		IFLL-SRF		DSOGI		FFDSOGI	
	RMSE	**ME**	**RMSE**	**ME**	**RMSE**	**ME**	**RMSE**	**ME**	**RMSE**	**ME**
$t_1 - 2T_N \Rightarrow t_1$	4.4×10^{-6}	8.2×10^{-3}	1.3×10^{-4}	2.3×10^{-4}	8.3×10^{-15}	8.2×10^{-3}	9.0×10^{-13}	7.8×10^{-3}	5.8×10^{-13}	7.8×10^{-3}
$t_2 - 2T_N \Rightarrow t_2$	5.0×10^{-4}	8.2×10^{-3}	2.4×10^{-4}	2.6×10^{-4}	4.6×10^{-4}	8.2×10^{-3}	3.4×10^{-4}	7.8×10^{-3}	4.4×10^{-4}	7.8×10^{-3}
$t_3 - 2T_N \Rightarrow t_3$	13×10^{-3}	5.6×10^{-3}	17×10^{-3}	-18×10^{-3}	4.0×10^{-3}	5.3×10^{-3}	3.3×10^{-3}	7.9×10^{-3}	4.5×10^{-3}	7.8×10^{-3}
$t_4 - 2T_N \Rightarrow t_4$	13×10^{-3}	5.6×10^{-3}	17×10^{-3}	-18×10^{-3}	4.0×10^{-3}	5.3×10^{-3}	3.3×10^{-3}	7.9×10^{-3}	4.5×10^{-3}	7.8×10^{-3}
$t_5 - 2T_N \Rightarrow t_5$	13×10^{-3}	6.1×10^{-3}	17×10^{-3}	-18×10^{-3}	4.2×10^{-3}	5.7×10^{-3}	3.5×10^{-3}	7.9×10^{-3}	4.7×10^{-3}	7.8×10^{-3}

Through analysis of Figure 12, it is clear that the IFLL-SRF results in the most stable angle estimation when compared with the IFLL-atan2 and IFLL-ZCD. Hence, the non-linearity on phase reset at every grid period quarter (IFLL-ZCD) and the high oscillations in the IFLL-atan2 indicate that the $v^{+}_{\alpha\beta}$ components resulting from the DSOGI-FLL are not strictly sinusoidal nor do they present a phase difference of exactly 90°. Such distortions are introduced mostly by the low order harmonics as already concluded before in the frequency analysis. In [7,23], it is suggested to add multiple DSOGIs tuned at different harmonic frequencies for the elimination of the respective low order harmonics; however, such an extension is not explored in this paper.

The PLL methods perform very similarly as expected, though the DSOGI-PLL outperforms all the other methods in terms of overall performance as it can be concluded by analyzing the *RMSE* during steady states, presented in Table 6.

For the test #1 conditions, it can be concluded that the performance of both PLL methods is superior to the FLL. Where the FFDSOGI presents the best results in frequency estimation and the DSOGI in the phase angle, both perform very similarly in both estimations. Despite the differences, as far as harmonics and unbalancing conditions are considered, all methods based in the SOGI-QSG show great performance under unbalancing conditions and good harmonics filtering capability.

To qualify the obtained results for the different methods during test #1, it is considered only the steady-state oscillations (RMSE). During test #1, the ME remains practically constant for both frequency and phase estimations, making it more meaningful to analyze the ME with the results obtained during test #2. Furthermore, the RMSE is applied to the frequency estimation since in the case of the phase angle estimation, the differences can be disregarded. The final classification is shown later in Table 12, where the mark is defined by the averaged ratio of the method RMSE by the minimum RMSE obtained for the different grid distortion intervals.

6.2. Test #2*—Frequency Steps and Phase Jump*

Test #2 consists of applying frequency steps followed by a phase jump. The test, as already stated before, also considers unbalancing and low-order harmonics in accordance with Table 2. The frequency and phase profile is equally applied to the three phases and is summarized in Table 7.

Table 7. Frequency steps and phase jump applied during test #2.

$t = 0$	Nominal frequency of 50 Hz
t_1	Frequency step change to 55 Hz
t_2	Frequency step change to 45 Hz
t_3	Frequency step change back to 50 Hz
t_4	Phase jump of $\pi/4$ rad

The results obtained for the estimated frequency and respective frequency errors during test #2 are shown in Figure 13.

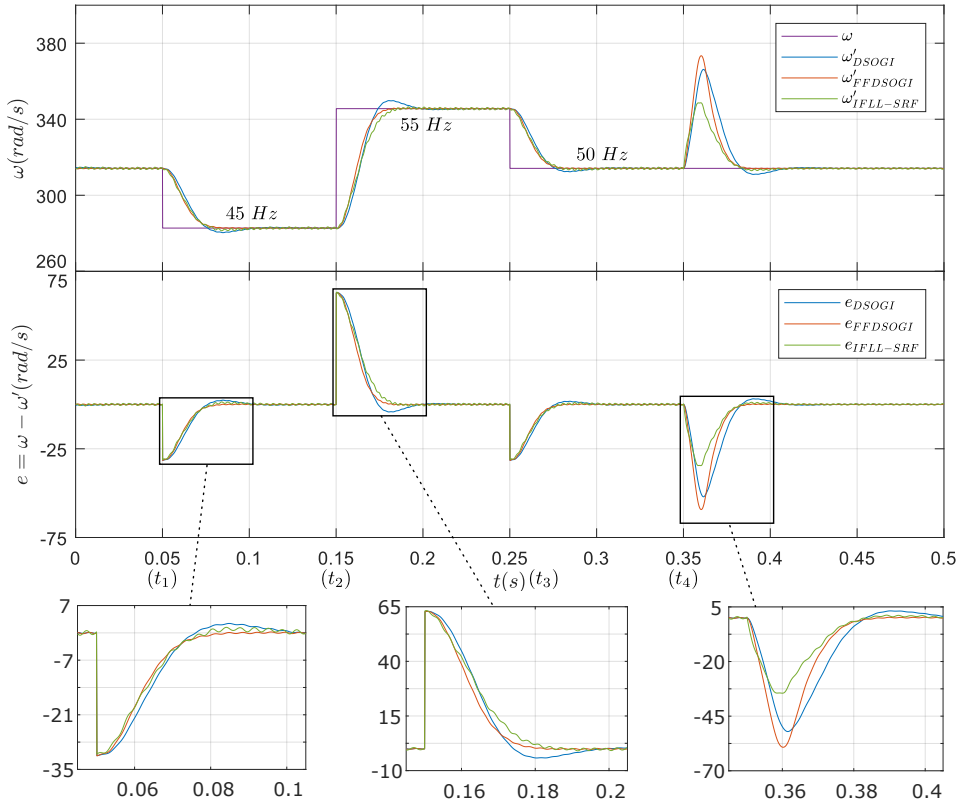


Figure 13. Estimated frequency errors for the different methods during test #2.

In Figure 13, the steady state of the different methods is coherent with the results obtained during test #1, and, therefore, it is not analyzed again. The frequency steps at (t_1) and (t_3) are the same ($\Delta\omega$ = 5 Hz), and it can be seen that the transient response of the FFDSOGI and IFLL are very similar, both in terms of overshoot and settling time. During this step, the DSOGI takes almost 20 ms more to reach the steady state. At (t_2) occurs the biggest frequency step ($\Delta\omega$ = 10 Hz) and during this transient, the FFDSOGI presents a slightly faster response. Finally, at (t_4) occurs the 45° phase shift, and the results, in terms of the response time, follow the same behavior as during (t_1). Nevertheless, the IFLL presents significantly less overshoot than other methods, which indicates that the FLL scheme is less sensitive to phase jumps when compared with the PLL.

To evaluate the performance in terms of phase estimation, the results in Figure 14 are presented. In terms of phase estimation, during frequency step changes, the differences are more obvious, where the FFDSOGI performance is better than the others, both in terms of overshoot and settling time. The FFDSOGI reaches its steady state in $\approx$ 0.03 s, with the following taking 0.02 s more. Still, during the phase jump, the FLL presents less overshoot and takes the same time to reach the steady state, which corroborates the estimated frequency results.

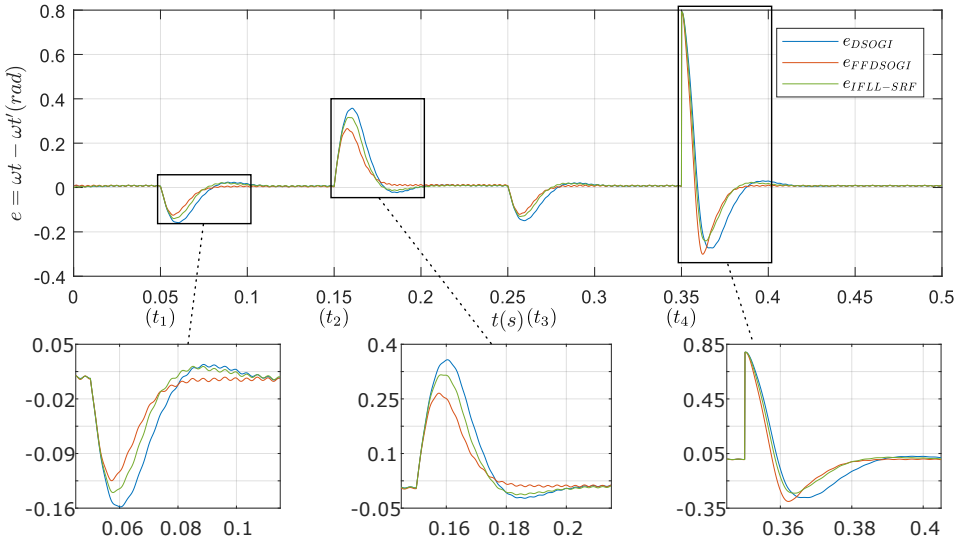


Figure 14. Estimated phase errors for the different methods during test #2.

In Tables 8 and 9, the results are summarized for the methods that presented the best performance during test #2. In Table 8, *OS* is the overshoot and t_s the settling time. In Table 9, it is shown the ME for estimation of the steady-state frequency and phase at different grid frequencies.

Table 8. Results summary obtained for test #2—overshoot (*OS*) and settling time (t_s).

		DSOGI			**FFDSOGI**			**IFLL**		
		$\Delta\omega =$ 5 Hz	**$\Delta\omega =$ 10 Hz**	**$\Delta\omega t = \pi/4$**	**$\Delta\omega =$ 5 Hz**	**$\Delta\omega =$ 10 Hz**	**$\Delta\omega t = \pi/4$**	**$\Delta\omega =$ 5 Hz**	**$\Delta\omega =$ 10 Hz**	**$\Delta\omega t = \pi/4$**
ω'	t_s (ms)	45.0	45.0	45.0	30.0	30.0	30.0	30.0	33.0	33.0
	OS (rad/s)	31.4	62.8	52.0	31.4	62.8	59.0	31.4	62.8	34.0
$\omega t'$	t_s (ms)	60.0	60.0	65.0	38.0	38.0	40.0	60.0	60.0	65.0
	OS (rad)	0.16	0.36	0.79	0.13	0.27	0.79	0.14	0.32	0.79

Table 9. Results summary obtained for test #2—steady state ME.

		DSOGI			**FFDSOGI**			**IFLL**		
		$\omega =$ 45 Hz	**$\omega =$ 55 Hz**	**$\omega =$ 50 Hz**	**$\omega =$ 45 Hz**	**$\omega =$ 55 Hz**	**$\omega =$ 50 Hz**	**$\omega =$ 45 Hz**	**$\omega =$ 55 Hz**	**$\omega =$ 50 Hz**
ω'	*ME* (rad/s)	4.8 m	25 m	0.3 m	14 m	6.4 m	0.9 m	22 m	46 m	46 m
$\omega t'$	*ME* (rad/s)	6.8 m	8.4 m	7.8 m	5.0 m	11 m	7.8 m	6.9 m	8.8 m	8.0 m

Based on the results summarized in Tables 8 and 9, the final classification is presented later in Table 12. The classification is based in the average ratio of each evaluated value with the minimum value obtained during that test for the different conditions. Hence, the best result corresponds to the smaller classification value 1.0.

6.3. Test #3—Voltage Sags

During test #3 the grid frequency is kept constant (nominal value), while harmonics and unbalancing are the same as those applied in test #2 (Tables 2 and 4). Hence, the

changes applied during the present test focus on the voltage amplitude, i.e., the sags are applied to the symmetrical voltage components and also the harmonics.

The voltage sags periods and amplitudes are summarized in Table 10 and the resulting grid voltage waveforms are shown in Figure 15.

Table 10. Voltage sags applied during test #3.

$t = 0$	No voltage sag
t_1	Voltage sag of 30% with 75 *ms* duration
t_2	Voltage sag of 60% with 150 *ms* duration
t_3	Voltage sag of 90% (permanent)

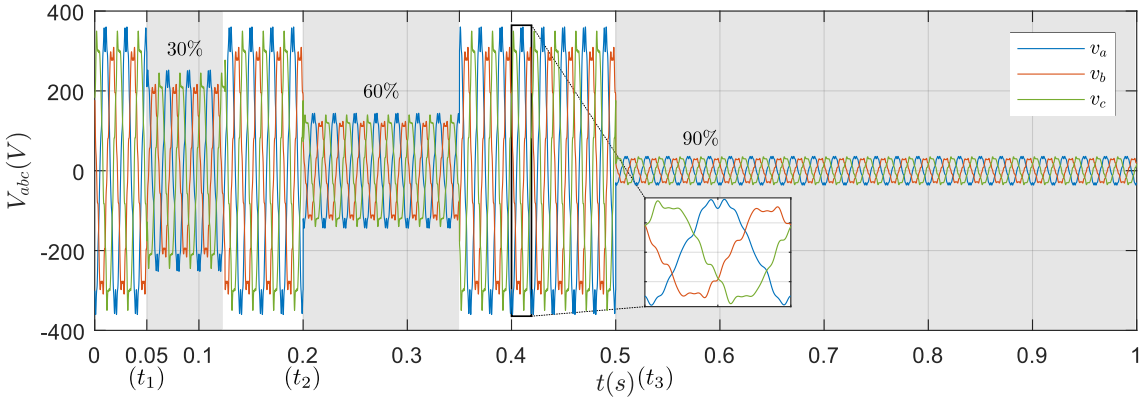


Figure 15. Voltage sags applied during test #3.

The errors associated with frequency and phase estimations, obtained during test #3, are shown in Figure 16, where the top plots refer to the frequency and the bottom ones to the phase.

Analyzing the frequency dynamic response of Figure 16 allows concluding that all methods respond very similarly to the 30% voltage sag (t_1). During the 60% voltage sag (at t_2), both FFDSOGI and IFLL-SRF also perform with the same settling time, despite the first response with larger oscillations. In the same interval, it is noticeable the weaker performance of the DSOGI, which takes ≈20 ms more to reach a steady state. The 90% voltage sag is the perturbation with a higher impact of all the analyzed tests, where it can be seen the long settling time of both FFDSOGI and DSOGI, with both taking, respectively, 200 ms and 350 ms to reach a steady state. On the other hand, the IFLL-SRF presents a significantly faster response time, taking 100 ms to reach the steady state.

In terms of phase dynamic response, the results are coherent with the aforementioned comments for the estimated frequency. The only exception is during (t_3), where the IFLL-SRF presents a phase response, similar to the FFDSOGI, of ≈200 ms.

The summary of the voltage sag results is presented in Table 11, where the steady-state ME is not shown since it remains approximately constant for all methods.

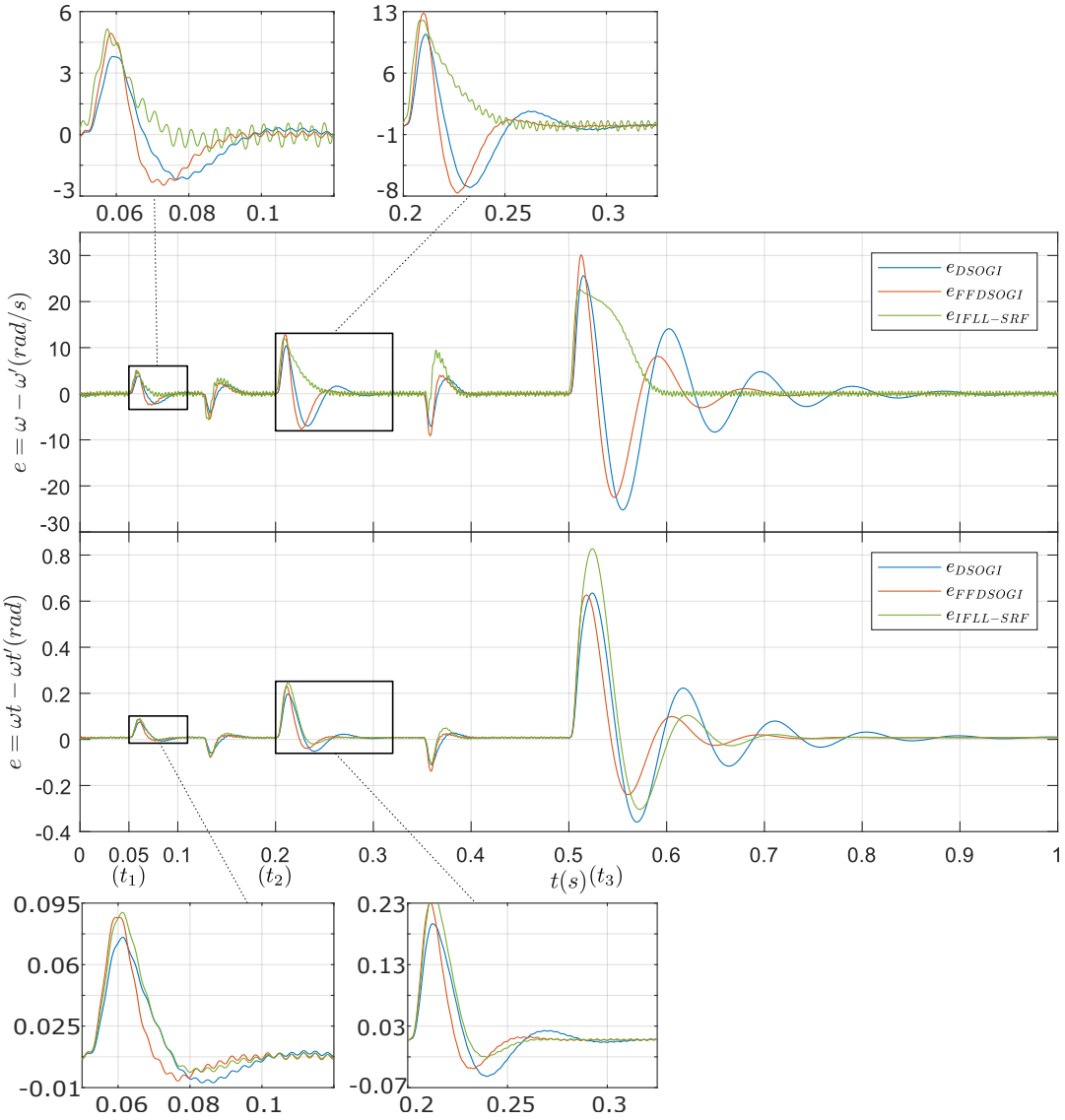


Figure 16. Estimated frequency and phase errors for the different methods during test #3.

Table 11. Results summary obtained for test #3- voltage sags.

		DSOGI			FFDSOGI			IFLL		
		***VS* = 30%**	***VS* = 60%**	***VS* = 90%**	***VS* = 30%**	***VS* = 60%**	***VS* = 90%**	***VS* = 30%**	***VS* = 60%**	***VS* = 90%**
ω'	t_s (ms)	42.0	70.0	360	38.0	60.0	160	38.0	60.0	90.0
	OS (rad/s)	3.81	10.4	25.6	4.94	12.8	30.1	5.15	12.0	22.6
$\omega t'$	t_s (ms)	51.0	113	500	41.0	75.0	280	48.0	75.0	280
	OS (rad)	0.061	0.200	0.635	0.087	0.230	0.627	0.090	0.240	0.827

6.4. Tests Benchmark

Taking into account Tables 5, 8, 9 and 11, classification Table 12 is presented. For classification purposes, the marks were calculated by considering the ratio of the averaged registered values (per method of each test transition) by the minimum average obtained from all tests for each test transition. Therefore, the best result (minimum value) for each test/transition is 1.0 and the choice of the suitable method should be based on the

minimum classification value obtained. The table classifications are divided into two categories (frequency and phase), where for each category, the methods are classified in terms of the steady-state performance *SS* (RMSE or ME), dynamic response to frequency step changes $\Delta\omega$, phase jumps (*p.j.*), and voltage sags *VS* (evaluating both the overshoot and settling time). It can be noticed that the steady state is based only on the average of the RMSE for the frequency and the average of the ME for the phase angle estimations (both from test #1). The choice of the steady-state error indicators was based on its significance, i.e., the RMSE in the case of the frequency, and ME in the phase estimation.

Table 12. Classification table of the methods' performance during different tests.

			DSOGI	***FFDSOGI***	***IFLL***	***Description***
ω	*RMSE*		1.0	1.0	4.3	Steady-state frequency oscillations—test #1
	$\Delta\omega$	*OS*	1.0	1.0	1.0	Overshoot during frequency step—test #2
		t_s	1.9	1.0	1.6	Settling time during frequency step—test #2
	p.j.	*OS*	1.5	1.7	1.0	Overshoot during phase jump—test #2
		t_s	2.0	1.0	1.7	Settling time during phase jump—test #2
	VS	*OS*	1.0	1.3	1.2	Overshoot during voltage sag—test #3
		t_s	2.1	1.3	1.0	Settling time during voltage sag—test #3
ωt	*ME*		1.0	3.9 *	1.2	Steady-state phase deviance—test #2
	$\Delta\omega$	*OS*	1.3	1.0	1.2	Overshoot during frequency step—test #2
		t_s	1.6	1.0	1.6	Settling time during frequency step—test #2
	p.j.	*OS*	1.0	1.0	1.0	Overshoot during phase jump—test #2
		t_s	1.6	1.0	1.6	Settling time during phase jump—test #2
	VS	*OS*	1.0	1.2	1.3	Overshoot during voltage sag—test #3
		t_s	1.5	1.0	1.1	Settling time during voltage sag—test #3
MCU execution time			1.0	1.0	1.3	MCU processing time— experimental result

* for operation frequency of $\omega = \omega_n \pm 5\%$, consider 1.3 for the FFDSOGI.

For the grid-following operation with the main grid (strong grid) sudden changes are not expected, such as voltage sags or frequency steps, since the grid voltage transients are slow and smooth when compared with the converter and PLL dynamics. Hence, in this case, it is recommended to consider the steady-state phase and frequency estimation (RMSE and ME) and the MCU burden as the selection criteria. In such conditions, the DSOGI-PLL is the best choice by a marginal difference when compared with the FFDSOGI (selection based on the method simplicity and MCU execution time of Figure 23). The IFLL is only recommended if fast-tracking of frequency is important during voltage sags or phase jumps, where mostly because of its gain normalization, a smoother and faster response is achieved when compared with the other methods but at the cost of a higher MCU burden. Such a requirement can be considered in power converters operating with reactive power compensation in inductive weak grids. The FFDSOGI outperforms the other methods in the overall results of the test, making it the most suitable choice when uncertain conditions are expected. The only constraint with high impact in its selection is related to the grid frequency variation, which must be small ($\omega_n \pm 5\%$).

Through the presented classification table, it is possible to apply weights to the different marks and select the best method based on the minimum value obtained.

As an example, in this paper, the choice of a PLL to be applied on a power converter control loop is considered, operating in a low-voltage microgrid as described in [27]. In such conditions, the grid can be either weak (island) or strong (grid connected). In the grid connected (strong grid) condition, the most important requirements are as discussed in the previous paragraph. When operating in island mode (weak grid), the lack of inertia may result in the occurrence of any of the earlier mentioned perturbations. Since the phase

angle estimation is the crucial variable of interest, in the operation of the power converter, the following weights (applied to each component in parenthesis) are suggested:

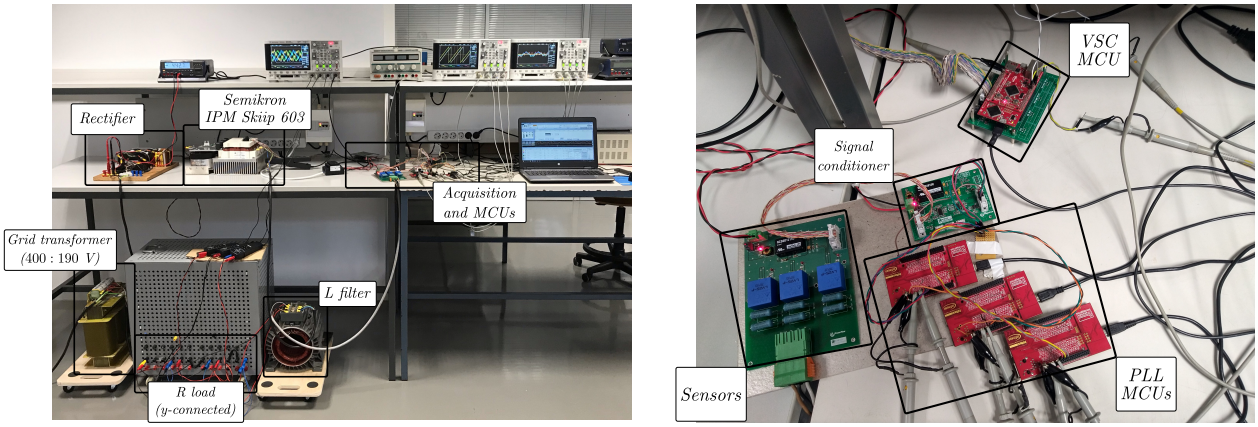
- Phase angle steady-state estimation is of high importance since controllers are designed to operate in the SRF (25%);
- Frequency should be according to EN 50438, i.e., deviance inside the limit $\omega_n \pm 3\%$;
- Phase jumps may occur during re-connection with the main grid (25%);
- Voltage sags may occur during overload conditions or heavy-load connection (25%);
- Low MCU processor burden (25%).

Following the marks and listed criteria in Table 12, the best choice is FFDSOGI-PLL (1.03 pts), followed by DSOGI (1.25 pts), and IFLL (1.30 pts).

6.5. Experimental Results

To evaluate and confirm the synchronistic performance of the methods discussed in the previous section, a voltage source converter (VSC) is configured to generate a local grid voltage (instead of a DAC board) so that the switching EMI can be present in the measurements. The VSC operates in an open-loop as a programmable voltage source with a filter inductance supplying a resistive load that is y-connected. Hence, it is possible to generate any three-phase voltage through VSC modulation signal manipulation.

Additionally, voltage measurements are taken at filter output; therefore, the modulation phase angle leads the measured phase voltage, due to the load angle. As a consequence, the estimated phase angle presents a DC error resulting from the load angle when the modulation phase angle is taken as reference. The resulting setup is presented in Figure 17. The harmonics injected in the modulation are also adjusted so that the voltage, measured at inductance output, contains the harmonics as indicated in Table 2.



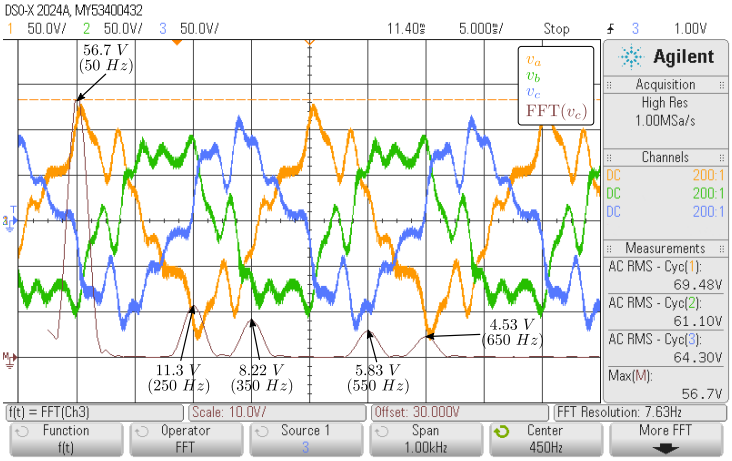
(**a**) (**b**)

Figure 17. Laboratory setup for three-phase voltage generation and evaluation of the PLL's performance. (**a**) shows the full setup and (**b**) the acquisition board, conditioning board, and MCUs.

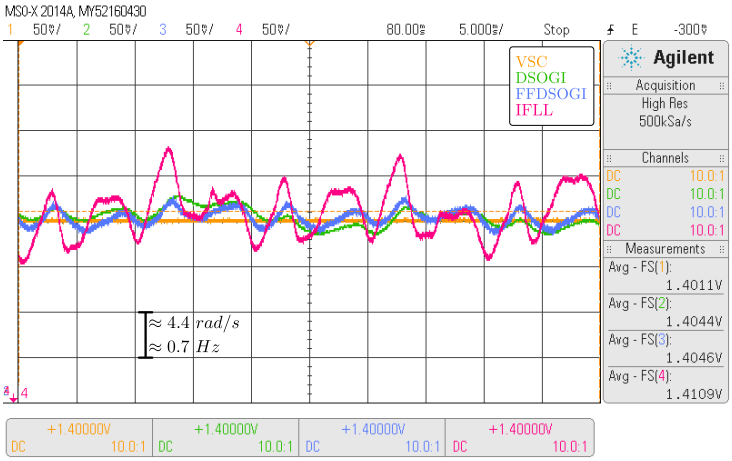
For evaluation of the methods, three identical MCUs (Infineon XMC 4500) were programmed, each with a different method. The sensed three-phase voltage was fed into each of the MCU boards and the two DACs available per board were tuned for further evaluation of the results. The PLL MCU DACs generated signals according to the estimated frequency and phase angle of each method and were compared with the VSC MCU modulation frequency and phase. The generated voltages were limited below 70 V_{rms}, though MCU readings were amplified by a factor of 3 so that the measured voltage approached near nominal grid conditions. Notably, the presented setup does not allow to apply steps as applied during the simulation, due to the RL time constant.

In Figure 18 are shown the results obtained for test #1 considering conditions similar to t_3 of Table 4. In the figure, it is shown the voltage waveforms at filter inductance output

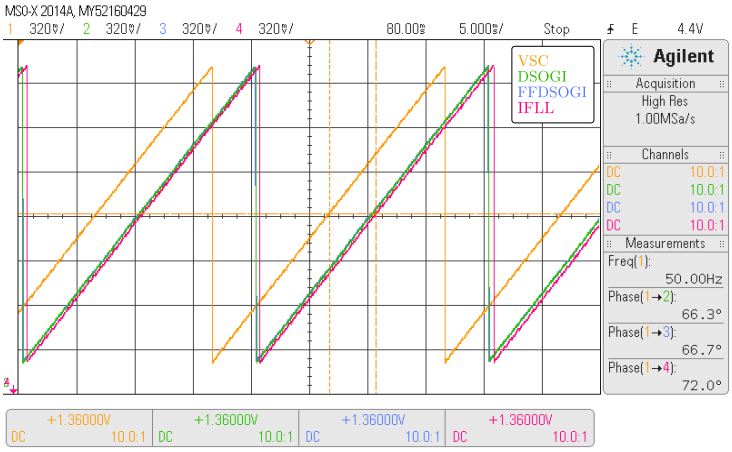
with unbalanced phase voltages and harmonic content, measured through the oscilloscope FFT function.



(**a**)



(**b**)



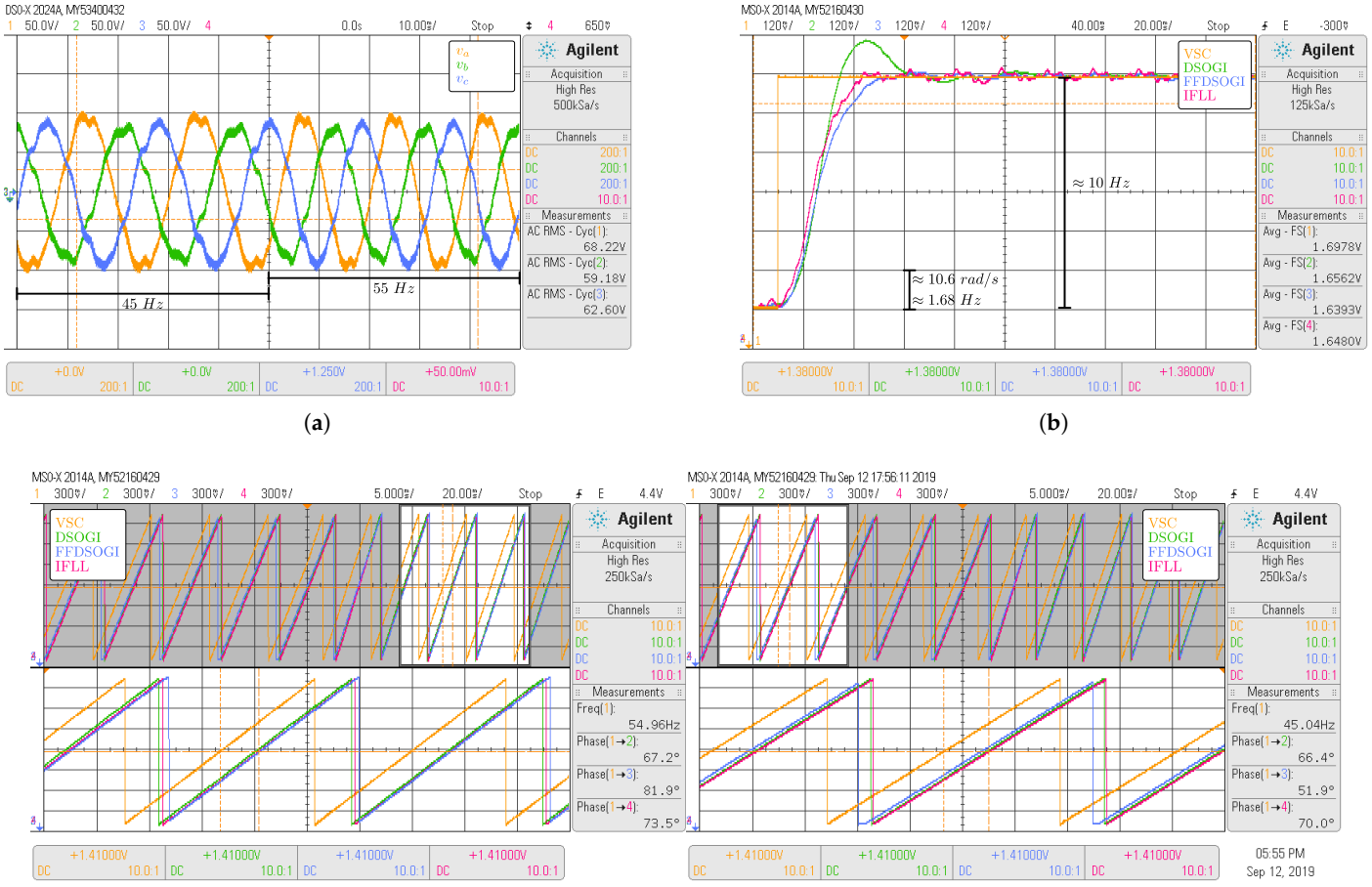
(**c**)

Figure 18. Experimental results for test #1. (**a**) Measured voltages with the FFT of phase v_c, (**b**) estimated frequency and (**c**) estimated phase angle.

Analysis of the results obtained for test #1 allows concluding that, as discussed in Section 6.1, the DSOGI and FFDSOGI methods perform very similarly in terms of

frequency estimation. The IFLL presents higher oscillations than the other two, though such differences are not as noticeable in practice as the ones obtained during simulation. The phase estimation of the IFLL presents a higher ME (DC error) than the other methods, as also discussed in Section 6.1. Despite not being noticeable in Figure 18, the steady-state phase estimation oscillations are identical in all three methods. Such a fact was concluded by monitoring the PI outputs of all methods.

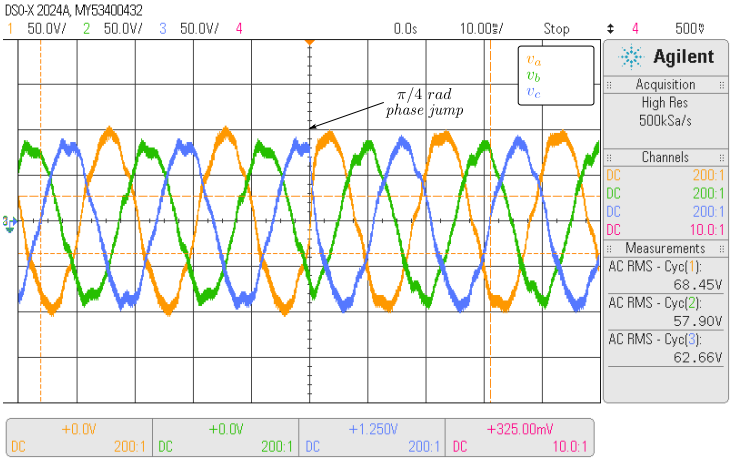
For test #2, it was applied a frequency step ($45 \rightarrow 55\ Hz$), as shown in Figure 19, and a phase jump of 45° at nominal frequency (Figure 20). Additionally it is shown in Figure 21 the estimated angle in a steady state for both limit frequencies.



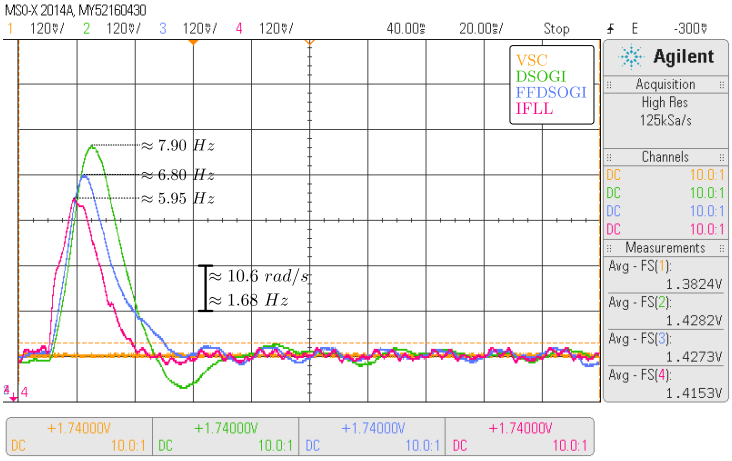
(**a**) (**b**)

(**c**)

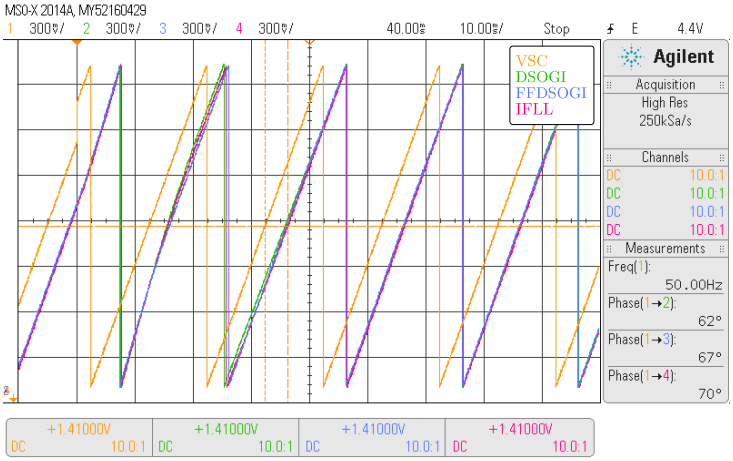
Figure 19. Experimental results for test #2 frequency step. (**a**) Measured voltages, (**b**) estimated frequency, and (**c**) estimated phase angle.



(**a**)

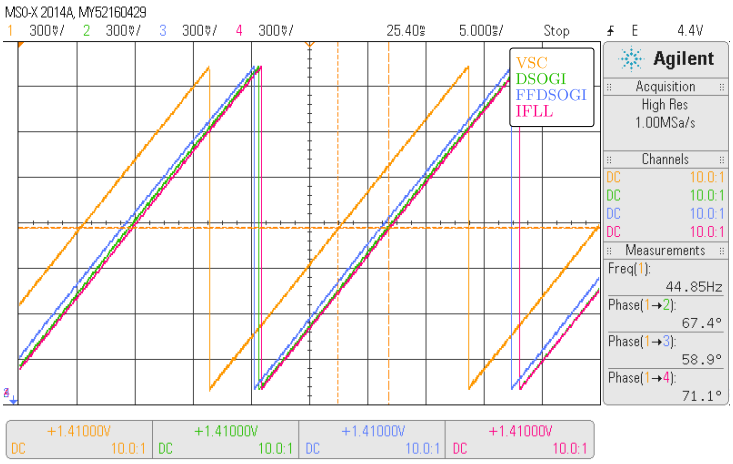


(**b**)

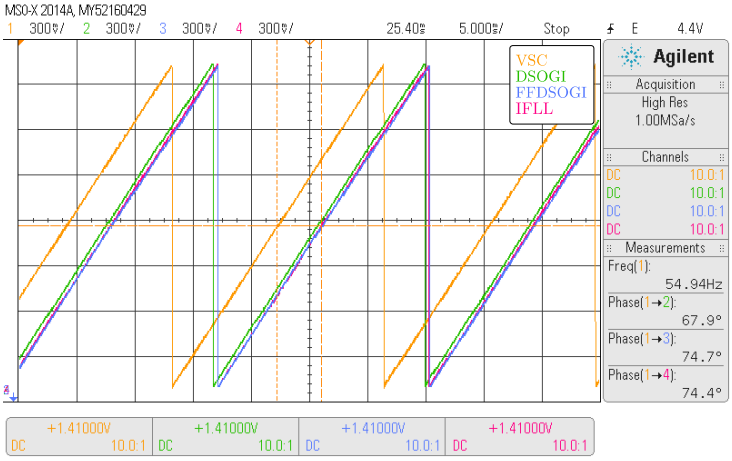


(**c**)

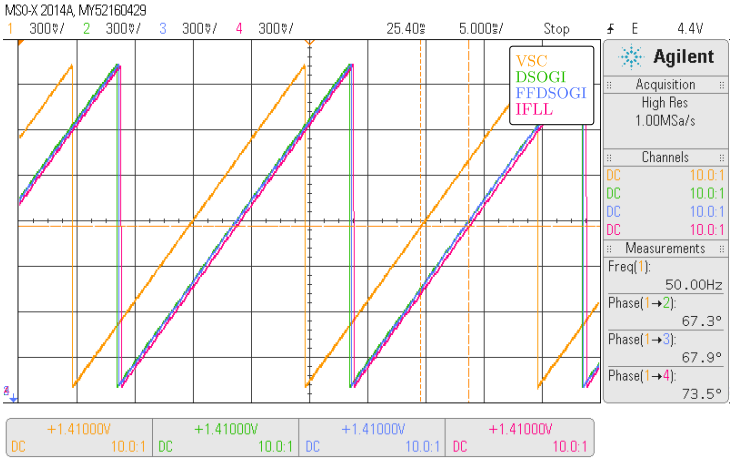
Figure 20. Experimental results for test #2 phase jump. (**a**) Measured voltages, (**b**) estimated frequency, and (**c**) estimated phase angle.



(**a**)



(**b**)



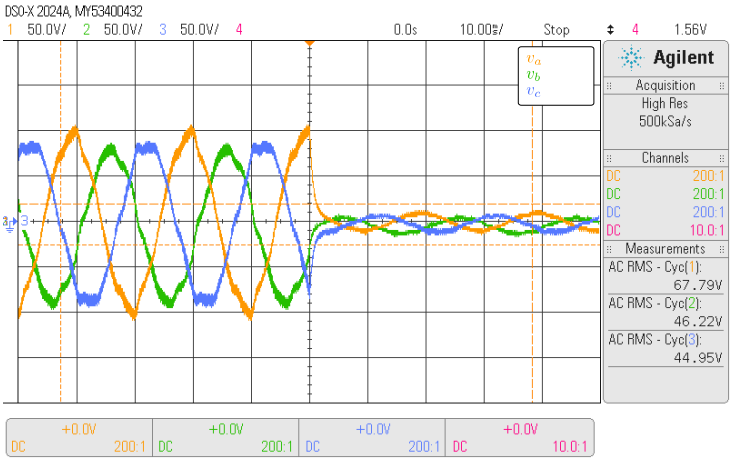
(**c**)

Figure 21. Steady state angle estimation for different frequencies. (**a**) 45 Hz, (**b**) 50 Hz and (**c**) 55 Hz.

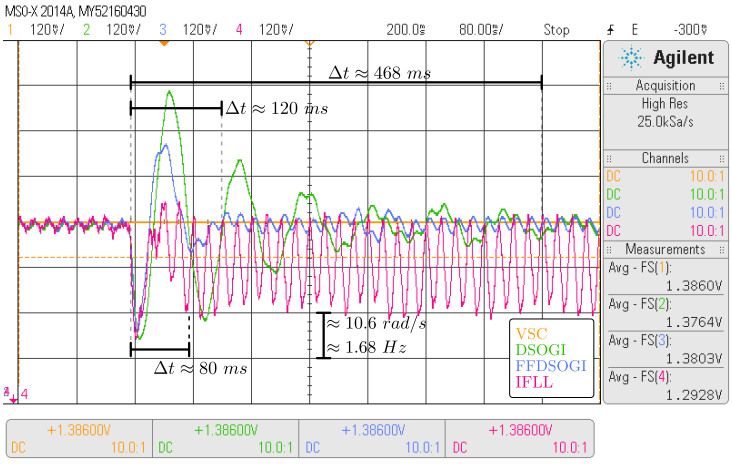
The obtained results agree with the discussion in Section 6.2. The estimated frequency of both tests (Figures 19 and 20) follows the results already discussed. The only exception is for the phase estimation by the FFDSOGI during limit frequencies, i.e., there is a DC error of the phase estimation that changes depending on the frequency. Such behavior is justified by the method linearization for the phase estimation and can be visualized in Figure 21 by checking the change in the phase difference between the modulation phase

angle (VSC) and the FFDSOGI.

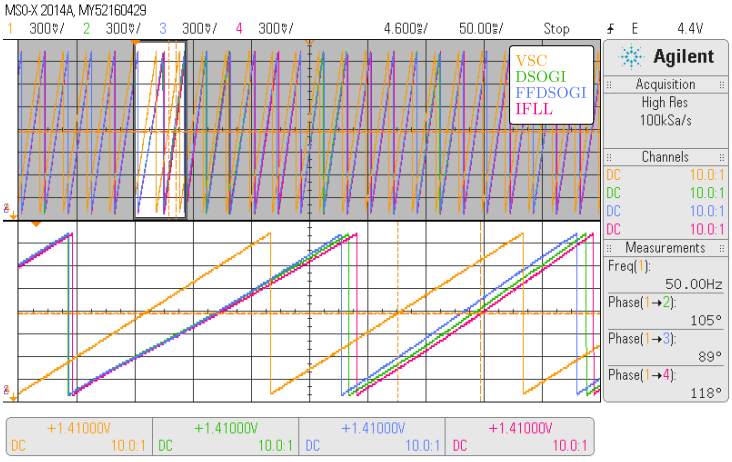
For the voltage sag of test #3, a 90% sag is applied since it corresponds to the simulated worst case, and the respective obtained results are presented in Figure 22.



(**a**)



(**b**)



(**c**)

Figure 22. Experimental results for test #3. (**a**) Measured voltages, (**b**) estimated frequency and (**c**) estimated phase angle.

From Figure 22, it can be noticed that the IFLL is the method that responds faster,

although it presents significantly higher steady-state oscillations and a change in the average frequency estimation value. The FFDSOGI takes 1.5× more than the IFLL to reach a steady state, though it presents significantly fewer oscillations and the steady-state average error can be neglected. The DSOGI behavior follows the FFDSOGI one with the difference of taking longer, by 4×, to reach a steady state.

The last test is related to the MCU processing times and it is shown in Figure 23. In the figure, it is shown the execution times of each method, i.e., the pulse width of each square wave represents the execution time of the algorithm, including the ADCs acquisition time.

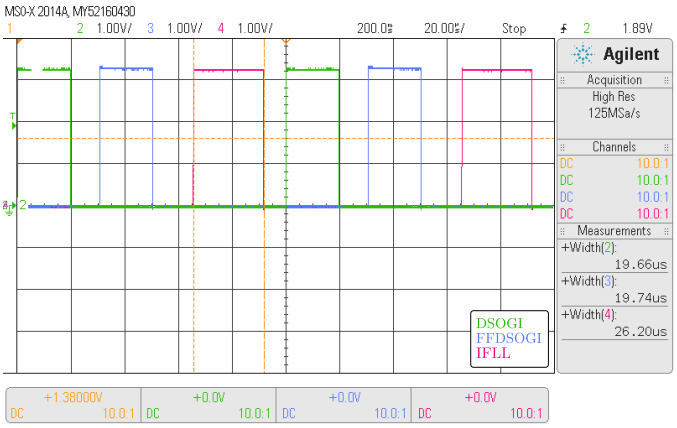


Figure 23. Algorithms process time, including ADCs acquisition time.

7. Conclusions

In the paper, different DSOGI PLL implementations for grid synchronization in weak grids were analyzed. Based on the obtained simulation and experimental results it is possible to conclude that all the DSOGI-based PLL allow to track the three-phase voltage amplitude, frequency, and phase, but show different dynamic and steady-state responses. Based on such results, a benchmark table is presented.

The benchmark table aims to ease the DSOGI-based PLL selection, considering the performance of each implementation for different grid conditions, or events such as low-order harmonics, unbalanced phases, voltage sags, and frequency or phase-step changes. Through the selection of expected individual expected disturbances, it was possible to identify particular scenarios that would result in the choice of each method. The DSOGI is suitable for connection with strong grids, the IFLL in applications where it is required a fast-tracking of the grid frequency during voltage sags or phase jumps, and the FFDSOGI is the most suitable when the phase and/or frequency estimation is required and any of the disturbances can be expected, as far as the grid frequency variations are within the interval of $\omega_n \pm 5\%$.

Criteria based on expected weak-grid disturbances were applied, resulting in the choice of a suitable DSOGI implementation. Therefore, the FFDSOGI-PLL is adopted as the most performant, according to the requirements within the scope of a weak grid.

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Abbreviations

The following abbreviations are used in this manuscript:

ADC	Analog to digital converter
DSOGI	Double second-order generalized integrator
FFPS	Fundamental frequency positive sequence
FFDSOGI	Frequency-fixed double second-order generalized integrator
FLL	Frequency-locked loop
MCU	Micro-controller unit
ME	Mean error
PLL	Phase-locked loop
RMSE	Root-mean-square error
SOGI	Second-order generalized integrator
TOGI	Third-order generalized integrator

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