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Power Sharing for a Multi-Source Low-Voltage Urban Microgrid

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Resumo

O aumento da geração local proveniente de energias renováveis assim como do número de cargas pesadas na rede de distribuição, como é o caso dos carregadores de veículos elétricos, apresentam vários problemas com impacto direto na estabilidade da rede. Uma possível resposta para resolver alguns desses problemas passa pelo conceito de micro-rede, onde a rede é subdividida em várias sub-redes com os seus próprios sistemas de gestão de balanceamento de potência e energia. A micro-rede pode operar conectada ou desconectada da rede principal, sendo necessário garantir de forma dinâmica o balanceamento local entre a potência da geração e da carga. Adicionalmente, considerando um sistema com várias unidades de produção, é também necessário garantir equidade na participação de potência de cada unidade. Os conversores de potência são essenciais para alcançar tais objetivos, sendo necessário que os mesmos apresentem uma operação flexível e expansível. Na tese é explorado um cenário de micro-rede durante a operação em modo isolado com múltiplas fontes, que integram sistemas de armazenamento de energia, que partilham potência com múltiplas fontes. Tal cenário é representativo de uma rede citadina num futuro próximo. A tese apresenta e discute o projeto de aspetos críticos no conversor de potência, que incluem o sincronismo com a rede, o filtro de c.a., e o projeto das principais malhas de controlo do conversor. É também apresentada uma solução baseada no controlo local (descentralizado) que permite a operação estável da micro-rede em termos de balanceamento e participação de potência. Tal solução permite ainda garantir o balanceamento do estado de carga (SoC) das unidades de armazenamento de energia elétrica conectadas na micro-rede, permitindo maximizar a disponibilidade local de potência. Os métodos de controlo investigados são validados por meio dos resultados obtidos por simulação e experimentalmente.

Abstract

The growth of local renewable energy sources and heavy loads in the power distribution networks, such as the increasing electric vehicle charging stations, causes several issues with a direct impact on the stability of the electrical grid. A possible solution to overcome such issues is the microgrid concept, with the grid structured into local sub-grids that manage their power and energy balancing. A microgrid may operate connected or disconnected from the main-grid being dynamically necessary to guarantee a power balancing between local sources and loads. Furthermore, as several power units are connected to the same microgrid, it is also required equity in terms of power-sharing. The power converters are crucial to achieving such targets requiring to present flexible and expandable operation. In the thesis it is explored a scenario of an island operation of a microgrid with multiple sources, including energy storage systems, sharing power with multiple loads. Such a scenario is representative of a city grid in the near future. The thesis presents and discusses the design of critical aspects of the power converter, which includes the synchronism with the grid, AC filter, and converter inner loop controllers design. A local control solution (decentralized) for a stable operation of the microgrid in terms of both power balancing and power-sharing is also presented. Such approach also ensures balanced state of charge (SoC) of the connected electric storage systems allowing to maximize the local power availability. The researched control methods are validated through simulation and experimental results.

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Acronyms

Acronyms

ADC	Analog to Digital Converter
BMS	Battery Management System
CAES	Compressed Air Energy Storage
CC	Current Control (or Current Controller)
CCHP	Combined Cooling Heat and Power
CHP	Combined Heat and Power
CSC	Current Source Converter
DAC	Digital to Analog Converter
DBS	DC-Bus Signaling
DER	Distributed Energy Resource
DG	Distributed Generator (or Distributed Generation)
DL	Dual Loop
DSOGI	Double Second Order Generalized Integrator
DUPWM	Double Update Pulse-Width Modulation
EDLC	Electric Double-Layer Capacitor
EES	Electrical Energy Storage
ESS	Energy Storage System
FFC	Feeder Flow Control
FFDSOGI	Fixed-Frequency Double Second-Order Generalized Integrator
FFPS	Fundamental Frequency Positive Sequence
HFB	Hybrid-Flow Battery
LC	Local Control
LIB	Lithium-Ion Battery
LPF	Low-Pass Filter

LV	Low Voltage
MCC	Microgrid Central Controller
MCU	Micro-Controller Unit
MG	MicroGrid
MIC	Microgrid Intermediate Control
MPPT	Maximum Power Point Tracking
MV	Medium Voltage
OCD	Over-Current Detector
OCV	Open Circuit Voltage
PCC	Point of Common Coupling
PHP	Pumped Hydro-Power
PHS	Pumped Hydro Storage
PL	Parallel Loop
PLL	Phase-Locked Loop
PV	Photo-Voltaic
RES	Renewable Energy Source
RFB	Redox-Flow Battery
SM	Synchronous Machine
SOC	State of Charge
SOGI	Second-Order Generalized Integrator
SPWM	Sinusoidal Pulse-Width Modulation
SRF	Synchronous Reference Frame
SUPWM	Single Update Pulse-Width Modulation
SVPWM	Space Vector Pulse-Width Modulation
TDD	Total Demand Distortion
THD	Total Harmonic Distortion
THIPWM	Third-Harmonic Injection Pulse-Width Modulation
TSO	Transmission System Operator

UPC	Unit Power Control
QSG	Quadrature Signal Generator
VC	Voltage Control (or Voltage Controller)
VISMA	VIrtual Synchronous MAchine
VOC	Voltage Oriented Control
VRB	Vanadium Redox flow Battery
VSC	Voltage-Source Converter
VSG	Virtual Synchronous Generator
VSM	Virtual Synchronous Machine

CHAPTER 1

Introduction

1.1 Thesis Context and Motivation

The current centralized and regulated electric utility is highly dependent on fossil fuels, such as coal, petroleum, and natural gas, to fulfil the consumer's energy demand. This fact is of high concern since the millions of tons of pollutant gases resulted from fossil fuel power generation, are the main cause of global warming [1]. Nowadays the energy market is in disruption with an increase of distributed and local energy sources as well as with the emergence of local high demanding loads, *e.g.* electric vehicles (EV) chargers. Following [2], the energy industry is the sector with the highest net reduction of greenhouse gas emissions, with a reduction of around 500 million tonnes of CO_2, that corresponds to a 30 % reduction in 27 years. This achievement is due to the increase in the penetration of renewable energy sources in the European Union (EU). Specifically, the share of renewable energy almost doubled between 2004 and 2018 [3].

Contrary to the energy sector, the transportation sector is still increasing its greenhouse emissions, with an increase of around 30 %. Nevertheless, the number of electric and hybrid-electric cars registered in the EU is on the rise, with an exponential increase of around 600 % in 5 years [4]. Globally, this exponential growth trend is visible in the 2018 IEA global EV outlook, where the yearly growth between 2016 and 2017 is over 50 %.

Looking at the panorama in Portugal, data from Redes Energéticas Nacionais (REN) and the *Associação de Energias Renováveis* (APREN) [5,6] reveals that in 2019 the imported/exported energy was set in a ratio of $7.0/3.6\ TWh$. Additionally, the total yearly electricity consumption was produced by the different energy sources, accordingly with the numbers illustrated in figure 1.1, for the total electricity production of 51 TWh.

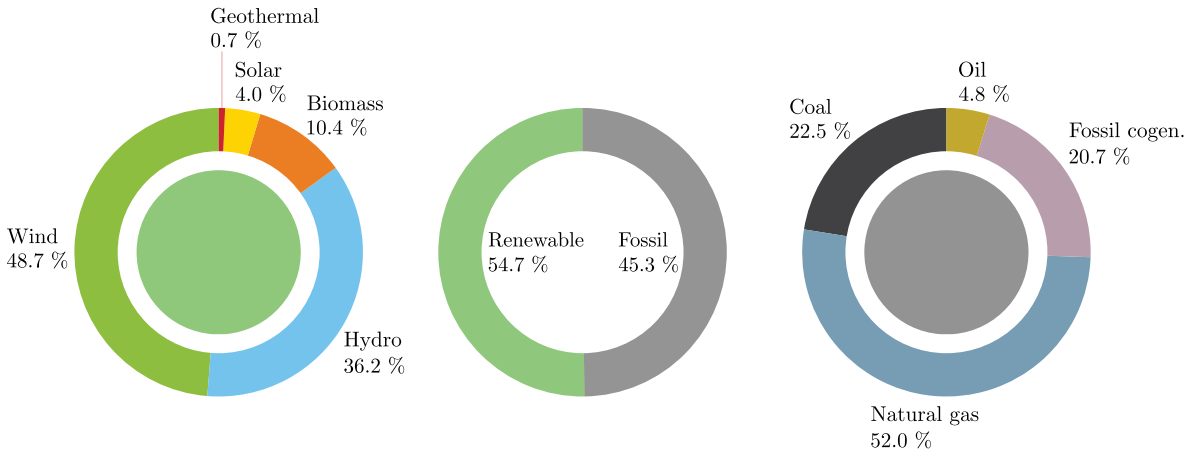


Figure 1.1: Share of renewable and fossil electricity in the overall electricity generation, for a total of 51 TWh.

Another important aspect is the figures related to the increasing penetration of renewable energy sources in the last years. In figure 1.2 it is shown that the increasing load demand, was mostly supported by the increase of fossil generation until 2005. In 2006 and later, the load demand has stabilized, but there is an increase of the renewable energy source (RES), which is a good indicator that energy sources are taking important adoption steps. Though, there is a considerable share provided by fossil fuels, suggesting that there is still a long way to fulfil a completely green energy scenario.

The growth of available RES and its trend are positive steps to decarbonize the energy sector, though it gives rise to other problems. The present energy utility system is based on a centralized control with unidirectional power flow: energy is generated on bulky power plants and supplied to the loads through the transport and distribution grids. Additionally, the global energy generation is expected to increase 2.4 % each year, from 16.424 billion kWh in 2004 to 30.364 billion kWh in 2030. The increase of the energy demand/generation increases the burden on the transmission and distribution systems since the update of these lines is economically challenging [7, 8]. To avoid the update of the transmission infrastructure and distribution lines, the integration of distributed generators based on RES has been studied as a viable solution. Their integration near the loads causes that the power demand can be fulfilled by the distributed generator (DG) power sources without flowing through the transportation and distribution chain. This leads to higher overall system efficiency and scalability since the transport losses are highly reduced and avoids overload of the transport lines [9].

Despite the benefits in the energy penetration from DG based on RES, there are several challenges for its integration such as the intermittent power availability due to weather conditions dependency,

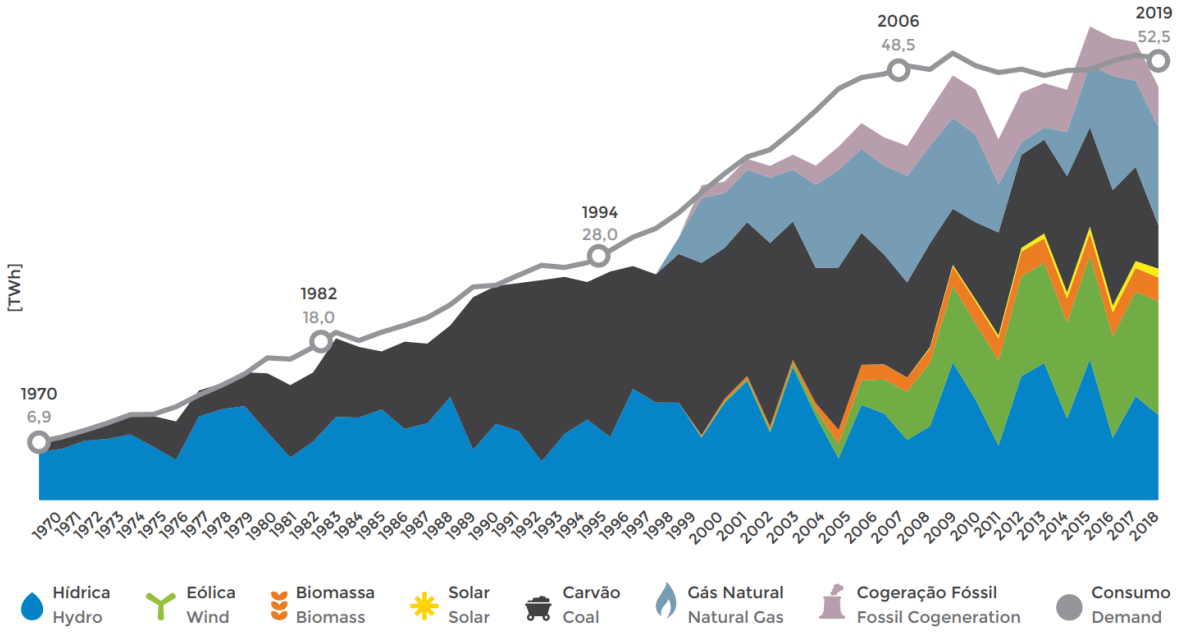


Figure 1.2: Historical evolution of the generation mix in Portugal mainland (from [6]).

change of the conventional power-flow direction (becomes bidirectional), and issues with power balancing resulting from inertia-less of DG interface with power converters. To overcome these problems the concept of microgrids has been a topic of high interest and study since it allows to integrate DG in the energy system as a single entity despite its composition. The microgrid allows the creation of an independent "subgrid" with independent power control that interfaces the main grid with fast response power converters and advanced power management units [7].

The microgrids also allow the integration of DG units near the loads, *e.g.* in the distribution grid, as well to optimize energy efficiency by considering applications with combined heat and power (CHP) or combined cooling heat and power (CCHP). These concepts also influence the project planning when installing new DG units. The electricity is more readily transported than heat, therefore overall energy efficiency can be improved by placing new DG units closer to the heat loads instead of the electrical loads. On present conditions, the introduction of CHP co-generation is often impeded by utility objections (legitimate or obstructionist). The microgrids allow overcoming some of that utility issues [9].

The introduction of DG leads to a growing concern for high quality, reliability, and usability of the electric power utility due to the increasing number of loads and energy penetration which has an impact on the power quality demanded, for these loads to work properly. This fact led to the emer-

gence of new control methods for power converters for advanced and proper power conversion and conditioning systems. The power converters are nowadays integrated into systems such as static VAR compensators, active power filters, uninterrupted power supplies (UPS) and grid-connected RES [10]. Microgrids need to overcome power quality issues related to their flexibility in the power supplied and fast response times. This fact can be further highlighted when considering the integration of ESS within the microgrids alongside with DG units based on RES [9, 11].

The ESS plays a critical role in the introduction of microgrids due to their power and energy availability. The ESS's along with the RES's allow to overcome the intermittent nature of RES and due to its fast power response support the local grid stability. Such aspects become critical when the islanding operation of the microgrids is considered, where the support from the main grid ceases to exist, and local grid stability becomes dependent only on the local power balancing.

1.2 Problem Description

The microgrids are by definition subgrids, with their own power management system, that may operate connected or disconnected from the main grid. The two modes of operation are defined as grid-connected or island modes of operation. There is no standard or definition relative to the microgrid size: there are several different approaches toward microgrids (from *kW* to *MW* range). Noteworthy that a *kW* range microgrid should be located in the distribution grid, and can hardly support the main grid. On another hand, if a context of massive adoption is considered, the grid interacts with hundreds of these microgrids, turning the participation of such microgrids in the support of the main grid valuable. In the scope of the thesis, the support of the microgrid is based only on the disconnection with the main grid, *i.e.* by disconnecting with the main grid, and keeping the ability to supply the local load demand, the microgrid is compensating part of the grid load contributing to lower the transported and centralized power generation demand. Such an approach requires that the microgrid must be capable of managing the local load demand by itself.

When operating in island mode, a microgrid may operate on a centralized, decentralized, or distributed power management basis. The centralized and distributed methods require the use of communication links to exchange information between the DG and ESS units what results in higher costs and harder expandability. On another hand, in a decentralized microgrid, each unit must be able to operate following the local grid power needs, based only on local measurements of the local microgrid.

The decentralized approach, based on the local control of each unit, presents several challenges as

there is no dedicated exchange of information with any of the interconnected units or loads. Nonetheless, the power balancing between generation and load must be guaranteed, and proper power sharing between units is required. Such issue becomes even more important when ESS's are considered, where improper power sharing may result in unbalanced energy availability of the ESS's, and ultimately the loss of a power unit (due to energy depletion). Furthermore, by sharing the power with equity, the power losses in the ESS units converters and lines are minimized, due to reduced I^2. Another aspect is the microgrid voltage waveform, which must be regulated under the standards to prevent tripping of local generation or preventive disconnection of the local loads.

1.3 Thesis Contributions

Based on the previously identified problems, the thesis has as the main goal to find a suitable decentralized control strategy that enables the operation of ESS's in the scope of three-phase AC low voltage island microgrids. Since the decentralized control is focused on local control, the operation of the voltage source converter that interfaces the ESS with the microgrid is crucial to achieving the main goal. Hence the thesis focus on all the control characteristics of the voltage source converter. The thesis contributions are:

1 A comparative evaluation and selection of double second-order generalized integrator (DSOGI) based phase-locked loop (PLL) - there are some different DSOGI based PLL but no clear differences are highlighted in the literature. In the thesis the more performant PLL's are compared, evaluated under different grid conditions, and ranked with weights chosen accordingly with its application (chapter 3);

2 A *LCL* filter design algorithm - the output filter plays a crucial role in the mitigation of the voltage harmonics produced by the converter switching, and in the design of the converter inner loop. It also has a significant impact on the converter cost. In the thesis, it is presented an algorithm that extends a design method found in the literature and allows to iteratively design the *LCL* filter (chapter 4);

3 A new voltage control loop - the proposed voltage control loop allows a faster voltage response to load changes, minimizing the voltage amplitude change during load transients (when compared with the traditional dual-loop). The proposed scheme also provides over-current protection (chapter 4);

4 An adaptive droop control - the proposed adaptive droop allows a properly active and reactive power sharing among connected units while balancing the different ESS's *SoC* (chapter 5);

5 A decentralized strategy based on AC signalling and master-slave configuration - the strategy consists of a single converter forming the grid and *n*' converters operating as grid support. The microgrid voltage amplitude and frequency set by the grid-forming unit sets an indicator for the grid-support converters to follow accordingly with the adaptive droop control (chapter 5).

Publications:

- J. Pinto, A. Carvalho, and V. Morais, "Power Sharing in Island Microgrids", Frontiers in Energy Research, vol. 8, no. January, pp. 1-14, 2021 (DOI: 10.3389/fenrg.2020.609218)

- J. Pinto, A. Carvalho, A. Rocha, and A. Araújo, "Comparison of DSOGI-Based PLL for Phase Estimation in Three-Phase Weak Grids", Electricity 2021 2, 244-270 (DOI: 10.3390/electricity2030015)

1.4 Thesis Structure

The thesis comprehends 6 chapters including the current one. Each chapter discusses a different theme, but simulation results follow the chapters sequence, *e.g.* simulation results from chapter 4 partially include results from chapter 3.

In chapter 2 it is presented the state of the art: it starts by exploring different microgrids architectures, principal operation modes of the voltage source converters in a microgrid, some of the services that microgrids may provide to the main grid, and the different microgrid management layers. The chapter continues by exploring the principal control blocks of the voltage source converter local control, identifying the state of the art strategies and trends. The chapter ends with a macro overview of different ESS's.

Chapter 3 analyses the different DSOGI based PLL. The different algorithms are discussed and worked to improve the performance of these methods at island microgrid operation. The analysed methods are compared under simulation and experimental results. Based on the achieved results it is established a benchmark.

The design of the *LCL* filter and inner control loops are discussed in chapter 4. The chapter begins with the *LCL* filter design procedure leading to the proposed design algorithm. From design

examples, it is discussed the impact on the current control loop design. The current control loop design is established considering the single and double-update methods. The impact of the considered designs is compared on different *LCL* design examples. The chapter includes a possible design for the voltage control loop (to form the conventional dual loop) and proposes a better alternative voltage control loop, here called parallel voltage control loop. The chapter ends by presenting the simulation results and the respective discussion.

The adaptive droop control and adopted approach for the microgrid decentralized system are presented in chapter 5. The chapter discusses the power coupling in the grids with emphasis on distribution lines. It is shown the origin of the conventional droop loop and it is analysed how virtual inertia can be added to such droop loop. The proposed adaptive droop scheme applied to the grid-forming and grid-support converters and the theory behind the proposed master-slave approach are then analysed. The chapter ends with the achieved simulation results, partially validated through an experimental setup and the respective discussion.

In chapter 6 the main conclusions of the thesis are summarized, as well significant and possible future work.

CHAPTER 2

State of the Art

The present chapter presents the research carried during the thesis period to identify the key aspects and challenges related to the integration and control of microgrids.

In sections 2.1 and 2.2 all aspects related with the fundamental operation and design of the microgrid are presented. The first section starts with the definition of microgrids, including the types of microgrids and the two fundamental modes of operation. In section 2.2 complementary modes of operation are described, as an extensions to the basic microgrid operation modes. Additionally, it is presented the control strategies that ensure proper power management in microgrids for both microgrid common buses current types (AC and DC).

At the end of the chapter (section 2.3) it is presented a macro overview of different energy storage systems that can be applied in microgrids.

2.1 Microgrid Definitions

In the literature, it can be found several definitions for the microgrid concept which differ based on the advantages that are pretended to be highlighted. A definition that is broadly cited, developed for the U.S. Department of Energy by the Microgrids Exchange group, defines microgrids as *"a group of interconnected loads and distributed energy resources within clearly defined electrical boundaries that acts as a single controllable entity concerning to the grid. A microgrid can connect and disconnect from the grid to enable it to operate in both grid-connected or island mode."* [12, 13]. From the point of view of smart grids, the microgrid (MG) can be seen as a controllable source/load and, from a more abstract point of view, as a system of systems [7, 11, 14]. The presented definitions adequately describe the microgrid concept depending on the target application and the problems that may be solved with its integration. Independently of the definition, the designing process of a MG system, must include at least the two main operating modes: grid-connected (the microgrid is connected to the main grid) and island mode (the microgrid is isolated from the main grid).

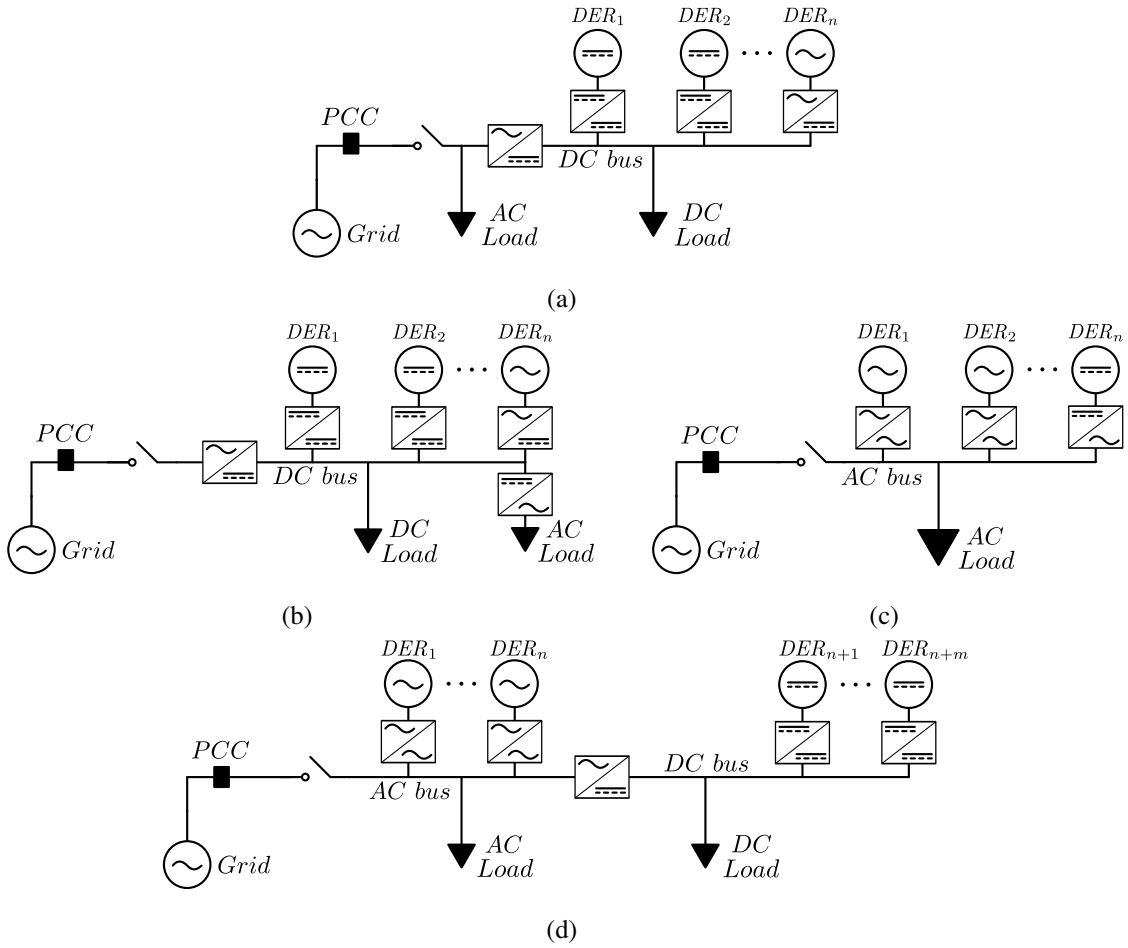


Figure 2.1: Examples of microgrid configurations schematics, where converters represent controllable units: (a) DC microgrid, (b) DC microgrid with isolated AC load, (c) AC microgrid (d) Hybrid microgrid.

Based on the two working modes, and the MG definition, it is possible to have many configurations for the MG which will defer mainly with the common bus current type. In figure 2.1 it is shown some schematics representing different types and configurations for the MGs, where independently of the source (AC or DC), it exists a power converter interfacing the distributed energy resource (DER) unit with the respective common bus [15]. Additionally, the static switch, at the point of common coupling (PCC) transformer, allows switching between modes (grid-connected or island mode).

The type of MG can be defined by the type of bus used to interconnect the DER units with local loads, *e.g.* if both DER and loads are connected through a DC bus, it is considered a DC microgrid. As stated before, independently of the DER unit output power to be AC or DC, it can be connected to

both types of buses: directly or through a power converter [11].

The AC waveform has been the standard choice for the commercial energy system (main grid) mostly because it allows to easily transform power between different voltage levels (through power transformers). Additionally, it allows the direct connection of power plant generators based on fossil fuels. The AC MG (as illustrated in figure 2.1c) has a clear advantage when compared with the DC MG, related to the fact that the main grid and the majority of the appliances are currently AC. Therefore the AC MG can connect directly (normally through a power transformer) with the main grid [11] and does not require generating a dedicated AC bus for typical appliances. On another hand, there is an increased complexity on the AC MGs such as the necessity of synchronization between each DER unit and the AC bus (becomes worst during islanding) and power balancing/sharing (*e.g.* Q-V and P-ω droop control), which is highly dependent on the output power converter filter and line impedances [11, 16, 17].

The DC MGs, contrary with the AC MGs, obviously do not suffer from synchronization or reactive compensation problems, being a suitable solution to overcome the aforementioned problems. There is also an increasing number of DC RES solutions, DC electrical storage systems, and DC loads, which are suitable to connect with DC buses. Some of the aforementioned technologies are photovoltaic cells (PV), batteries, fuel cells, plug-in electric vehicles (PEV), LEDs for illumination systems, portable device chargers, *etc*. Besides, there is no need for phase balancing, no problems related to harmonics, no electromagnetic interferences, no reactive power, and therefore the DC transport is more efficient than the AC, allowing to reduce energy transport costs [11, 18, 19]. Additionally, it should be noticed that nowadays power converters can handle MVA at high efficiency and reliability [20]. Therefore, DC MGs are a suitable choice for new installations and future power system scale-up.

It is clear that DC offers better benefits when compared with AC, though it is very expensive to implement it since the existing infrastructure is AC, and change it to DC would (or will) require a lot of financial investment. Hence it seems natural that in near future, most of the microgrids will be AC or hybrid.

In figures 2.1a and 2.1b it is shown possible topologies applied to a DC MG where the only difference is in the AC loads connection. In figure 2.1a it is presented a topology that allows the MG DER units to trip (due to some failure or insufficient energy storage/production) without compromising the power delivered to the AC local load since power demand is ensured by the main grid. Furthermore, during island mode, the AC/DC converter must generate the AC voltage supplied to the AC

load, which gives rise to new challenges, mostly during grid reconnection, where generated voltage waveform must be fully synchronized with grid voltage or otherwise reconnection will result in high current transients. In figure 2.1b, the AC voltage is generated by a dedicated inverter, and therefore it is never directly connected to the main grid. This approach allows a seamless operation mode transition though, in the situation of a MG failure, the isolated AC load is shed. It seems natural that evaluating both scenarios, the preference should be to value the interruptibility of the power supplied to AC loads. For that reason the DC MG of figure 2.1a is prone to be chose in a real-life application.

The hybrid MG, presented in figure 2.1d, obviously offers the advantages of both DC and AC MGs but may also present drawbacks. The fact of having to monitor and regulate two buses instead of one increases the overall complexity of the system. Nevertheless, a common DC bus may offer the possibility of cut costs by allowing to integrate DC DER without inverters. Furthermore, if a MG is considered, *e.g.* for an existing neighbourhood, it is impractical to add a DC bus to the actual infrastructure instead of taking advantage of the existing AC bus. In that scenario, DC buses, geographically dispersed, interconnect different DER units where each may behave as an independent co-generation system with a single power converter interfacing the existent AC line. If the several DC co-generation systems are connected to the same AC line and covered by the same PCC, the existent system becomes an MG with shared AC and DC buses, and therefore the overall system may be considered a hybrid MG. The given example is the most promising scenario for the nearest future and for that reason neither AC nor DC MG should be ignored.

The MG interest can be shown by the growing number of testbeds around Europe and the United States, where different configurations and control strategies are adopted to prove different concepts [21, 22]. Some of the recent projects and testbeds in the U.S. and China are highlighted in [23].

2.2 Microgrid Power Management and Control

In the present subsection, it is discussed the control and different modes of operation of the microgrid. Despite some differences between the control strategies between AC and DC MGs, most of the topics to be discussed are somehow transversal to any configuration.

The control of the MG is currently one of the topics of exhaustive investigation since, as already been said, the MG plays a crucial role in the integration of DER in the actual energy system. That role is mostly based on the control flexibility that the MGs should present. To achieve so, the MG capability to operate not just autonomously but also in cooperation with the main grid, is of utmost

importance.

The control of the MG can generally be separated into three different control layers: primary, secondary and tertiary [7, 24, 25].

The primary control level is an autonomous and local controller (LC), implemented in the power converters (microcontrollers) interfacing the DER units with the common bus. The control loops applied on this level are mostly based on the converter elementary control algorithms, *e.g.* voltage, and current loops. Those are the basic controls necessary to operate with the MG and, to avoid compromising the MG safety, no communication networks are used on this level. Also, one of the most explored topics is to include the power-sharing control, which is commonly centralized in the secondary control level, in the first level. The most explored technique is the droop control, applied as a voltage droop control (for DC buses), or P-ω and Q-V droop controls in the case of the AC buses. [1, 7, 8, 24, 26].

The secondary control level, also known as microgrid intermediate control (MIC), is responsible to switch between operation modes of the MG (grid-connected or island mode) and some other operation features. It makes use of low bandwidth communications to acquire measurements on MG nodes of interest and processes the measured information to generate references to the LCs. Those actions may be based on local necessities but must also follow the grid requirements. Some of the operations carried out by the secondary control layer may include the restoration of V-ω steady-state errors, ensure synchronization between MG and main grid voltages (seamless reconnection), change of operation modes (island to grid-connected and *vice-versa*) and correction of droop gains. For the DC buses, the task of the secondary layer is mainly to restore the DC voltage while in the AC to restore voltage magnitude and frequency. From the point of view of control communications, the MIC is responsible to generate the power references, reference voltage and frequency for the LCs [7, 11, 24, 27].

The tertiary level operates in cooperation with the grid and is responsible for making the decisions about the different operating modes of the MG. The tertiary control level is responsible for the MG management and is known as the microgrid central controller (MCC). The tertiary level is responsible for setting the operational tasks such as control of power flow at the PCC (power flow with the main grid), pricing and economical optimization, islanding detection, generation of voltage and frequency external references, etc. Some known operation modes are the unit power control (UPC), feeder-flow control (FFC), peak shaving, load shedding or ranked load shedding [7, 14, 26, 28].

On the following subsections, the MG controllers will be focused on MGs LC.

2.2.1 DC microgrid local control

On the following subsections, the MG controllers will be focused on MGs LC. As already mentioned, the primary control level is the local control implemented in the power converters that interface the DER units and the common bus, hereby called by LCs. The inner loops, of the LC, are composed of the current and voltage controllers which are commonly implemented with *PI* controllers. Despite of such common approach, there are alternative methods that makes use of *PD*, *PID*, *fuzzy* logic or non-linear control [26]. The converters may work in two different modes: current source converter (CSC) or voltage-source converter (VSC) by adding control close loops, depending on the control variable of interest. In the CSC the voltage at the converter terminals is adjusted to produce the desired output current. In the VSC an extra loop is added to regulate the current fed to the current loop, accordingly with the desired converter output voltage reference. Furthermore, considering that several DER converters are sharing the same bus, the reference voltage can be generated by the power-based droop or the current-based droop blocks. Alternatively, if an ESS with enough capacity is presented in the system, each DER unit can operate as a CSC and the ESS as a VSC. In this scenario, there is no need of adding droop controllers since there is no shared regulation of the DC bus voltage, *i.e.* only one unit is in charge of balancing the power flow (regulate voltage). Though even if a single VSC regulates the DC bus voltage, a P-V droop may be added to change the regulated voltage level proportionally with the instantaneous converter power. This way, other DER connected as *CSC* to the DC bus may follow a V-P droop and consequently contribute to the power-sharing. To summarize, when a common bus is shared by more than one VSC it is necessary to handle guarantee a stable power-sharing between the VSCs to ensure a stable power flow of the system.

To illustrate the converter controllers described above, figure 2.2 is shown. Note that when the converter works as a CSC, the illustrated droop and voltage controllers are turned off. Though current droop can be employed.

The droop coefficients have a great impact on the power-sharing between the DER units and the system stability. Furthermore, the coefficients are dependent on the number of the connected DER converters operating as VSC and the distances between power loads and sources. The power-sharing methods vary accordingly with the implementation scheme: as a centralized, decentralized, or distributed control [24, 26]. The centralized and decentralized control is based on a digital communication structure and for that reason is implemented in the secondary control level (subsection 2.2.3).

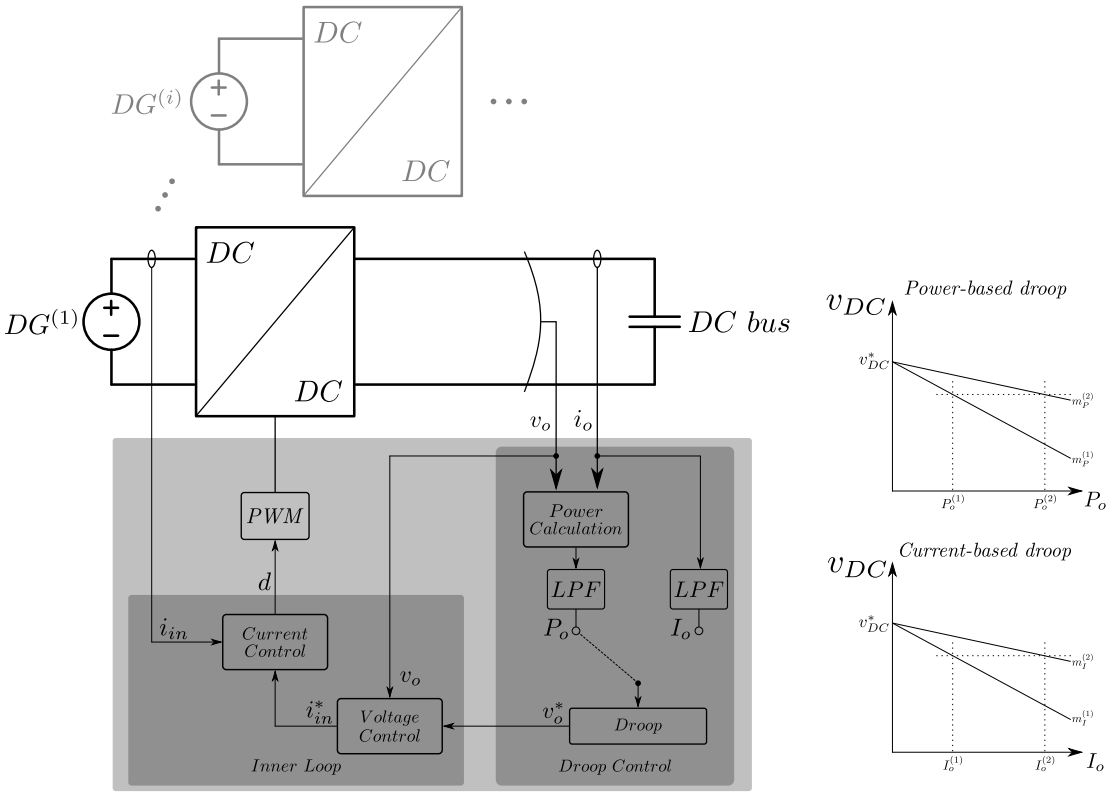


Figure 2.2: Control diagram of DC bus interface power converters (adapted from [26]).

The decentralized control, contrary to other approaches, does not require digital communications resulting in a more robust approach. When decentralized control is adopted, there is no need for a secondary control level resulting in cost reduction, power quality enhancement, and in a more reliable system [27]. Some of the most common methods of the decentralized control applied in DC MGs are DC-bus bus signaling (DBS), adaptive droop, and adaptive virtual impedance.

The DBS method is a method that makes use of the DC bus voltage to change the units operating mode. Considering that several DERs are connected to a DC bus of a certain MG, it is possible to balance the system by considering that part of the DER units are working as CSC (*e.g.* a photovoltaic operating in MPPT) and the others as VSC. The units working as VSC regulate the DC bus voltage, while the units working as CSC only inject current without regulating the DC bus voltage. The power unbalance in the DC bus is translated by an increase of the DC bus voltage if the power supply is greater than the load power. In the case, that load power is greater than the power supplied, the DC bus voltage drops. Considering this principle of work it is possible to monitor the power unbalance by monitoring the DC bus voltage magnitude and knowing the rated DC voltage. The LC of each

DER unit may be defined to work as a CSC or a VSC accordingly with fixed thresholds on the DC bus variation. This method allows to prioritize which DERs should work in voltage regulation or power injection, and simultaneously do not depend on a single device. The independence is intrinsic to the control method since if a DER stops regulating the DC bus for some reason, the DC bus voltage changes, crossing a threshold that triggers the control mode of other DER units [16, 29].

The local adaptive calculation of virtual resistance is based on the power or current droops presented earlier. The fact of operating in a DC bus allows considering the *V-I* droop coefficient as a virtual resistance. The virtual resistance may be changed to increase or decrease the power contribution of the respective DER unit. Noteworthy, that in this case the virtual resistance only offers a more meaningful determination of the droop curve slope, as the methods are equivalent. This kind of control may be particularly useful for power-sharing between ESS so that the state of charge of both remain approximately balanced and simultaneously avoid deep discharges or overcharges. A method presented in [30] is base on *fuzzy* adjustment of the virtual resistance accordingly with the DC bus voltage and the state of charge (SoC) of the battery. In the same article, the *fuzzy* rules are adjusted to work with photovoltaic panels when the batteries are discharged and can no longer work as DC bus regulators.

In [31] it is mentioned that regulating the virtual resistance of the droop is only effective in steady-state and does not consider transients. The authors suggest a hybrid storage system (batteries and supercapacitors) where the virtual resistance should be treated as a virtual impedance instead. This approach allows controlling both dynamic and steady-state power-sharing. In the given example the virtual impedance is adjusted to behave as a low pass filter to the batteries and a high pass filter for super-capacitors, hence it can be possible to take advantage of the respective power density, energy density, and response time capabilities of each ESS nature. The supercapacitors compensate for the fast transient power, while batteries balance the power during steady-state.

2.2.2 AC microgrid local control

As discussed earlier in this chapter, independently of considering a DC, hybrid, or AC MG, at least one converter to interface with the main grid is needed. Otherwise, it would not be possible to switch between operation modes (grid-connected and island mode). Furthermore, on the present electric power system, all existent loads interface the AC grid independently of their nature. For those reasons, the AC interface is crucial for the integration of MGs. The LC of the AC interface, similar to

the DC LC, is composed of an inner loop and droop control. Different from the DC case, the power unbalance is reflected in the AC interface in terms of frequency and voltage deviations. Similarly, with the DC MG, the most common approach to achieve power-sharing between converters is through droop control, though different alternatives are suggested in literature such as virtual impedance or virtual inertia (virtual synchronous generator).

2.2.2.1 Power sharing - Droop

The typical droop control is applied by considering decoupled power components and its linearity with the line voltage and frequency. To illustrate that linearity, the simplified circuit diagram shown in figure 2.3 is considered. The resulting power flow through the line is expressed in therms of active and reactive power by (2.1), where δ represents the power angle and R line resistance and X line reactance. The X/R ratio obviously depends on the impedance phase angle θ (2.2). Considering a distribution low voltage line, where $R >> X$ and a small power angle δ, (2.1) can be simplified into (2.3), becoming clear the decoupled influence of P and Q in voltage magnitude and phase angle respectively. Expression (2.3) is the base of droop control expressions (2.4), the so known P-V and Q-ω relations [17,27,32]. Noteworthy, that conventional droop relationship (2.4) is derived from (2.3) assuming that a power angle change is caused by a change in frequency. The droop control is further explained in detail, later in chapter 5.

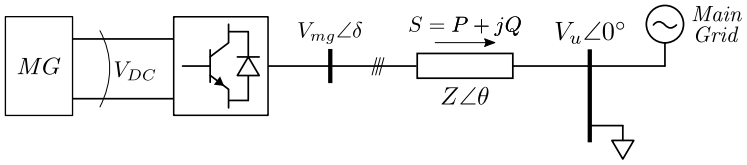


Figure 2.3: Microgrid AC interface equivalent model
(adapted from [27]).

$$\begin{aligned} P &= \frac{V_{mg}}{Z^2}\left[R\left(V_{mg} - V_u\cos(\delta)\right) + XV_u\sin(\delta)\right] \\ Q &= \frac{V_{mg}}{Z^2}\left[-RV_u\sin(\delta) + X\left(V_{mg} - V_u\cos(\delta)\right)\right] \end{aligned} \tag{2.1}$$

$$\theta = \tan^{-1}\left(\frac{X}{R}\right) \Leftrightarrow \begin{cases} X >> R: & \frac{R}{Z} \simeq 0 \ \wedge \ \frac{X}{Z} \simeq 1 \Leftrightarrow Z \simeq X \\ R >> X: & \frac{R}{Z} \simeq 1 \ \wedge \ \frac{X}{Z} \simeq 0 \Leftrightarrow Z \simeq R \end{cases} \tag{2.2}$$

$$\begin{cases} P \simeq \dfrac{V_{mg}}{R}\left(V_{mg} - V_u\right) \\ Q \simeq -\dfrac{V_{mg}V_u}{R}\delta \end{cases} \Leftrightarrow \begin{cases} V_{mg} - V_u \propto \dfrac{RP}{V_{mg}} \\ \delta \propto -\dfrac{RQ}{V_{mg}V_u} \end{cases} \tag{2.3}$$

$$\begin{aligned} V &= V^* - k_P\left(P - P^*\right) \\ \omega &= \omega^* + k_Q\left(Q - Q^*\right) \end{aligned} \tag{2.4}$$

To be noticed that contrary to the given demonstration, typically high X/R ratios (*e.g.* medium voltage transport lines) are considered. In such conditions (2.1) can be rewritten as (2.5) which is the basis of the power-angle (or voltage-angle) control [33]. Additionally the corresponding droops follow the P-ω and Q-V relations.

$$\begin{cases} P = \dfrac{V_{mg}V_u}{X}\sin(\delta) \\ Q = \dfrac{V_{mg}^2 - V_{mg}V_u}{X}\cos(\delta) \end{cases} \tag{2.5}$$

In general, both X and R may be considered. To be able to influence the grid frequency and amplitude through independent and separate power components, without considering a pure resistive or inductive line, a method is originally proposed in [34]. The method consists of the rotating power components accordingly with the line impedance phase angle, resulting in a modified P' and Q'. The rotation is achieved by applying the transformation matrix T_{PQ} (2.7) to the P and Q power components (2.6).

In (2.7) $\phi = \pi/2 - \theta = \arctan(R/X)$ is the transformation matrix rotation angle and θ the angle of the line impedance. Applying the transformation matrix (2.6), (2.3) is transformed into (2.8). Additionally, considering that the power angle only takes small values, (2.8) can be further simplified into (2.9).

$$\begin{bmatrix} P' \\ Q' \end{bmatrix} = T_{PQ}\begin{bmatrix} P \\ Q \end{bmatrix} \tag{2.6}$$

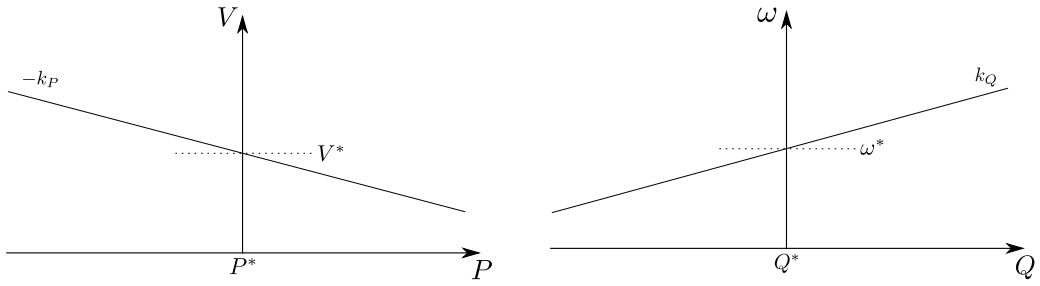
$$T_{PQ} = \begin{bmatrix} \cos(\phi) & -\sin(\phi) \\ \sin(\phi) & \cos(\phi) \end{bmatrix} = \begin{bmatrix} \sin(\theta) & -\cos(\theta) \\ \cos(\theta) & \sin(\theta) \end{bmatrix} = \begin{bmatrix} \frac{X}{Z} & -\frac{R}{Z} \\ \frac{R}{Z} & \frac{X}{Z} \end{bmatrix} \tag{2.7}$$

$$\begin{aligned} P' &= \frac{V_{mg}V_u}{Z}\sin(\delta) \\ Q' &= \frac{V_{mg}}{Z}\left(V_{mg} - V_u\cos(\delta)\right) \end{aligned} \quad \Leftrightarrow \quad \begin{aligned} \sin(\delta) &= \frac{ZP'}{V_{mg}V_u} \\ V_{mg} - V_u\cos(\delta) &= \frac{ZQ'}{V_{mg}} \end{aligned} \tag{2.8}$$

$$\begin{aligned} \delta &= \frac{ZP'}{V_{mg}V_u} \\ V_{mg} - V_u &= \frac{ZQ'}{V_{mg}} \end{aligned} \tag{2.9}$$

Equation (2.9) shows that if the impedance angle is adjusted correctly, then it is possible to control the power angle through the modified active power P' and the voltage magnitude through the modified reactive power Q'. To be noticed that the phase frequency is influenced by the power angle and for that reason P' and Q' allow to control line frequency and magnitude. Besides, to be able to apply the transformation matrix, the X/R ratio must be known independently of its values. Moreover, for pure inductive lines it results $(P' = P) \wedge (Q' = Q)$, and for pure resistive lines $(P' = -Q) \wedge (Q' = P)$. Hence, the frequency and voltage droop control becomes (2.10) and are represented in figure 2.4 [32, 34], where the converter operates as an inverter or rectifier when its output power is negative or positive respectively.

$$\begin{aligned} \omega - \omega^* &= -k_P(P' - P'^*) = -k_P\frac{X}{Z}(P - P^*) + k_Q\frac{R}{Z}(Q - Q^*) \\ V - V^* &= -k_Q(Q' - Q'^*) = -k_P\frac{R}{Z}(P - P^*) - k_Q\frac{X}{Z}(Q - Q^*) \end{aligned} \tag{2.10}$$



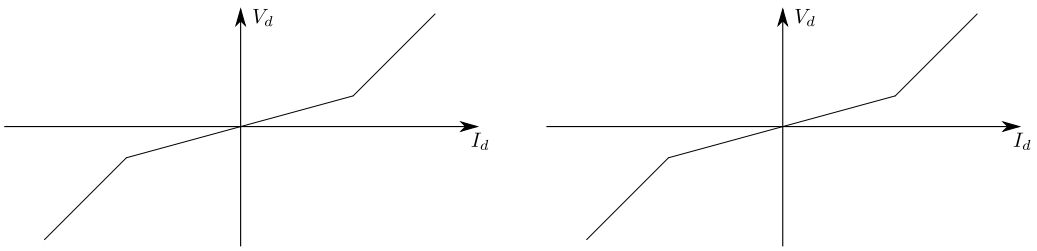
(a) (b)

Figure 2.4: Droop control curves for a resistive line: (a) P-V curve, and (b) Q-ω curve (adapted from [32]).

Despite the proven concept of droop methods in the medium-voltage (MV) networks, for the regulation of voltage amplitude and frequency, the performance of the droop method is highly dependent on the X/R ratio of the line. This dependency limits the kind of networks where the droop control

can be employed, since it may not be possible to have perfect knowledge about the line impedance resulting in unbalanced power sharing [32].

There are other droop control methods based on the conventional droop of figure 2.4, where droop relations are changed but fundamentally follow the same logic of the conventional droop. In [35, 36] it is proposed a V-I droop characteristic ($V_d - I_d$ and $V_q - I_q$) instead of the conventional $P - V$ and $Q - \omega$ droops, claiming that current flow is easier analysed than power flow. Additionally, the authors suggested that droop curves should be piecewise linear instead of linear, to decrease sharing error and improve damping under heavy load conditions. The resulting curves are depicted in figure 2.5.



(a) (b)

Figure 2.5: $V - I$ piece-wise linear droop curves for an inductive line: (a) $V_d - I_d$ curve, and (b) $V_q - I_q$ curve (based in [35]).

2.2.2.2 Virtual impedance

The virtual impedance concept consists of changing control loop references (voltages, currents, or power). The reference changes are emulated by implemented passive elements, that are not physically added to the circuit, in the control loop. This approach allows changing the equivalent system closed-loop impedance, which justifies its name.

A comprehensive description of the existent virtual impedance techniques and their goals are explained in [37]. The virtual impedance methods can be divided into two main subgroups: inner-loop virtual impedance and outer-loop virtual impedance.

The inner-loop virtual impedance consists of adding feed-forward paths to the control loop so that virtual impedance has a direct impact on the modulation voltages of the power converter. This approach allows adding virtual impedances whose dynamics are independent of the control loop. The most common application of the inner loop virtual impedance is in the active damping of the *LCL* filter, where a resistive impedance is added to the capacitor current feedback allowing to mimic the

resistive passive damping, without adding the extra losses. In [38] it is suggested a virtual impedance that allows achieving the capacitor damping with the grid-side current feedback, allowing damping filter resonant frequency, without an extra current sensor.

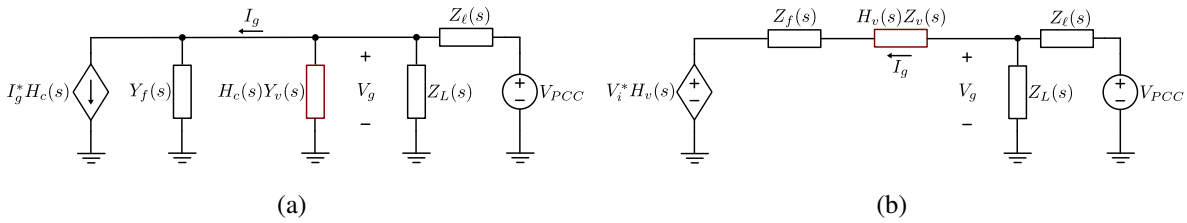
The outer-loop virtual impedance is applied to the control loop references and hence, it is also dependent on the control loop dynamics. There are several applications for the outer-loop virtual impedance, where the most common are power decoupling, harmonics [39], unbalance phase compensation [40], and fault-ride through [41]. For the scope of this thesis, the study on virtual impedance has been focused on power decoupling. Additionally, the virtual impedance is normally applied along with the droop control, allowing to improve the droop performance and consequently improve the power-sharing accuracy.

To solve the uncertainty of line impedance ratio, a common approach is to add a large link inductor to the converter's output, making the equivalent line impedance mostly inductive. In this case, the droop control can be applied considering a pure inductive line, as in the case of droop control employed in MV transport lines. This approach can obviously solve the power coupling problem, improving the power-sharing of the droop control, but it is far from being optimal since it demands: more space, higher costs, and higher DC bus voltage to compensate the voltage drop in the inductor, and consequently lowering the overall system efficiency. A more efficient solution is to virtually add the impedance Z_v to the control loop through a compensation loop of the reference voltage generated by the droop control (2.11). This way the virtual impedance is known and can be adjusted for successful power-sharing, as far as the virtual impedance has a higher value than line impedance. The virtual impedance becomes a control variable of the system allowing to control not just the power-sharing contribution but also the converter dynamics to the line voltage frequency and amplitude changes [32, 42].

$$V^* = V - Z_v(s) I_{grid} \tag{2.11}$$

The virtual impedance $Z_v(s)$ for power decoupling purposes can present a resistive or reactive nature, and it can be included in grid-forming (voltage controlled) or grid-support (current-controlled) converters. To illustrate its implementation it is presented figure 2.6 where $Z_v(s)$ can behave as a positive resistance, negative resistance, inductance, capacitor, or mixed impedance. In the figure $H_c(s)$ and $H_v(s)$ are the close loop current and voltage transfer functions, Z_f and Y_f the close-loop filter impedance and respective admittance, and Z_v and Y_v the added virtual impedance and respective

admittance.



(a) (b)

Figure 2.6: Virtual impedance equivalent circuit when applied to the outer loop of the: (a) current control loop , or (b) voltage control loop (based in [37]).

As represented in figure 2.6, the added virtual impedance accounts with the control loop dynamics and does not influence the converter filter transfer function.

2.2.2.3 Virtual synchronous generator

A more recent approach is called virtual synchronous generator (VSG) control, also known as virtual synchronous machine (VISMA) or virtual synchronous machine (VSM) [38, 43–45]. The concept consists of controlling the converter so that it can mimic the fundamental synchronous machine dynamics. To achieve such behaviour, the swing equation (2.12) is added to the control loop to generate the rotational frequency angle ω_m. Considering that the inverter modulation voltage is equivalent to the generator back electromotive force and inverter output filter to the synchronous machine (SM) windings impedance, then ω_m can be integrated to obtain the modulator phase angle. The modulator voltage amplitude is obtained by the $Q-V$ droop.

$$P_{in} - P_{out} = J\omega_m \left(\frac{d\omega_m}{dt} \right) + D(\omega_m - \omega_{grid}) \tag{2.12}$$

The VSG has the advantages of offering virtual rotational inertia to the system and also does not require a phase-locked loop (PLL), since the swing equation provides synchronization. Though during severe AC faults, the inner current loop is necessary, and therefore in that case a PLL must be provided [46]. To be noticed that despite the basic VSG structure mentioned here, several extensions make use of inner control loops such as the dual loop that will be discussed in the next subsection. An interesting conclusion is a fact that droop is equivalent to the VSG in the particular case that no inertia or damping is provided. Although in [38, 47] it is shown that if the measured power provided to the droop is filtered through a low-pass filter, the filter time constant is somehow equivalent to the

inertia provided by the VSG.

2.2.2.4 Inner loop and converter mode of operation

The AC converter can present and/or switch between two different configurations: grid-following (CSC) or grid-forming (VSC). The converter operation modes are summarised in figure 2.7.

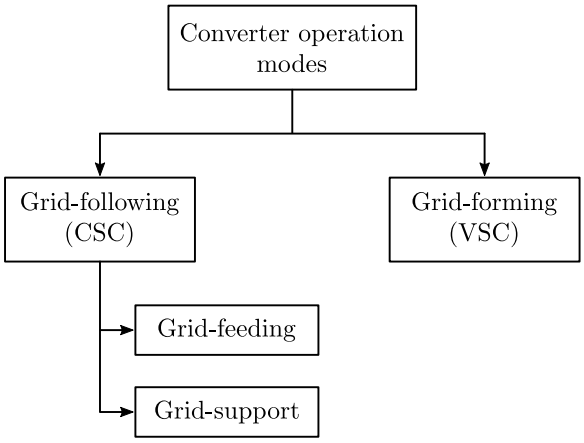


Figure 2.7: Converter operation modes.

Converters operating in grid-following mode may operate as grid-feeding or grid-support. The typical example in grid-feeding is the operation with MPPT. The grid-support operation is when the converter control loop includes methods that aids in the grid voltage waveform stability or regulation such as droop control, virtual impedance, harmonics elimination, *etc.*. During those operation modes, the converter requires a formed grid for syncing purposes and stable operation.

When the converter includes a voltage control loop, it can operate in grid-forming. During this mode, the converter can form the grid, though it is required some external power source connected to its DC bus. When several grid-forming converters are connected in parallel, all converters contribute to forming the grid, increasing the formed grid stiffness. When considering two grid-forming converters connected in parallel with high differences in the respective power ratings, it becomes obvious that the resulting voltage waveform is imposed by the converter that presents a higher power rating. In this case, the lower power rate converter can at most support/aid in the voltage regulation. For clarity, in this particular example, it is also considered that both converters operate as grid-forming.

Depending on the chosen configuration and employed strategy, the converters can be working as grid-forming, grid-feeding, grid-supporting, or ultimately switch between modes. The AC converters are configured as CSC when working as grid-feeding or grid-support, and as VSC when in grid-

forming (either in the island or grid-connected microgrid operation). The typical control loops for the CSC and VSC are presented in figure 2.9. It can be noticed that the CSC requires the feedback of the PLL for synchronization with the main grid voltage, adjusting the current (current control) accordingly with the desired power output.

The VSC when operating in grid-forming, has an additional control loop (voltage control) to regulate its output voltage. When the microgrid operates in grid-connected, the regulation of voltage can also be achieved, but pre-synchronism with the grid is required. When a microgrid is connected to the main grid, the difference between the grid-forming and grid-support converter modes is that the grid-support converter regulates its output power based on measured voltage amplitude and frequency, while the grid-forming regulates the generated voltage magnitude and frequency, based on the measured instantaneous output power. Such differences are highlighted in figure 2.8. Noteworthy that during grid-forming operation, the generated voltage is based on internal voltage and frequency references, while in grid-support the voltage frequency and magnitude are measured/estimated (normally through a PLL). In both modes, the droop control, virtual impedance, or similar methods, can be included for power-sharing purposes [7, 25, 27, 48].

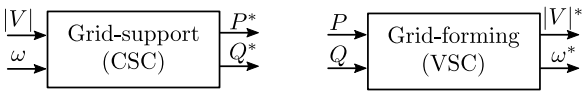


Figure 2.8: Main I/O's of the grid-support and grid-forming control blocks.

The control structure for both VSC and CSC configurations are shown in figure 2.9 (a) and (b). In both configurations one of the voltage components (normally the q component) is desired to be null, under three phase balanced conditions. Hence the rotating reference frame dq has the d versor aligned with the converter output voltage ($v_{mg} = v_{o_{dq}} = v_{o_d}$) [49].

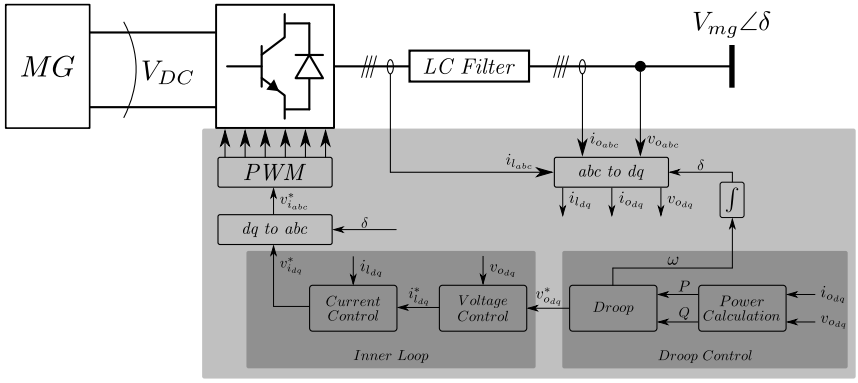
In the CSC the PLL estimates the voltage magnitude (v_{o_d}) and the respective frequency (ω), and phase angle (θ). Since the rotating reference frame is aligned with the estimated voltage, the estimated angle is applied in the transformation of the measured line currents ($i_{l_{abc}}$) into the rotating frame. The estimated voltage and frequency are fed into the droop control for power estimation. From the estimated power it is possible to generate the desired line current, knowing that the d component of the current contributes with active power and the q component with reactive power. The current control loop is shown in figure 2.9c, where L_f is the output filter inductance (or virtual inductance). The dq current components are decoupled accordingly with equation (2.13) [49, 50].

$$\begin{bmatrix} v_{l_d} \\ v_{l_q} \end{bmatrix} = (R_f + sL_f) \begin{bmatrix} i_{l_d} \\ i_{l_q} \end{bmatrix} + \omega L_f \begin{bmatrix} -i_{l_q} \\ i_{l_d} \end{bmatrix} + \begin{bmatrix} v_{o_d} \\ v_{o_q} \end{bmatrix} \tag{2.13}$$

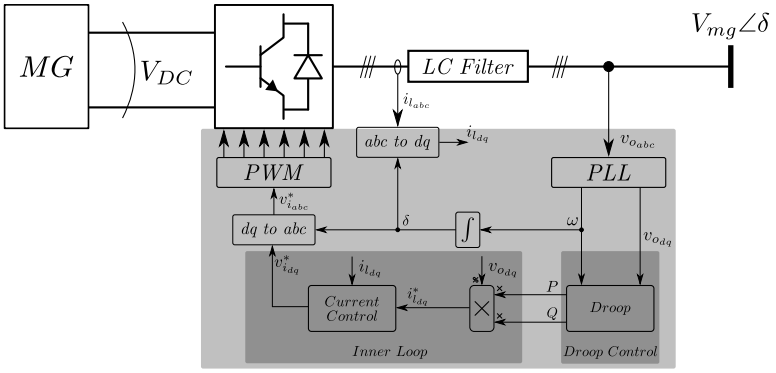
During grid-forming, the VSC, contrary to the CSC, does not require the external synchronism provided by the PLL if a single unit is responsible for grid-forming or by implementing a power synchronization control (PSC) as suggested in [46]. The latter is based on the synchronization mechanism of synchronous machines by making use of the virtual swing equation for synchronism, as mentioned earlier, but it may result in high transient currents during the process.

The measured currents and voltages allow estimating the power which is fed to the droop control, returning the desired phase voltage ($v_{o_{dq}}$) and frequency (ω) deviances. The resulting frequency from droop (or reference frequency if droop is excluded) is integrated and the resulting phase angle is applied for further transformation of all measures into the rotating frame. The desired phase voltage ($v_{o_{dq}}$) is fed into the voltage control loop and, as described before, the q component of the voltage is set to zero so that $v_{o_{dq}} = v_{o_d}$. The voltage control loop allows guaranteeing the synchronism by guaranteeing that the q component of the voltage is null and generates the desired currents to fulfil the desired power output. The voltage control loop is shown in figure 2.9c, where C_f represents the output filter capacitance. The dq voltage components are decoupled accordingly with equation (2.14) [49, 50].

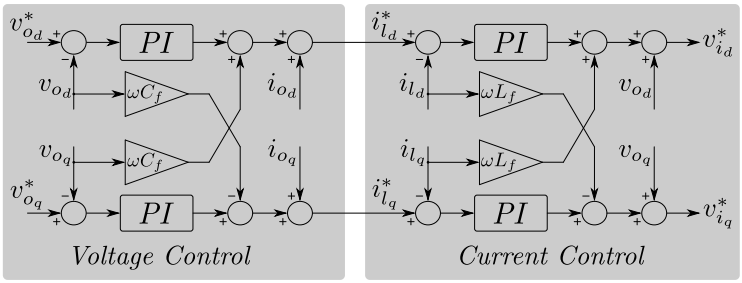
$$\begin{bmatrix} i_{l_d} \\ i_{l_q} \end{bmatrix} = \begin{bmatrix} i_{o_d} \\ i_{o_q} \end{bmatrix} + sC_f \begin{bmatrix} v_{o_d} \\ v_{o_q} \end{bmatrix} + \omega C_f \begin{bmatrix} -v_{o_q} \\ v_{o_d} \end{bmatrix} \tag{2.14}$$



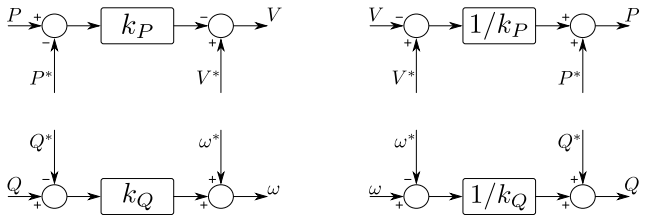
(a)



(b)



(c)



(d) (e)

Figure 2.9: Microgrid AC interface equivalent model (adapted from [27]): (a) VSC control structure, (b) CSC control structure, (c) voltage and current control loops, (d) VSC droop control and (e) CSC droop control.

As mentioned before, the CSC can not operate in grid-forming. For that reason if an AC MG switches to island mode, it is necessary to, at least one DER unit, be able to generate the grid, otherwise, the DER units will not be able to synchronize and will eventually trip. The VSC on another hand, allows the operation of both connected and in island mode, which provides good arguments for its application in MG interface. The CSC is mostly used in the grid-feeding operation associated with DG units connected to the MG since it allows to operate with maximum power point tracking (MPPT) control. During such operation, the droop can still be applied with reverse relation, *e.g.* the $P-\omega$ droop is expressed reversely as $\omega - P$.

The inner loop operation modes will be further discussed later in chapter 4.

2.2.3 Microgrid intermediate control

As already mentioned before in section 2.2, the secondary control level (MIC) introduces small bandwidth communications with the LCs. The MIC can be used just as an interface between the MCC and each LC in a distributed approach, or be a single point of communication with every LC in a centralized approach. As an alternative to the decentralized method mentioned in the previous section, the power-sharing control can be implemented in the MIC following one of the mentioned approaches.

The centralized control of power-sharing is implemented in the second control level of the DC MG requiring digital communications between the MG central controller and the LCs. The centralized control presents the advantage of turning the power-sharing algorithm as simple as it can be since all the information required is centralized and can be processed together. The information is exchanged based on a master-slave configuration where the master is the MG central controller and the slave each one of the LCs. The drawbacks of this approach are the dependency on the communications for the proper power-sharing: the delays introduced by the communications and the existence of a single point of failure (single MIC). Since the coefficients influence the overall system stability, this dependency may compromise the safe operation of the MG, which is not desirable [26].

The distributed control, as the centralized control, requires communications to exchange information. Differently from the centralized controller, in the distributed architecture the LCs communicate among themselves through dedicated digital network lines. On this communication topology, a digital communication channel between two LCs turns them neighbours and each LC should have at least two neighbours. Considering this scenario, the distributed control presents a better solution in terms

of flexibility, when compared with the centralized control, since it is immune to a single point of failure. To be noticed that if one of the LC suffers from some kind of fault, the overall system communication remains stable through the remaining neighbours. On another hand, the information must be processed locally by each LC to take proper actions. Besides, the information accessed by each LC is limited to the neighbours, which may result in a poor overall system observation. To solve the lack of information it is suggested in the literature to apply a consensus algorithm [7, 26]. Nevertheless, the fact of existing communications will always affect negatively the system reliability and increased costs.

Independently of the adopted control structure, one of the main goals of the MIC is to compensate the steady-state error of the MG voltage amplitude and frequency, restoring their values to the nominal ones. To be noticed that the droop control is a proportional control system and for that reason exists a steady-state error. Even considering a power-sharing method implemented in the primary control level that results in no steady-state error, the secondary level may be used for supervising the system variables adding redundancy. Furthermore, the MIC is responsible for controlling the common bus voltage profile to keep it within the allowed operational limits and, under particular operation modes, to provide power references to the LC layer, *e.g.* during FFC [32, 51].

2.2.4 Microgrid Central Controller

The tertiary control level is implemented in the MCC. The name explicitly indicates that this layer is centralized and it is responsible for decision making in terms of the MG global management. To be noticed that if the MIC is also centralized, both control levels may be merged and implemented in the same device.

The tertiary level handles issues related to the power exchange between the MG and main grid, *i.e.* the power flow at the PCC. It is noteworthy that the main grid can be either the utility or a master MG if the local MG is a sub-grid of another MG. Additionally, it can set modes of operation or power references to the different connected converters within the local MG. Since it can control the power flow at the PCC and local DER units, some of the tasks performed on this level are: optimization of the power flow based on an energy-production or energy-market objective, transition between the island and grid-connected modes, grid shaving, *etc.*.

2.3 Energy Storage Systems

As mentioned before, the ESS's play a crucial role in the operation of micro-grids constituted mainly by microgeneration units dependent on renewable resources. In this section, an overview of the ESS applied in stationary and high power systems is presented to evaluate which ESS are most suitable for the micro-grid application. The present study is focused on the basic principles of work and characteristics, from the electrical engineer point of view. At the end of the current chapter, a brief comparison between different energy storage systems technologies is presented.

There are several types of ESSs that can be distinguished in a variety of ways, being one of the distinguishing factors, the physics associated with the storage form. Nowadays, most of the large-scale energy storage is performed in the form of mechanical energy, through pumped hydro-power (PHP) systems ($\simeq 99$ %) followed by compressed air energy storage (CAES) system (< 1 %) . Furthermore, in the case of Europe, the amount of energy that is stored represents only 10 % of the total power delivered [52]. In recent years there have been considerable developments on different ESS technologies to be applied on high power systems, mostly based on three types: chemical, electrochemical and electric storage [52, 53]. In figure 2.10 it is shown a diagram with the most known storage systems, grouped by storage type [54].

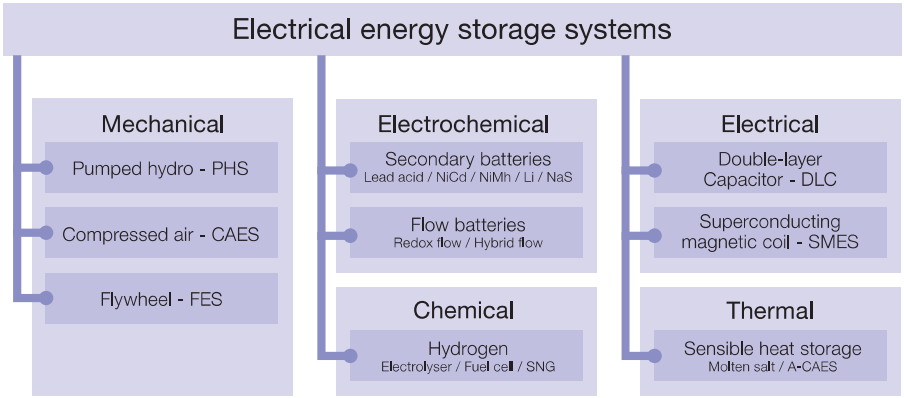


Figure 2.10: Energy storage systems for different energy storage types [54].

2.3.1 Mechanical Storage

The mechanical form of storage is suited for larger amounts of energy with power ratings in the order of the $10 - 100$ MW. The amount of energy and building costs are highly dependent on the

construction site geography: the PHP requires a river and a dam to store the water, and the CAES, caves to store the compressed air. Those aspects turn those systems bulky and not suitable for urban low-voltage (LV) micro-grids where the available space is more restricted and has much lower power demands. Nevertheless this kind of storage suits the power demands of large-scale systems for the reasons mentioned above and because it has a long life cycle ($>$ 40 years) [54–56].

2.3.2 Fuel Cell and Electrolyzer

The typical fuel cell is a unidirectional power flow cell that transforms an external supply of fuel into electricity but does not allow to reverse the reaction. The cell has as input flows: fuel (in anode side) and an oxidant (cathode side), and as outputs: electricity and the reaction product [56]. When the reactants (input flows) flow in the cell, they react in the presence of an electrolyte, triggering the reaction. Many possible combinations of fuel and oxidant will influence the storage system characteristics, *e.g.* the hydrogen fuel cell uses hydrogen as fuel and oxygen as the oxidant, producing electricity, heat, and water (H_2O) [55, 56].

To consider the fuel cell as a storage system, *i.e.* with bidirectional power flow, the fuel cell must be considered in combination with a fuel production unit, like an electrolyser. The electrolyser, in the case of hydrogen fuel, splits water (H_2O) into hydrogen and oxygen but requires electricity (*e.g.* polymer electrolyte membrane electrolysers- PEM) and/or heat (*e.g.* solid oxide electrolyser cells-SOEC) to trigger the reaction depending on the type of electrolyser [54, 55]. The produced hydrogen could then be fed to the hydrogen fuel cell and both systems as a whole would result in a bi-directional energy storage system.

Some of the topics that are currently most explored are the production of solar fuels and reversed solid oxide fuel cells (RSOFC). Solar fuels are produced with electrolysers where the reaction is triggered with high temperatures collected from a heat source such as solar accumulators. The RSOFC is a cell that has materials that allow the chemical reaction to occur in both ways and for that reason, the cell can work as a fuel cell or as an electrolyser (similarly with the electrochemical storage) [57]. An advantage of the described storage system is that if a hydrogen storage system is composed of a solar fuel production unit, a hydrogen fuel cell, and an electrolyser, it is possible to have an ESS that can produce, supply, and store electrical energy.

Some of the drawbacks of hydrogen fuel cells are related to the capability to store and supply the hydrogen in terms of system hermeticity, *i.e.* the system is subject to small leaks that can ultimately

result in serious consequences. Furthermore, to minimize the leaks on the system, expensive materials must be employed on the construction of the fuel cell and fuel tanks, making the initial investment very high [57].

2.3.3 Electrochemical Storage

The fundamental working principle of electrochemical storage is based on the oxidation-reduction (redox) reactions, which is a family of reactions that are concerned with the transfer of electrons between species. The oxidation occurs when there is a loss of an electron, while reduction when there is a gain of an electron. Because the redox reaction is balanced, i. e. when oxidation occurs there is also a reduction, which means that there are four different oxidation states (two in the cathode and two in the anode). For this reason, it is common to refer that an electrochemical battery, with a certain redox couple, is composed of two half-cells where each has its redox couple, that can cycle between two oxidation states depending on the redox reaction direction (charging/discharging). Furthermore, depending on the redox couple, an open circuit voltage (OCV) is obtained which is defined by the electrical potential difference between the redox couple elements. The choice of the redox couple has a large influence on the battery performance [53].

Currently, the electrochemical form of storage is one of the most explored in the bibliography and exists already a broad of different electrochemical storage systems with different characteristics. The electrochemical systems can be separated into two subgroups as shown in figure 2.10. The working principle, as already mentioned, is the same for all the different electrochemical systems, where the differences between the two subgroups are dictated by the place where the reactions occur which results in different characteristics for each storage type. For the sake of simplicity, only the Li-ion battery will be considered to represent the secondary batteries subgroup and the vanadium redox flow battery representing the flow batteries.

2.3.3.1 Li-ion Battery

The lithium-ion battery (LIB) was first commercialized by Sony in the early 1990s, outperforming the competition by at least a factor of 2.5, in terms of delivered energy and specific power. The LIB is currently the electrochemical battery that offers better performance in terms of energy and power density (it has a redox potential of $-3.04\ V$ vs standard hydrogen electrode) making this battery type very suitable for mobile applications where the size and weight are important factors. Additionally,

the application of LIB batteries in electrical vehicles, calls for a reduction of the LIB price to half and to double the present energy density. Those achievements should also benefit, with some differences, the stationary applications [52,56]. Along with power and energy density characteristics, the LIB can offer a better life cycle when compared with other secondary batteries [55].

The working principle of the battery has already been described before, so only some complementary aspects will be now emphasized. The cathode plays a vital role in the performance of the LIB and its material accounts for about 40 % of the battery cost. The cathode is a Li- intercalation compound: usually an metal oxide due to its higher potential (*e.g.* $LiMO_2, M = Co, Mn, Ni$, etc.). Currently, there are cathode materials that allow reaching higher OCV (*e.g.* $5\ V$) at the cost of poor performance on other aspects that may be: low life cycle, poor rate stability, sensibility to temperatures, etc. The anode is made of graphitic carbon with a layering structure and the electrolyte of lithium salts dissolved in organic carbonates. Along with the cathode and anode, there are current collectors to allow the electrons to transport between the external circuit and the electrodes. The current collectors for the cathode and anode are usually made of aluminium and copper respectively since those metals do not react with the electrode materials. In figure 2.11 a schematic of the LIB is shown. When the battery is being charged, the lithium atoms in the cathode become ions and migrate through the electrolyte toward the carbon anode where they are combined with external electrons becoming lithium atoms deposited between the carbon layers and balancing the redox reaction. When discharging, the process is reversed [52,56,58,59].

One of the main drawbacks of the LIB (and other solid-state batteries) is that the charge/discharge cycles make the materials in the electrodes expand and contract, which results in degradation over time and consequently harms the battery cyclic time [53]. Additionally, and specifically in the LIB, the overcharge and undercharge affect the battery lifetime, and therefore it must be carefully controlled. Also, a short-circuit or overcharge may result in a fire. For those reasons, it is critical to include a battery management system (BMS) to safely operate with the battery. The BMS allows supervising the battery, by monitoring the battery (*e.g.* temperature, current, voltage, estimation of the state of charge, etc.). It also operates the security system in the case that some of the security conditions are violated. Additionally, when considering a battery pack, there are cells at different charges (imbalanced). The imbalance may be caused by the manufacturing variance of the cell's internal volume, variations of each cell's internal impedance, differences in self-discharge rates, or other external reasons such as temperature gradients along with the battery pack. It should be noticed that

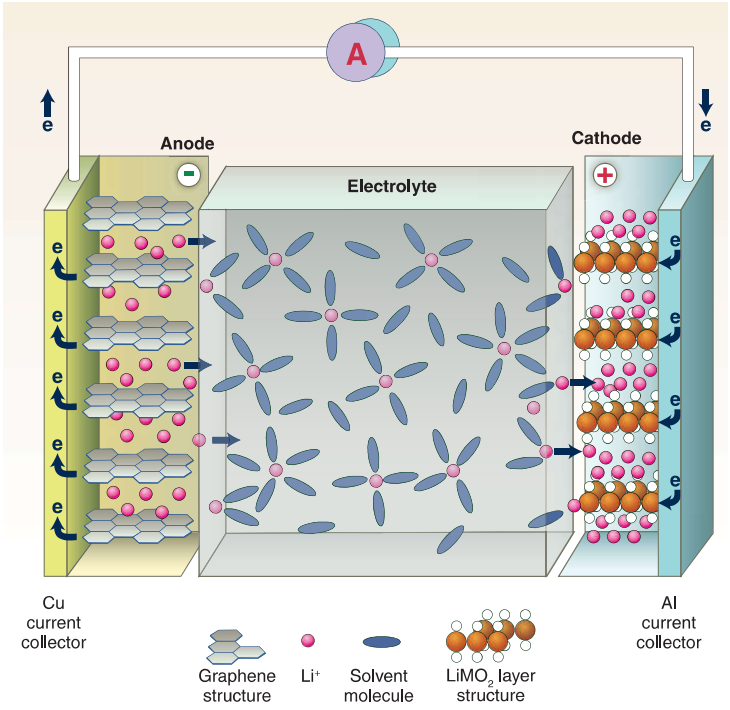


Figure 2.11: Schematic of the LIB during discharge [52].

such imbalances would only occur on cells in series since cells in parallel balance themselves. Some BMS includes a balancing system to make sure that every cell per stack is balanced to avoid overcharge or undercharge any cell, that may be imbalanced, and consequently result in a fire [60]. Those electronics must be added to the battery pack when a real system is considered which may influence significantly the battery pack overall price and the system design complexity.

2.3.3.2 Flow Battery

The redox flow battery (RFB) electrochemical working principle differs from conventional batteries, mainly in two different aspects [61]:

1. The active species are dissolved in the electrolyte, instead of being deposited in the electrode layers. This fact allows changing the battery operation principle resembling somehow a fuel cell, *i.e.* the electrolyte (like the fuel cell fuel) can be stored in external tanks and fed to the interior of the cell where the reactions occur. Differently from fuel cells, in the RFB the power flow is bidirectional since the reaction is a redox (as discussed before);

2. The reaction occurs between two electrolytes, rather than in the interface between the elec-

trolyte and the electrode, as in the case of conventional batteries. Therefore there is no electro-deposition or loss of electro-active substances with cyclic time.

The items mentioned before allow designing the battery with a flexibility that is not possible in conventional batteries. Because the electrolyte can be stored in tanks, the energy capacity of the battery is dependent only on the tank's volume. Furthermore, the battery power is only dependent on the stack design: the surface area defines the maximum allowed current and the number of cells in the stack the output voltage. Additionally, the fact that the electrodes do not swell and shrink, caused by the redox reaction during charge and discharge, leads to a considerable longer cyclic life.

There are two main different types of RFB: full-flow and hybrid-flow. On the first both active species are dissolved in the electrolytes. On the second one of the species is dissolved in the electrolyte while the other species are deposited on the electrode. It should be noticed that the hybrid-flow types of RFB suffer from the same cyclic time ageing as the conventional type of batteries, and this is the main reason why this kind of battery was excluded from this study. From now on the discussion will be based on the full-flow type of battery, specifically, the all-vanadium redox flow battery (VRB) [53].

The VRB cell is composed of the following parts: bipolar plates (electrodes), the carbon felts (electrode layers), an ion-exchange membrane, and a non-conductive polymer frame [53].

The bipolar plate is made of graphitic carbon and it is used as an interface between the carbon felts of every pair of cells in the stack. In both ends of the stack, the corresponding bipolar plates interface with an end plate (normally made of some metal to offer mechanical support and compress the stack) containing also the electrical contacts for the external circuitry. The materials used for the bipolar plate should have good mechanical strength, high electrical conductivity, good chemical resistance, corrosion resistance, high electrochemical activity for the desired redox reaction, and low cost. Nowadays, the material used in the bipolar plates is a carbon-composite material. The carbon felt also has the same properties as the bipolar plates, but contrary to the bipolar plate, it should be porous and does not need to present relatively high mechanical strength. As an alternative to the carbon felts, sometimes it is used carbon paper [53, 61].

The ion-exchange membrane is the most expensive component in a RFB stack (considering $€/m^2$). It has as objective to separate the cathode and anode compartments (mitigate crossover of the redox species), and at the same time to allow the passage of the charge-carrier ions to balance the redox reaction. It plays a crucial role in the RFB performance with impact in the Coulombic and voltage efficiency. The state of the art membranes are the Nafion ® that were originally developed for a dif-

ferent application and for that reason are not optimized for use with VRB. Those membranes were designed to maximize the ion conductivity neglecting the selectivity, which results, when applied in the VRB, in some vanadium species crossover. This a common problem in the VRB that demands periodically re-balancing of the electrolytes as will be further discussed later in this section.

The non-conductive polymer frame is used on the stack to support the layering parts and prevent flow leaks. Additionally, it cannot be electrically conductive and must be resistant to the electrolyte solution (the supporting electrolyte for the VRB is normally sulphuric acid). It must also contain a pair of fittings for the inlet and outlet flows.

In order to illustrate the building layer structure of a VRB stack (multi-cell), figure 2.12 is shown.

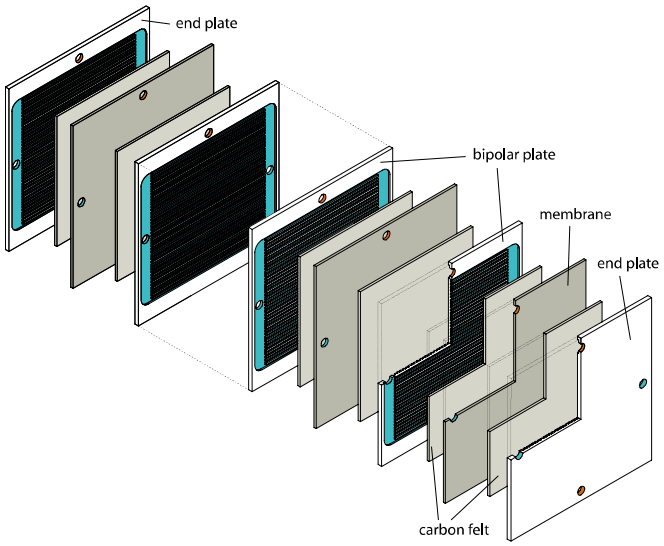


Figure 2.12: RFB stack layers [61].

Some of the drawbacks related to the VRB were already mentioned such as the necessity of re-balance the electrolytes (or the lack of ions selectivity), the high cost of the membrane, and the complexity in terms of design/assembly of the stack. On another hand, because the electrolyte flows over the stack, there is no need for a balancing system such as the one mentioned in the LIB packs. In terms of safe operation, the fact of having the electrolyte stored in tanks allows controlling the battery SoC by direct measurement of species concentration in the tanks. Some other aspects that need particular attention, are related to the price of the vanadium, thermal stability of the electrolyte (and temperature influence in the battery efficiency), the trade-off between pressure drop and fluid forced-convection in the electrodes (flow- fields), and the shunt currents. The last requires longer and

thinner reactants supply channels for each cell at the cost of increasing the pressure drops and the cell size. Nevertheless, the tanks can be installed in such a way that allows having a controlled temperature of the electrolyte, increasing system efficiency and safety. Common in all the issues addressed, is the impact they have on the VRB performance in therms of efficiency. [53].

Despite the problems related to the VRB, there are available solutions in the market (CellCube from GILDEMEISTER or VRB from redT). Furthermore the fact of several problems have already been identified, may suggest that there are promising advances to be achieved in a near future, increasing the VRB performance and the chance of asserts its place in the utility and/or micro-grid ESS market.

2.3.4 Supercapacitors

A supercapacitor (or ultra-capacitor, or electric double-layer capacitor) is composed of two porous electrodes, an ion-permeable membrane, and the electrolyte (may be aqueous or organic-based). Differently, from conventional electrochemical storage, the electric double-layer capacitor (EDLC) stores energy in the interface between the electrolyte and each electrode, forming two capacitance layers (double-layer). Because the energy is stored electrostatically, no redox reactions occur (which limits the cell voltage). Furthermore, the charge is stored by adsorption of electrolyte ions onto the surface of the electrode material, contrary to the conventional batteries where the electrode, that allows the redox reaction, is diffusion-controlled and can be slow [62–64].

The conventional capacitors use a dielectric to isolate both electrodes (made of ceramic, glass, plastic film, or aluminium oxide). When charged, the energy is stored in the dielectric material in an electrostatic field. The voltage limits are then dictated by the breakdown voltage of the dielectric, allowing to design of different voltages by using different dielectric materials with different thicknesses. In the case of the EDLC, similarly, with conventional batteries, it is necessary to connect cells in series to respectively reach a certain voltage [55]. The capacitance is proportional to the dielectric area and dielectric constant, and inversely proportional to the dielectric thickness. Since EDLC electrodes are normally thinner and more porous (normally made of a porous activated carbon), it presents a substantially higher electrode surface area and reduces the dielectric thickness (the layer between the ions and the electrodes), leading to a much higher capacitance [62, 64].

The EDLC due to its principle of work, similar to conventional capacitors, has high power density. The main drawback is the energy density since the amount of energy it can be deposited is

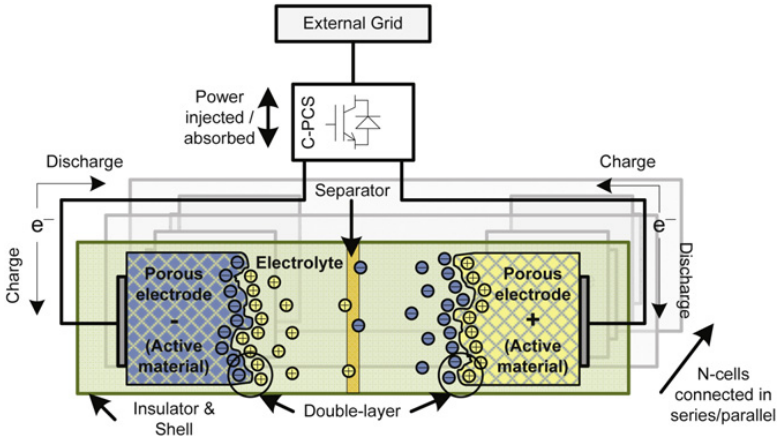


Figure 2.13: EDLC charges schematic [62].

proportional to the electrode area highly limiting the amount of energy that can be stored (when compared with electrochemical batteries). Studies are suggesting that changing the nature of one of the conventional electrodes (non-Faradaic) to a Faradaic electrode, transforming the supercapacitor on a hybrid. This way the energy would be partially stored: electrostatically (higher power density) and electrochemically (higher energy density). This hybrid supercapacitor is known to exhibit a pseudo-capacitance [64].

2.3.5 ESS Characteristics and Comparison

In this section, a brief comparison of what was considered to be the main technological attributes, for different ESS, is presented in table 2.1. It is pretended, based on the available information, to choose the ESS to be treated in the scope of the thesis.

Based on some information already mentioned during the review of each ESS, some of the above solutions were excluded from the ESS selection: the mechanical forms of storage because are bulky and not appropriate for urban LV MG, and the hydrogen-based storage for safety issues.

Despite the available information about costs [54–56] there was no certainty on how the costs were obtained. As already mentioned before in the case of conventional batteries, if the cost is based only on a single cell it may vary significantly when considered as a system (final product), since there are the cost increments due to mechanical structures, safety circuitry, energy management, etc.

If the above ESS are sorted by a ranking that extra-value the lifetime, cyclic lifetime, efficiency, and daily self-discharge, which are the most valuable characteristics for static storage, the top storage

Table 2.1: Characteristics of different ESS- adapted from [54, 55].

Electric Sorage	Nominal Voltage (V)	Self Discharge (%)	Energy Density (Wh/Kg)	Energy Density (Wh/l)	Power Density (W/l)	Efficiency η (%)	Lifetime (years)	Cyclic Lifetime (#)
PHS	-	very small	0.2 - 2	0.2 - 2	0.1 - 0.2	70 - 80	>50	>15k
CAES	-	very small	-	2 - 6	0.2 - 0.6	41 - 75	>25	>10k
Lead Acid	2	0.1 - 0.3	30 - 45	50 - 80	90 - 700	75 - 90	3 - 15	250 - 1.5k
NiCd	1.2	0.2 - 0.6	30 - 45	80 - 110	75 - 700	60 - 70	5 - 10	500 - 800
NiMH	1.2	-	40 - 80	80 - 200	500 - 3k	65 - 75	5 - 10	600 - 1.2k
Li-ion	3.7	0.1 - 0.3	60 - 200	200 - 400	1.3k - 10k	85 - 98	5 - 15	500 - 10k
Zinc air	1	-	130 - 300	130 - 200	50 - 100	50 - 70	>1	>1k
NaS	2.1	very small	100 - 250	150 - 300	120 - 160	70 - 85	10 - 15	2.5k - 4.5k
VRB	1.6	small	15 - 50	20 - 70	0.5 - 2	60 - 75	5 - 20	>10k
HFB	1.8	-	75 - 85	65	1 - 25	65 - 75	5 - 10	1k - 3.65k
Hydrogen	-	very small	33.33k	600 (200 bar)	2 - 20	34 - 44	10 -30	1k - 10k
EDLC	2.5	20 - 40	1 - 15	10 - 20	40k - 120k	85 - 98	4 - 12	10k - 100k

systems are the VRB and the LIB. From both storage systems, it was decided to select the VRB mostly for its design flexibility, but also because it is a safer solution and has promising advances that should be achieved in a near future. Additionally, and independently of the decision, supercapacitors will also be included in the thesis for their power density and response time.

To be noticed that if the storage system is composed by a VRB (or LIB) and EDLC then it is possible to have a ESS that supports high power peaks and can store/supply energy for a long time. In other words, the EDLC allows suppressing sudden load changes (due to its fast response time and power capability) giving time for the VRB to adjust properly and further compensate those changes. Such is particularly interesting when considering operation in islanding mode. Additionally, the VRB characteristics allow to dimension (and expand) the energy necessities in a straightforward manner.

CHAPTER 3

Phase-Locked Loop

The power converters require accurate measurements from the grid such as the three-phase voltage amplitude, frequency, and phase. The control loop is normally fully or partially performed as in the synchronous reference frame (SRF), where voltage estimation becomes even more critical as the phase estimation errors are propagated to the synchronous voltage and current measurements, through the Park transform. Additionally, methods like the droop control or virtual synchronous generator ones demand stable frequency measurement/estimation to achieve robust and proper power sharing. The phase-locked loop (PLL) is designed primarily to estimate the phase of the voltage fundamental frequency positive sequence, but it also allows to obtain a stable voltage amplitude and frequency, as it is discussed in this chapter.

There are several PLL algorithms presented in the literature, where the double second-order generalized integrator (DSOGI) is considered the best filtering method based on its robustness and design simplicity. Despite such advantages, there are different DSOGI implementations, with no clear advantages between them. Hence, in the chapter, implementations are compared through model simulation in *Matlab/Simulink* under a variety of grid conditions such as unbalanced phase voltages, high low-order harmonics distortion, frequency steps, phase jumps, and voltage sags. Following the simulation results, the three implementations identified with the overall best performance, are compared through an experimental setup for further validation with a voltage-source converter forming the grid. At the end of the chapter, it is presented a benchmark of the implementations, synthesized in a table for the aforementioned grid conditions. The benchmark allows choosing the most suitable DSOGI PLL for certain expected grid conditions. Since the different DSOGI implementations perform differently depending on each particular grid condition, the respective performance order of importance is weighted. Based on the benchmark results, and considering the characteristics of an island microgrid with high renewable energy penetration (weak-grid), it is identified the most appropriate DSOGI PLL implementation.

This chapter is separated into eight sections. In section 3.2 it is introduced the basic principle of work of the closed-loop PLL's based on the synchronous reference frame (SRF-PLL). The generation of the quadrature signal, its extension to form the double second-order generalized integrator, and the extraction of the positive and negative phases sequence are presented in section 3.3. In section 3.4 it is presented the complete structure of the PLL's for synchronization with the grid positive sequence and in section 3.5 the synchronization through the frequency-locked loop (FLL). Section 3.6 presents the simulation, experimental results and the benchmark table.

3.1 PLL Introduction

There are currently several techniques to achieve grid synchronization, though it is not possible to point to a single synchronization algorithm that can simultaneously be the most accurate, fast, robust and lightest, for every grid condition. Therefore it is naturally necessary to establish a compromise between different goal objectives or grid conditions before choosing a particular synchronization algorithm.

Accordingly with [65] there are two main methods to achieve grid synchronization: open-loop or close-loop. In an open-loop approach, the phase angle is directly estimated from a filtered signal. In the closed-loop, it may exist a filtering stage, but angle estimation is obtained through a closed-loop structure normally involving a PI or PID controller.

An open-loop and simple technique for grid synchronization is the zero cross-detection which allows synchronizing with the grid every instant that grid voltage crosses a reference zero. The synchronization is achieved by detecting the zero-cross events generating a rectangular waveform accordingly. The resulting waveform allows estimating the frequency and consequently the respective phase. Though phase feedback error is only possible during the zero-cross instants and for that reason, it presents phase tracking slow dynamics and it is susceptible to external interference's, leading to phase tracking errors [10, 66]. With this technique, it is only possible to guarantee zero phase error at every half period (for single phase systems). Additionally, if no filters are added, voltage harmonics or measurement noise may lead to undesired zero-crossing detection. There are several other open-loop approaches such as the use of filters in the $\alpha\beta$ frame and prior angle calculation through trigonometric relationship. Some of these filters are the Butterworth low-pass filter, space vector filter, adaptive notch filter, *etc.*. As an alternative to digital filters, it can be found methods that suggest the use of discrete Fourier transform, Kalman filters, or application of the least mean square [67, 68].

Another method, and the most common synchronization technique in grid-tied power converters, is a closed-loop approach known as the synchronous reference frame phase-locked loop (SRF-PLL). The SRF-PLL presents fast dynamics with a very low steady-state error in the absence of low order harmonics and three-phase balanced conditions [69]. Such assumptions are unrealistic in most real cases, especially when considering weak grids. Hence most of the advanced PLL algorithms consist in the application of techniques to extract the fundamental frequency positive sequence (FFPS) of the grid voltage and further phase tracking through the SRF-PLL [70–72].

In [71, 73] different PLL methods, including the DSOGI-based PLL, are compared and qualified where the DSOGI is highlighted as one of the most performant. Though it does not discriminate the performance of different DSOGI-based methods and it lacks numerical performance quantification.

To extract the FFPS the authors in [74] suggests considering a double synchronous reference frame: one rotating with positive frequency and another in opposite direction. A decoupling network is presented that allows the positive sequence extraction. Furthermore, a second-order low pass filter is applied at the output to reduce harmonics interference in the positive sequence synchronous voltage estimation.

Another method is based on the single-phase enhanced PLL (EPLL). In this method it is applied a quadrature signal generator based on the second-order generalized integrator (SOGI-QSG) to obtain a lagging 90° phase shift of the input signal, offering simultaneously filtering capability at frequencies beyond the filter centre frequency [75]. An extension of this method [76] consists in considering a double SOGI-QSG (DSOGI-QSG), *i.e.* two SOGI-QSG are used to obtain the direct and quadrature signals of the alpha and beta components respectively, for further positive sequence calculation. This method allows obtaining the positive sequence with intrinsic filtering capability. Since DSOGI-QSG centre frequency is adjusted accordingly with the PLL frequency, the DSOGI is a frequency-adaptive filter. Additionally, in [71] is shown that the DSOGI-PLL is equivalent to the DSRF-PLL under certain conditions, therefore the analysis on this thesis will disregard the second. The DSOGI-QSG can be applied with phase tracking (PLL) or frequency tracking, becoming a frequency-locked loop (FLL).

3.2 Synchronous reference frame phase-locked loop

The SRF-PLL is based on the *dq0* frame and it is illustrated in figure 3.1. The principle of operation consists of orienting the voltage vector in the *dq0* frame to be aligned with a reference phase of the three-phase voltage system. To achieve so, the quadrature component of the voltage in the *dq0* frame

is controlled to zero typically through a proportional-integral (PI) controller. It is important to notice that in the synchronous frame (*dq0* frame) all vectors rotating at synchronous speed are represented in steady-state by a constant direct and quadrature component. The output of the PI is further integrated to obtain the phase angle that is used as feedback to the calculation of the *dq0* transformation matrix. In steady-state, the PI output and the forward compensation represent the grid frequency ω'.

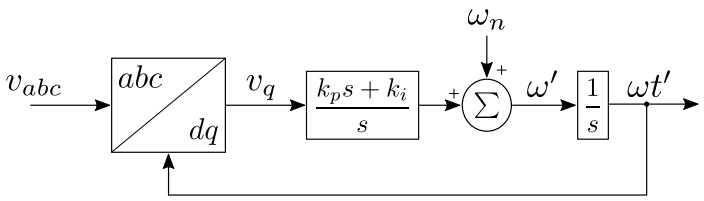


Figure 3.1: Block diagram of the SRF-PLL.

The Clarke and Park (3.1) transformation matrix, presented in figure 3.1, are in the power invariant form and aligned with the co-sine of phase v_a. Noteworthy that the zero component is disregarded since it does not influence the synchronization loop. Additionally, the PI gains k_p and k_i are tuned accordingly with [10] and synthesized in equations 3.2, where ω_c represents the filter natural (or controller) frequency, ζ the damping and E_g the grid peak voltage amplitude.

$$T_{abc\to\alpha\beta} = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}, \quad T_{\alpha\beta\to dq} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix} \tag{3.1}$$

$$\begin{cases} k_p = & \frac{2\omega_n \zeta}{E_g} \\ k_i = & \frac{E_g}{4\zeta^2} \end{cases} \tag{3.2}$$

3.3 Fundamental frequency positive sequence extraction

This section reviews the principle of operation of the SOGI filter, its extension to the DSOGI, and the decoupling network that allows extracting the positive and negative grid phase sequence.

3.3.1 Second-order generalized integrator- quadrature signal generator

The SOGI-QSG is based on a band-pass filter tuned at a centre frequency ω_0 and quality factor k $(= 1/Q)$. There are two main particularities on this filter: one is that it presents at the centre

frequency two outputs with unitary gain (the input signal with 0° and with 90° phase delay); the second is that allows to adapt the centre frequency. Hence, at the centre frequency, the SOGI-QSG generates the direct and quadrature signals of the input filtered signal. Such behaviour can be further understood by analysing the filter block diagram of figure 3.2, the transfer functions (3.3) and the respective bode plots as illustrated in figure 3.3.

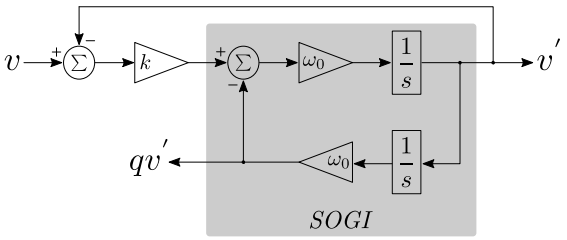


Figure 3.2: SOGI-QSG block diagram.

$$\begin{aligned} D(s) &= \frac{v'}{v}(s) = \frac{k\omega' s}{s^2 + k\omega' s + \omega'^2} \\ Q(s) &= \frac{qv'}{v}(s) = \frac{k\omega'^2}{s^2 + k\omega' s + \omega'^2} \end{aligned} \tag{3.3}$$

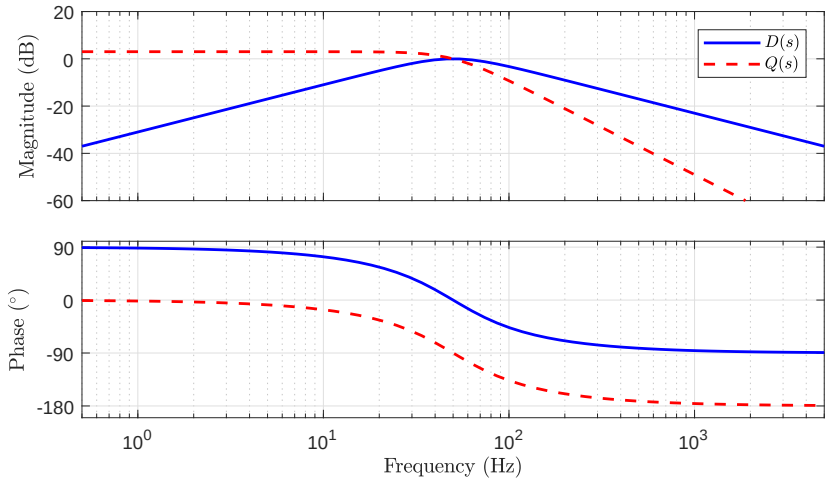


Figure 3.3: SOGI-QSG bode plot for a centre frequency of 50 Hz and a quality factor $k = \sqrt{2}$.

In figure 3.3 it can be noticed that at the centre frequency, the gain of both direct $D(s)$ and quadrature $Q(s)$ is unitary while the phase of $Q(s)$ is lagging 90°. Another interesting feature of this filter, highlighted in [76], is the fact that independently of the input signal frequency, the output qv' always lags 90° from v', therefore when the frequency of the input signal deviates from the centre frequency,

the filter output signals will differ only in magnitude.

The SOGI-QSG, as shown before, it allows to filter the input signal with an attenuation of $20\,dB/dec$ and simultaneously generate the direct and quadrature component of the filtered signal. Additionally, it is possible to ensure unitary gain if the filter centre frequency is properly adjusted.

3.3.2 Double SOGI-QSG and positive sequence extraction

The SOGI-QSG can be extended to extract the fundamental frequency of an unbalanced phase system. To achieve it, it is considered the symmetrical components method (3.4) to extract both positive and negative sequences of the unbalance three-phase system. As suggested in [75], the DSOGI consists in two SOGI-QSG (one for each component of the Clarke transform), which allows extracting the positive sequence of the three-phase voltage through the positive sequence calculator (PSC) (3.5), where qv_α and qv_β are obtained through two different SOGI-QSG's. In figure 3.4, it is represented the DSOGI-QSG block diagram.

$$\begin{matrix} v^+_{abc} = T_p v_{abc} \\ v^-_{abc} = T_n v_{abc} \end{matrix}, \quad T_p = \frac{1}{3}\begin{bmatrix} 1 & a & a^2 \\ a^2 & 1 & a \\ a & a^2 & 1 \end{bmatrix}, \quad T_n = \frac{1}{3}\begin{bmatrix} 1 & a^2 & a \\ a & 1 & a^2 \\ a^2 & a & 1 \end{bmatrix}, \quad a = e^{j\frac{2\pi}{3}} \tag{3.4}$$

$$\begin{aligned} v^+_{\alpha\beta} = \left[T_{\alpha\beta}\right] v^+_{abc} = \left[T_{\alpha\beta}\right]\left[T_p\right] v_{abc} = \left[T_{\alpha\beta}\right]\left[T_p\right]\left[T_{\alpha\beta}\right]^T v_{\alpha\beta} \Leftrightarrow \\ \Leftrightarrow v^+_{\alpha\beta} = \frac{1}{2}\begin{bmatrix} 1 & -q \\ q & 1 \end{bmatrix} v_{\alpha\beta}, \quad q = e^{-j\frac{\pi}{2}} \end{aligned} \tag{3.5}$$

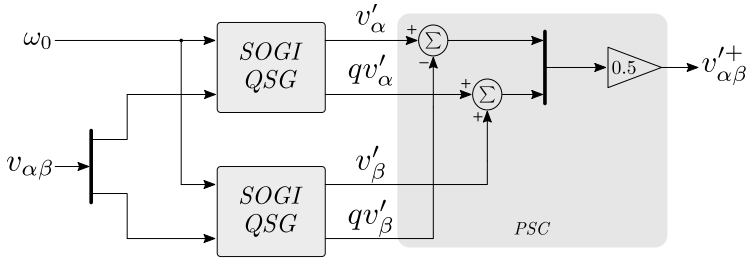


Figure 3.4: DSOGI-QSG block diagram.

As shown before it is possible to extract the FFPS of the three-phase voltages represented in the static orthogonal frame (Clarke). Furthermore, the same procedure can be applied to obtain the negative sequence (3.6) despite its omission in figure 3.4. It worth nothing to add that $v_{\alpha\beta}$ is obtained

directly from the three-phase voltage measurement, while ω_0 must be set or estimated accordingly with the grid conditions.

$$v^{-}_{\alpha\beta} = \frac{1}{2}\begin{bmatrix} 1 & q \\ -q & 1 \end{bmatrix} v_{\alpha\beta} \tag{3.6}$$

3.4 DSOGI based phase-locked loop

In previous sections, it was presented the base of the DSOGI filter and it was shown how it can be used for extraction of the three-phase voltage FFPS.

In the current section, it is discussed two methods for the filter centre frequency feedback: the DSOGI-PLL with a low pass filter in the frequency feedback (here simply called DSOGI-PLL) and the frequency-fixed DSOGI-PLL (FFDSOGI-PLL). Both algorithms consist of adding the SRF-PLL to the positive sequence obtained from the DSOGI-QSG, for frequency and phase estimation. The methods differ in how the DSOGI-QSG center frequency is adapted.

3.4.1 DSOGI-PLL

In the DSOGI-PLL, the estimated frequency of the SRF-PLL is added as a feedback path to the DSOGI filter centre frequency. Furthermore, to smooth the frequency feedback from the PLL estimated frequency transients, it is proposed to add a low-pass filter to the frequency feedback path. The estimated frequency is provided by the SRF-PLL as a result of the PI controller keeping the phase angle error to zero. During voltage transients, such as phase jumps, the frequency estimation spikes to bring the phase error back to zero, independently if the actual grid frequency changed or not. The added LPF attenuates the interference of such transients as well the normal ripple produced by the PI controller. This scheme is represented in figure 3.5, where the SRF-PLL estimated frequency ω'' is filtered by the LPF (ω') before being fed to the DSOGI-QSG. Hence, there are four tuneable parameters: DSOGI damping (k), SRF-PLL gains (kp, k_i), and the LPF cut-off frequency (ω_c).

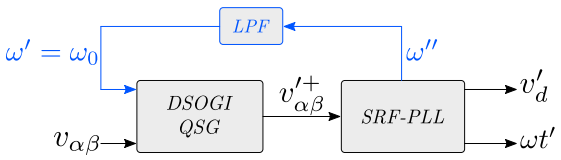


Figure 3.5: DSOGI-PLL with LPF block diagram.

3.4.2 FFDSOGI-PLL

A more recent approach, suggested in [77, 78], considers a SOGI filter with a fixed centre frequency ($\omega_0 = \omega_n$) for single-phase systems (FFSOGI). The method was further extended in [79] to a double SOGI becoming an FFDSOGI. Contrary to the DSOGI, the FFDSOGI operates with a fixed frequency (there is no frequency feedback path to the SOGI's). Instead, frequency deviances ($\omega' - \omega_0$) are further compensated in the filter output magnitude and phase. To achieve so, the authors present a linearized small-signal model of the DSOGI filter, considering small deviance's $|\omega_0^2 - \omega'^2| << k\omega'\omega_0$. Under these circumstances, deviance's can be compensated by adding a gain correction to the quadrature signal of both $\alpha\beta$ components SOGI's and adding an angle correction to the estimated angle of the SRF-PLL (3.7). These changes result in the schematic of figure 3.6, where grey areas highlight the amplitude and angle compensations. Comparing it with the previous method, the FFDSOGI-PLL has one less tuneable parameter (the LPF time constant), as it is suggested to extract the frequency from the PI error integral [77]. Noteworthy, that in steady-state the error is zero and the frequency is given by the PI error integrative component. Furthermore, without frequency filtering, the estimated frequency oscillations are feed-forward to both frequency and angle compensations. In the thesis, it is proposed to filter the estimated frequency as in the case of the DSOGI-PLL, before feeding it to the compensation blocks, as shown in figure 3.7. The option of adding the LPF, instead of using the PI error integral output, allows decoupling the synchronization dynamics (angle) from the frequency estimation. With this change, the FFSDOGI-PLL and DSOGI-PLL present the same number of tuneable parameters, tuned with the same parameters for a fair comparison of both methods.

$$\begin{cases} qv' = \dfrac{\omega'}{\omega_0} qv' \\ \omega t' = \omega t' + \delta \\ \delta = \dfrac{\omega'^2 - \omega_0^2}{k\omega'\omega_0} \end{cases} \tag{3.7}$$

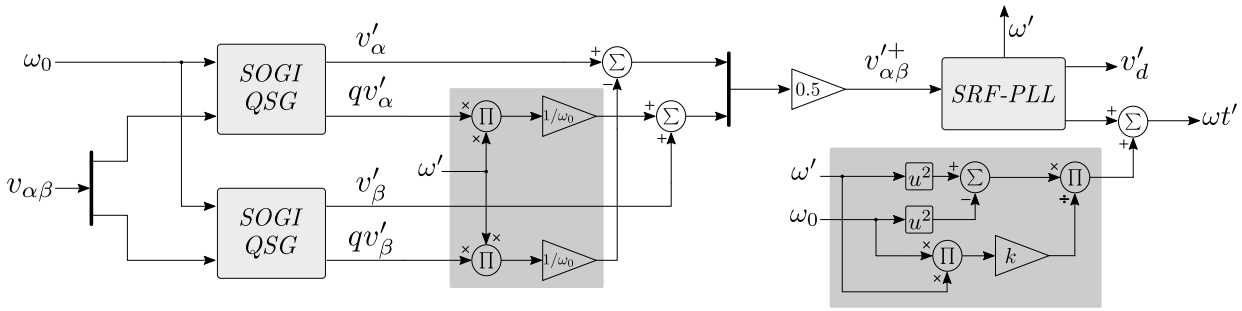


Figure 3.6: FFDSOGI-PLL block diagram.

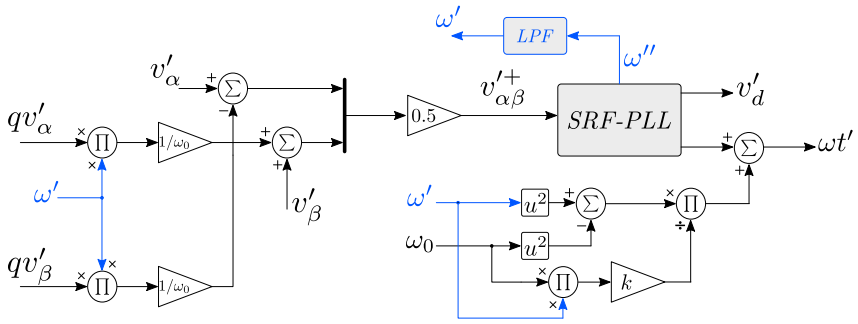


Figure 3.7: FFDSOGI with frequency LPF.

3.5 DSOGI based frequency-locked loop

Another approach to adapt the DSOGI-QSG centre frequency ω_0, is proposed and well described in [80]. The author suggests an extension of the EPLL frequency adaptive structure to be applied in the SOGI-QSG. Such modifications result in the block diagram presented in figure 3.8, where ω_N is the nominal grid frequency, and the grey area represents the gain normalization GN (3.9). The input error $\varepsilon_{\alpha\beta}$ is given by (3.8), considering the SOGI-QSG nomenclature shown in figure 3.2). To highlight that the $\sum \varepsilon_{\alpha\beta}$ in negative for $\omega' < \omega$, zero for $\omega' = \omega$ and positive for $\omega' > \omega$. Hence, it is possible to obtain zero steady-state error ($\omega' = \omega$) with an error integral and gain $-\Gamma$.

$$\begin{cases} \varepsilon_\alpha = (v_\alpha - v'_\alpha) q v_\alpha \\ \varepsilon_\beta = (v_\beta - v'_\beta) q v_\beta \end{cases} \tag{3.8}$$

$$GN = \frac{k\omega'}{(v'^+_\alpha)^2 + (v'^+_\beta)^2} \tag{3.9}$$

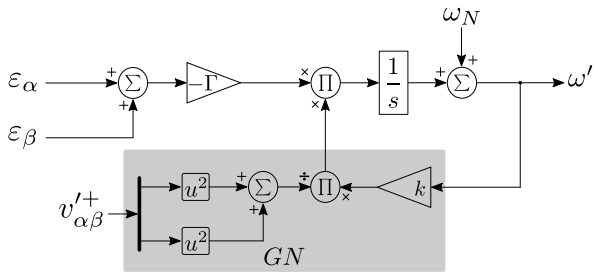


Figure 3.8: FLL block diagram.

Taking into account the FLL block diagram of figure 3.8, it can be noticed that the FLL has only one tuning parameter Γ, since k is the DSOGI-QSG filter quality factor and ω_N is a known constant. Furthermore, it is shown in [80] that with the gain normalization, the FLL presents a first-order transfer function (3.10) which allows tuning Γ accordingly with the desired system response settling time t_s.

$$\frac{\omega'}{\omega} = \frac{\Gamma}{s+\Gamma} \Rightarrow \Gamma \approx \frac{5}{t_s} \tag{3.10}$$

In [81] it is presented an improved frequency locked-loop (IFLL), that differs from the previous FLL, in a slight change on how the gain is normalized. Instead of considering only the positive sequence, negative sequence is also considered (3.11). Such modification only improves the method, when the negative sequence becomes significant compared to the positive sequence (very high unbalancing). Additionally, the DSOGI-FLL (or the DSOGI-IFLL) has only two tuneable parameters: the DSOGI-QSG damping k and the FLL gain Γ.

$$GN = \frac{k\omega'}{(v'^{+}_{\alpha})^2 + (v'^{+}_{\beta})^2 + (v'^{-}_{\alpha})^2 + (v'^{-}_{\beta})^2} \tag{3.11}$$

To compare the synchronization of both PLL and FLL, it is suggested to add a phase estimation stage to the previously discussed FLL scheme. To achieve so, it is suggested to use the FFPS ($v'^{+}_{\alpha\beta}$) filtered by the DSOGI-FLL to estimate the phase angle. Three different approaches were considered: zero-cross detection, SRF-PLL, and arc-tangent function. To be noticed that, contrary to the PLL schemes, in the FLL both frequency and phase are tracked independently despite the phase tracking accuracy be dependent on the FLL performance.

3.5.1 DSOGI-FLL with zero-cross detection

The zero-cross detection method employed here consists of integrating the frequency estimated by the FLL, but with an angle reset at every zero-cross detected, *i.e.* when v'^{+}_{α} or v'^{+}_{β} crosses zero the frequency integral is reset to the known angle. This way it is possible to correct the estimated phase four times per period. Every time a zero-cross occurs, a flag is triggered ($\delta_{tr,\alpha}$ or $\delta_{tr,\beta}$) and feeds into a lookup table (LUT), to obtain the respective reset angle value accordingly with table 3.1. Though it only allows at synchronizing during four instants per wave period, this method is simple and with low processing demand, though it may lead to significant phase deviations during transients. This method does not add tuneable parameters to the DSOGI-FLL.

Table 3.1: Zero-cross detection: angle reset LUT.

	$v'^{+}_{\alpha} > v'^{+}_{\beta}$	$v'^{+}_{\alpha} < v'^{+}_{\beta}$
$\delta_{tr,\alpha} > 0$	$\frac{3\pi}{2}$	$\frac{\pi}{2}$
$\delta_{tr,\beta} > 0$	0	π

3.5.2 DSOGI-FLL with SRF-PLL

The SRF-PLL can be added to the DSOGI-FLL to further estimate the phase frequency. Different from the PLL methods, in the FLL the PI dynamics of the SRF-PLL does not influence the positive sequence extraction since the centre frequency feedback of the DSOGI-FLL does not depend on the PI but in the FLL block diagram instead.

This scheme is here called DSOGI frequency and phase-locked loop (DSOGI-FPLL). The method adds two tuneable parameters to the original DSOGI-FLL (kp and ki), resulting in a total of four tuneable parameters.

3.5.3 DSOGI-FLL with atan2

The last considered method consists in calculate the arc-tangent of $v'^{+}_{\alpha\beta}$ and obtain the respective angle at any time instant. To reduce the processing burden associated to the typical arc-tangent methods, the fast arc-tangent suggested in [82] is employed. The proposed function is implemented through a LUT (or array) with limited angle representation, *i.e.* $\omega t' = \arctan(u) \ \wedge u \in [0,1]$ or $\omega t' \in [0, \pi/4]$.

To extend its operation for the four quadrants, the functional properties (3.12) and (3.13) are considered. The resulting flowchart is illustrated in figure 3.9 where γ is a scaling factor for the output angle representation, *i.e.* for $\omega t \in [-\pi, \pi] \rightarrow \gamma = 0$ and for $\omega t \in [0, 2\pi] \rightarrow \gamma = 2\pi$. To avoid extending the LUT size, it is considered that the table is composed by 101 entries, corresponding to the arctan function of interval $[0, 1]$. Hence the integer part of the scaled input value, $k = int(u * 100)$, corresponds directly to the desired (or neighbour) position in the LUT, considering the presented mapping. Additionally, a linear relation is considered between every two consecutive values of the LUT, therefore the output value is calculated taking into account a linear interpolation (3.14). It worth nothing to add, that this method do not require any additional tuning parameter.

$$\begin{cases} \arctan(-u) = -\arctan(u) \\ \arctan(u) + \arctan\left(\frac{1}{u}\right) = \frac{\pi}{2}, \quad u > 0 \\ \arctan(u) + \arctan\left(\frac{1}{u}\right) = -\frac{\pi}{2}, \quad u < 0 \end{cases} \tag{3.12}$$

$$\text{atan2}(y,x) = \begin{cases} \arctan(\frac{y}{x}), \quad x > 0 \\ \pi + \arctan(\frac{y}{x}), \quad y \geq 0, x < 0 \\ -\pi + \arctan(\frac{y}{x}), \quad y < 0, x < 0 \\ \frac{\pi}{2}, \quad y > 0, x = 0 \\ -\frac{\pi}{2}, \quad y < 0, x = 0 \\ \text{NaN}, \quad y = 0, x = 0 \end{cases} \tag{3.13}$$

$$\begin{cases} k = int(u * 100) \\ \text{atan2LUT}(u) = \text{LUT}[k] + (u * 100 - k) * (\text{LUT}[k+1] - \text{LUT}[k]) \end{cases} \tag{3.14}$$

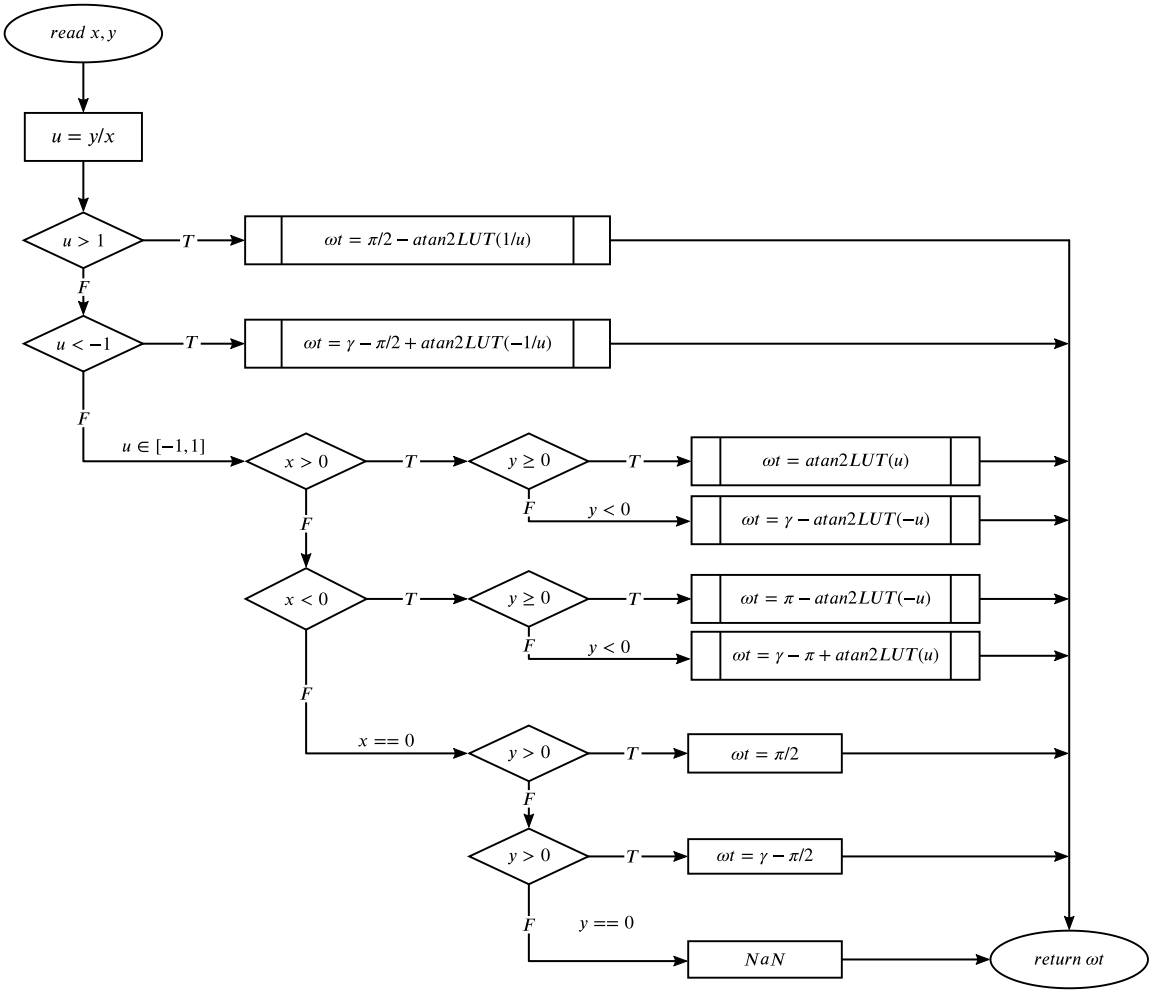


Figure 3.9: Flow chart of the fast atan2 function.

3.6 Results and discussion

To compare the different SOGI-based PLL performance under severe grid conditions of a weak grid, several simulations are performed in *Matlab/Simulink*. Furthermore, all aforementioned methods were implemented in the discrete-time domain with a sampling rate at 10 kHz, to emulate the micro-controller behaviour. Discretization was performed considering the forward Euler integration method.

The performed tests are divided into three different subgroups: unbalancing and harmonics (test #1), frequency and phase jumps (test #2), and voltage sags (test #3). Although, in the last two, harmonics and unbalancing are also considered but with a smaller impact. In table 3.3 it is shown the harmonic content considered in the different tests as a percentage of the FFPS voltage.

The grid voltage is generated directly from pre-defined positive and negative sequences, while

harmonics are posteriorly added. Hence at any instant, it is possible to know the exact frequency, phase, and magnitude of fundamental positive (and negative) sequence and harmonics magnitude.

Additionally, it is considered that the PLL is locked when the estimated frequency reaches steady-state. Therefore if both FLL and PLL dynamic response presents the same frequency settling time, it is possible to carry a fair comparison between methods. Hence, PI was tuned (3.2) considering $\omega_c = 314\ rad/s$ and $\zeta = 1/\sqrt{2}$, while the FLL gain was tuned (3.10) with $t_s = 0.1\ s$. The SOGI damping, in all different methods, was set as $k = \sqrt{2}$. The tuned gains are summarized in table 3.2.

Table 3.2: Tuned gains.

k_p	k_i	ω_c	Γ	k
1.37	163	78.5	40	$\sqrt{2}$

Table 3.3: Harmonics magnitude ($\%V^+$).

h	Highly polluted [81] (Test #1)	Limits in EN 50160 [83] (Tests #2 and #3)
5^{th}	20 %	6 %
7^{th}	15 %	5 %
11^{th}	10 %	3.5 %
13^th	8 %	3 %

3.6.1 Test #1- Unbalancing and harmonics

This test considers balanced three phases (positive sequence only) at 50 Hz with all methods already in steady-state at the simulation start. Unbalancing is achieved by injecting a negative sequence component, followed by harmonics with an amplitude as presented in table 3.3. Moreover, for the phase estimation, results in this test are first applied to the FLL (DSOGI-IFLL) and further compared with the PLL (DSOGI-PLL and FFDSOGI-PLL).

The analysis of the three-phase voltages are illustrated in figure 3.10, where t_1 to t_4 are the time instants that mark the added changes, to the subsequent conditions listed in table 3.4. The estimated frequency ω' and the respective errors ($\omega - \omega'$) are illustrated in figures 3.11 and 3.12 respectively. In figure 3.11 it can be noticed that all methods remain near the nominal frequency with exception of the SRF-PLL. Its performance is significantly poor when facing unbalanced conditions and further deteriorates when high low-order harmonics are present in the three-phase voltage. For these reasons the following analysis disregards the SRF-PLL and justifies the need for methods capable of extracting the FFPS.

Table 3.4: Introduced voltage unbalancing and harmonics during test #1.

$t = 0$	Positive sequence only with $v^{+}_{\alpha\beta} = [325\ 0]\ V$ (balanced three-phase)
t_1	Negative sequence is added with $v^{-}_{\alpha\beta} = [25\ 12]\ V$
t_2	Injection of the 5^{th} and 7^{th} order harmonics (highly polluted)
t_3	Injection of the 11^{th} and 13^{th} order harmonics (highly polluted)
t_4	Negative sequence is changed to $v^{-}_{\alpha\beta} = [100\ 0]\ V$

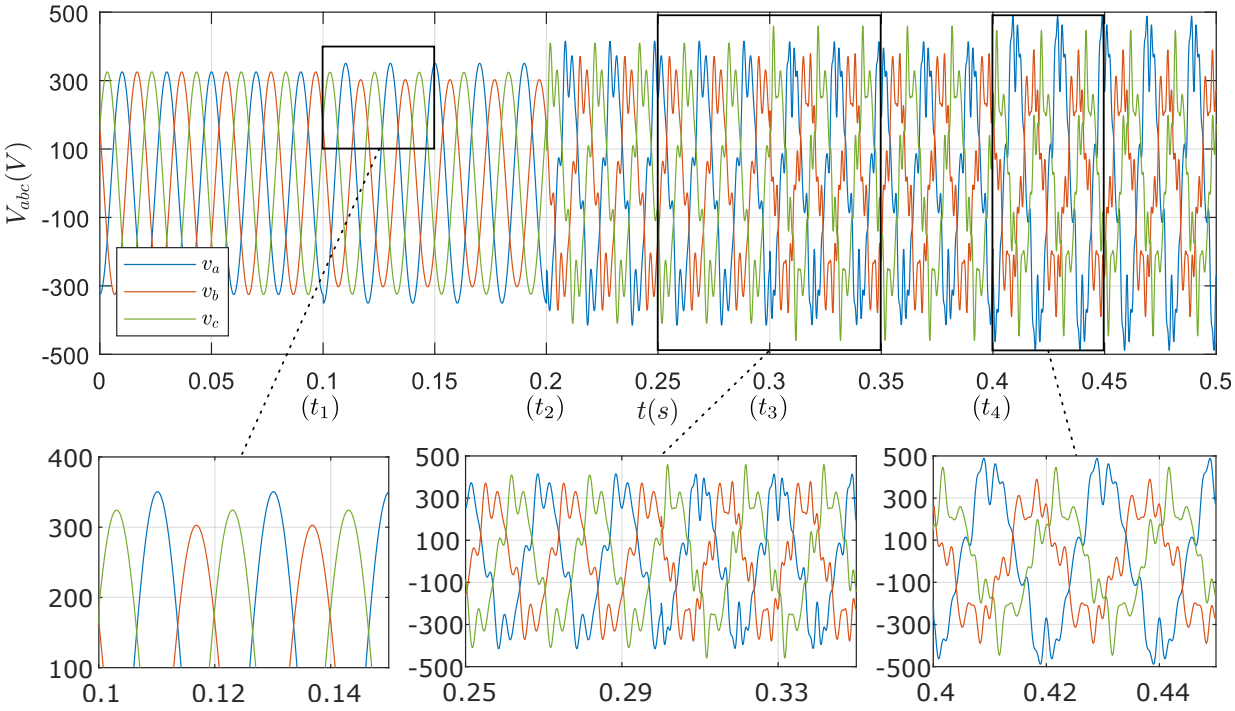


Figure 3.10: Three-phase voltage and the respective changes introduced during test #1.

In figure 3.12 it is noticeable that the DSOGI and FFDSOGI (PLL) presents similar behaviour, both with lower estimated frequency steady-state oscillations when compared with the FLL methods. Furthermore, both FLL and IFLL perform very similarly, mostly until t_4, where the negative sequence is reduced. After t_4, unbalancing is more noticeable and the IFLL presents lower oscillations than the FLL, though such difference may be neglected. To allow a quantification analysis of the results, in table 3.5 it is presented the root mean square error (RMSE) as a measure of the error oscillations, and the mean error (ME) as its DC value, during steady-state stages. In table 3.5 $T_N = 0.02\ s$ and refers to the FFPS voltage waveform time period.

Analysing data from table 3.5, it can be noticed that under ideal conditions $t = [0;\ t_1]$ the FLL and

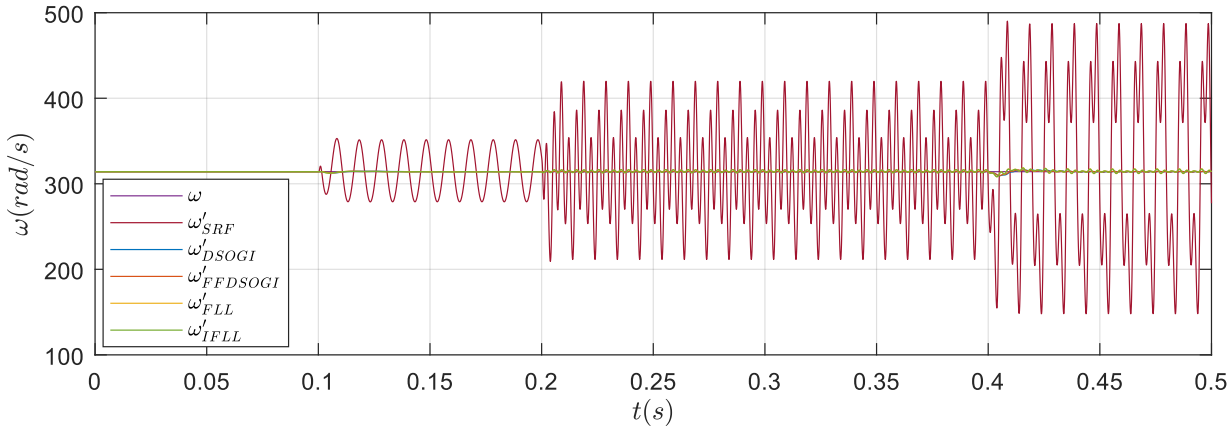


Figure 3.11: Estimated frequency for the different methods during test #1.

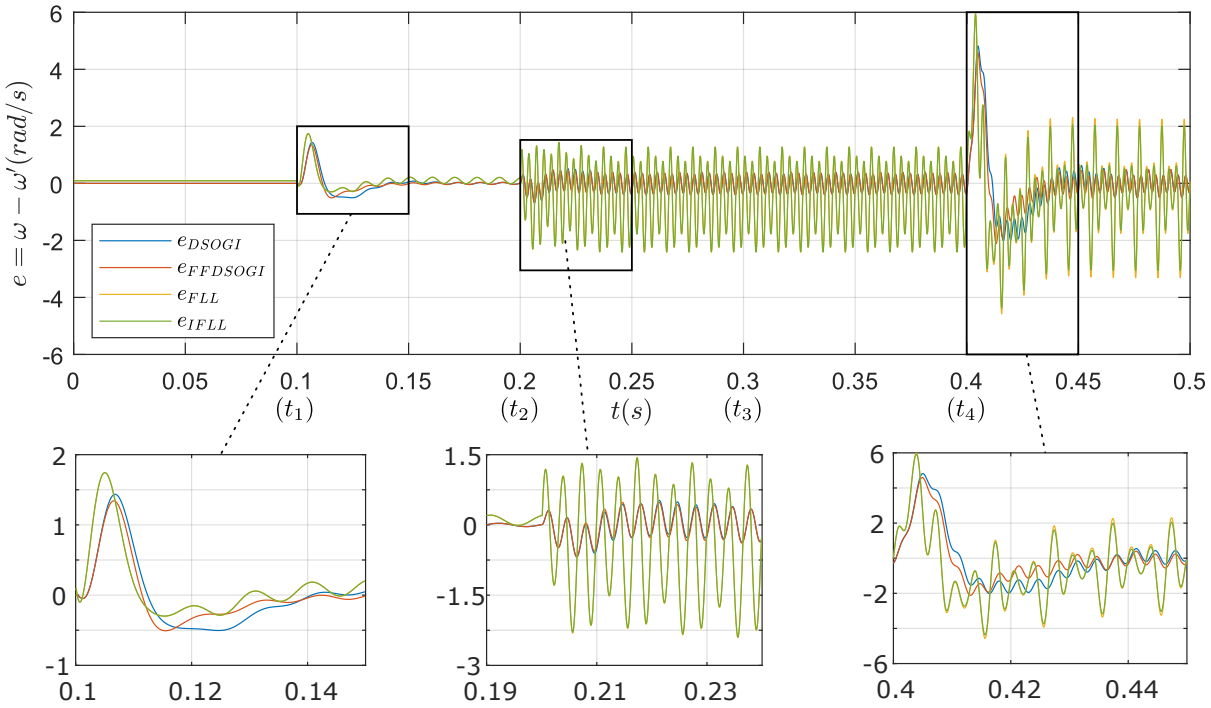


Figure 3.12: Estimated frequency errors for the different methods during test #1.

IFLL present an higher steady-state error (ME) when compared with the DSOGI based PLL structures. Though in such conditions all methods perform very well. With the introduction of the three-phase unbalancing and harmonics, oscillations are more noticeable in the FLL methods than in the PLL. An interesting behaviour of the FLL methods is in the change of the steady-state frequency ME with the changes in grid conditions. Observing the integral error of the FLL, it is concluded that the integral error gain is high enough to guarantee zero steady-state error, which indicates that the small ME is

Table 3.5: Steady-state estimated frequency RMSE and ME obtained during test #1.

	SRF		*DSOGI*		*FFDSOGI*		*FLL*		*IFLL*	
	RMSE	*ME*	*RMSE*	*ME*	*RMSE*	*ME*	*RMSE*	*ME*	*RMSE*	*ME*
$t_1 - 2T_N \Rightarrow t_1$	8.3×10^{-13}	1.8×10^{-9}	1.1×10^{-10}	1.8×10^{-9}	1.2×10^{-10}	1.9×10^{-9}	4.9×10^{-14}	90×10^{-3}	5.2×10^{-14}	90×10^{-3}
$t_2 - 2T_N \Rightarrow t_2$	26	-54×10^{-3}	27×10^{-3}	6.1×10^{-4}	25×10^{-3}	-2.5×10^{-3}	78×10^{-3}	0.10	78×10^{-3}	0.10
$t_3 - 2T_N \Rightarrow t_3$	56	-2.5×10^{-3}	0.26	-7.2×10^{-3}	0.26	-6.5×10^{-3}	1.1	-0.56	1.1	-0.56
$t_4 - 2T_N \Rightarrow t_4$	56	-2.5×10^{-3}	0.26	-7.1×10^{-3}	0.26	-7.2×10^{-3}	1.1	-0.56	1.1	-0.56
$t_5 - 2T_N \Rightarrow t_5$	105	33×10^{-3}	0.27	-9.0×10^{-3}	0.27	-14×10^{-3}	1.3	-0.40	1.2	-0.40

caused by the FLL structure, particularly in the way that the error $\varepsilon_{\alpha\beta}$ is generated for adapting the frequency.

Since both FLL and IFLL performance are similar, only the IFLL is considered in the following performance evaluation.

In figure 3.13 it is presented the errors obtained for the phase estimation $\omega t'$. To be noticed that the different methods presented in section 3.5 for phase estimation, are applied to the IFLL (FLL is not shown since it presents similar results). Furthermore, the RMSE and ME were obtained under steady-state conditions for the same intervals of table 3.5 and are shown in table 3.6.

Table 3.6: Steady-state estimated phase angle RMSE and ME obtained during test #1.

	IFLL − atan2		*IFLL − ZCD*		*IFLL − SRF*		*DSOGI*		*FFDSOGI*	
	RMSE	*ME*	*RMSE*	*ME*	*RMSE*	*ME*	*RMSE*	*ME*	*RMSE*	*ME*
$t_1 - 2T_N \Rightarrow t_1$	4.4×10^{-6}	8.2×10^{-3}	1.3×10^{-4}	2.3×10^{-4}	8.3×10^{-15}	8.2×10^{-3}	9.0×10^{-13}	7.8×10^{-3}	5.8×10^{-13}	7.8×10^{-3}
$t_2 - 2T_N \Rightarrow t_2$	5.0×10^{-4}	8.2×10^{-3}	2.4×10^{-4}	2.6×10^{-4}	4.6×10^{-4}	8.2×10^{-3}	3.4×10^{-4}	7.8×10^{-3}	4.4×10^{-4}	7.8×10^{-3}
$t_3 - 2T_N \Rightarrow t_3$	13×10^{-3}	5.6×10^{-3}	17×10^{-3}	-18×10^{-3}	4.0×10^{-3}	5.3×10^{-3}	3.3×10^{-3}	7.9×10^{-3}	4.5×10^{-3}	7.8×10^{-3}
$t_4 - 2T_N \Rightarrow t_4$	13×10^{-3}	5.6×10^{-3}	17×10^{-3}	-18×10^{-3}	4.0×10^{-3}	5.3×10^{-3}	3.3×10^{-3}	7.9×10^{-3}	4.5×10^{-3}	7.8×10^{-3}
$t_5 - 2T_N \Rightarrow t_5$	13×10^{-3}	6.1×10^{-3}	17×10^{-3}	-18×10^{-3}	4.2×10^{-3}	5.7×10^{-3}	3.5×10^{-3}	7.9×10^{-3}	4.7×10^{-3}	7.8×10^{-3}

Through analysis of figure 3.13, it is clear that the IFLL-SRF results in the most stable angle estimation when compared with the IFLL-atan2 and IFLL-ZCD. Hence, the non-linearity on phase reset at every grid period quarter (IFLL-ZCD) and the high oscillations in the IFLL-atan2, indicates that the $v^+_{\alpha\beta}$ components resulting from the DSOGI-FLL are not strictly sinusoidal and neither present a phase difference of exactly 90°. Such distortions are introduced mostly by the low order harmonics, as already concluded before in the frequency analysis. In [69,81] it is suggested to add multiple DSOGIs tuned at different harmonic frequencies for the elimination of the respective low order harmonics, though such extension is not explored in this thesis.

The PLL methods perform very similarly as expected. Though the DSOGI-PLL outperforms all

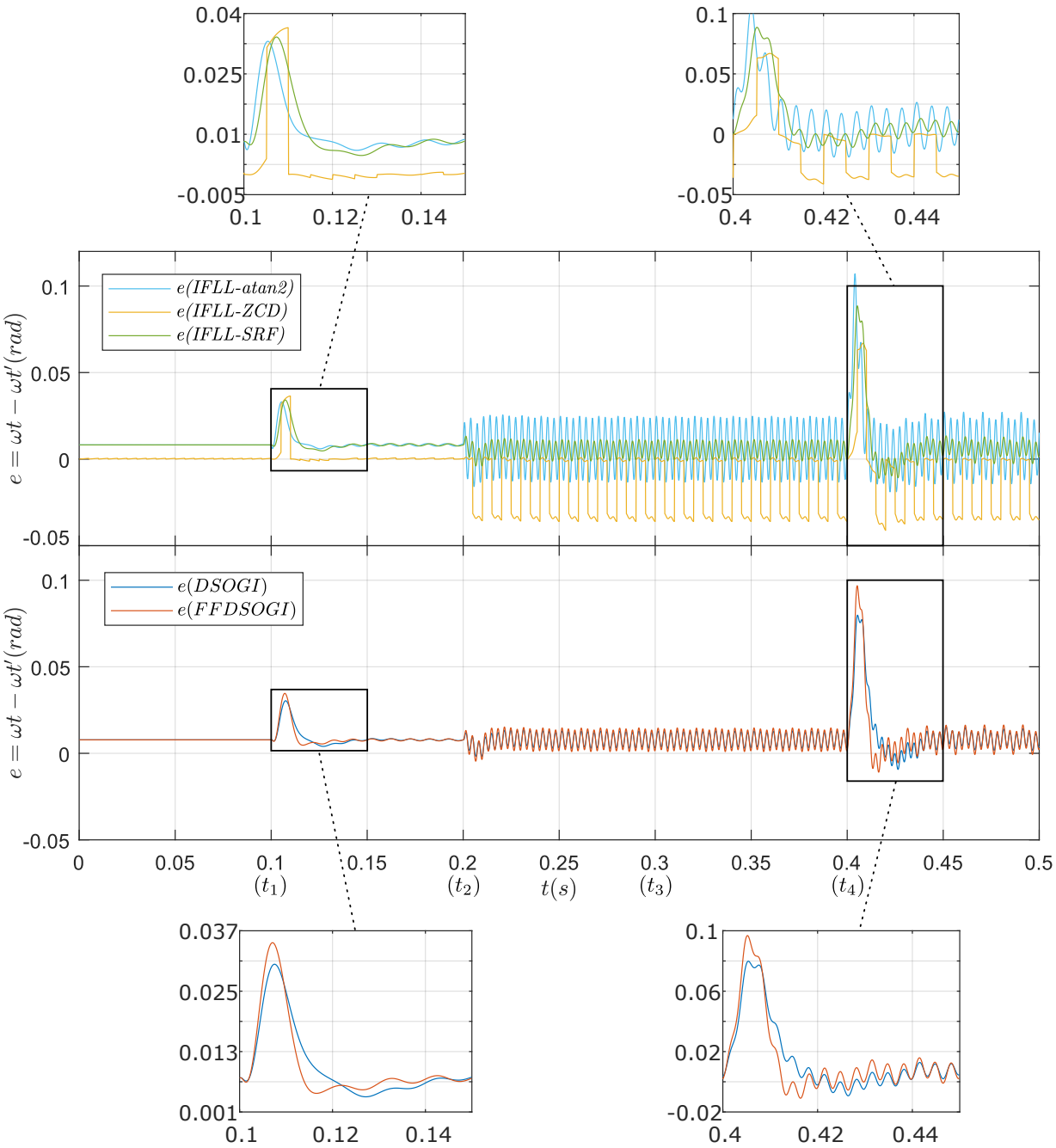


Figure 3.13: Estimated phase errors for the different methods during test #1. In top figure it is shown the different phase estimation methods applied to the IFLL, and in the bottom estimated phase by the PLL methods.

the other methods in terms of overall performance, as it can be concluded by analysing the *RMSE* during steady-states, presented in table 3.6.

For the test #1 conditions, it can be concluded that the performance of both PLL methods is superior to the FLL. Where the FFDSOGI presents the best results in frequency estimation and the DSOGI in the phase angle, although both perform very similarly in both estimations. Despite the differences, as far as harmonics and unbalancing conditions are considered, all methods based in the SOGI-QSG presented a great performance under unbalancing conditions and good harmonics filtering capability.

To qualify the obtained results, for the different methods during test #1, it is considered only the steady-state oscillations (RMSE). During the test #1, the ME remains practically constant for both frequency and phase estimations, being more meaningful to analyse the ME with the results obtained during test #2. Furthermore, the RMSE is applied to the frequency estimation, since in the case of phase angle estimation, the differences can be disregarded. Classification is shown in table 3.12, where the mark is defined by the averaged ratio of the method RMSE by the minimum RMSE obtained for the different grid distortion intervals.

3.6.2 Test #2- Frequency steps and phase jump

Test #2 consists of applying frequency steps followed by a phase jump. The test, as already stated before, also considers unbalancing and low-order harmonics accordingly with table 3.3. The frequency and phase profile is equally applied to the three phases and is summarized in table 3.7.

Table 3.7: Frequency steps and phase jump applied during test #2.

$t = 0$	Nominal frequency of 50 Hz
t_1	Frequency step change to 45 Hz
t_2	Frequency step change to 55 Hz
t_3	Frequency step change back to 50 Hz
t_4	Phase jump of $\pi/4$ rad

The results obtained for the estimated frequency and respective frequency errors, during test #2, are shown in figure 3.14.

In figure 3.14 the steady-state of the different methods is coherent with the results obtained during test #1 and therefore it will not be analysed again. The frequency steps at (t_1) and (t_3) are the same $(\Delta\omega = 5\ Hz)$ and it can be seen that the transient response of the FFDSOGI and IFLL is very similar both in terms of overshoot and settling time. During this step, the DSOGI takes almost 20 *ms* more

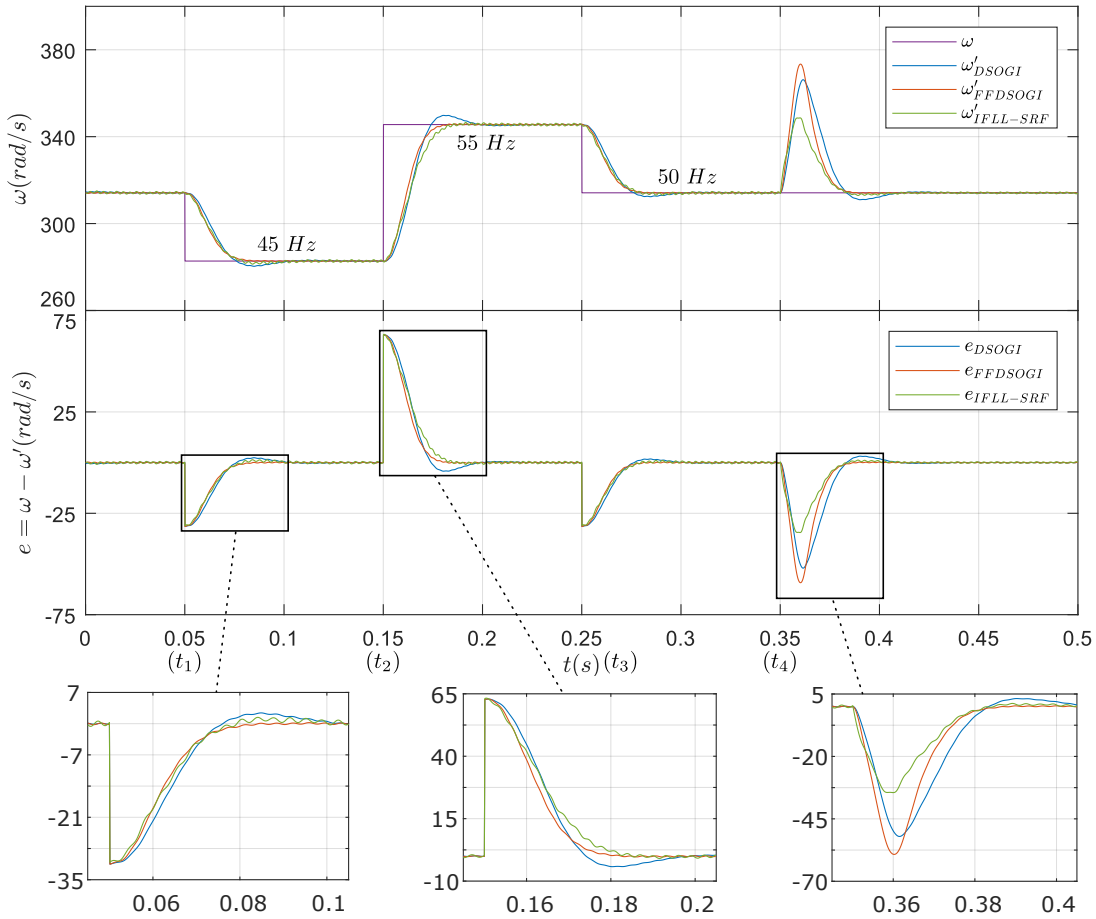


Figure 3.14: Estimated frequency errors for the different methods during test #2.

to reach the steady state. At (t_2) occurs the biggest frequency step ($\Delta\omega = 10\ Hz$) and during this transient, the FFDSOGI presents a slight fester response. Finally at (t_4) occurs the 45° phase shift and the results in terms of response time follow the same behaviour as during (t_1). Nevertheless, the IFLL presents significantly less overshoot than other methods, which indicates that the FLL scheme is less sensitive to phase jumps when compared with the PLL.

To evaluate the performance in terms of phase estimation, the results in figure 3.15 is presented. In terms of phase estimation, during frequency step changes, the differences are more obvious, where the FFDSOGI performance is better than the others, both in terms of overshoot and settling time. The FFDSOGI reaches its steady-state in $\approx 0.03\ s$ with the following taking $0.02\ s$ more. Still, during the phase jump, the FLL presents less overshoot and takes the same time to reach the steady-state, which corroborates with the estimated frequency results.

In tables 3.8 and 3.9, results are summarized for the methods that presented the best performance

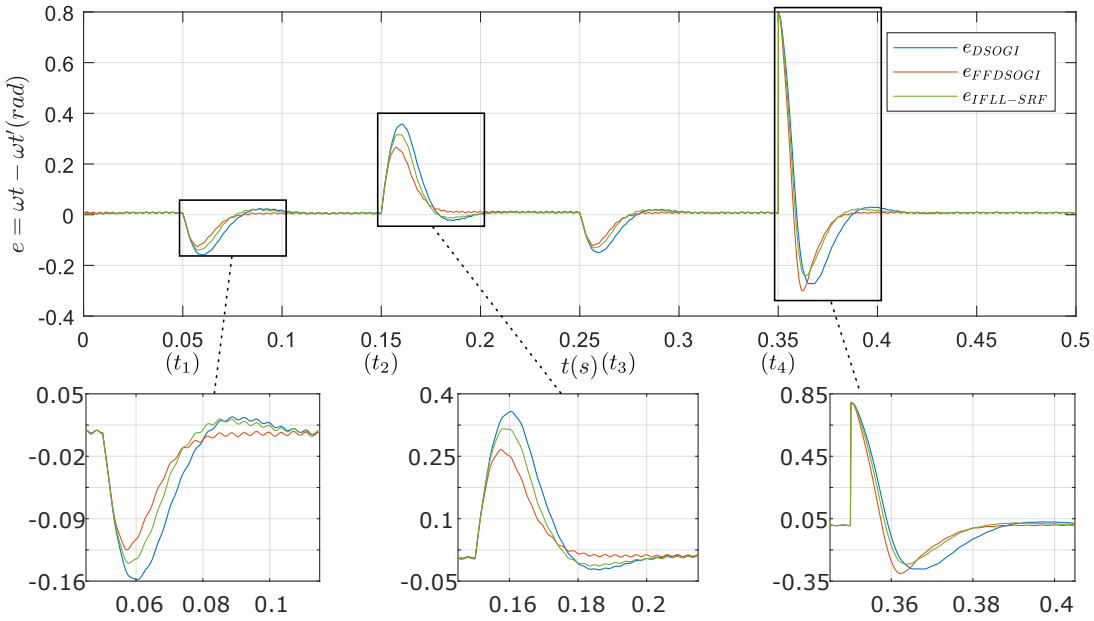


Figure 3.15: Estimated phase errors for the different methods during test #2.

during test #2. In table 3.8, *OS* is the overshoot and t_s the settling time. In table 3.9 it is shown the ME for estimation of steady state frequency and phase, at different grid frequencies.

Table 3.8: Results summary obtained for test #2- Overshoot (OS) and settling time (t_s).

		DSOGI			*FFDSOGI*			*IFLL*		
		$\Delta\omega = 5\ Hz$	$\Delta\omega = 10\ Hz$	$\Delta\omega t = \pi/4$	$\Delta\omega = 5\ Hz$	$\Delta\omega = 10\ Hz$	$\Delta\omega t = \pi/4$	$\Delta\omega = 5\ Hz$	$\Delta\omega = 10\ Hz$	$\Delta\omega t = \pi/4$
ω'	$t_s(ms)$	45.0	45.0	45.0	30.0	30.0	30.0	30.0	33.0	33.0
	OS (rad/s)	31.4	62.8	52.0	31.4	62.8	59.0	31.4	62.8	34.0
$\omega t'$	$t_s(ms)$	60.0	60.0	65.0	38.0	38.0	40.0	60.0	60.0	65.0
	OS (rad)	0.16	0.36	0.79	0.13	0.27	0.79	0.14	0.32	0.79

Table 3.9: Results summary obtained for test #2- steady state ME.

		DSOGI			*FFDSOGI*			*IFLL*		
		$\omega = 45\ Hz$	$\omega = 55\ Hz$	$\omega = 50\ Hz$	$\omega = 45\ Hz$	$\omega = 55\ Hz$	$\omega = 50\ Hz$	$\omega = 45\ Hz$	$\omega = 55\ Hz$	$\omega = 50\ Hz$
ω'	*ME (rad/s)*	$4.8m$	$25m$	$0.3m$	$14m$	$6.4m$	$0.9m$	$22m$	$46m$	$46m$
$\omega t'$	*ME (rad/s)*	$6.8m$	$8.4m$	$7.8m$	$5.0m$	$11m$	$7.8m$	$6.9m$	$8.8m$	$8.0m$

Based on the results summarized in tables 3.8 and 3.9, classification table 3.12 is presented. The classification is based in the average ratio of each evaluated value with the minimum value obtained during that test, for the different conditions. Hence the best result corresponds to the smaller classification value 1.0.

3.6.3 Test #3- Voltage sags

During test #3 the grid frequency is kept constant (nominal value), while harmonics and unbalancing are the same applied in the test #2 (tables 3.3 and 3.4). Hence, the changes applied during the present test focus on the voltage amplitude, *i.e.* the sags are applied to the symmetrical voltage components and also harmonics.

The voltage sags periods and amplitudes are summarized in table 3.10 and the resulting grid voltage waveforms are shown in figure 3.16.

Table 3.10: Voltage sags applied during test #3.

$t = 0$	No voltage sag
t_1	Voltage sag of 30% with 75 *ms* duration
t_2	Voltage sag of 60% with 150 *ms* duration
t_3	Voltage sag of 90% (permanent)

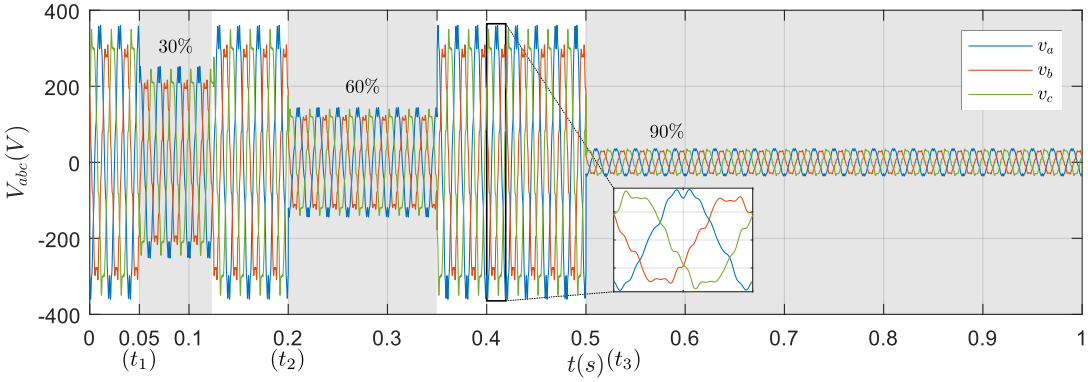


Figure 3.16: Voltage sags applied during test #3.

The errors associated with frequency and phase estimations, obtained during test #3, are shown in figure 3.17, where the top plots refer to the frequency and the bottom ones to the phase.

Analysing the frequency dynamic response of figure 3.17 allows concluding that all methods respond very similarly to the 30% voltage sag (t_1). During the 60% voltage sag (at t_2), both FFDSOGI and IFLL-SRF also perform with the same settling time, despite the first response with larger oscillation. In the same interval, it is noticeable the weaker performance of the DSOGI, which takes ≈ 20 *ms* more to reach steady-state. The 90% voltage sag is the perturbation with a higher impact of all the analysed tests, where it can be seen the long settling time of both FFDSOGI and DSOGI, with both

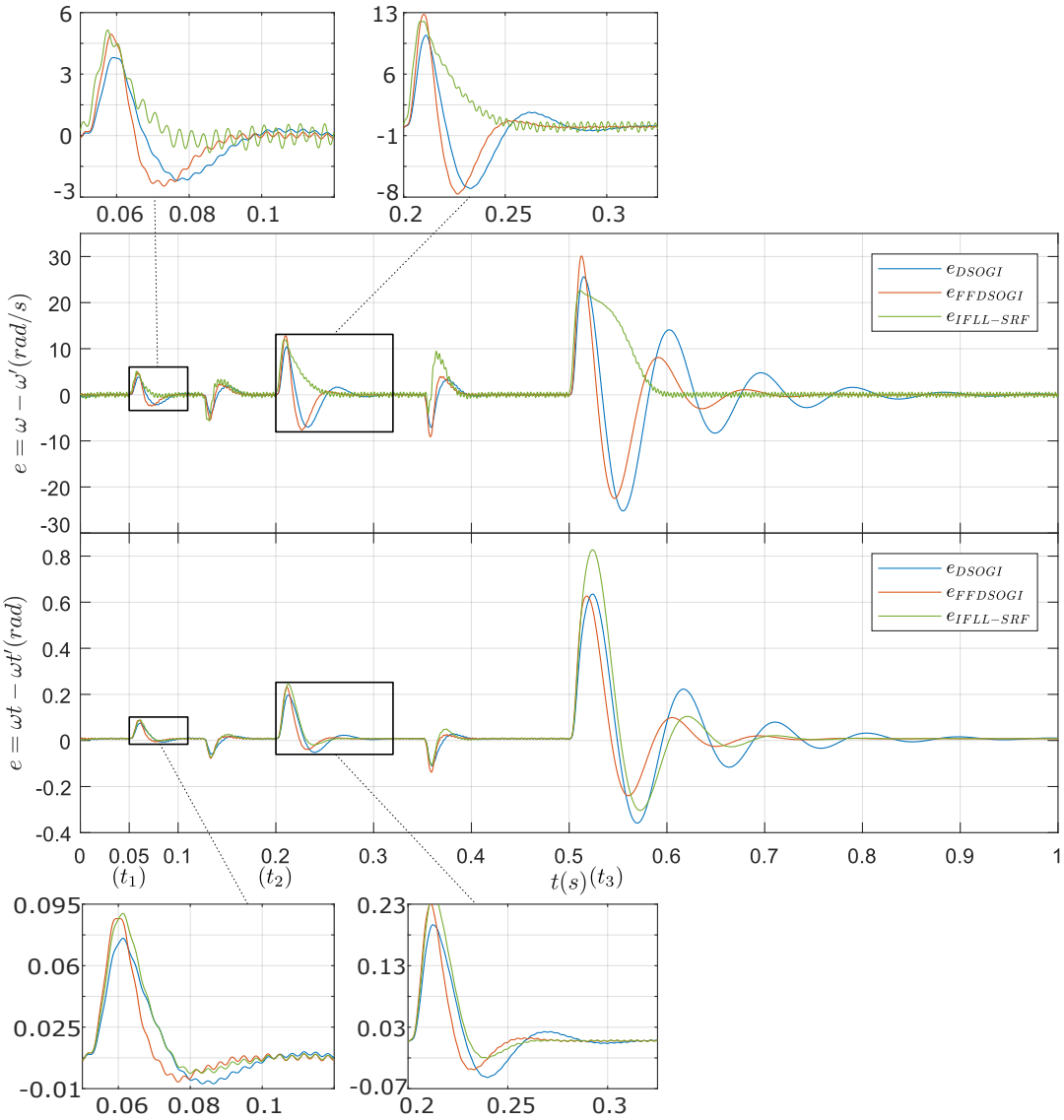


Figure 3.17: Estimated frequency (top) and phase (bottom) for the different methods during test #3.

taking respectively 200 *ms* and 350 *ms* to reach steady-state. On another hand, the IFLL-SRF presents a significantly faster response time taking 100 *ms* to reach the steady-state.

In terms of phase dynamic response, the results are coherent with the aforementioned comments for the estimated frequency. The only exception is during (t_3), where the IFLL-SRF presents a phase response similar to the FFDSOGI of $\approx$ 200 *ms*.

The summary of the voltage sag results is presented in table 3.11, where steady-state ME is not shown, since it remains approximately constant for all methods.

Table 3.11: Results summary obtained for test #3- voltage sags.

		DSOGI			*FFDSOGI*			*IFLL*		
		$VS = 30\%$	$VS = 60\%$	$VS = 90\%$	$VS = 30\%$	$VS = 60\%$	$VS = 90\%$	$VS = 30\%$	$VS = 60\%$	$VS = 90\%$
ω'	$t_s(ms)$	42.0	70.0	360	38.0	60.0	160	38.0	60.0	90.0
	OS (rad/s)	3.81	10.4	25.6	4.94	12.8	30.1	5.15	12.0	22.6
$\omega t'$	$t_s(ms)$	51.0	113	500	41.0	75.0	280	48.0	75.0	280
	OS (rad)	0.061	0.200	0.635	0.087	0.230	0.627	0.090	0.240	0.827

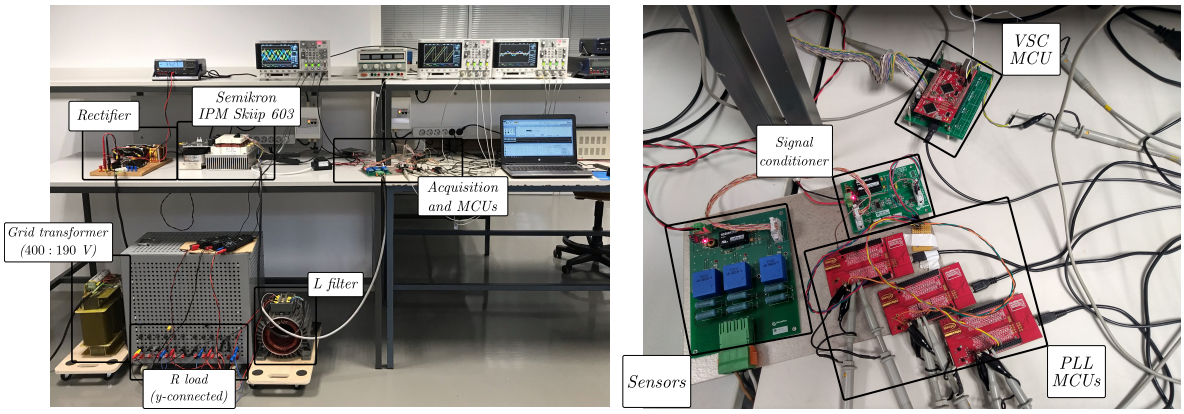
3.6.4 Experimental results

To evaluate and confirm the synchronism performance of the methods discussed in the previous section, a voltage source converter (VSC) is configured to generate a local grid voltage (instead of a DAC board) so that the switching EMI could be present in the measurements. The VSC operates in an open-loop as a programmable voltage source with a filter inductance supplying a resistive load y-connected. Hence, it is possible to generate any three-phase voltage through the VSC modulation signal manipulation.

Additionally, voltage measurements are taken at filter output, therefore the modulation phase angle is leading the measured phase voltage due to the load angle. As a consequence, the estimated phase angle presents a DC error resulting from the load angle, when the modulation phase angle is taken as reference. The resulting setup is presented in figure 3.18. The harmonics injected in the modulation were also adjusted so that voltage, measured at inductance output, contains the harmonics as indicated in table 3.3.

For evaluation of the methods, three identical MCUs (Infineon XMC 4500) were programmed, each with a different method. The sensed three-phase voltage is fed into each of the MCU boards and the two DACs available per board were tuned for further results evaluation. The PLL MCU DACs generate signals accordingly with the estimated frequency and phase angle of each method and compared with VSC MCU modulation frequency and phase. The generated voltages were limited below 70 V_{rms}, though MCU readings are amplified by a factor of 3 so that measured voltage becomes near nominal grid conditions. Noteworthy that the presented setup does not allow to apply steps as applied during the simulation, due to the *RL* time constant.

In figure 3.19 it is shown the results obtained for the test #1 considering conditions similar with (t_3) of table 3.4. In the figure it is shown the voltage waveforms at filter inductance output with unbalanced phase voltages and harmonic content, measured through the oscilloscope FFT function.

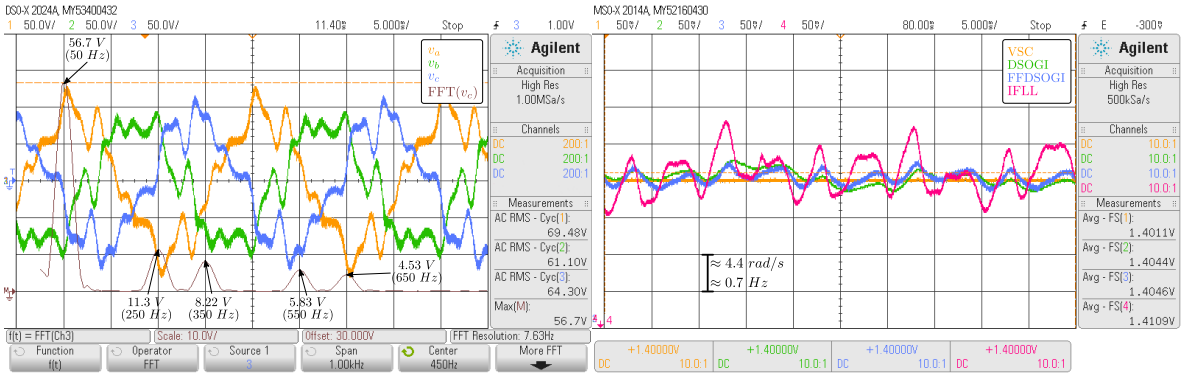


(a) (b)

Figure 3.18: Laboratory setup for three-phase voltage generation and evaluation of the PLL's performance. (a) shows the full setup and (b) the acquisition board, conditioning board, and MCUs.

Analysis of the results obtained for test #1 allows concluding that, as discussed in section 3.6.1, the DSOGI and FFDSOGI methods perform very similarly in terms of frequency estimation. The IFLL presents higher oscillations than the other two, though such differences are not as noticeable in practice as the ones obtained during simulation. The phase estimation of the IFLL presents a higher ME (DC error) than other methods, as also discussed in section 3.6.1. Despite not being noticeable in figure 3.19, the steady-state phase estimation oscillations are identical in all three methods. Such a fact was concluded by monitoring the PI's output of all methods.

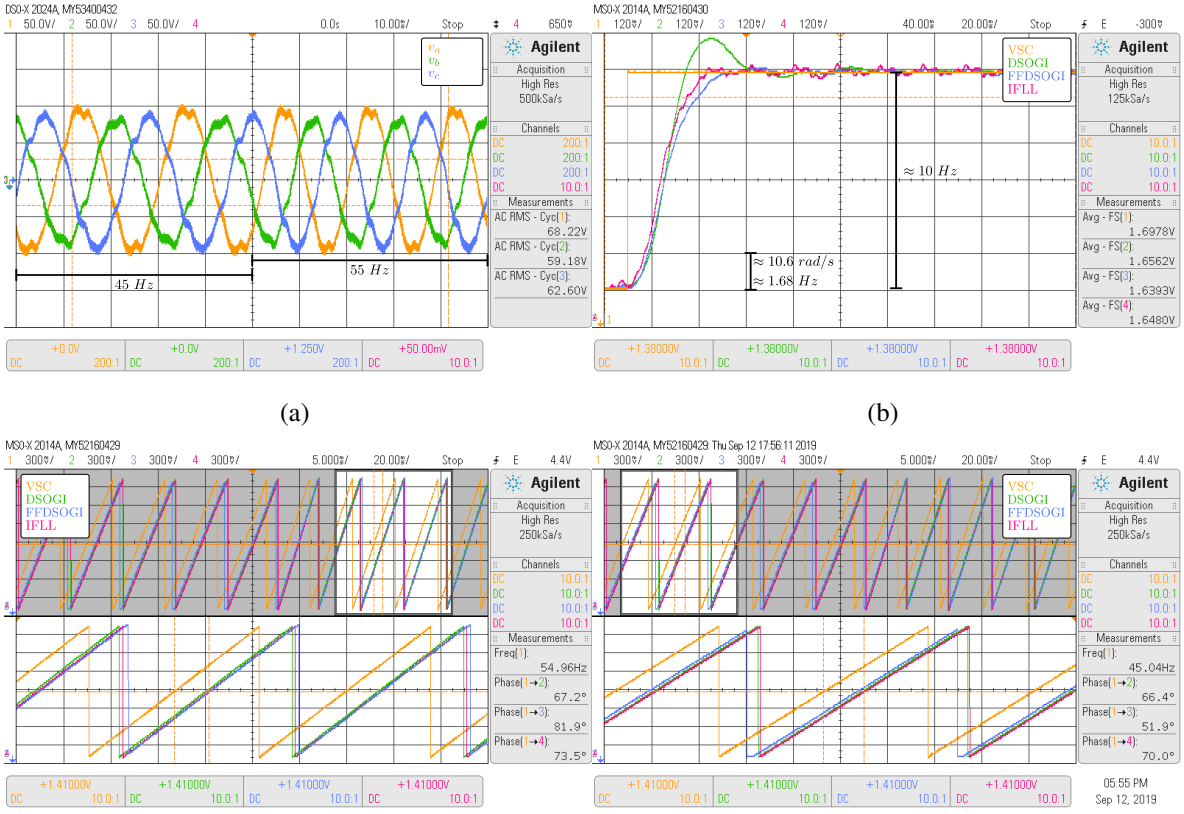
For test #2, it was applied a frequency step ($45 \rightarrow 55\ Hz$), as shown in figure 3.20, and a phase jump of 45° at nominal frequency (figure 3.21). Additionally it is shown, in figure 3.22, the estimated angle in steady state for both limit frequencies.



(a) (b)

(c)

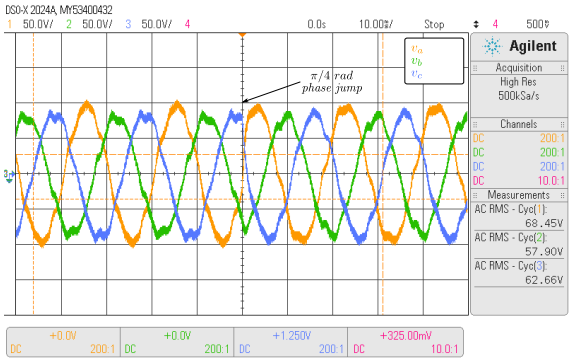
Figure 3.19: Experimental results for test #1. (a) Measured voltages with the FFT of phase v_c, (b) estimated frequency and (c) estimated phase angle.



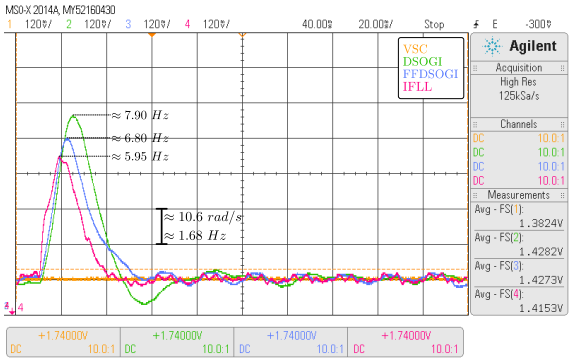
(a) (b)

(c)

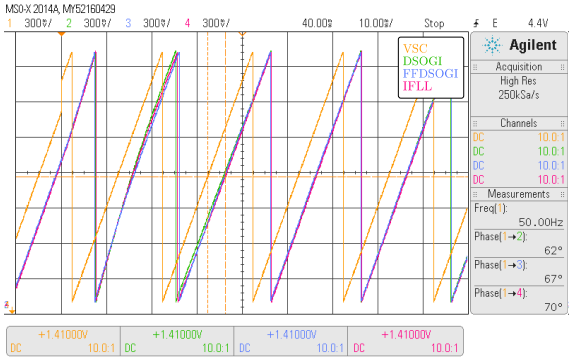
Figure 3.20: Experimental results for test #2 frequency step. (a) Measured voltages, (b) estimated frequency, and (c) estimated phase angle.



(a)

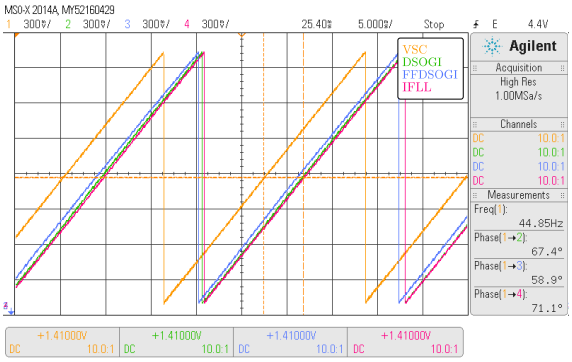


(b)

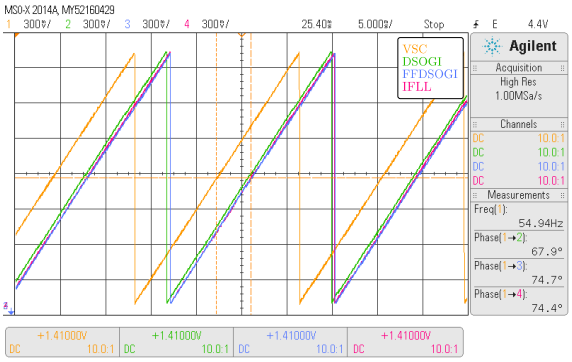


(c)

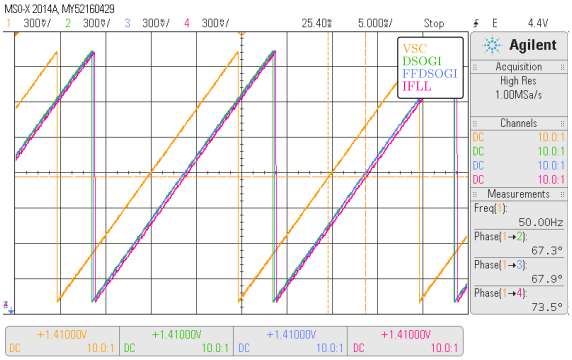
Figure 3.21: Experimental results for test #2 phase jump (a) Measured voltages, (b) estimated frequency, and (c) estimated phase angle.



(a)



(b)

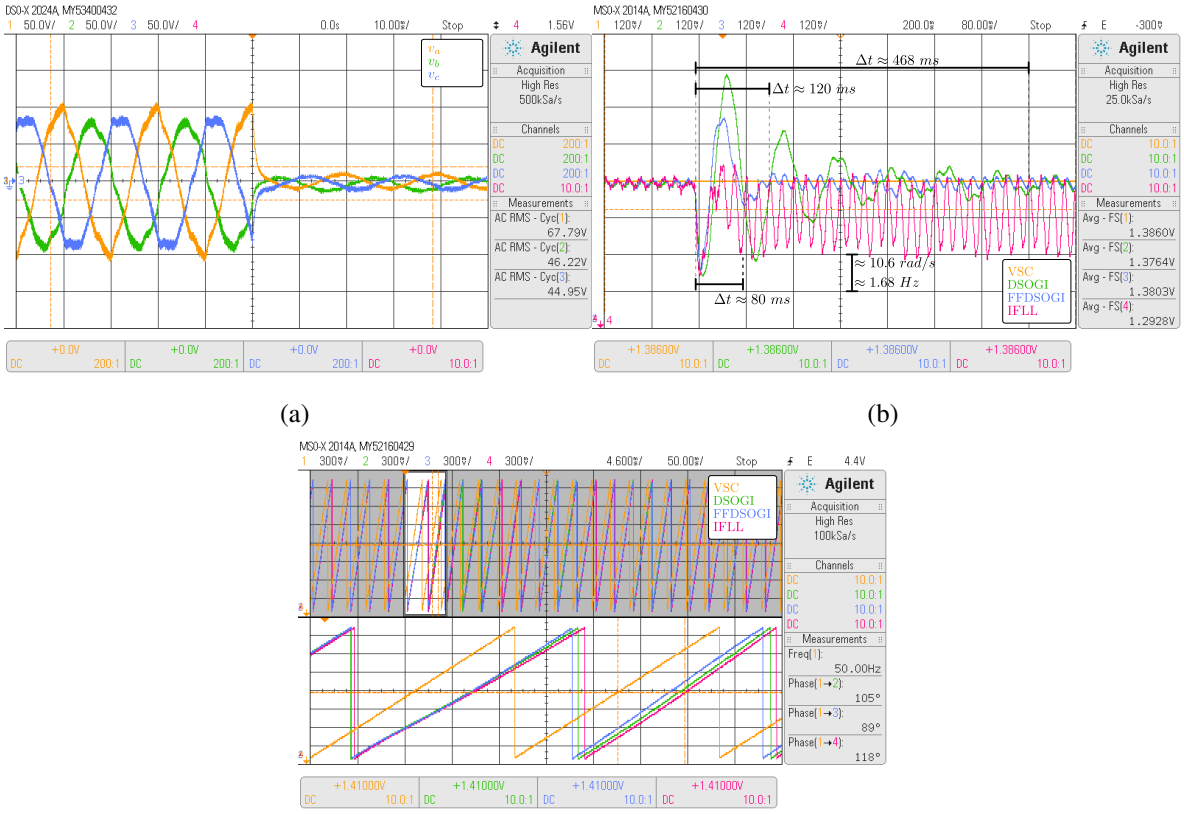


(c)

Figure 3.22: Steady state angle estimation for (a) 45 Hz, (b) 55 Hz and (c) 50 Hz frequencies.

The obtained results agree with the discussion carried in section 3.6.2. The estimated frequency of both tests (figures 3.20 and 3.21) follows the results already discussed. The only exception goes to the phase estimation by the FFDSOGI during limit frequencies, *i.e.* there is a DC error of the phase estimation that changes depending on the frequency. Such behaviour is justified by the method linearization for the phase estimation and can be visualised in figure 3.22 by checking the change in the phase difference between the modulation phase angle (VSC) and the FFDSOGI.

For the voltage sag test #3 a 90% sag is applied since corresponds to the simulated worst case, and the respective obtained results are presented in figure 3.23.



(a) (b)

(c)

Figure 3.23: Experimental results for test #3. (a) Measured voltages, (b) estimated frequency and (c) estimated phase angle.

From figure 3.23, it can be noticed that the IFLL is the method that responds faster, though it presents significantly higher steady-state oscillations and a change in the average frequency estimation value. The FFDSOGI takes 1.5× more than the IFLL to reach steady-state, though it presents significantly fewer oscillations and the steady-state average error can be neglected. The DSOGI be-

haviour follows the FFDSOGI one with the difference of taking more than 4× to reach a steady-state.

The last test is related to the MCU processing times and it is shown in figure 3.24. In the figure it is shown the execution times of each method, *i.e.* the pulse width of each square wave represents the execution time of the algorithm including the ADCs acquisition time.

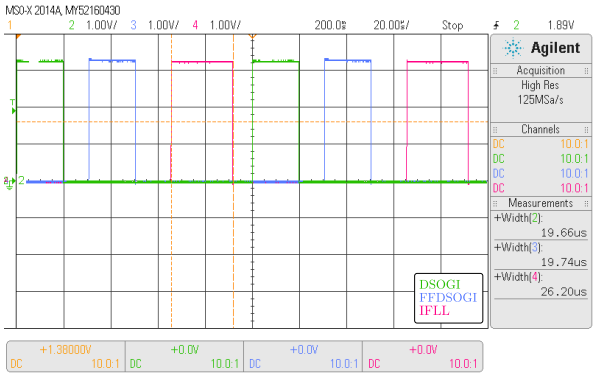


Figure 3.24: Algorithms process time including ADCs acquisition time.

3.6.5 Tests Benchmark

Taking into account tables 3.5, 3.8, 3.9 and 3.11, classification table 3.12 is presented. For classification purposes, the marks were calculated by considering the ratio of the averaged registered values (per method of each test transition), by the minimum average obtained from all tests for each test transition. Therefore the best result (minimum value) for each test/transition is 1.0 and the choice of the suitable method should be based on the minimum classification value obtained. The table classifications are divided into two categories (frequency and phase), where for each category, the methods are classified in terms of the steady-state performance *SS* (RMSE or ME), dynamic response to frequency step changes $\Delta\omega$, phase jumps (*p.j.*), and voltage sags *VS* (evaluated both the overshoot and settling time). It can be noticed that the steady-state is based only on the average of the RMSE for the frequency and the average of the ME for the phase angle estimations (both from test #1). The choice of the steady-state error indicators was based on its significance, i.e. the RMSE in the case of the frequency, and ME in the phase estimation.

As an example, for grid-following operation with the main grid (strong grid), there are no expected voltage sags or frequency step changes. Hence, in this case, it is valid to consider the steady-state phase estimation and the MCU burden as the selection criteria. In such conditions, the DSOGI-PLL is the best choice. The IFLL is highly recommended if fast-tracking is important during voltage sags,

Table 3.12: Classification table of the methods performance during different tests.

			DSOGI	*FFDSOGI*	*IFLL*	*Description*
ω	*RMSE*		1.0	1.0	4.3	Steady-state frequency oscillations- test #1
	$\Delta\omega$	*OS*	1.0	1.0	1.0	Overshoot during frequency step- test #2
		t_s	1.9	1.0	1.6	Settling time during frequency step- test #2
	p.j.	*OS*	1.5	1.7	1.0	Overshoot during phase jump- test #2
		t_s	2.0	1.0	1.7	Settling time during phase jump- test #2
	VS	*OS*	1.0	1.3	1.2	Overshoot during voltage sag- test #3
		t_s	2.1	1.3	1.0	Settling time during voltage sag- test #3
ωt	*ME*		1.0	3.9*	1.2	Steady-state phase deviance - test #2
	$\Delta\omega$	*OS*	1.3	1.0	1.2	Overshoot during frequency step- test #2
		t_s	1.6	1.0	1.6	Settling time during frequency step- test #2
	p.j.	*OS*	1.0	1.0	1.0	Overshoot during phase jump- test #2
		t_s	1.6	1.0	1.6	Settling time during phase jump- test #2
	VS	*OS*	1.0	1.2	1.3	Overshoot during voltage sag- test #3
		t_s	1.5	1.0	1.1	Settling time during voltage sag- test #3
MCU execution time			1.0	1.0	1.3	MCU processing time- experimental result

* for operation frequency of $\omega = \omega_n \pm 5$ %, consider 1.3 for the FFDSOGI.

mostly because of its gain normalization but at the cost of a higher MCU burden. The FFDSOGI is the clear choice when frequency and phase tracking is desired for small frequency variations (< 5 %).

Through the presented classification table, it is possible to apply weights to the different marks and select the best method based on the minimum value obtained.

As an example, on this thesis it is considered the following requirements, all related with the phase angle estimation (weight applied to each component in parenthesis):

- Phase angle steady-state estimation is of high importance since controllers are designed to operate in the SRF (25%);
- Frequency should be according to EN 50438 [84], *i.e.* deviance inside the limit $\omega_n \pm$ 3 %;
- Phase jumps may occur during re-connection with the main grid (25%);

- Voltage sags may occur during overload conditions or heavy-loads connection (25%).
- Low MCU processor burden (25%);

Following table 3.12 marks and the listed criteria, the best choice is the FFDSOGI-PLL (1.03 pts), followed by the DSOGI (1.25 pts), and the IFLL (1.30 pts).

In the following chapter, it is addressed the converter filter and control loop designs, where the FFDSOGI is included in the SRF phase angle estimation. In chapter 5, the FFDSOGI is also responsible for providing the microgrid voltage amplitude and frequency to the droop control. In both chapters, the FFDSOGI is designed as described in the current chapter.

CHAPTER 4

Voltage-Source Converter Design

As discussed in the state of the art chapter 2, the converter can operate in grid-following or grid-forming modes. Independently of the converter operation mode, the VSC must include a current control loop to allow its operation with regulated current or to limit its operation during voltage sags or over-voltages events. Operation in the grid-following mode implies synchronous operation with the grid, where the current control inner loop must be present. The current controller bandwidth also dictates the converter power control dynamics. In grid-forming, the converter regulates the formed grid voltage amplitude and frequency. The synchronous frame phase angle is generated through the integration of an internal frequency set-point, hence it is not regulated directly but instead through the direct and quadrature voltage components. The dual-loop voltage control allows regulating the voltage components whose dynamic is dependent on the inner control loop bandwidth. In section 4.2.4.2 a better alternative to the dual-loop voltage controller is presented, allowing to exploit the open-loop voltage dynamics of the VSC and ensuring operation with currents within the converter limits.

The converter filter is crucial for the attenuation of the current harmonics, but also has a great impact on the current control loop bandwidth, mostly when a fast controller dynamic response is desired. In literature, it can be found substantial work related to the *LCL* design but it is rarely addressed its design in the context of weak-grids. Furthermore, the presented methods suggest some guidelines for the filter design but lack a deterministic procedure. In the chapter, the *LCL* design is reviewed and the respective analysis is extended to include particular aspects such as the influence of the grid impedance on the filter resonant frequency and consequent current control loop bandwidth. In section 4.1.2 it is presented a design algorithm that allows to deterministically design the filter, based on pre-defined constraints.

The chapter discusses the design of the voltage source converter presenting the research achievements at performing as a component of a microgrid. The research focuses on the aforementioned control loop components: the power converter output filter (*LCL*), the inner control loop (current),

and the outer control loop (voltage) designs. To limit the extent of the document, details like the choice of topology, semiconductors, and converter modulation techniques, were excluded from the present work. As discussed in previous chapters, the power converter and its control play a key role in the power stability of microgrids and consequently contribute towards an increasing development of needed decentralized grids.

The chapter comprehends four main sections. In section 4.1 it is presented the applied procedure for the converter filter design, followed by the current and voltage control loops design, in section 4.2. In section 4.3 are presented the achieved simulation results and the respective discussion.

4.1 VSC filter

The output filter of grid-connected converters has considerable importance in the power converter performance as it interfaces with the grid. Parameters like the converter switching frequency, the produced switching harmonics, and converter power rating, conditionate the design. Considering the power converter as a source of harmonics, produced by a pulse-width modulation (PWM) scheme operating at high switching frequencies, the generated current harmonics must be properly filtered for a seamless connection with the grid.

There are typically three types of filters used: *L*, *LC*, and *LCL*. The first-order *L* filter is the simplest and most widely used, though it is big and bulky when compared with the other two types and it cannot meet some of the regulatory requirements [85]. The *LC* and *LCL* filters, beyond their resonant frequency, present a higher attenuation rate of current harmonics when compared with the *L* filter. Hence, for the attenuation of high order harmonics, the *LCL* or *LC* are preferable over the *L* filter, allowing the design of smaller filter size. Comparing the *LC* with the *LCL* filter, for grid-tied converters, a clear disadvantage of the first is the uncertainty in the resonant frequency when considering line or load impedance variations [86]. So the *LCL* filter is a proper filter choice for the interface of the converter with the grid. Furthermore, an optimal *LCL* present a higher attenuation rate than the *LC* under certain conditions. For these reasons, this section is focused on the *LCL* filter design.

The *LCL* filter transfer function $i_g(s)/v_i(s)$ is expressed as (4.1). The transfer function is obtained by considering the grid voltage e_g null, *i.e.* grid voltage is considered a system disturbance [87].

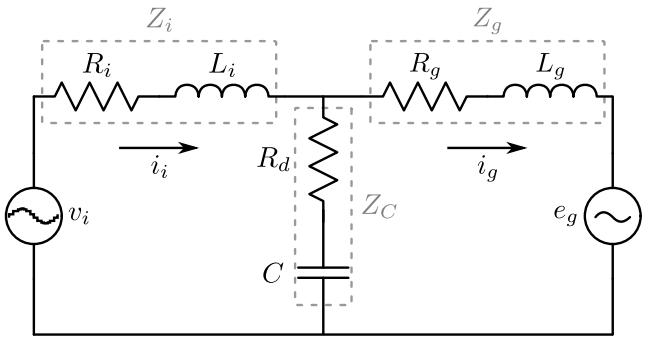


Figure 4.1: Per phase schematic of the *LCL* filter.

$$\frac{i_g(s)}{v_i(s)} = \frac{A_1 s + A_0}{B_3 s^3 + B_2 s^2 + B_1 s + B_0}, \quad \begin{cases} A_1 = R_d C \\ A_0 = 1 \\ B_3 = L_i L_g C \\ B_2 = [R_g L_i + R_i L_g + R_d (L_i + L_g)] C \\ B_1 = [R_i R_g + R_d (R_i + R_g)] C + L_i + L_g \\ B_0 = R_i + R_g \end{cases} \tag{4.1}$$

Considering the transfer function (4.1), the extraction of the resonant frequency becomes cumbersome due to a large number of terms. Additionally, the filter resonant frequency is dependent only on the reactive component of the filter. The active component of the filter impedance (resistance) contributes to damp the resonance gain therefore it can be neglected for the resonant frequency determination. Under these conditions, the filter transfer function (4.1) is simplified into (4.2) allowing to obtain the respective resonant frequency ω_0 (4.3). The inductances resistances (R_i and R_g), normally take small values and consequently are usually neglected. Furthermore, considering $R_d \gg (R_i + R_g)$ allows to obtain the transfer function of the damped filter (4.4).

$$\frac{i_g(s)}{v_i(s)} = \frac{1}{L_i L_g C s^3 + (L_i + L_g) s} \tag{4.2}$$

$$\omega_0 = \sqrt{\frac{L_i + L_g}{L_i L_g C}} \tag{4.3}$$

$$\frac{i_g(s)}{v_i(s)} = \frac{R_d C s + 1}{C L_i L_g s^3 + R_d C (L_i + L_g) s^2 + (L_i + L_g) s} \tag{4.4}$$

In figure 4.2 it is presented the i_g/v_i transfer function Bode diagram of a given *LCL* filter design. The filter presents a resonant frequency of $f_0 = 1.5\ kHz$ to filter a switching frequency of $f_{sw} = 5\ kHz$. The yellow and blue curves represent the undamped and damped *LCL* filter respectively. The equivalent $L_t = L_i + L_g$ and $L_{kt} \approx 5.2L_t$ (for the given example) filter curves were added for comparison purposes. The red curve L_t represent the equivalent single inductance filter, and the pink curve L_{kt} the total single inductance needed to obtain the same attenuation gain of the damped *LCL* (LCL_d) at switching frequency.

In the Bode plots of figure 4.2, it is noticeable the triple attenuation rate of the undamped *LCL* filter ($-60\ dB/dec$) for frequencies higher than the resonant frequency f_0. Additionally, the high gain at the resonant frequency has to be damped. Though, adding the damping resistance R_d (resistive damping) decreases the attenuation rate of the filter and increases the Joule losses in the added resistance (attenuation rate drops to $-40\ dB/dec$). Therefore, a proper design of the current control loop with an active damping scheme, or a proper impedance-based passive damping, is necessary. Some of the passive damping schemes for the *LCL* filter can be found in [88], and an example of the active damping is given in [89]. A more recent active damping approach is based on virtual impedance control, where a passive damping scheme is virtually added in the control loop [90].

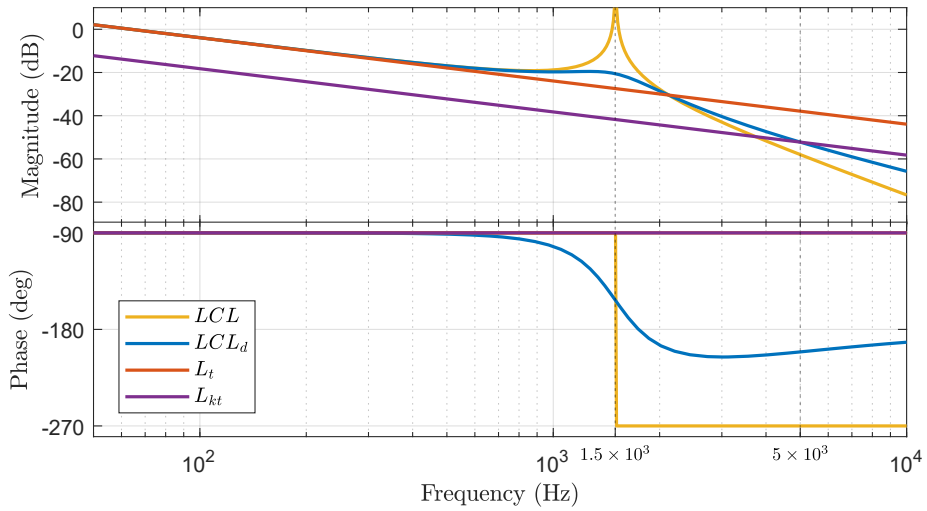


Figure 4.2: Example of the *LCL* filter i_g/v_i transfer function Bode plot and comparison with the *L* filter.

The main goal of the converter output filter is to reduce the current harmonics produced by the converter modulation scheme switching voltage. The current harmonics must be reduced following

the grid standards, *e.g.* the IEEE 519 which is considered a reference standard. Additionally it is of high importance to [91–93]:

- minimize filter size (inductances and capacitor): lower costs, lower voltage drop, higher DC bus utilization, reduced energy stored in the filter;
- ensure reduced capacitor reactive power: increased power factor;
- increase robustness to external parameters: *e.g.* uncertain grid line impedance.

There are several *LCL* design procedures in the literature but rarely cope with all the aforementioned objectives. In [93] it is presented a design procedure that addresses almost all the identified objectives, but it fails in giving a straightforward design procedure, suggesting arbitrage of certain design conditions (resonant frequency ratio). Furthermore, the presented method does not consider the line impedance which is critical in a microgrid, mostly when considering a grid-forming converter.

In the following sections it is described the different design steps of the *LCL*.

4.1.1 *LCL* filter design

The main objective of the *LCL* filter design is to achieve the desired attenuation of the high order frequency harmonics to avoid distorting grid voltage. Hence, filter design follows the IEEE-519 standard, where limits of individual current harmonics are defined in table 4.1. The given harmonic limits represent the worst case, *i.e.* the lowest limits, and are normalized around the nominal current I_n. When a ESS converter is operating as a grid forming in a microgrid, it becomes hard to define its nominal current since the resulting current results from the power balance between the local generation and loads. Hence, the nominal current is considered as the current at maximum power and nominal grid voltage. The present section extends the methodology presented in [93].

Table 4.1: Current odd harmonics limit ($\%I_n$), following IEEE-519.

Individual harmonic order (odd harmonics)						
I_{sc}/I_n	$3 \leq h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h \leq 50$	TDD
< 20	4.0	2.0	1.5	0.6	0.3	5.0

In the following subsections, all filter values are normalized accordingly with the system base values (4.5-4.8) allowing to follow the presented filter design methodology to any converter project.

$$Z_b = \frac{V_n^2}{S_n} \tag{4.5}$$

$$C_b = \frac{1}{\omega_n Z_b} \tag{4.6}$$

$$L_b = \frac{Z_b}{\omega_n} \tag{4.7}$$

$$h_{sw} = \frac{\omega_{sw}}{\omega_n} \tag{4.8}$$

Considering the ratio of the resonant frequency f_0 and the switching frequency f_{sw}, the resonant frequency becomes (4.3) as a function of the resonant frequency ratio $k_f = f_{sw}/f_0$ (4.9). The second term of (4.3) can also be rewritten as a function of the total inductance $L_T = L_i + L_g$ and the inductance ratio $\mu = L_g/L_i$, resulting in (4.10). Replacing (4.9) and (4.10) into (4.3), results in (4.11) allowing to correlate the filter size ($L_T C$ product) with the filter resonant frequency ratio k_f and inductances ratio μ [92, 93].

$$\omega_0^2 = 4\pi^2 f_0^2 = \frac{4\pi^2 f_{sw}^2}{k_f^2} \tag{4.9}$$

$$\omega_0^2 = \frac{L_i + L_g}{L_i L_g C} = \frac{(L_i + L_g)^2}{L_T C L_i L_g} = \frac{1}{L_T C} \frac{L_i^2 (1+\mu)^2}{L_i^2 \mu} = \frac{1}{L_T C} \frac{(1+\mu)^2}{\mu} \tag{4.10}$$

$$L_T C = \frac{k_f^2}{4\pi^2 f_{sw}^2} \frac{(1+\mu)^2}{\mu} \tag{4.11}$$

Through observation of (4.11), it is clear that there are two key parameters for the design process: the inductance and frequency ratios. Hence it is important to understand its impact on the filter size and performance.

4.1.1.1 Impedance ratio (μ)

Taking the derivative of the impedance product (4.12), for a given resonant frequency ω_0, it becomes clear that the filter product $L_T C$ is minimized when considering $\mu = 1$. In other words, for a given C, choosing $L_i = L_g$ allows minimizing the total inductance L_T contributing to smaller filter size. Furthermore, the unitary inductance ratio also results in the minimum voltage drop (L_T is minimized), allowing to achieve higher dynamic response [92]. Noteworthy, that the grid side inductance includes all the known series inductances of the grid side. Such known inductances may include a transformer leakage inductance or line impedance from the converter to the PCC. Once the *LCL* grid

side inductance L_g is determined, it may be adjusted to include known inductances. In figure 4.3 it is plotted the inductance ratio influence in the filter size for a fixed resonant and switching frequencies k_f.

$$\frac{\partial(\omega_0^2 L_T C)}{\partial \mu} = 0 \Leftrightarrow \mu = 1 \tag{4.12}$$

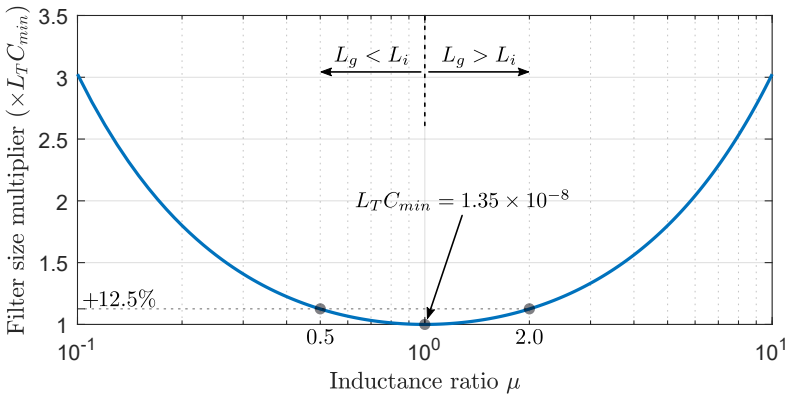


Figure 4.3: Influence of inductance ratio μ in the *LCL* filter size.

Another important factor is the minimization of energy stored in the filter. To evaluate the total energy stored, the energy on each passive element is summed (4.13) and rewritten in terms of μ and k (4.14). It should be noticed that, for a certain frequency ratio, resonant voltage V_r and current I_r, the minimization of inductance energy is achieved when $\mu = 1$, got through $\partial E_{L_T C}/\partial t = 0$. Though, as discussed in [94], μ has a minor impact on the total stored energy of the filter, when compared with the choice of the resonant frequency k_f.

$$E_{L_T C} = \frac{1}{2} L_i I_r^2 + \frac{1}{2} L_g I_r^2 + \frac{1}{2} C V_r^2 \tag{4.13}$$

$$E_{L_T C} = \frac{1}{2} \frac{k^2}{C \omega_{sw}^2} \frac{(1+\mu)^2}{\mu} I_r^2 + \frac{1}{2} C V_r^2 \tag{4.14}$$

It can be concluded that $\mu = 1$ results in minimum filter size and slightly contribute to the filter stored energy minimization.

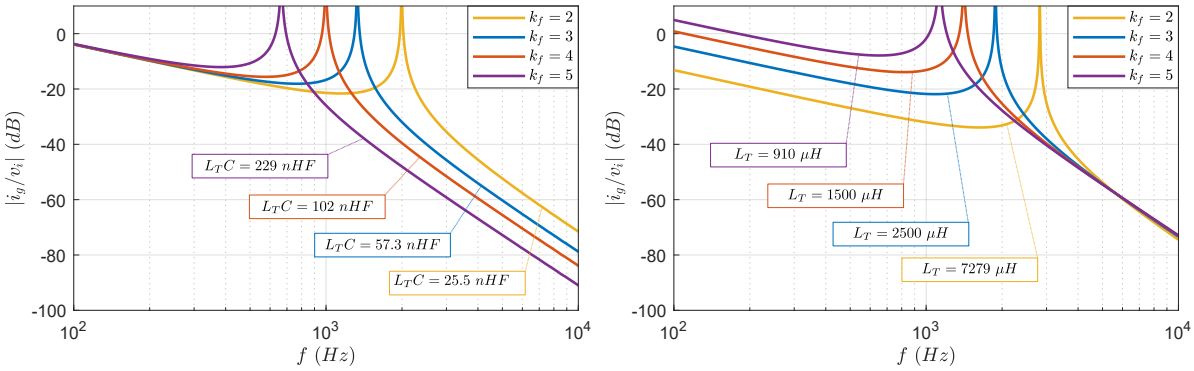
4.1.1.2 Resonant frequency ratio (k_f)

According to [91], the filter resonant frequency should be between half of the converter switching frequency and a decade above the rated grid frequency: $\omega_0 \in [10\omega_n; 0.5\omega_{sw}]$. When ω_0 tends to

ω_n (k_f increasing), the attenuation of higher harmonic components increases what results in reduced filter size for a certain constant target filter gain. Though, such behaviour increases the capacitive reactive power and lowers the current controller bandwidth, leading to slow/poor disturbance rejection (considering the design method described later in section 4.2). Hence, a suitable trade-off between the fast response of the current control loop and filter size (ω_0) must be established.

The filter size has been previously analysed considering the L_TC product, which is a suitable metric when considering a fixed L_T and resonant frequency ratio k_f. In (4.15) it is shown the relationship between $C(L_T,\ k_f)$ for $\mu = 1$. Equation (4.15) shows that increasing L_T results in a smaller C and vice-versa, for a given k_f. It is also noticeable that the L_TC product increases exponentially with k_f, though such an increase does not result in a bigger filter size (physically). The filter size is mainly dictated by the L_T, hence minimizing L_T results in a smaller filter, which means an increase in the L_TC product and minimization of C. Figure 4.4 illustrates the discussed behaviour.

$$C = \frac{1}{L_T}\frac{k_f^2}{\pi f_{sw}^2} \tag{4.15}$$



(a) (b)

Figure 4.4: Influence of the resonant frequency ratio k_f and L_T in the magnitude Bode plot and filter size L_T. (a) k_f influence in the LCL Bode diagram for a given L_T. (b) Influence of k_f in the Bode when L_T is adjusted to achieve a target gain (at $f = 10\ kHz$).

Figure 4.4(a) shows the magnitude Bode diagram for a fixed L_T and different k_f, where for each k_f the respective filter C is calculated as in (4.28). It can be seen that resonant frequency changes with k_f, L_T remains constant (the $-20\ dB$ region is the same for all curves) and the resulting L_TC product increases with k_f. However, the attenuation gain at high frequencies also changes. Figure 4.4(b) represents the curves for different k_f but, with L_T adjusted to obtain a certain target attenuation

gain through (4.18), as it will be later discussed. For this example the curve corresponding to $k_f = 2$ of figure 4.4(a) was chosen as a reference to calculate the target gain at $f = 10\ kHz$. In both plots the $L_T C$ product remains unchanged for each k_f curve, *i.e.* the curves with the same colour present the same $L_T C$ product, though significant differences in the L_T and corresponding C are depicted. It is clear that if $L_T C \propto k_f^2$ is chosen to reflect the filter size, the objective should be to maximize its value. Hence, for a certain target attenuation, increasing k_f leads to a higher $L_T C$ product but, with a smaller L_T and consequently a reduced filter size.

Another important aspect in the selection of the resonant frequency ratio is the choice of the damping scheme. In [95], the authors identify a critical resonant frequency $\omega_{crit,D}$ (4.16) for a double update PWM scheme with T_s sampling time ($T_{sw} = 2T_s$). The defined $\omega_{crit,D}$ refers to the frequency from where damping schemes must be necessarily employed, *i.e.* for $\omega_0 > \omega_{crit,D}$ there is no need for damping, while for $\omega_0 < \omega_{crit,D}$ damping is compulsory. Noteworthy that, despite the carried analysis, the authors suggest that employing damping increase the filter performance. If damping is included, the critical frequency ratio $k_{crit,D}$ analysis can be disregarded.

$$\omega_{crit,D} = \frac{\pi}{3T_s} \tag{4.16}$$

Taking in consideration expression (4.11), and admitting $\mu = 1$, it is possible to verify an exponential increase of the filter size with decreasing resonant frequency (k_f increasing) as shown in figure 4.5, where $k_{crit,D}$ refers to the critical frequency for double update PWM scheme. The values of k for single update PWM are the ones shown ($k_{min,D}$ and $k_{crit,D}$) multiplied by a factor of 2, *i.e.* $k_{x,S} = 2k_{x,D}$ where $x = \{_{min},\ _{crit}\}$. Additionally, for grid side current control and passive damping, k_f should be as low as possible to achieve the maximum damping of resonant harmonics [93].

In figure 4.6 it is presented the change of the resonant frequency k_f with the inductance ratio μ for some constant values of $L_T C$. The curve shows that for a given $L_T C$, $\mu = 1$ allows the resonant frequency ratio maximization, *i.e.* maximum harmonics attenuation, resulting in a smaller filter size L_T.

4.1.1.3 Total inductance L_T and capacitance C

To obtain the filter gain at a certain frequency ω_x, (4.2) is rewritten by substituting $s = j\omega_x$ (4.17). At switching frequency $\omega_x = \omega_{sw}$, the filter gain can be obtained considering $\omega_{sw}^2 = \omega_0^2 k_f^2$ and substituting (4.3) in (4.17). The result is the filter gain at switching frequency (4.18).

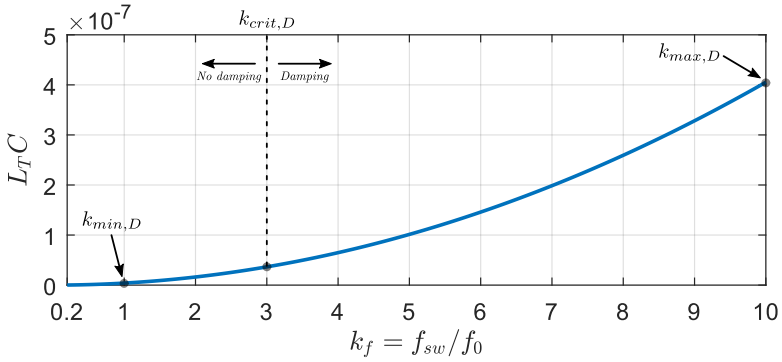


Figure 4.5: Example of the influence of resonant frequency ratio k_f in the L_TC product. Higher L_TC results in smaller filter size (L_T).

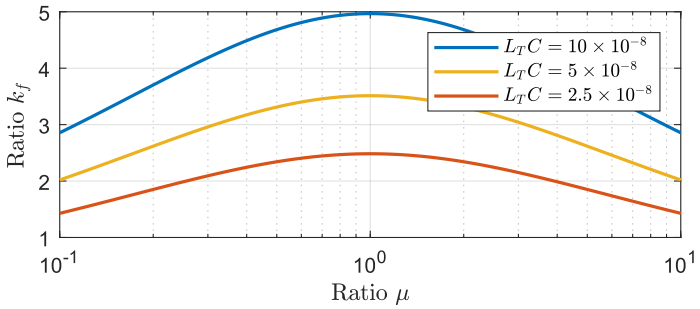


Figure 4.6: Influence of inductance ratio in the resonant frequency ratio k_f for a given *LCL* filter size.

$$a(j\omega_x) = \frac{i_g(j\omega_x)}{v_i(j\omega_x)} = \frac{1}{j\omega_x L_T \left(1 - \frac{CL_gL_i}{L_T}\omega_x^2\right)} \tag{4.17}$$

$$|a(j\omega_{sw})| = \frac{1}{\omega_{sw} L_T \left|1 - k_f^2\right|} \tag{4.18}$$

The filter gain (4.18) is relative to the transfer function $i_g(s)/v_i(s)$, though the target attenuation harmonics in IEEE-519 are relative to the normalised current $i_g/i_{g,n}$. Hence, if (4.18) is converted to the *p.u.* system $i_{g,pu}/v_{g,pu}$, the desired filter gain is directly obtained. Given a target filter gain $|a_{pu}| = |a|.v_{i,n}/i_{g,n}$ and frequency ratio k_f, it is possible to calculate $L_{T,min}$ (4.19). The *p.u.* system bases are presented in (4.5-4.8).

$$\frac{L_{T,min}}{L_b} = \frac{1}{h_{sw}\,|a_{pu}|\left|1 - k_f^2\right|} \tag{4.19}$$

Considering the $L_{T,min}$ obtained through (4.19), it is possible to calculate the respective *LCL* capacitor C (4.11) that results in the desired attenuation gain. Though, as suggested in [91], to limit the

decrease of the power factor at nominal power, the capacitor is usually limited to a maximum of 5 % of the reactive power absorbed under rated conditions (4.20). Hence, reactive power consumed by the capacitance can be defined by x and calculated as shown in (4.20-4.22) [96]. For a chosen k_f and harmonic attenuation $|a_h|$, (4.11) may result in an oversize capacitor $C > x_{max}C_b$. In such a case, L_T must be increased (reducing k_f) to lower the capacitor size.

$$\cos(\phi) = \frac{P_n}{\sqrt{P_n^2 + Q_n^2 + Q_C^2}},\ |Q_C| = \omega_n C_f V_n^2 \tag{4.20}$$

$$C = xC_b\ \wedge x \leq x_{max}(= 0.05) \tag{4.21}$$

$$C_{max} = x_{max}\frac{S_n}{\omega_n V_n^2} \tag{4.22}$$

4.1.1.4 Critical modulation harmonic $v_{i,pu}$ and target filter gain a_{sw}

The harmonic content produced by the power converter depends on the modulation technique, modulation index m_a, and DC bus voltage V_{dc}. Furthermore, voltage harmonics produced by the semiconductors switching must be converted to the *p.u.* system to obtain the desired filter gain $|a_{pu}|$ to comply with the harmonic content presented in table 4.1. Noteworthy that table 4.1 shows individual harmonics only until $f_h = 2.5\ kHz$ (for 50 Hz system) therefore, for higher frequencies it is considered the same odd harmonic limit of $h = 49$ (0.3%).

In figure 4.7 it is presented the most relevant line-line voltage (V_{LL}) harmonic content produced by the typical PWM techniques applied to two-level three-phase VSC. It is noticeable that the critical harmonic appears at $m_f - 2$, being m_f the modulation frequency or switching frequency harmonic (4.23). Furthermore, if the *LCL* filter is designed for sinusoidal PWM (SPWM), it is also guaranteed that harmonic limits for the other two methods are below the limits recommended by IEEE-519.

$$m_f = h_{sw} = f_{sw}/f_n \tag{4.23}$$

As mentioned before, the filter target gain is defined at switching frequency $h = m_f$. Though, as shown in figure 4.7, harmonics at m_f are cancelled out in the line-line voltage [97]. To estimate the attenuation needed at switching frequency, a correction gain offset (4.24) is added considering a constant gain rate M_{dB} between m_f and $m_f - 2$ frequencies. The gain correction transforms the

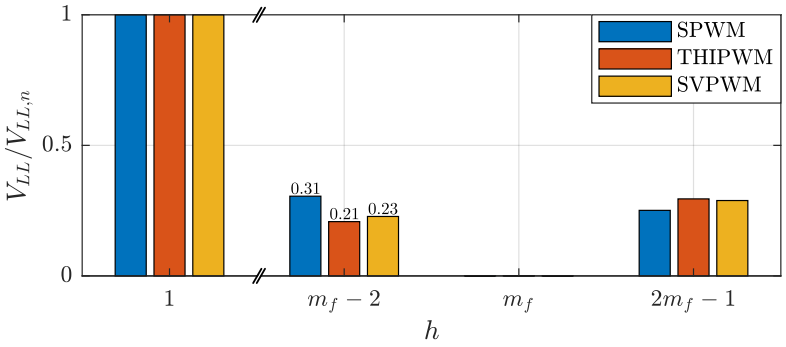


Figure 4.7: Most relevant V_{LL} harmonics produced by different PWM techniques.

m_f-2 harmonic amplitude in equivalent harmonics at m_f with an amplification rate of $-M_{dB}$. As an example, the correction factor is $|\Delta v_{m_f}| = 1.0625$ and $V_{i,pu}(m_f) = 0.3294$, considering the SPWM values of figure 4.7 for an attenuation rate of $-60\ dB/dec$ and grid frequency of $50\ Hz$. The offset $|\Delta v_{m_f}|$ allows to obtain the gain needed at m_f to properly attenuate harmonics at m_f-2 (4.25).

$$|\Delta v_{m_f}| = 10^{\frac{-M_{dB}}{20}\log_{10}\left(\frac{f_{sw}}{f_{sw}-2f_n}\right)} \tag{4.24}$$

$$v_{i,pu} = \left|V_{pu}(m_f)\right| = \Delta v_{m_f} v_{m_f-2} \tag{4.25}$$

Based on the estimated $v_{i,pu}$ (4.25) and target $i_{g,pu}$ (table 4.1), it is possible to calculate the target attenuation rate $|a_{pu}|$ and further calculation of $L_{T,min}$ (4.19).

Another condition is the impact of resistive damping in the filter. As mentioned before, when a series resistance is added to damp the *LCL* resonant frequency, the gain slope drops to $-40\ dB/dec$ (figure 4.2). Since the design method is based on the undamped transfer function, the algorithm will fail to comply with the target gain. Noteworthy, that if the reactive power limit is set to 5 %, the resonant frequency will be close enough to the critical harmonic and the target gain error may be neglected. Otherwise, an approximation should be considered by applying the correction factor K_D (4.26) to the target harmonic content V_{pu} (4.25). The correction factor is established by considering the asymptotic Bode curves of both filters (with and without damping). The filter gain is equivalent in both filter designs until the resonant frequency. Beyond resonant frequency, each filter presents a different gain ratio. If resonant frequency is considered constant (same k_f in both filter designs), it results in a voltage gain difference Δv_D given by (4.27).

$$K_D = \frac{1}{1-\Delta v_D} \tag{4.26}$$

$$\begin{aligned} \Delta v_D =& 10^{\frac{-M_{dB,40}}{20}\log_{10}\left(-\frac{1}{k_f-1}\right)} - 10^{\frac{-M_{dB,60}}{20}\log_{10}\left(-\frac{1}{k_f-1}\right)} \Leftrightarrow \\ \Leftrightarrow \Delta v_D =& \left(\frac{-1}{k_f-1}\right)^{\frac{M_{dB,40}}{20}} - \left(\frac{-1}{k_f-1}\right)^{\frac{M_{dB,60}}{20}} \end{aligned} \tag{4.27}$$

The approximation obtained with the given factor K_D is a conservative approach since it results in a bigger inductance when compared with the undamped equivalent (for the same k_f). Therefore, the resonant frequency is the same, but the asymptotic Bode gain at the resonant frequency is lower for higher inductance filters.

4.1.1.5 Effect of grid impedance in the resonant frequency ω_0

Another important aspect to discuss is the robustness of the filter to line and load impedance changes. To be noticed that inductor winding or damping resistances have no impact on the resonant frequency, as can be seen in figure 4.2. If $L_g = \mu L_i$ is considered, then (4.10) turns into (4.28) and the impedances ratio change due to L_g perturbation, results in changes in the filter resonant frequency ω_0, as illustrated in figure 4.3 (red line). As highlighted in [92], increasing the inductance ratio leads to higher robustness of the filter to line inductance changes, though it also increases the total filter size ($\mu > 1$). To analyse such behaviour it is considered a design based on the previous assumptions, resulting in the parameters presented in table 4.2.

$$\omega_0^2 L_i C = \frac{1+\mu}{\mu} \tag{4.28}$$

Table 4.2: *LCL* design parameters.

μ	k_f	x	L_i	C	f_0	f_{sw}
1.0	2.9	2.3 %	1.26 mH	14 μF	1.7 kHz	5.0 kHz

Considering that filter grid side inductance ($L_g = \mu L_i$) changes with line impedance $L_l = \gamma L_i$, the filter grid side inductance becomes $L_g = \mu L_i(1+\gamma)$ and the *LCL* transfer function (4.2) can be rewritten as (4.29) including the line inductance factor γ.

$$\frac{i_g(s)}{v_i(s)} = \frac{1}{\mu L_i^2 C(1+\gamma)s^3 + L_i(1+\mu+\mu\gamma)s}, \quad \gamma \geq 0 \tag{4.29}$$

In figure 4.8 it is presented the influence of line inductance factor on the filter resonant frequency f_0 (4.30). As expected, resonant frequency decreases with increasing line inductance leading to a higher attenuation of high order harmonics. Nevertheless, if no damping scheme is considered, the resonant frequency deviance may result in undesired resonant oscillations and possibly leading to system instability (k_f crossing critical frequency).

$$\omega_0 = \sqrt{\frac{1+\mu+\mu\gamma}{\mu L_i C(1+\gamma)}} \tag{4.30}$$

To be noticed that, as illustrated in figure 4.16, for higher k_f then $k_{crit,D}$ passive damping is compulsory. When no damping is considered ($k_f < k_{crit,D}$), line inductance further contributes for decreasing f_0 (increasing k_f) which may bring k_f to the critical resonant frequency $k_{crit,D}$ or even to the damping region ($k_f > k_{crit,D}$).

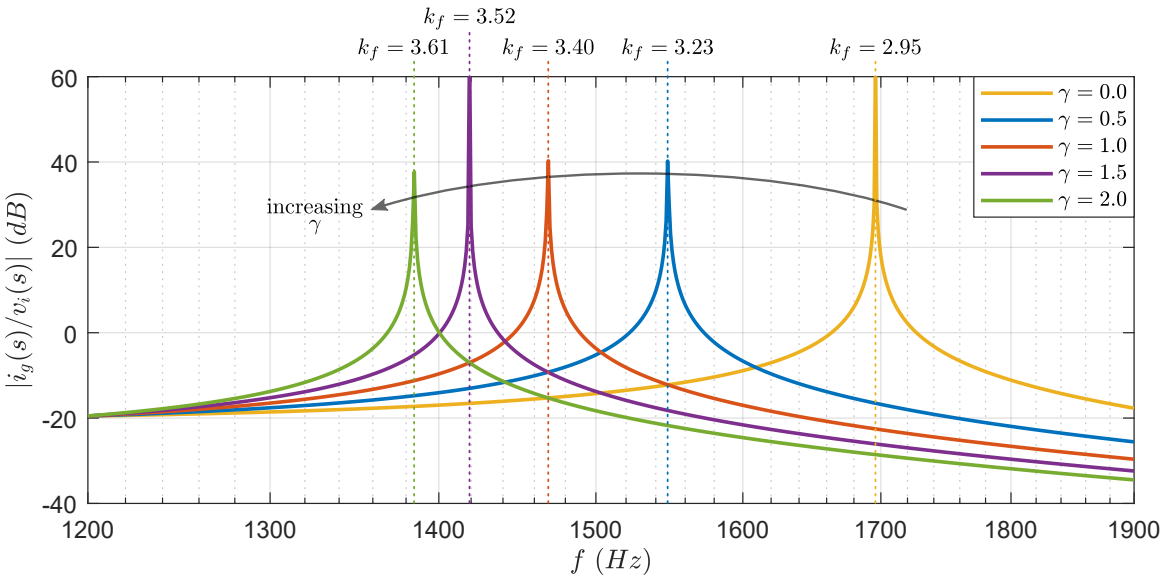


Figure 4.8: Influence of line inductance (γ) in the filter resonant frequency for a given LCL filter with $\mu = 1$.

The described behaviour of the resonant frequency deviance with the line inductance allows setting some boundaries in the *LCL* impedance design. If there is previous knowledge of the line impedance (worst case) measures can be taken to minimize line inductance influence. As presented in appendix A, the cable impedance for low voltage grid is known and independent of the cable

cross-section. Hence the line inductance may be grossly estimated considering the physical size of the microgrid. For a certain maximum line and filter inductances (γ, μ, L_i), L_T can be limited to a minimum value to minimize resonant frequency deviance.

Based on the previous discussion, it is noteworthy that when there is high uncertainty about line impedance, to include damping is mandatory to avoid resonant oscillations, either if k_f is in the damping region or not (but close to the critical resonant frequency). Nevertheless, active damping may also be a good choice through either a capacitor or grid-side current sensing. In most cases, the *LCL* design is chosen over a single *L* to reduce the filter size, therefore it is implied that inductance, should always take a large value when comparing with the line inductance. Hence, γ will normally take small values ($\gamma \ll 1$).

4.1.1.6 Current ripple in the inverter side L_i

The last topic covered in the *LCL* design constraints is the current ripple in the semiconductors, *i.e.* in the inverter side inductance L_i. The bode plot of the $i_i(s)/v_i(s)$ transfer function (4.31) is shown in figure 4.9 for some *LCL* designs with different resonant frequencies but all with the same target attenuation gain $|a_{m_f-2}|$. The inverter side current attenuation gain at frequency ω is given by (4.32). From figure 4.9 increasing the resonant frequency increases total inductance and hence reduces current harmonics at the converter side what implies a smaller capacitance.

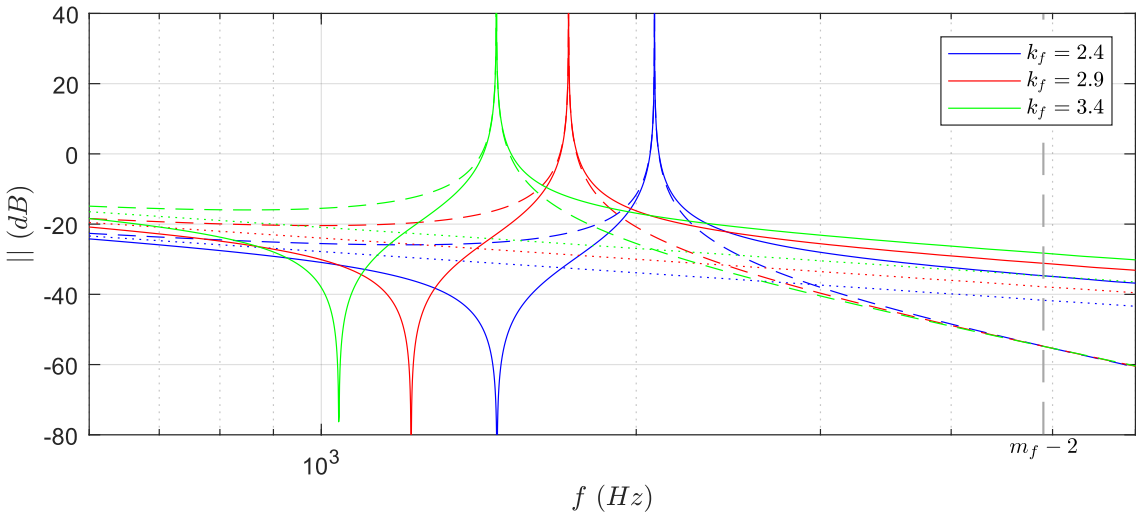


Figure 4.9: Inverter voltage to currents transfer functions magnitude Bode plots. Solid line represents $i_i(s)/v_i(s)$, dashed line $i_g(s)/v_i(s)$ and dotted line the L_T filter.

$$\frac{i_i(s)}{v_i(s)} = \frac{L_g C s^2 + 1}{L_i L_g C s^3 + (L_i + L_g)s} \tag{4.31}$$

$$\left|\frac{i_i(j\omega)}{v_i(j\omega)}\right| = \left|\frac{L_g C \omega^2 - 1}{\omega(-L_i L_g C \omega^2 + L_i + L_g)}\right| \tag{4.32}$$

For a given *LCL* design, substituting $\omega = m_f - 2$ in (4.32) the attenuation gain can be calculated and check if inverter side current harmonics limits are fulfilled. Otherwise, the resonant frequency must be increased. To be noticed that if the harmonics limit for the inverter side is too low, there will be no solution for the *LCL* design and in that case, a single *L* should be considered.

A more straightforward estimation of the harmonics in inverter side inductance is considering $i_i(s)/i_g(s)$ (4.33). Hence, with some algebraic manipulation $|i_i(j\omega_{sw})/i_g(j\omega_{sw})|$ results in (4.34) allowing to estimate the current ripple in the inverter side inductance based on the filter gain obtained for the grid side.

$$\frac{i_i(s)}{v_i(s)}\frac{v_i(s)}{i_g(s)} = \frac{i_i(s)}{i_g(s)} = L_g C s^2 + 1 \tag{4.33}$$

$$\begin{aligned} L_g C = \frac{k_f^2(1+\mu)}{w_{sw}^2}, \quad \left|\frac{i_i(j\omega_{sw})}{i_g(j\omega_{sw})}\right| &= |-k_f^2(1+\mu)| \Leftrightarrow \\ &\Leftrightarrow I_{i,pu} = k_f^2(1+\mu) I_{g,pu} \end{aligned} \tag{4.34}$$

4.1.2 *LCL* design algorithm

Figure 4.10 illustrates the *LCL* design flow chart. The developed design flow chart is adjusted by a single tuning parameter (k_f). The update PWM scheme K_{pwm}, target harmonic content $I_{g,pu}$, maximum capacitive reactive power x, and minimum resonant frequency $f_{0,min}$ are suggested as flexible constraints, for the case that changing k_f does not result in a solution that complies with all the constraints. All variables were already mentioned in the present section, with the exception of K_{R_d}, K_{pwm} and $f_{0,min}$. K_{R_d} represents a flag to indicate if resistive damping is used, allowing to indicate if the correction factor K_D should be applied (4.26), and also to inform the algorithm if critical resonant frequency ratio should be checked. K_{pwm} dictates if single (= 1) or double (= 2) PWM update is applied for the respective k_{min} and k_{crit} constraints calculation. The minimum resonant frequency $f_{0,min}$ is added to limit the k_f increase and hence, ensure a certain current controller bandwidth. When no current control bandwidth is desired, $f_{0,min} = 0\ Hz$.

As illustrated in figure 4.10, the designing method considers a set of close constraints given by the physical parameters and strict constraints. If the algorithm is not able to find a solution that can comply with all the defined constraints, the flexible constraints are variables that can be adjusted. The constants include the base values, calculated following equations (4.5-4.8), the normalized switching frequency h_{sw} (4.24) and the voltage harmonic content produced by the PWM at switching frequency $v_{i,pu}$ (4.25).

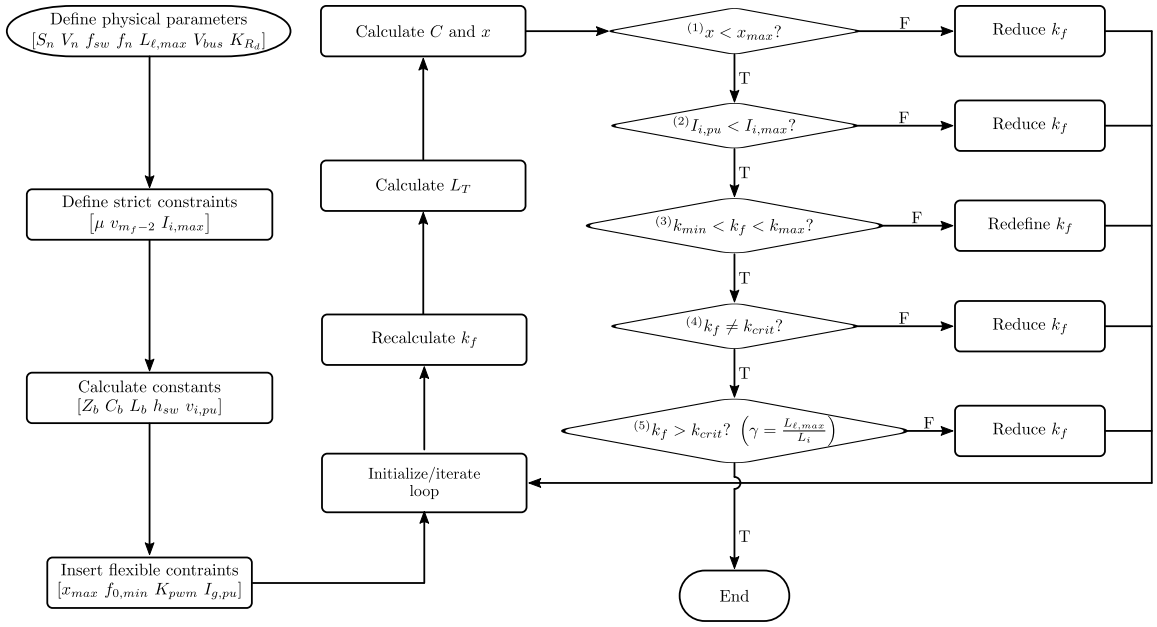


Figure 4.10: *LCL* design algorithm flow chart.

During the first run, the algorithm initialize the constants k_{min}, k_{crit} and k_{max}, considering K_{pwm}, as mentioned in subsection 4.1.1.2. If $f_{0,min}$ is non zero, the maximum resonant frequency ratio is updated to $k_{max} = f_{0,min}/f_{sw}$. The k_f variable is also initialized in this stage ($k_f^{(0)}$), where the value is set depending if damping is included or not (4.35).

$$\begin{cases} k_f^{(0)} = k_{max}\ , & K_{R_d} = 1 \\ k_f^{(0)} = k_{min}\left(1 + \dfrac{k_{crit-k_{min}}}{2}\right)\ , & K_{R_d} = 0 \end{cases} \tag{4.35}$$

The L_T is calculated accordingly with equation (4.17), and the resulting capacitor C and respective reactive power x, through equations (4.11) and (4.21). Following the previous steps, the algorithm can calculate a possible solution for the *LCL* followed by the validation constraints check. The capacitive reactive power x and resonant frequency ratio k_f intervals can be compared without additional

calculus. The current $I_{i,pu}$ is calculated through (4.34), and γ validation is tested considering the recalculation of k_f when resonant frequency is given by (4.30).

The algorithm starts by initializing $k_f = k_f^0$ with the maximum value allowed by k_{max} and decrease it until all constraints are fulfilled. In the checking stage it is noticeable that when a constraint is not fulfilled, k_f should always be reduced with exception of condition $^{(3)}$, where k_f may be increased if $k_f > k_{min}$ is not fulfilled. When damping is considered the algorithm iterates k_f until all constraints are fulfilled. As a result, the *LCL* is designed with the minimum L_T, *i.e.* minimum filter size. In the absence of damping, it is mandatory a more conservative approach where k_f is initialized with a lower value than k_{crit} (4.35). Despite not being included in the presented flowchart of figure 4.10, an extra stopping criteria is added when constraints checking stage results in opposing orders (increase and reduce k_f simultaneously). In this case, it means that there is no solution for the defined set of constraints and the algorithm returns no solution.

The *LCL* design *Matlab* script is available in the appendix B.

4.1.2.1 Design example

To exemplify the use of the presented algorithms, the constraints of table 4.3 are considered. Furthermore, the voltage harmonics were calculated based on the FFT obtained for the sinusoidal PWM and ignoring the voltage drop in the semiconductors and filter impedance. As already illustrated in figure 4.7 of the previous subsection, the sinusoidal PWM represents the modulation scheme that results in higher harmonic content, representing the worst case.

The flexible variables represented in table 4.3 refers to the respective initial values, though are further changed by the algorithm to fit in a suitable solution.

Table 4.3: Example of *LCL* design initialization parameters.

Type	Physical and strict constraints										Flexible			
Symbol	S_n	$V_{LL,n}$	f_{sw}	f_n	$L_{\ell,max}$	V_{bus}	K_{R_d}	μ	v_{m_f-2}	$I_{i,max}$	K_{pwm}	$f_{0,min}$	x_{max}	$I_{g,pu}$
Value	30	400	5	50	320	700	0	1	0.32	10	1	100	2.5	0.3
Units	kVA	V	kHz	Hz	μH	V	–	–	–	%	–	Hz	%	%

Running the algorithm with the constraints presented in table 4.3, results in the filter design presented in table 4.4, where R_d is calculated as suggested in [93] (4.36).

$$R_d = \frac{1}{3\omega_0 C} \tag{4.36}$$

Table 4.4: Example of *LCL* design parameters result.

L_i	L_g	C	R_d	x
1196 μH	1196 μH	15.00 μF	2.1 Ω	2.5 %

4.2 VSC controller design

This section discusses the method employed in the current and voltage control loops design. The current loop design is based on the voltage oriented control (VOC), and it may be applied to the conventional dual loop (cascaded voltage and current controller), or the proposed parallel loop.

This thesis is focused on power control, therefore the outer voltage loop is relative to the AC voltage instead of the DC bus voltage. Therefore, it is considered that the DC bus has infinite capacitance with regulated DC voltage. All the control loops are designed in the synchronous reference frame (SRF) hence, voltage and currents are obtained through the Clarke and Park transformation matrix.

The power converters considered in this thesis may operate in the current control mode (CC), power control (PC) mode, or voltage control mode (VC). The control block diagram for each mode is illustrated in figure 4.11. In the following subsections, it will be discussed the design of each control loop.

Figure 4.11(a) illustrates a grid-connected VSC with the following voltage sensors: dc bus voltage (V_{DC}), *LCL* capacitors voltages ($v_{c,abc}$), and filter output grid voltage ($v_{g,abc}$). The three-phase sensed currents are either on the inverter side ($i_{i,abc}$) and/or grid side ($i_{g,abc}$) *LCL* inductances. The converter control principle can be based on grid-following or grid-forming operation, as explained in chapter 2. Independently of the operation mode, all controllers include the current control (CC) of figure 4.11(c). The grid-following based converter can include only the CC, or also include a power calculation (PC) stage, as shown in figure 4.11(d). The grid-forming converter also includes a voltage control loop (VC) that can be cascaded or placed in parallel with the current loop, as shown in figures 4.11(b) and 4.11(e) respectively. The input of the CC is the reference current I^*_{dq} and can be applied to control the inverter or grid side currents. Hence, the controller feedback I_{dq}, can be either $I_{i,dq}$ or $I_{g,dq}$. The same

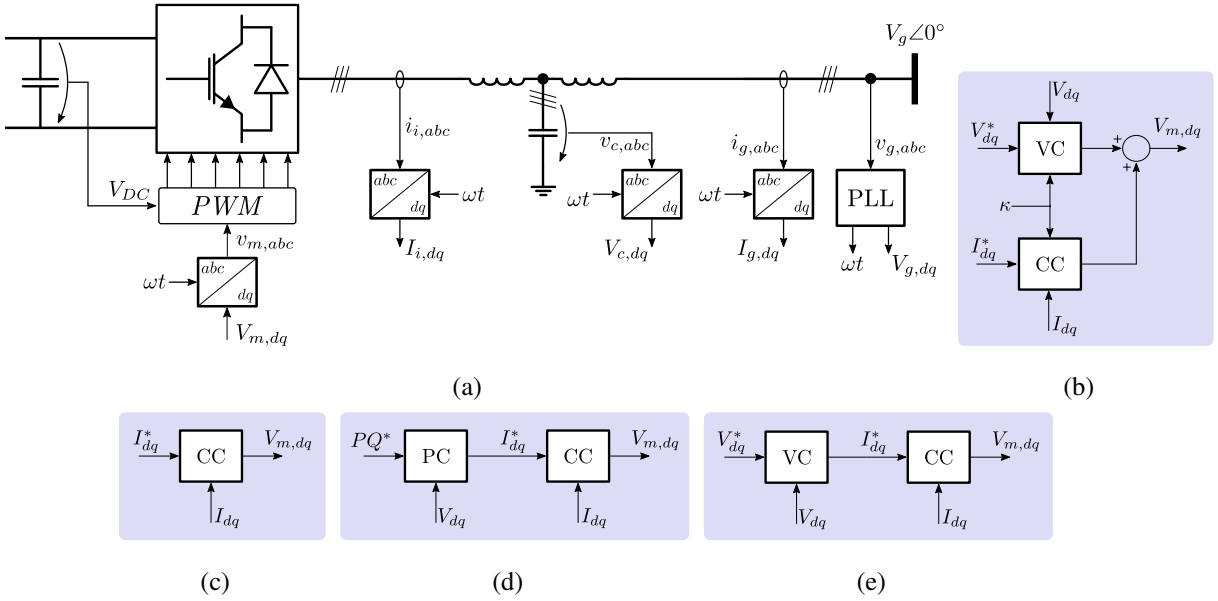


Figure 4.11: Grid-connected VSC schematic. (a) Measurement variables, PLL block and Park transform. (b) Parallel loop. (c) Current control loop. (d) Power control loop. (e) Dual loop - cascaded voltage and current control loops.

can be applied to the power and voltage control loops through the selection of the respective voltage feedback: $V_{c,dq}$ to control power/voltage at the *LCL* capacitor, or $V_{g,dq}$ to control power/voltage at converter output (grid side). The selection of the feedback signals will be a topic of discussion later in this chapter.

In the following subsections, it is described each control loop design.

4.2.1 Current loop

The current control loop is based in the voltage oriented control (VOC). Furthermore, the considered current sign and power factor follow the convention illustrated in figure 4.12.

To simplify the control design, it is considered that the control bandwidth frequency ω_c is significantly lower than the *LCL* filter resonant frequency [91], *e.g.* $\omega_c = 10\omega_0$. When $\omega_c \ll \omega_0$, the *LCL* filter impedance is represented only by the filter inductances, *i.e.* $Z_f = R_f + jX_f$, where R_f and $X_f = j\omega L_f$ refers to the equivalent series resistance and inductance of the filter including the line impedance. Hence, for current control design purposes, the *LCL* filter is represented by a single inductance equivalent to the total *LCL* inductance and the respective resistance, as shown in figure 4.13.

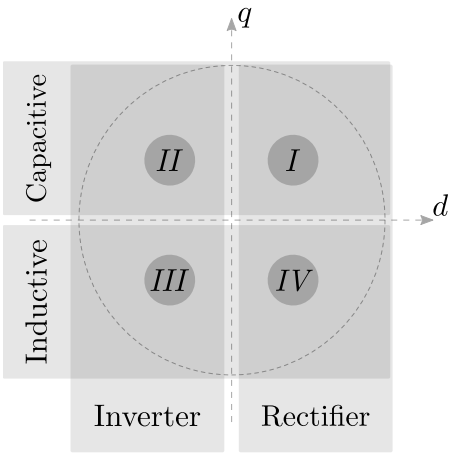


Figure 4.12: Operation regions of the grid-tied converter.

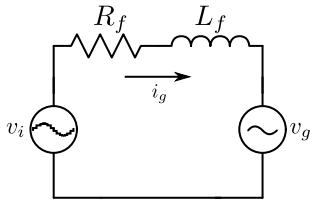
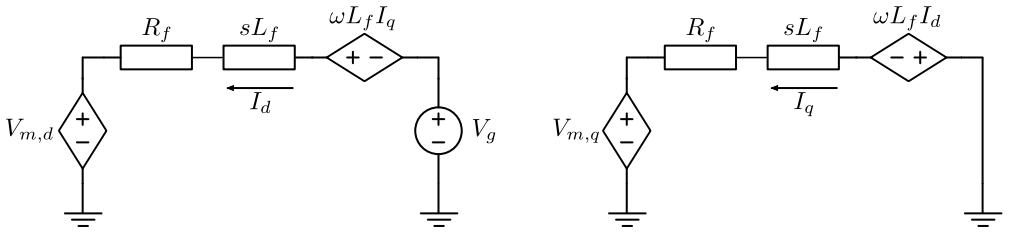


Figure 4.13: Simplified equivalent circuit model for current loop design $\omega_c \ll \omega_0$.

The dynamic circuit diagram of the grid-tied converter is presented in figure 4.14, along with the respective system equations (4.37) [98, 99]. As represented in the figure, there is a compensation of the cross-coupling of the *dq* current components, as will be explained later in this subsection. Furthermore, the null quadrature component of the grid voltage ($V_{g,q} = 0$) indicates that the PLL is synchronized with the grid voltage, therefore the synchronous frame *d*-axis is aligned with $\vec{v}_g$ ($|\vec{v}_g| = V_{g,d} = V_g$).



(a) (b)

Figure 4.14: Equivalent circuit model of the grid-tied converter in the SRF. (a) direct components. (b) quadrature components.

$$\begin{bmatrix} V_g \\ 0 \end{bmatrix} = \begin{bmatrix} V_{m,d} \\ V_{m,q} \end{bmatrix} + sL_f \begin{bmatrix} I_d \\ I_q \end{bmatrix} + \begin{bmatrix} R_f & -\omega L_f \\ \omega L_f & R_f \end{bmatrix} \begin{bmatrix} I_d \\ I_q \end{bmatrix} \tag{4.37}$$

Since the control variable is the modulation voltage $V_{m,dq}$, (4.37) can be rewritten as (4.38). Equation (4.38) represents the system model for the design of the controller of the VOC, where the derivative terms are compensated through the close loop PI controller. The remaining variables are compensated in the forward path. To illustrate the employed control scheme, figure 4.15 is presented, where R_f is considered small and therefore the voltage drop in the filter resistance is neglected.

$$\begin{bmatrix} V_{m,d} \\ V_{m,q} \end{bmatrix} = \begin{bmatrix} V_g \\ 0 \end{bmatrix} - sL_f \begin{bmatrix} I_d \\ I_q \end{bmatrix} - \begin{bmatrix} R_f & -\omega L_f \\ \omega L_f & R_f \end{bmatrix} \begin{bmatrix} I_d \\ I_q \end{bmatrix} \tag{4.38}$$

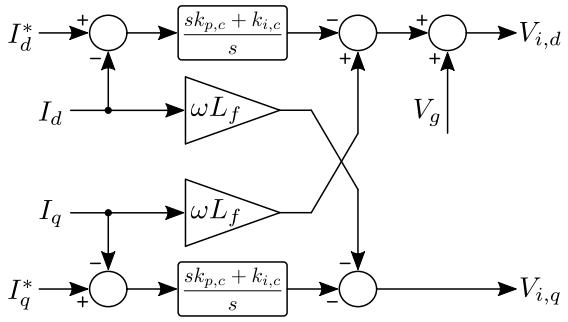


Figure 4.15: Voltage oriented control scheme.

4.2.1.1 Current cross-coupling in the synchronous reference frame

To illustrate the cross-coupling between current components in the SRF, the steady-state per phase phasor diagram is presented in figure 4.16(a). The phasor diagram represents phasors when the converter is operating in the fourth quadrant according to figure 4.12, *i.e.* operating as a rectifier with inductive power factor.

Considering the *dq* components of the current, as shown in figure 4.16(b), when the filter voltage drop V_f is computed, the voltage drop due to the reactance, is reflected in the d axis according to I_q, and in the q axis according to I_d (4.38). Such happens because of the vector rotation, imposed by the reactance ($j = e^{j\frac{\pi}{2}}$) [98]. Though, for the given example, when XI_q is computed, the negative I_q signal forces the vector orientation towards the negative d-axis resulting in an incorrect vector orientation.

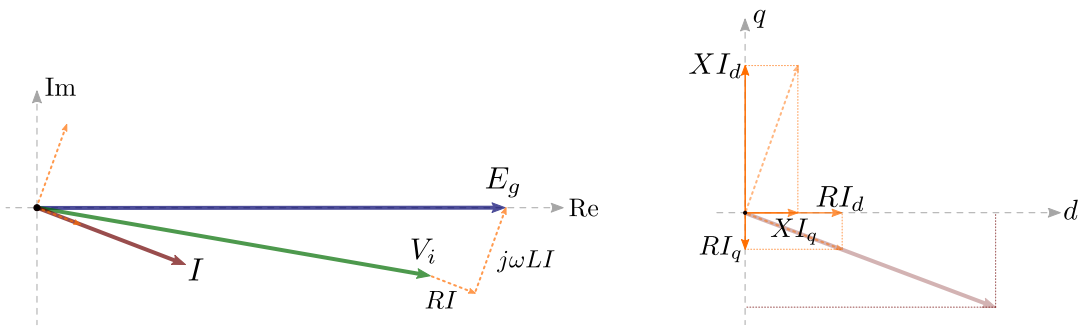


Figure 4.16: Grid-tied converter phasor representation: (a) steady state representation in stationary frame and (b) detail of the steady state voltage drop components in the filter impedance.

Hence, the voltage drop XI_q signal must be inverted to fulfil the phasor diagram presented in figure 4.16(a).

$$Z_f = R + \omega L e^{j\frac{\pi}{2}} \tag{4.39}$$

$$\begin{aligned} V_{f,dq} = I_{dq}\, Z_f \Leftrightarrow \begin{bmatrix} V_{f,d} \\ V_{f,q} \end{bmatrix} &= R \begin{bmatrix} I_d \\ I_q \end{bmatrix} + \omega L \begin{bmatrix} I_d \\ I_q \end{bmatrix} e^{j\frac{\pi}{2}} \Leftrightarrow \\ \Leftrightarrow \begin{bmatrix} V_{f,d} \\ V_{f,q} \end{bmatrix} &= R \begin{bmatrix} I_d \\ I_q \end{bmatrix} + \omega L \begin{bmatrix} -I_q \\ I_d \end{bmatrix} \Leftrightarrow \\ \Leftrightarrow \begin{bmatrix} V_{f,d} \\ V_{f,q} \end{bmatrix} &= \begin{bmatrix} R & -\omega L \\ \omega L & R \end{bmatrix} \begin{bmatrix} I_d \\ I_q \end{bmatrix} \end{aligned} \tag{4.40}$$

4.2.2 Current PI tuning

The PI tuning method applied in this section is based on an analytical closed-loop pole placement technique. First, it is considered that the system open-loop transfer function $P(s)$, given by the simplified *LCL* plant first-order model, is known (4.41). Noteworthy that the considered transfer function is valid only for $\omega_c \ll \omega_0$. Furthermore, uncertainties in the model can be added as system disturbances being analysed afterwards. The control transfer function $C_c(s)$ is designed so that the close loop system transfer function $H_c(s)$ presents a second-order response. In such conditions the control parameters can be obtained by adjusting the desired system natural frequency ω_c and damping factor

ζ [100, 101]. The canonical form of the second-order transfer function is given by (4.42).

$$P_c(s) = \frac{I_i(s)}{E_g(s) - V_i(s)} = \frac{1}{sL_f + R_f} \tag{4.41}$$

$$H(s) = \frac{\omega_c^2}{s^2 + 2\zeta\omega_c s + \omega_c^2} \tag{4.42}$$

A PI controller in its parallel form (4.43) is added to the control loop, resulting in the closed-loop transfer function H_c (4.44), or (4.45) when rewritten in the canonical form.

$$C_c(s) = \frac{k_{p,c}s + k_{i,c}}{s} \tag{4.43}$$

$$H_c(s) = \frac{P_c(s)C_c(s)}{1 + P_c(s)C_c(s)} = \frac{k_{p,c}s + k_{i,c}}{L_f s^2 + (k_{p,c} + R_f)s + k_{i,c}} \tag{4.44}$$

$$H_c(s) = \frac{\frac{k_{p,c}}{L_f}s + \frac{k_{i,c}}{L_f}}{s^2 + \frac{k_{p,c}+R_f}{L_f}s + \frac{k_{i,c}}{L_f}} = \frac{k_{i,c}}{L_f}\frac{\frac{k_{p,c}}{k_{i,c}}s + 1}{s^2 + \frac{k_{p,c}+R_f}{L_f}s + \frac{k_{i,c}}{L_f}} \tag{4.45}$$

Observing the closed-loop transfer function $H_c(s)$, it is noticeable that the system presents a zero which will result in a high overshoot on the reference to output step response. Hence, as suggested in [100], the controller design is carried considering the characteristic equation, *i.e.* the denominator on (4.45), and further compensating the zero.

The controller zero is placed considering the transfer function H_c characteristic equation, according to the controller gains $k_{p,c}$ and $k_{i,c}$. Hence, the PI gains are tuned aiming to model the closed-loop system response based on the second-order system characteristic equation (4.46). For a given settling time $t_{ss,c}$ and damping ζ_c, the PI gains can be calculated applying the equation system (4.47).

$$s^2 + \frac{k_{p,c} + R_f}{L_f}s + \frac{k_{i,c}}{L_f} = s^2 + 2\zeta\omega_c s + \omega_c^2 \tag{4.46}$$

$$\begin{cases} \omega_{c,c} = & \dfrac{4}{\zeta_c t_{ss,c}} \\ k_{p,c} = & 2L_f\zeta_c\omega_{c,c} - R_f \\ k_{i,c} = & L_f\omega_{c,c}^2 \end{cases} \Leftrightarrow \begin{cases} k_{p,c} = & \dfrac{8L_f}{t_{ss,c}} - R_f \\ k_{i,c} = & \dfrac{16L_f}{(\zeta_c t_{ss,c})^2} \end{cases} \tag{4.47}$$

The reference (set-point) to output transfer function, presents a zero at $z = -k_{i,c}/k_{p,c}$. To cancel its effect, a first-order low-pass filter is added to the current reference (4.48), with a pole placed at

$-k_{i,c}/k_{p,c}$ ($\tau_{r,c} = k_{p,c}/k_{i,c}$). To avoid a reference to output overshoot, independently of the chosen $\zeta_c(\leq 1)$ in equation (4.47), the reference time constant $\tau_{r,c}$ is calculated for $\zeta_c = 1$ (4.49).

$$F_c(s) = \frac{1}{\tau_{r,c}s + 1} \tag{4.48}$$

$$\tau_{r,c} = \frac{8L_f t_{ss,c} - R_f t_{ss,c}^2}{16L_f} \tag{4.49}$$

When considering the reference filter, the closed-loop transfer function (4.45) results in (4.50), allowing to obtain the desired closed-loop system response. Noteworthy, that the reference filter only affects the reference forward system path, *i.e.* does not influence the system response to perturbations or noise.

$$H_c(s) = \frac{F_c(s)P_c(s)C_c(s)}{1 + P_c(s)C_c(s)} = \frac{\frac{k_{i,c}}{L_f}}{s^2 + \frac{k_{p,c}+R_f}{L_f}s + \frac{k_{i,c}}{L_f}} \tag{4.50}$$

Another important condition to discuss in the implementation of the current controller, is the fact that the controller output is limited by hardware constraints. As an example, to guarantee proper filtering of the converter currents, it is important to operate in the linear region of the modulation, *i.e.* amplitude modulation index m_a should not become higher than unity. Hence, in order to prevent over-modulation ($m_a > 1$) the current controller output must be limited to $|V^*_{m,dq}| \leq V_{bus}/2$ to the SPWM scheme, or $|V^*_{m,dq}| \leq 1.15V_{bus}/2$ for the third-harmonic injection pulse-width modulation (THIPWM) or space vector PWM (SVPWM) schemes [102]. When the controller output becomes saturated, due to the imposed output limit, the integral winds up (undesired accumulation of the error) and may lead to the saturation of the integral action, oscillations in the control dynamics, and ultimately lead to the system instability [100]. To prevent such behaviour, the anti-windup scheme illustrated in figure 4.17 is added. When the PI output is saturated by the output limiter, the difference between the PI and the limiter outputs is non-zero and the integral action is disabled (clamped). Such behaviour is equivalent to the known back-calculation method when the back-calculation and integral gains are equivalent. While clamped, the integral output is maintained, but the error is not accumulated (no windup). Once the PI and limiter outputs become equal (no output saturation) the integral action is enabled again. Since the PI acts independently in the direct and quadrature current components, a second saturation is added to guarantee that the modulation voltage $V^*_{m,dq}$ calculated by the current controller is lower than the maximum allowed modulation voltage. This second saturation stage is

performed through equation (4.51), where the saturation is weighted over the dq component, allowing the modulation voltage vector rotation within the SRF ($V_{g,d}/V_{g,q}$ ratio change) even when modulation voltage is saturated.

The final current control loop is presented in figure 4.18, where decoupling is fed with the reference currents to reduce measurement noise perturbation in the control loop. Furthermore, voltage forward compensation is provided by the PLL during grid-following operation, or by the voltage loop reference, when operating in grid-forming.

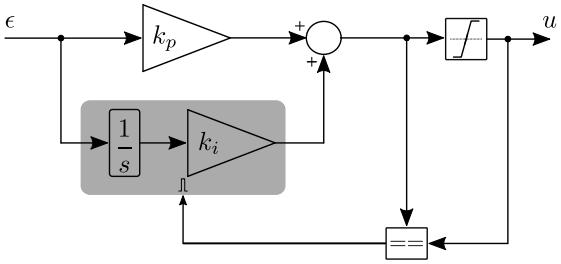


Figure 4.17: Generic PI block diagram including anti-windup clamping.

$$\begin{cases} |V_{m,dq}|^2 = V_{m,d}^2 + V_{m,q}^2 \\ V_{m,d}^* = \dfrac{V_{m,d}}{|V_{m,d}|}\sqrt{\dfrac{V_{m,d}^2}{|V_{m,dq}|^2}} \\ V_{m,q}^* = \dfrac{V_{m,q}}{|V_{m,q}|}\sqrt{\dfrac{V_{m,q}^2}{|V_{m,dq}|^2}} \end{cases} \tag{4.51}$$

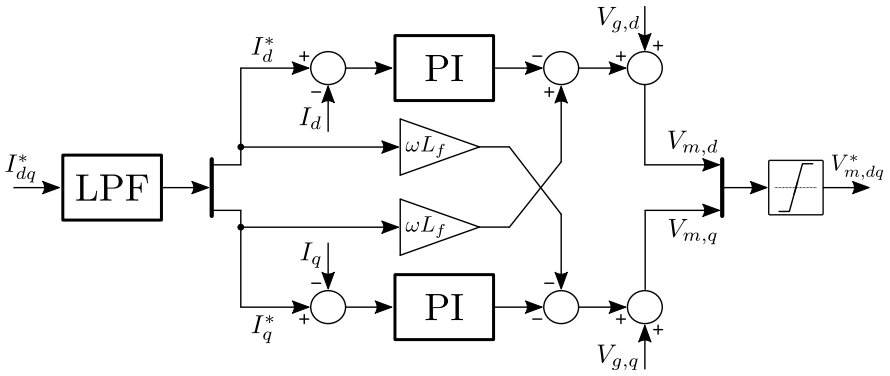


Figure 4.18: dq Current control loop with PI, anti-windup, voltage forward compensation, current decoupling, and modulation voltage saturation.

4.2.3 Power calculation

The power calculation of a three-phase balanced system in the synchronous reference frame is given by (4.52). Furthermore, if power is controlled at the reference voltage node and synchronism transients are neglected (PLL dynamics), then the voltage quadrature component is considered null and (4.52) becomes (4.53).

$$\begin{cases} P = \dfrac{3}{2}\left(V_d I_d + V_q I_q\right) \\ Q = \dfrac{3}{2}\left(V_q I_d - V_d I_q\right) \end{cases} \tag{4.52}$$

$$\begin{cases} P = \dfrac{3}{2} V_d I_d \\ Q = -\dfrac{3}{2} V_d I_q \end{cases} \tag{4.53}$$

To control the converter as a controllable power source (PC) in the grid-following operation, the power equation (4.52) is rewritten to obtain the reference current I^*_{dq} that results in the desired power P^* and Q^* (4.54). Noteworthy that, in a practical implementation of this method, the measured voltage should be properly filtered, otherwise it will result in current reference oscillations. When power control performs at the reference voltage node (voltage feedback node), the PLL ensures that $V_q = 0$, allowing to simplify (4.54) into (4.55).

$$\begin{cases} I^*_d = \dfrac{2}{3}\dfrac{V_d P^* + V_q Q^*}{V_d^2 + V_q^2} \\ I^*_q = -\dfrac{2}{3}\dfrac{V_q P^* - V_d Q^*}{V_d^2 + V_q^2} \end{cases} \tag{4.54}$$

$$\begin{cases} I^*_d = \dfrac{2}{3}\dfrac{P^*}{V_d} \\ I^*_q = -\dfrac{2}{3}\dfrac{Q^*}{V_d} \end{cases} \tag{4.55}$$

4.2.4 Voltage loop

This section discusses two different voltage control (VC) strategies: the dual loop and parallel loop. The dual-loop is the conventional approach for the VC of grid-forming or grid-firming converters, where the voltage loop control variable is the reference current I^*_{dq} that is fed into the inner CC loop. In the parallel loop, the voltage loop control variable is the modulation voltage $V^*_{m,dq}$ and the current instead of being controlled, is only monitored. Though once the monitored current surpasses

the converter current limits, the CC added in parallel is enabled and the converter voltage is limited by the CC. The last will be discussed further in subsection 4.2.4.2. Noteworthy that, independently of the VC strategy, the CC is designed as mentioned in the previous subsection.

4.2.4.1 Dual loop voltage controller tuning

When the VC is cascaded with the CC, forming a dual loop control, the resulting system can be seen as a current source whose dynamics is dictated by the current control loop. Such assumption allows considering the VSC as a current source connected to the *LCL* capacitor, as shown in figure 4.19.

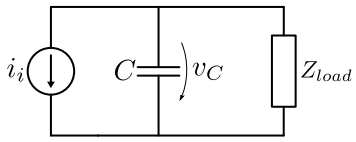
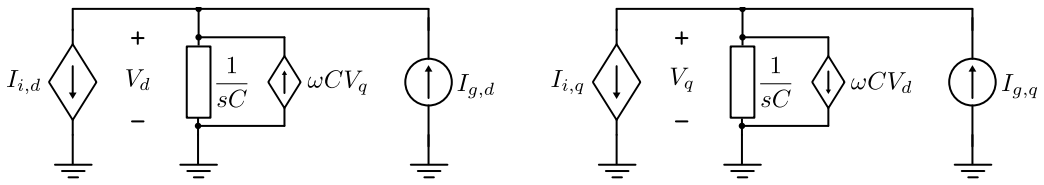


Figure 4.19: Simplified equivalent circuit model for the voltage control loop design.

The voltage control (VC) design is based on the simplified plant model of figure 4.19, where the current source i_i (or i_g), allows to regulate the voltage in the *LCL* capacitor C or the sensing resistors at the filter output. Since load Z_{load} is uncertain, it is considered as a system disturbance. Under the previously described assumptions, the equivalent circuit of figure 4.20 is obtained, along with the respective node equations (4.56).



(a) (b)

Figure 4.20: Dynamic model of the grid-forming converter in the SRF. (a) direct components. (b) quadrature components.

$$\begin{bmatrix} I_{i,d} \\ I_{i,q} \end{bmatrix} = \begin{bmatrix} I_{g,d} \\ I_{g,q} \end{bmatrix} - sC \begin{bmatrix} V_{c,d} \\ V_{c,q} \end{bmatrix} - \omega C \begin{bmatrix} -V_{c,q} \\ V_{c,d} \end{bmatrix} \tag{4.56}$$

As earlier mentioned, and to avoid using additional current sensors, the first term of equation (4.56) is disregarded. Hence, the plant model becomes a single C (4.57), where decoupling is forward

compensated. Noteworthy that with such simplification, the $I_{i,dq}$ current can be either the current sensed at the inverter-side or grid-side inductance. When current is sensed at grid-side inductance and pre-synchronism is desired, it is required to add some load to the filter output, *e.g.* the voltage sensing resistances. Otherwise, it is not possible to form the voltage before connection with the microgrid.

Adding the respective PI, similar to the current loop design, results in the close loop transfer function (4.58), as also suggested in [102, 103]. Following the same strategy, employed on the current loop design on subsection 4.2.1, the VC gains can be calculated by (4.59).

$$P_v(s) = \frac{1}{sC} \tag{4.57}$$

$$C_v(s) = \frac{k_{p,v}s + k_{i,v}}{s} \tag{4.58}$$

$$H_v(s) = \frac{k_{i,v}}{C} \frac{\frac{k_{p,v}}{k_{i,v}}s + 1}{s^2 + \frac{k_{p,v}}{C}s + \frac{k_{i,v}}{C}} \tag{4.59}$$

$$H_v(s) = \frac{k_{i,v}}{C} \frac{\frac{k_{p,v}}{k_{i,v}}s + 1}{s^2 + \frac{k_{p,v}}{C}s + \frac{k_{i,v}}{C}} \tag{4.60}$$

$$\begin{cases} \omega_{c,v} = & \frac{4}{\zeta_v t_{ss,v}} \\ k_{p,v} = & 2C\zeta_v\omega_{c,v} \\ k_{i,v} = & C\omega_{c,v}^2 \end{cases} \Leftrightarrow \begin{cases} k_{p,v} = & \frac{8C}{t_{ss,v}} \\ k_{i,v} = & \frac{16C}{(\zeta_v t_{ss,v})^2} \end{cases} \tag{4.61}$$

To reduce the delay introduced by the current control loop, the CC reference low pass filter is removed, when operating with the dual-loop, and is instead introduced at the VC reference (4.62).

$$F_v(s) = \frac{1}{\tau_{r,v}s + 1}, \quad \tau_{r,v} = \max\left\{5\tau_{r,c}, \frac{k_{p,v}}{k_{i,v}}\right\} \tag{4.62}$$

In figure 4.21 it is represented the complete block diagram of the dual-loop controller, including the voltage and current control loops. In the figure, voltages and currents do not present any subscript but can be relative to the grid or capacitor voltages, and grid or inverter side currents.

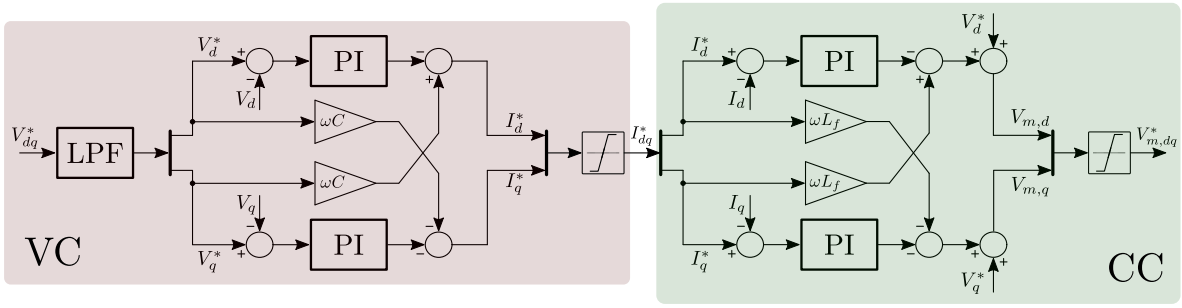


Figure 4.21: Dual loop control block diagram.

4.2.4.2 Parallel loop tuning

The parallel loop operation principle is based on typical workbench power supplies, and it is supported by the VOC presented earlier in subsection 4.2.1. The VSC behaves as a voltage source when operating in an open-loop, hence its characteristic is exploited for the grid-forming operation. During the normal operation of the parallel loop, the modulation voltage is generated based on the reference voltage, in a feed-forward manner, allowing a voltage control dynamic as fast as the converter hardware and load allows to. To limit the voltage reference rate of change, the voltage reference is filtered as in the case of the dual loop.

The parallel loop can also include an additional loop in case that the desired regulated voltage is not at the converter bridge output v_m, *e.g.* choose regulating the capacitors voltage (v_c), or grid voltage (v_g) instead. With such consideration, the feed-forward path also accounts for the voltage drop at filter impedance (current measurement needed). Furthermore, a voltage close loop is added to ensure that reference voltage is followed. To achieve it, a simple error integral is sufficient to ensure zero steady-state error.

The parallel loop, as described so far, presents a major flaw since the converter current is not regulated. During grid-forming operation, current regulation is important mainly for the protection of the power converter (avoiding operation with over-currents). In the dual loop, the inner current loop ensures that such a situation does not happen. To add the demanded current protection, a second loop is added in parallel to the VC and feed-forward path [104]. When current crosses the maximum allowed current, an over-current detector (OCD) generates a flag that clamps the voltage integral, and enables the added current control (CC), allowing it to regulate the converter current.

The added current loop integrates a PI, designed as explained in subsection 4.2.2, without including the reference filter and feed-forward voltages, as these are already included in the VC. The

decoupling can be disregarded if v_m is chosen, otherwise decoupling is already included in the feed-forward path of the VC.

To illustrate the described control principle, the block diagram of figure 4.22 is presented.

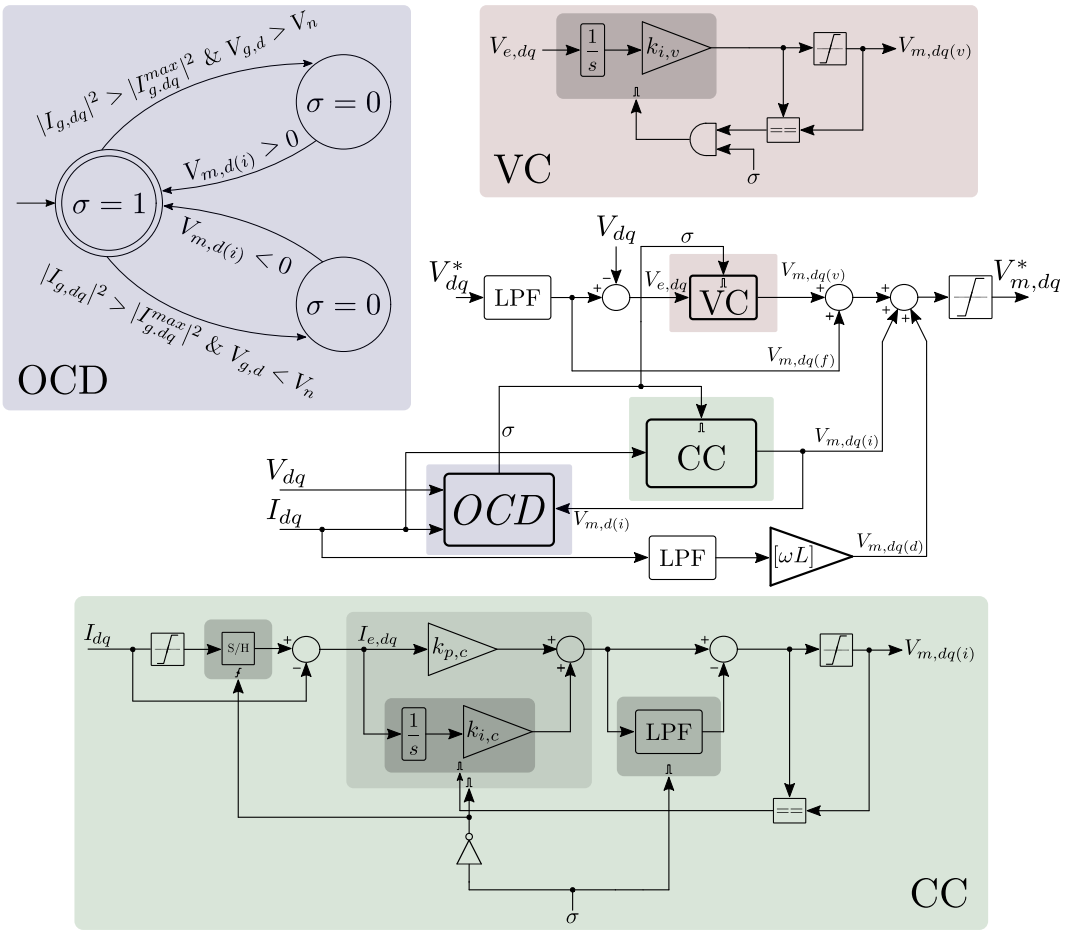


Figure 4.22: Parallel loop control block diagram.

In the figure, it is noticeable that the modulation voltage $V_{m,dq}$ is generated through the combination of the feed-forward voltage $V_{m,dq(f)}$, the VC voltage $V_{m,dq(v)}$, decoupling voltage $V_{m,dq(d)}$, and the CC voltage $V_{m,dq(i)}$. As mentioned before, if the reference voltage is chosen at converter output (v_m), the system block is further simplified, as the VC and decoupling are disregarded. Though such an approach does not ensure regulation of the voltage with null steady-state error, as no feedback voltage exists, and the produced modulated voltage presents non-null steady-state errors inherent to the PWM scheme and uncertainty in the semi-conductors impedance. The low-pass filter present in the decoupling path is added to ensure that the measured current does not introduce undesired current harmonics or measurement noise in the current decoupling control variable $V_{m,dq(d)}$.

A low-pass filter is also added to the CC, to flush the PI integral accumulated error, *i.e.* bring the integral error back to zero and reset the controller state variables. In the figure 4.22, it can be noticed that the low-pass filter is enabled only when no over-current is detected ($\sigma = 1$). Adding the flush low-pass filter (LPF) is of high importance to prevent the CC integral windup and minimize system perturbation during the transition from current to voltage control. To be noticed that, if the integral buffer is not flushed, the integral buffer remains unchanged between successive overload occurrences. Additionally, if the CC integral is reset without flushing, it introduces a step-change in the control variable $V_{m,dq(i)}$ and consequently a disturbance in the voltage regulation. To prevent such behaviour, the flush LPF should be tuned with a time constant higher or equal to the voltage control loop one, so that the integral flush can be seamlessly compensated by the voltage integral action.

The over-current detection $\sigma = 0$ is simple since it only requires processing the SRF current magnitude and comparing it with the configured limit. The challenge of the OCD is focused on identifying when the system is back to normal operation ($\sigma = 1$). In a typical application where no more sources contribute for forming the grid, the OCD presented in figure 4.22 is sufficient. Though, when parallel sources contribute to support the formed grid, the more complete scheme presented in figure 4.23 should be considered. The difference between both OCD's will be discussed later in section 5.3.4 of chapter 5.

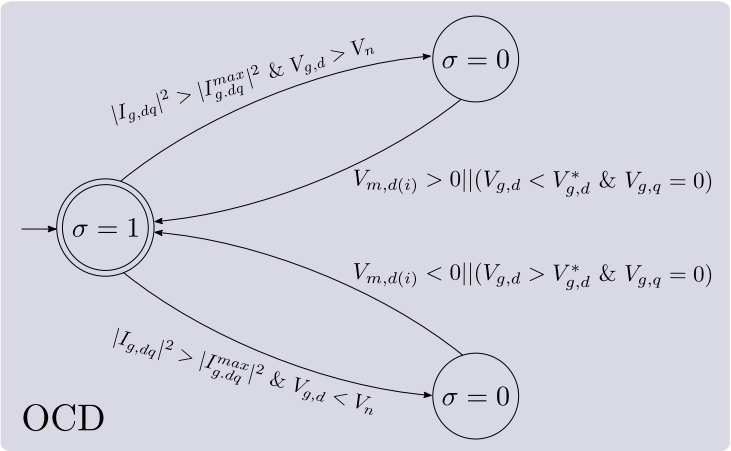


Figure 4.23: OCD scheme for the VC-PL operation with multiple sources.

To design the VC loop, a plant with a unitary gain is considered (4.63). Adding the integrative action over the voltage error (4.64), results in the close loop system (4.65). The integral gain $k_{i,v}$ is determined based on the desired settling time t_{ss}, through equations (4.66). In (4.66) it is also

included the choice condition for the CC flush low-pass filter cut-off frequency ω_{fl}. The voltage reference filter is the same used in the dual loop (4.62). An alternative implementation of the parallel loop is presented in [104], where the parallel loop is as described in the current section, but it uses the voltage feedback from the PLL. In such conditions, the quadrature voltage zero error is ensured by the PLL. Consequently, the voltage integral only acts over the direct voltage component. When the PLL feedback is used, the voltage integral should be in accordance with the PLL dynamics.

$$P_v(s) = 1 \tag{4.63}$$

$$C_v(s) = \frac{k_{i,v}}{s} \tag{4.64}$$

$$H_v(s) = \frac{1}{\tau_{i,v}s + 1} \tag{4.65}$$

$$\begin{cases} \tau_{i,v} = \dfrac{t_{ss,v}}{4} \\ k_{i,v} = \dfrac{1}{\tau_{i,v}} \\ \omega_{fl} \leq k_{i,v} \end{cases} \tag{4.66}$$

4.3 Chapter results and discussion

In this section it is presented the simulation results obtained for validation of the *LCL* filter and controller designs. Noteworthy, that the chosen PLL is the fixed-frequency double second-order generalized integrator (FFDSOGI) presented in chapter 3.

The current controller is validated through the analysis of the system response to reference changes and perturbations. The simulation results are obtained through the co-simulation between *Matlab/ Simulink* and *Ansys Simplorer*. The control system is discretized, using Tustin's method, and model in the *Matlab/ Simulink*. The PWM generation, converter hardware, and loads are modelled in the *Ansys Simplorer*. The control and hardware are delimited by the orange and blue squares in figures 4.24 and 4.30.

The *LCL* design performance, including the current control loop and PLL dynamics, is evaluated through the analysis of the produced total demand distortion (TDD). The filter is analyzed considering: passive damping with R_d, and without damping (respecting the critical frequency criteria

discussed in the previous section). Furthermore, the damped and undamped designs are analyzed considering the grid or inverter side current feedback, to the current control loop.

4.3.1 *LCL* filter and current controller

To validate the controller gains, it was considered three different *LCL* designs, obtained with the algorithm presented in subsection 4.1.2, for different K_{pwm} and K_{R_d}. The filter designs #1 and #3 represent undamped filters operating respectively with the single and double update PWM. The design #2 represents a resistive damped filter and hence it can be operated with single or double update PWM. Additionally, for each design, it was calculated the respective current controller gains following the analytical approach presented in subsection 4.2.2. The obtained parameters are summarized in table 4.5. In the three designs, the restrictions are a settling time of at least half of the grid voltage waveform period ($< 10\ ms$ to reach 95 % of the reference) and present a minimum overshoot in the reference to output step response (< 5 %). For a first-order filter response, the maximum τ_{max} that comply with the desired settling time is given by (4.67), therefore the time constant of the reference filter must be $\tau_r < \tau_{max}$.

$$\tau_{max} = \frac{-0.01}{\ln(1-0.95)} \approx 3.34\ ms \tag{4.67}$$

In table 4.5 the design #1 and #3 were obtained considering no damping in the *LCL* filter, where #1 is obtained for single update PWM (SUPWM) and #3 to the double update PWM (DUPWM). The design #2 considers resistive damping, hence it is equally suitable for operation with SUPWM or DUPWM.

Table 4.5: *LCL* filter and current controller parameters obtained for different designs.

	LCL filter								Current controller				
Design	K_{pwm}	K_{R_d}	k_f	x	L_i	L_g	C	R_d	$\omega_{c,c}$	ζ_c	$k_{p,c}$	$k_{i,c}$	$\tau_{r,c}$
#1	1	0	2.966	2.5 %	1196 μH	1196 μH	15 μF	0.0 Ω	1056 rad/s	1	4.998	2667	1.874 ms
#2	1, 2	1	2.999	2.5 %	1224 μH	1224 μH	15 μF	2.1 Ω	1044 rad/s	1	5.057	2667	1.896 ms
#3	2	0	2.121	0.6 %	2667 μH	2667 μH	4 μF	0.0 Ω	1370 rad/s	1	14.55	10000	1.455 ms

To validate the controller and *LCL* filter, the circuit illustrated in figure 4.25 is considered. As mentioned before, the control loop was discretized through the Tustin's method for a sampling rate of $T_s = 1/(2f_{sw})$ when $K_{pwm} = 2$ (double update PWM), and $T_s = 1/f_{sw}$ when $K_{pwm} = 1$ (single update

PWM). The current and voltage is sensed at grid side (or filter output) and $V_{pcc} = V_n$. The loads $Z_{load,1}$ and $Z_{load,2}$ are connected to evaluate the converter response to system disturbances. The load $Z_{load,1}$ is a linear load of 30 kVA with a power factor of 90 % (at nominal voltage), and $Z_{load,2}$ represents a three phase rectifier with a fire angle at 32° and a DC load $R = 10\ \Omega$, which is equivalent to a DC power of $\approx 30\ kW$ (at nominal voltage). The L_ℓ represents the line inductance from the local loads to the PCC with a value of 320 μH.

The simulation tests were performed into two stages:

1) The first stage aims to validate the transient response of the current controller. At starting simulation, the converter is already synced with the grid voltage with a null current reference $I^*_{dq} = [0;\ 0]\ A$. At time instant t_0, the converter is set to operate in rectifying mode at maximum current $I^*_{dq} = [I_n;\ 0]\ A$ and later, at t_1, the VSC is changed to inverter mode $I^*_{dq} = [-I_n;\ 0]\ A$. The loads $Z_{load,1}$ and $Z_{load,2}$ are connected to the grid respectively at time instants t_2 and t_3. Both loads are switched off simultaneously at time instant t_4;

2) During the second stage, it is analysed the steady-state response of the converter, when connected to a strong grid (L_ℓ is reduced to 10 %). The objective is to quantify the converter injected harmonic content (TDD analysis) accordingly with IEEE 519 standard. Hence, loads are disconnected and currents are analysed in steady-state with the converter operating as an inverter with unit power factor.

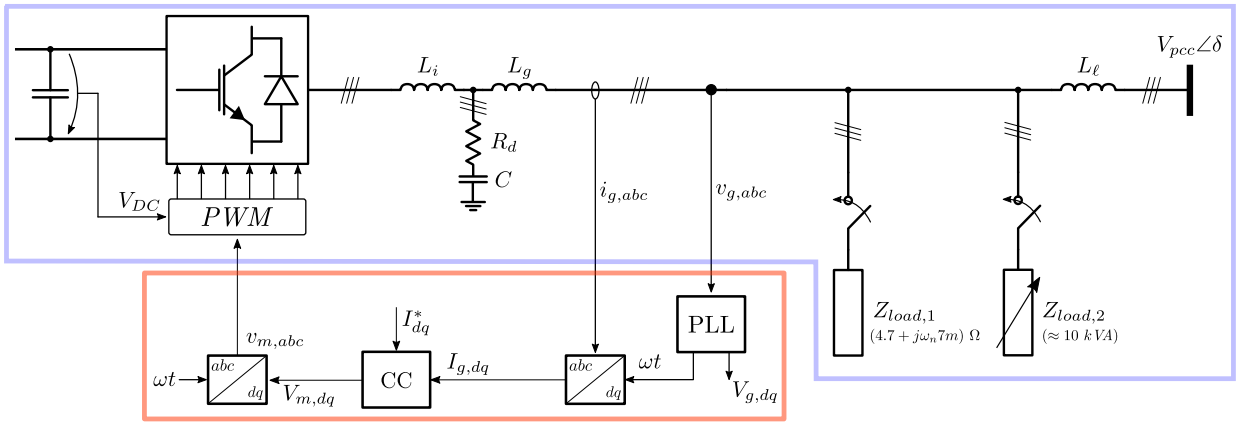
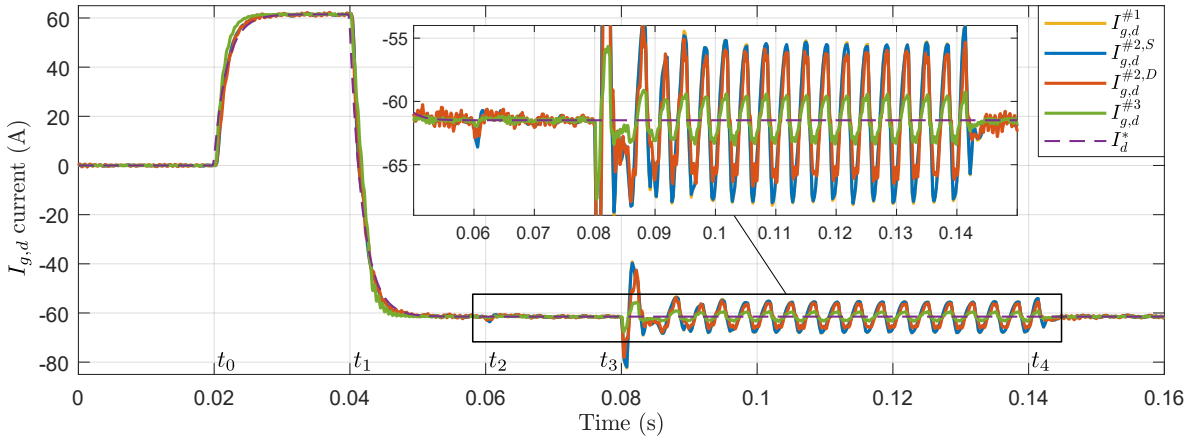


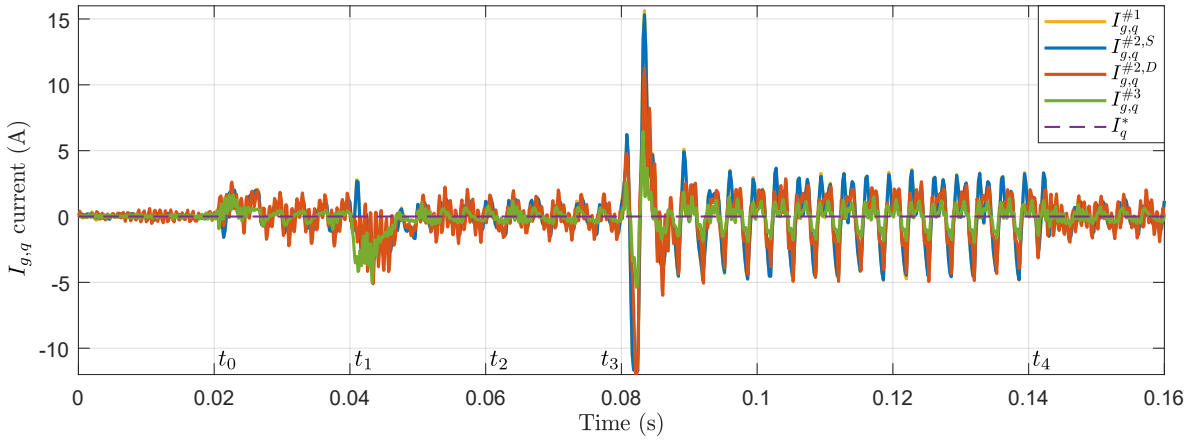
Figure 4.24: Current controller and *LCL* design validation circuit.

4.3.1.1 Current controller transient test

Figure 4.25 shows the first stage simulation results obtained for the designs of table 4.5. Noteworthy, that each design has its current reference I^*_{dq} (due to different τ_{cr}) though, differences between reference curves are hardly distinguishable and for that reason, it was omitted from figure 4.25. The I^*_{dq} current references are represented by the purple dashed lines I^*_d and I^*_q. The yellow and green lines represent respectively the measured synchronous currents ($I_{g,d}$ and $I_{g,q}$) for the designs #1 and #3. The design #2 currents are represented by the lines in blue and red, for the single and double update methods respectively.



(a)



(b)

Figure 4.25: VSC current controller synchronous grid side currents for the first stage simulation tests: (a) direct, and (b) quadrature current components.

Figure 4.26 illustrates the current at reference phase 'a', obtained for the different designs. Addi-

tionally, it is also shown the grid voltage obtained for the design #2, D test (similar for all tests).

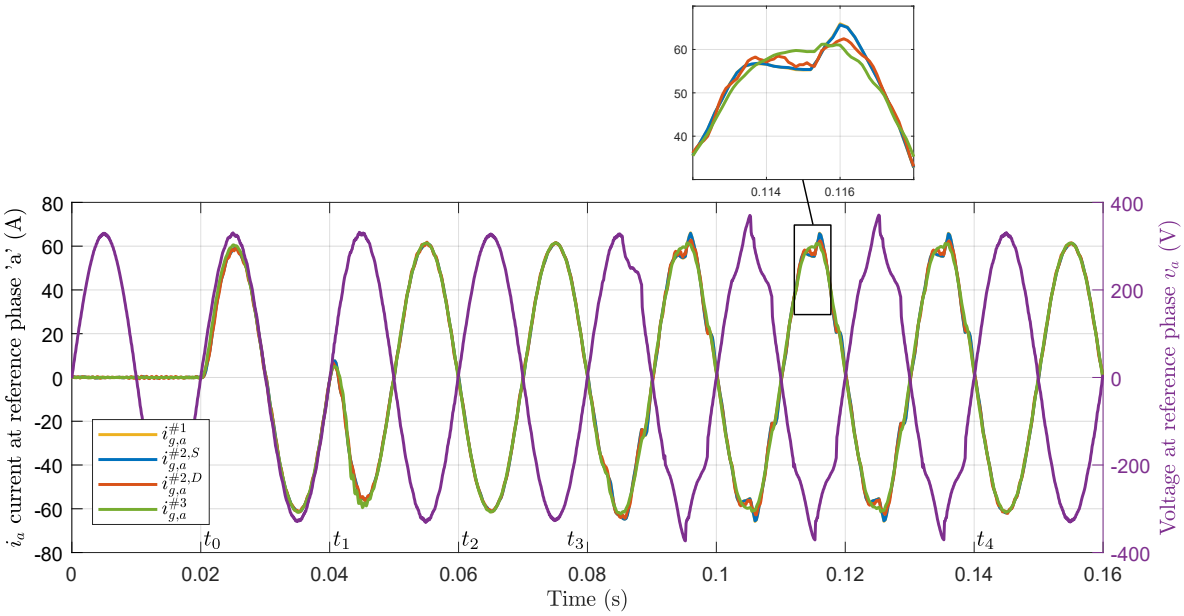


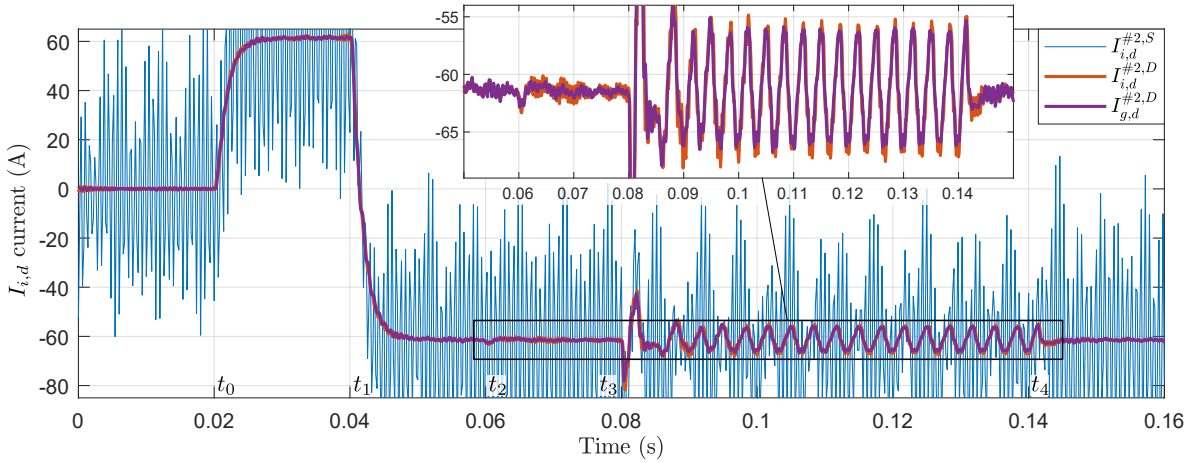
Figure 4.26: VSC filter output current and voltage at reference phase $'a'$, obtained for the different designs.

Since the controller design and gains are the same for the direct and quadrature current components, similar results were obtained, as it can be perceived through the comparison of the current curves from figures 4.25(a) and (b).

The dynamic behaviour at time instants t_0 and t_1 allows concluding that the controller design fulfils the settling time and overshoot requirements for all the given design examples.

The balanced load connection (at t_2) introduces a barely noticeable transient response, with no impact in the steady-state current regulation. The non-linear load connection (at $t3$) has a greater transient response impact and deteriorates the steady-state regulation. The non-linear load introduces low-order harmonics generated by the thyristor active rectifier, resulting in distorted local grid voltage and consequently results in converter current oscillations. The voltage distortion caused by the non-linear load $Z_{load,2}$ can be visualized in the voltage waveform of figure 4.26. The designs #1 and #2, S (#2 for the SUPWM) results are hardly discriminated, but the similar behaviour allows to validate the stability criteria applied for the undamped design. To be noticed that the design #1 does not include the damping resistance R_d while design #2 does. The designs #2, S and #2, D (DUPWM) are referred to the same LCL filter and current gains, where the only difference between both is in the PWM update sampling times. When comparing both, it is observable that the #2, D presents better dynamics

during system load change, as indicated by the lower overshoots (at t_2 and t_3), and lower oscillations while feeding the non-linear load (between time instants t_3 to t_4). The design #3 outperform the other designs, at the cost of a considerable larger inductance (increased filter size). When the *LCL* transfer function is considered, it becomes obvious that the total filter inductance $L_i + L_g$ is responsible for the attenuation of low order harmonics (harmonics which frequency is smaller than the filter resonant frequency). Such facts justify the better performance of the design #3. Nevertheless, the harmonic disturbance is only included in the simulation tests to guarantee that such loads would not lead the controllers to instability, since complementary control methods could be included to compensate such harmonics.



(a)

Figure 4.27: Design #2 inverter side current control $I_{i,d}$.

Figure 4.27 presents the same test of figure 4.26, but considering the feedback from inverter side current $I_{i,dq}$. In the figure, it is also included $I_{g,d}^{\#2,D}$, from figure 4.26, for comparison purposes. Since the undamped schemes are only stable for grid side current control, the test was performed only for the design #2.

Through the observation of figure 4.27, it is noticeable the poor performance of the SUPWM when inverter side currents are chosen over the grid side ones. The DUPWM presents very similar results for both currents, which is a good indicator of the higher robustness of the PWM update method.

4.3.1.2 Steady-state test results

The harmonic content obtained during the steady-state results is shown in figure 4.28, where it is

represented the individual current harmonics content for the designs presented in table 4.5, with i_g as the feedback current. In figure 4.29, it is represented the harmonic content when inverter side currents i_i are chosen over i_g. The TDD obtained for each design is summarized in table 4.6, where i_i^* and i_g^* indicate if the current was controlled in the grid or inverter side inductance. For the un-damped designs, controlling the current at the inverter side leads to instability, therefore harmonics are not presented in these cases. The amplitude of the harmonic h_k, is the sum of the amplitude at frequency $f_k = h_k f_n$ with the neighbour harmonics amplitudes ($\pm 5\ Hz$ bin), as recommended in IEEE-519.

Table 4.6: TDD for the steady state analysis of the different filter and current controller designs.

	#1 (i_g)	#2, S (i_i)	#2, S (i_g)	#2, D (i_i)	#2, D (i_g)	#3 (i_g)	Limit (%)
$\text{TDD}_{I_{i,a}}$ $(\%I_n)$	8.7	8.6	8.5	8.4	8.4	4.3	10*
$\text{TDD}_{I_{g,a}}$ $(\%I_n)$	2.4	2.7	2.3	1.9	2.3	1.2	5.0

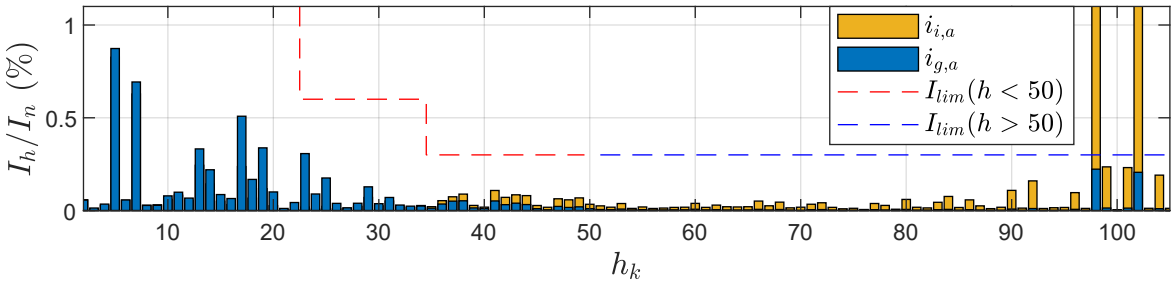
* limit set by design.

Analysing the results obtained in figure 4.28, it is clear that the produced TDD for all designs are within the IEEE-519 limits. Though the individual limits are crossed by the DUPWM methods with grid side current i_g feedback. Furthermore, all designs presented a TDD considerably lower than the IEEE-519 limits, validating the *LCL* design algorithm. As expected, the higher amplitude odd harmonics are concentrated in the lower frequencies, $h_k = \{5,\ 7\}$. The harmonics presented in figure 4.28 excludes the fundamental frequency component.

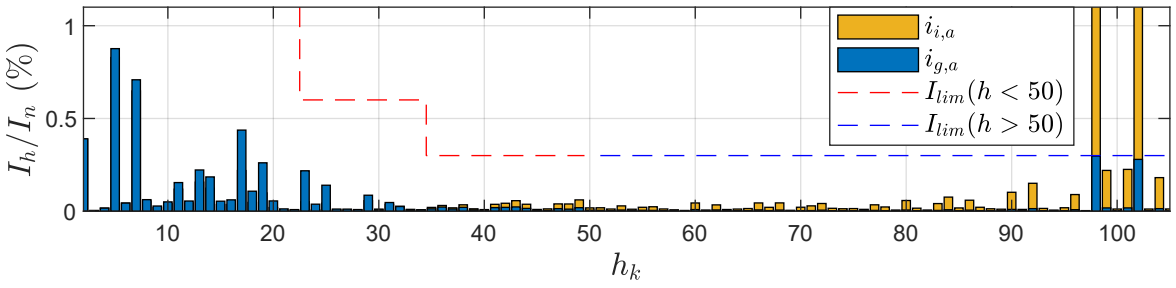
The design #3, in figure 4.28(d), is the design that presents lower harmonic content as expected and discussed in the previous subsection. The larger inductance reduces significantly the inverter side harmonics and consequently, the grid side harmonics content is improved over the overall spectrum. Despite presenting a single harmonic at $h_k = 35$ (near the resonant frequency $h_k = 33$) that crosses the recommended value, the design performance is still very satisfactory. Eliminating such individual harmonic would be achievable, *e.g.* by reducing the controller damping ζ. The same idea can be applied to the #2, D design, of figure 4.28(c), where the limit is violated at $h_k = 25$.

When comparing designs #1 and #2, $S(i_g)$, of figures 4.28 (a) and (b), it can be seen that the second presents lower harmonic content, since it presents a lower resonant frequency (higher inductance for the same capacitance).

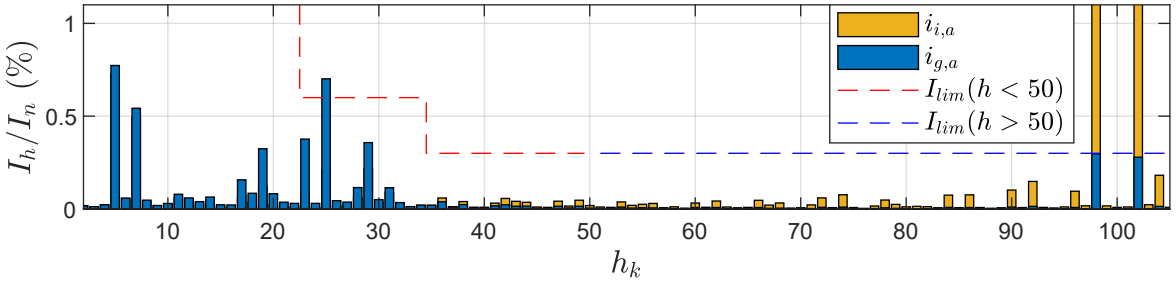
The resultant harmonics for the SUPWM and DUPWM, of figures 4.28 (b) and (c), indicates



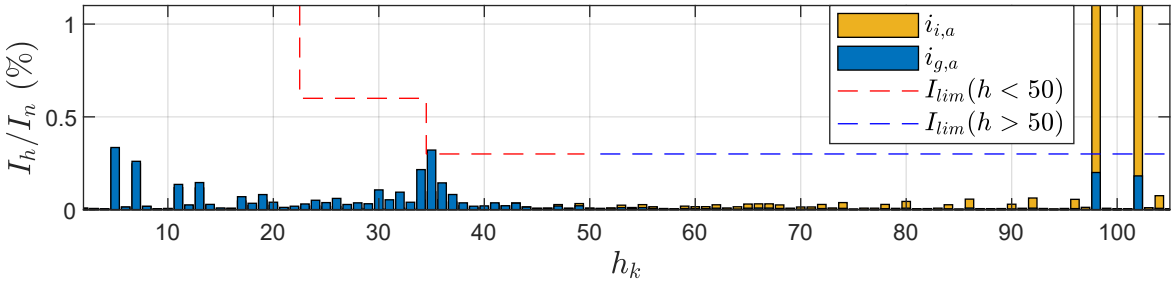
(a)



(b)



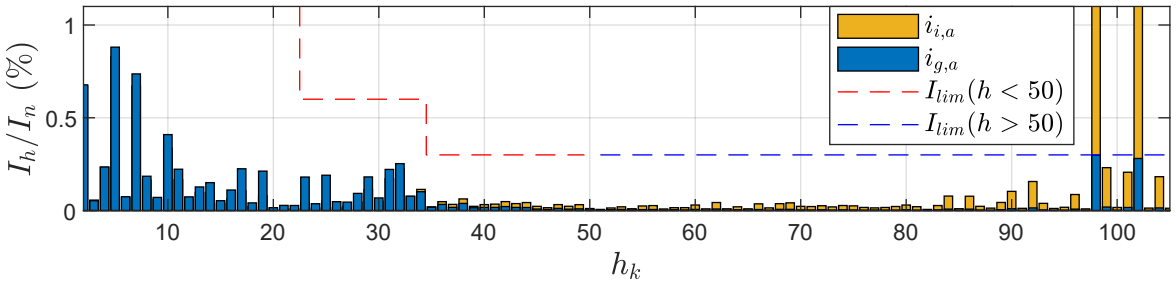
(c)



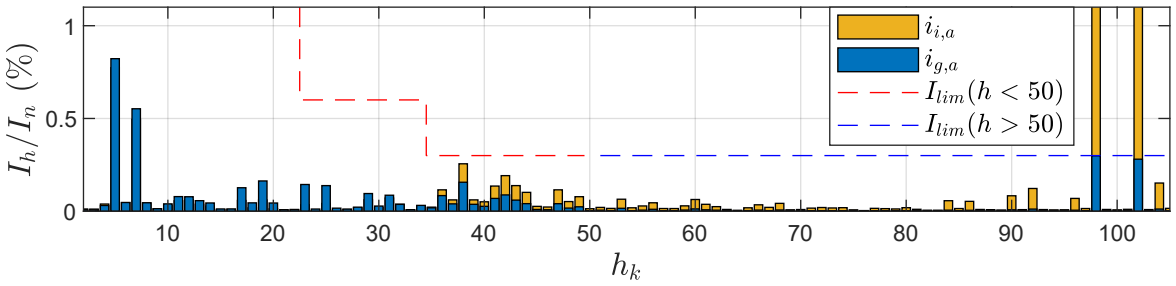
(d)

Figure 4.28: i_i and i_g current harmonics obtained for the given designs when operating as an inverter with unitary power factor and i_g feedback: (a) SUPWM design #1(i_g), (b) SUPWM design #2,$S(i_g)$, (c) DUPWM design #2,$D(i_g)$, and (d) DUPWM design #3(i_g).

that the DUPWM shifts the low order harmonics to higher frequencies, being subjected to a higher attenuation gain. The most relevant harmonics (5^{th} and 7^{th}) are significantly reduced, which justify



(a)



(b)

Figure 4.29: i_i and i_g current harmonics obtained for designs #2 when operating as an inverter with unitary power factor and i_i feedback: (a) SUPWM design #2, $S(i_i)$, and (b) DUPWM design #2, $D(i_i)$

the lower harmonic content, despite the higher harmonics at $h_k = \{23,\ 25,\ 29\}$.

In the transient test, it was already concluded that the i_i control with the SUPWM results in high oscillations when line impedance is considered. During test 2 the line impedance is disregarded, allowing a stable control of the SUPWM with the inverter side current feedback i_i. Though, through comparison of 4.28 (b) and 4.29 (a), it is noticeable that produced harmonics are slightly higher when the inverter side current is chosen, what reinforces the choice of i_g feedback when SUPWM is chosen.

The DUPWM contrary to the SPWM benefits significantly with the inverter side current control, where the TDD is reduced in ≈ 17 %, comparing with the harmonics produced when grid-side current is used, and all individual harmonics limits are fulfilled.

4.3.1.3 Remarks in the current controller design

In previous subsections the results obtained for different filter and controller design cases are analysed. Reached results are analysed for a limited number of design cases to limit the discussion and number of figures. Some remarks that can partially improve the presented results are also discussed.

When grid-connected operation with a strong grid is considered, the SUPWM scheme is stable for both currents feedback. However, the obtained results reveal that the SUPWM performance is improved when grid-side current is chosen. When damping resistance is disregarded, i_g feedback is compulsory, and the dynamics and TDD of the system are barely affected.

For grid-forming or grid-following in a weak-grid such as the case of microgrids, it is significant to increase controller bandwidth to mitigate grid disturbances, which leads to higher gains. When higher gains are considered (as in the studied cases), the controller control variable is more prone to saturate, and the reference to output may present undesired overshoots. To solve this issue, the reference time constant τ_r should be increased. An alternative option is to increase the DC bus voltage (it affects the produced harmonics by the modulation and for that reason, it is not recommended), or choose a modulation scheme that allows higher usage of the DC bus voltage, *e.g.* the THIPWM or SVPWM.

Based on the previous results, it is possible to conclude that the DUPWM with inverter side current feedback and damping resistance is the method that results in the best overall performance. The CC remains stable during weak and strong grid-connection and it is the method that presents a better TDD$/L_T$ ratio.

4.3.2 Voltage controller

For operation in grid-forming condition it is necessary to include a voltage control loop. In this mode of operation, the converter forms the microgrid voltage and consequently, the controller dynamics is conditioned by the load impedance. So the converter must include a damping scheme. Given the mentioned conditions, only the *LCL* and current controller design #2 is considered. Additionally, during grid-forming operation both voltage amplitude V_{dq}^* and phase angle ωt^* (and frequency) are internally generated. To allow the grid side voltage v_g sensing, it is included in the scheme the respective measurement resistance R_m ($= 100\ k\Omega$).

The dual loop (DL) voltage controller (VC) design was performed considering the procedure described in subsection 4.2.4.1. In grid-forming operation the voltage control requires a fast response to reduce voltage sags during the load changes. The parallel loop (PL) voltage controller is designed following subsection (4.2.4.2). The calculated VC gains are shown in tables 4.7 and 4.8. For comparison purposes, it is also included a design based on the symmetrical optimum (SO) as suggested in [102]. The gains obtained through the SO are equivalent to the ones obtained through the procedure discussed above, multiplied by a factor of 0.5.

To test and compare both controllers, the simulation test-bed of figure 4.30 is considered in order to validate the three simulation tests:

1) The first test is a transient operation, where it is intended to evaluate the converter response to the reference step as well the robustness to load changes (with different load angles). The dual loop is evaluated for different controller gains, and feedback configurations, aiming to find suitable VC parameters and identify the feedback configurations that result in the most stable loops. There are two different local loads (line impedance is disregarded) considered in the test ($Z_{load,1}$ and $Z_{load,2}$). The loads present a power factor of 1 and 0.1 respectively. The converter starts by forming the grid with a voltage reference of V_n, and with no load connected. At t_0 the converter is connected to the load, and at t_1 the voltage reference is changed to 0.85 V_n. The loads are tested separately, allowing the evaluation of the different controller responses in similar conditions;

2) The second test is a mixed load transient test aiming to evaluate the impact of changing load angle, and test the overload dynamic response and controller stability. In this test, a third load is also included ($Z_{load,3}$), and dynamics are evaluated under the connection and disconnection of the different loads. The converter starts by forming the grid with $Z_{load,1}$ and $Z_{load,3}$ connected. At t_0, $Z_{load,2}$ is also connected, creating a situation of overload (at nominal voltage, the total load is greater than the converter power rating). $Z_{load,1}$ is disconnected at t_1, proceeding with the disconnection of $Z_{load,2}$ at t_2. During this test, all local loads are connected/disconnected through static switches;

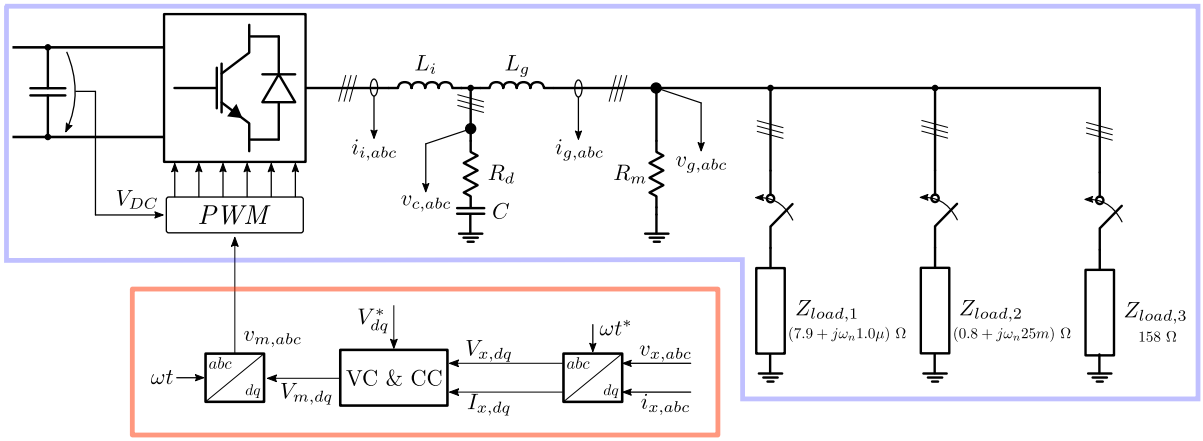
3) The third test is a steady-state test where a single resistive load is considered. The resistive load is calculated so that the converter operates at nominal power and voltage. This test is performed to evaluate the THD of the forming voltage.

Table 4.7: Dual loop VC parameters.

Design	$\omega_{c,v}$	$k_{p,v}$	$k_{i,v}$	$\tau_{r,v}$
DL$^{\#1}$ [102]	1044 rad/s	0.0157	8.255	1.896 ms
DL$^{\#2}$	1044 rad/s	0.0313	16.34	1.896 ms
DL$^{\#3}$	2087 rad/s	0.0626	65.36	1.896 ms

Table 4.8: Parallel loop VC parameters.

Design	$k_{i,v}$	ω_{fl}	$\tau_{r,v}$
PL	208.7	100 rad/s	1.896 ms



(a)

Figure 4.30: Voltage controller design validation circuit, where subscript 'x' can be either 'g' for grid, 'i' for inverter, or 'c' for capacitor.

4.3.2.1 Voltage controller single load test

To validate the choice of VC gains for the dual-loop, the single load test is divided in two different sub-tests. In the first sub-test both loads ($Z_{load,1}$ and $Z_{load,2}$) are applied for each VC design, using the capacitor voltage and inverter side current feedback's, as these are common choices in the bibliography. The VC gains that lead to the most suitable result are used to further study the VC stability when using different feedback configurations, *i.e.* through the combinations between v_g, or v_c, as voltage feedback, and i_g, or i_i, as the sensed current. The stability is checked considering only the inductive load $Z_{load,2}$ since it represents the worst case in terms of VC dynamics.

Figure 4.31 presents the results for a step load change. The converter reference is similar for all tests and designs, hence it is common for all curves of each plot. The simulation starts with the direct voltage reference V_d^* step to the microgrid nominal value V_n, while V_q^* remains unchanged during the simulation and equal to zero. During the interval $0 < t < t_0$ the converter has no load connected. At time instant t_0, the converter is connected with the respective load, *i.e.* with the resistive load $Z_{load,1}$ in figures 4.31(a) and (b), and with the inductive load $Z_{load,2}$ in figures 4.31(c) and (d). The voltage reference reference V_d^* is stepped to $0.85V_n$ at time instant t_1.

Through observation of the simulation results of figure 4.31, it can be noticed that the inductive load, in figures 4.31 (c) and (d), result in considerable higher controller oscillations than the resistive load, of figures 4.31 (a) and (b). Additionally, the proposed parallel loop controller presents a much

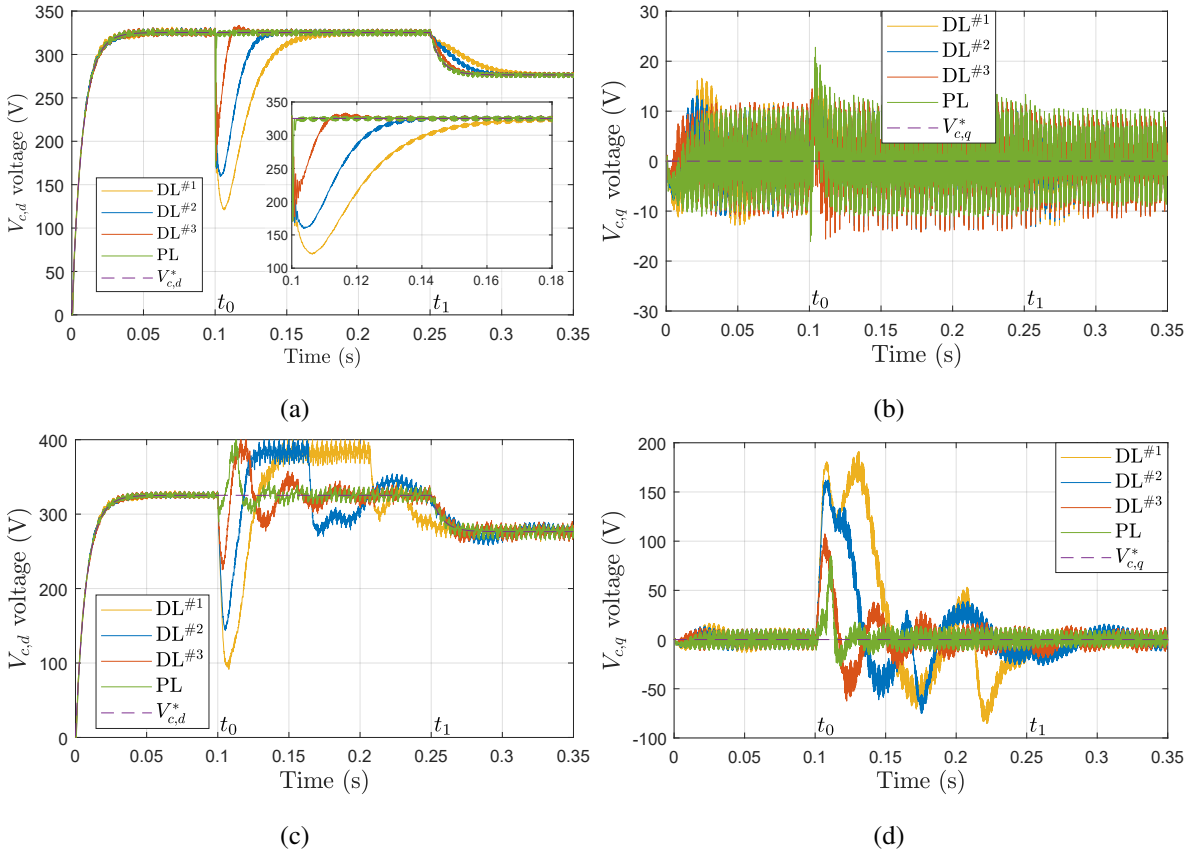


Figure 4.31: SRF voltage transient response of different VC designs, with v_c and i_i feedback's (DUPWM). (a) Capacitor voltage $V_{c,d}$ and (b) $V_{c,q}$ during resistive load $Z_{load,1}$ test. (c) Capacitor voltage $V_{c,d}$ and (d) $V_{c,q}$ during inductive load $Z_{load,2}$ test.

faster and smoother response to load change, than the conventional dual loop.

An important aspect to highlight is the voltage and current oscillations observed for all designs during the inductive load change. The oscillatory behaviour can be expected, since the inductive load presents a very high time constant (≈ 31 *ms*), which results in transient unbalanced phase currents and voltages, during the load connection. The unbalanced phases are responsible for the introduction of oscillations in the SRF measurements, as already mentioned in chapter 3. The unbalance introduced by the load is represented by three-phase voltages and currents in figure 4.32.

Despite of the oscillatory system response, the DL$^{\#1}$ and PL control loops present a response time to the perturbation smaller than 100 *ms*, based on images 4.31 (c) and (d). Furthermore, it is noticeable the saturation over the $V_{c,d}$ component, after recovering from the inductive load connection at t_0. Such saturation is longer, as slower is the VC response, and contributes to slow the VC. The saturation of

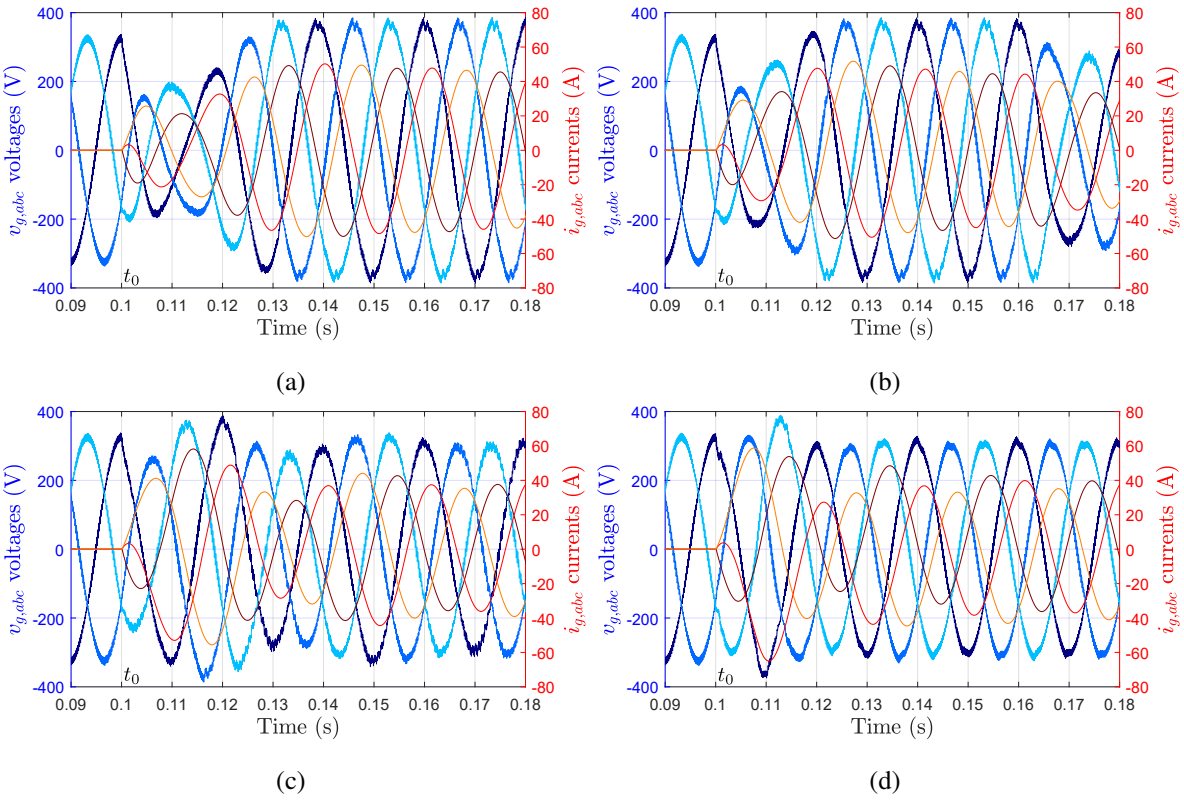


Figure 4.32: Grid side three phase voltages and currents, during reference and inductive load step change test. (a) VC design DL$^{\#1}$, (b) VC design DL$^{\#2}$, (c) VC design DL$^{\#3}$, and (d) VC design PL.

the control variable limits the controller gain. Such behaviour supports the need for a faster controller design.

When considering the dual loop designs, it can be noticed that the settling time increases, as the respective controller design natural frequency $\omega_{c,v}$ decreases. The obtained results response time, reveals that the model used for the VC tuning is insufficient as it does not account for the load dynamics. In this thesis, such an aspect is not further studied, but it is identified as a subject that deserves to be explored.

In table 4.9 it is presented the stability results obtained for the dual-loop design DL$^{\#3}$. The results are relative to the same inductive test presented earlier, but considering different feedback variables configurations and update methods.

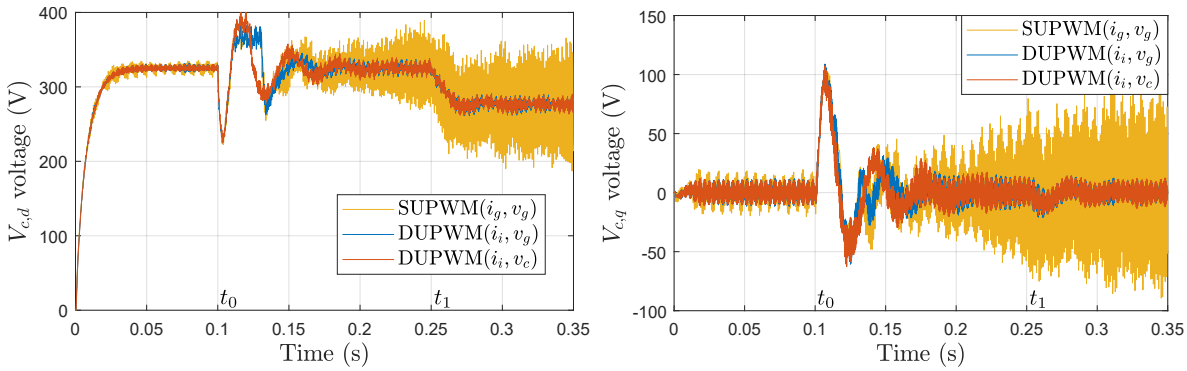
In the parallel loop, the CC design only influences the loop response when an overload occurs, since the voltage and current control loops are independent. For that reason, the impact of the feedback

currents choice can not be evaluated in this test. The parallel loop is evaluated considering different voltage feedback configurations and update methods in subsection 4.3.2.2.

As concluded in the CC tests, the SUPWM is only stable with the grid side current feedback, hence instability is expected with the i_i feedback. Though even with i_g feedback instability is always observed independently of the chosen feedback voltage. Noteworthy that the PWM update method also influences the VC loop. For the DUPWM, instability only occurs when i_g is chosen. In figure 4.33 it is illustrated the DUPWM stable responses, and well the less severe instability response, which is presented by the SUPWM with grid voltage and current feedback's.

Table 4.9: Tested configurations and dual loop stability result.

	Feedback variables			
	i_i, v_c	i_i, v_g	i_g, v_c	i_g, v_g
SUPWM	✗	✗	✗	✗
DUPWM	✓	✓	✗	✗



(a) (b)

Figure 4.33: SRF voltage transient response for different measurements feedback and update methods applied to the dual-loop VC. (a) V_d and (b) V_q voltages.

Based on the analysed tests in the present subsection, it is possible to evaluate the VC performance and stability for different gains, feedback configurations, and update methods. When the dual loop is considered, the results show that the choice of the DUPWM with i_i feedback is mandatory, while voltage feedback choice does not influence significantly the transient response or stability. In the next sections, it is analysed the response to overloads, as well the steady-state voltage harmonic content.

4.3.2.2 Voltage controller overload test

This test is an extension of the previous test, *i.e.* the simulation starts with the converter forming the grid, with two connected loads: an inductive load $Z_{load,2}$ and a high resistance load $Z_{load,3}$. At time instant t_0, a second inductive load is connected (50 % reduction of $Z_{load,2}$) overloading the power converter. At time instant t_1 the voltage reference is changed to $0.85V_n$, while the system remains overloaded. At time instant t_2, one of the inductive loads is disconnected, followed by the second at t_3. The resistive load remains connected during all the tests.

In table 4.10, it is presented the stability results for the different feedback variables configurations and update methods, considering the parallel loop. If SUPWM is mandatory, the parallel loop is the only valid solution for the VC, with the given dynamic response.

Table 4.10: Tested configurations and parallel loop stability result.

	Feedback variables			
	i_i, v_c	i_i, v_g	i_g, v_c	i_g, v_g
SUPWM	✗	✗	✓	✓
DUPWM	✓	✓	✓	✓

Figure 4.34 it is shows the SRF voltages, obtained for the configurations of table 4.10 that result in a stable response.

The obtained results allow the confirmation of the stability with the different configurations, as identified in table 4.10. Additionally, the VC responses seem identical, independently from the chosen configuration or update method, with the differences focused on the steady-state waveform (analysed in the next section).

Between t_0 and t_2, the voltage sag results from the overload condition, as the current is regulated to its maximum value. During this time interval, the voltage reference change at t_1 has a minor impact on the current regulation but introduces a perturbation in the control system since reference voltage is feed-forward in the control loop. Furthermore, the regulated direct and quadrature voltages, during the overload, are a result of the current references regulation. To be noticed that in the parallel loop scheme, the over-current detector clamps the VC, enabling the CC.

In figure 4.35 it is illustrated the SRF voltages for the dual loop, where for comparison purposes,

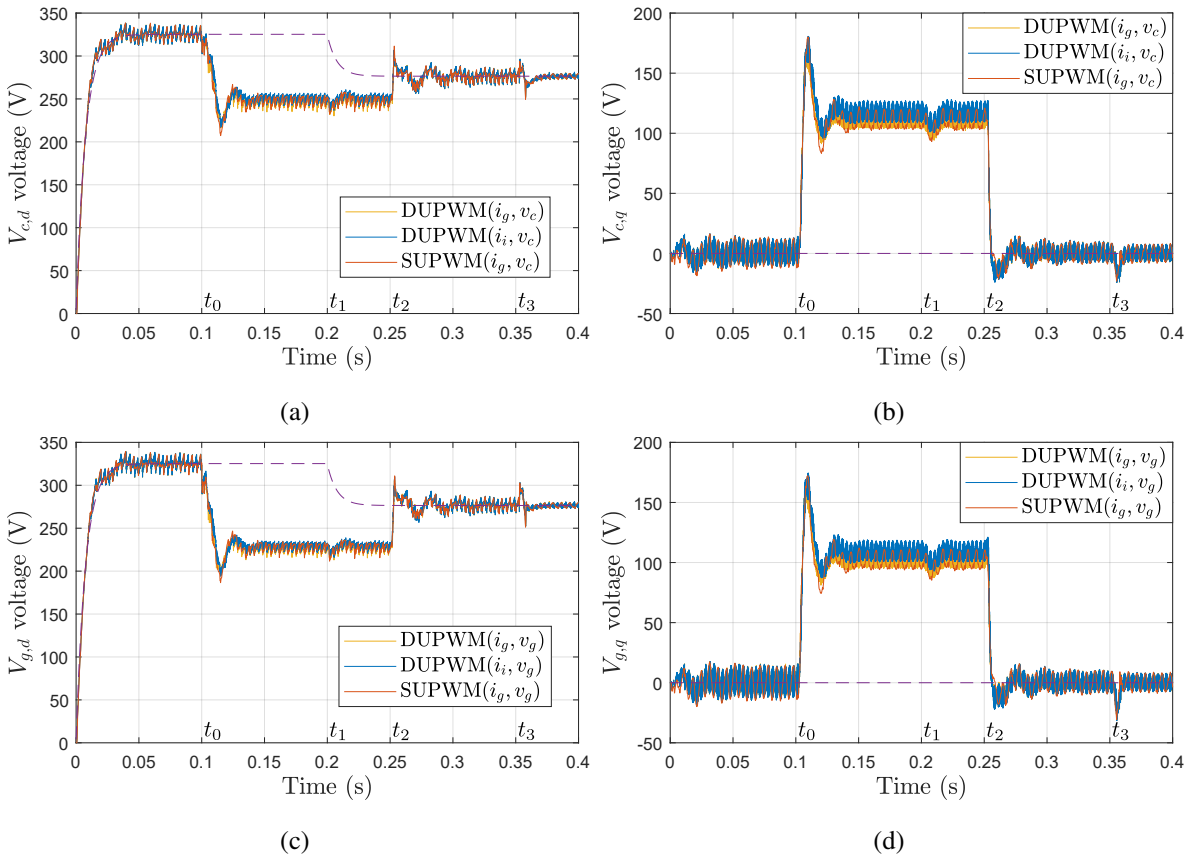


Figure 4.34: SRF voltage transient response of the parallel loop VC, with different feedback configurations and update methods. (a) Capacitor $V_{c,d}$ and (b) $V_{c,q}$ voltages feedback. (c) Grid side $V_{g,d}$ and (d) $V_{g,q}$ voltages feedback.

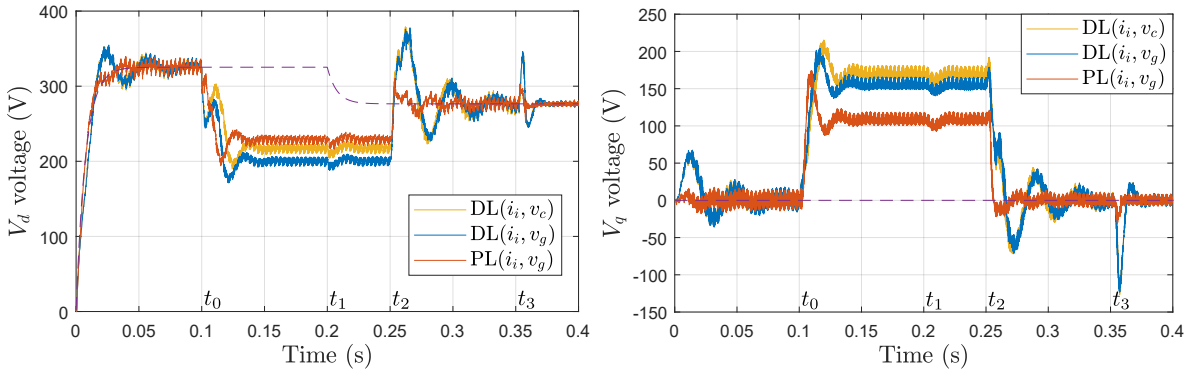
it is also included the parallel loop DUPWM (i_i, v_g).

In the figure, it can be noticed that both dual loop configurations present similar results, while the PL presents a smoother response, confirming the results obtained in subsection 4.3.2.1.

To complement the SRF voltages analysis, it is presented in figure 4.36 the SRF currents resulting from the operation with the dual and parallel loops - both operating with the DUPWM (i_i, v_g).

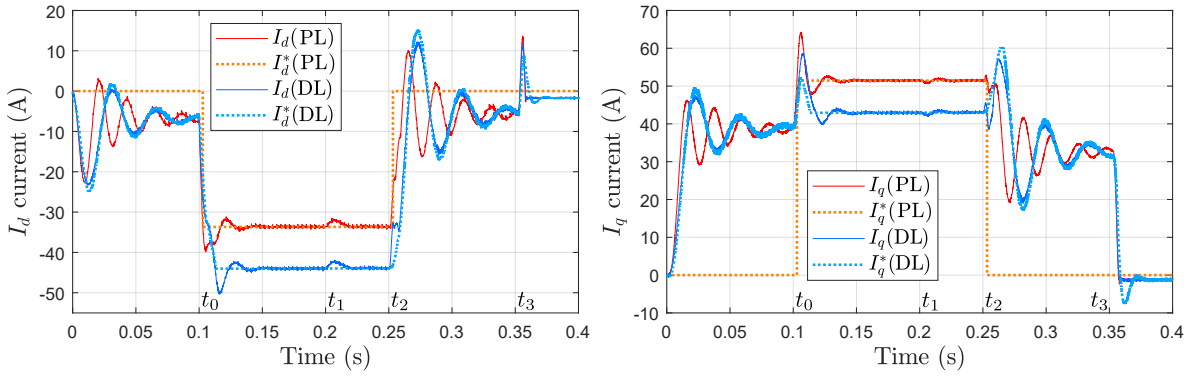
In figure 4.36, the parallel loop reference currents (red dotted lines), present a step-change during the overload instant. Noteworthy that the step change also represents the instant where the OCD flag activates the current loop and clamps the VC integral. Once it returns to zero, the OCD flag also switches signal triggering the following actions: enable the VC integral, disable the CC PI, and enable the CC flush low-pass filter.

When comparing the obtained currents with the voltages of figure 4.35, it becomes clear why



(a) (b)

Figure 4.35: SRF voltage transient response for the dual and parallel loops with the DUPWM. (a) V_d, and (b) V_q voltages.

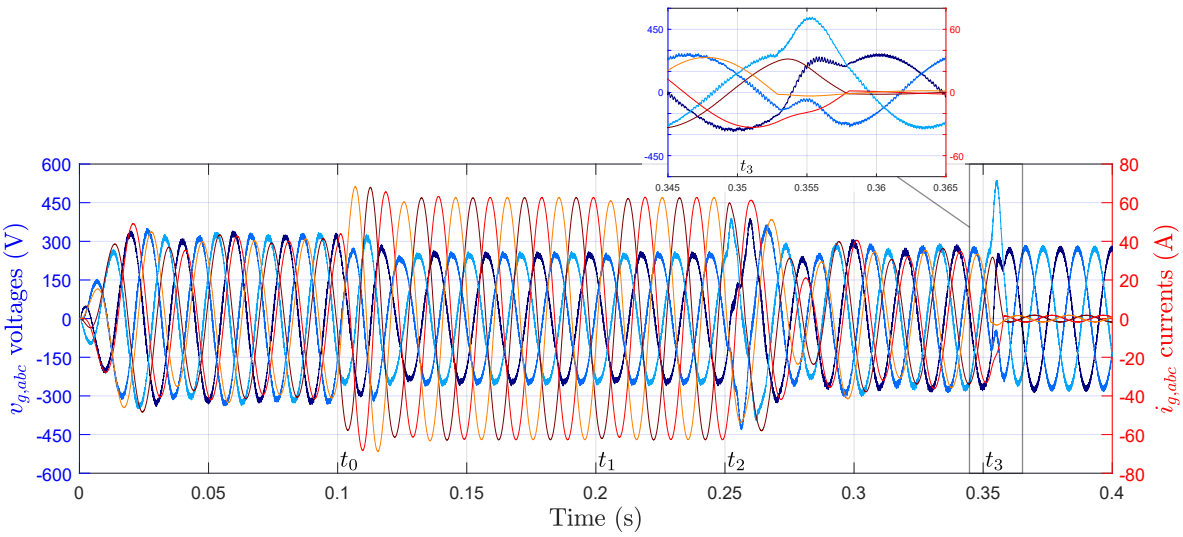


(a) (b)

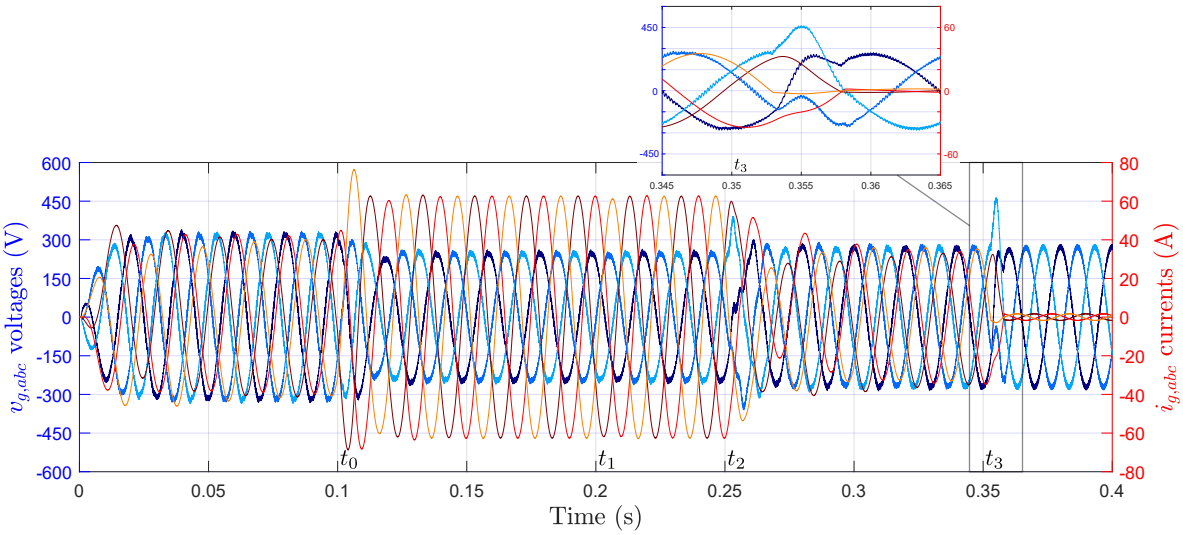
Figure 4.36: SRF current transient response for the dual and parallel loop with DUPWM (i_i, v_g). (a) $I_{i,d}$ and (b) $I_{i,q}$ and respective reference currents.

during the overload condition, the voltages of the different configurations present different values of V_d and V_q. These differences can be explained by the saturation of the reference current at different I_{dq}^* values for each configuration tested. Nonetheless, the voltage and current phasors amplitude, are similar in both configurations. For better comprehension, in figure 4.37 is presented the three-phase voltages and currents for each configuration, where it can be seen between the time interval $[t_0;\ t_2]$, the respective current phasor saturation, and the respective voltage sag.

A curious detail in figure 4.37 is the voltage overshoot after the inductive load disconnection at time instant t_3 (highlighted image). The overshoot presents a value of $\approx 537\ V$ in the dual loop response and $\approx 463\ V$ in the parallel. Though, the same overshoot is considerably attenuated in



(a)

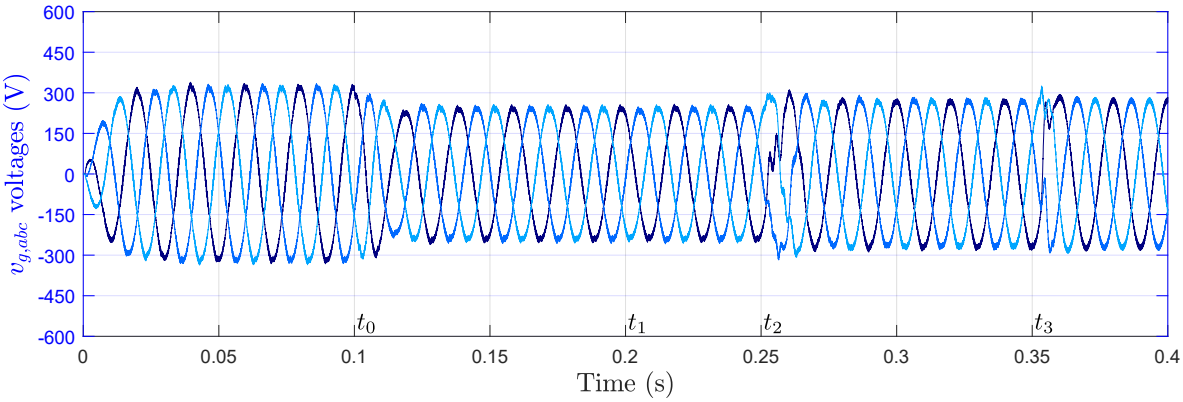


(b)

Figure 4.37: Three phase voltages and currents transient response of the dual and parallel loop, with DUPWM (i_i, v_g). (a) Dual loop and (b) parallel loop.

the measured SRF voltages, represented in figure 4.35. The observed differences can be justified by the fact that when the inductive loads are disconnected, the three-phase load inductance discharges the stored energy back to the grid through the static switches. As a result, it is formed a non-null homopolar component (zero component of the Park transform) that is not included in the presented control loop. In figure 4.37 highlight at $t = t_3$, the averaging of the three-phase voltages is around $\approx 201\ V$, which is close to the zero component obtained applying the complete Park transform to the

measured v_{abc} ($V_0 \approx 199\ V$). In figure 4.38, it is presented the resulting voltages for the parallel loop of figure 4.37, when the measured zero sequences are feed-forward to the modulation scheme.



(a)

Figure 4.38: Three phase voltages of the parallel loop with DUPWM (i_i, v_g), including the zero sequence component in the modulation.

4.3.2.3 Voltage controller steady-state test

For the steady-state test, the converter is forming the grid with $V^*_{dq} = [V_n, 0]\ V$. The load is set at $R_{load} = 5.29\ \Omega$ for full load condition, or $R_{load} = 109\ \Omega$ for 5 % of the rated power. The total harmonic distortion (THD) produced by each of the stable VC configuration studied in the current chapter, is synthesized in table 4.11. The measured THD is relative to the line-to-neutral voltage of reference phase 'a', independently of the applied VC scheme, configuration, or update method. The configurations that consider v_c as a feedback, does not account with the voltage drop at grid-side inductance, resulting in a slightly lower grid voltage ($< 2\%$). To ensure a fair comparison between v_c and v_g feedbacks, the THD is calculated based on the measured output RMS voltage (at v_g).

Table 4.11: THD obtained for all the stable VC schemes, feedback configurations and update methods, according to IEEE-519 standard.

	DUPWM						SUPWM		Limit
	DL (i_i, v_c)	DL (i_i, v_g)	PL (i_i, v_c)	PL (i_i, v_g)	PL (i_g, v_c)	PL (i_g, v_g)	PL (i_g, v_c)	PL (i_g, v_g)	
$R = 5.29$	0.62 %	0.63 %	0.84 %	0.65 %	0.84 %	1.05 %	0.99 %	1.02 %	8 %
$R = 106$	2.66 %	2.67 %	2.70 %	2.69 %	2.70 %	2.69 %	2.75 %	2.74 %	

In figure 4.39 it is illustrated the individual harmonics, and a single period of the respective line-to-neutral voltage waveform, for the best and worst cases tested. In figures 4.39 (a) and (c) it is presented the best result - obtained for the higher load with the VC operating in the dual loop and (i_i, v_c) feedback. The worst tested is relative to the SUPWM applied to the parallel loop with (i_g, v_c) feedback, and it is illustrated in figures 4.39 (b) and (d).

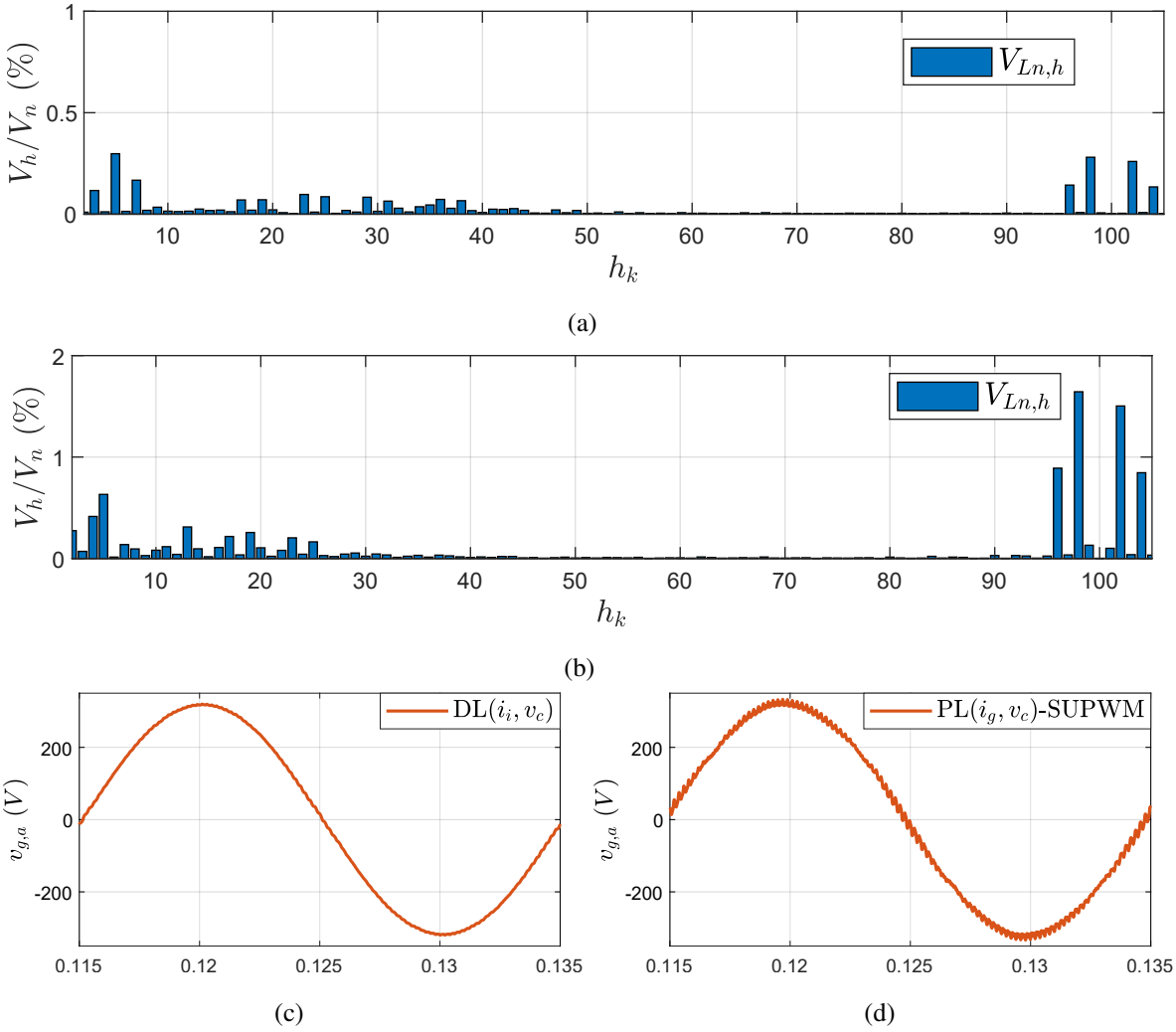


Figure 4.39: Voltage harmonics measured at v_g and respective waveform sample. (a) full load DL(i_i, v_c), (b) low load PL(i_g, v_c) with SUPWM, (c) Voltage waveform of (a), and (d) voltage waveform of (b).

The results presented in table 4.11 show that the DL choice results in the lowest THD, for both full and low load tests, where the (i_i, v_c) feedback presents the THD overall best result. The best PL result is obtained using the DUPWM with (i_i, v_g), followed by (i_i, v_c) and (i_g, v_c) feedbacks. When

comparing the best result for the DL with the best for the PL, the difference is considerably small: 0.03 % THD increase, valid for the full and low load test. Despite the mentioned differences, it is important to highlight that all presented methods comply with the IEEE519 standard.

Based on the current chapter study and respective discussion, the design applied in the following chapters is the design #2, D (table 4.5), with the newly proposed parallel loop VC. The choice of the voltage feedback variables will continue to be a target of discussion in the next chapter, where it is discussed the application of the control loops in converters connected in parallel and operating in an island microgrid.

CHAPTER 5

Island Microgrid Operation

When considering the operation of microgrids, the ESS's are crucial for the stability of the microgrid when operating in island mode. Once the microgrid is disconnected from the main grid, the power balance is no longer ensured by the strong grid. The microgrid control strategy must ensure the power balancing between the loads and RES and simultaneously maximize the ESS energy availability through proper power-sharing and *SoC* balancing. As discussed in the chapter 2, the decentralized control of power converters operating in microgrids has several advantages and challenges, that are addressed in the chapter.

This chapter analyses and discusses a strategy that ensures a distributed power-sharing, and power balancing, of parallel voltage-source converters (VSC) interfacing ESS's, in the scope of a low-voltage microgrid operating on the island mode. The chapter revises the operation principles of the conventional power system, as an introductory operation principle for the proposed technique used for power balancing and sharing.

The droop equations are derived considering different conditions related to the power decoupling dependency on the voltage measurements feedback choice. Droop curves are further extended to adaptively change according to the respective ESS *SoC*. Furthermore, a decentralized approach based on a single grid-forming converter and multiple grid-support converters, where all converters operate with droop curves, resulting in an equity steady-state decentralized power-sharing (active and reactive), and balanced *SoC* of the connected ESS's is analysed and purposed.

The parallel converters considered in the chapter are designed following the procedures presented in chapters 3 and 4, where the control layer is extended to include the proposed adaptive droop.

5.1 Active and reactive power flow

The active and reactive power influence in the grid voltage can be obtained through the classic power flow between two voltage sources V_m and V_g, as shown in figure 5.1. In the figure, the line

impedance is given by $Z = R + jX$, and the power flow S is obtained through equations (5.1). Separating the real and reactive power components of (5.1), results in the power flow (5.2) in terms of R and X, or (5.3) in terms of the impedance angle θ.

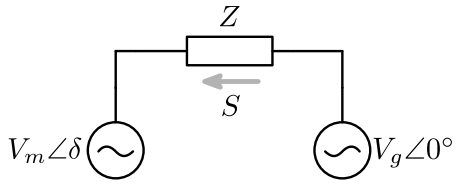


Figure 5.1: Equivalent model of grid-connected voltage source through a line impedance.

$$
\begin{aligned}
&S = V_g\angle 0\left[\frac{V_g\angle 0 - V_m\angle\delta}{R+jX}\right]^* = V_g e^{j0}\left[\frac{V_g e^{j0} - V_m e^{j\delta}}{R+jX}\right]^* = V_g\left[\frac{V_g - V_m e^{-j\delta}}{R-jX}\right] \Leftrightarrow \\
&\Leftrightarrow S = \frac{V_g^2 - V_g V_m e^{-j\delta}}{R-jX} = \frac{V_g^2 - V_g V_m\cos(-\delta) - jV_g V_m\sin(-\delta)}{R-jX}\left(\frac{R+jX}{R+jX}\right) \Leftrightarrow \\
&\Leftrightarrow S = \frac{R\left[V_g^2 - V_g V_m\cos(-\delta) - jV_g V_m\sin(-\delta)\right] + jX\left[V_g^2 - V_g V_m\cos(-\delta) - jV_g V_m\sin(-\delta)\right]}{R^2+X^2}
\end{aligned}
\tag{5.1}
$$

$$
\begin{cases}
P = \dfrac{\left[V_g^2 - V_g V_m\cos(-\delta)\right]R + V_g V_m\sin(-\delta)X}{|Z|^2} \\
Q = \dfrac{-V_g V_m\sin(-\delta)R + \left[V_g^2 - V_g V_m\cos(-\delta)\right]X}{|Z|^2}
\end{cases}
\tag{5.2}
$$

$$
\begin{cases}
P = \dfrac{\left[V_g^2 - V_g V_m\cos(-\delta)\right]\cos(\theta) + V_g V_m\sin(-\delta)\sin(\theta)}{|Z|} \\
Q = \dfrac{-V_g V_m\sin(-\delta)\cos(\theta) + \left[V_g^2 - V_g V_m\cos(-\delta)\right]\sin(\theta)}{|Z|}
\end{cases}
\tag{5.3}
$$

For small power angles, $\cos(-\delta) \approx 1$ and $\sin(-\delta) \approx -\delta$, the power equation (5.2) can be rewritten as (5.4). Based on (5.4), expression (5.5) is obtained by considering a predominant inductive line, or (5.6) considering a resistive line.

$$
\begin{cases}
P = \dfrac{RV_g(V_g - V_m) - XV_g V_m\delta}{|Z|^2} \\
Q = \dfrac{RV_g V_m\delta + XV_g(V_g - V_m)}{|Z|^2}
\end{cases}
\tag{5.4}
$$

$$
\begin{cases}
P = -\dfrac{V_g V_m}{X}\delta \\
Q = \dfrac{V_g}{X}(V_g - V_m)
\end{cases}
, \; Z \approx X
\tag{5.5}
$$

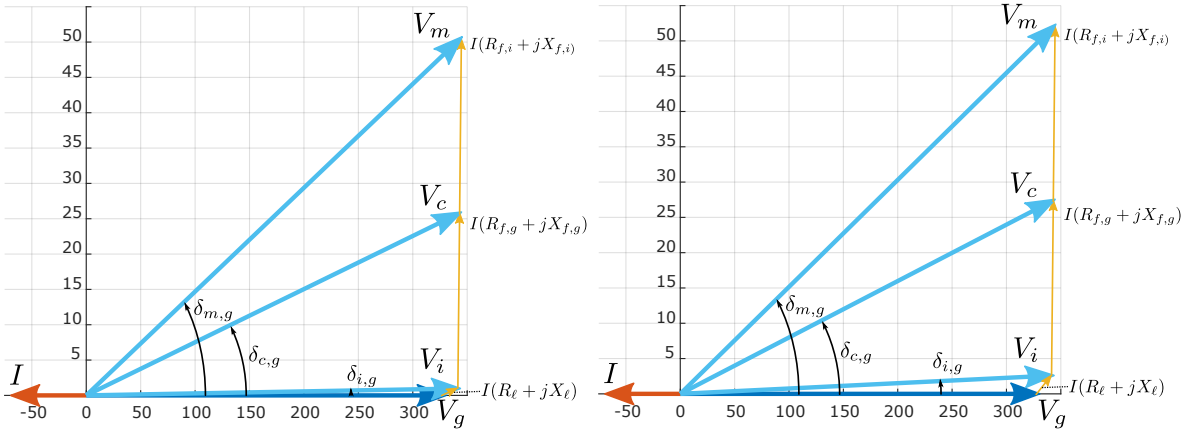
$$\begin{cases} P = \dfrac{V_g}{R}(V_g - V_m) \\ Q = \dfrac{V_g V_m}{R}\delta \end{cases}, \; Z \approx R \tag{5.6}$$

The authors in [105] presents an expression to determine the power control error (5.7), given the power angle approximation and impedance consideration of equation (5.5). Defining a maximum error for the active power $|\varepsilon_{P,X}| = 2\%$ results in a $\delta_{\max} = 0.109\pi$ and consequently the region of operation is determined. The same approach can be applied to calculate the active power control error when resistive line impedance is considered (5.8).

$$\varepsilon_{P,X} = \left| \frac{\delta - \sin\delta}{\sin\delta} \right| 100\% \Rightarrow \delta \in [-0.109\pi; 0.109\pi], \; (\varepsilon_{P,X} < 2\%) \tag{5.7}$$

$$\varepsilon_{P,R} = \left| \frac{1 - \cos\delta}{\cos\delta} \right| 100\% \Rightarrow \delta = [-0.063\pi; 0.063\pi], \; (\varepsilon_{P,R} < 2\%) \tag{5.8}$$

To exemplify the resulting power angle, the phasor diagram of figure 5.2 is presented. The represented phasors illustrate the operation with a unit power factor of the converter design presented in chapter 4. In figure 5.2 (a) the converter is operating with high R/X line impedance ratio, and in figure 5.2 (b) with low, based on the low-voltage line impedances presented in appendix A.



(a) (b)

Figure 5.2: Converter operation with unit power factor phasor diagram. In (a) operation with high R/X line impedance ratio, and in (b) with low R/X line impedance ratio.

The represented line impedances follow the line impedance characterization presented in the appendix A for the cable cross-sections of 95 mm^2, and 35 mm^2, and the respective maximum cable

lengths. The phasor nomenclature is accordingly with the voltage nodes of figure 5.3. Taking 5.2(a) as the worst case scenario and choosing the filter output node V_i as the reference voltage, it is clear that the power angle is within the interval given by equation (5.8). The power angle $\delta_{i,g}$ of figure 5.2 (a) takes a value of $\approx 0.0024\pi$ ($\ll 0.063\pi$). When V_c or V_m is chosen, the respective power angles are $\delta_{c,g} = 0.025\pi$, and $\delta_{m,g} = 0.048\pi$. Hence, it becomes clear that independently of the chosen voltage control node, the power angle approximation of equation (5.4) remains valid. Therefore, power decoupling becomes dependent only in the R/X ratio.

5.1.1 Droop control

Equations (5.5) and (5.6) show that there is a decoupled relationship between $P \propto \delta$, $Q \propto \Delta V$ for inductive lines, or $P \propto \Delta V$, $Q \propto \delta$ for resistive lines. Considering that the power angle change is caused by a frequency variation $\delta \propto \omega_m - \omega_g$, the relationships (5.9) can be considered.

$$\begin{aligned} Z \approx X \Rightarrow \begin{cases} \omega_m > \omega_g \rightarrow P < 0 \\ V_m > V_g \rightarrow Q < 0 \end{cases} \\ Z \approx R \Rightarrow \begin{cases} V_m > V_g \rightarrow P < 0 \\ \omega_m > \omega_g \rightarrow Q > 0 \end{cases} \end{aligned} \tag{5.9}$$

Assuming that $V_g = V_n$ and $\omega_g = \omega_n$ it is possible to obtain the droop curves (5.10) and (5.11). In the droop equations, P_0 and Q_0 are the external active and reactive power reference set-points, P^* and Q^* the set-points resulting from the droop (supplied to the power control loop), and V and ω the measured voltage amplitude and frequency. Noteworthy, that the droop equations (5.10) and (5.11) present the opposite behaviour of (5.9), indicating that droop contributes to mitigate voltage amplitude and frequency variations. Taking (5.10) as an example, it is deduced that when measured frequency $\omega > \omega_n$, the active power increases positively acting as a load to the system, contributing to lower the frequency.

$$\begin{cases} P^* = P_0 + \dfrac{1}{k_{P,X}}(\omega - \omega_n) \\ Q^* = Q_0 + \dfrac{1}{k_{Q,X}}(V - V_n) \end{cases}, Z = X \tag{5.10}$$

$$\begin{cases} P^* = P_0 + \dfrac{1}{k_{P,R}}(V - V_n) \\ Q^* = Q_0 - \dfrac{1}{k_{Q,R}}(\omega - \omega_n) \end{cases}, Z = R \tag{5.11}$$

In (5.12) and (5.13) it is presented the inverse of (5.10) and (5.11), where P and Q are the measured active and reactive power, and V^* and ω^* the reference voltage magnitude and frequency (supplied to the voltage control loop or modulation scheme).

$$\begin{cases} \omega^* = \omega_n + k_{P,X}(P - P_0) \\ V^* = V_n + k_{Q,X}(Q - Q_0) \end{cases}, Z = X \tag{5.12}$$

$$\begin{cases} V^* = V_n + k_{P,R}(P - P_0) \\ \omega^* = \omega_n - k_{Q,R}(Q - Q_0) \end{cases}, Z = R \tag{5.13}$$

From previous analysis, the power decoupling, and consequently the presented droop accuracy, is highly dependent on the impedance nature between both voltage sources. Taking the SRF representation of a VSC connected to the grid (or microgrid), illustrated in figure 5.3, it is possible to apply the different power decoupled droop equations in the same scenario. In the figure, $V_{m,dq}$, $V_{c,dq}$ and $V_{i,dq}$ are the modulation, *LCL* capacitor and filter output voltages. $V_{g,dq}$ is the voltage at PCC. The impedances $Z_{f,i}$, $Z_{f,g}$ and $Z_{f,c}$ are referred to the *LCL* filter impedances. The impedance Z_n is the equivalent impedance seen from the chosen voltage-controlled node ($V_{m,dq}$, $V_{c,dq}$ or $V_{i,dq}$).

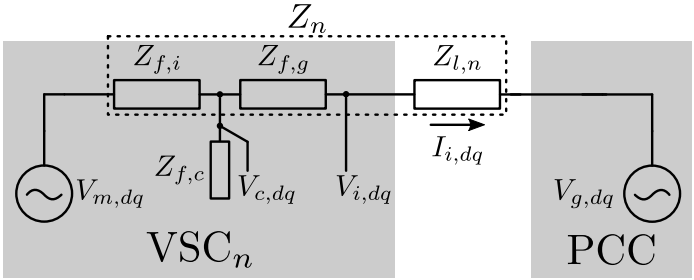


Figure 5.3: SRF equivalent model of the VSC connected to the grid including the *LCL* filter impedance.

Assuming that the filter impedance of the VSC$_n$ and the respective line impedance present the following relationship, $(Z_{f,i} + Z_{f,g} = X) \gg (Z_{l,n} = R)$, three scenarios can be considered (presented in detail on appendix A):

- Voltage controlled at V_m: in this case the resulting impedance $Z_n = Z_{l,n} + Z_{f,g} + Z_{f,i}$ is dominated by X. Hence, power flow respect equations (5.5) and droop curves (5.10);
- Voltage controlled at V_i: the resulting impedance is $Z_n = Z_{l,n}$ and the power flow equations (5.6) and droop curves (5.11) are applied;
- Voltage controlled at V_c: the resulting impedance is $Z_n = Z_{l,n} + Z_{f,g}$ and power decoupling is only achieved if $X_{f,g} \gg X_{l,n}$.

In the last scenario, and considering that line impedance is not dominated by $Z_{f,g}$ or $Z_{l,n}$, according to chapter 2, there are two main approaches to achieve the power decoupling: considering a rotational power frame, or add a virtual impedance to the droop control. The first approach requires knowledge about the X/R ratio, hence if the line impedance is uncertain or changes, the method becomes ineffective. The virtual impedance may be resistive or inductive depending on the desired resulting impedance nature. Since the filter grid-side reactance is usually higher than the line resistance (in LV), it is normally preferable to add a virtual inductance. Though the estimation of the added inductance must take into account the change of the line impedance (depending on the microgrid size and load distance). In the appendix A it is presented the typical values of the LV line impedance for different rated powers, and the required virtual inductance needed to ensure a $R/X \leq 0.1$ for inductive or $R/X \geq 10$ for resistive predominance.

Such an approach gives rise to limited DC bus voltage usage, as part of the available converter voltage is used to supply the virtual impedance. Furthermore, inaccurate prediction of line length also leads to power coupling. Therefore, a strategy that allows power balancing and sharing which does not depend on either line impedance or virtual impedances is desired.

5.1.2 Virtual synchronous machine

The virtual synchronous machine (VSG), with related virtual inertia, has been one of the most discussed topics in the past few years. The control strategy consists of emulating the SM behaviour in the operation of the VSC. One of the greatest advantages of the VSG is the fact that such converters allow being connected in parallel with real SM's, as the fundamental operating principle is equivalent in both cases.

5.1.2.1 VSG model

In steady-state, a synchronous machine (SM) without pole saliency can be represented by its Thevenin equivalent, i.e. a voltage source with a series inductance [106]. The equivalent AC voltage source amplitude is controlled by the DC field generated by the exciter V_e, while frequency follows the rotational equation of motion (5.14). In (5.14) T_m is the prime mover torque, T_e the electromagnetic torque, J the moment of inertia, D the damping, δ the power angle, and ω_e and ω_m the electrical and prime mover frequencies. The choice of the signals is to follow the convention of positive torque for rotational load, and negative torque for generation.

$$\begin{cases} J\dfrac{\partial^2\delta}{\partial t^2} = T_e - T_m - D\dfrac{\partial\delta}{\partial t} \\ \dfrac{\partial\delta}{\partial t} = \omega_e - \omega_m \end{cases} \tag{5.14}$$

A typical simplification of the equation of motion (5.14) is to consider that electrical angular speed ω_e is subjected to small excursions [107], resulting in $\omega_e \approx \omega_n$, where ω_n is the grid nominal frequency. Substituting ω_e and multiplying all terms by ω_n results in (5.15). In (5.16) it is shown the Laplace equation that completes the frequency control of the VSG, where the mechanical power is the external reference P_0, and P_e is the converter measured electric power P.

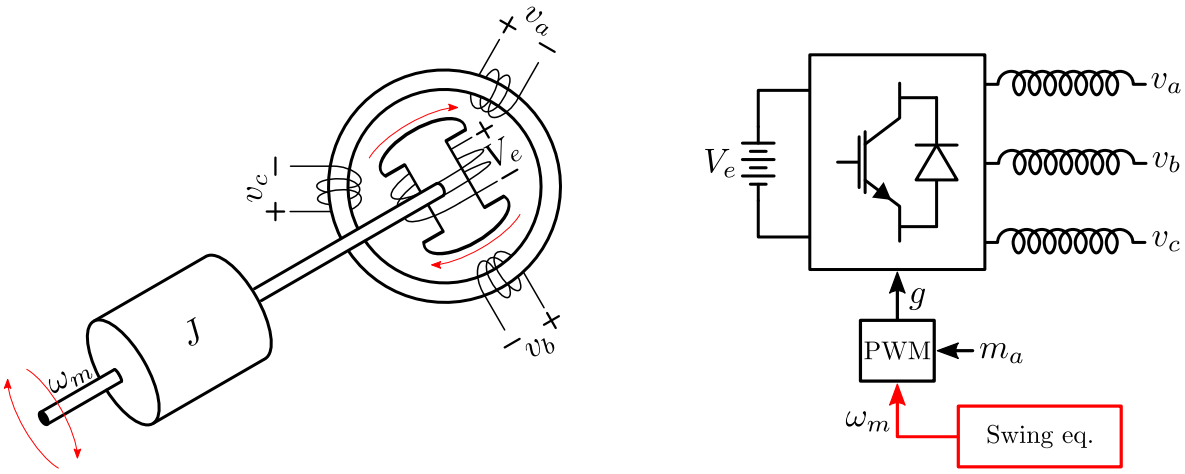
$$\begin{aligned} &\underbrace{J\omega_n}_{k_J}\frac{\partial(\omega_n-\omega_m)}{\partial t} = \omega_n T_e - \omega_n T_m - \underbrace{D\omega_n}_{k_D}(\omega_n-\omega_m) \Leftrightarrow \\ \Leftrightarrow &k_J\left(\frac{\partial\omega_n}{\partial t} - \frac{\partial\omega_m}{\partial t}\right) = P_e - P_m - k_D(\omega_n-\omega_m) \end{aligned} \tag{5.15}$$

$$sk_J\omega_m = P - P_0 - k_D(\omega_n-\omega_m) \tag{5.16}$$

To complete the VSG model, the $Q-V$ droop of equation (5.12) is added to obtain the reference voltage magnitude, where Q is normally filtered with a first-order LPF.

In the SM Thevenin equivalent, the series inductance represents the stator windings, where resistance is usually neglected. When the synchronous machine is connected to another voltage source (e.g. grid or microgrid voltage) the power angle between the two sources results in an active power flow between both (as earlier discussed). The source of energy that flows between the generator and the grid is provided by the kinetic energy stored in the rotating mass and the prime mover, given by the swing equation (5.16).

The power converter is usually a VSC, therefore is representable by its Thevenin equivalent circuit, which is similar to the SM (a voltage source with a series inductance). The inductance in the VSC is added to filter the current harmonics produced by the semi-conductor switching and hence it also reduces the harmonics distortion introduced in the grid. The VSC voltage amplitude and frequency are both controlled by the converter modulation scheme (conventionally a sinusoidal PWM). Therefore, there are no constraints in the frequency rate of change, imposed by the VSC hardware (it is an inertialess system). To introduce inertia and mimic the SM behaviour, the VSC control loops must integrate the swing equation and reactive power $Q-V$ droop, as described earlier. The control loop adds inertia (virtually) but allows the manipulation of the virtual system in such ways that can not be accomplished in an SM, e.g. dynamically change the inertia of the system as suggested in [108]. There are no rotating parts in the VSC, hence active power is supplied by the energy stored in the DC bus capacitance and interconnected sources. To illustrate the comparison between the SM and the VSC operating as a VSG, figure 5.4 is presented. For the analogy, it is considered that the SM presents a single pole pair, the internal voltage induced in the stator winding is $0.5V_e$, windings inductance present the same value as the VSC filter inductances, and a VSC modulation index of $m_a = 1$.



(a) (b)

Figure 5.4: Analogy between the (a) SM, and (b) the VSC operating as a VSG.

The importance of inertia has a physical meaning in power systems since the rotation speed of SM's is synchronized with the grid frequency and frequency level is an indicator of the system active power balance. Though, the inertia concept can be also virtually applied to converters operating with resistive lines and the $P-V$ droop. In such case, the converter inertia can be measured by the

equivalent DC energy available in the converter DC bus capacitance. The virtual inertia is no longer related to the converter frequency but instead with the generated voltage. The described analogy is mathematically reinforced in the following subsection.

5.1.2.2 Equivalence between droop and the VSG

The VSG swing equation shows that there is a $P-\omega$ relationship just as in the case of the conventional droop. In fact, according to [47] the swing equation (5.16) is equivalent to the $P-\omega$ droop when active power feedback is filtered by a first-order LPF. Taking the droop $P-\omega$ equation (5.10), and adding a LPF to the measured power P, results in the transfer function (5.17), where τ_P is the LPF time constant. From the Laplace of (5.17) and rearranging the terms allows to obtain the VSG swing equation transfer function (5.18).

$$\frac{\omega-\omega_n}{P-P_0}=\frac{1}{s\frac{\tau_P}{k_{P,X}}+\frac{1}{k_{P,X}}} \tag{5.17}$$

$$\frac{\omega-\omega_n}{P-P_0}=\frac{1}{sk_J+k_D} \tag{5.18}$$

Comparing both transfer functions it results that the VSG swing equation and the droop with an LPF are equivalent as far as the relationships (5.19) are considered.

$$\begin{cases} k_J=\dfrac{\tau_P}{k_{P,X}} \\ k_D=\dfrac{1}{k_{P,X}} \end{cases} \tag{5.19}$$

From the analysis at the end of the last subsection and comparison of the $P-V$ droop (5.13) with the $P-\omega$ (5.10) it results a similar relationship between the VSG and the $P-V$ droop, where $k_{P,R}$ is considered instead of $k_{P,X}$. The transfer function of active power becomes function of ΔV (5.20).

$$\frac{V-V_n}{P-P_0}=\frac{1}{s\frac{\tau_P}{k_{P,R}}+\frac{1}{k_{P,R}}}\equiv\frac{\omega-\omega_n}{P-P_0}=\frac{1}{sk_J+k_D} \tag{5.20}$$

5.1.3 Steady state analysis of parallel sources

In the scope of modern low voltage island microgrids, the intrinsic behaviour of traditional power systems is not necessarily observed. The power converters interface all sorts of sources (including rotational ones) and therefore synchronous machines operate as not directly connected to the grid. So the active and reactive power sharing should be addressed considering the line impedance, converter dynamics, and the respective control loops.

Figure 5.5 schematic facilitates understanding the impact of load changes in the voltage and currents flowing in the local grid. The figure illustrates a converter operating in grid-feeding (VSC_n) and a voltage source forming the grid at PCC (can be either the main grid or a converter). Performed analysis is based on steady-state or slow transients since current derivatives are considered null.

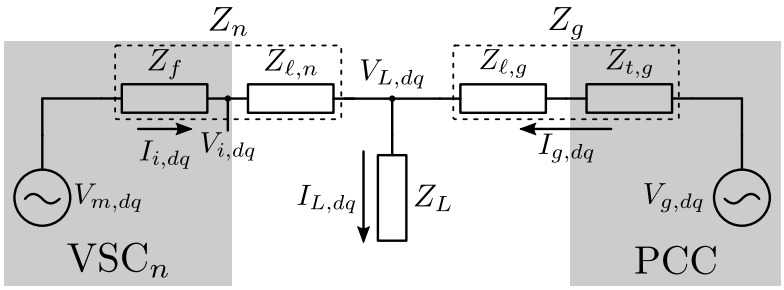


Figure 5.5: Equivalent model of parallel converters.

Assuming that $I_{i,dq}$ is controlled (and constant in this analysis), it can be concluded that load changes are compensated by the PCC source (5.21). The load voltage can be determined by the *PCC* voltage and current (5.22), and therefore load change has direct impact in the load voltage: $|\Delta V_{L,dq}| \propto |\Delta I_{g,dq}| = |\Delta I_{L,dq}|$ (5.23).

$$\begin{cases} I_{L,dq} = I_{i,dq} + I_{g,dq} \\ |\Delta I_{L,dq}| = |\Delta I_{g,dq}|, \quad \Delta I_{i,dq} = 0 \end{cases} \tag{5.21}$$

$$\begin{bmatrix} V_{L,d} \\ V_{L,q} \end{bmatrix} = \begin{bmatrix} V_{g,d} \\ V_{g,q} \end{bmatrix} - \begin{bmatrix} R_g & -X_g \\ X_g & R_g \end{bmatrix} \begin{bmatrix} I_{g,d} \\ I_{g,q} \end{bmatrix} \tag{5.22}$$

$$\begin{bmatrix} V_{L,d} + \Delta V_{L,d} \\ V_{L,q} + \Delta V_{L,q} \end{bmatrix} = \begin{bmatrix} V_{g,d} \\ V_{g,q} \end{bmatrix} - \begin{bmatrix} R_g & -X_g \\ X_g & R_g \end{bmatrix} \begin{bmatrix} I_{g,d} + \Delta I_{L,d} \\ I_{g,q} + \Delta I_{L,q} \end{bmatrix} \Leftrightarrow \begin{bmatrix} \Delta V_{L,d} \\ \Delta V_{L,q} \end{bmatrix} = \begin{bmatrix} R_g & -X_g \\ X_g & R_g \end{bmatrix} \begin{bmatrix} \Delta I_{L,d} \\ \Delta I_{L,q} \end{bmatrix} \tag{5.23}$$

The current flowing in the VSC$_n$ branch is dependent in the modulation voltage of the converter $V_{m,dq}$ and the sensed output voltage $V_{i,dq}$, which is also dependent on the voltage drop across the line (constant due to constant $I_{i,dq}$) and the load voltage $V_{L,dq}$ (5.24). Hence, when $V_{L,dq}$ changes with $\Delta I_{g,dq}$, $V_{m,dq}$ and $V_{i,dq}$ also changes in the same proportion. Therefore the converter can sense load voltage variations (5.25).

$$\begin{bmatrix} I_{i,d} \\ I_{i,q} \end{bmatrix} = \begin{bmatrix} \frac{R_{f,i}}{Z_{f,i}^2} & \frac{X_{f,i}}{Z_{f,i}^2} \\ -\frac{X_{f,i}}{Z_{f,i}^2} & \frac{R_{f,i}}{Z_{f,i}^2} \end{bmatrix} \begin{bmatrix} V_{m,d} - V_{i,d} \\ V_{m,q} - V_{i,q} \end{bmatrix} \tag{5.24}$$

$$\begin{bmatrix} \Delta I_{i,d} \\ \Delta I_{i,q} \end{bmatrix} = \begin{bmatrix} \frac{R_{f,i}}{Z_{f,i}^2} & \frac{X_{f,i}}{Z_{f,i}^2} \\ -\frac{X_{f,i}}{Z_{f,i}^2} & \frac{R_{f,i}}{Z_{f,i}^2} \end{bmatrix} \begin{bmatrix} \Delta V_{m,d} - \Delta V_{i,d} \\ \Delta V_{m,q} - \Delta V_{i,q} \end{bmatrix} \Leftrightarrow$$
$$\Leftrightarrow \begin{bmatrix} \Delta I_{i,d} \\ \Delta I_{i,q} \end{bmatrix} = 0 \Leftrightarrow \begin{bmatrix} \Delta V_{m,d} \\ \Delta V_{m,q} \end{bmatrix} = \begin{bmatrix} \Delta V_{i,d} \\ \Delta V_{i,q} \end{bmatrix} \left(= \begin{bmatrix} \Delta V_{L,d} \\ \Delta V_{L,q} \end{bmatrix} \right) \tag{5.25}$$

During load transients significantly fast considering the converter current control bandwidth, the converter modulation voltage $V_{m,dq}$ becomes constant instead of the converter current $I_{i,dq}$. In this case, the load is still sensed by the converter (5.26) and it is partially compensated by the power converter.

$$\begin{bmatrix} \Delta I_{i,d} \\ \Delta I_{i,q} \end{bmatrix} = \begin{bmatrix} \frac{R_i}{Z_i^2} & \frac{X_i}{Z_i^2} \\ -\frac{X_i}{Z_i^2} & \frac{R_i}{Z_i^2} \end{bmatrix} \begin{bmatrix} -\Delta V_{L,d} \\ -\Delta V_{L,q} \end{bmatrix} \tag{5.26}$$

Taking into account previous analysis and considering N converters connected at $V_{L,dq}$ node (neglecting line impedances) there are three important characteristics to highlight:

1. To share the load power is necessary to know the PCC current;

2. Converter PLL does not allow to track power angle change since each converter is synchronized with $V_{i,dq}$ ($V_{i,q} = 0$) through a PLL and consequently changes in quadrature load voltage $V_{L,q}$ (considering PCC as the reference node) are hardly discriminatingly sensed - a change of $V_{L,q}$ in steady state is sensed as a change in $V_{i,d}$ by the power converter;

3. Since load voltage is equally sensed by each converter, it would be necessary information about how many converters are connected for proper load sharing.

To overcome the described issues, droop control is included in each converter control loop considering resistive line impedance, *i.e.* $P-V$ and $Q-\omega$. Hence, voltage source at PCC regulates the

output voltage amplitude and frequency depending on the active and reactive power measurements respectively. Such voltage regulation allows to qualitatively inform connected converters, operating as current sources (current-controlled), of the voltage source converter instantaneous power. The fact of using frequency as signalling of the instantaneous reactive power allows to overcome the issue in the power angle detection since the frequency is measurable by the PLL and common to the full system. In next section 5.2 it is described the droop control loops for each converter.

5.2 Grid-forming and grid-support operation modes

Addressing the problems discussed in previous sections it is presented a power sharing control strategy based on both droop and AC bus signalling. The strategy consists of a converter operating as grid-forming responsible for grid generation and n slave converters that participate in the grid stability (operating in grid-support). The method resembles the master-slave approach, where a single unit generates references to the slave units. Though in this case there are no communications evolved and instead droop curves are designed to transmit the information about the microgrid power needs, *i.e.* through AC bus signalling.

The grid-forming converter generates the microgrid voltage based on internal references (V_n and ω_n) and supplies the fast load's transient power. The grid-forming converter based on its instantaneous output active and reactive power regulates the generated voltage and frequency following a droop curve (*e.g.* $P-V,\ Q-\omega$). The change in the microgrid voltage amplitude and frequency allows signalling the grid-support converters. The converters operating in grid-support regulate its active and reactive power based on the measured grid voltage and frequency (*e.g.* $V-P,\ \omega-Q$ droops). The converters have regulated current/voltage at its output therefore the adopted droop characteristic is based on the low voltage line impedance which is mainly resistive, accordingly with the cable impedance data presented in the appendix A.

5.2.1 Grid-forming converter

The grid-forming converter is presented in figure 5.6, where filter output (grid side) voltage $v_{i,abc}$ is chosen as the feedback voltage.

The current measurement $i_{i,abc}$ is carried at the converter-side inductance. The measured voltages and currents are transformed into the SRF considering the internally generated angle ωt_m. In the

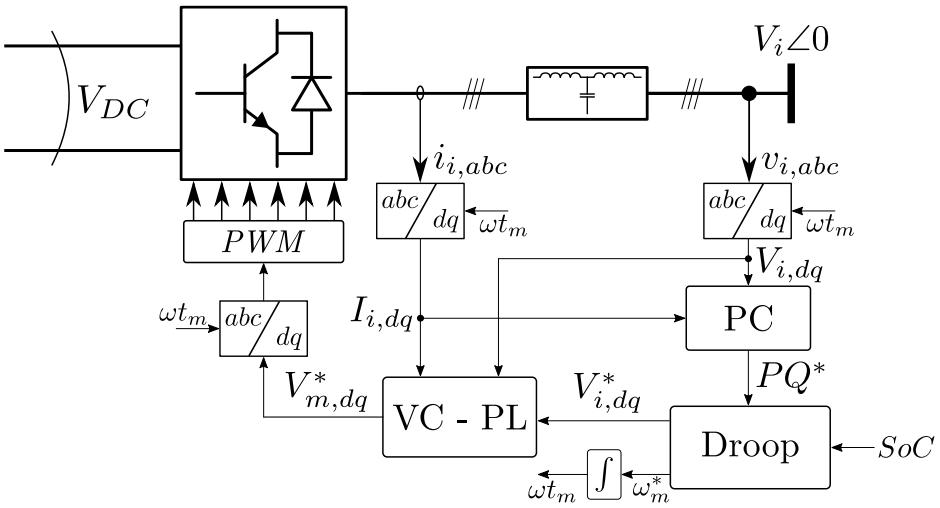


Figure 5.6: Simplified scheme of the Grid-forming converter.

Droop Control block, power is calculated (5.28), processed accordingly with the droop characteristic, and filtered with a first-order LPF with $\omega_{0,V}$ and $\omega_{0,\omega}$ cut-off frequencies. The LPF's are added to increase system inertia and therefore can be adjusted according to. Though, for the sake of system stability and droop interaction between the parallel converters, the LPF should always be included and respect inequations (5.27), where $\omega_{r,v}$ is the VC voltage reference, and ω_{PLL} the PLL cut-off frequencies.

The droop control block outputs are the reference output voltage $V^*_{i,dq}$ and frequency ω^*, where $V^*_{i,q} = 0$. Grid-forming control generates the modulation voltage that results in the desired output voltage $V^*_{i,dq}$ at V_i. The voltage control is achieved through the VC-PL (voltage control with parallel loop) presented earlier in chapter 4.

$$\begin{aligned} \omega_{0,V} &< \omega_{r,v} \\ \omega_{0,\omega} &< \omega_{PLL} \end{aligned} \tag{5.27}$$

$$\begin{aligned} P &= \frac{3}{2} V_{g,d} I_{g,d} \\ Q &= -\frac{3}{2} V_{g,d} I_{g,q} \end{aligned} \tag{5.28}$$

The reference voltage $V^*_{i,dq}$ of figure 5.6 is generated through internal references (grid nominal values) and changed with the droop. Since the converter available power is supplied by an electric storage system, and the line is considered mainly resistive, in this work it is presented an active power droop $P/SoC - V$ that dynamically adjusts the droop curve with the storage system SoC. The

method consists in shifting the conventional droop curve accordingly with the measured *SoC*. The reactive power droop maintains the $Q-\omega$ relationship. The described droop control is synthesized as illustrated in figure 5.7. Furthermore, the change in voltage and frequency introduced by the droop curves are within the limits recommended by the EN 50438 (2013), *i.e.* $V \in [0.9V_n;\ 1.1V_n]$ and $\omega \in [0.97\omega_n;\ 1.03\omega_n]$.

The presented droop curves generate the AC bus signalling of the grid-forming converter. For a given *SoC* the output voltage is adjusted proportionally with the measured active power that mimics the voltage drop in the line. Additionally, it can be noticed that for lower ESS *SoC* voltage remains below nominal value while for higher *SoC* remains above. The *SoC* action can be seen as a change in the value of an equivalent virtual resistance. The voltage set-point indicates to other ESS grid-support converters when should supply power (voltage below nominal) or absorb (voltage above nominal).

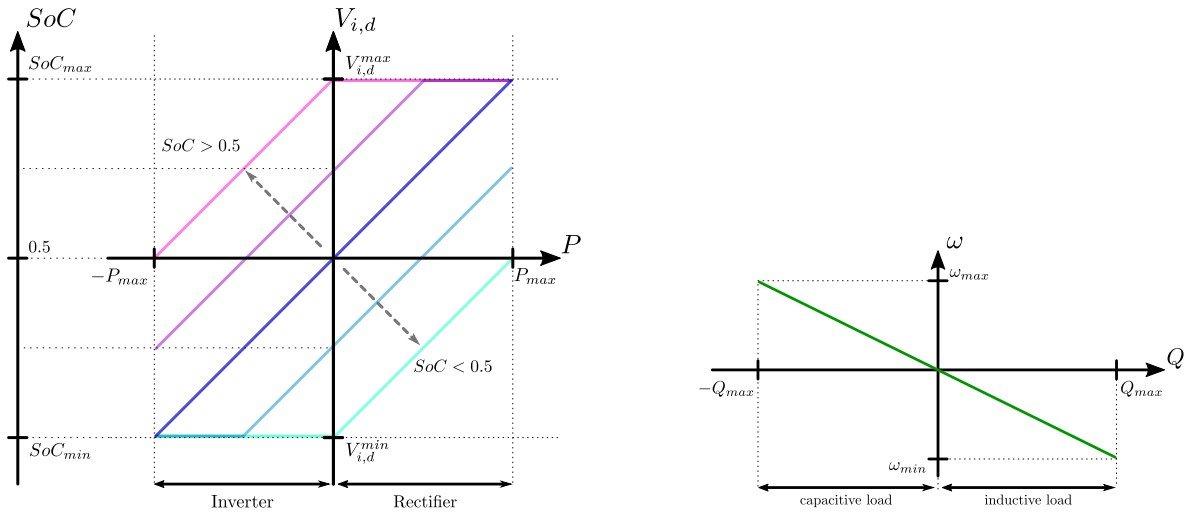


Figure 5.7: Representation of the grid-forming converter droop curves. (a) the $P/SoC-V$ droop, and (b) the $Q-\omega$ droop.

5.2.2 Grid-support converters

The grid-support converters considered in this work are bi-directional power sources that interface an energy storage system. The converter control scheme is illustrated in figure 5.8.

The control architecture consists of an inner current control loop based on the VOC whose current references are obtained directly from the computation of power references (5.29). The current control

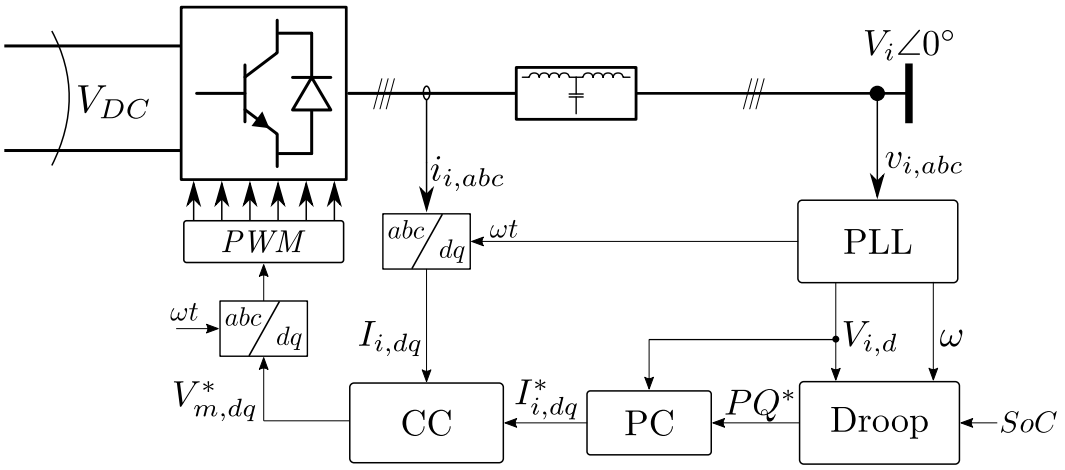


Figure 5.8: Simplified scheme of Grid-support converter.

loop is designed as presented earlier in chapter 4. Similarly with the grid-forming converter, the converter-side currents and filter output voltages were chosen as feedback variables. Since the grid-support converter operates as grid-following, the phase angle and grid frequency are estimated through the PLL. The estimated angle is used to convert the three phase measurements into the SRF. The estimated frequency and SRF voltage $V_{i,d}$ are fed into the Droop block.

$$\begin{aligned} I_d^* &= \frac{2P^*}{3V_{g,d}} \\ I_q^* &= -\frac{2Q^*}{3V_{g,d}} \end{aligned} \tag{5.29}$$

The Droop generates the active and reactive power references PQ^*. The power references are filtered at block output, with a first-order LPF with $\omega_{0,P}$ and $\omega_{0,Q}$ cut-off frequencies. Since grid voltage and frequency are primarily set by the grid-forming converter, the power references from grid-supporting converters droop should be filtered with an higher time constant. Otherwise, oscillations will certainly occur. The droop references time constants follow the relationships (5.30).

$$\begin{aligned} \omega_{0,V} &= \frac{1}{6}\omega_{0,P} \\ \omega_{0,\omega} &= \frac{1}{6}\omega_{0,Q} \end{aligned} \tag{5.30}$$

The droop curves are similar to the grid-forming converter, for a null external active power set-point as shown in figure 5.9(a). The droops are inverted therefore, converter power references are adjusted accordingly with the measured output voltage and frequency. As discussed before, the grid-forming converter lowers the microgrid voltage when its supplied power is increased. Such behaviour

signals the grid-support converters to increase their output power and consequently share the load power demand. The same logic is applied to the frequency and reactive power. Since active power curves are similar, for two units with the same *SoC* and power rating, the power-sharing in steady-state will be equally distributed among them, unless significant differences in the line impedance are observed. In such a case, higher line impedance will result in a higher voltage drop and the respective unit will contribute less. This behaviour is desired since indicates that converters near the loads tend to contribute more. Additionally, when ESS *SoC* drops, the droop curve shifts towards positive active power (ESS charging) while for higher *SoC* the droop curve shifts towards negative active power (ESS discharging).

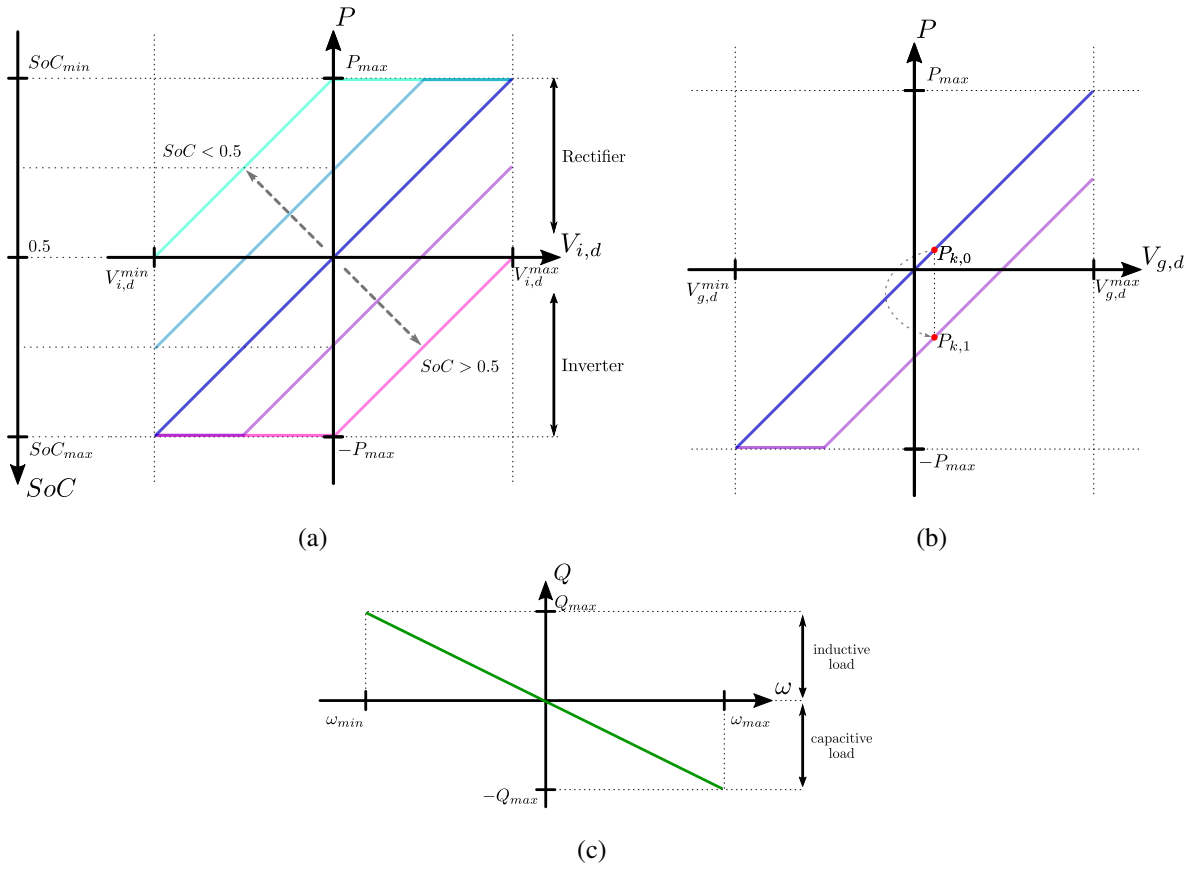


Figure 5.9: Representation of the grid-support converter droop curves. (a) the $V-P/SoC$ droop, (b) example of an external power reference impact on the droop curve, and (c) the $\omega - Q$ droop.

When the unit's power set-point is externally changed in grid-supporting mode, the droop curve is shifted accordingly. The adjustment is equivalent to a change in the *SoC* and therefore this mode will not be emphasized. The described behaviour is illustrated in figure 5.9(b), *i.e.* for a certain measured

voltage, when an external reference P_{ext} changes from $P_{k,0}$ ($P_{ext} = 0$) to $P_{k,1}$ ($P_{ext} = -0.5P_{max}$), the droop curve change accordingly.

5.3 Proposed droop simulation results and discussion

The previously described methods were initially implemented through co-simulation with *Matlab (Simulink)* and *Ansys (Simplorer)*. For the sake of simplicity, the converter switching model was replaced by controllable voltage sources, *i.e.* generated modulation voltages control directly a voltage source, instead of being compared with a carrier and generate the respective PWM's. Noteworthy that all units are three-phase converters operating in the synchronous reference frame with ratings as shown in table 5.1. Furthermore, phase synchronization is achieved through the FFDSOGI-PLL discussed in chapter3, and the *LCL* filter is designed accordingly with chapter 4. The controller gains are also designed as presented in chapter 4 and are listed in table 5.2.

Table 5.1: Converters rating and *LCL* filter parameters.

Converter Ratings				LCL Filter			
S_N	$V_{LL,rms}$	V_{bus}	f_{sw}	L_i	L_g	C	Rd
30 kVA	400 V	700 V	5 kHz	1.224 mH	1.224 mH	15 μF	2.1 Ω

Table 5.2: Controllers parameters.

Current PI		Voltage PI (PL)		PLL		Droop							
$k_{p,c}$	5.057	$k_{p,V}$	0.0	$k_{p,PLL}$	1.370	$\omega_{0,P}/\omega_{0,Q}$	10 Hz/3 Hz	P_{max}	30 kW	$V_{g,d}^{max}$	358 $V_{pk}(1.1V_{Ln,N})$	ω_{max}	324 $rad/s(1.03\omega_N)$
$k_{i,c}$	2667	$k_{i,V}$	200.0	$k_{i,PLL}$	163.0	$\omega_{0,V}/\omega_{0,\omega}$	1.7 Hz/0.5 Hz	Q_{max}	30 kVA	$V_{g,d}^{min}$	293 $V_{pk}(0.9V_{Ln,N})$	ω_{min}	305 $rad/s(0.97\omega_N)$

The considered testbed consists of three independent ESS inverters with similar characteristics as described before. The converter $'0'$ is the master converter and therefore operates in grid-forming. The converters $'1'$ and $'2'$ operate as slaves in grid-support mode. Figure 5.10 shows the testbed equivalent circuit, where Z_x is the *RL* load connected to the $'x'$ node and $Z_{\ell(i,j)}$ is the *RL* impedance of the line between the node $'i'$ and $'j'$, in accordance with the line impedance characteristics presented in the appendix A, for a distance of $\ell_{(i,j)}$.

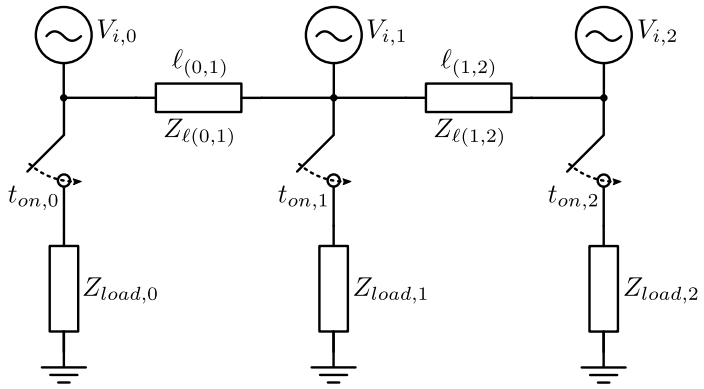


Figure 5.10: Island mode test bed.

5.3.1 Power-sharing with normal load: different line lengths

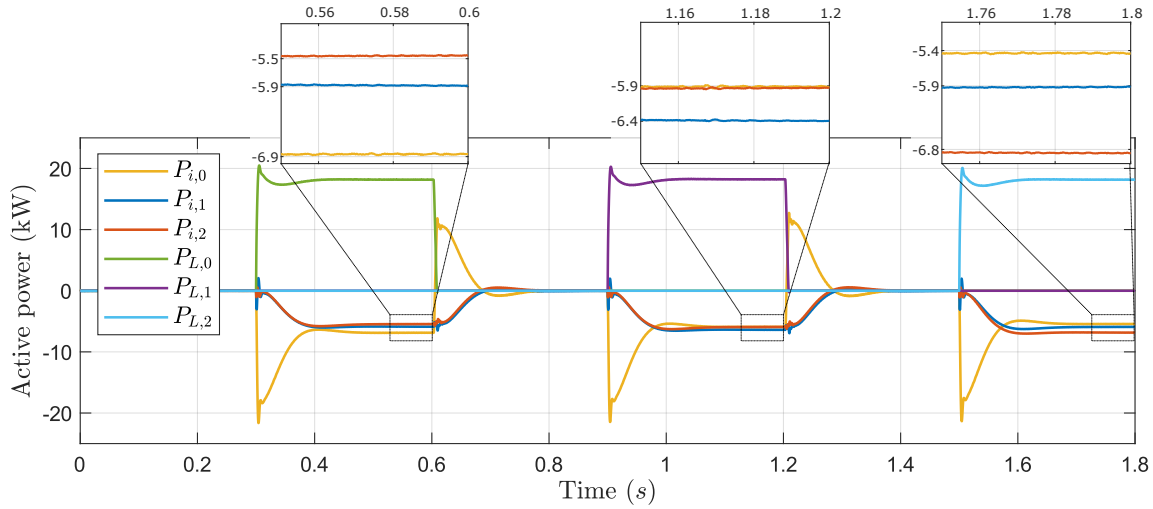
The first test is carried considering normal loads, *i.e.* individual load power inferior to the power rating of each converter. In this simulation test it is considered that $Z_{load,0} = Z_{load,1} = Z_{load,2} = 7.5 + j\omega 7.9m\ (\Omega)$ what corresponds approximately to an individual load power of $S \approx 20\ k$VA with a power factor of 0.95. Furthermore each converter ESS presents a constant $SoC = 0.5$.

The loads are switched on and off sequentially with the $t_{on,0} = [0.0; 0.0]\ ms$, $t_{on,1} = [0.0; 0.0]\ ms$, and $t_{on,2} = [0.0; 0.0]\ ms$. In figure 5.11 it is presented the active and reactive power of each converter and load, for the given test conditions and a line length of $\ell_{(0,1)} = \ell_{(1,2)} = 0.1\ km$, with an aluminium cable with a cross-section of 95 mm^2. In figure 5.12 the results obtained for the same test conditions are shown, with exception of the line length that was changed to $\ell_{(0,1)} = \ell_{(1,2)} = 0.5\ km$.

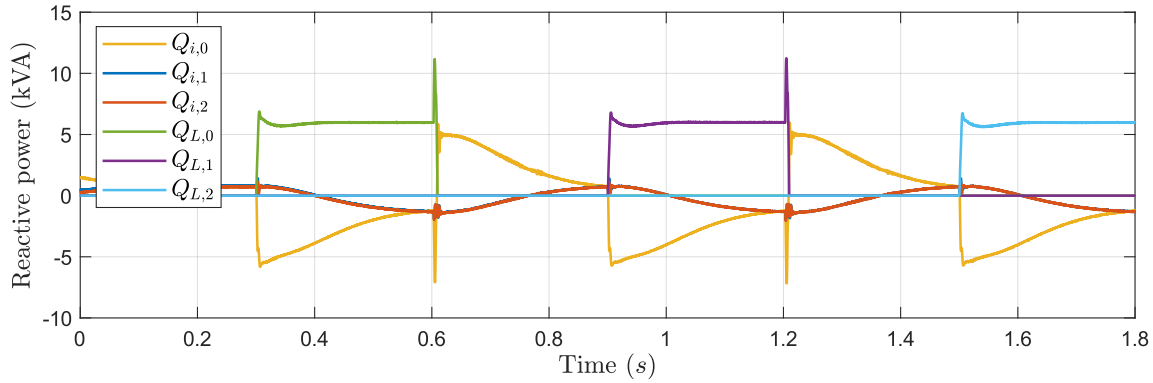
In figures 5.11 and 5.12 it can be visualized that the proposed method allows to share the load power (both active and reactive). The active power presents steady state sharing differences, caused by the different local voltage measurements due to the line voltage drop. Though, as previously mentioned, such behaviour allows increasing the power share of the converter nearest to the local load. For the same reason, it becomes clear that when the line impedance increases (distance change from 0.1 *km* to 0.5 *km*) the power-sharing differences become more severe, as quantified in table 5.3.

In the table it is presented the power share, as a percentage of the load power, of each unit $P_{i,x}$ when feeding the corresponding load $Z_{load,x}$. To ease the evaluation of the line length impact on the power-sharing, it is also shown the corresponding maximum standard deviation σ_{max} for each load interval.

The symmetry of the testbed allows to evaluate the influence in the choice of the grid-forming



(a)

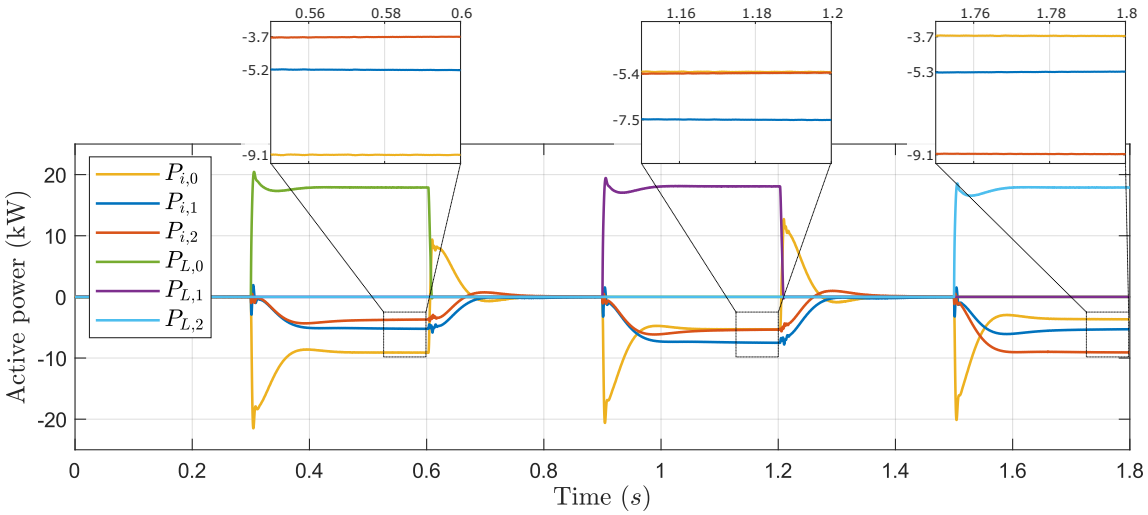


(b)

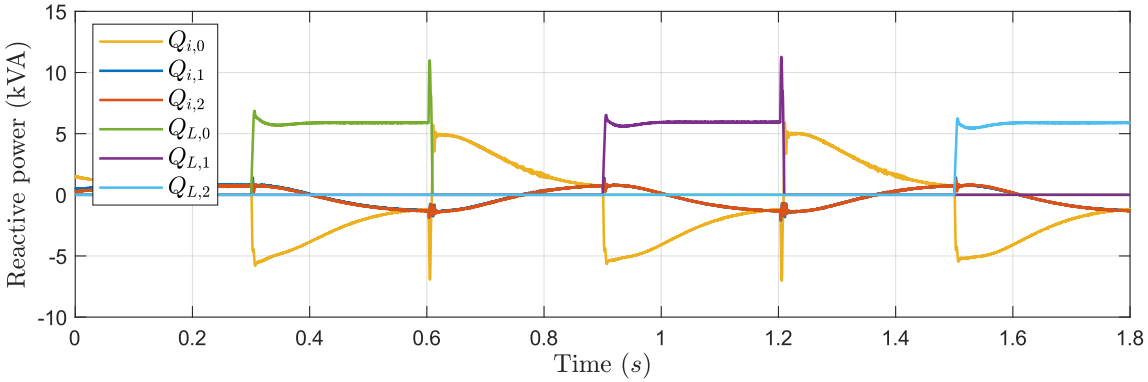
Figure 5.11: Power sharing with normal load and $\ell_{(0,1)} = \ell_{(1,2)} = 0.1\ km$. (a) active power, and (b) reactive power.

node. Steady-state identical power-sharing while supplying $Z_{load,0}$ and $Z_{load,2}$ means that the grid-forming does not bias the steady-state power-sharing. The 1^{st} and 3^{rd} columns (or 4^{th} and 6^{th}) of table 5.3 show that the power-sharing is very similar in both the analysed situations. This result allows at concluding that the power-sharing differences are exclusively due to the line impedance and it is not influenced by the choice of the grid-forming converter.

With the proposed droop $Q - \omega$, the reactive power set-point follows the imposed microgrid frequency changes. Since frequency is imposed by the grid-forming converter and is not influenced by the line impedance, the steady-state reactive power-sharing of each converter converges to a single point value. On another hand, the frequency cannot be directly measured (it is estimated) and



(a)



(b)

Figure 5.12: Power sharing with normal load and $\ell_{(0,1)} = \ell_{(1,2)} = 0.5\ km$. (a) active power, and (b) reactive power.

therefore, reactive power takes more time to reach steady-state.

In both figures, it is also possible to verify the fast response of the grid-forming converter during load change, by observing the load power that is initially fully compensated by the grid-forming converter. The grid-forming converter fast dynamics is achieved due to the proposed VC-PL control loop strategy.

5.3.2 Power-sharing with normal load: different converter power ratings and *SoC*

The testbed and load connection scheme of the test performed on this subsection is similar to the previous test. The testing differences are the change of the converter's power rating and in the

Table 5.3: Steady-state power sharing as a percentage of the load power for the tested line lengths.

	$\ell = 0.1\ km$			$\ell = 0.5\ km$		
	$Z_{load,1}$	$Z_{load,2}$	$Z_{load,3}$	$Z_{load,1}$	$Z_{load,2}$	$Z_{load,3}$
$P_{i,0}$	37.7	32.5	29.9	50.5	29.4	20.3
$P_{i,1}$	32.3	35.0	32.5	29.0	41.2	29.4
$P_{i,2}$	30.0	32.5	37.6	20.5	29.4	50.3
σ_{max}	4.37	1.67	4.27	17.2	7.9	17.0

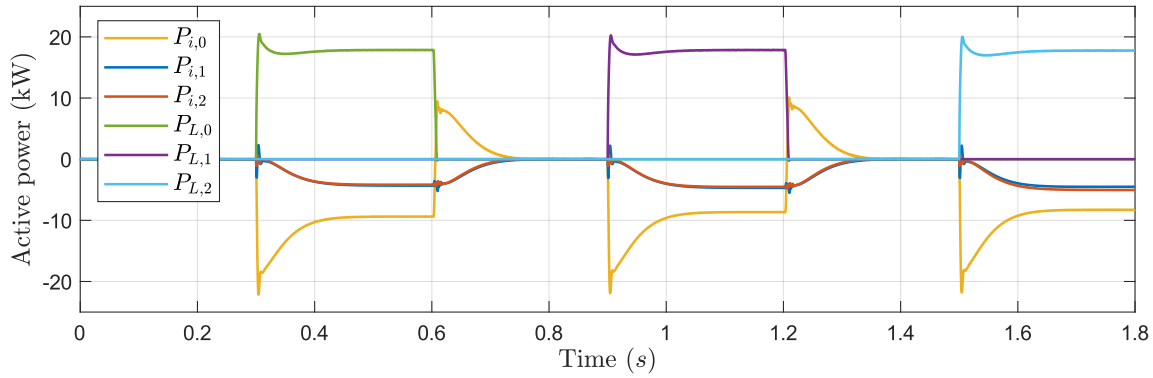
respective ESS *SoC*.

In a real-world example, the change on the converter power rating would demand to design a new *LCL* filter, hardware, etc., and consequently obtain new controller gains. Though for the sake of simplicity, the power rating change is imposed in the control scheme, *i.e.* droop and saturations are configured accordingly with the desired power rating. Additionally, the power-sharing dynamics are slow when compared with the inner control loop one, hence such approximation of the power rating should not bias the results.

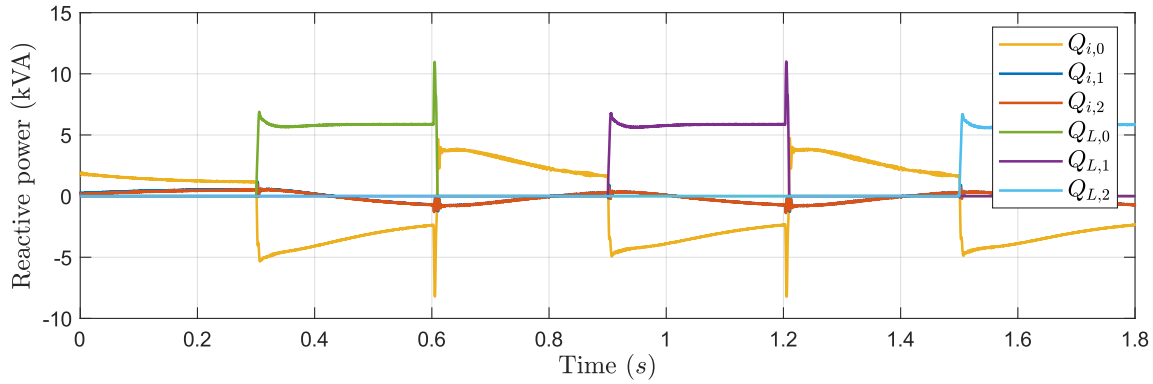
Figure 5.13 shows the results obtained in the aforementioned conditions for different converter power ratings. The converter power ratings are set to $S_{n,0} = 30\ k$VA, and $S_{n,1} = S_{n,2} = 15\ k$VA, where $S_{n,x}$ refers to the rated apparent power of the converter $'x'$. All units present a constant $SoC = 0.5$ and both line lengths present an $\ell = 0.1\ km$.

Figure 5.13 shows that the power-sharing is split between the grid-forming converter and both the grid-supporting converters. The power share of each grid-supporting converter is about 25 %, and 50 % for the grid-forming converter. Such power-sharing is proportional with the rated power of each converter. The reactive power is also affected by the change in the converters power rating, similarly with the active power. The converter rated power influences both active and reactive power droop curves, since both active and reactive power curves are designed considering the rated power.

Figure 5.14 represents the power sharing when each converter unit presents a different *SoC*: $SoC_0 = 0.35$, $SoC_1 = 0.50$, and $SoC_2 = 0.65$. The rated power of each unit is set back to $S_n = 30\ k$VA. In the figure it is only presented the power-sharing of the active power since reactive power is not influenced by the *SoC*, pre-setting the same behaviour shown earlier in figure 5.11(b).



(a)



(b)

Figure 5.13: Power-sharing with converters with different power ratings. $S_{n,0} = 30$ kVA, and $S_{n,1} = S_{n,2} = 15$ kVA. (a) active power, and (b) reactive power.

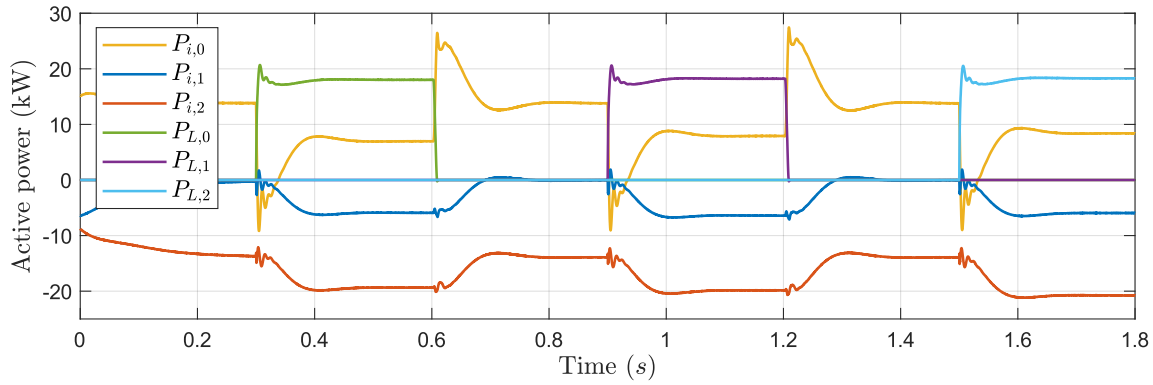


Figure 5.14: Active power-sharing for different ESS SoC ($SoC_0 = 0.35$, $SoC_1 = 0.50$, and $SoC_2 = 0.65$).

All converters participate in the load demand, though with different power magnitudes. In this specific case, converter 0 (grid-forming) fulfils the load power demand transients while keeping charging

its ESS. To be noticed that during this test, the grid-support converters present higher energy availability. Furthermore, it can be noticed that converter 2 (presenting the highest energy availability) is constantly discharging, feeding the load or charging converter 0. During no load, converter 1 does not contribute for the *SoC* balancing, but participate in the power-sharing when loads are connected. Such behaviour indicates that the different units *SoC* will converge to a single value.

In the next subsection is addressed the *SoC* balancing during longer periods of operation.

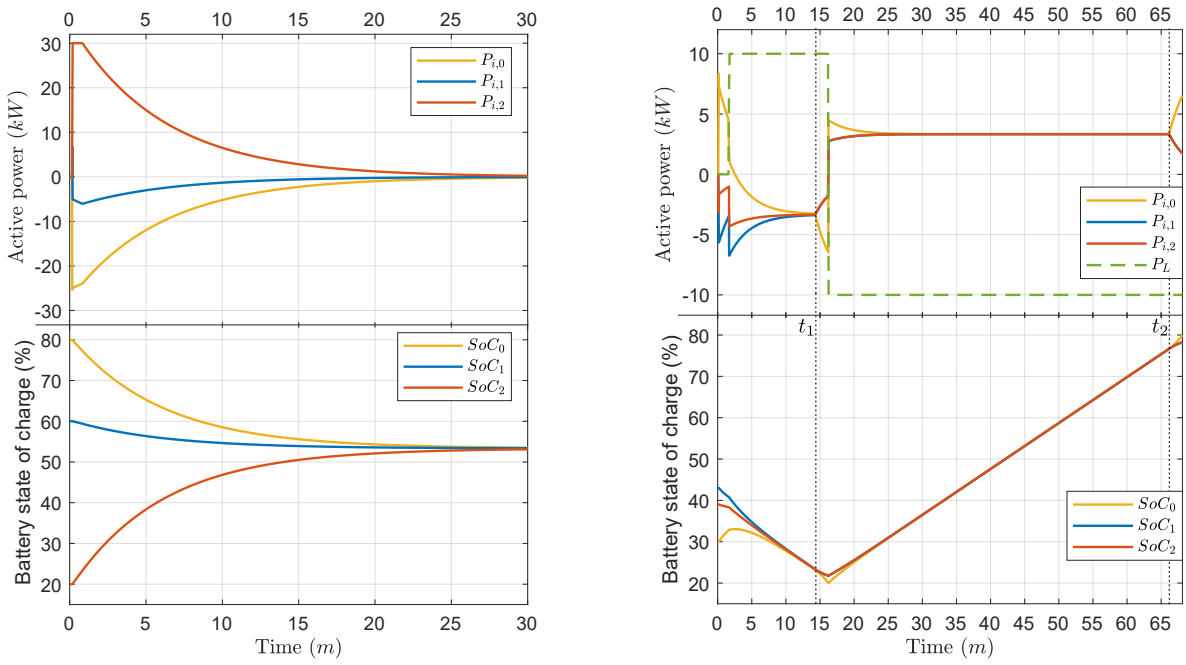
5.3.3 *SoC* balancing through the proposed power-sharing strategy

Exceptionally for this test it was adopted a model based only on the droop curves characteristic, the respective low pass filters, and an additional low pass filter to replace the PLL dynamics with a cut-off frequency of ω_{PLL}. Additionally, the ESS *SoC* is modelled considering that each converter has a 10 kWh ESS and a linear relationship between the available ESS energy and the respective *SoC* (ESS dynamics are neglected).

In figure 5.15(a) they are presented the results for the *SoC* balancing achieved only by interconnecting the three units, *i.e.* there is no additional loads. It can be noticed that the initial unbalanced *SoC* of each units converges to the resulting balanced *SoC*.

To evaluate the interaction between the power-sharing and the *SoC* balancing, the initial *SoC* conditions were changed and it is introduced a constant load during $t \approx [0;16]\,m$, followed by an excess of generation during $t \approx]16;70]\,m$. It is important to highlight two important operation points at: t_1 and t_2 (denoted by dashed lines). Both lines represent a particular condition where the shared load power demand is higher than the grid-support converter's capability. In t_0, such happens because the droop curve shifting limits the maximum negative power accordingly with the *SoC* of each unit, resulting in a limited power contribution. On another hand, the grid-forming converter power limit is independent of the droop curve, instead only the reference voltage amplitude is changed and limited, but will always fulfil the power demand as far as it is within the limits imposed by the hardware. That is the reason why, at these particular points, the load power-sharing divergence is observed (consequently also reflected in the respective *SoC*'s). The scenario repeats at t_2 when there is an excess of power injected in the microgrid.

There are two characteristics to be highlighted when considering the grid-forming converter operating with $P/SoC-V$ and grid-supporting converters operating with $V-P/SoC$ (all with null external power references):



(a) (b)

Figure 5.15: Active power and storage system *SoC*. (a) results with no load, and (b) with load power.

1) converter power sharing is proportional with the available energy and power rating;

2) the system tends toward ESS energy balancing among the connected units. Hence, as far as some units have available energy, system blackout or re-connection with the main grid is prevented.

5.3.4 Power-sharing during overload

In the scope of this thesis, a load which power demand is greater than the grid-forming converter power rating is considered an overload event. For sake of clarity it is not considered the system overload, which would be described as a load power demand greater than the sum of the rated power of all the connected power supply units.

To test the overload detection and system operation, it is considered that the same $Z_{load,0}$, applied in the previous tests, is connected at $t = 0.05\ s$. A second load $Z_{load,1} = 2.5 + j\omega 2.6m\ \Omega$ is applied between $t = [0.35; 1.15]\ s$, resulting in the overload event. In figure 5.16 it is shown the active and reactive power, and the grid-forming converter SRF voltage and current. In the SRF voltage and current plots, the grey areas indicate the time intervals where the corresponding controller (VC for

voltage or CC for the current) is deactivated by the OCD.

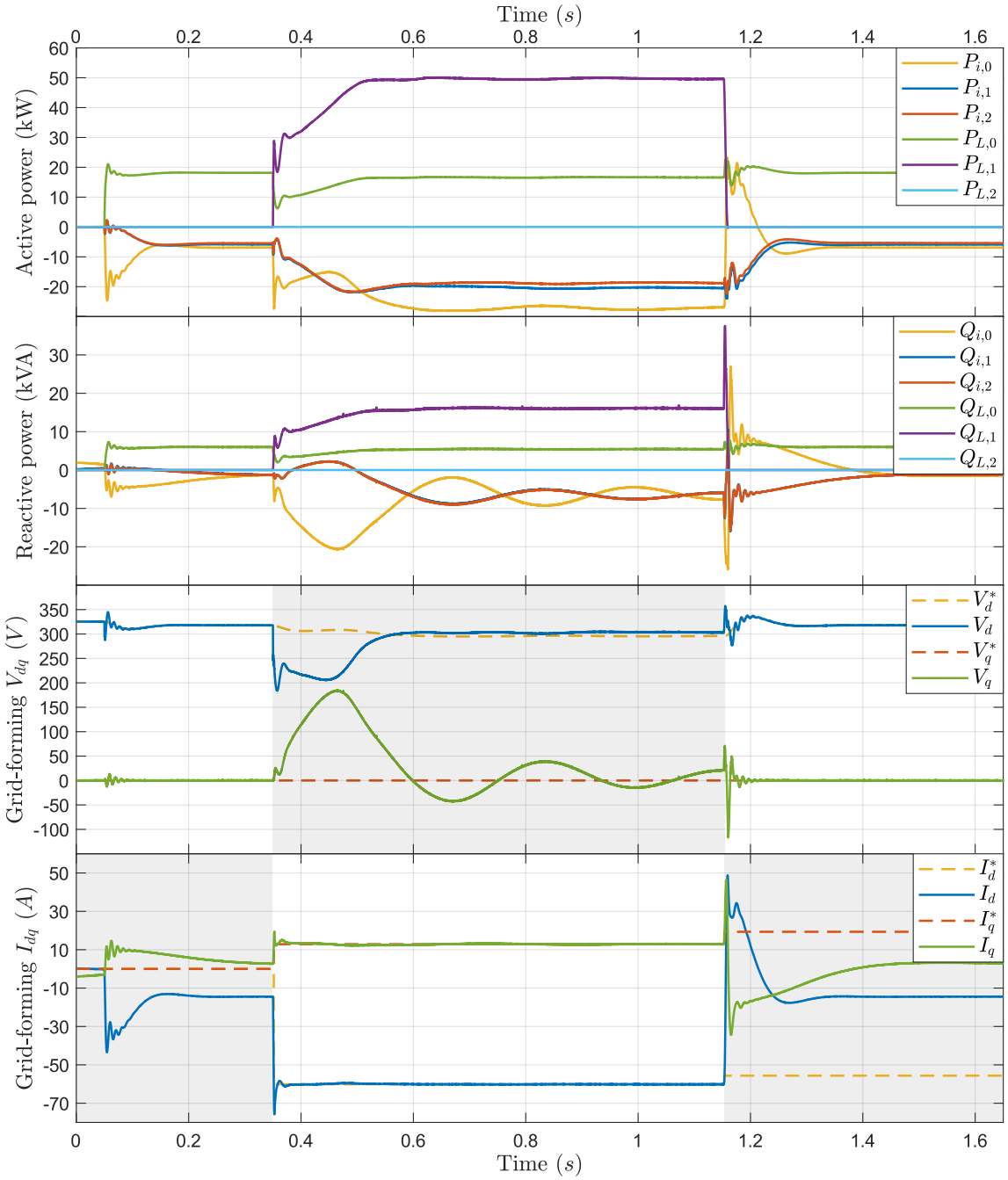


Figure 5.16: Active power, reactive power, SRF voltage and SRF current during overload test with the OCD based on the $|I_{dq}|$ and $V_{m,d(i)}$ as presented in chapter 4.

The results shown in figure 5.16 allow the validation of the current protection offered by the VC-PL with the OCD scheme, since current (I_{dq}) is controlled within the rated limits, despite the initial

overshoot of approximately 10% during the load connection at $t = 0.35\ s$. On another hand, it can be noticed that around $t = 0.6\ s$ the V_d voltage component is higher than the respective reference, while V_q is around 0, which indicates that the current controller is no longer needed, as the CC is already generating a grid voltage above the voltage reference V^*_{dq}. The result helps to explain why in chapter 4 it was introduced an alternative OCD method which includes the described normal operation detection.

Figure 5.17 shows the results, when the OCD presented in chapter 4 identifies the normal operation through the previously described analysis. In the same figure, it can be noticed that the region where the current is controlled has been considerably reduced and consequently, it allows to share the heavy load power with the grid-support converters.

To clarify, figure 5.18 presents the $V_{m,dq(i)}$ during the over-load time period for both OCD configurations, of figures 5.16 and 5.17. The different OCDs only differ in the detection of the normal voltage operation, though such difference has an impact on the formed grid voltage and power-sharing.

The curves illustrated in figure 5.18 are similar in both cases, until the time instant $t \approx 0.6\ s$. At this time, the $V_d > V^*_d \wedge V_q = 0$ conditions are verified, and the respective OCD disable the CC, enabling the VC, as it can be seen by the flushing of $V_{m,dq(i)}$ in figure 5.18 (b). The simpler OCD of figure 5.18 (a) does not verify such condition and waits for the condition of $V_{m,dq(i)} \leq 0$. Such a condition only occurs when the load is disconnected at $t = 1.15\ s$. This result is considerably different from the result obtained in chapter 4, for a single connected unit. The connection of the parallel converters, operating in current (power) control, results in an uncontrolled phase of the voltage phasor, which explains the quadrature component oscillations. Due to the oscillation caused by the interaction with the other parallel converters, $V_{m,dq(i)}$ does not return to 0 and the OCD fails in recognizing that the over-load event no longer exists. Furthermore, independently of the droop voltage, the controlled current increases the formed grid voltage, what also reduces the grid-support converter's power-sharing. It could be noticed that during current control $V_{g,q} = V_{m,q(i)}$ and hence any of these variables could be used to command the OCD trigger back to the voltage control.

To show that there is no filtering effect in the shown SRF voltage and current, the reference phase 'a' of the three phase voltages and currents of the grid-forming converter are shown in figure 5.19. The illustrated voltages and currents are referred to the test conditions of figure 5.17, and the reference phase is chosen as transitions occur during the respective peak values, *i.e.* overload during reference phase current negative peak, and overvoltage (de-loading) during positive peak voltage.

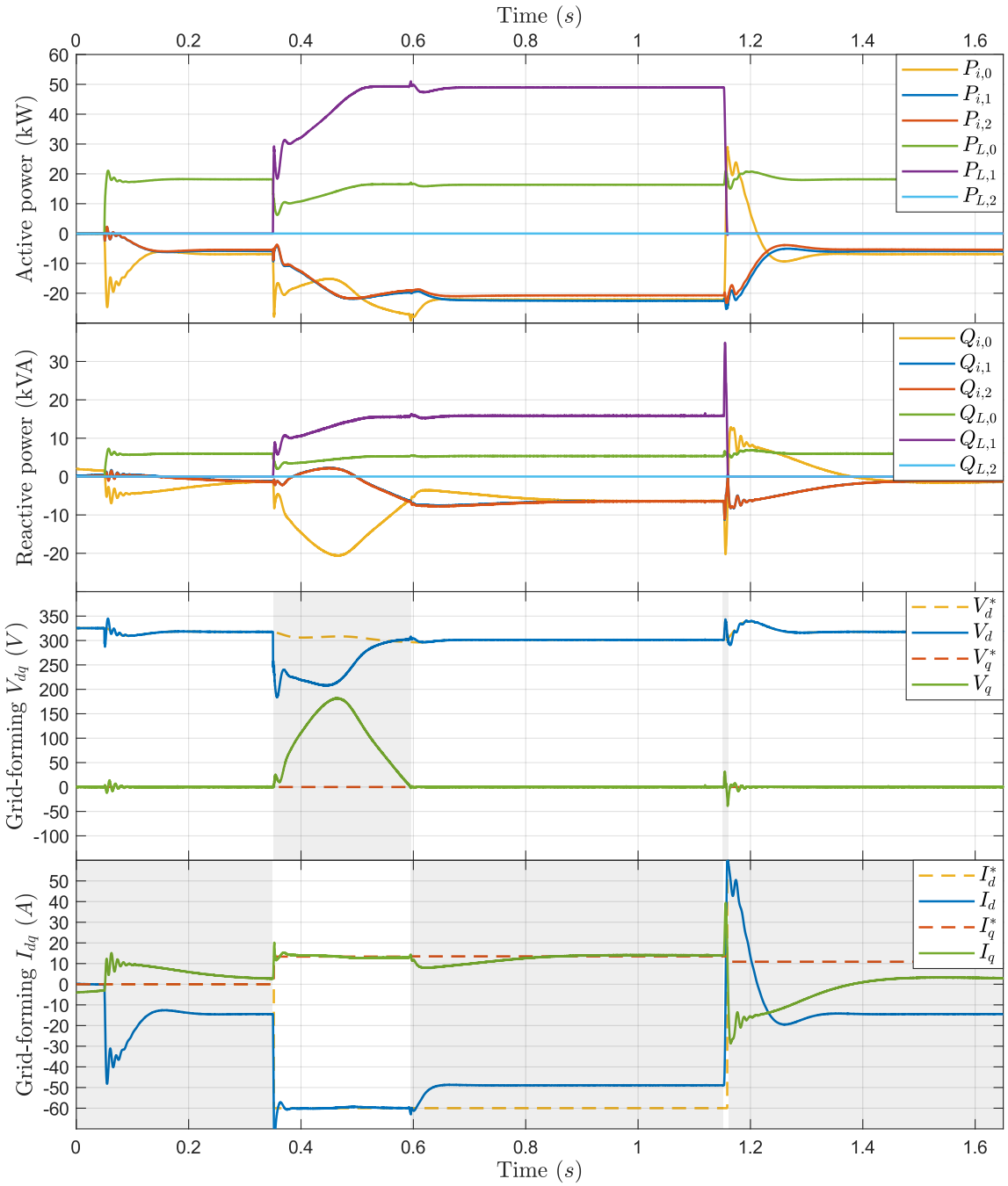


Figure 5.17: Active power, reactive power, SRF voltage and SRF current during overload test with the OCD based on the $|I_{dq}|$, V_{dq}, V_{dq}^* and $V_{m,d(i)}$ as presented in chapter 4.

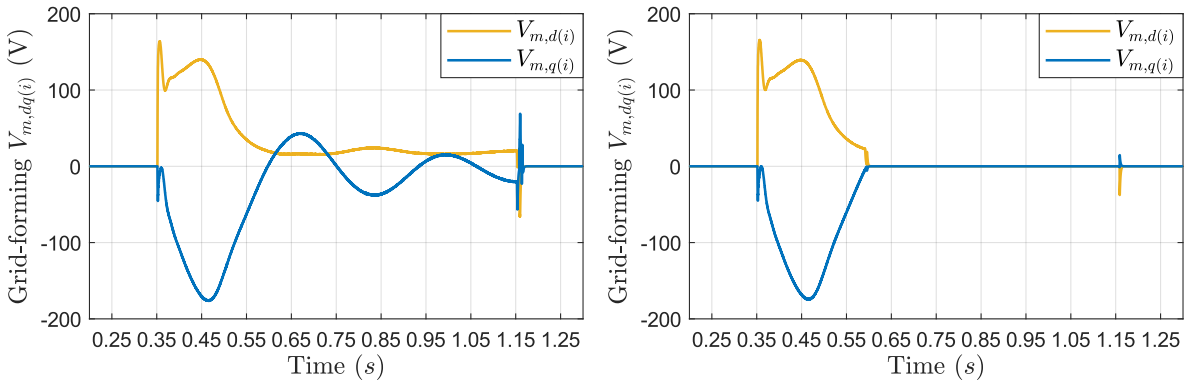


Figure 5.18: Voltage correction from the CC loop of the grid-forming converter during over-load condition. (a) OCD with $|I_{dq}|$ and $V_{m,dq(i)}$, and (b) OCD with $|I_{dq}|$, V_{dq}, V^*_{dq} and $V_{m,d(i)}$, as presented in chapter 5.

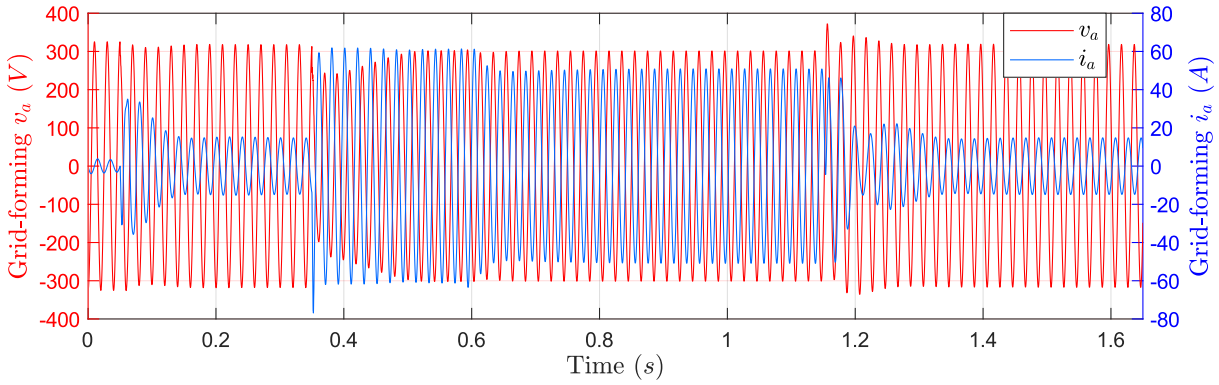
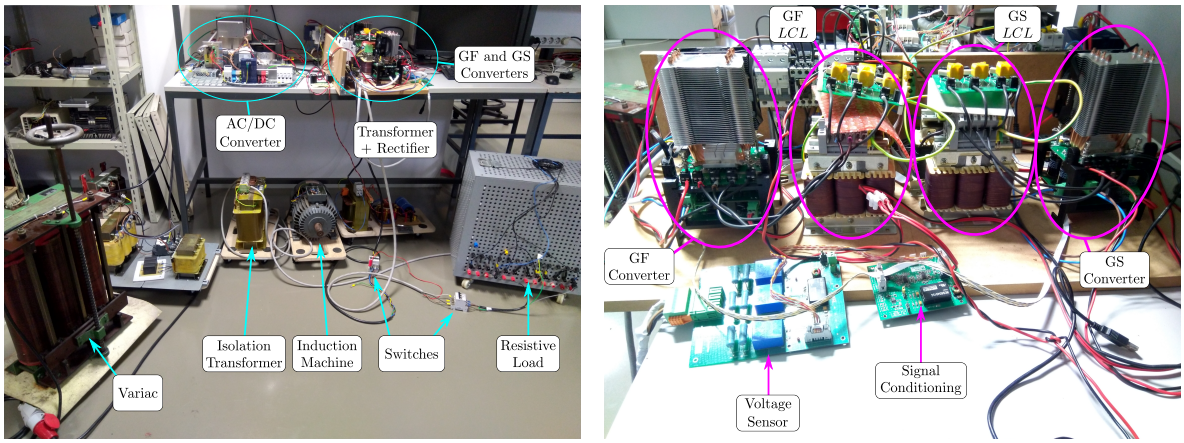


Figure 5.19: Reference phase 'a' voltage and current of the grid-forming converter during test conditions of figure 5.17.

5.4 Experimental results

Figure 5.20 shows the experimental setup used for validation of the researched methods. It consists of a downscale of the previous testbed of figure 5.10, where only two units are used and the line impedance between them can be neglected. Hence, the experimental testbed can be considered a single node system. Additionally, there are no actual batteries in the system, therefore *SoC*'s are defined through software. The grid forming (GF) unit DC bus is regulated by the AC/DC converter connected to the grid through the isolation transformer and the Variac. The grid support converter (GS) DC bus is imposed by the transformer + diode bridge rectifier. The two switches allow connecting/disconnecting the resistive load or the inductive load (induction machine).

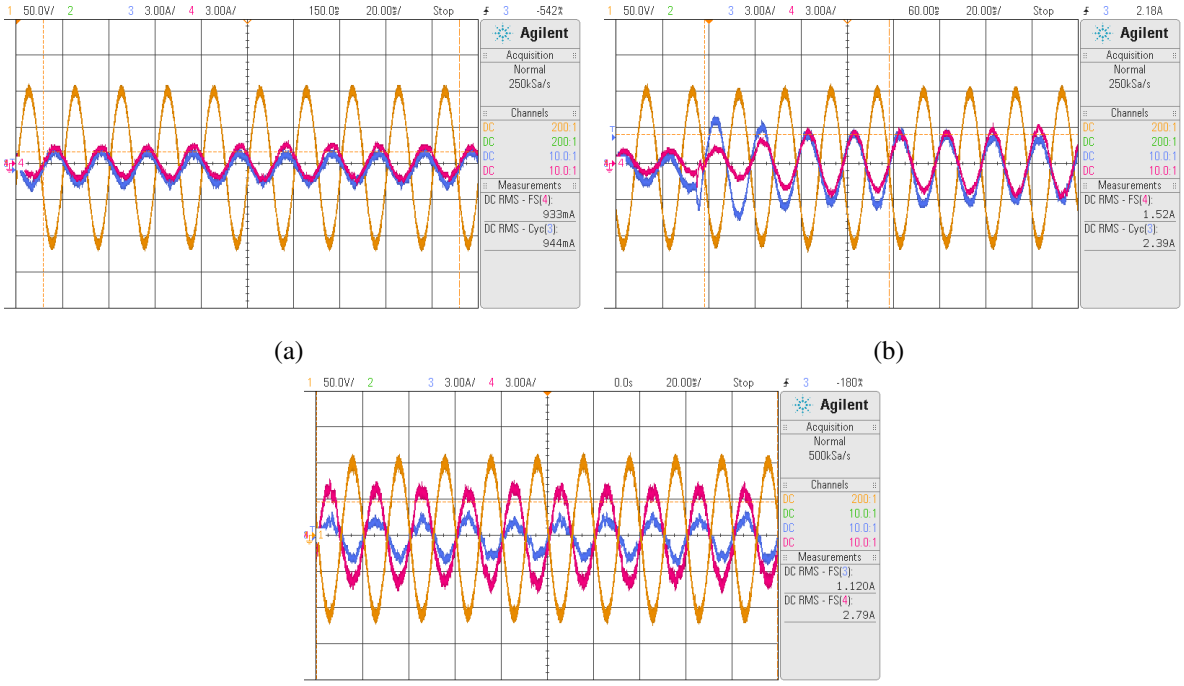


(a) (b)

Figure 5.20: Laboratory experimental setup. (a) Full setup and (b) GF and GS converters, respective filters, and voltage measurements.

Figure 5.21(a) presents the steady state voltage and currents of reference phase '*a*' with the *SoC* of both converters set at 50%. The voltage is measured at the common node, while currents are measured in the output of each converter *LCL* filter. It can be noticed that load power is properly shared by both converters since the currents of each converter present a similar amplitude and phase. The dynamic behaviour during a resistive load change is shown in figure 5.21(b). It can be visualized the fast transient behaviour of the grid-forming converter (blue) and the slower compensation of the grid-support converter (magenta) in which at the end shares the load power with the grid-forming converter. In 5.21(c) it is presented the same load conditions of figure 5.21(b), but with the grid-forming converter presenting a $SoC = 40\%$. In this case, it is noticeable that the grid-forming converter

decreases its power share since it presents less energy availability. For $SoC_0 = 40\%$ and $SoC_1 = 50\%$ the theoretical power share should be of $\approx 30\%$ for the grid-forming converter and $\approx 60\%$ for grid-support, which is close to the obtained values of 28.6% and 71.4% respectively.

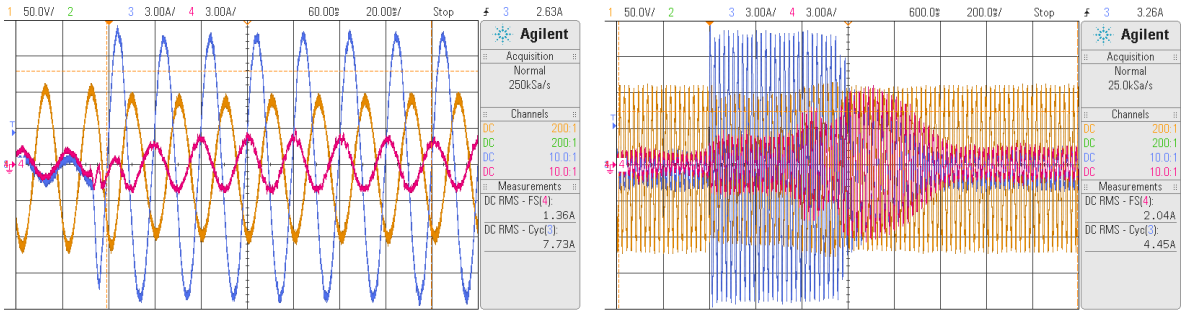


(a) (b)

(c)

Figure 5.21: Steady state condition. Line-neutral voltage at reference phase (yellow), reference phase current of grid-forming converter (blue) and reference phase current of grid-support converter (magenta). (a) initial steady state, (b) resistive load change with $SoC_0 = SoC_1 = 0.5$, and (c) steady state with resistive load with grid forming $SoC_0 = 0.45$ and grid support $SoC_1 = 0.5$.

To show the over-current protection, the figure 5.22(a) is presented, which results were obtained during an induction motor startup. The grid-forming maximum current was set at $|I_{max}| = 7.7\ A_{rms}$. It is noticeable that the voltage sag (yellow) is caused by the maximum current limitation (blue). Additionally, the grid-support converter increases the output current (magenta) to maintain the reference power (droop is on halt when voltage sag is detected). Once the induction motor reaches a certain speed the respective electromotive force increases and the over-current protection is turned off, as it can be seen in figure 5.22(b).



(a) (b)

Figure 5.22: Transient during heavy load change- induction motor startup. Line-neutral voltage at reference phase (yellow), reference phase current of grid-forming converter (blue) and reference phase current of grid-support converter (magenta). (a) initial transient, and (b) total transient.

CHAPTER 6

Conclusions

In the current chapter, it is presented a summary of the thesis's main conclusions (section 6.1). Furthermore, it is also discussed some possible real-world applications of the developed methods and suggested some steps for future work (section 6.2).

6.1 Main Conclusions

In the thesis, it has been addressed some of the critical aspects in the design of power converters to be connected into weak-grids (island microgrids): the PLL, the converter filter design, current and voltage control loops design, and power balancing and sharing between parallel converters.

In chapter 3, different DSOGI PLL implementations for grid synchronization in weak grids were analyzed. Based on the obtained simulation and experimental results it was possible to conclude that all the DSOGI based PLL's allowed to extract with success the fundamental frequency positive sequence grid voltage under different grid conditions. All the tested implementations presented a proper tracking of the grid voltage amplitude, frequency, and phase angle, but showing different dynamic and steady-state responses. Since no clear differences between the considered implementations are highlighted in the literature, based on the obtained test results a benchmark table was presented.

The benchmark table aims to ease the DSOGI based PLL selection considering the performance of each implementation for different grid conditions or events such as low-order harmonics, unbalanced phases, voltage sags, and frequency or phase step changes. The criteria applied in the thesis to the choice of the DSOGI implementation were shown as an example. So the FFDSOGI-PLL was adopted as the most performant according to the requirements within the scope of this work - operation in a weak grid.

The FFDSOGI was also included in the SRF phase angle estimation addressed in chapter 4 where the obtained results also allow to validate the FFDSOGI performance when integrated in the converter inner loop. In chapter 5, the FFDSOGI was also responsible for providing the microgrid voltage

amplitude and frequency to the droop control.

The converter filter and control loops design was presented in chapter 4. The most common filters were discussed, where the *LCL* filter was identified as the filter that offers the best attenuation rate per size. A design algorithm was developed to obtain the filter parameters that minimize the filter size, considering a given maximum capacitive reactive power and target attenuation gains. The algorithm also includes a set of restrictions such as the desired current control bandwidth, damping scheme, PWM update method, expected line impedance, and maximum ripple at inverter side inductance. A design example was shown and later validated in simulation through the evaluation of the resulting current TDD. Contrary to the general guidelines found in the literature, the proposed design algorithm allowed to deterministically obtain the *LCL* filter parameters considering important aspects during operation in weak-grid such as the current controller bandwidth or the impact of line impedance in the filter resonant frequency.

In the same chapter, it is presented a design method for the current and voltage control loops (dual-loop). To overcome the slow voltage response of the dual-loop, an alternative approach is proposed based on a disjointed parallel operation of the current and voltage controllers. The proposed parallel voltage controller results in faster voltage regulation, maintaining the over-current protection capability of the dual-loop. Both the parallel and dual-loop voltage controllers allow the operation with heavy loads, with the parallel loop presenting better performance during load transients (mitigation of transient voltage sags). Through comparison of the different results obtained for the current controller and *LCL* filter, it was possible to further conclude:

- To achieve the smallest filter inductance, in grid-connected operation, SUPWM should be chosen with no damping (or either the SUPWM or DUPWM if active damping is included). Under such conditions, the minimum inductance will be dictated by the reactive power factor x and the *LCL* design solution is found in a single algorithm iteration;

- Decreasing the reactive power factor x in the *LCL* design results in a bigger filter size (higher total inductance), but increases the filter robustness to low order harmonics and consequently improves current harmonics overall spectrum;

- During grid-connected operation, with i_g feedback, the SUPWM and DUPWM presented similar results, with a slight performance improvement of the last one in terms of dynamic response to system perturbations. Though, such a choice implies a higher processing capability and com-

pulsory *LCL* damping (R_d or other) for the same filter size. Additionally, when i_i is chosen, the improved performance of the DUPWM, compared with the SUPWM, is notorious what results in the best TDD$/L_T$ ratio;

- When grid-forming is also considered, it is clear through the obtained simulation results that the DUPWM (damped) robustness is essential to achieve a stable voltage control for the dual loop VC. On another hand, for the parallel loop VC, the control loop remains stable independently of the chosen feedback current (i_i or i_g) or update method, but the DUPWM offers higher robustness and results in lower grid voltage THD;

- Comparing the results obtained for the conventional dual loop and the newly proposed parallel loop, it becomes noticeable the advantages of the second one: fewer tuning parameters, better dynamic response as well as stability with both update methods and for all the different voltage feedback configurations. The advantages of the dual loop are a simpler implementation, since the VC scheme is the same as the CC, and slightly outperforms the parallel loop in the produced THD (0.98 % to 1.06 %), at full power and unity power factor.

In chapter 5 it is presented a new control method to ensure the power balancing and sharing between different ESS's in low voltage microgrids operating in island mode.

Based on the simulation and experimental results, it was possible to validate the proposed adaptive droop strategy that allowed proper power balancing and sharing, overload capability, and balancing of the connected ESS's *SoC*. Using a single grid-forming converter to signal the power demand to the grid-support converters, allows achieving proper power-sharing without requiring previous knowledge about the line impedance or the addition of a virtual impedance. The researched method takes advantage of the transient response of the grid-forming converter dynamics (operating with the VC parallel loop) adding inertia to the system by allowing it to seamlessly fulfill the load power demand. The presented adaptive droop shifts the active power droop accordingly with the ESS *SoC*, ensuring that load is compensated mostly by the storage system with higher energy availability while charging the storage systems that present less energy availability. The balancing of the different units *SoC* allows to avoid the energy depletion of a single unit and consequently lose its power availability.

An additional advantage of the proposed strategy is that using a single grid-forming converter to signal the power demand to the grid-support converters, allows achieving a proper power-sharing without requiring previous knowledge about the line impedance. Since the unequal line impedances

increase the share of the nearest ESS converter (lower line impedance) overall power losses are reduced as far as the different ESS's *SoC* remain balanced.

Less good performance of the researched method is related with the operation near limit conditions:

- when global $SoC \approx SoC_{max}$ with excess of power generation, or $SoC \approx SoC_{min}$ with excess of load power, the proposed scheme results in power-sharing deviances, overloading the grid-forming converter and requiring anticipation of re-connection with the main grid, to prevent local system blackout;

- during fast transients, the grid-forming converter fulfils the power transients without the support of the grid-support converters. With the increasing number of fast loads connection, the power availability of the grid-forming converter decreases leading to a higher number of over-current detection events (voltage sags occurrences). The voltage sags in combination with the voltage deviance intrinsic to the proposed method may compromise the local grid stability, since units may trip (sensible loads) or operate at de-rated conditions (passive loads).

The work presented in the thesis expresses a step-by-step design of some of the critical aspects of power converters in the scope of operation in island microgrids. The proposed method allows operating with multiple ESS's in parallel based only on its local control, *i.e.* without requiring a communication link, which was the main goal of this thesis. Furthermore, the decentralized approach also allows a seamless expansion of the number of connecting units increasing the steady-state power and energy availability.

6.2 Applications, Limitations and Future Work

The proposed strategy can be applied in a vast number of applications. Some examples could be in charging stations with renewable energy resources and storage systems, allowing islanding without compromise the vehicle charging. Additionally, the method can be also implemented in a vehicle-to-grid approach, allowing multiple cars to generate a local grid in off-grid areas. Another example is the application in a vehicle-to-vehicle charging, where several vehicles may share the available energy and balance their batteries *SoC*.

In an urban scenario, the proposed scheme could be applied to residential or office buildings, or extended to entire neighborhoods. A particularly interesting application to be explored on such sce-

nario is to include the proposed method in a solid-state power transformer. In this particular case, the transport line MV could be transformed to a regulated LV, following the proposed grid-forming converter droop. Such a scenario could justify the choice of a single grid-forming unit. Furthermore, through manipulation of the adaptive droop, the power-flow between the LV and MV could be modified to regulate the power flow between the MV and LV accordingly with different necessities. As an example it could be adapted according to the daytime, for main grid peak-shaving purposes, or adapted to achieve a steady-state constant power, allowing it to operate as a feeder-flow controller (dispatchable load).

It is also proposed to extend the method to handle unbalanced phases by implementing a virtual impedance to the zero and negative sequence as suggested in [109]. Another extent of the current work can be to further study the $P - SoC$ adaptive droop performance considering different power/energy ratios of the storage systems of each unit, and to enhance the method to fully use the grid-support storage system energy before blackout or re-connection with the main grid. Furthermore, it is also suggested to study the method transient power scalability, *i.e.* considering multiple grid-forming converters operating in parallel, and optimize the different time constants of the system.

It was already referred the advantages of the proposed scheme, though some of the less good aspects can be highlighted, as mentioned in chapter 5. Despite the parallel loop voltage control advantages, its design may be more complex due to the non-linear nature introduced by the control loop selection by the over-current detector. The disturbance occurrence during control loop switching after an overload event may present a severe impact on the system stability when a higher number of grid-support converters are connected. Therefore, it is suggested to address such stability studies to measure the expandability of the proposed method. The operation in the identified limit regions (near the connected ESS's overall *SoC* limits) is another topic that should be addressed in the future. An idea to overcome such limitation is to implement a mechanism in the grid-forming converter, *e.g.* through a virtual power component, that could bring the measured active power to zero with slow dynamics. Consequently, the grid-forming converter would present maximum power availability in steady-state, independently of the overall *SoC* of the grid-support converters. Such an approach could also justify the study on different ESS technologies, *e.g.* through the application of hybrid supercapacitors in the grid-forming converter.

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Appendices

APPENDIX A

Line impedance characteristics

In this appendix, it is presented the line impedance characteristics applied to the low voltage grids, following [110]. The line impedance is or accounting with the output filter inductance, based on the chosen controlled voltage node. In both cases equivalent line R/X is analysed, followed by a discussion about the need for real or virtual impedances to decouple the power flow in the line.

The line impedance for different cable cross-sections is presented in table A.1, where resistance is given at 80 ^oC and impedance is normalized over cable length.

Table A.1: Line impedance for different cable cross-sections. Resistance is given at 80 ^oC.

	$A\ (mm^2)$	$R\ (\Omega/km)$	$X\ (\Omega/km)$	R/X	$\lvert Z\rvert\ (\Omega/km)$	$\theta\ (^o)$	cos	sin
Cu	1.5	15.10	0.118	128.0	15.10	0.45	1.00	0.01
	2.5	9.080	0.109	83.30	9.081	0.69	1.00	0.01
	4.0	5.680	0.101	56.24	5.681	1.02	1.00	0.02
Al	10	3.740	0.086	43.44	3.741	1.32	1.00	0.02
	16	2.356	0.082	28.84	2.357	1.99	1.00	0.03
	25	1.494	0.081	18.38	1.496	3.11	1.00	0.05
	35	1.077	0.078	13.76	1.080	4.16	1.00	0.07
	50	0.796	0.078	10.22	0.800	5.59	1.00	0.10
	95	0.397	0.076	5.210	0.404	10.9	0.98	0.19
	185	0.206	0.074	2.776	0.219	19.8	0.94	0.34
	300	0.129	0.075	1.720	0.149	30.2	0.86	0.50

Considering the line impedances list, given in table A.1, it is possible to choose the right cable cross-section considering a given maximum line length (ℓ) and voltage drop, where the last is considered to be 4 % (as defined in IEC 60364-5-52) at maximum power (S_{max}). For simplicity, it is

considered that a single line connects the converter with the feeder, and therefore normative maximum voltage drop is only relative to a single cable.

As an example of cable selection, the 30 *kVA* converter of chapter 4 is considered, where the designed *LCL* presents a total inductance of 2448 μH, equally split between the grid-side and inverter-side inductances. The respective connection schematic is presented in figure A.1, where v_m is the modulated voltage at fundamental frequency, v_c is the voltage measurement at the *LCL* capacitor, v_i the voltage measurement at filter output and v_g the microgrid or grid voltage. Neglecting high order current harmonics, the figure presents a single current loop between v_m and v_g. Hence, equivalent line impedance is dependent on the voltage measurement node:

- v_i voltage node: line reactance is uniquely dependent on the cable selection ($X = X_\ell$);
- v_c voltage node: line reactance also accounts with the *LCL* filter grid-side inductance ($X' = X_\ell + X_{f,g}$);
- v_g voltage node: the total line reactance includes both line and total filter impedance ($X'' = X_\ell + X_{f,g} + X_{f,i}$). In this case voltage is controlled in open-loop.

The resulting cable selection and respective impedance is given in table A.2, where it is shown the cross-section of the cable applied in the case of Portuguese distribution lines [111]. The line reactances (X, X', and X'') take into consideration the reactance seen from the voltage control node, as explained before.

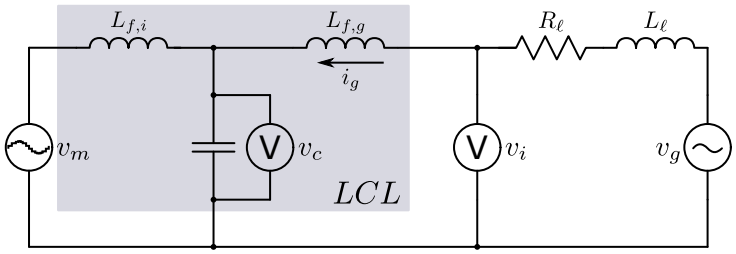


Figure A.1: Schematic of grid-connected converter.

In table A.2 it is considered that power coupling exists only when $0.1 < R/X < 10$ which results in a line impedance angle of approximately $5\ ^o < \theta < 95\ ^o$ (cells coloured in red). Hence, for the presented values, when power is controlled at filter output ($X = X_\ell$), power coupling exists only when considering a cable length of $\ell > 190\ m$. On another hand, if power is controlled at *LCL* capacitor or

Table A.2: Cable selection, line impedance, maximum power flow for 4 % voltage drop, and R/X ratio considering: only line (X), accounting also with grid-side filter (X'), or including the total filter (X'') reactances.

					X	X'	X''
ℓ (km)	A (mm^2)	S_{max} (kVA)	R_ℓ (Ω)	X_ℓ (Ω)	R_ℓ/X	R_ℓ/X'	R_ℓ/X''
0.09	16	31.7	0.212	0.007	28.8	0.541	0.273
0.19	35	30.9	0.205	0.015	13.8	0.512	0.261
0.52	95	30.2	0.206	0.040	5.21	0.487	0.255

in open-loop, output grid reactance becomes part of the line and consequently, there is power coupling at any considered line length.

To ensure power decoupling in the aforementioned examples, it is assumed that a resistor is placed in series with line impedance when v_g measurement is considered. When v_c or v_m nodes are chosen, the obtained R/X ratio suggests a stronger inductive nature ($R/X < 0.5$), and therefore an inductance is added instead of the resistance. Noteworthy that impedance may be physically inserted in the circuit or virtually added in the control loop. Following the example of table A.2, to guarantee power decoupling, considering the aforementioned conditions, a $R_v = 0.19\ \Omega$ is added in the v_g case, and a $L_v = 5.6\ mH$ ($X_{v,g} = 1.76\ \Omega$) or $L_v = 4.3\ mH$ ($X_{v,i} = 1.35\ \Omega$) in the v_c and v_m alternatives. The resulting line impedance characteristic is shown in table A.3. It is noticeable that the additional impedance in all cases allows a decoupled power control for any of the given cable lengths.

Table A.3: Cable selection, line impedance, maximum power flow for 4 % voltage drop and R/X ratio considering line and virtual impedance. $R' = R_\ell + R_v$ for controlled v_i node, or $X'_v = X_\ell + X_{f,i} + X_{v,g}$ for controlled v_c node, and $X''_v = X_\ell + X_{f,i} + X_{f,g} + X_{v,i}$ for controlled v_m node.

					X	X'	X''
ℓ (km)	A (mm^2)	S_{max} (kVA)	R_ℓ (Ω)	X_ℓ (Ω)	R'/X	R_ℓ/X'_v	R_ℓ/X''_v
0.09	16	31.7	0.212	0.007	54.7	0.099	0.100
0.19	35	30.9	0.205	0.015	26.5	0.095	0.096
0.52	95	30.2	0.206	0.040	10.0	0.095	0.096

APPENDIX B

LCL design algorithm

In this appendix, it is shared the *LCL* design algorithm coded in *Matlab*. The algorithm flow-chart is presented in chapter 3.

Matlab Code

```
%% Converter parameters
% [Sn Vn  fsw  fn Vbus]
P=[30e3  400 5e3  50 700];

Sn=P(1);                    % W- nominal power
Vn=P(2);                    % V- rms line-to-line voltage
In=sqrt(3)/3*Sn/Vn;         % I- rms line current
fsw=P(3);                   % Hz- switching frequency
fn=P(4);                    % Hz- fundamental frequency
Vbus=P(5);                  % V- DC bus Voltage

%% 1) LCL design configuration
% Strict constraints
% 1.1) Select current control: 1.Grid CC or 2.Converter CC
cm=1; % not used
% 1.2) Select desired inductance ratio rl
mu=1.0;
% 1.3) Insert harmonic voltage produced by modulation in p.u. (at
    mf-2)
```

```
19 Vmf_2=0.31; %(@ ma=0.89 - Vn+dV(L));
20 % 1.4) Maximum expected grid impedance
21 dLg=320; % 1 km of cable
22 % 1.5) Insert maximum current ripple at semi-conductors (%)
23 di_i=10;
24
25 % 1.6) (=2) if resistive damping in series with C is used...
26       ...(=1) for active damping and...
27       ...(=0) for no damping.
28 damp=2;
29 % 1.7) Insert kf step
30 dkf=0.001;
31
32 %% 2. Flexible constraints
33 % 2.1) Select target current ripple in grid side inductance at mf
       (%)
34 i_h=0.3;
35 % 2.2) Select update PWM method: 2. double update or 1. single
       update
36 Kpwm=1;
37 % 2.3) Select minimum resonant frequency (for control loop porposes
       )
38 fmin=100;
39 % 2.4) Insert maximum reactive power at capacitor (p.u.)
40 x_max=0.025;
41
42 %% 3. Filter initial processing
43 s=sprintf('Initialize variables...');disp(s);
44
45 Ts=1/(fsw*Kpwm);
46 wn=2*pi*fn;
```

```
47 wsw=2*pi*fsw;
48 fs=Kpwm*fsw;    % single or double update PWM
49
50 % 3.1) Calculate frequency ratios: minimum, critical and maximum
51 %     kf_lim = [kf_min kf_crit kf_max]
52 kf_max=fsw/(fmin*10);
53 kf_lim=round([fsw/(0.5*fsw) 6*Ts*fsw-0.001 min(fsw/(10*fn),kf_max)]
       , 3);
54 if (damp>0)
55     kf_lim(2)=20; % to ignore critical frequency ratio
56 end
57
58 % 3.2) Initialize kf
59 % w/damping: kf gets kf_max or kf_crit w/o damping
60 kf=kf_lim(end);
61 if (damp==0)
62     kf=kf_lim(2)+0.5*(min(kf_lim(2),kf_lim(3))-kf_lim(1)); % kf=(
          kcrit+kmin)/2
63 end
64 kf=round(kf,2);
65 kf0=kf;
66
67 % 3.3) initialize target variables
68 if damp==2
69    kVd=1/(1-((fsw/kf/(fsw-fsw/kf))^(40/20)-(fsw/kf/(fsw-fsw/kf))
          ^(60/20)));
70 else
71    kVd=1;
72 end
73 V_pu=Vmf_2*1.0625*kVd; % Converter factor
74 Ig_pu=i_h/100;
```

```
75 Ii_pu_max=di_i/100;
76
77 % 3.4) Calculate base impedances and target harmonic frequency
78 Zb=Vn^2/Sn;
79 Cb=1/(wn*Zb);
80 Lb=Zb/wn;
81 hsw=fsw/fn;
82
83 % 3.5) Initialize checking flag, cycle counter and maximum #cycles
84 fcheck=zeros(1,8);
85 loop=1;
86 n=1;
87 N_cycles=round(max(kf_lim)/dkf);
88
89 %% 4. filter design cycle
90 % Begin cycle
91 s=sprintf('Checking constraints...');disp(s);
92 while(loop>0)
93     % 4.1) Calculate Lt min (kf, hsw, i_pu)
94     Lt_pu=1/(hsw*abs(Ig_pu/V_pu)*abs(1-kf^2));
95     Lt=Lt_pu*Lb;
96     Li=Lt*mu/(1+mu);
97
98     % 4.2) Calculate C from Lt*C
99     C=kf^2*(1+mu)^2/(4*pi^2*fsw^2*mu*Lt);
100    x=C/Cb;
101
102    % 4.3) Calculate damping resistance Rd and ressonant frequency
103    fres=fsw/kf;
104    Rd=1/(3*2*pi*fres*C);
105    gamma=dLg/Li;
```

```
106
107     %% 5. check constraints
108     % fcheck(i) = -1 (reduce kf) ; +1 (increase kf)
109
110     % 5.1) Reactive power in C inside limits
111     if (x>x_max), fcheck(1)=-1;
112     else, fcheck(1)=0;
113     end
114
115     % 5.2) Filter fulfill inverter side harmonics
116     Ii_pu=kf^2*(1+mu)*Ig_pu;
117     if (Ii_pu>Ii_pu_max), fcheck(2)=-1;
118     else, fcheck(2)=0;
119     end
120
121     % 5.3) kf within min and max limits
122     if (kf<kf_lim(1)), fcheck(3)=+1;
123     elseif (kf>kf_lim(3)), fcheck(3)=-1;
124     else, fcheck(3)=0;
125     end
126
127     if (damp==0) % No damping
128     % 5.4) Check kf_crit
129         if (kf>=kf_lim(2)), fcheck(4)=-1;
130         else, fcheck(4)=0;
131         end
132
133     % 5.5) Ressonant frequency change with line inductance
134         kf_l=wsw/sqrt((1+mu+mu*gamma)/(mu*Li*C*(1+gamma)));
135         if (kf_l>=kf_lim(2)), fcheck(5)=-1;
136         elseif (kf_l<kf_lim(1)), fcheck(5)=1;
```

```
137             elseif (kf_l>kf_lim(3)), fcheck(5)=-1;
138             else, fcheck(5)=0;
139             end
140         end
141
142         %% 6. Evaluate contraints check and update kf
143         % 6.1 Check if kf signaling present opposite signals
144         if (sum(fcheck+abs(fcheck))~=0)
145             s=sprintf('(1) No solution found!');disp(s);
146             loop=-1;
147         end
148
149         % 6.2 Check if maximum number of cycles was reached
150         if (n>N_cycles)
151             s=sprintf('(2) Maximum #cycles reached!');disp(s);
152             loop=-1;
153         end
154
155         % 6.3 Update kf or check if a suitable solution was found
156         check=sum(fcheck);
157         if (check>0), kf=kf+dkf;
158         elseif (check<0), kf=kf-dkf;
159         else
160             loop=0;
161             s=sprintf('Solution found at kf= %.3f, after %i iteration(s
                    )',kf, n);disp(s);
162         end
163         n=n+1;
164 end
165
166 if loop==0
```

```
167         s=sprintf('LCL parameters obtained:');disp(s);
168         s=sprintf('Li = Lg = %i uH',ceil(Li*1e6));disp(s);
169         s=sprintf('C = %.2f uF',ceil(C*1e6));disp(s);
170         s=sprintf('LtC = %.3f uHF',Lt*C*1e6);disp(s);
171         s=sprintf('Li Lg C= %.3f nHF',Li*mu*Li*C*1e9);disp(s);
172         s=sprintf('Rd = %.2f Ohm',Rd);disp(s);
173         s=sprintf('fres = %.3f kHz',fres*1e-3);disp(s);
174         s=sprintf('fc = %.3f Hz',fres/10);disp(s);
175         s=sprintf('x = %.3f',x);disp(s);
176 end
```

The resulting command line output, for the given configuration in the code, is:

```
Initialize variables...
Checking constraints...
Solution found at kf= 2.999, after 2002 iteration(s)
LCL parameters obtained:
Li = Lg = 1224 uH
C = 15.00 uF
LtC = 0.036 uHF
Li Lg C= 0.022 nHF
Rd = 2.14 Ohm
fres = 1.667 kHz
fc = 166.722 Hz
x = 0.025
```