FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO



Implementation of Wireless Communication for IoT with Vortex Nano-Oscillators

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WORKING VERSION

Mestrado Integrado em Engenharia Eletrotécnica e de Computadores

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November 30, 2020

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Abstract

This thesis aims to test the ability to use (Spin Torque Vortex Oscillators) STVOs, provided by INL (International Iberian Nanotechnology Laboratory), and current sources as a simple and complete MFSK transmitter/receiver systems, eliminating the need to use traditional electronic elements such as frequency mixers, local oscillators, PLLs and more complex systems such as multiple single frequency detectors. The main objective is to make this system compatible with real world applications.

To achieve this purpose a system, controllable via TCP/IP, in this case by a computer, capable of interacting with the STVOs was designed and tested. This system consists of a computer, a FPGA development board, and two designed PCBs. A carrier PCB to wirebond the STVOs and a PCB responsible for data conversion between analog and digital domains and additional signal conditioning.

A transmitter based on the STVOs provided can have an output power as high as -30 dBm. Under certain conditions, their output frequency can be almost linearly dependent on an input current. One possible configuration for a receiver based on a STVO (frequency sensor) is characterized by translating an input frequency directly to a voltage level. This type of receiver requires an high input power, typically higher than 0 dBm.

It was possible to demonstrate a transmission system based on MFSK modulation using 3 symbols at a maximum symbol rate of 1.25 MSPS for frequencies between 220 MHz and 235 MHz. It was also possible to demonstrate the frequency sensor behaviour on a STVO, although it was not possible to achieve a stable and repeatable operating point to be able to further characterize the receiver.

Resumo

Esta tese tem como objetivo testar a capacidade de utilizar STVOs (Spin Torque Vortex Oscillators), fornecidos pelo INL (International Iberian Nanotechnology Laboratory), e fontes de corrente como sistemas simples e completos para transmissão / recepção de sinais MFSK(M-FSK) . Este sistema elimina a necessidade de utilizar elementos eletrónicos tradicionais, como frequency mixers, osciladores locais, PLLs e sistemas mais complexos, como múltiplos detetores de uma única frequência . O objetivo principal é viabilizar este sistema com aplicações do mundo real.

Para tal foi desenhado e testado um sistema, controlável via TCP / IP, neste caso por um computador, capaz de interagir com os STVOs. Este sistema consiste num computador, numa placa desenvolvimento com um FPGA e em duas PCBs. Uma das PCBs serve de portadora para os STVOs, conectando-os à PCB. A outra PCB é responsável pela conversão de dados entre domínios analógicos e digitais e pelo condicionamento de sinal.

Um transmissor baseado nos STVOs fornecidos pode ter uma potência de saída de até -30 dBm. Em certas condições a sua frequência de saída pode ser quase linearmente dependente da corrente nele imposta. Uma configuração possível para um receptor baseado em um STVO (sensor de frequência) é caracterizada por traduzir uma frequência de entrada diretamente para um nível de tensão. Este tipo de recetor requer uma alta potência de entrada, normalmente superior a 0 dBm.

Foi possível demonstrar um sistema de transmissão baseado em modulação MFSK usando 3 símbolos a uma taxa de símbolo máxima de 1,25 MSPS para frequências entre 220 MHz e 235 MHz. Foi ainda possível demonstrar o comportamento do sensor de frequência de um STVO. No entanto, não foi possível alcançar um ponto de operação estável e repetível, o que impossibilitou uma posterior caracterização do desempenho do recetor.

Acknowledgement

First of all I am grateful to The INL International Iberian Nanotechnology Laboratory, in particular to Ricardo Ferreira, Group Leader of the Spintronics research group at INL and Alex Jenkins staff researcher at INL for arranging an internship at INL and providing their time and the necessary help required to make this thesis viable.

I am also thankful to my supervisors and professors at FEUP Cândido Duarte and Vítor Tavares for accompanying me throughout the thesis development.

A special thanks to Pedro Alves, Professional Engineer at FEUP for providing his expertise and time necessary to assemble the implemented PCBs.

João Presa

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Abreviaturas e Símbolos

FL	Field Line
FSK	Frequency Shift Keying
GMR	Giant magnetoresistance
INL	International Iberian Nanotechnology Laboratory
MTJ	Magnetic Tunnel Junction
PCB	Printed Circuit Board
STNO	Spin Transfer Nano-Oscillator
STVO	Spin Torque Vortex Oscillator
TL	Transmission Line
TMR	Tunnel magnetoresistance

Chapter 1

Introduction

1.1 Context

Spintronics is a field of research focused on the spin of electron [1]. An elementary device of spintronics consists of two magnetic layers separated by a non magnetic layer. A direct current flowing through such a device can transfer spin angular momentum between the two magnetic layers [2] leading to changes in the magnetization. Together with magnetoresistance, which is the change of electrical resistance with the magnetization of the material, there is a large number of interesting physical phenomena that can occur, such as magnetization reversal and self-sustained, large amplitude magnetization oscillations [3].

Two of the most successful applications are Tunneling magnetoresistive reading heads (TMR) [4] used in the magnetic data storage systems and Magneto-resistive Random Access Memory (MRAM) [5].

Recently there has been a lot of work in developing spin transfer nano-oscillators (STNOs): nanometric devices capable of transforming DC to RF and RF to DC [6], based on self-sustained, large amplitude magnetization oscillations. STNOs are nanoscale devices that can be integrated in IC's. Relatively to normal oscillators STNO's exhibit stronger non linear properties which result, on one hand, their large frequency tunability. On the other hand, in a large spectrum linewidth, due to phase noise created by a nonlinear phase-amplitude dependence.

Progress has been made on these devices increasing the emission power, reducing the phase noise and eliminating the dependence on an external applied field [7–11].

1.2 Motivation

Spin torque nano oscillators (STNOs) exhibit a set of features that make them very attractive:

- low power consumption
- high frequency range (0.1 MHz–1 Ghz with vortex STNOs; 1–10 GHz with homogeneous STNOs; <10 GHz with nano-contact STNOs)

- high dynamic range, capable of quickly changing the operation frequency with short transient response.
- compatible with CMOS technology, allowing them to be integrated in ICs.

1.3 Objectives

The objective of this thesis is to produce and characterize an electric circuit based on lumped components that uses a spin torque vortex oscillator (STVO) to implement an RF transmitter and a second circuit based on an identical STVO to implement a receiver. These circuits should make use of the STVO to modulate and demodulate the RF signals. The electrical circuit should be designed to enhance the unconventional characteristics of the nano-oscillator in order to gain advantages over conventional modulator / demodulator circuits. It is intended to demonstrate that such nano-devices can have advantages over conventional circuits, such as its ability to be reconfigured. The same device / circuit can be used as a modulator or demodulator. These circuits should make the implemented systems compatible with real world applications.

In order to solve this problem a system using FSK will be developed. Both a transmitter and a receiver will be implemented based on the schematics from figures 2.10a and 2.11 respectively. The STVOs are integrated on a silicon die which will be wire bond to a PCB.

1.4 Document Structure

In this chapter, the context, motivation and objectives for this thesis was discussed.

Chapter 2 provides a theoretical background on the physical principles responsible for the operation of STNOs and STVOs. This chapter ends with a brief characterization of the STVOs provided by INL, as well as, an overview of the state of the art of RF systems based on STVOs.

Chapter 3 starts by implementing a simple electrical model that captures the functional characteristics of existing oscillators and characterized in the laboratory. This step is followed by the design and implementation of a PCB capable of carrying and providing electrical contact with the nano-oscillators provided, as well as, the design and simulation of a system capable of modulating/demodulating them based on a TCP/IP connection.

The assembly, characterization and improvements of the system developed in chapter 3 is discussed in chapter 4. This chapter also provides the results obtained by modulating/demodulating the STVOs with the developed system.

Finally, chapter 5 presents the conclusions obtained from the developed work, as well as, a discussion on possible future work.

Chapter 2

Background

This chapter is dedicated to a simplified analysis of the physics responsible for spin transfer nano oscillators. Spin transfer nano-oscillators are devices capable of producing a RF/microwave electric signal from a DC input current. These devices are based on two spintronic physical phenomena present in magnetic multilayers: spin transfer effect and magnetoresistive effect.

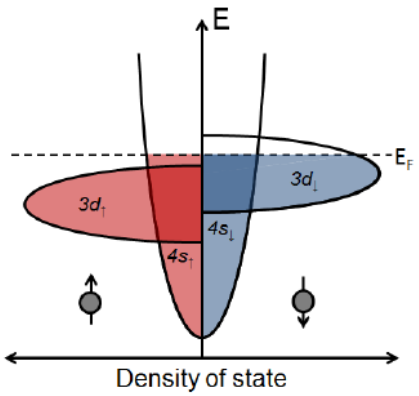
2.1 Introduction

2.1.1 Ferromagnetism

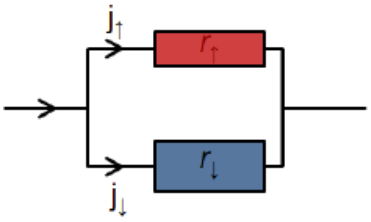
Electrons beside charge also have a fundamental property designated by spin. The spin of the electron is one of the causes of its magnetic dipole moment. From a point of view of classic electrodynamics, a rotating electron (charged particle) produces a magnetic dipole, making the electron behave like a small magnet. Due to Pauli's exclusion principle and Hund's rules only atoms with partially filled shells can have a net magnetic moment. A macroscopic field is created when there is a tendency for the spins of a large number of electrons to align themselves, for example in an external magnetic field. (paramagnetism). Some materials have a natural tendency to become magnetized, which means that they have a more stable configuration when the unpaired valence electrons along the material are aligned with the same spin. These are called ferromagnetic materials. (ex Co,Fe,Ni)

2.1.2 Electronic transport in ferromagnets

Figure 2.1a shows the band shells 3d and 4s at the Fermi level, on a ferromagnetic transition metal. It is shown that the 3d shell is not fully filled and that there is a discrepancy in the energy levels between spin up and spin down. The exchange interaction determines whether the spins are aligned parallel or anti-parallel, being the difference in energy between the two states designated exchange energy. In a ferromagnetic the less energetic state is aligning the electrons in one preferential direction. This leads to a splitting of the conduction electron bands in two channels with different density of states which lead to different resistivities according to their spins, as seen in figure 2.1b.



(a)



(b)

Figure 2.1: a) Bandshell structure of a soft ferromagnet transition metal with E_F the Fermi level. b) Equivalent circuit in the two current model – from [8].

The reference axis for the spins is the magnetization vector of the material, so, a electron current in a transition metal ferromagnets are therefore spin polarized along this axis.

2.1.3 Macro-spin theory

Assuming that the magnetization in a given layer is uniform it can be described by a continuous field $M = M_S\hat{m}(r)$, where m is the magnetization direction vector with a constant norm equal to 1 and M_s is the saturation magnetization of the material, then the time evolution of the magnetization vector is described by the torque equation:

$$\frac{\mathrm{d}\hat{\mathbf{m}}}{\mathrm{d}t} = -\gamma_0\hat{\mathbf{m}} \times \mathbf{H}_{\text{eff}} + \sum_i \mathbf{T}_{i,\text{NC}} \tag{2.1}$$

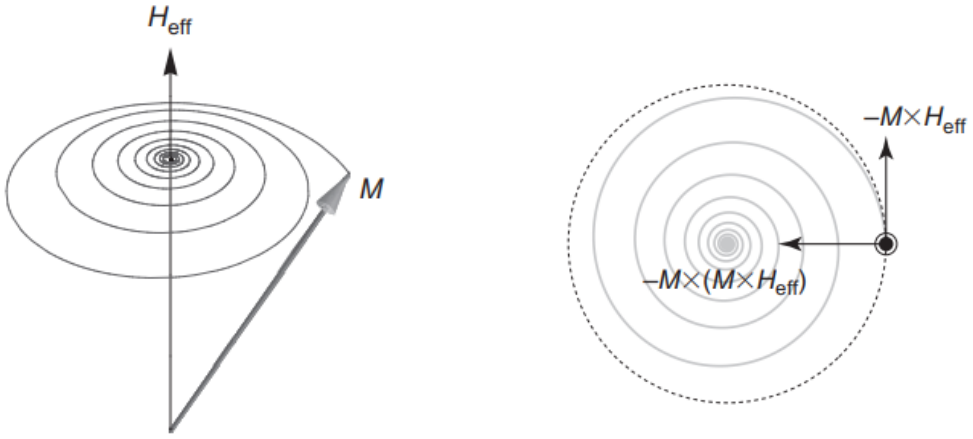
where γ_0 is the gyromagnetic constant. The first term describes magnetization precession around the effective field H_{eff},

$$\mathbf{H}_{\text{eff}}(\mathbf{r}) = -\frac{1}{\mu_0}\frac{\partial \mathscr{E}(\mathbf{r})}{\partial \mathbf{M}(\mathbf{r})} \tag{2.2}$$

where ε is the magnetic energy.

The main contributions to the magnetic energy are the Zeeman, exchange and dipole-dipole interaction. The Zeeman term describes the interaction of the magnetization with an external applied magnetic field.It includes the magnetic field generated by a current passing through the layer. The exchange term was discussed before and it is responsible for the spontaneous magnetization. The dipole-dipole interaction couples all the local moments in a system. This term dictates all the possible stable magnetization states.

The second term represent all the non conservative torques applied. Due to dissipative processes Gilbert propose damping term. This term is one of the non conservative torques from



(a) (b)

Figure 2.2: (a) Damped spiraling trajectory of the magnetization M about its effective field Heff. (b) Top view of the dynamics, with the directions of the precessional and damping torques drawn. – obtained from [12].

equation 2.1 and can be expressed by:

$$\mathbf{T}_{\mathrm{G}} = \alpha \hat{\mathbf{m}} \times \frac{\mathrm{d}\hat{\mathbf{m}}}{\mathrm{d}t} \tag{2.3}$$

where α is a damping constant. This term represents the equivalent of friction in a mechanical system. Using both term discussed before it is possible to derive [12]:

$$\frac{\mathrm{d}\hat{\mathbf{m}}}{\mathrm{d}t} = -\frac{\gamma_0}{1+\alpha^2}\hat{\mathbf{m}} \times \mathbf{H}_{\mathrm{eff}} - \frac{\alpha\gamma_0}{1+\alpha^2}\hat{\mathbf{m}} \times (\hat{\mathbf{m}} \times \mathbf{H}_{\mathrm{eff}}) \tag{2.4}$$

The second term viewed in this manner is the equivalent to term proposed by Landau and Lifshitz.

Figure 2.2 shows a system with both the precession term and the damping term from the torque equation. The magnetization vector of a system only containing the precession term with and a magnetization vector not aligned with H_{eff} would move around in a circle. It should be noted that H_{eff} depends on M, which leads to the nonlinearity of the equation of motion.

2.1.4 Spin transfer torque

Another non - conservative torque to take in consideration is the spin transfer torque. Spin transfer was first discover in 1996 by Slonczewski [2] and Berger [13]. Figure 2.3 demonstrates how torques are applied to the free layer. When a current passes through a ferromagnetic layer, as discussed in 2.1.2, it becomes spin polarized along its magnetization $\overrightarrow{M_1}$. If this current reaches another ferromagnetic layer, FM_B, that has a magnetization non colinear to $\overrightarrow{M_1}$ then the electron spin axis will change to $\overrightarrow{M_2}$ leading to a transfer of spin magnetic moment, causing a torque. This phenomenon occurs at the interface of FM_B over its first atomic layers. In this configuration the

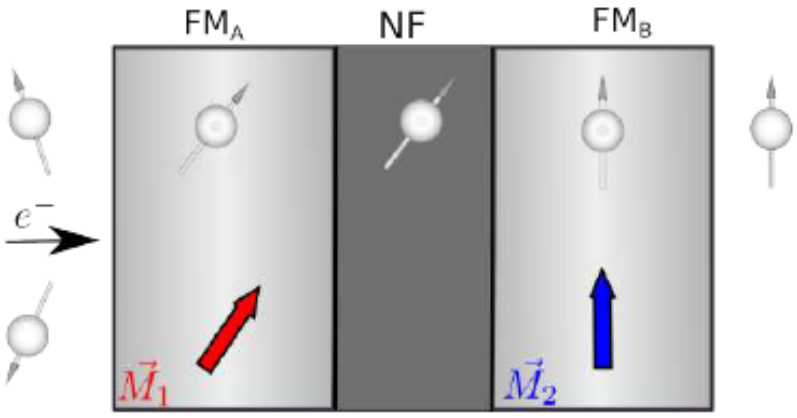


Figure 2.3: Spin transfer torque in a spin valve, from [7].

torque can be described by:

$$T_s = \tau_S[\overrightarrow{M_2} \times (\overrightarrow{M_2} \times p)] \tag{2.5}$$

It should be noted that the sign of the current changes the sign of the torque. If the second layer is thin enough so that the spin torque transfer has the ability to change its magnetization, than it is considered a free layer. By adding this term to torque equation it is easy to see that it can either increase the damping term or subtract from it, as seen in figure 2.4. If the current is large enough it can compensate the damping leading the magnetization vector to a state of self oscillation.

2.1.5 Landau-Lifshitz-Gilbert-Slonczewski equation

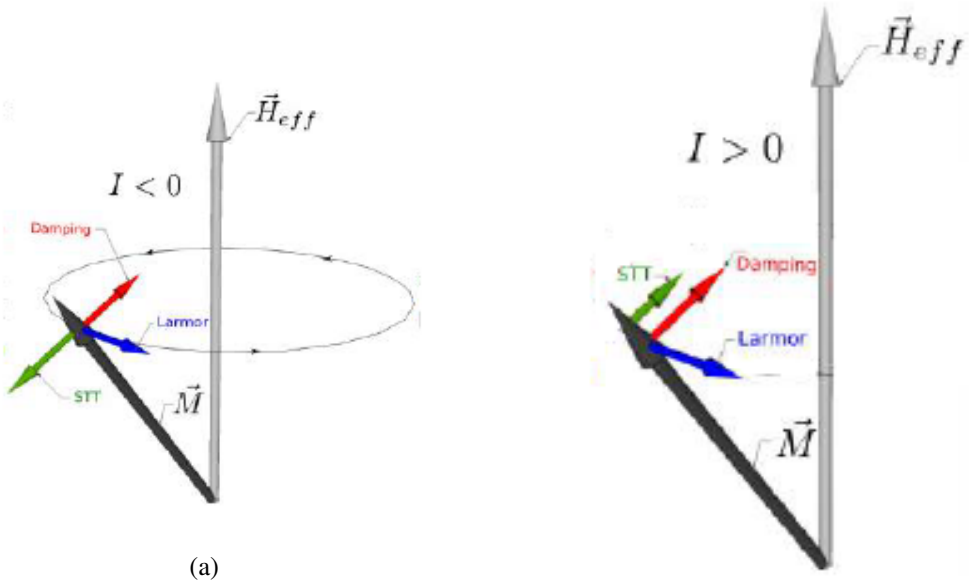
A more detailed version of the torque equation 2.1 that describes the evolution of the local magnetization is known as the Landau-Lifshitz-Gilbert-Slonczewski equation :

$$\frac{d\overrightarrow{m_2}}{dt} = -\gamma\overrightarrow{m_2} \times \vec{H}_{eff} + \alpha\overrightarrow{m_2} \times \frac{d\overrightarrow{m_2}}{dt} + \tau_{Slonc}\overrightarrow{m_2} \times (\overrightarrow{m_2} \times \vec{p}) + \tau_{FL}\overrightarrow{m_2} \times \vec{p} \tag{2.6}$$

The first term is the conservative precession around H_{eff}, the second term is the Gilbert damping torque, the third term is the the Slonczewski spin transfer torque and the last term is the field-like torque. The filed-like torque was neglected for simplicity. This torque is perpendicular to the damping torque, and it has the same effect as an applied magnetic field.

2.1.6 Magnetoresistance

Magnetoresistance transforms the magnetization oscillations in electric resistance oscillations. In multilayered devices such as spin valves and MTJ the angle between the magnetization of the two ferromagnetic layers will influence the resistance. The magnetoresistance is caused by different effects in spin valves and MTJs. These effects are giant magnetic resistance (GMR) and Tunnel magnetoresistance (TMR) respectively. Since the device used in this thesis uses a MTJ the effect



(a) (b)

Figure 2.4: Terms of the torque equation. The larmor term represents the conservative precession in the torque equation - (a) The spin transfer torque is opposite to the damping, leading to self sustained oscillation (both the magnitude and frequency change with I). (b) The spin transfer torque is in line with the damping, increasing the damping – reprinted from [7].

is TMR. Article [8] presents a more detailed explanation on TMR and also shows a simplified model of magnetoresistance in multilayered systems.

2.1.7 Overview

A simple spintronic device is composed by three layers: two ferromagnet layers (one designated by fixed or pinned layer and the other by free layer) separated by non ferromagnetic layer. This

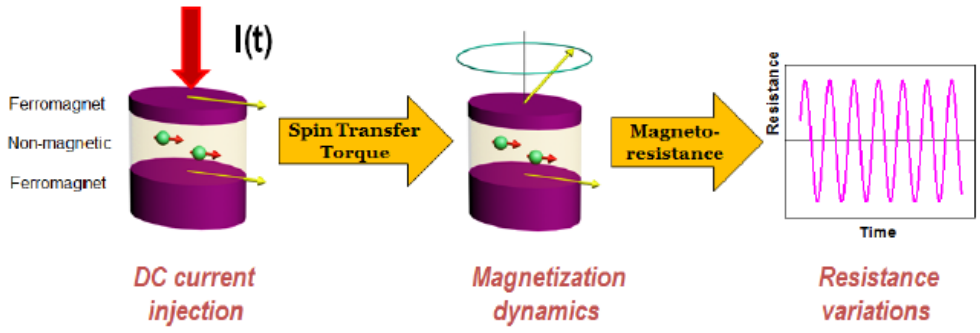


Figure 2.5: Principle of a spin-torque oscillator. Reprinted from [8].

devices can be considered either spin valves or magnetic tunnel junctions based on the non magnetic layer. If this layer is conductive then it is a spin valve. If the layer is non conductive but allow tunneling from the electrons the it is a MTJ. The pinned layer is thicker and its magnetization is constant so that it acts as a spin polarizer. The free layer is thinner and its magnetization is free to move. The non magnetic barrier has to be thin enough that the spin induced by the fixed layer is not altered until the electrons reach the free layer. Under certain conditions (i.e. external field and the magnetization orientation of the layer), an electrical current can cause a self sustained oscillation in the magnetisation of the free layer, which, due to magnetoresistance, leads to a resistance oscillation, as seen in 2.5. Under an constant current the voltage will also oscillate. An RF signal can be created through a bypass capacitor.

2.1.8 RF emission/detection

Since the conservative term of the torque equation depends on H_{eff} which depends on all external magnetic fields, it is possible to change frequencies either by changing an external magnetic field or by changing injected the current changing the oersted field. Article [14] shows a transmitter based on a STNO. It is also possible to detect rf signals with the STNOs discussed in this section, since they can work as spin diodes. Article [15] simulates a spectrum analyser based on a STNO with a MTJ for microwave detection. This detection scheme is based on phase locking the microwave current with the STNO precession. Mixing the resistance with the RF/microwave current leads to an extra DC voltage term. The STNO natural frequency is changed with a ramped DC current. They achieved a 10GHz bandwidth with a frequency scanning rate exceeding $100\,\mathrm{MHz/ns}$ and a sensitivity of $1\,\mathrm{nW}$ at a scanning rate of $10\,\mathrm{MHz/ns}$. Article [16] shows another detector with a sensitivity of $12{,}000\,\mathrm{V/W}$, which exceeds semiconductor Schottky diode detectors.

2.2 Spin Transfer Vortex Oscillators

The STNO used in this thesis is a Spin Transfer Vortex Oscillator based on a MTJ nanopilar. A nanopilar is a cylinder (i.e. a $500\,\mathrm{nm}$ diameter cylinder) that includes some layers of the device. A vortex is a micromagnetic structure in which the magnetization of a layer curls culminating on a out of plane magnetization in the middle, known as core, as seen in figure 2.6a. Figure 2.6b shows the polarity and chirality of the core. The curl can be either clock wise or counter clock wise defining the chirality. The core magnetization is perpendicular to the plane. The polarity defines its orientation. In a nanopilar the vortex configuration is favourable under certain conditions minimizing the stray fields at the edges [17]. The macro spin approach is not applicable to the vortex state since the layer magnetization is not uniform. One can use micromagnetic simulations (i.e. solving the LLGS) to find the magnetization in each point of the layer. An analytic alternative is described in [18]. Tunnel magnetoresistance and spin transfer torque are still the effects responsible for RF/DC and DC/RF conversion.

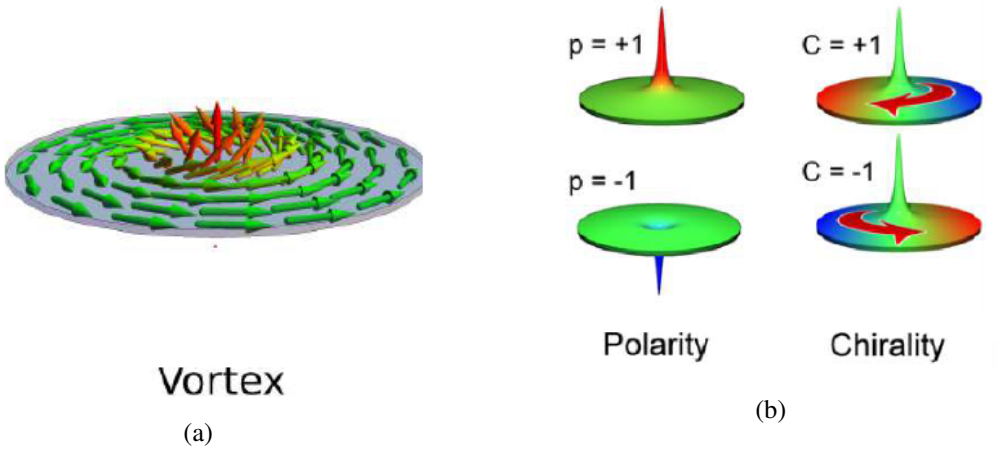


Figure 2.6: Reprinted from [7]-(a) Vortex state. (b) Polarity and chirality of the vortice.

2.2.1 In plane magnetic field

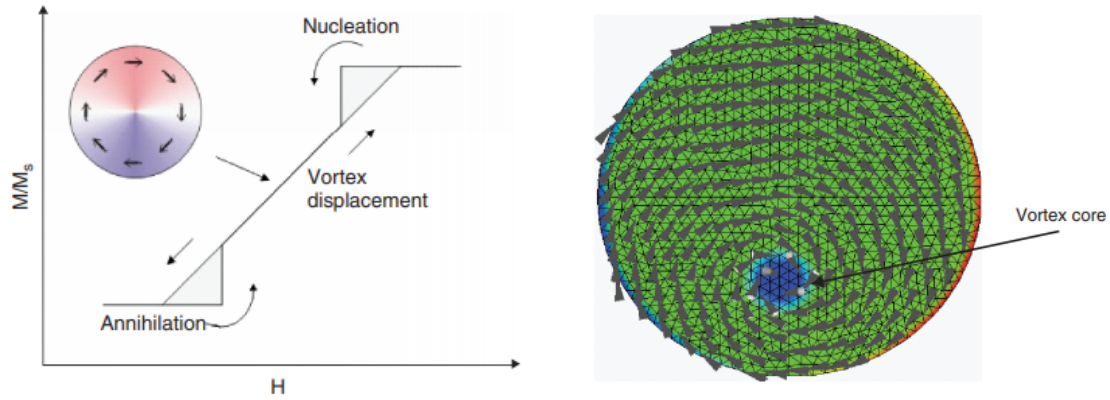
Figure 2.6a represents a vortex centered with the layer. This configuration as a null in plane net magnetization. By applying an in plane magnetic field the vortex core moves so that the net in plane magnetization is aligned with the external field. The core moves in a perpendicular direction with respect to the applied magnetic field. This can be seen in figure 2.7b. When a strong enough magnetic field is applied the vortex core moves out of the layer (it is annihilated) forming a quasi uniform magnetization. This is a hysteretic process. For a positive magnetic field the nucleation of the core requires a lower magnetic field than the annihilation, as seen in figure 2.7a.

2.2.2 Vortex Dynamics

In STVOs, typically the only excited mode observed is the gyrotropic mode. The Thiele model [19] can be used to describe this mode in the linear regime as the translation of the vortex core in a confined parabolic potential [20]. When this mode is excited it will lead to an oscillatory movement around the equilibrium point of the core . Two possible ways to excite this mode are with spin transfer torque (i.e. with a DC spin polarized current) and changing the equilibrium point (i.e. with an in plane magnetic field as seen in 2.2.1). Under spin transfer torque a self sustained oscillatory regime around the equilibrium point can be achieved as seen in figure 2.9 by the red line. If the equilibrium point changes without any other stimulus than the core will spiral until its new equilibrium point. Without any external excitation the core will spiral until its original equilibrium point.

$$\vec{G} \times \dot{\vec{X}} - \frac{\partial E}{\partial \vec{X}} - D(\vec{X})\dot{\vec{X}} + \vec{F}_{STT}(\vec{X}) = \overrightarrow{0} \tag{2.7}$$

The first term is a force perpendicular to the velocity, since the gyroforce vector $\vec{G} = -2\pi PL\frac{M_s}{\gamma}\overrightarrow{e_z} = -PG\overrightarrow{e_z}$. The second term is the confinement force and it is the gradient of the potential energy



(a) (b)

Figure 2.7: Reprinted from [17]-(a) Hysteretic diagram of the magnetization due to an in plane magnetic field. (b) Top view of an off centered vortex core due to an in plane magnetic field.

(magnetostatic and zeeman). The third term is the damping force and the last term is the spin tranfer torque force. A diagram of the forces is represented in 2.9. The time evolution of the core position, excited by magnetic fields, solved by the Thiele model can be seen in figure 2.8.

The Thiele model cannot fully describe the dynamics of a vortex core in a nanopillar. However it can be used to get some insight on the general behaviour of a vortex and demonstrate how spin transfer torque can lead to self sustained magnetization oscillations. A more accurate analytic model is described in [18]. This article also shows the frequency dependence on the current density through the MTJ, which allows for frequency modulation.

The net magnetization of the layer containing the vortex changes with the core position, as it can be easily seen by comparing figure 2.7b with figure 2.6a. A MTJ containing a vortex in its free layer and a uniformly polarized fixed layer will thus exhibit magnetoresistance, since the difference in magnetization from the two ferromagnetic layers is dependent on the core position.

2.2.3 Emitted Power

One of the advantages of the MTJ over a spin valve is a much larger relative change in resistance:

$$\mathrm{MR_r} = \frac{R_{\mathrm{ap}} - R_{\mathrm{p}}}{R_{\mathrm{p}}} \tag{2.8}$$

where R_{ap} is the resistance in the anti-parallel state (FM layers polarized in opposite direction) and R_{p} is the resistance in the parallel state (FM layers polarized in same direction). The greater this ratio the larger the resistance oscillations can be which results in a greater emitted power.

According to [18] the power emitted by a STNO is given by:

$$P = \left(\frac{I_{dc}\Delta R_{\mathrm{osc}}}{R_s + Z_0}\right)^2 Z_0 \tag{2.9}$$

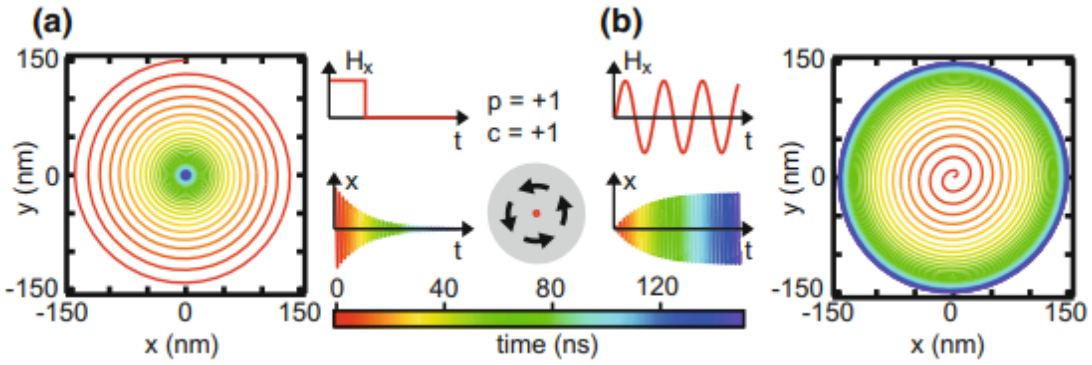


Figure 2.8: (a) Trajectory of the vortex core back to its equilibrium position with the frequency of the gyrotropic mode after it has been deflected with a magnetic field that is then switched off instantaneously. (b) The vortex core is resonantly excited with an alternating magnetic field near the frequency of the gyrotropic mode. It performs a transient motion until it reaches circular trajectories in the stationary case. Reprinted from [20].

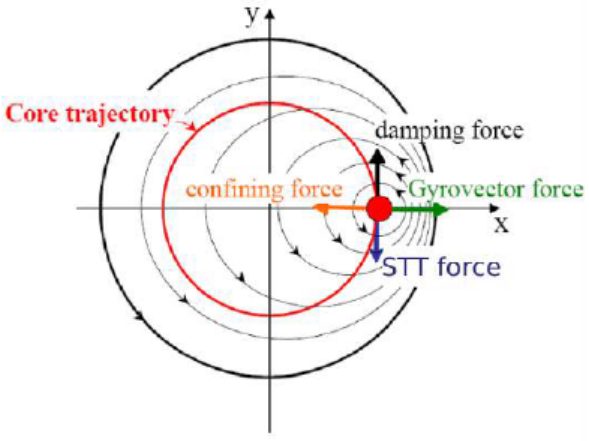


Figure 2.9: Forces acting on the vortex core. Reprinted from [8].

where R_s is the sample resistance, ΔR_{osc} is the amplitude off the resistance oscillation and Z_0 is the load resistance. For a MTJ with $R_s = 50\Omega$, $\Delta R_{\text{osc}} = 0.5R_s$, with $I_{dc} = 500\mu A$ and $Z_0 = 50\Omega$ the emitted power is -31dBm.

The output voltage amplitude also depends on its frequency. Increasing the oscillation amplitude with an increase in I_{dc} would lead to a change in frequency.

2.2.4 STVO in use

The STVOs will be provided by INL. There is the possibility to work with three different versions of STVOs. The first two versions mainly for testing and to obtain preliminary results. This version requires an external magnetic field, achievable with a permanent magnet. In this version the MTJ resistance is expected to be 25 ohms and the peak power emitted -34dBm. The third version consists off better performing devices. This version is capable off exhibiting oscillations without the need for an external magnetic field. It is capable of producing a peak power of -30dBm and its expected resistance is 50 ohm. As off this moment there is not an accurate explanation for the oscillations at zero field in this STVO. Article [11] shows another STVO capable of operating at zero field based on a similar MTJ combined with and out of plane polarized spin valve.

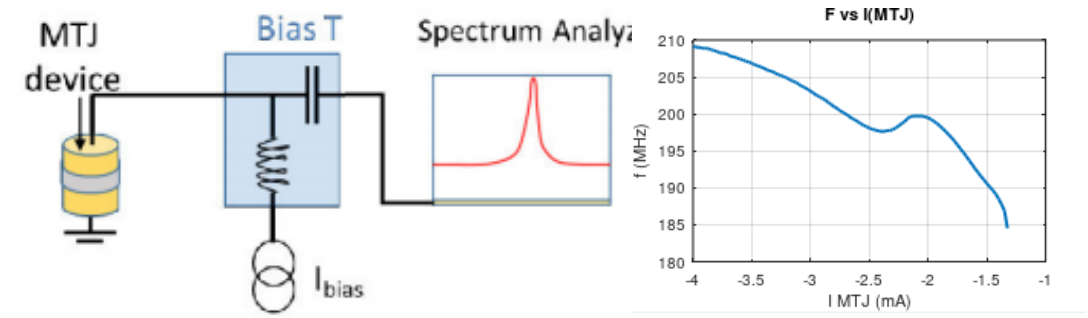
Both versions consist of a MTJ in a nanopillar. The fixed layer is uniformly in plane polarized and the free layer has a vortex. The STVO has an field line antenna which is a wire placed above the MTJ. A current in this wire will induce an Oersted-Ampère field that will intersect the MTJ and act as an in-plane magnetic field. The expected resistance for this line is 20 ohm. Spin transfer vortex oscillators operate from several hundred MHz up to 1GHz. Both STVOs will operate between 200–300MHz. The detection method used is able to detect a power of 4dBm. It should be noted that the MTJ maximum voltage is close to 1V for the second version (version 2) and 0.5V for the first (1,1.2). It should be avoided working close to this limit since it can permanently damage the non magnetic layer.

2.3 RF System

In this section it will be presented the RF communication system as well as a comparison to some of the state of the art methods used. A simple communication system requires a receiver and a transmitter. In this case two equal STVOs will be used to accomplish that, which shows the versatility of these devices. The DC component of the resistance can be controlled in the fabrication process (i.e. changing the nanopilar diameter).

2.3.1 Modulation

One important parameter is the maximum modulation bandwidth which defines the maximum achievable rate at which an STNO can be modulated by a signal. A known limit to this rate is the amplitude relaxation rate which occurs for current modulated signals. This is due to the amplitude-frequency dependence of STNOs. In the case of vortex oscillators a frequency change imposed by



(a) (b)

Figure 2.10: Reprinted from [17]-(a) Diagram of a transmitter adapted from [10] (b) Frequency vs I applied to the MTJ from a similar device.

a change in current will occur when the core radius of rotation changes. This process is dependent on the damping constant of the material. For vortex oscillators modulated by a square wave this rate is on the order of a few Mcycles/s, as seen in [21], which uses another STVO from INL. [22] proposes an improvement by modulating the signal via a magnetic field. Although the STVOs in use can create a magnetic field using their field line antenna this will be seen as an possible improvement and not as a starting point.

The most common protocols in STNOs are ASK [23] and FSK. More recently a phase modulation method was implemented [21]. Due to the frequency-amplitude relation ASK is based on on-off keying (OOK). In this case FSK is a clear improvement on ASK since it can be seen as multiple ASK channels in parallel. The PSK method implemented in [21] achieved a 4Mbit/s bit rate with a STVO operating at 300MHz. This method will not be used since it requires an external ac source or a PLL to synchronize the STNO. It would also require coherent demodulation which would not be viable.

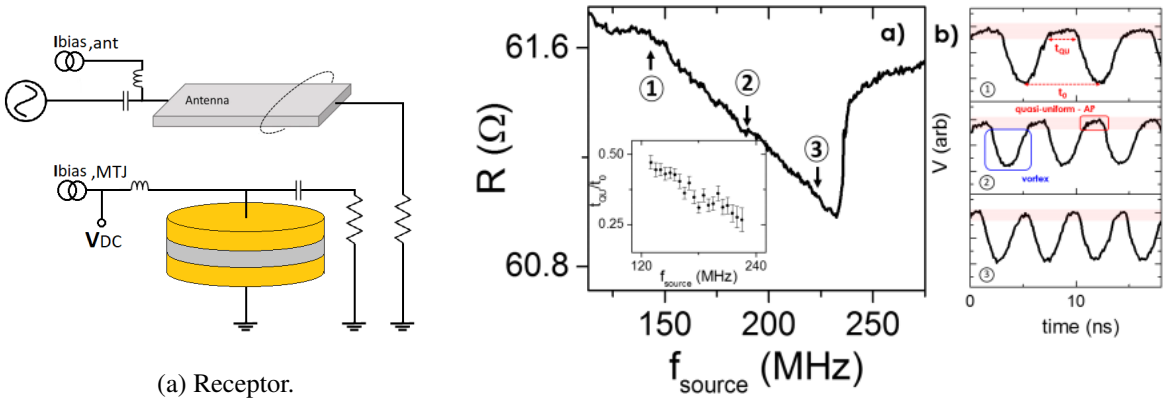
2.3.2 Transmission system

For a FSK system the STVO operating as the transmitter will be connected via a bias T to a signal generator to change the bias current as seen in figure 2.10. An appropriate bias T should be chosen or implemented so that it will not affect the maximum modulation bandwidth.

2.3.3 Receiver system

There are two main different types of RF detectors based on STVOs. According to [24] these are frequency detectors and frequency sensors.

Frequency detectors, as the name indicates, are intended to detect a single frequency. They are designed to detect small bandwidths, which defines their frequency resolution. These detectors can be based on spin-diodes (seen in section 2.1.8) or on resonant expulsion of the vortex core [25]. [25] also performs a comparison between these two types of detectors, showing that spin diodes have a higher frequency resolution (smaller bandwidth) but their maximum output voltage



(a) Receptor.

(b) Frequency sensor - reprinted from [24].

Figure 2.11: Receptor circuit and detected signal based on a STVO.

decreases with the input power. On the other hand the method using resonant core expulsion has a constant and higher output voltage since the RF signal only acts as the excitation that leads to the core expulsion but the average resistance from the time spent in the vortex state and quasi uniform state is constant. The DC output voltage is given by the product between the polarizing DC current and the average resistance. Which also leads to a higher voltage. They achieved a effective sensitivity of 40,000 V/W. In both detectors the RF signal is applied to the MTJ which results in a higher sensitivity (minimum input power). For the detector based on resonant core expulsion a sensitivity of -43 dBm was achieved.

Frequency sensors are design to operate on a larger bandwidth as seen in figure 2.11. One sensor is analyzed in [24]. They also operate by resonant core expulsion although in this case the RF signal is applied in the field line antenna. The antenna will produce a magnetic filed that will act as a in plane magnetic field on the MTJ. Figure 2.8(b) shows how an ac in-plane magnetic field close to the gyrotropic mode resonant frequency can influence the core position. Figure 2.11b shows, for a specific antenna and MTJ bias points how the resistance $V_{DC}/I_{bias,MTJ}$ varies with frequency. This occurs because the inductance from the bias T acts as a filter averaging the time dependent resistance associated with the core movement, annihilation and re-nucleation. A linear relation between resistance and frequency is ideal for a FSK demodulation system since it will create a linear relation between the output voltage V_{DC} and input RF frequency. This system requires a much higher RF power since it needs to create a significant magnetic field, on the other hand allows for a single device operating as a FSK demodulator.

For both type of systems the bias Ts have to be carefully dimensioned/ chosen. If the inductance is to low then the average resistance will be incorrect. If the inductance is to high the demodulator will be slow.

In this thesis it will be used a sensor type system.

Chapter 3

Design and simulation of the communication system

The purpose of this chapter is to develop a system capable of interacting with the provided oscillators, thus creating a transmitter and a receiver system based on FSK.

3.1 STVO Electrical model

The first step for developing a communication system based on STVOs is to obtain a working electrical model of the oscillators provided. This first step was not possible due to the limited access to the laboratory at the time. The alternative found was to base the model on previously obtained data from similar STVOs, also made at INL.

As seen in section 2.2.4 some of the basic characteristics of these oscillators are presented in table 3.1. It should be noted that both version 1 and 1.2 require and external magnet to work as an oscillator / sensor and that the magnet position greatly impacts the performance.

3.1.1 Transmitter

The relation between current applied to a MTJ from a STVO, version 2 from table 3.1, and output frequency can be seen in figure 2.10b. This figure shows a 25 MHz shift in frequency over a span of ∼2.5 mA. In section 2.3.1 the amplitude relaxation rate was discussed. This leads to a limit in maximum modulation rate via the MTJ of the STVO. One way to test this parameter would be to apply several current steps with different amplitudes to a MTJ and capture the time domain signal.

Table 3.1: Some characteristics from three versions of STVOs.

Version	MTJ resistance	FL resistance	Peak power	Frequency	Max voltage
1	25 Ω	20 Ω	-34 dBm	200-300MHz	0.5 V
1.2	40 Ω	20 Ω	-30 dBm	200-300MHz	0.5 V
2	50 Ω	20 Ω	-30 dBm	150-300MHz	1 V

Table 3.2: Characteristics for a modulating current source.

	voltage range @50 Ω	voltage range @25 Ω	modulation (square wave)	resolution
current source MTJ	+1 V	+0.5 V	>few Mcycles/s	>1 mA

The resolution should be as large as possible to reduce the space between adjacent FSK frequencies, figure2.10b.

A spectrogram would show the shift in frequency over time. In this case, instead of using real time data, data from a simulation was provided by INL. The spectrogram of the magnetization is shown in figure 3.2a. The different steps applied are used to verify if the shift in frequency is amplitude dependent. Although the data from this figure is not very conclusive, it is possible to see a shift in frequency. It is also possible to see that the shift in frequency, for the step used, occurs over a fraction of a μs. This is in accordance with the limit in modulation rate to a few Mcycle/s previously discussed. Table 3.2 shows some characteristics that would help to create a current source capable of modulating the oscillator via the MTJ. The selected voltage range covers the whole region in which the STVOs from table 3.1 can safely operate. The modulation rate capacity should be above the limit imposed by the amplitude relaxation rate. Finally, the current source resolution should be high enough that multiple output frequencies can be detected. From the 25 MHz shift in frequency over a span of ∼2.5 mA discussed above, one can conclude that the current source should have a resolution, ideally, much greater than 1 mA. The higher the resolution the smaller the minimum output current step.

A simple electrical model for a STVO, for a single frequency, can be made with ADS, using a time dependent resistor such as the one present in figure 3.1. This model creates a 50 Ω resistor in series with a resistor that oscillates with an amplitude of 2 Ω at 250MHz. This figure also shows the effects of applying a 8 mA current to such a device.

3.1.2 Receiver

Figure 2.11b, 3.2b and article [24] show data from an oscillator similar to version 2 from table 3.1 working as a sensor, excited by modulating frequencies similar to the gyrotropic mode of the sensor. To achieve a curve like the one in figure 2.11b.a) it is necessary to filter 2.11b.b) with a low pass filter. In this article they were able to achieve a maximum resolution of 250 kHz with a separation of 0.12 mV between adjacent levels.

The receiver needs to have two current sources to establish the DC bias point of both the MTJ and the FL (field line antenna), as seen in 2.11a. Table 3.3 shows some basic characteristics for these sources. In this case a specific electrical model would be difficult to achieve since the particular curves seen in figure 2.11b are both device dependent and bias dependent. Moreover for the version 1/1.2 from table 3.1 the position of the external magnet will also greatly affect this curve. The plan to overcome this problem is to characterize a specific oscillator (working as a sensor) before its use under a stable environment.

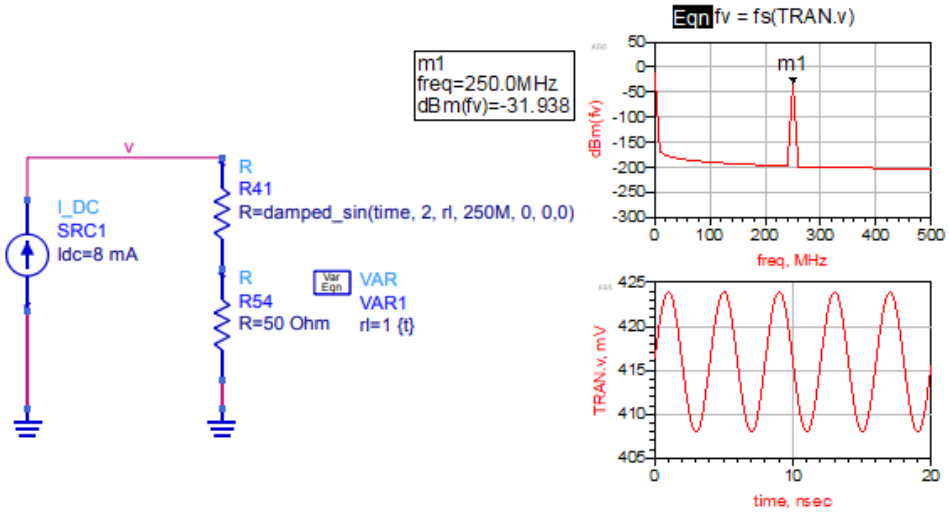
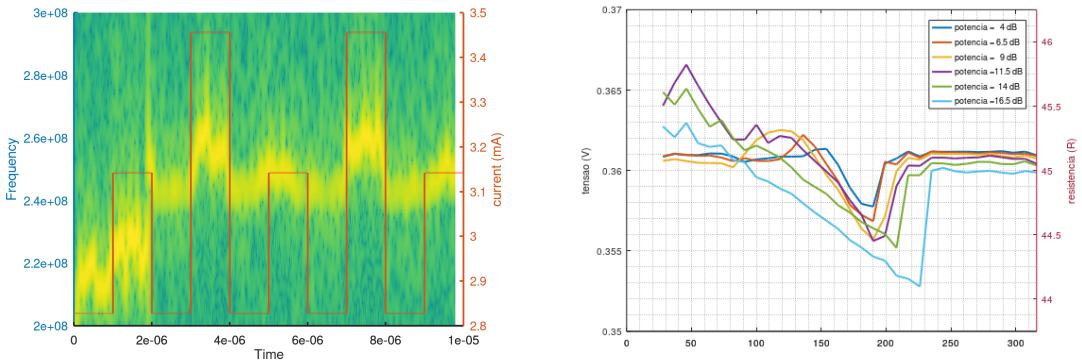


Figure 3.1: ADS model of a transmitter for a single frequency.



(a) (b)

Figure 3.2: (a) Spectrogram of the magnetization obtained from the simulation of a STVO vs current. (b) Frequency sensor: Resistance and voltage vs frequency for different input powers applied to the field line ($I_{MTJ} = 8\,\text{mA}$ $I_{FL} = 40\,\text{mA}$).

Table 3.3: Characteristics for the receiver current sources.

	voltage range @50 Ω	voltage range @25 Ω	modulation rate	resolution
current source MTJ	+1 V	+0.5 V	$\sim DC$	>1 mA
	current range	voltage range @ 20 Ω		
current source FL	±50 mA	±1 V	$\sim DC$	>1 mA

The resolution should be as large as possible to reduce noise in the DC bias point

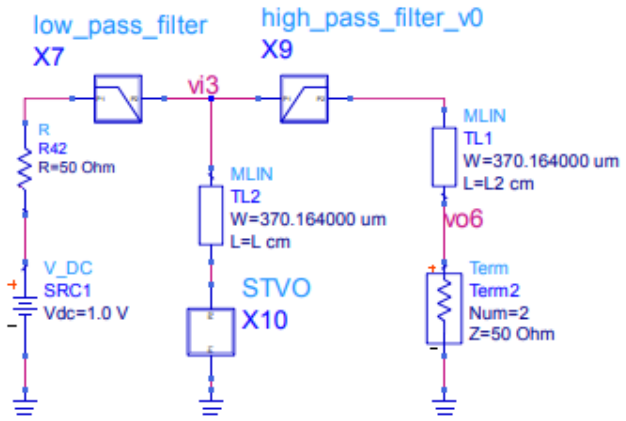


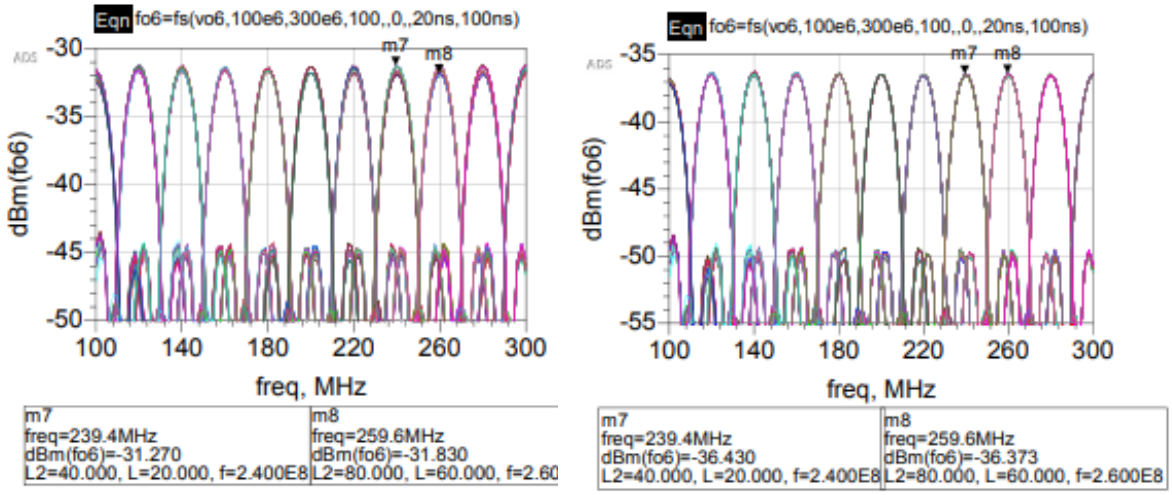
Figure 3.3: Equivalent circuit modeling a transmitter based on a STVO.

3.2 Interacting with the STVOs

The STVOs are integrated in a die. Each one can be interfaced by two connections, its MTJ (magnetic tunnel junction) and its FL (field line). For practicality it is necessary to wire bond several oscillators to a carrier, either a chip or a PCB. It is also convenient to be able to safely separate the oscillators from the communication system, as it is also necessary to test them in the laboratory.

Using figure 2.10a as a reference one could interpret the circuit as the circuit represent in figure 3.3, where the STVO is the model represented in figure 3.1, the low pass filter and high pass filter are, respectively, the inductance and capacitance from the bias T, V_{DC} is a source capable of modulating and establishing the MTJ bias point, $TL_{1,2}$ are transmission lines and Term2 is a 50 Ω load such as a RF amplifier or the input impedance of an instrument. Assuming 50 Ω transmission lines (TL), this circuit is not very sensitive to L2 (length of the TL between output of the bias T and the load (TL1)) neither to L (length of TL2), provided that the filters are intended to operate with 50 Ω TLs. This independence from the length of the TLs applies for both versions of STVOs (25 Ω,50 Ω) and can be seen in figures 3.4a and 3.4b, where a sweep of both lengths and the frequency of the resistor oscillation (according to the model of the STVO referenced above) was performed in the time domain followed by an fft. It should be noted that the difference between the peak values from oscillators with 25 Ω and 50 Ω presented is due to the decrease in current applied when the impedance increases.

Having these results in mind a simple and flexible system to bond the oscillators would be an external PCB matched to 50 Ω which could be connected via SMA connectors and coaxial cables. A diagram for this PCB can be seen in figure 3.5a and the die in figure 3.5b. The final product is presented in figure 3.6. The transmission lines are (CPWG) Coplanar Waveguides with Ground with 50 Ω characteristic impedance.



(a) (b)

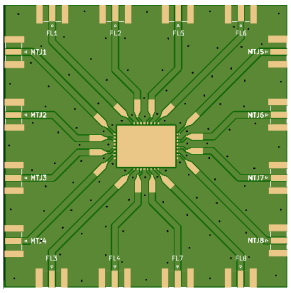
Figure 3.4: Nested sweep of length L and L2 from Transmission lines TL2 and TL1 and frequency from the STVO. The STVO model contains a fixed load + a oscillating resistance with an amplitude of 2 Ω (a) Analysis for STVO with 25 Ω: nested sweep 1)STVO frequency (100 MHz-300 MHz), 2)L(0-100cm),3)L2(0-100cm) (b)Analysis for STVO with 50 Ω: nested sweep 1)STVO frequency (100 MHz-300 MHz), 2)L(0-100cm),3)L2(0-100cm)
Note: - the difference in the peak value from (a) to (b) comes from the change in DC current.
- In both figures the smaller peaks are side bands.

3.3 Overall communication system

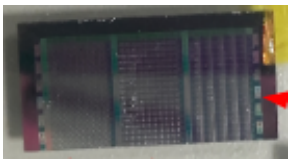
The next step is to figure out a way of controlling the oscillators both for the transmission and reception of signals. This can be done, for example, by adapting a SDR (Software Defined Radio). In a SDR a computer can control an RF system by using a FPGA as an interface connecting the computer to a DAC and a ADC. Figure 3.7 shows a way of controlling implemented dedicated hardware with a computer, while figure 3.8 shows the dedicated hardware necessary and its interaction with the STVOs.

In order to choose a DAC and an ADC for the system, some parameters should be defined. Table 3.2 indicates that the maximum frequency for a square wave that can be used to modulate the MTJ is in the order of Mcycles/s. Maximizing it to 10Mcycles/s a DAC with a settling time close to $\frac{1}{10}\frac{1}{10Mcycles/s} = 10ns$ would be sufficient. If the DAC is intended to be used across the whole voltage range shown in table 3.1 then a resolution of 12 bits would be enough as it corresponds to a resolution of 100 divisions per mA for a 25 Ω load.

If for each cycle from the square wave modulating the STVO two symbols are generated, corresponding to the low and high levels of the square wave, then the maximum expected symbol rate at the receiver would be less than 20 MSPS. Despite not having an estimated value for the bandwidth of the input signal expected at the receiver, a sampling rate of 5 to 10 times the 20 MSPS would suffice, as the symbol rate is already an overestimation. The resolution required for the ADC will depend on the gain of the receiver.



(a)



(b)

Figure 3.5: (a) PCB used to wire bond the die (b) Die containing the STVOs.

Relatively to the FPGA, FEUP provided a ZC706 Evaluation Board, from XILINX. This board contains a ZYNQ-7000 XC7Z045-2FFG900C SoC which integrates two Cortex-A9 processors and a FPGA. The user guide for this evaluation board can be seen in [26]. This board can be connected to Mezzanine Cards (Daughter boards) through two different FMC connectors. Some important connections from one of FMC connectors, HPC Connector J37 are:

- 34 differential user-defined pairs (34 LA pairs, LA00–LA33);
  - 3 of them are connected to clock capable pins
- 2 differential clocks + 3 from LA pairs
- power connections:
  - 159 ground;
  - 12P0V - 12 V board power supply (currently 12 V @ 5 A);
  - VADJ - default 2.5 V (capable of 2.5 V @ 6A);
  - 3P3V - (capable of 3.3v @ 10 A)

The evaluation board manual does not indicate if the differential pairs can be separated in single end transmission lines thus limiting the DAC and ADC input type to differential. Both the differential pairs and the differential clocks support the standard LVDS 25 which is compatible with LVDS. [26], [27] and [28] can be used to confirm that. Low speed control signals (SPI /I2C) can be used in a single end configuration.

A DAC that follows the requirements discussed above is the DAC3171 from Texas Instruments [29].

The choice of ADC has a large impact on the rest of the receiver. It is important to remember figure 3.2b, which is an example of the expected signal after filtering the output from the receiving STVO by a low pass filter. The region of interest for a FSK system is the linear region, which corresponds to an output voltage proportional to the input frequency. This voltage is in the order of a few mV. The greater the resolution the greater the number of frequencies that can be detected. The resolution can be achieved with a high resolution ADC, for example 16 bits or by amplifying

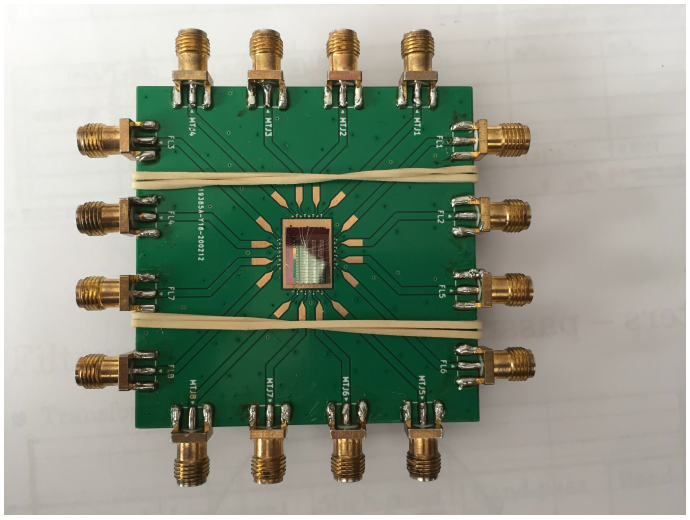


Figure 3.6: PCB containing the STVOs.

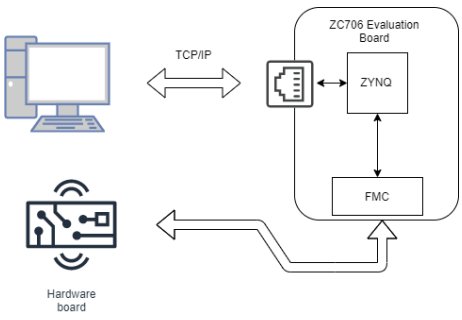


Figure 3.7: Functional flow chart representing the system.

Table 3.4: Some ADCs that can be used.

ADC	# of bits	Sampling rate	data input	supports LVDS	# of converters	price*
AD9467	16	200/250	differential	X	1	123.21€
LTC2208	16	130	differential	X	1	77.48€
ADS4145	14	125	differential	X	1	33.02€
ADS4129	12	250	differential	X	1	31.63€
AD9608	10	125	differential	X	2	30.31€
AD9480	8	250	differential	X	1	31.53€

*prices according to Digikey

the signal and possibly compensating its offset followed by a lower resolution ADC. A 16 bit ADC with a full scale of 1 Vpp could detect ∼65 levels per mV. Table 3.4 shows some ADCs that meet the requirements needed. Price wise both the 16 bit ones are to expensive for the project.

All the ADCs presented require a differential input. To convert the single ended signal to a differential signal one could use a RF transformer or a differential amplifier. The transformer would lead to a better noise performance by eliminating $1/f$ noise, on the other hand DC coupling is desirable since it would make it easier to characterize the STVOs, specially because there is no exact model. Each device is different from the other, and in the case to version 1 and 1.2 from table 3.1 dependent on the magnet position. This introduces the need to use a differential amplifier.

To improve the resolution of the ADS4145 (14 bits) to 16 bits a gain of 4 is required. Since all the ADCs presented already need a driving amplifier this would not come at much cost. On the other hand a gain of 4 introduces the need to compensate the DC offset from the bias point of the oscillator. For example, in figure 3.2b the DC offset is ∼0.36 V, multiplied by 4 it would result in a voltage of 1.44. Further increasing the bias point would results in voltages outside the supported range of the ADCs.

The introduction of the differential amplifier and the DC offset compensation scheme diminishes the importance of the ADC resolution since adding gain, even by cascading more amplifiers of similar noise performance does not come at much cost.

The final choice was the ADS4129 [30].

An overview of the system to be developed can be seen in figure 3.8. At this point the interface between the FPGA and both the DAC and ADC seems viable. The choices for the DAC and ADC where discussed above.

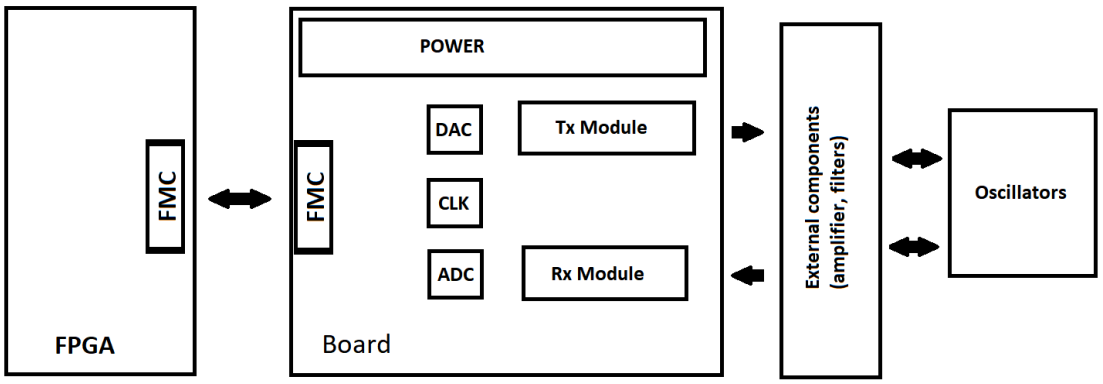
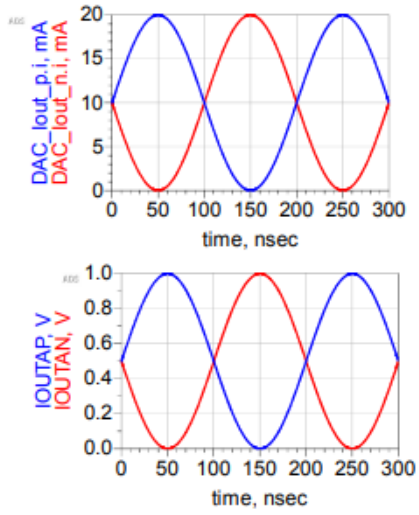


Figure 3.8: Diagram of the system to be developed.

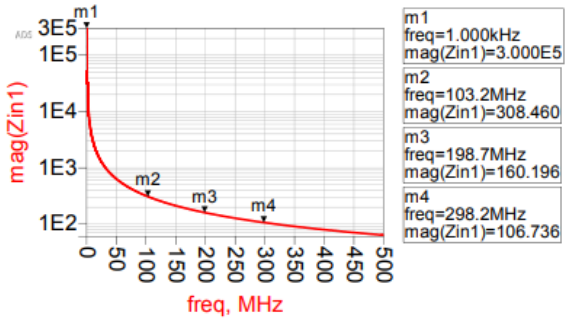
3.4 Transmitter Module

The transmitter module depicted as a block in figure 3.8 has, as its input the differential output from the DAC and its output is a single ended current source. Remembering table 3.2, the current source should be able to follow a voltage of 1 V for a 50 Ω load and 0.5 V for a 25 Ω load. For convenience of the wire bonding process, due to the die of the STVOs and their carrier PCB layout this current source is required to be bipolar, so it should be able to output ±1 V and ±0.5 V for 50 Ω and 25 Ω, respectively.

Each DAC output (IOUTAP, IOUTAN) is a current source capable of sourcing 0-20 mA with a compliance range of −0.5 V to 1 V. It presents an output resistance of $300K\Omega$ and an maximum output capacitance of 5 pF. The output current for a full scale 5 MHz sine wave can be seen in figure 3.9a. This figure also show the voltage when each output (IOUTAP, IOUTAN) is terminated in a 50 Ω load to ground. Figure 3.9b shows a simulation of the output impedance vs frequency curve from the DAC, based on its resistance ($300K\Omega$) and capacitance (5 pF).



(a)



(b)

Figure 3.9: (a) IOUTAP, IOUTAN output current and voltage when terminated on a 50 Ω load (b) DAC output impedance vs frequency.

In order to convert the differential output from the DAC to a single ended signal a DAC output amplifier was used. The amplifier selected is a THS3217 [31] which is able to operate from DC to 800 MHz. This device offers three stages, an input buffer, a differential to single end stage (D2S) and an output power stage (OPS). For the application in hand only the input buffer stage and the D2S were used. The D2S stage has a fixed gain of 2 V/V and typical current drive of 70 mA. The input referred noise relative to this 2 stages is $\sim 80nV/\sqrt{Hz}$@200 Hz and $\sim 8nV/\sqrt{Hz}$ for frequencies above 200 kHz. The device can be operated with a split supply (±4 V to ±7.9 V) or with a single supply (8 V to 15.8 V). A split supply of ±5 V was used.

Figure 3.10 depicts a circuit connecting the DAC3171 to the DAC output amplifier THS3217. The transmission lines TL3 and TL4 should have the characteristic impedance of the resistors

Table 3.5: Tx filters – parameters used in the design tool from RF Tools [33].

Filter	Response	Type	Topology	Order	Cutoff Frequency	Input/Output Impedance	Component Values
low	low pass	Bessel	Shunt First	10	30 MHz	50/50	E24
high	high pass	Elliptic	Series First	5	100 MHz	50/50	E24

Note: The elliptic filter used a Passband Ripple of 0.1 dB and Stopband Attenuation of 60 dB.

terminating the DAC output, in this case 50 Ω. Two 10 Ω resistors are required at the input of the THS3217 for better performance, as denoted in the THS3217 Evaluation Module User guide [32]. A simulation of the system is present in figure 3.11a. The group delay is flat until about 400 MHz. The gain at 100 MHz is 5.78 dB which is only 0.22 less than the 6 dB (2 V/V). At 380 MHz the gain is 3.8 dB. Assuming 50 Ω characteristic impedance the effect of the transmission lines length does not have an impact on the gain when the DAC output is terminated near the DAC, as seen in figure 3.11a, on the other hand, terminating the output near the THS3217 has a small impact (figure 3.11b).

Figure 3.12 shows the voltage and current on the output load. From this figure it is possible to see that the voltage requirements are met, although the output at this time is a voltage source and not a current source.

In section 3.2 a circuit capable of driving the STVOs based on a voltage source was demonstrated (figure 3.3). This circuit connects a voltage source with a 50 Ω impedance to a bias T. The low pass filter and high pass filter present there will now be discussed in more detail. The circuit and values for the filters are shown in page 14th from the schematics in Appendix A.1. The low pass filter is represented by the inductors L19-L23 and capacitors C108-C116. The high pass filter is represented by the inductors L24-L25 and capacitors C117-C121.

Both these filters were design using [33], which is a online calculator from RF Tools that allows the user to select the component values from a specific standard. Their characteristics are presented in table 3.5

It is crucial that the STVO detects:

- a high impedance in respect to the low pass filter, for frequencies above 100 MHz.
- a low impedance in respect to the high pass filter, for frequencies above 100 MHz.

It is also important that there is no signal path between the modulating signal and the RF output (output from the high pass filter).

The group delay should be constant for frequencies below 30 MHz since it means that the modulating signal, coming from the DAC does not get distorted. In this application, for frequencies above 100 MHz the group delay is less important because the phase on a FSK system is not the main concern. These are the reasons that lead to the filter parameters choice.

Adding the low pass filter discussed between the voltage source and the 50 Ω load from figure 3.10 creates the current source. The modulation ability of this current source can be seen in figure 3.13a, where the gain and group delay viewed from the DAC are described. In the pass band (DC–30 MHz) the change in group delay is less than 1ns, which is much less than the period of the a 30 MHz sinusoid ($T_{30\,MHz}$=33.3ns). The gain for low frequencies is similar to the gain of

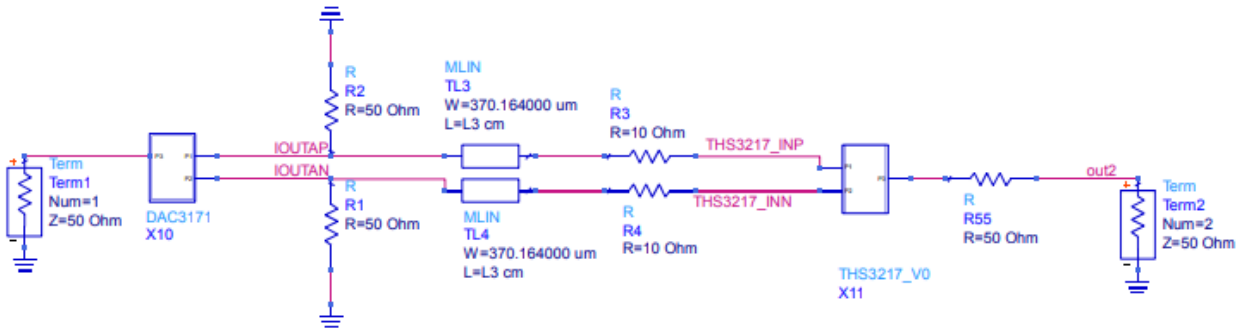
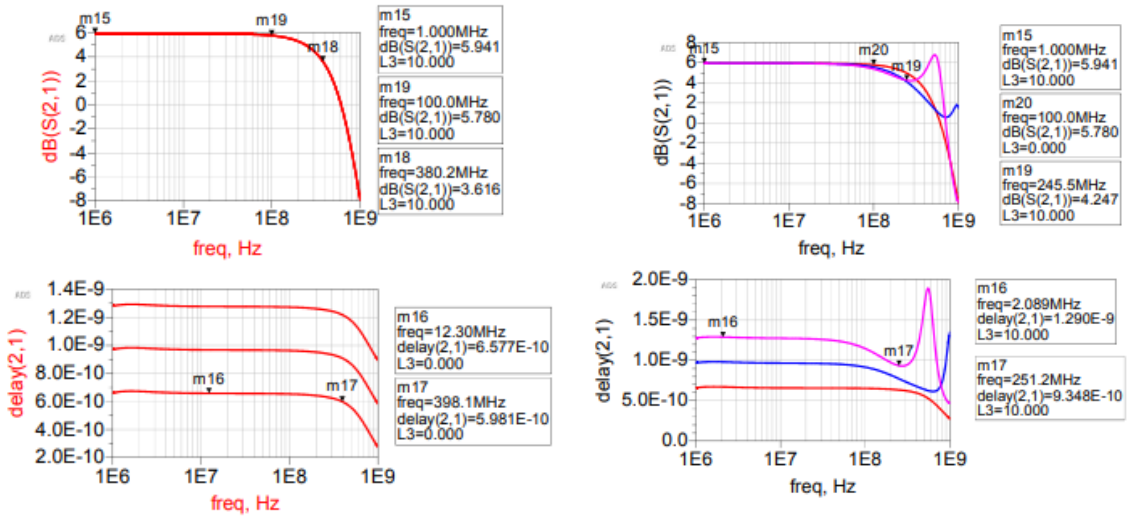


Figure 3.10: DAC + THS3217 diagram.



(a) (b)

Figure 3.11: (a) S(2,1) and group delay from the diagram in figure 3.10 for transmission line length = 0cm, 5cm and 10cm. (b) S(2,1) and group delay when the DAC output terminations are after the the transmission line for transmission line length = 0cm, 5cm and 10cm.

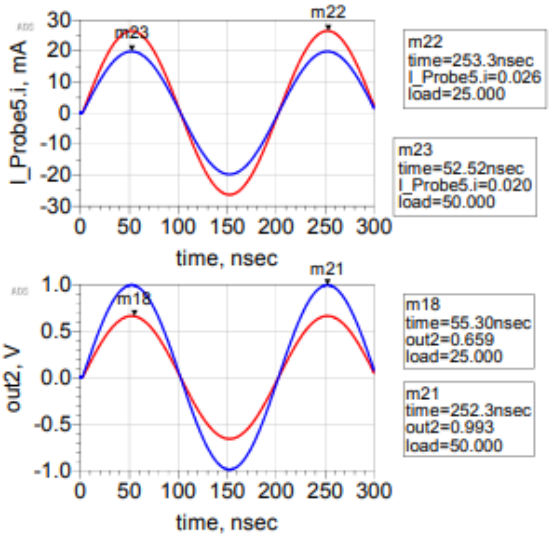
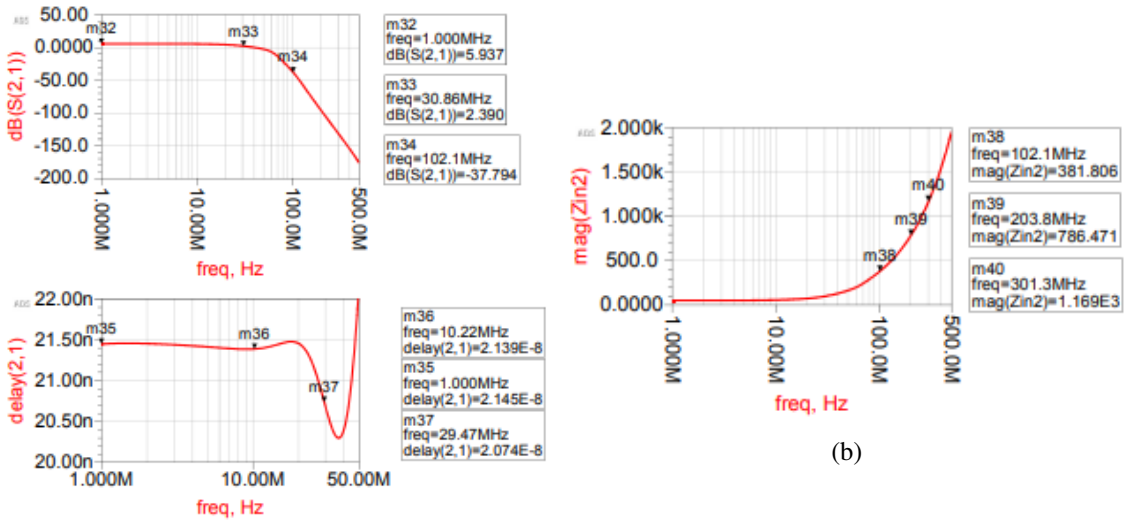
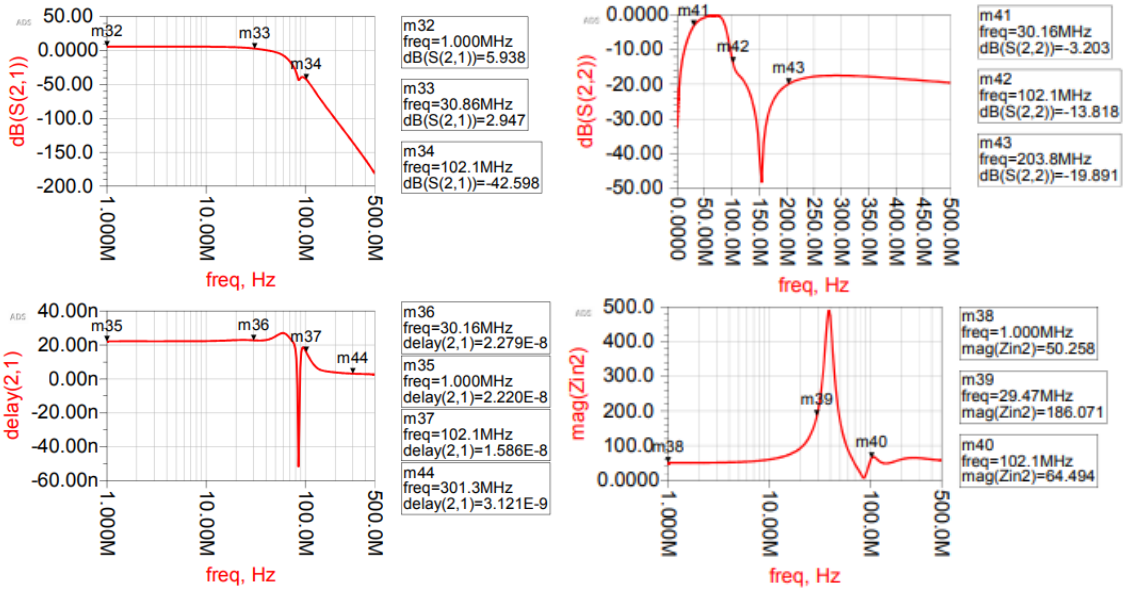


Figure 3.12: Output voltage and current for 2 loads: 50 Ω, 25 Ω



(a) (b)

Figure 3.13: Simulation of the transmitter current source based on the voltage source from figure 3.10 and the low pass filter used. Port 1 is the DAC input and Port 2 is the output of the low pass filter. Both Port have a 50 Ω impedance. (a) Gain and group delay from the current source. (b) Impedance detected by a 50 Ω load from the output of the low pass filter towards the DAC.



(a) (b)

Figure 3.14: Simulation of the transmitter current source from 3.13 with the added high pass filter and a 50 Ω load terminating the filter. Port 1 is the DAC input and Port 2 is the output of the low pass filter and input of the high pass filter. Both Port have a 50 Ω impedance. (a) Gain and group delay, relative to the DAC, detected at Port2, which simulates the STVO. (b) Reflection coefficient and impedance view from Port2, simulating the STVO.

the voltage source. At the cut off frequency the gain is closer to -3 dB relative to the inital system, which is a characteristic of bessel filters. Figure 3.13b describes the impedance view from the load towards the DAC. For frequencies above 100 MHz, which is the the operation region of the STVOs discussed, the higher the impedance, relative to the expected loads, the better the current source performance.

To complete the system a signal path for the output of the STVO needs to be provided. This is done by adding a high pass filter, as discussed before. The high pass filter should be terminated on a 50 Ω load, such as the input of an amplifier or test equipment. Figure 3.14a shows that adding the design high pass filter does not have an impact on the pass band of the current source (DC–30 MHz). On the other hand, figure 3.14b shows that for frequencies above the cut off frequency of the high pass filter (100 MHz) the STVO detects an impedance close to 50 Ω, which was not detected before.

The schematics for the DAC can be found in page 10 of Appendix A.1. The analog part of the transmitter module can be found in page 14.

3.5 Receiver Module

As seen previously in section 3.3 the receiver requires some gain, DC offset compensation and single ended to differential conversion. It also requires two current sources to bias the receiving STVO. The characteristics for these current sources was discussed in table 3.3. As in the transmitter module, the current source for the MTJ will also be changed to a bipolar one.

To get a resolution of ∼65 levels per mV with a 12 bit ADC, the input signal would require a gain above $16\times = 24\,\text{dB}$. Relatively to the bandwidth of the system two options were studied, a 10 MHz and a 40 MHz. The intention behind this choice was to implement the 10 MHz option, but to have a receiver capable of being upgrade without much cost.

3.5.1 Current sources

Beginning by the current sources, it is useful to remember figure 2.11a. That figure shows that the the current source that bias the MTJ should provide a signal path for the filtered oscillations that occur in the MTJ. This path is the input signal for the receiver module. As seen in the transmitter module, a current source can be achieved by adding a series high inductance to a voltage source.In the receiver, the voltage source used for both sources was based on a 16-bit DAC [34]. This DAC has 2 outputs that are being used in the selected range of 0 to 2.5 V. It offers a short circuit current of 40 mA. One of the main reasons for this choice is its low noise at low frequencies (1/f noise). The integrated noise 0.1 Hz– 10 Hz is only 6 μVpp. Its output referred voltage noise for frequencies above 10 kHz is $300nV/\sqrt{Hz}$. If the DAC injects a noise spectral density of $300nV/\sqrt{HZ}$ at the receiver input, an approximation for the expected peak to peak voltage at the input, on the 10 MHz system, would be $300n \times \sqrt{10\,\text{MHz}} \times 6.6 = 6.3\,\text{mVpp}$. This approximation applies for white noise since it assumes a constant spectral density. A square window was used for the bandwidth. The 6.6 value comes from 2×3.3 standard deviations converting Vrms to Vpp for Gaussian distributions. This conversion (Vrms to Vpp) also applies to 1/f noise. [35]

To create the current sources is, therefore necessary to filter this noise. It is also still needed to offset the voltage to create a bipolar source, to scale the voltage range for the appropriate range and to add the series inductance.

Shifting and scaling the voltage output can be done using an ampop in a inverting configuration. Some of the requirements for this opamp are:

- needs to have low 1/f noise, since it is not possible to filter low frequency noise when DC coupling is required
- needs to supply the output current necessary for the current sources
- It should have a low offset drift with temperature
- short circuit protection

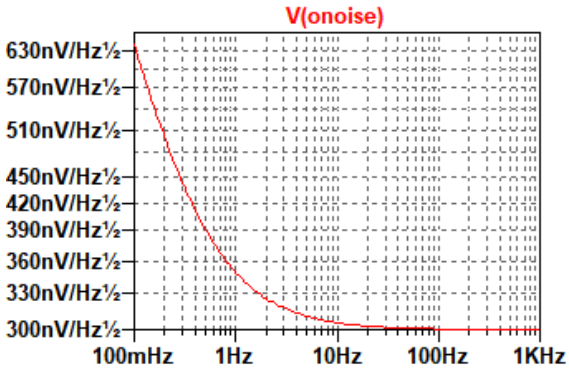


Figure 3.15: Model for DAC output noise based on [38] using LTSPICE: Integrated noise 0.1 Hz– 10 Hz= 1 μVrms=6.6 μVpp / 0.1 Hz– 10 MHz = 949 μVrms=6.2 mVpp.

An ampop that follows these criteria is the LTC6228 [36]. Its 0.1 Hz to 10 Hz is 0.94 μVpp. Analog Devices also provides a model for this amplifier which can be used in LTSPICE [37]. This model includes noise, which is a benefit.

For simulating the DAC output noise on LTSPICE a model based on [38] was used. The model includes both 1/f and white noise. Figure 3.15 shows the output of the model used and mentions the values for the integrated noise.

At this point the only two things missing are the high inductance and filtering the noise.

For the current source applied to the field line antenna of the STVO, since there is no signal path, the inductor should be as high as possible, as long as,it supports the frequency range of the STVO. For the current source applied to its MTJ, as in the case of the transmitter, a filter with an high inductor on the side of the MTJ could be used. Table 3.6 shows two options, one for the 10 MHz system and other for the 40 MHz system. Figure 3.16 shows the current source implemented to bias the MTJ with the filter for the 10 MHz system. In this figure the source V1 is the DAC and the points ns1n and ns1 are connected to the DAC noise model. V5 represents a 50 Ω load. L1-L3, C3,C4 is the output filter that provides the signal path to the Rx module represented by Vin_Rx_module. The capacitors C1 and C2 provide a filter for the noise. The simulated integrated voltage noise (0.1 Hz– 10 MHz) at Vin_Rx_module, with C1 and C2 is 5.715 μVrms = 37.7 μVpp . Without them the noise level is 880.75 μVrms = 5.8 mVpp. Further increasing C1 and C2 to 1 mF results in 4.95 μVrms = 32.67 μVpp. For noise levels between 32.67 μVpp and 37.7 μVpp the maximum resolution possible is between 27 and 30 divisions per mV. At the moment of the initial design this was deemed acceptable. Later, upon a better analysis of the circuit it was found that reducing the values of R5,R3 and R4, for example, to 1/8th of their current value for $C1, C2 = 200\,\mu$F, while maintains the same gain, further decreases the voltage noise level to 2.77 μVrms = 18.2 μVpp resulting in a resolution of 55.6 levels per mV, provided that the system is limited to 10 MHz. It should be noted that the component numbers (i.e. Cxx,Rxx) referenced above are relative to figure 3.16. These components have different numbers in the schematic A.1. Both current sources are present in page 16 from the schematic. The DAC mentioned is present in page 13.

Table 3.6: Rx filters - parameters used in the design tool from RF Tools [33].

Filter	Response	Type	Topology	Order	Cutoff Frequency	Input/Output Impedance	Component Values
F_10MHz	low pass	Bessel	Series First	5	15MHz	50/50	E24
F_40MHz	low pass	Bessel	Series first	5	50MHz	50/50	E24

3.5.2 Rx module

In this section the module that connects the input signal to the ADC input will be discussed. The input impedance for the filtered signal is design to be $\sim 50\,\Omega$, as can be seen in figure 3.16. Considering the filters from table 3.6 the input impedance is represented in figure 3.17.

The output from this filter is connected to a ampop chain with 4 stages:

1. pre amplifier - provides a gain of 4 V/V = 12 dB;
2. DC offset compensation and gain
3. provides selectable gain (user can select between 4 resistors)
4. Single ended to differential conversion, attenuation to protect ADC, filters ADC input

Table 3.7 summarizes the properties of the stages, as well as the over all system. Relatively to the 10 MHz system, it shows three out of four options for the selectable gain. The 40 MHz system is shown as a possibility for future upgrade of the system. A more thorough discussion of the performance will follow the system description.

The first three stages use the same ampop used for the current sources, LTC6228 [36]. Besides the low 1/f noise and low offset drift discussed before, some additional characteristics are, very low voltage noise $0.88nV/\sqrt{Hz}$, high gain-bandwidth product (GBW = 890 MHz), rail-to-rail output (± 5), unity gain stable and a slew rate of $500\,V/\mu s$. These four stages, with the exception of ADC input filter are present is page 15 of the schematics A.1. The ADC input filter is located in page 12. It should be noted that the values used in the schematics are for the 10 MHz configuration. The values for the 40 MHz configuration are located in table 3.7. The first stage is in a non-inverting configuration (U19), its function is to apply the maximum gain possible without saturating the

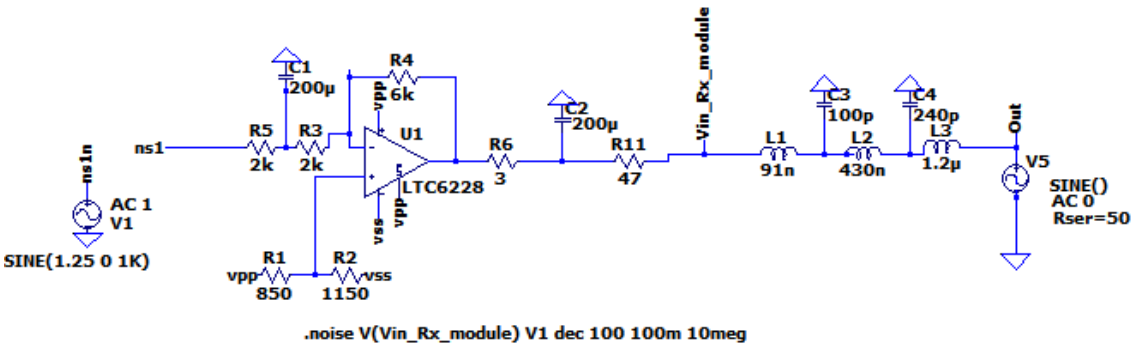
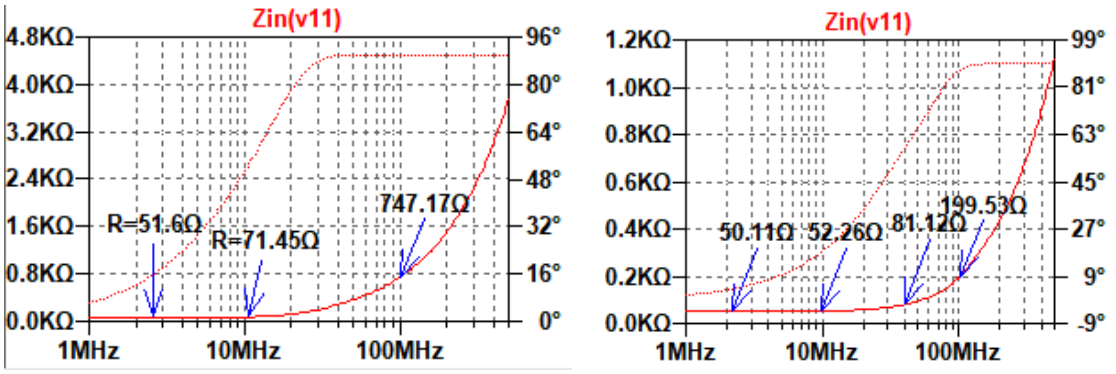


Figure 3.16: Current source (bias receiver MTJ) and signal path for Rx module.



(a) (b)

Figure 3.17: (a) Input impedance using first filter from table 3.6. (b) Input impedance using second filter from table 3.6.

output. Its layout does not require much space (few external components), which facilitates its placement near the signal input.

The second stage (U21) is in a inverting configuration. Two back to back diodes were added between IN+ and IN- to protect the opamp. The forward voltage must be below 0.7 V (currently used 0.5 V [39]) and they should support the expected frequency at the input. The input of the opamp is also internally protected by two diodes with a forward voltage of 0.7 V, but they are specified for a maximum of 10 mA. The simulation showed that not to be enough. A Pspice model for the external diodes used was included in the simulation. The opamp non inverting input is connected to a potentiometer so that the user can compensate the DC offset of the input signal.

The input of the third stage is connected to one of 4 resistors (R84-R87), selected by 4 switches (U18,U25,U26,U27). This allows the user to select between 4 different predefined gains. The switches are TS12A4517 from Texas Instruments. Texas Instruments provides a model which was used in the simulation. This stage also requires two back to back diodes for input protection.

U22 (ADA4927) is a differential ADC driver. It provides single ended to differential conversion with output common mode level adjustment. This device is recommended for frequencies ranging from DC to 100 MHz. At this stage the most important parameters are its bandwidth and slew rate. A large bandwidth ensures that the phase difference between each signal from the differential output is a small as possible leading to a better ADC performance. In the configuration used this stage will deal with large signals, so a large slew rate is also recommended. The output of this device is connected to a voltage divider and a filter (page 12 from the schematics A.1). The voltage divider provides the required ADC input protection. The filter helps limiting the input bandwidth and it also provides some group delay compensation. The simulated gain and group delay for the 10 MHz system, measured at the ADC differential input, with a selective gain resistor of 8 kΩ can be seen in figure 3.18. For frequencies between 1 MHz and 10 MHz the gain magnitude differs 0.5 dB. The group delay differs 3ns, which is much less than the period of these signals. A 10 MHz signal has a period of 100ns. Limiting this system to 10 MHz, with a digital filter with constant group delay, will therefore provide a receiver with a good performance.

Table 3.7: Rx module: Gain and cut off frequency of the receiver (LTSPICE simulation).

system	filter		1st stage	2nd stage		3rd stage			4th stage		Fc (-3 dB)	total gain(1)
	25 Ω(1)	50 Ω(2)	gain	gain	R100	gain	R selected	R96	differential gain	C91		
F_10 MHz	-3.7 dB	-6.3 dB	12.0 dB	35.6 dB	24 kΩ	7.0 dB	R86 (U25) = 4 kΩ		-12.9 dB	100 pF	16.1 MHz	38.0 dB
						27.9 dB	R87 (U18) = 350 Ω	5 kΩ			12.7 MHz	58.9 dB
						1 dB	R85 (U26) = 8 kΩ				18.4 MHz	31.9 dB
F_40 MHz				20 dB	4 kΩ	20.9 dB	R87 (U18) = 350 Ω	0 Ω		60 pF	39.3 MHz	36.3 dB

(1),(2) corresponds to the impedance of the source, the total gain was calculated with a 25 Ω source
The system is based on the input filter from table 3.6

Table 3.8 shows results of noise simulations including the whole receiver (filter, current source and opamp chain). Two particular cases for output referred noise are shown. The first, with the receiver configure to have a gain on 31.9 dB is the system that was mostly used to capture data. The second, with a gain of 71.8 dB, was used for debugging purposes. For a 77.88 μVpp input referred noise the receiver has a maximum resolution of 12.8 divisions per mV.

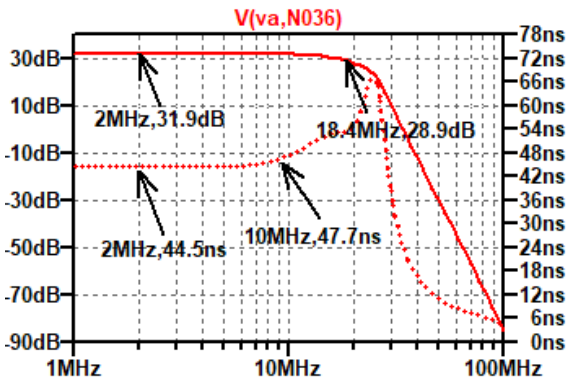


Figure 3.18: Simulation of the receiver gain and group delay for the 10 MHz system using a selective gain resistor of 8 kΩ, measured at the ADC differential input.

Table 3.8: Receiver noise simulation including the current source considering a 25 Ω MTJ as input (LTSPICE simulation).

	Vrms	**Vpp(0.10%)***
Input referred voltage noise (0.1 Hz– 10 Hz)	5.7 μV	37.6 μV
Input referred voltage noise (0.1 Hz– 10 MHz)	11.8 μV	77.88 μV
Gain = 31.9 dB**, selective gain resistor = 8** kΩ (measured at the ADC differential input)		
Output referred voltage noise (0.1 Hz– 10 MHz)	463.1 μV	3.056 mV
Output referred voltage noise (0.1 Hz– 100 MHz)	793.0 μV	5.234 mV
Gain = 71.8 dB**, selective gain resistor = 350** Ω (measured at the output of the third stage)		
Output referred voltage noise (0.1 Hz– 10 MHz)	45.2 mV	298.3 mV
Output referred voltage noise (0.1 Hz– 100 MHz)	61.0 mV	402.6 mV

* Vpp= 6.6Vrms, meaning that only 0.1% will exceed this value [35]

3.6 Clock

A clock source [40] was placed on the board to clock both the ADC and DAC. Using an external clock source, instead of the FPGA/ZYNQ pins is a standard practice for high speed ADCs and DACs. The main concern is the jitter level. To obtain a reference value for the ZYNQ output clocks jitter a Clocking Wizard LogiCORE^{TM} IP was used. This is a module, present in Vivado Design Suite, that implements clocking circuits and summarizes the output characteristics. For an input clock of 125 MHz, a jitter of 97.227ps peak to peak was obtained. Article [41] shows how to calculate, for an ADC, the signal to noise ratio (SNR) for a specific jitter value:

$$SNR_{ideal} = 20log_{10}\left(\frac{1}{2\pi ft}\right) \tag{3.1}$$

where f is the ADC input frequency and t is the jitter (rms) in seconds. To convert the jitter peak to peak to rms a factor of 14 is typically used. So, for a 97ps peak to peak which is equal to 7ps rms, and an input frequency limited to 40 MHz the SNR is 55 dB. The SNR required for a N bit ADC to operate in the full scale, also calculated based on [41], is:

$$SNR = [6.02N + 1.76] \tag{3.2}$$

Then, for a 12 bit ADC the SNR is 74 dB. The clock generator used [40], with a reference input clock of 25 MHz has an jitter rms of ∼400fs for both LVPECL and LVDS clock outputs, which are required by the DAC, ADC and FPGA. With this jitter value and for a input frequency of 40 MHz the SNR is 80 dB, which is greater than a 12 bit ADC requires. This clock generator provides 5 output clocks that can be independently programmed via SPI. Each output can operate for frequencies of 4.25 MHz to 1.175 GHz and supports LVDS and LVPECL and LVCMOS. For the implement design only 3 outputs puts are required. Both the DAC and ADC will use an LVPECL input clock, while the ZYNQ will use a LVDS input clock. The selected frequency for these clocks is 125 MHz. The following application reptorts from Texas Instruments, [42] and [43] were useful for both the schematic and layout of the clock signals.

3.7 Power supply

Table 3.10 shows the maximum current requirements and the voltage rails necessary for the ICs and modules previously discussed. The values for the transmitter and receiver module were simulated under normal operation, saturating the opamps to both rails and with the outputs shorted to ground.

As seen before, the ZC706 evaluation board provides to the FMC connector a 12P0V voltage rail directly from the board power supply, which at the moment is capable of providing 5 A. The implemented board uses this rail to create a 6 V rail based on the ADP2384 step-down dc-to-dc regulator and a −6 V rail based on the ADP5074 dc-to-dc inverting regulator. The schematics for these two regulators and shown in the Appendix A.1 on pages 2 and 7 respectively. Both these

Table 3.9: LDOs used to establish the power rails.

			Voltage	Schematics (apendix A.1)
LDO1	TPS7A87	output1 output2	3.3 V 1.8 V	page 6
LDO2	TPS7A87	output1 output2	1.8 V 3.3 V	page 11
LDO3	TPS7A87	output1 output2	5 V 5 V	page 9
LDO4	TPS7A33	output	-5 V	page 8

high performance voltage regulators are supported by the Analog Devices ADIsimPower which is an excel based tool that provides a bill of material for the external components needed and the layout for an evaluation board, as well as, the expected performance of the regulator based on the user specifications.

With the exception of the 2.5 V rail used for the SPI interface, which is provided by the ZC706 evaluation board all the other voltage rails were derived from the 6 V and -6 V rails using low dropout regulators (LDOs). The LDO used for the positive rails was the TPS7A87 [44], which is a with two outputs, each capable of sourcing 500 mA and short circuit protection. The output voltage noise can be as low as 3.8 μVRMS (10 Hz-–100 kHz). For the negative voltage rail the TPS7A33 [45] LDO was used. This LDO has a single output capable of sinking 1A and also provides short circuit protection. The output voltage noise can be as low as 16 μVRMS (10 Hz to 100 kHz).

3.8 Board layout

The final layout of the implemented board can be seen in Appendix F.1.The layout and schematics were generated with KICAD. A starting point for this PCB layout was the Analog Devices AD-FMCDAQ2-EBZ evaluation board [46], which is also a Mezzanine board (daughter board) compatible with the ZC706 evaluation board. This board contains a 14 bit ADC at 1 GSPS and a 16 bit ADC at 2.5 GSPS. ANALOG DEVICES and Texas Instruments also provide evaluation boards with both the schematics and layout for most of the ICs used.

The first step before starting the layout was to choose a manufacturer, which was JLCPCB [47]. This is important because the PCB needs to be designed according to the manufacturer capabilities (i.e. the minimum via size and clearance between adjacent vias from different/same nets, clearance between vias and tracks, ...). This manufacturer also provides an impedance calculator for single ended and differential signals for their controlled impedance PCB stackups. The stackup selected is a 4 layer PCB with a thickness of 1.6mm and made of JLC7628, which as an dielectric constant of 4.6. A choice was made to place the signals that require a controlled impedance in the outer layers. Under these conditions, the track width for 50 Ω single ended signals is 0.2934mm. For

Table 3.10: Worst case scenario current requirements for the ICs on the Board.

	Current requirements (worst case scenario) Power rails				
	5 V	-5 V	3.3 V	1.8 V	2.5 V
Transmitter module (current source short)	80 mA LDO3 (U10) output 1	80 mA LDO4 (U9)	-	-	-
Receiver module (both current sources shorted)	360 mA LDO3 (U10) output 2	280 mA LDO4 (U9)	-	-	-
DAC (AD5689) output 1,2 (open/short)	0.7 mA/80 mA	-	-	-	<1 mA
DAC (DAC3171)	-	-	35 mA LDO1 (U7) output 1	181 mA LDO1 (U7) output 2	<1 mA ZC706
ADC (ADS4129)	-	-	-	185 mA LDO2 (U12) output 1	-
CLKGEN (CDCE62005)	-	-	200 mA LDO2 (U12) output 2	-	-
2x SPI level shifter (FXLA108BQX)	-	-	<20 mA LDO2 (U12) output 2	<20 mA LDO2 (U12) output 1	<40 mA ZC706

differential signals with a 100 Ω differential impedance and a spacing of 0.2032mm the width of each trace is 0.2052mm. All the differential signals in the board obey to this specification.

The following considerations were followed:

1. maximize power traces width (low impedance)
2. maximize ground plane area (thermal dissipation)
3. expose copper on the back layer underneath the LDOs (thermal dissipation/heat sink)
4. clear GND/POWER planes underneath opamp in+/in- pins and, when possible, underneath high impedance sensitive traces (i.e. opamp chain. Reduce parasitic capacitance.)
5. minimize trace length in the receiver opamp chain
6. minimize trace length between the first stage of the receiver opamp chain and the 50 Ω termination of the controlled impedance input signal.

To route the differential signals the following application report [48] from Texas Instruments was followed. Some of the recommendations are:

1. when possible maximize spacing between different pairs
2. after the package escape and before connector terminations keep a minimum spacing of 5W = 1mm between different pairs
3. keep differential pairs 2.3mm away from the edges of the ground plane and 1.5W = 0.3mm away from voids
4. keep signals away from noise sources (i.e. switching regulators)
5. compensate inter and intra pair skew

In the DAC case all LVDS DATA signals and LVDS DATA clock signal were length match to 63.0mm with a maximum inter pair skew of 0.100mm.The maximum intra pair skew is 0.071mm.

In the ADC case all LVDS DATA signals and LVDS DATA clock signal were length match to 60mm with a maximum inter pair skew of 0.070mm. The maximum intra pair skew is 0.056mm for the clock signal and 0.000mm for the DATA signals. Due to layout constraints the ADC differential DATA outputs and DATA clock output are reversed in relation to what the FPGA expects. This is later compensated in the FPGA fabric.

3.9 FPGA

As mentioned before, the interaction between a computer and the developed PCB is made through the use of a ZYNQ-7000 SoC. It was also mentioned before that this device integrates two Cortex-A9 processors and a FPGA. Figure 3.19 shows simplified diagram of the implemented system, as

well as, some of the ZYNQ internal architecture. The ZYNQ device is divided in two parts, the processing system (PS) and programmable logic (PL). The PL corresponds to the FPGA, while the application processor unit (APU), contained in the PS holds the two processors. Only one of the processors was utilized in this project.

As the name indicates, the APU is capable of running applications. Two such applications, useful for this project and provided by XILINX are a TCP client and server based on the FreeRTOS^{TM} operating system and the lwIP (lightweight IP) TCP/IP stack. These applications appear as templates when creating an application project through Vitis^{TM} from XILINX. Vitis was the software used to create and run all application projects from this project. The hardware (platform projects) where developed through Vivado Design Suite.

By default the example code provided sets the board network interface IP, MASK and gateway address as:

```
#define DEFAULT_IP_ADDRESS "192.168.1.10"
#define DEFAULT_IP_MASK "255.255.255.0"
#define DEFAULT_GW_ADDRESS "192.168.1.1"
```

One way to run the server and client example code is to connect the board to a PC through a Ethernet cable, configure the Ethernet interface on the PC so that it is in the same network as the evaluation board and run a script that creates/accepts a TCP connection with the board and either sends or receives data based on whether the computer is acting as a client or server. By changing the lwIP configuration file to a TCP window of 65536 bytes the following throughtputs were obtained:

For the TCP connection between the ZC706 board and PC:

```
[  1] 55.0-60.0 sec   154 MBytes   259 Mbits/sec
[  1] 60.0-65.0 sec   163 MBytes   273 Mbits/sec
[  1] 65.0-70.0 sec   161 MBytes   269 Mbits/sec
[  1] 70.0-75.0 sec   161 MBytes   271 Mbits/sec
```

For the TCP connection between the PC and the ZC706 board:

```
[  1] 55.0-60.0 sec   221 MBytes   371 Mbits/sec
[  1] 60.0-65.0 sec   203 MBytes   341 Mbits/sec
[  1] 65.0-70.0 sec   206 MBytes   345 Mbits/sec
[  1] 70.0-75.0 sec   213 MBytes   357 Mbits/sec
```

These two examples were used to create a system where control signals and data could be traded between the computer and the ZC706 evaluation board. The PS has access to 1GB of external memory included in the evaluation board (DDR). This memory can be used to store the data.

Each block within the PL and the whole PS itself are designated by Intellectual Property (IP) cores. XILINX uses a master, slave communication interface for the IP cores designated by AXI. It also provides an AXI Reference Guide in [49]. A simple overview is listed bellow:

- Memory-Mapped Protocols (AXI4, AXI4 LITE, ...)

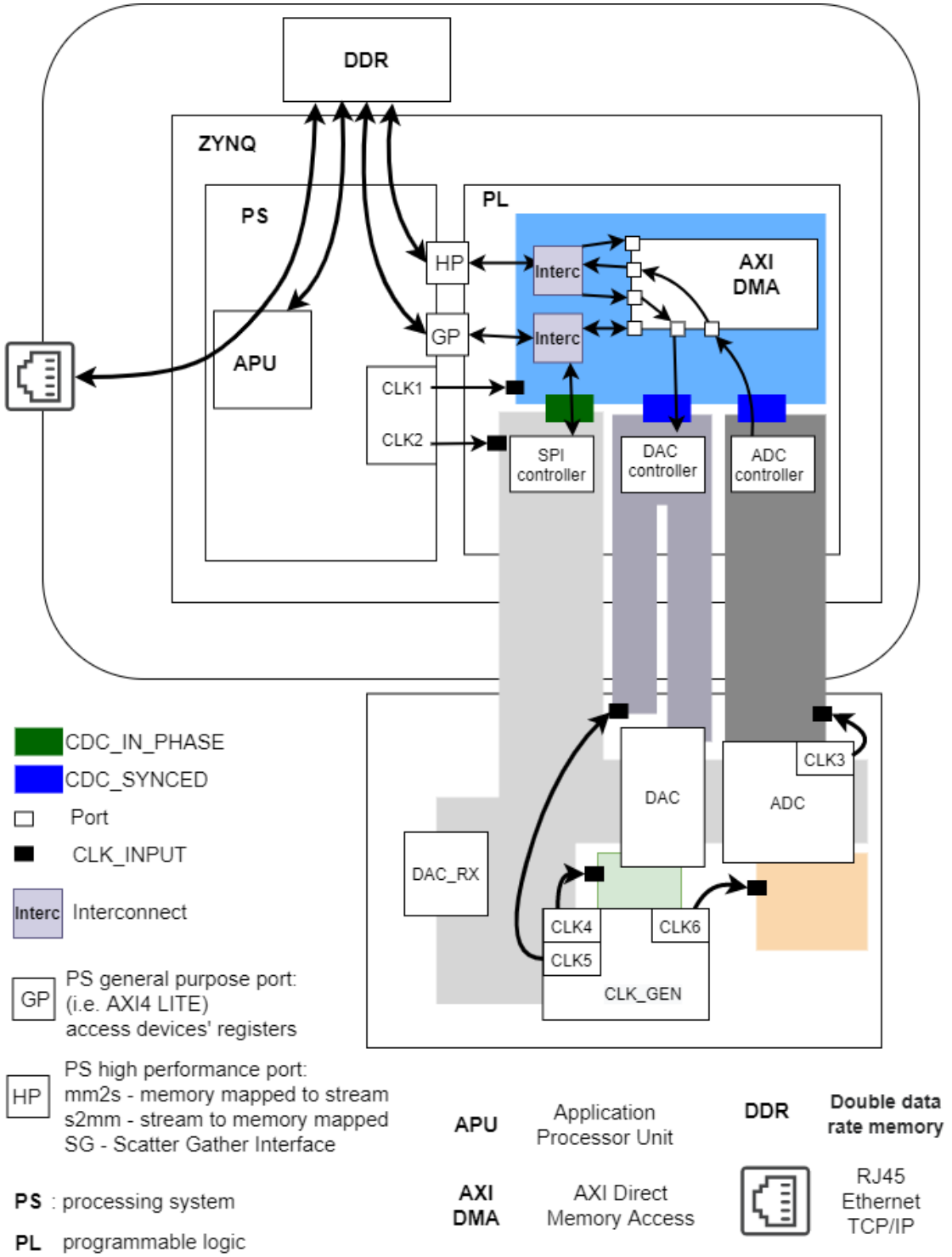


Figure 3.19: Functional diagram of the system implemented on the ZC706 evaluation board and clock regions interacting with the developed PCB.

  - These interfaces provide a defined memory map to the IP cores. An application can interact with these IP cores by performing read / write operations to the specified memory region.

- AXI4-Stream Protocol
  - Allows for a well defined and efficient mechanism to transfer data between IP cores when the concept of memory is not needed. For example systems that need to drive DACs and ADCs where the main focus is to send/receive data continuously at each clock cycle. A stream has an associated data bus width, for example a interface with a 32 bit data bus width means that each cycle 32 bits are transferred in parallel.
- Infrastructure IP (AXI DMA, ...)
  - AXI Direct Memory Access (DMA) used for memory-mapped to stream conversion

The PS corresponds to the ZYNQ7 Processing System IP core which allows for customization of its interfaces, for example, the number of output clocks and the frequency from each of them such as CLK1 and CLK2 visible in figure 3.19. The HP and GP ports are AXI interfaces that, among other uses, provide datapaths from the PL to the DDR. The AXI interconnects are used to route transactions between one or more memory-mapped master and slave.

The AXI DMA IP core [50] allows memory access to AXI4 stream interfaces. In the current configuration the AXI DMA is operating in Scatter/Gather mode and has two channels, one read channel, responsible for reading a specified region from memory and outputting a stream and one write channel, responsible for writing an input stream to a specified memory region. The Scatter/Gather mode works by reading from memory a set of read/write operations in a linked list format (descriptor chain). Each element from the list is designated by buffer descriptor (BD). This is done through the AXI4 Scatter Gather Read/Write interface that can be seen in figure 3.19 as one of the connections that originates in the DDR, goes through the HP port and reaches the AXI DMA. The other two connections on the HP port are the read and write channels discussed above. In the Scatter/Gather mode each BD can describe a data buffer up to 8,388,607 bytes. The current driver API (application programming interface) used for the AXI DMA IP core allows a maximum of 255 BDs per descriptor chain. This allows for a continuous transfer of 2GB for each of the two channels. The Scatter/Gather engine also allows the AXI DMA to operate in a Cyclic mode in which the last buffer descriptor points to the first allowing for continuous uninterrupted transfers. The application developed uses these two modes, allowing the user to either send a continuous packet at a time or to repeat the same packet in cyclic mode, creating periodic signals. Finally, the last connection with the AXI DMA IP core is a bidirectional connection that passes through the AXI GP port. This connection uses a AXI4 LITE interface and provides access to initialization, status, and management registers. The CLK1 mentioned is running at 200 MHz and clocks all interfaces of the AXI DMA.

In figure 3.19, bellow the AXI DMA there are three additional blocks, SPI controller DAC controller and ADC controller. Between the clock regions from the AXI DMA and the controllers

there are two blocks, CDC IN PHASE and CDC SYNCED, these blocks are only there to represent clock domain crossing. The CDC IN PHASE indicates that the two regions share clocks that may operate at different frequencies but originated from the same source, which allows Vivado to ensure a safe clock domain crossing. The CDC SYNCED indicates that the data transfer between the two regions needs to be synced. The mechanism used for syncing was the AXI4 Stream Data FIFO which allows different clocks for read and write operations and allows the user to choose an appropriate number of CDC sync stages. These FIFOs are actually included in the DAC and ADC controllers as can be seen in Appendix B.4 and B.5, respectively. The SPI controller can be seen in Appendix B.6.

Underneath the controllers there are different coloured regions. These regions represent the different clock regions. For example, the SPI controller zone touches the 4 ICs in the external board (DAC_RX,DAC,ADC,CLK_GEN) meaning that the interaction with them are in phase. Both the DAC and ADC controllers regions originate in the external board. The ADC clock region comes directly from the ADC IC since the output data and clock are synced together. In the DAC case the data flow originates in the FPGA, so the data is synced with the DAC controller.

All block designs for the hardware implemented for the Zynq device are include in B. The next to subsections will discuss the SPI, DAC and ADC controllers.

3.9.1 SPI controller

The SPI controller, as can be seen in B.6, has 4 myip_v3 IP cores. Each of these cores has a slave AXI4 LITE interface with 16 32bit memory mapped registers that allows an application running in the APU to interacted with them. These IP cores allow the user to choose which IC it will interact with, DAC_RX (AD5689 [34]),DAC (DAC3171 [29]),CLK_GEN (CDCE62005 [40]) and ADC (ADS4129 [30]) and implements the required protocol according to the ICs datasheets. This core also allows the user to specify up to 5 inputs and 5 outputs to interact with control signals. When creating IP cores through Vivado it will automatically create the AXI interfaces specified.

This module works by writing, from the running application, to its AXI4 LITE slave register 1 (slv_reg_1) the desired SPI command. The application then needs to send a start command. This is achieved by setting bit 0 from slv_reg0 . The transmission starts on the rising edge of the bit 0 from slv_reg0. The following code shows how the core interprets the start operation.

```
//  -------- spi_clk_en -------
    always @( posedge S_AXI_ACLK )
    begin
        spi_clk_en <= spi_clk_en + 1;
    end

//---------  spi_start gen ---------
    reg slv_reg0_prev;
    always @ (posedge S_AXI_ACLK)
    begin
        if(spi_clk_en)
        begin
```

```
            slv_reg0_prev <= slv_reg0[0];

        end
    end
    assign spi_start = (slv_reg0[0]==1'b1 &&
                        slv_reg0_prev==1'b0) ?1'b1:1'b0;
```

When the core detects a read command it will write the received data to the AXI4 LITE interface slv_reg3 so that the application can read.

```
    slv_reg3 <= spi_ans;
```

The verilog code for that implements the SPI interface specific for each IC is shown in Appendix C.

To verify the correct operation of this IP a test-bench was performed followed by the implementation of the design with a Integrated Logic Analyzer (ILA) IP core. This last step allows to test both the logic of the module as well as its interaction with the application running in the PS. A simple driver was implemented to send SPI commands. In case of a read command the function returns the value read:

```
//
    u32 SPI_(MyIP* inst , u32 command){

        xil_printf("SPI: sending command: %x.\n\r",command);

        MYIP_mWriteReg(inst->BaseAddress, MYIP_S_AXI_SLV_REG1_OFFSET, command);
        MYIP_mWriteReg(inst->BaseAddress, MYIP_S_AXI_SLV_REG0_OFFSET, 0
            x00000001);
        MYIP_mWriteReg(inst->BaseAddress, MYIP_S_AXI_SLV_REG0_OFFSET, 0
            x00000000);

        usleep(1000);

        return MYIP_mReadReg(inst->BaseAddress, MYIP_S_AXI_SLV_REG3_OFFSET);

}
```

Listing 3.1: SPI Driver implemented – C

For demonstration purposes, the results obtained by the ILA IP core for the my_ip_v3 configured for both the DAC AD5689 (DAC_RX) and clock generator CDCE62005 (CLKGEN) are represented in figures 3.20 and 3.21, respectively. Comparing these figures to the datasheets ([34], [40]) specifications one conclude that both the IP core developed and driver are working as intended. The same applies for the ADS4129 and DAC3171 configuration.

3.9.2 DAC/ADC controller

The DAC and ADC controller can be seen in Appendixes B.4 and B.5 respectively. These two modules are somewhat similar to each other, being the main difference the data flow direction. Both diagrams have a SelectIO wizard IP core. This module can be used to facilitate the input and output of data to the external pins. It supports single to differential / differential to single ended conversion, so that the FPGA can accept differential signals such as LVDS 25. It also supports double data rate (DDR) transfers which was the mode selected for both ICs. If needed, this module can be used to delay the data signals or the clock signal.

Both diagrams also have an AXI4 stream data FIFO, responsible for a safe clock domain crossing. As seen before, the AXI DMA runs at 200 MHz from an internal clock source, while the controllers run from an external clock source, in this case running at 125 MHz.

On the DAC block diagram the differential output clock DAC_DATA_clk_p/n goes through a clocking wizard and an oddr IP core to add a 90º delay relative to the data edge, as seen in figure 3.22.

The ADC diagram shows a tlastgen IP core, this module was obtained from XILINX examples and creates a signal (tlast) that can be used by an AXI4 stream interface to indicate that a certain number of samples has arrived.

Figures 3.22 and 3.23 show a diagram for the input and output data for the DAC and ADC respectively. Both ICs are running at double data rate, but the data format is different. For a given sample, the DAC expects the MSBs (most significant bits) and the rise edge of the input data clock and the LSBs (least significant bits) at the next fall edge of the same clock signal. On the other hand the ADC alternates between even and odd bits. To account for this a new IP core was developed (ddr2dr). The verilog code for this IP core is located in Appendix D. The block diagram for the DAC and ADC controllers were simulated on a testbench. Even to verify the logic functionality from these diagrams, it is necessary to synthesise the design, otherwise the delays from the Clocking wizard and SelectIO IP cores are not accounted for. The results from these simulations are depicted in figures 3.24 and 3.25.

Figure 3.24 shows that the data that enters the AXI4 stream data FIFO (DAC_FIFO_INPUT) appears at the output pins delayed by a few clock cycles. The input sample 0x1e41 (first marker) appears at the output pins as 0x3141 (second marker). This occurs because the data is divided in the 7 MSBs and 7 LSBs. The alignment of the data with the output clock can also be verified. The dac expects data in two's complement.

Figure 3.25 shows the simulation for the ADC controller. It is important to remember that the ADC differential inputs are reversed due to layout constraints. As such the testbench clock (tb_adc_clk_p) is applied to the adc_clk_n which is the input pin from the FPGA. From the ADC output timing, represented in figure 3.23, it is seen that the even bits from a sample need to be read at the falling edge of CLKOUTM (adc_clk_n) and the odd bits of the same sample on the next rising edge. This can be confirmed on the second marker from figure 3.25 where the output from the SelectIO wizard (data_in_to _device) concatenates the data seen at the FPGA input pins

(adc_p) from the two previously clock edges. At this point the data bits have the opposite value and the bits are separated in even and odd. The ddr2dr IP core corrects this. The correct value is shown at the output of the AXI4 stream data FIFO (ADC_FIFO_OUTPUT) on the third marker (0xfffffeee). The ddr2dr module also performs the correct sign extension since the data format selected is in two's complement.

3.9.3 Constraining and implementing the design

Constraining the design is important for several different reasons:

- connecting the design ports to the correct package pins
- selecting the correct standard for each port (i.e. LVCMOS, LVDS, ...)
- selecting the desired termination (i.e. LVDS 25 can be used with an internal or external 100 Ω termination).
- avoid design failures / incorrect optimizations due to paths perceived as problematic but that are actually safe, using set false path constraint
- defining external clocks
- defining the timing requirements for inputs and outputs (from and to package pins) (set input delay and set output delay constraints)

The constraints applied to this design can be seen in Appendix E. The correct package pins can be seen by comparing the page 1 from the schematics, Appendix A.1, with the ZC706 board FMC connections [26].

Both the input and output signals from the SPI controller module are in the standard LVCMOS25 and do not have any termination. The clock signals and signals from the ADC and DAC controllers are all in the standard LVDS 25. The input signals require an internal 100 Ω termination.

The external clocks need to be defined, in this case as 125 MHz clocks.

The set input / output delay constraints for the ADC (ADS4129) and DAC (DAC3171) data paths need to be specified in accordance with their datasheets, as well as, the skew between different lvds pairs external to the FPGA.

The ADC datasheet [30] specifies, for a frequency of 125 MHz, a minimum setup time of 2.3ns and a minimum hold time of 0.6ns. This means that the ADC guarantees that the output data is ready to be read 2.3ns before the clock edge and wont become invalid until at least 0.6ns after same clock edge. The constraints applied to the input pins that originate in the ADC are of the type set input delay. The values selected were,-min 0.6, indicating that the data at the FPGA input will be valid for more 0.6ns and, -max 2, indicating that the next sample will be ready, at the FPGA input, 2ns after the clock edge. On a 125 MHz clock, when the data is being read at double data rate, the spacing between clock edges is 4ns, so, if the ADC guarantees that a sample will be ready

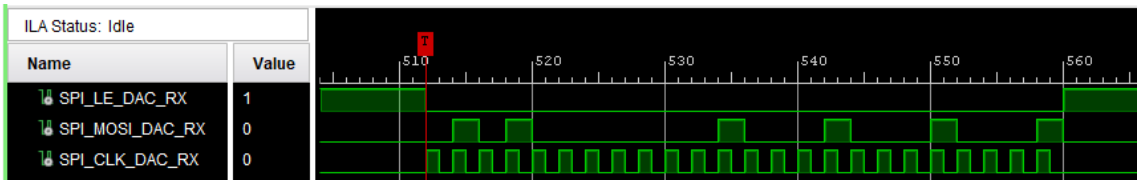


Figure 3.20: Waveform detected by the ILA IP core for the IC AD5689R (DAC_RX). Input commmand:$SPI_(\&AD5689R, 0x501111);$.

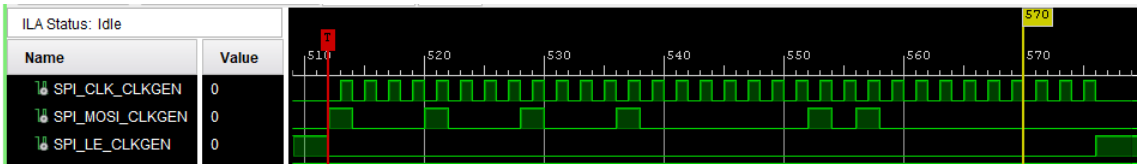


Figure 3.21: Waveform detected by the ILA IP core for the IC CDCE62005 (CLKGEN). Input commmand:$SPI_(\&CDCE62005, 0x00501111);$.

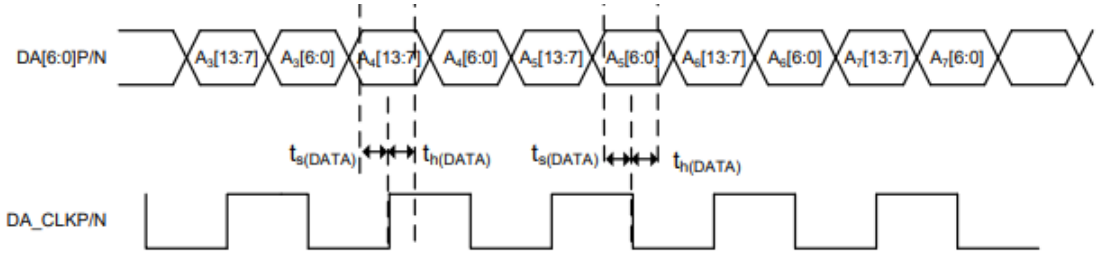


Figure 3.22: DAC3171 Input Data Timing Diagram for 7-Bit DDR Interface Mode, reprinted from [29].

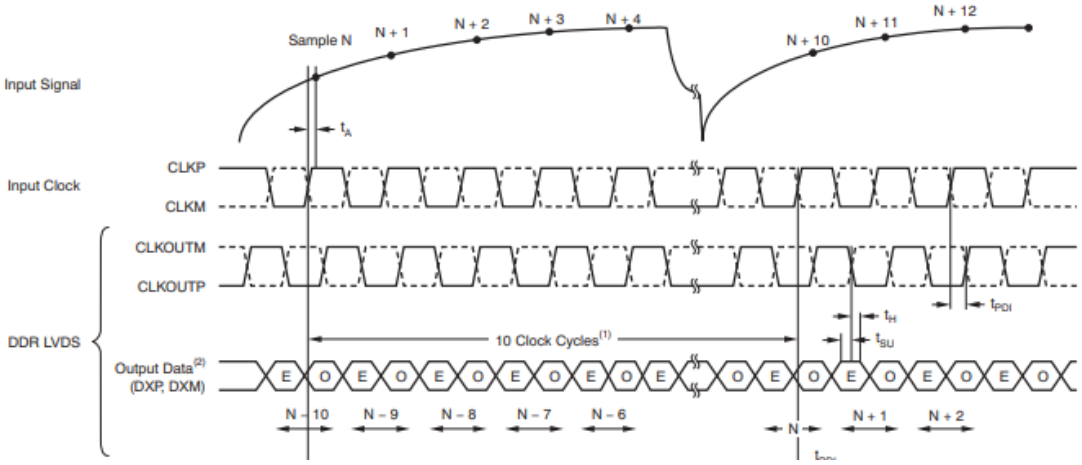


Figure 3.23: ADS4129 Output Data Timing Diagram for 6-Bit DDR Interface Mode, reprinted from [30].

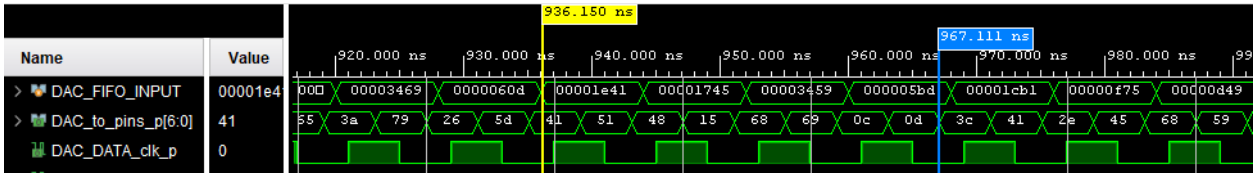


Figure 3.24: DAC controller block diagram: Post synthesis timing simulation.

2.3ns before the clock edge, specifying to the FPGA that the next sample will only become ready after 2ns implies that the data wont be read until 4-2=2ns before the next clock edge. This leaves a margin of 0.3ns on the setup time and 0 on the hold time. This margin was deemed sufficient because these values are based on the more constrained values and the ADC allows, via its SPI interface, some control of the phase between the clock edge and the data.

By default, the DAC [29] as a typical required setup time of -20ps and a typical required hold time of 710ps. This implies that the DAC requires its input data to be ready -20ps before the clock egde and that it needs do remain valid until 710ps after the clockedge. These values can also be controlled via the DAC SPI interface. The constraints applied to the output pins from the FPGA are of the type set output delay. Their values are, -min -1, indicating that the data at the output pins of the FPGA needs to be ready 1ns before the clock edge and, -max 0.5, indicating that the data needs to remain valid for at least more 0.5ns.

Having defined the constraints the next step is to implement the design and verify if it was successful. This happen to be the case, all user defined timing constraints were met.

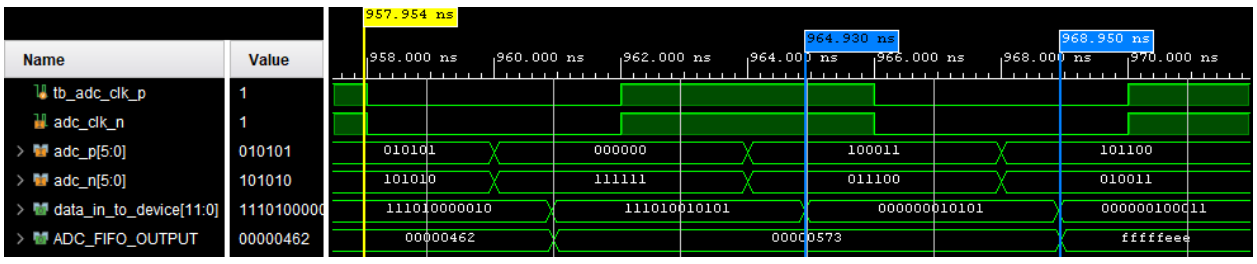


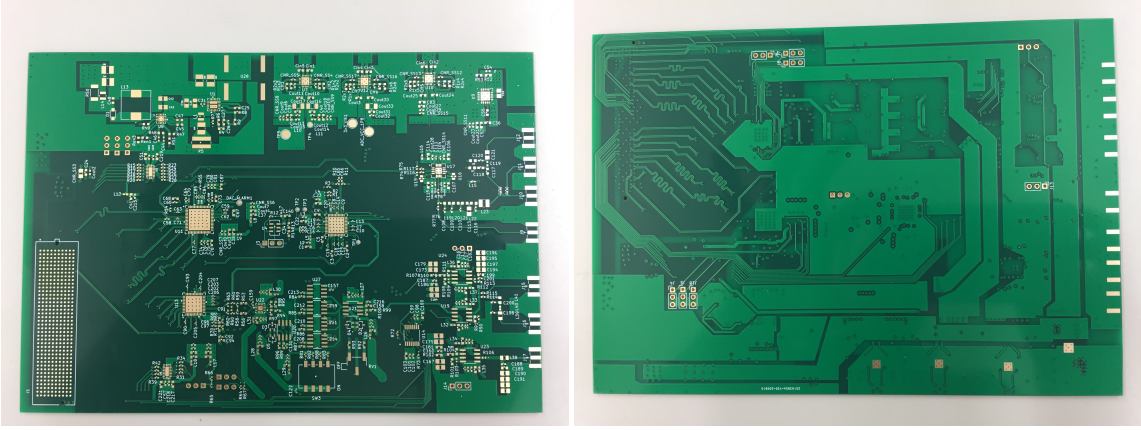
Figure 3.25: ADC controller block diagram: Post synthesis timing simulation.

Chapter 4

Results

4.1 Board assembly/ Preliminary test

The purpose of this chapter is to discuss the board assembly and characterize it, as well as, some improvements made to it. Later in the chapter the board will be used to test the oscillators.



(a) (b)

Figure 4.1: (a) Front view of the PCB. (b) Back view of the PCB.

Figure 4.1a and 4.1b show the produced PCB.

This PCB was soldered, almost in its totality by Pedro Alves, Professional Engineer at FEUP. The board assembly was divided in modules so that the PCB could be tested simultaneously with the PCB assembly. The first stages of the assembly are depicted in figure 4.2. In the first stage, figure 4.2a, the FMC connected was soldered. Testing this stage consisted, first, on performing continuity checks with a multimeter to verify that every connection needed was made. To pass this test it was necessary to reheat the connector several times. The high number of pins (400) and connector design made it difficult to solder the inner pins with a hot air station. After passing the continuity check, the PCB was connected to the ZC706 evaluation board and the 2.5 V and 12 V power rails were checked.

In the second stage, figure 4.2b, the 12 to 6 V switching regulator and 12 V to −6 V inverter were assembled and the output voltages checked.

The third stage, figure 4.2c, consisted in soldering all the positive rail voltage regulators (LDOs) leaving only the $-5v$ regulator left. Instead of completing the power supply with the −5 V rail, the next component selected was the DAC (AD5689) responsible for the current sources of the receiver. This choice was made out of convenience. Testing this DAC allowed to test part of the digital interface (SPI) with the ZC706 board, which in turn allowed to advance to the next stage. Figure 4.3 shows the two outputs from the DAC (AD5689) working with some test commands, since the board power up.

In the fourth stage, figure 4.2d, the power supply was completed. The clock generator and its dependencies (i.e. crystal oscillator, level shifter for the SPI interface) were soldered. The DAC (DAC3171) for the transmitter was also included in this stage. Several tests were performed on this stage. Testing the clock generator (CDCE62005), started by checking if the FPGA could detect its third output clock (output 3) which, by default is set to 125 MHz/ LVDS. The implemented design on the FPGA was also expecting a 125 MHz LVDS (LVDS 25) clock signal. Figure 4.4b shows part of the input stage implemented on the FPGA. This module connects the input clock to a counter and the counter to a ILA which was used to debug the counter output in real time. A module similar to this was included for all the external clocks. The SPI connections were also probed. Figure 4.4a shows two signals (Latch enable and clock) from the SPI connection, before the level shifter required to accommodate the 3.3 V level required by the clock generator. To test both the clock generator and DAC SPI interface, a series of read and write commands was sent using the diver shown in listing 3.1. The listing below shows some of the SPI commands sent required to configure these ICs, as well as, the answer received.

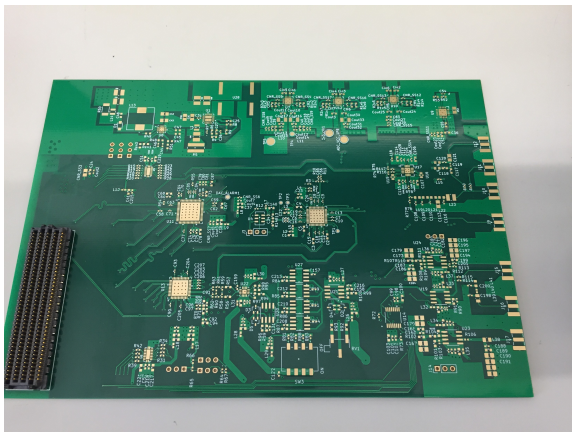
```
ans = SPI_(CDCE62005,0x0000000E); // reads CDCE62005 reg0
// ans:  CDCE62005 reg0 = 8184032 -- default: 8184032

SPI_(CDCE62005,81860320); // writes 0x8186032 to reg 0: sets output 0 to 125MHz
    LVPECL
ans = SPI_(CDCE62005,0x0000000E); // reads CDCE62005 reg0
// ans: CDCE62005 reg0 = 8186032
108

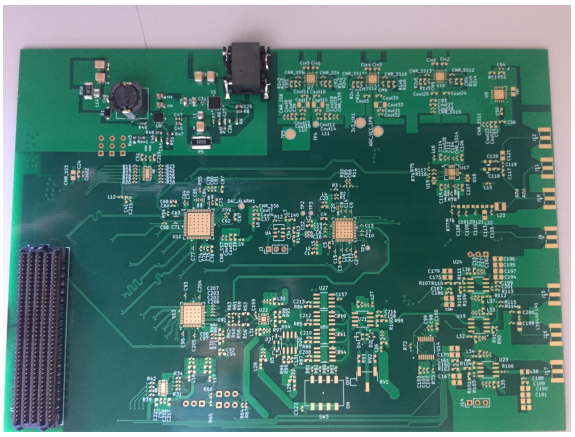

SPI_(DAC3171,0x023F80); //  writes 0x3F80 to DAC3171 config2: necessary to
   activate DDR 7bit mode: turns off bits(6:0)
ans = SPI_(DAC3171,0x820000); // reads DAC3171 config2.
// ans config2=3F80

SPI_(DAC3171,0x030001); // writes 0x0001 to DAC config3: necessary to activate
   DDR 7bit mode:  pins 6,7 become the DATACLK
ans = SPI_(DAC3171,0x830000); // reads DAC3171 config3.
// ans: config3=830001
```

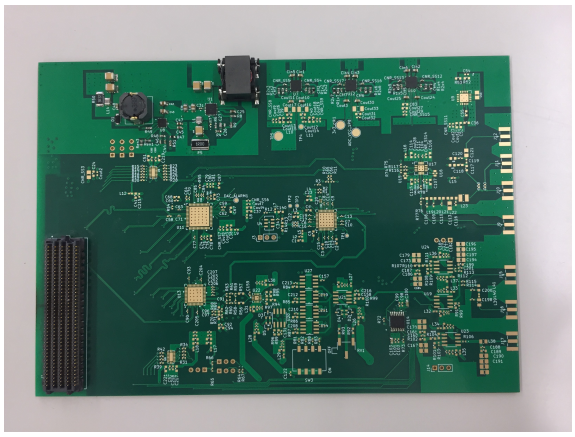
Listing 4.1: Some SPI commands sent / part of the required PCB initialization



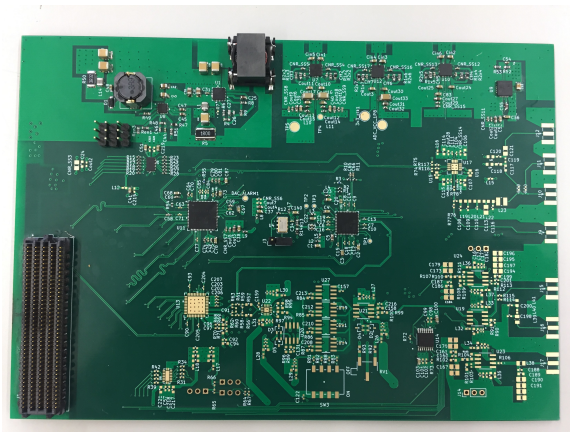
(a) FMC connector.



(b) Power supply: (+6 V,−6 V).



(c) LDOs: 3.3 V, 1.8 V, 5 V +DAC_RX.



(d) CLK generator + DAC TX.

Figure 4.2: (First stages of the PCB assembly.

The next few stages can be seen in figure 4.5.The only components left are the output filters, the SMA connectors and the passive elements that connect the Rx module to the ADC.

The addition of the Transmitter module, even without the output filters, allowed to test, in real time, both the DAC and the implemented system that connects the DAC to the application layer within the ZYNQ, consisting of the PCB traces, FPGA logic, APU to logic fabric transfer and the application itself. Figure 4.6 seems to indicate a correct implementation of the system, as it shows three different outputs detected in the transmitter module.

After that, the receiver module and ADC were added. The configuration of the receiver module is the F_system seen in table 3.7. The values for the four selective gain resistors are the two seen in the referred table (350 Ω, 4 kΩ) and two additional ones (2 kΩ, 8 kΩ). The analog input of the ADC was left unconnected to prevent over voltage in case of a malfunction of the receiver module. The ADC was included in this assembly stage as it provides the common mode voltage necessary to the last stage of the receiver (single ended to differential conversion). After powering up the board the following tests were passed successfully:

1. measuring the operating point of the two current sources

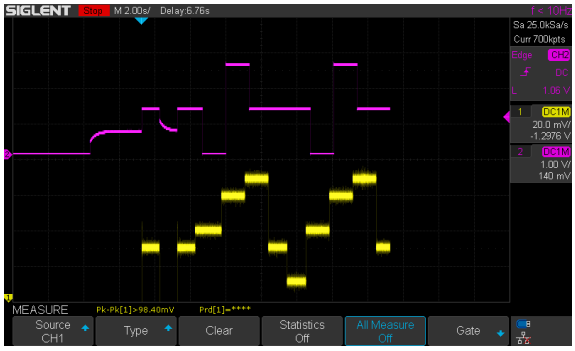
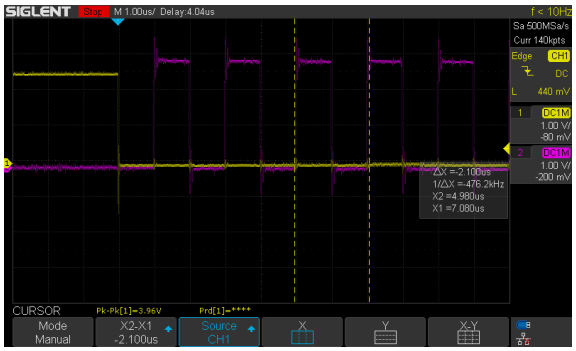
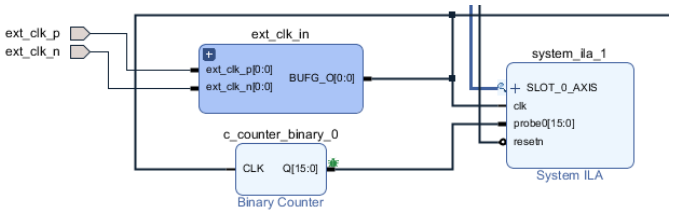


Figure 4.3: AD5689: DAC RX initialization and outputs (1,2) level changes – Time:2s/Div Ch1 (yellow) :20 mV/Div Ch2 (pink) :1 V/Div.



(a)



(b)

Figure 4.4: (a) Probing CDCE62005 SPI signals (b) Module used to debug one of the external clocks – included in Appendix B.1.

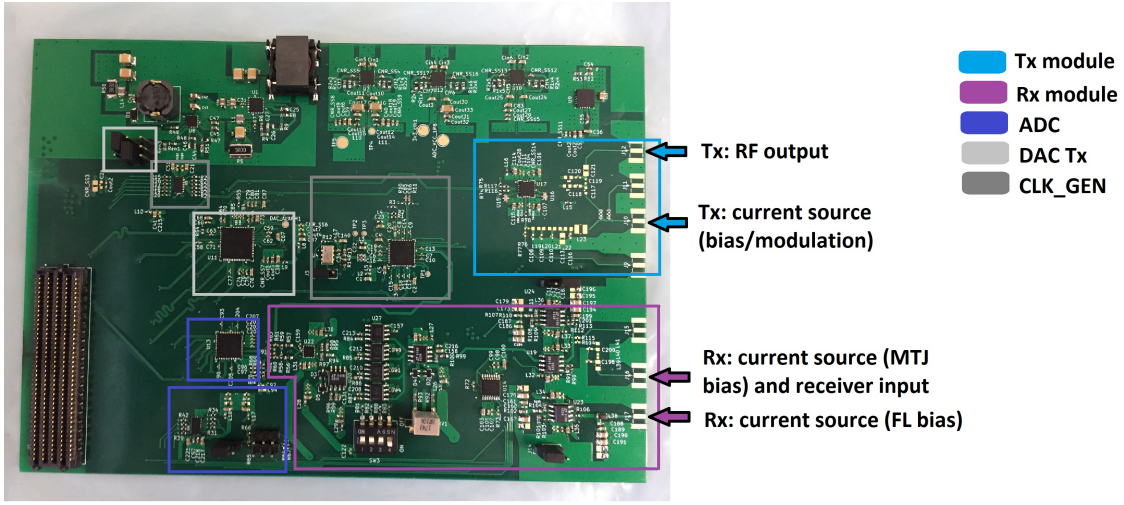
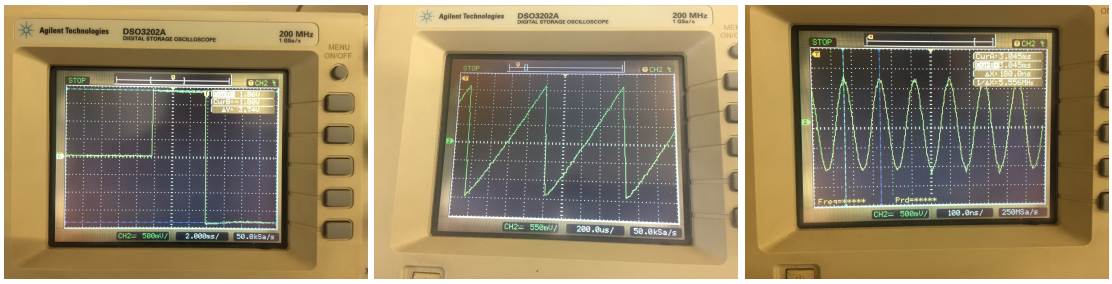


Figure 4.5: PCB divided in modules.



(a) (b) (c)

Figure 4.6: Single ended signal detected at the output of the Transmitter module with no output filters and no load. (a)step (b)saw tooth – full scale (c)sine wave – 5.6 MHz

2. changing the DC offset correction allowing the circuit to saturate to both power rails (±5 V)
3. measuring voltages along the receiver module and the ADC common mode voltage output
4. changing the operating point of the current sources by changing the DAC (DAC_RX AD5689) outputs
5. remeasuring voltages along the receiver module
6. checking that the differential output voltage levels were within the expected range, making it safe to interact with the ADC input.

On the other hand, two significant problems were detected.

1. the ADC does not output a clock signal
2. unexpected high level of low frequency noise

The first problem was identified, first by failing to detect a clock signal using a module equivalent to the one seen in figure 4.4b and secondly by probing the PCB. An attempt was made to identify the cause for this problem. All connections between the ADC and the PCB, and all the voltages at the appropriate input pins were rechecked and deemed correct. The input clock configuration was also appropriately set in the clock generator (LVPECL 125 MHz) . After having tried to resolder the ADC several times a decision was made to replace the component. This time, besides replacing the ADC, the connection between the receiver module and the ADC input was made. This solved the problem.

The second problem is discussed in the next subsection (4.1.1).

4.1.1 Receiver: noise performance and improvement

The unexpected high level of low frequency noise, discussed in the previous section, was identified by selecting the highest gain possible in the receiver module and probing the output of the third stage of the ampop chain. According to table 3.7 this stage has a gain of 58.9 dB+12.9 dB+3.7=75.5 dB∼

5957 V/V. The input filter is ignored since at this point it was not soldered. Figure 4.7 shows the noise level detected in this point. Assuming a peak to peak value of 9 V this would be equivalent to having an input signal with 1.5 mVpp (9/5957), which is not acceptable. To track down the noise source the receiver opamp chain was probed to see if there was coherence between the input and output of the various stages. This analysis can be seen in figure 4.8. Figure 4.8b, compares the receiver input with the output from the second stage and appears to be the one with the least coherence. This is expected since the noise level becomes less relevant as gain is introduced to the input signal.

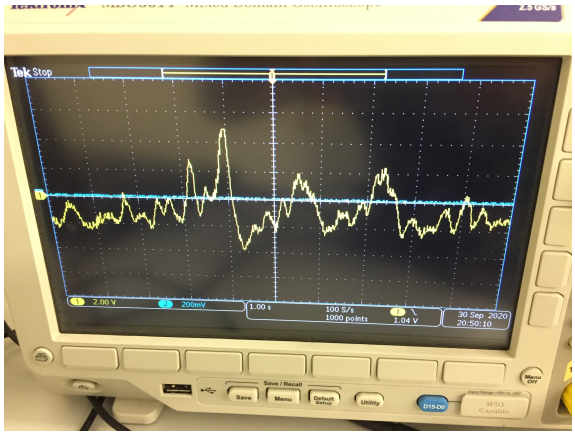
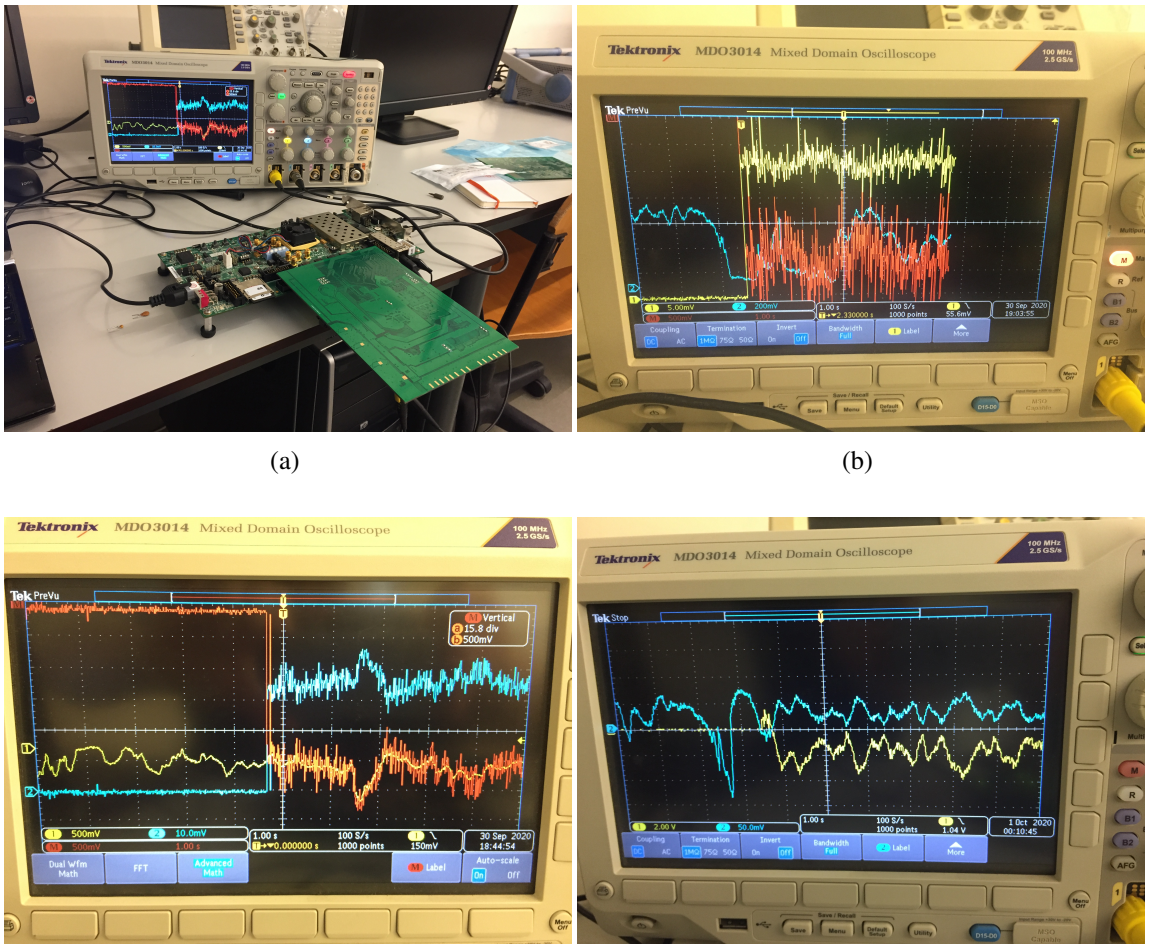


Figure 4.7: Noise level detected in the receiver module at the output of the third stage of gain: 1s/Div 2 V/Div

The second test performed was to short the receiver input to ground. The results can be seen in figure 4.9. In this figure the peak to peak noise level is about 1 Vpp. Corresponding to an input noise level of $\sim$167 μVpp. This value indicates two things. The first is that the main source of noise was connected to the receiver input, which is the current source that bias the MTJ, as seen in the sub section 3.5.1. The second is that the noise level of the receiver module (opamp chain) referred to its input is still high, compared to table 3.8, where the output referred noise measured at the output of the third stage was simulated (402.6 mVpp from 0.1 Hz to 100 MHz). It should be noted that the simulation includes both the filter with a 25 Ω load and the current source, which will result in a higher noise level compared to a short circuit at the input.

One possible cause for this low frequency noise is the noise introduced by the power supply. One critical node found that may be subject to this noise was found in the current source that bias the MTJ. This current source uses an opamp (U24 from page 16 of the schematics – Appendix A.1). Connected to the non inverting terminal of this opamp there is a voltage reference created by a resistor divider. This node was not bypassed. The other critical node was found in the receiver module (opamp chain) in the DC offset regulator. This regulator is based on a potentiometer connected to the non inverting input of the opamp U21, from page 15 of the schematics – Appendix A.1. This node is bypassed with a 10 μF capacitor. In the best case scenario, with the 10 kΩ potentiometer in the middle position, the cut off frequency would be equal to $1/(RC) = 20$ Hz. Figure 4.10 shows the result of bypassing this two points with 1mF capacitors, leaving the DC



(a) (b)

(c) (d)

Figure 4.8: Probing the noise along the receiver opamp chain. Time: 1s/Div. The red trace corresponds to the math function used to try to approximate one of the channels by scaling the other. (a) ZC706EVM and PCB (b) Ch1 (yellow): receiver input – 5 mV/Div Ch2 (blue):output of the second stage (2nd opamp) – 200 mV/Div (c) Ch1 (yellow): output of the second stage (2nd opamp) – 500 mV/Div Ch2 (blue):output of the first stage (1nd opamp) – 10 mV/Div Math (red)=Ch2$\times(-69)$ – 6 –500 mV/Div (d) Ch1 (yellow): output of the third stage (3rd opamp) – 2 V/Div Ch2 (blue):output of the second stage (2nd opamp) – 50 mV/Div

offset regulator and the voltage reference for the current source with a cut off frequency of $\sim$0.2 Hz and $\sim$2 Hz respectively. The peak to peak noise level is now close to 2 Vpp, which is equivalent to an input referred voltage noise of 336 μVpp. Although this improves the performance, the noise level is still to high. It should be noted that despite the current source filter being placed in figure 4.10a the noise analysis performed still ignores its effect as there is no load.

To further improve the noise performance these capacitors were removed and two low noise voltage references were added.

In the case of the current source, a fixed reference is sufficient since its function is to replace a fixed voltage divider. The voltage needed by this node is 750 mV. This was achieved by applying a resistive voltage divider to the LM4140ACM-1.2 [51] voltage reference output. The

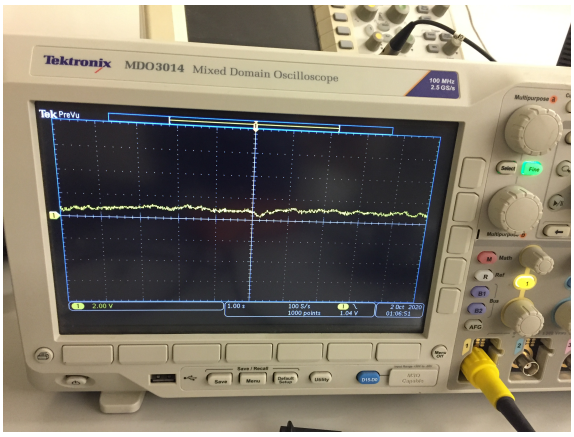
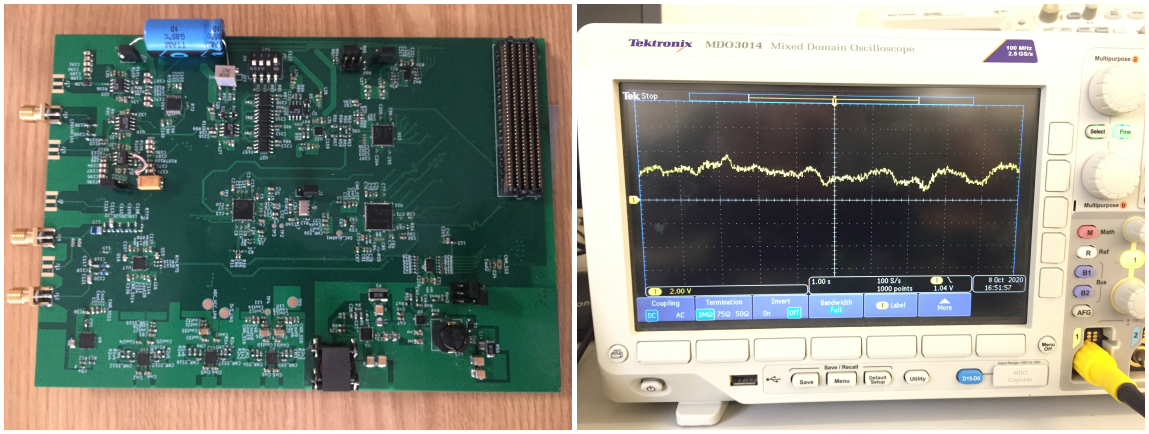


Figure 4.9: Noise level detected in the receiver module at the output of the third stage (opamp chain) with the module input short to ground: 1 s/Div 2 V/Div

LM4140ACM-1.2 is a 1.25 V reference with a voltage noise (0.1 Hz to 10 Hz) of 2.2 μVpp and low drift. The voltage divider was made with a 0.1% 604 Ω and a 0.1% 402 Ω resistor. The output of the the divider was bypassed with a 1 μF capacitor. The circuit for the voltage reference is shown in the first typical application from its datasheet [51] plus the resistive voltage divider discussed before. This circuit was soldered in an adapted veroboard that was connected to the PCB, as shown in figure 4.12a.

The DC offset regulator, on the other hand, needs to be adjustable. The circuit used for this regulator is described in figure 4.11. The potentiometer and the bypass capacitors connected to Vout belong on main the PCB. The rest of the circuit was also implemented on a veroboard. The voltage regulator used in this circuit is the LT6654 [52] and the opamp is the OPA735 [53]. The implemented circuit is shown in figure 4.12a.

The voltage noise after adding the voltage references is shown in figure 4.12b. This value is close to 1 Vpp which is similar to the one seen in figure 4.9, resulting in a similar performance. A noise level of ∼167 μVpp gives an resolution of ∼6 divisions per mV, which despite being much less than the expected is still enough to work as a detector, as the input signal expected is in the order of several mVs. Further improvement may be possible by applying the 1mF capacitors to these nodes and by changing the values of the feedback resistors from the opamp responsible for the current source, as discussed in 3.5.1.



(a) (b)

Figure 4.10: (a)Adding two 1mF capacitors to the critical points (b) noise performance after applying the bypass capacitors measured in the receiver module at the output of the third stage (opamp chain)– Time 1s/Div Ch1: 2 V /Div

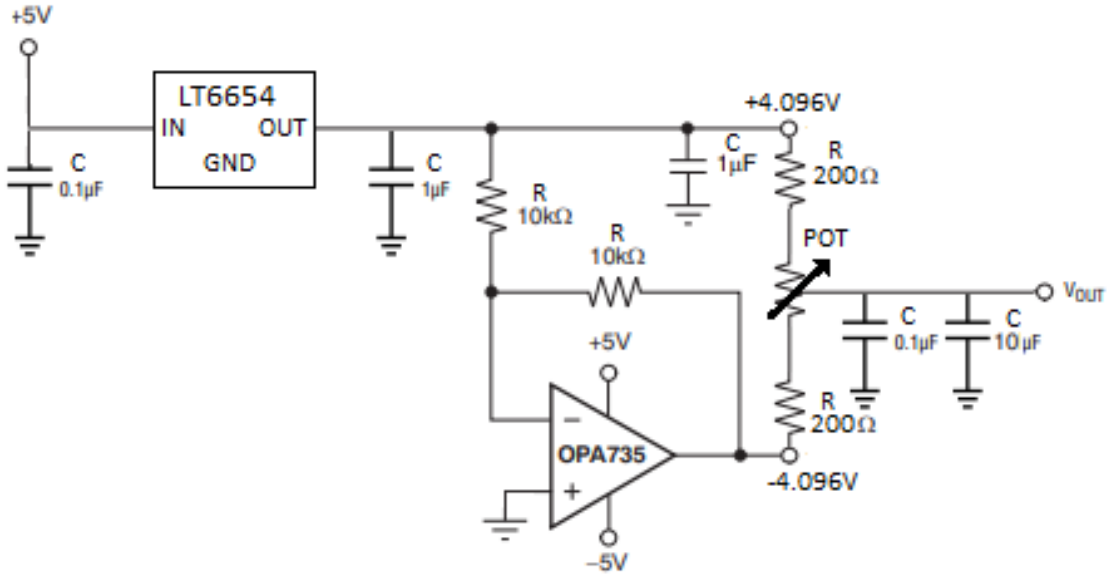
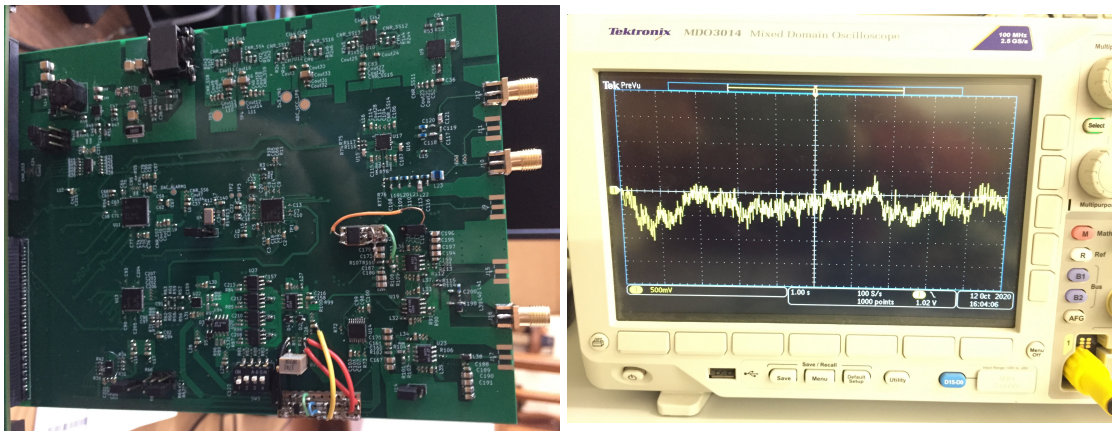


Figure 4.11: Circuit for implement for the DC offset regulator based on a voltage regulator – adapted from [52, 54].



(a) (b)

Figure 4.12: (a) Adding two voltage references to the critical points. (b) Noise performance after applying the references measured in the receiver module at the output of the third stage (opamp chain)– Time 1s/Div Ch1: 500 mV /Div.

4.1.2 Transmitter

In this section, the modulation capability of the transmitter will be analysed, now with the PCB assembly completed. In other words the output filters from table 3.5 are included. To perform this analysis, a 25 Ω load was applied to the current source from the transmitter.

The following Python script creates the amplitude modulated square wave used to perform this test.

```
import numpy as np

def square_wave2(samples,MAX,MIN,FS,f):
    N=int(FS/f)
    np.random.seed(10)
    sq_wv = (MAX-MIN)*np.random.rand(int(samples/N))+MIN
    sq_wv = sq_wv.astype(int)
    sq_wv = sq_wv.repeat(N)

    rise_fall_n = int(np.ceil(N/10))
    t=np.linspace(0,1,rise_fall_n+1)

    for x in range(N-1,samples-N,N):
        sq_wv[range(x-1,x+rise_fall_n)]=np.interp(t,[0,1],[sq_wv[x],sq_wv[x
            +1]])

    return sq_wv

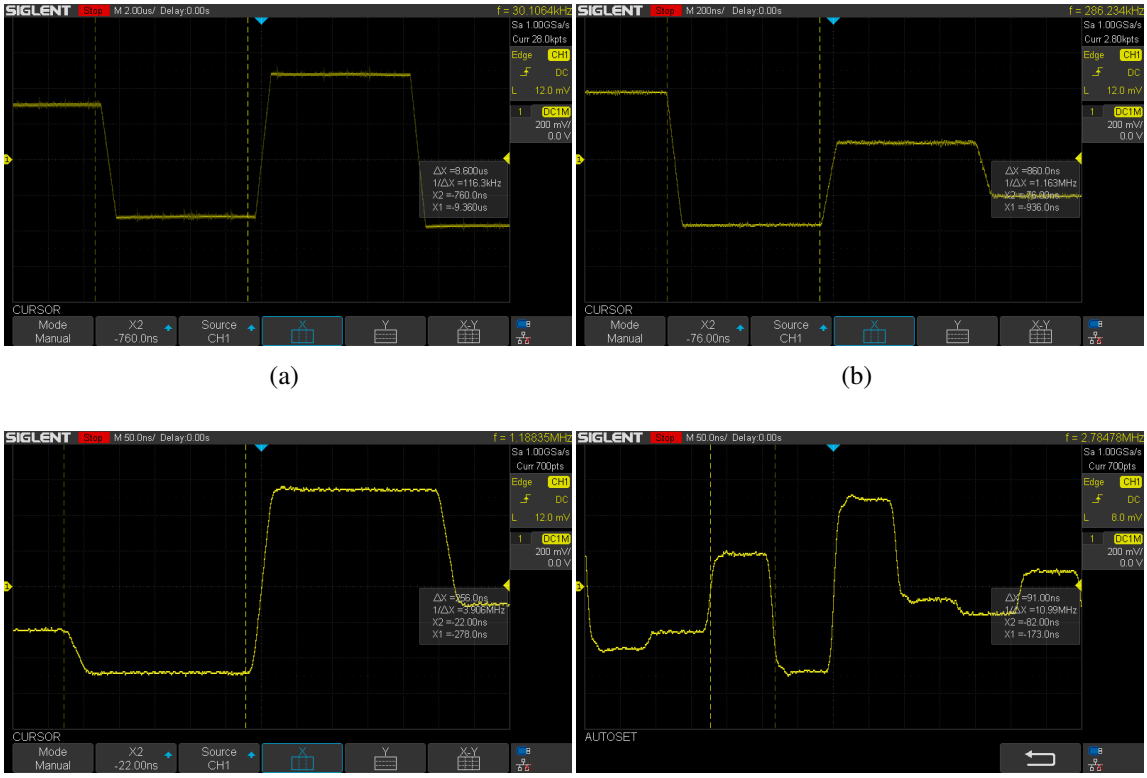
#sq_wv
samples=int(1e6)
FS=125e6
f=int(FS/100)
data = square_wave2(samples,-8100,8100,FS,f)
```

Listing 4.2: Python script used to generate a random square wave modulated in amplitude in rise/fall time equal to 1/10th of the period

This square wave is saved on the variable "data" which is an array with 1M (optional) integers. This array was sent, during execution time, to the ZYNQ via TCP/IP. An instruction to start a transfer from the application layer to the ZYNQ fabric logic using the AXI DMA in cyclic mode was also sent with the array. These means that the DAC will be receiving a continuous stream of data.

The frequency, f, corresponds to the symbol rate, which is double the frequency of a square wave. In this case the amplitude range was set to $-8100 - 8100$, approximating the full scale of the DAC. FS is the sampling frequency of the DAC (=125 MSPS). Setting the rise and fall time to 1/10th of the symbol time reduces the spectrum of a square wave and eliminates the ringing created by filtering high frequency transitions.

The results obtained for symbol rates (f) of FS/1000=125 kHz, FS/100=1.25 MHz, FS/30=4.17 MHz and FS/10=12.5 MHz can be seen in figure 4.13. With these results one can conclude that the computer is able to successfully modulate a 25 Ω load in real time. The voltages imposed on the load by the current source cover the voltage range that each MTJ can support (±0.5 V).



(a) (b)

(c) (d)

Figure 4.13: Transmitter current source modulating a 25 Ω load (a) Symbol rate: 125kSPS Time:2 µs/Div Ch1:200 mV/Div. (b) Symbol rate: 1.25 MSPS Time:200ns/Div Ch1:200 mV/Div. (c) Symbol rate: 4.17 MSPS Time:50ns/Div Ch1:200 mV/Div (d) Symbol rate: 12.5 MSPS Time:50ns/Div Ch1:200 mV/Div.

4.1.3 Receiver

In this section the capabilities of the receiver will be briefly presented and some results captured by the receiver will be discussed.

At the moment the application running on the ZYNQ can be commanded by the computer to capture and send frames, over TCP/IP, with 1,048,575 samples, which corresponds to ∼8.3ms at 125 MSPS. The number of samples from a frame can be easily changed. As an example, for a 500MB buffer holding 4 byte samples (int) at 125 MSPS each frame would represent ∼1s. The AXI DMA cyclic mode was not implemented for the receiver. Both current sources from the receiver can also the programmed. Figure 4.14 shows the interface used to capture data. The user as access to a real time plot of the ADC output and can update the the current sources in real time. This plot has an average update rate of 9 samples/s and is made by averaging multiple frames. Its

purpose is to help the user to regulate both the bias points and the DC offset regulator. The user can then save single 8.3ms frames to files for posterior analysis.

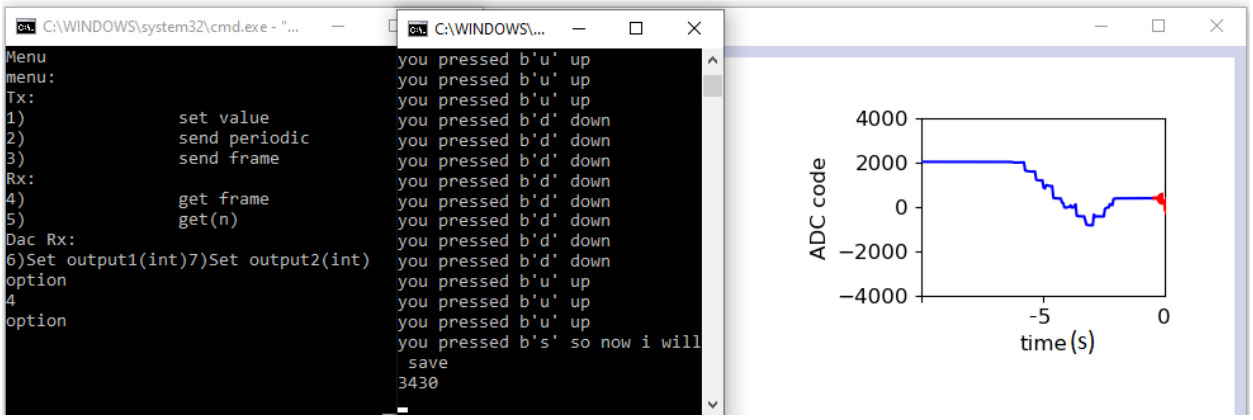


Figure 4.14: Computer Interface: Scope (time(s)) and MTJ current source modulation.

To test the ADC performance the receiver was connected to a 50 Ω signal generator. Segments of the captured data for different inputs can be seen in figure 4.15. The receiver selective gain resistor selected was 8 kΩ, resulting in a gain of 35.6 dB. The filter losses do not apply to the gain calculation since the input power takes in consideration a 50 Ω load. The selected gain will transform a 32 mVpp input signal to the full scale of the ADC (2 Vpp). Figure 4.15b shows the noise level on a captured frame by the ADC. Assuming that the peak to peak noise corresponds to 22 codes, and that the full scale corresponds to 32 mV, then the noise level is 0.17 mVpp.

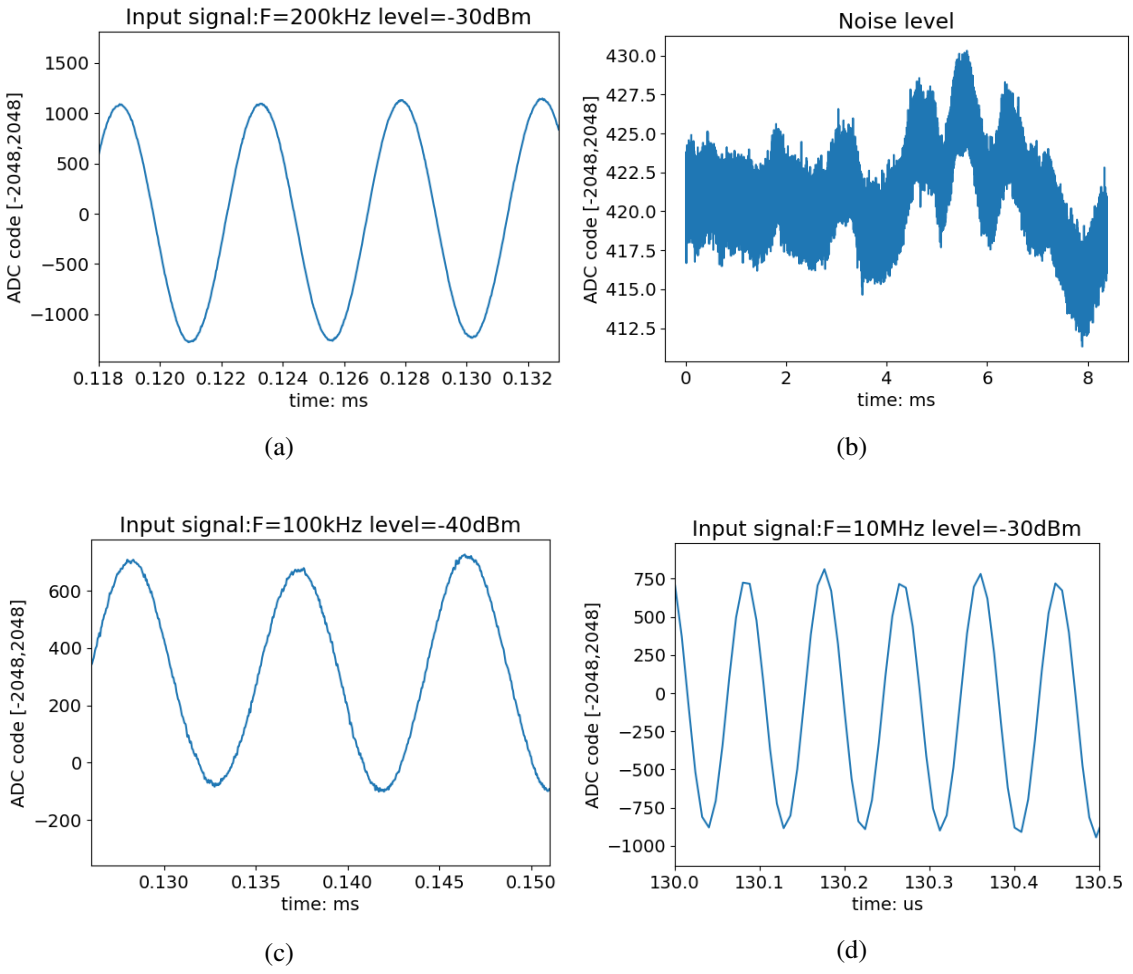


Figure 4.15: Data captured by the ADC for various frequencies and input power: selected gain resistor=8 kΩ, total gain = 35.9 dB, ADC scale: integer from -2048 to 2048 (a) F=200 kHz input signal = -30 dBm. (b) Detected noise level on a 8.3ms frame. (c) F=100 kHz input signal = -40 dBm (d)F=10 MHz input signal = -30 dBm.

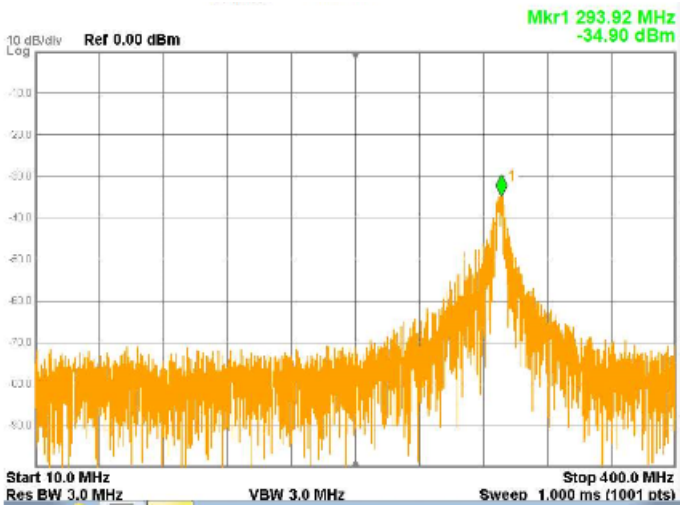
Table 4.1: State of the first STVOs wire bonded (version 1).

Oscillator	MTJ	FL	Peak Power dBm	Bandwidth (f2-f1) (MHz)	Fc (MHz)	Resistance	obs
1	ok	ok	-	-	-	∼25 Ω	-unable to get stable oscillation
2	dead	ok	-43	10	242	43 Ω	
3	dead	ok	-34	30	285	25 Ω	BW obtained via the FL
4–6	not connected	-	-	-	-	-	
7	ok	not connected	-	-	-	∼25 Ω	-unable to get stable oscillation
8	ok	not connected	-35	13	244	22 Ω	-hard to replicate

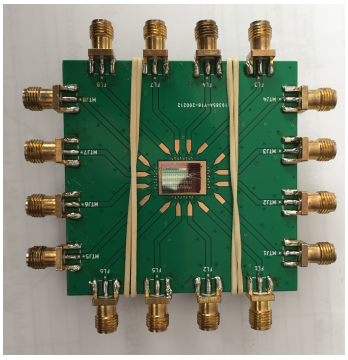
4.2 Testing the STVOs

Having received the PCB containing the STVOs from INL some preliminary tests were done. All the tests involving the STVOs where made at INESC TEC. The STVOs bonded to the carrier PCB were from version 1, table 3.1. The preliminary tests were based on the circuit depicted in figure 2.10a, and consisted on using a spectrum analyzer to detect oscillations from the STVOs. Applying a current to the MTJ from the STVOs may produce a voltage oscillation. These oscillations are depicted as peaks in the spectrum analyzer. The first objective was to find a stable oscillation by applying a current, using a voltage source and a bias T, and changing the magnet position. Once that was achieved, the current was changed around that value. The MTJ should exhibit different frequencies for different currents, so changing the current allows to see the maximum range in frequency that a specific peak can be shifted before it disappears. Figure 4.16c shows the magnet applied behind the PCB (figure 4.16b). Figure 4.16a shows the a peak obtained for the STVO number 3. This peak appears at 294 MHz with a value of −35 dBm. Some additional tests where made by applying a current on the field line, hence the two power supplies from figure 4.16d. Despite modulating the field line offering some advantages, such as, achieving a higher modulation rate and having a fixed resistance, it was not the main focus of this thesis. The best results obtained for these STVOs are shown in table 4.1. Several of the connections are represented as not connected indicating that the bond broke loose. Some MTJs are represented as dead, meaning that either a short circuit or an open circuit is detected when applying a signal. In both cases (not connected/ dead) they are indicated by the red background colour, as they can not be used. The values indicated in this case refer to the best performance obtained before they were damaged. The oscillators represented in orange are functional although only temporary peaks were detected in the spectrum analyser. The only STVO left is the number 8. This one was working. At this stage INL offered to rebond the MTJs. The STVOs were replaced by STVOs from version 1.2 (table 3.1).

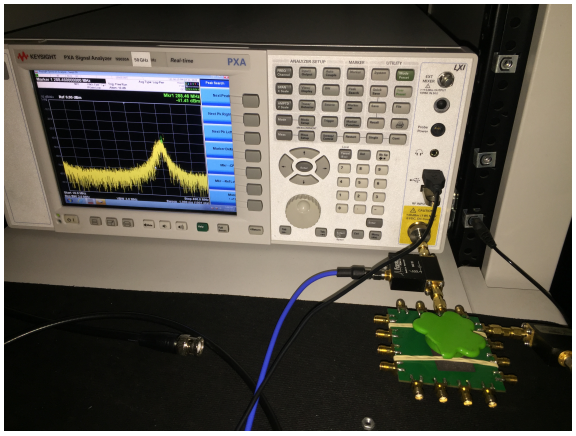
A similar analysis was performed to the new STVOs. The results can be seen in table 4.2.



(a)



(b)



(c)



(d)

Figure 4.16: Testing the STVOs (version 1) wirebonded. (a) Spectrum of the STVO 3: Voltage applied to the MTJ=0.327 V. (b) PCB used. (c) PCB with magnet connected to a spectrum analyser. (d) Test Equipment.

The outputs from the STVOs 1,5 and 6 were then analysed in an oscilloscope. The oscilloscope, besides allowing to visualize the waveform also performs some statistical inferences such as mean and standard deviation for both peak to peak voltage and frequency. The results for this analysis are shown in table 4.3. The STVO 1 was analyzed in a similar manner to the previous ones, just replacing the spectrum analyzer by the oscilloscope. For STVOs 5,6 the setup was changed, this time, instead of using the lab power supply and bias T to bias the MTJ, the implemented transmission system was used. This setup can be seen in figures 4.17b and 4.17c. A waveform from STVO 6 is displayed in figure 4.17a.

The discrepancy in power level for similar frequencies, that can be seen comparing the data from these 3 STVOs to the data obtained with the spectrum analyser, does not have a significant meaning. The tests from the spectrum analyzer were optimized to show the highest peak possible

Table 4.2: State of the STVOs (version 1.2).

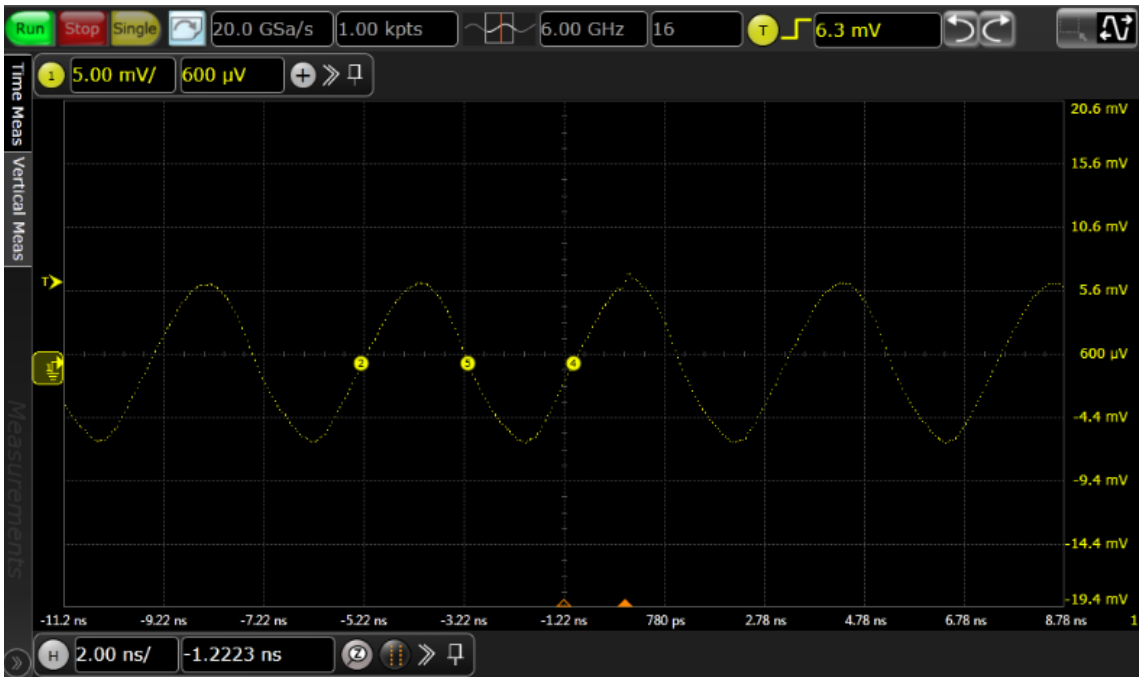
Oscillator	**MTJ**	**FL**	**Peak Power**	**Bandwidth (f2-f1)**	**Fc**	**Resistance**
1	ok	ok	-31.8 dBm	7 MHz	251 MHz	38
5	ok	ok	-33.4 dBm	9 MHz	249 MHz	45
6	ok	ok	-29.6 dBm	-	239 MHz	37
8	ok	ok	-35 dBm	5 MHz	233 MHz	34

in the frequency range indicated by table 4.2. Both the difference in power level and frequency can be explained by a change in the DC current applied and the magnet position.

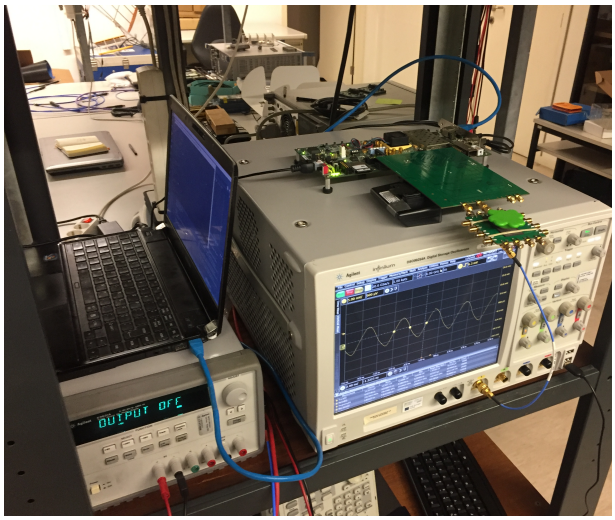
Table 4.3: Statistical measures from the STVOs.

Oscillator	Vpp mean	Vpp std	F mean	F std	Current/DAC code	Power
1	12.740 mV	126 μV	254.010 MHz	1.276 MHz	8 mA/ -	-33.9 dBm
	19.817 mV	170 μV	225.410 MHz	595 kHz	9 mA/ -	-30.1 dBm
5	12.453 mV	122 μV	234.051 MHz	457 kHz	7 mA / 2900	-34.1 dBm
6	13.197 mV	58 μV	236.166 MHz	606 kHz	10 mA/3500	-33.6 dBm

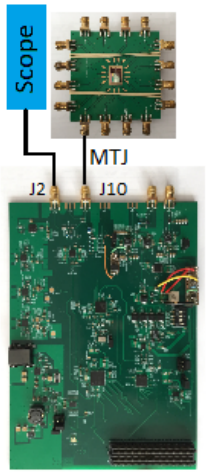
DAC code is an integer in the range -8192–8192, corresponding to a voltage of -2 V – 2 V in series with a 50 Ω resistor and the load



(a) Waveform from STVO 6 for the DAC code 3500 corresponding to 0.364 mV and 10 mA on a 37 Ω load.



(b) Setup used in (a).



(c) Connections required.

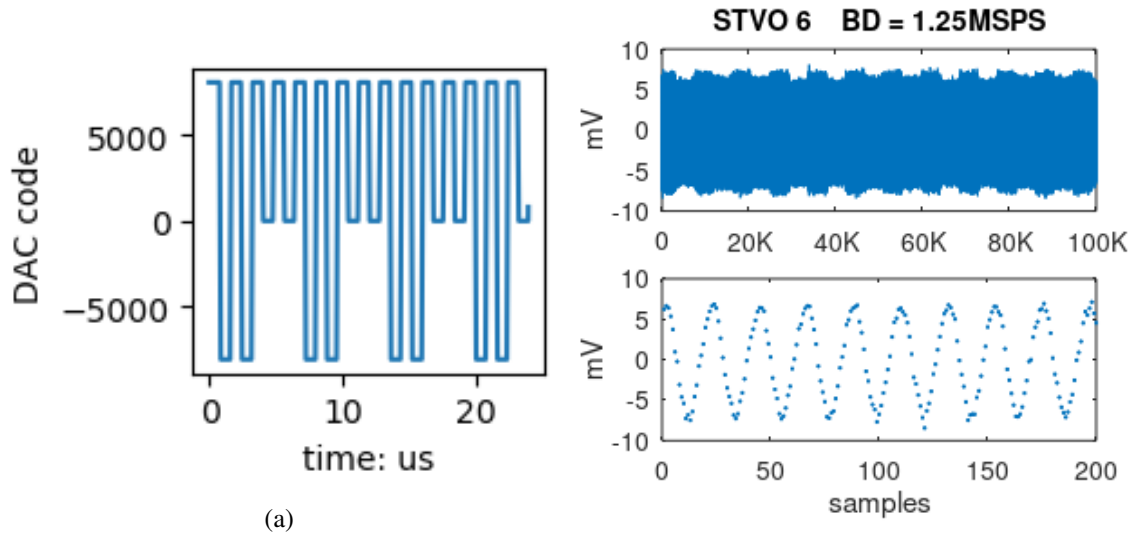
Figure 4.17

4.2.1 Transmitter: STVO modulation

In this section the results of modulating the STVOs with the implemented PCB will be discussed. The transmitter system performance will be analysed independently of receiver. The setup used is still the setup from figure 4.17b, as it allows to optimize the magnet position and the voltage range in which the STVOs would work as oscillators. The data was captured and saved using the oscilloscope for analysis.

Previously, to test the DAC modulation capability, the square wave generated by the code from listing 4.2 was used. For the current test, the code was changed to create a waveform with only three levels, maximum, minimum, and middle, alternating as depicted in figure 4.18a. The amplitude and symbol rate are tunable in real time. The rise and fall time from this wave is 1/10th of the sample time. Figure 4.18b shows an example of the data captured by the oscilloscope when modulating the MTJ of STVO 6.

The amplitude of the square wave selected for each capture was based on the maximum shift in frequency detected. Figure 4.19 shows spectrograms of the data captured in a similar way for STVOs 5 and 6. The plots shown are from data captured at 5 GSPS and, with the exception of 4.19d, demonstrate a successful implementation of a FSK system containing 3 symbols. A maximum symbol rate of 1.25 MSPS was obtained for both STVOs. For symbol rates higher or equal to 1.25 MSPS additional captures were performed at 20 GSPS, although, no significant difference was detected. Both STVOs presented a maximum shift in frequency close 5 MHz. Based on figure 4.19e, the spectral width at -3 dB from the peak value of the STVO 6 with a symbol rate of 1.25 MSPS is close to 2 MHz. These figures also show linearity between the current applied and the output frequency.



(a) (b)

Figure 4.18: (a) Example of the signal used to modulate the MTJs. (b) Data from STVO 6 captured with the oscilloscope at 5 GSPS. Signal: min,max DAC code = 3500,4000.

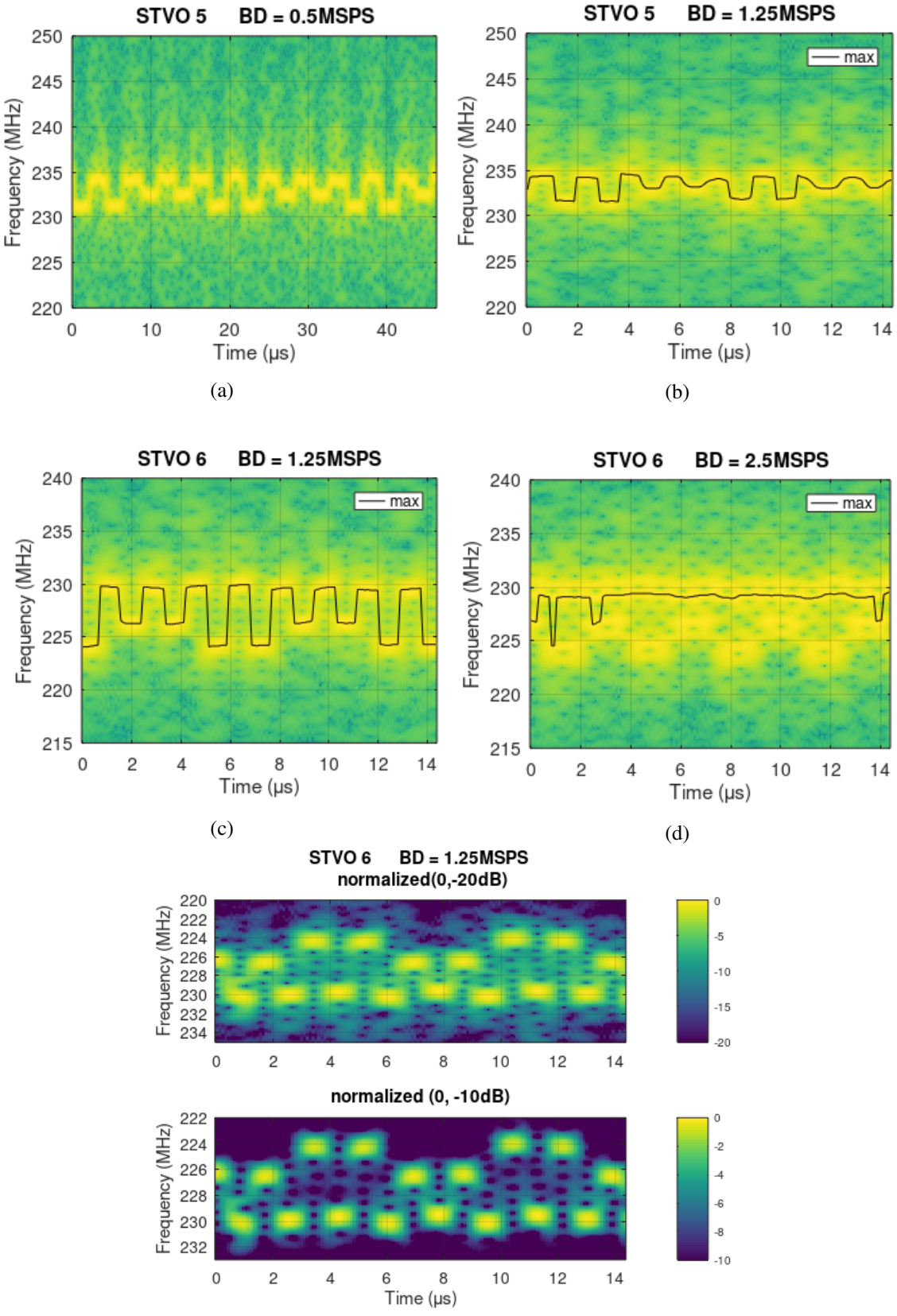
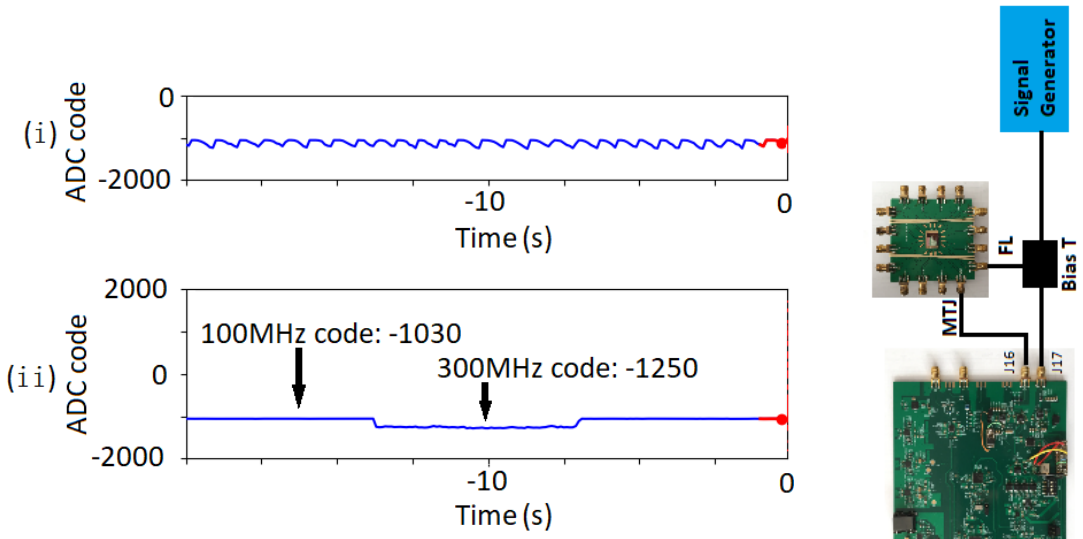


Figure 4.19: Spectrograms of the data captured by the oscilloscope for different symbol rates. This data was captured at 5 GSPS. The black line represents the maximum value of the spectrogram. (e) Shows a section of the normalized data from 0 to -10 dB/-20 dB for STVO 6 at 1.25 MSPS.

4.2.2 Receiver: frequency sensor based on a STVO

This section aims to show the data captured by the receiver system of the PCB implemented. Figure 2.11 shows the basic circuit needed to use a STVO as a frequency sensor and the basic principle of a frequency sensor. Under certain conditions, the "sinusoidal" oscillation of the resistance in the MTJ will get distorted creating an average resistance different from 0. A constant current flowing through the MTJ creates a voltage, that upon filtering will create a "DC" signal. To create an distorted oscillation a DC current is applied on the field line antenna, displacing the vortex core closer to the boundary of the nanopilar. If the filtered signal presents, for example, a linear dependence on the frequency of the RF signal also applied to the field line, it can be used as a frequency sensor. Figure 4.20b shows how the implemented PCB and a STVO should be connected to create a frequency sensor. The PCB provides two current sources, one to bias the field line and other, that includes a low pass filter and a path for the signal to both bias the MTJ and provide the averaging necessary. The input RF signal is ac coupled to the field line through an external Bias T.The current source that bias the field line is based on a inductor, so, connecting it to a bias T only increases the impedance. The user needs to set a bias point for both current sources and regulate the DC offset via the DC offset regulator included in the PCB so that the input does not saturate the ADC input.

Figure 4.20a shows some data captured by the receiver. The plot (ii) corresponds to two steps in frequency changing the signal generator from 100 MHz to 300 MHz and back to 100 MHz. The difference represents 1.97 mV detected at the receiver input. Plot (i) shows multiple continuous sweeps from 100 MHz to 300 MHz with a step back to 100 MHz. From this plot it appears that, for this specific bias point, the receiver is working as a frequency sensor, as there is a linear section detectable in each sweep. This specific state was not repeatable, hence it is only useful as a demonstration. The difficulty off establishing a bias point suitable for a frequency sensor comes in part due to the lack of feedback. As an example, for the transmitter, when connected to an oscilloscope/spectrum analyzer, sweeping the magnet across the back of the carrier PCB will create a detectable signal, such as a smaller oscillation/peak that allows the user to close in on a specific local optimum, by carefully moving the magnet. On the other hand, the receiver requires an additional signal to be applied, such as a step or sweep in frequency before either the change in currents or the magnet position. Additionally, the effects of moving the magnet on the back of the PCB containing the STVOs detected by the implemented receiver system can be seen in figure 4.21. As such, a continuous movement of the magnet as a feedback mechanism to find a to working bias point is difficult.



(a) (b)

Figure 4.20: (a) Real time capture using the ADC and STVO 1, selective gain resistor = 8 kΩ, ADC scale integer from -2048 to 2048, full scale = 32 mV, signal generator output power = 4 dBm, $I_{Bias,FL}$ = 40 mA established with a power supply and $I_{Bias,MTJ}$ = 8 mA setting DAC_RX output1 to 0xBAFC (DC voltage at load =0.293 V) Time scale: 2.5 s/Div, with an average of 9 samples per second (i) Signal generator several frequency sweeps 100 MHz–300 MHz. (ii) Detected ADC codes for input frequencies of 100 MHz and 300 MHz. The difference in codes corresponds to 1.97 mV at the MTJ output.

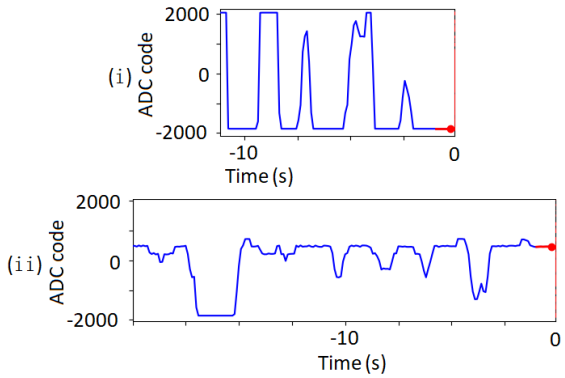


Figure 4.21: Influence of the magnet position on the STVO 1 working as a receiver. Real time data captured by the ADC

Chapter 5

Conclusion and Future Work

This thesis aimed to developed and characterize a system, compatible with real world applications, capable of using STVOs as MFSK transmitters and receivers.

The first step to achieve said system was the implementation of a simple electrical model that captured several functional characteristics of the STVOs, based on preexisting data. This step was followed by the design and simulation of analog modules capable of integrating the nano-oscillators and capable of modulating/demodulating them. To interact with the analog modules the feasibility to implement a subsystem based on analog to digital / digital to analog data conversion was analyzed. The main purpose of this subsystem was to allow the whole analog system to be controlled via TCP/IP. Upon a successful design and verification of the system the next step was the implementation based on printed circuit boards, a computer and the ZC706 evaluation board.

The use of STVOs as components in RF transmitters and receivers eliminates the need to use traditional electronic elements such as frequency mixers, local oscillators, PLLs and more complex systems such as multiple single frequency detectors. A transmitter based on the STVOs provided can have an output power as high as -30 dBm. Under certain conditions, their output frequency can be almost linearly dependent on an input current. One possible configuration for a receiver based on a STVO (frequency sensor) is characterized by translating an input frequency directly to a voltage level. This type of receiver requires an high input power, typically higher than 0 dBm.

5.1 Objectives Satisfaction

The following objectives were satisfied:

- Design, simulation and implementation of a system capable of providing a computer the ability to control a transmitter and a receiver based on STVOs.

- A transmission system based on FSK modulation achieved by modulating single STVOs, provided by INL, was demonstrated using 3 symbols at a maximum symbol rate of 1.25 MSPS for frequencies between 220 MHz and 235 MHz.

- A receiver with a noise level of 0.17 mVpp (-71 dBm) over a 10 MHz bandwidth, capable of operating for frequencies between DC and 10 MHz was also successfully implemented and tested. This receiver was used to demonstrate the frequency sensor behaviour on a STVO, although it was not possible to achieve a stable and repeatable operating point to be able to further characterize the receiver.

5.2 Future Work

At the moment of this analysis there are a few known problems/possible future upgrades.

Regarding the developed board the possible future upgrades are:

- noise reduction based on changing the resistors of the receiver current sources, as discussed in section 3.5.1,
- integrate the voltage references on a future redesign of the board,
- add an AC coupling option to eliminate 1/f noise,
- relocate the potentiometer to a more practical position
- use the bottom layer to reallocate the power supply LDOs closer to the ICs,
- consider upgrading the DC offset regulator to a digital one.

Regarding the developed software, in particular the interface for the receiver should be upgraded providing the user a interface closer to a digital oscilloscope, such as, changing both the time and voltage scale in real time and provide a trigger mechanism, allowing for a simpler mechanism to characterize the frequency sensor.

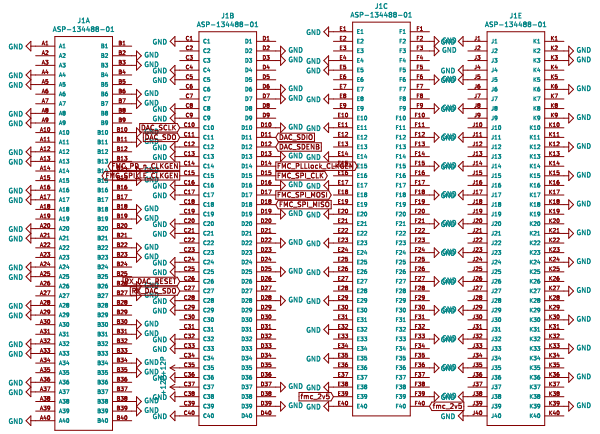
To improve the transmitter system it is possible to increase the number of symbols, and ideally to find a larger frequency band in which the STVOs operate as oscillators.

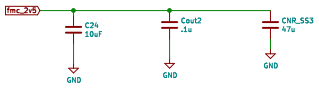
Finally, to achieve a complete communications system it is necessary, either to use two different carrier boards for the same type STVOs used in this thesis, allowing for two different magnet positions so that both the receiver and transmitter can be used simultaneously or replace the STVOs to the STVOs from version 2 (table 3.1).

Appendix A

Board Schematic

A.1 Board Schematic

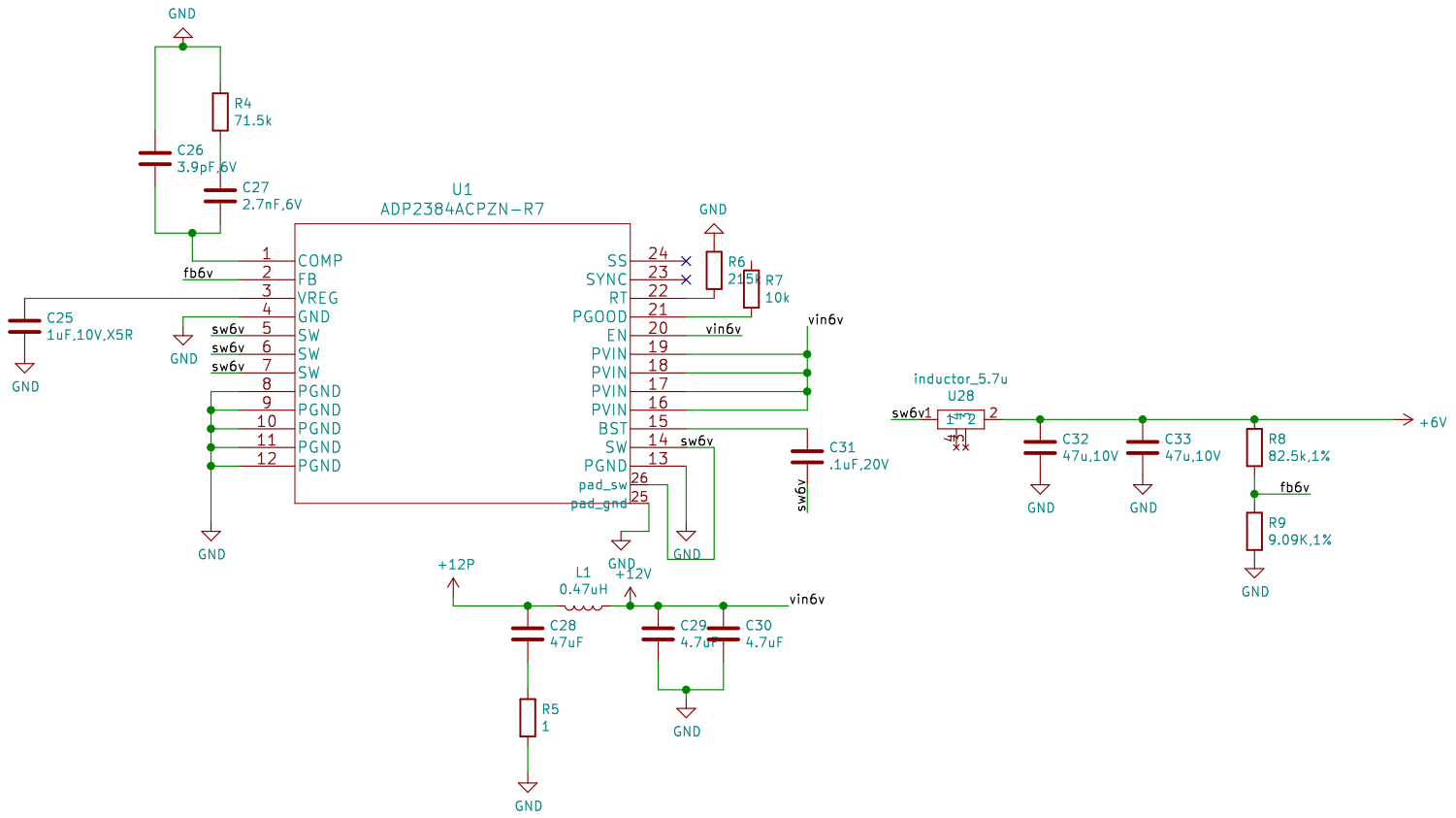




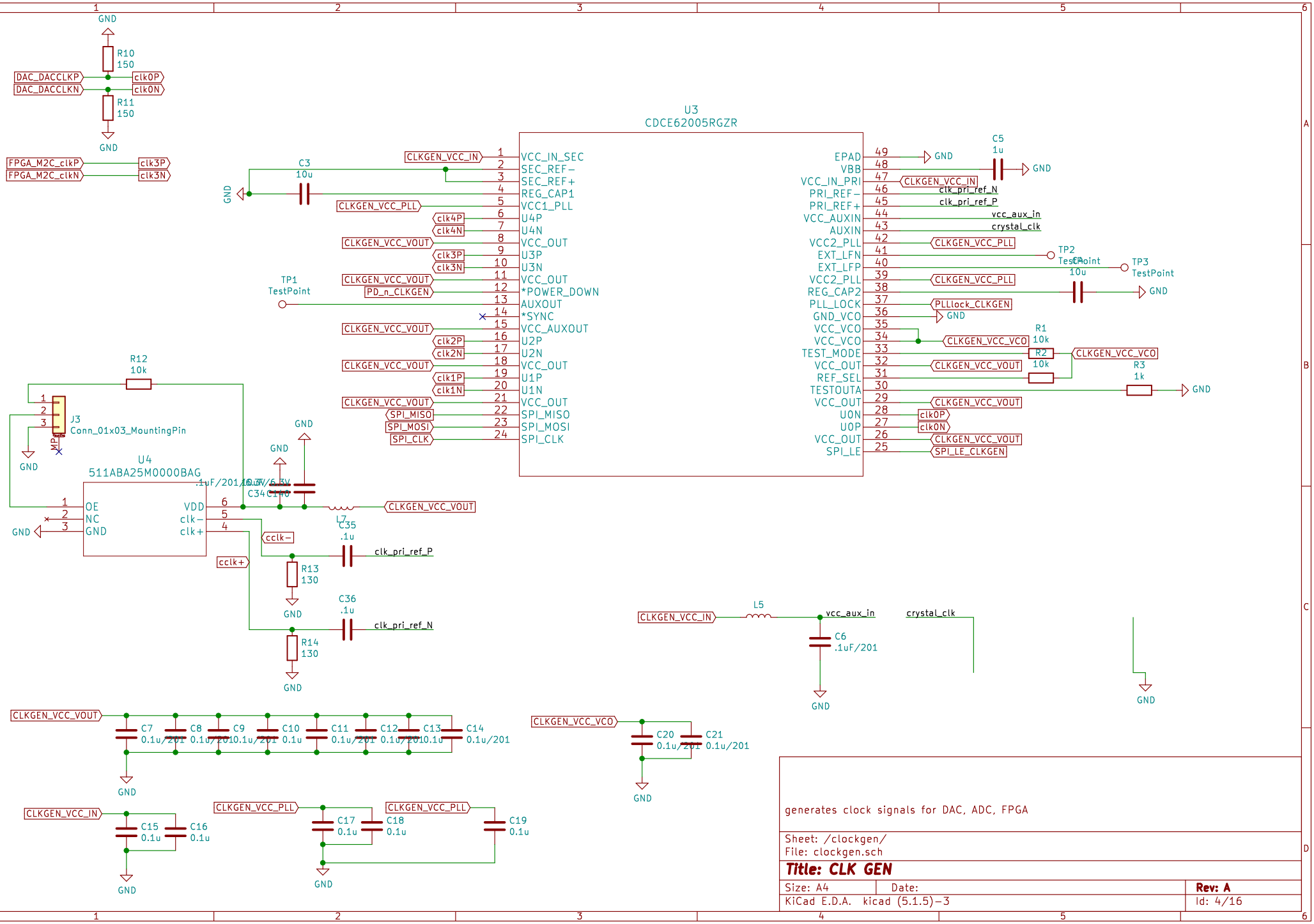
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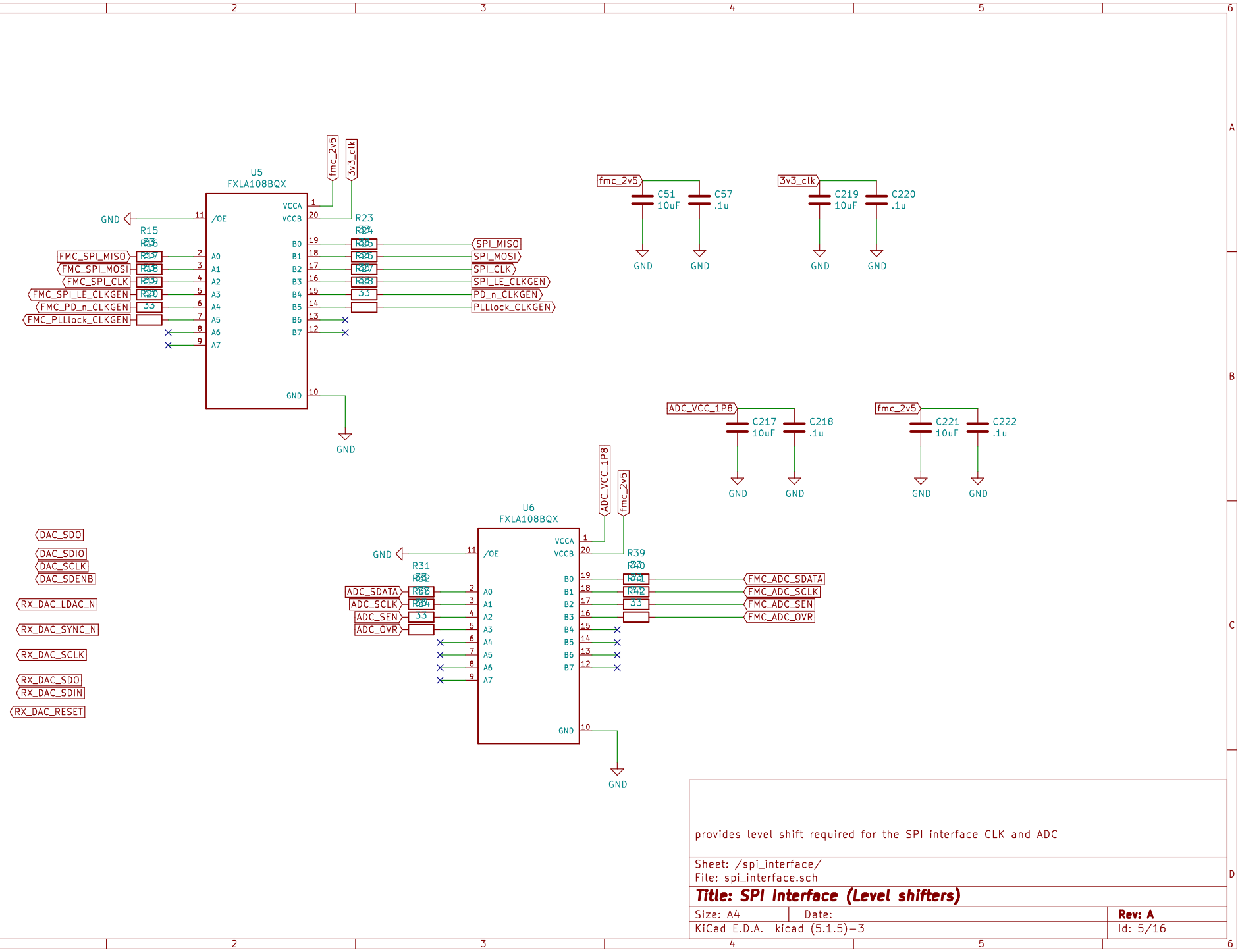
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DAC_DACCLKN
clk0P
clk0N
R11
150
GND
FPGA_M2C_clkP
FPGA_M2C_clkN
clk3P
clk3N
U3
CDCE62005RGZR
CLKGEN_VCC_IN
VCC_IN_SEC
SEC_REF−
SEC_REF+
REG_CAP1
CLKGEN_VCC_PLL
VCC1_PLL
clk4P
U4P
clk4N
U4N
CLKGEN_VCC_VOUT
VCC_OUT
clk3P
U3P
clk3N
U3N
CLKGEN_VCC_VOUT
VCC_OUT
PD_n_CLKGEN
*POWER_DOWN
AUXOUT
*SYNC
CLKGEN_VCC_VOUT
VCC_AUXOUT
clk2P
U2P
clk2N
U2N
CLKGEN_VCC_VOUT
VCC_OUT
clk1P
U1P
clk1N
U1N
CLKGEN_VCC_VOUT
VCC_OUT
SPI_MISO
SPI_MISO
SPI_MOSI
SPI_MOSI
SPI_CLK
SPI_CLK
EPAD
VBB
VCC_IN_PRI
PRI_REF−
PRI_REF+
VCC_AUXIN
AUXIN
VCC2_PLL
EXT_LFN
EXT_LFP
VCC2_PLL
REG_CAP2
PLL_LOCK
GND_VCO
VCC_VCO
VCC_VCO
TEST_MODE
VCC_OUT
REF_SEL
TESTOUTA
VCC_OUT
U0N
U0P
VCC_OUT
SPI_LE
C3
10u
TP1
TestPoint
C5
1u
CLKGEN_VCC_IN
clk_pri_ref_N
clk_pri_ref_P
vcc_aux_in
crystal_clk
CLKGEN_VCC_PLL
TP2
TestPoint
TP3
TestPoint
C4
10u
CLKGEN_VCC_PLL
PLLlock_CLKGEN
R1
10k
R2
10k
CLKGEN_VCC_VCO
CLKGEN_VCC_VOUT
R3
1k
CLKGEN_VCC_VCO
CLKGEN_VCC_VOUT
clk0P
clk0N
CLKGEN_VCC_VOUT
SPI_LE_CLKGEN
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J3
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OE
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VDD
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clk+
C34
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C1+0
L7
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cclk−
cclk+
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C36
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R14
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vcc_aux_in
crystal_clk
C6
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C21
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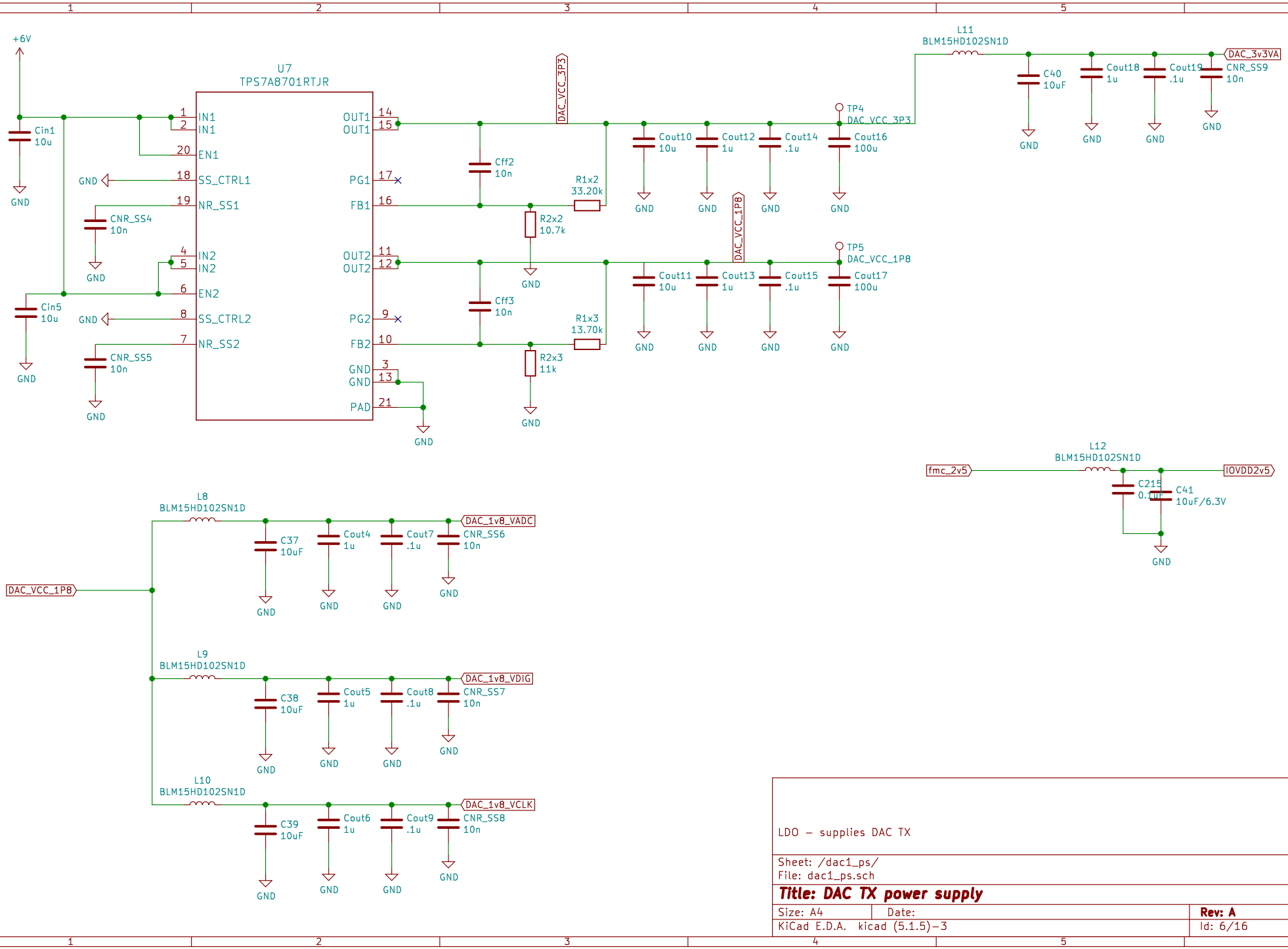


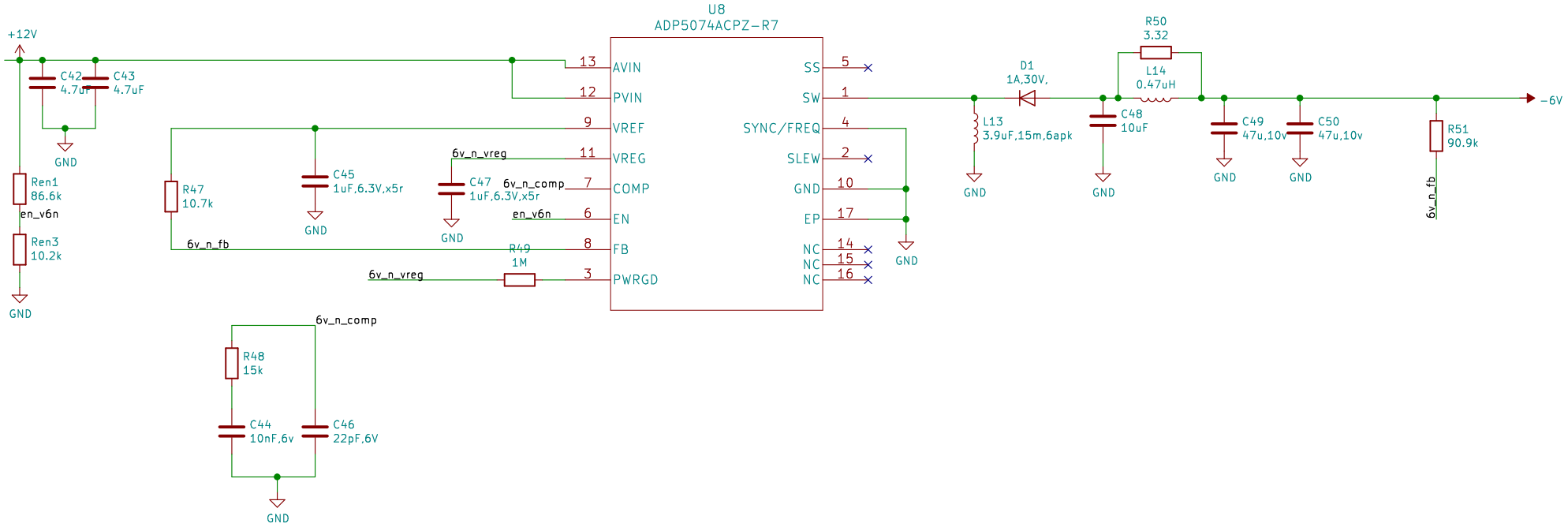
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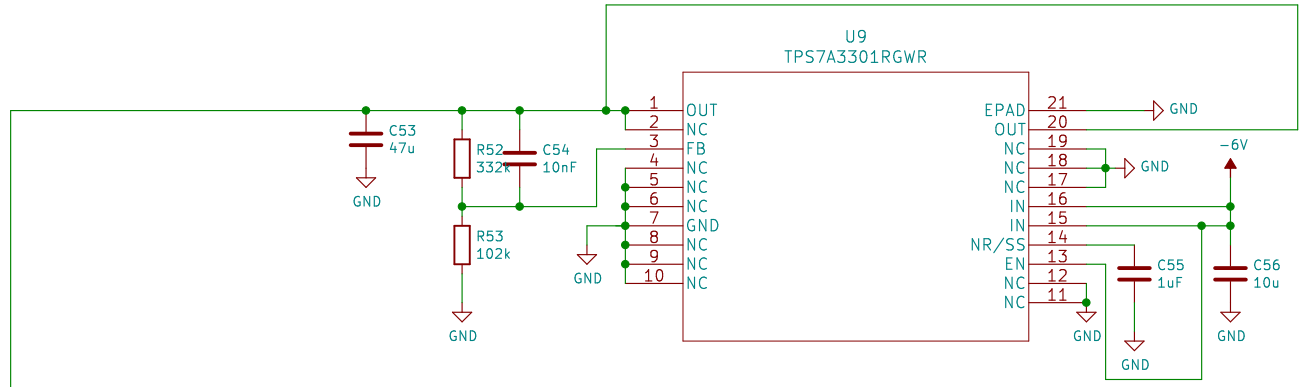
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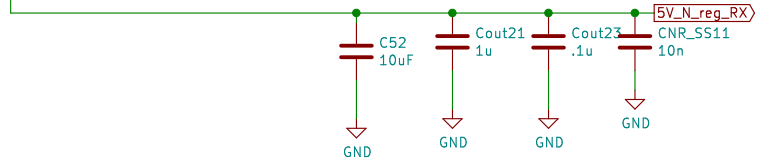

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EN1
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NR_SS1
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EN2
SS_CTRL2
NR_SS2
CNR_SS4
10n
Cin5
10u
CNR_SS5
10n
OUT1
OUT1
PG1
FB1
OUT2
OUT2
PG2
FB2
GND
GND
PAD
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33.20k
R2x2
10.7k
DAC_VCC_1P8
Cff3
10n
R1x3
13.70k
R2x3
11k
Cout10
10u
Cout12
1u
Cout14
.1u
Cout16
100u
TP4
DAC_VCC_3P3
Cout11
10u
Cout13
1u
Cout15
.1u
Cout17
100u
TP5
DAC_VCC_1P8
L11
BLM15HD102SN1D
C40
10uF
Cout18
1u
Cout19
.1u
CNR_SS9
10n
DAC_3v3VA
L12
BLM15HD102SN1D
fmc_2v5
IOVDD2v5
C215
0.1uF
C41
10uF/6.3V
L8
BLM15HD102SN1D
DAC_VCC_1P8
C37
10uF
Cout4
1u
Cout7
.1u
CNR_SS6
10n
DAC_1v8_VADC
L9
BLM15HD102SN1D
C38
10uF
Cout5
1u
Cout8
.1u
CNR_SS7
10n
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Title: Inverter -6V		
Size: A4	Date:	**Rev: A**
KiCad E.D.A. kicad (5.1.5)-3		Id: 7/16





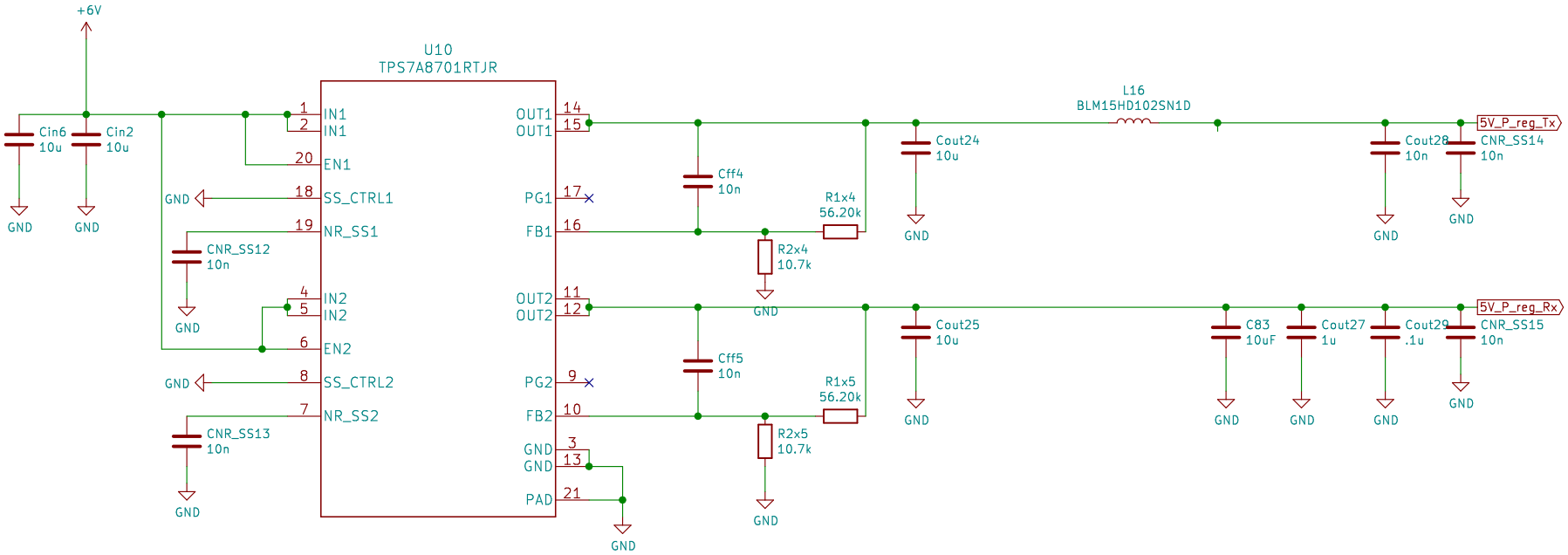


supplies TX and RX module with -5V

Sheet: /Sheet5EC795DA/
File: ldo_5N.sch

Title: LDO -5V

Size: A4	Date:	**Rev: A**
KiCad E.D.A. kicad (5.1.5)-3		Id: 8/16

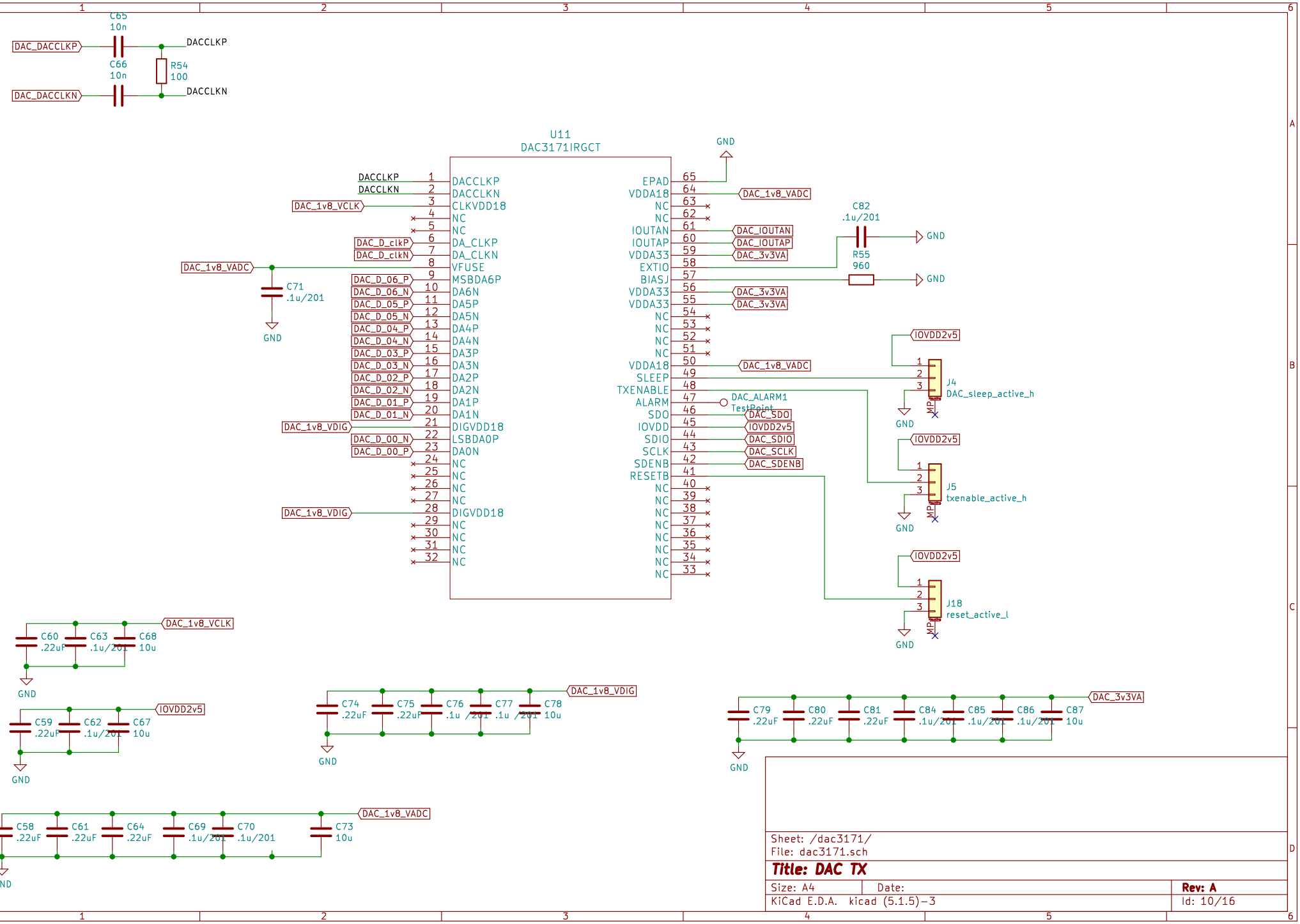


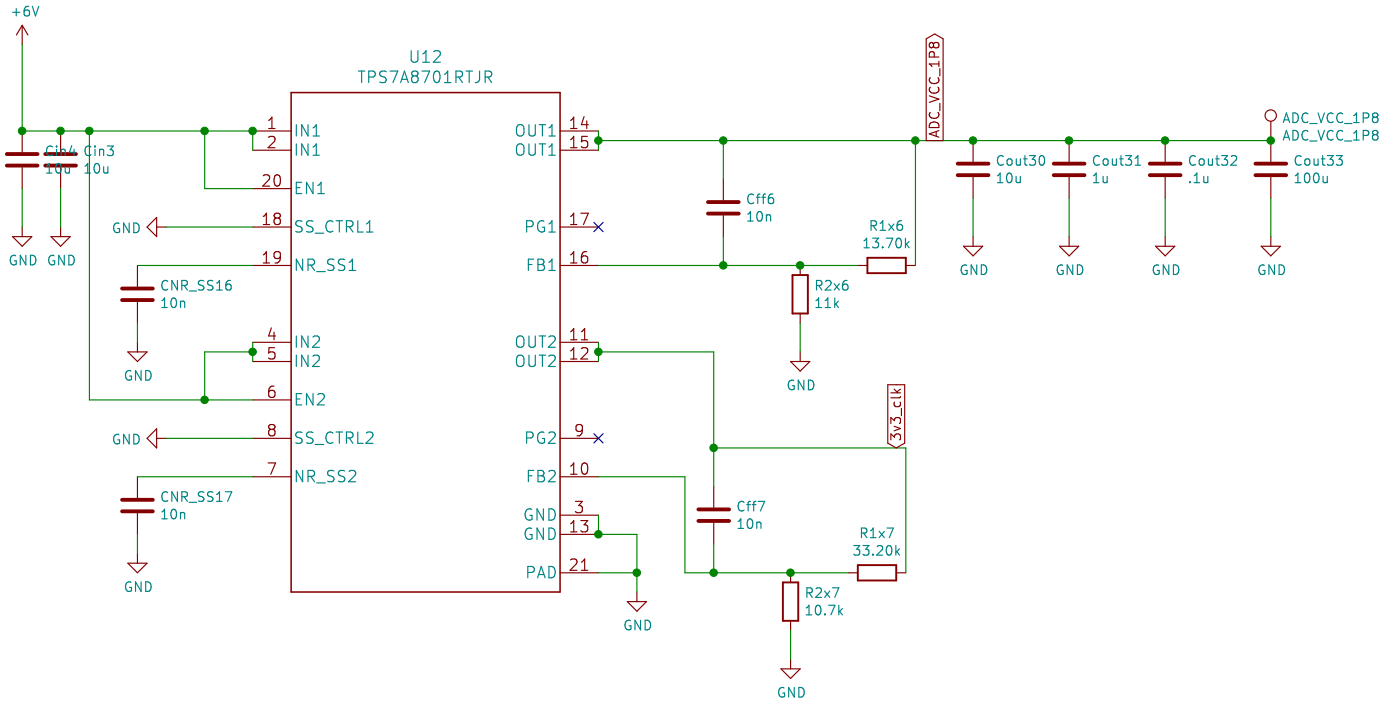
supplies TX and RX module with 5V

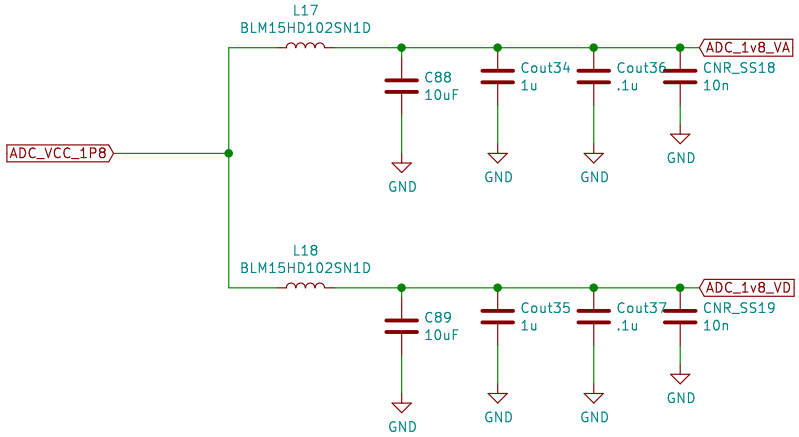
Sheet: /Sheet5EC8594D/
File: ldo_5v_P.sch

Title: LDO 5V

Size: A4	Date:	**Rev: A**
KiCad E.D.A. kicad (5.1.5)-3		Id: 9/16


C65
10n
DAC_DACCLKP
DACCLKP
C66
10n
R54
100
DAC_DACCLKN
DACCLKN
U11
DAC3171IRGCT
DACCLKP
DACCLKN
DAC_1v8_VCLK
DAC_D_clkP
DAC_D_clkN
DAC_1v8_VADC
DAC_D_06_P
DAC_D_06_N
DAC_D_05_P
DAC_D_05_N
DAC_D_04_P
DAC_D_04_N
DAC_D_03_P
DAC_D_03_N
DAC_D_02_P
DAC_D_02_N
DAC_D_01_P
DAC_D_01_N
DAC_1v8_VDIG
DAC_D_00_N
DAC_D_00_P
DAC_1v8_VDIG
C71
.1u/201
GND
CLKVDD18
NC
NC
DA_CLKP
DA_CLKN
VFUSE
MSBDA6P
DA6N
DA5P
DA5N
DA4P
DA4N
DA3P
DA3N
DA2P
DA2N
DA1P
DA1N
DIGVDD18
LSBDA0P
DA0N
NC
NC
NC
NC
DIGVDD18
NC
NC
NC
NC
NC
EPAD
VDDA18
NC
NC
IOUTAN
IOUTAP
VDDA33
EXTIO
BIASJ
VDDA33
VDDA33
NC
NC
NC
NC
VDDA18
SLEEP
TXENABLE
ALARM
SDO
IOVDD
SDIO
SCLK
SDENB
RESETB
NC
NC
NC
NC
NC
NC
NC
NC
NC
GND
DAC_1v8_VADC
DAC_IOUTAN
DAC_IOUTAP
DAC_3v3VA
DAC_3v3VA
DAC_3v3VA
DAC_1v8_VADC
DAC_ALARM1
TestPoint
DAC_SDO
IOVDD2v5
DAC_SDIO
DAC_SCLK
DAC_SDENB
C82
.1u/201
R55
960
GND
GND
IOVDD2v5
J4
DAC_sleep_active_h
GND
IOVDD2v5
J5
txenable_active_h
GND
IOVDD2v5
J18
reset_active_l
GND
C60
.22uF
C63
.1u/201
C68
10u
DAC_1v8_VCLK
GND
C59
.22uF
C62
.1u/201
C67
10u
IOVDD2v5
GND
C74
.22uF
C75
.22uF
C76
.1u /201
C77
.1u /201
C78
10u
DAC_1v8_VDIG
GND
C79
.22uF
C80
.22uF
C81
.22uF
C84
.1u/201
C85
.1u/201
C86
.1u/201
C87
10u
DAC_3v3VA
GND
C58
.22uF
C61
.22uF
C64
.22uF
C69
.1u/201
C70
.1u/201
C73
10u
DAC_1v8_VADC
GND
Sheet: /dac3171/
File: dac3171.sch
Title: DAC TX
Size: A4
Date:
Rev: A
KiCad E.D.A. kicad (5.1.5)-3
Id: 10/16



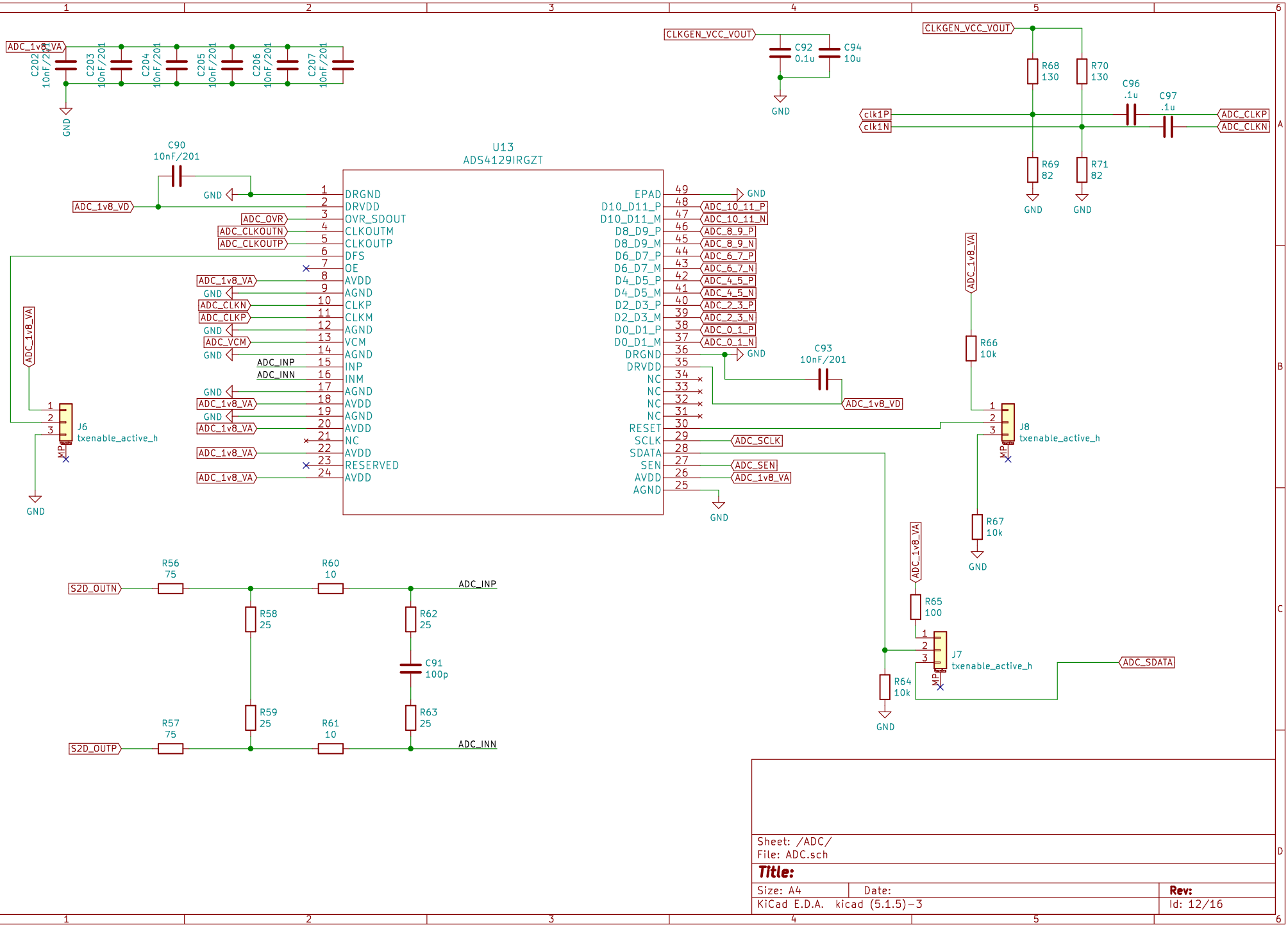


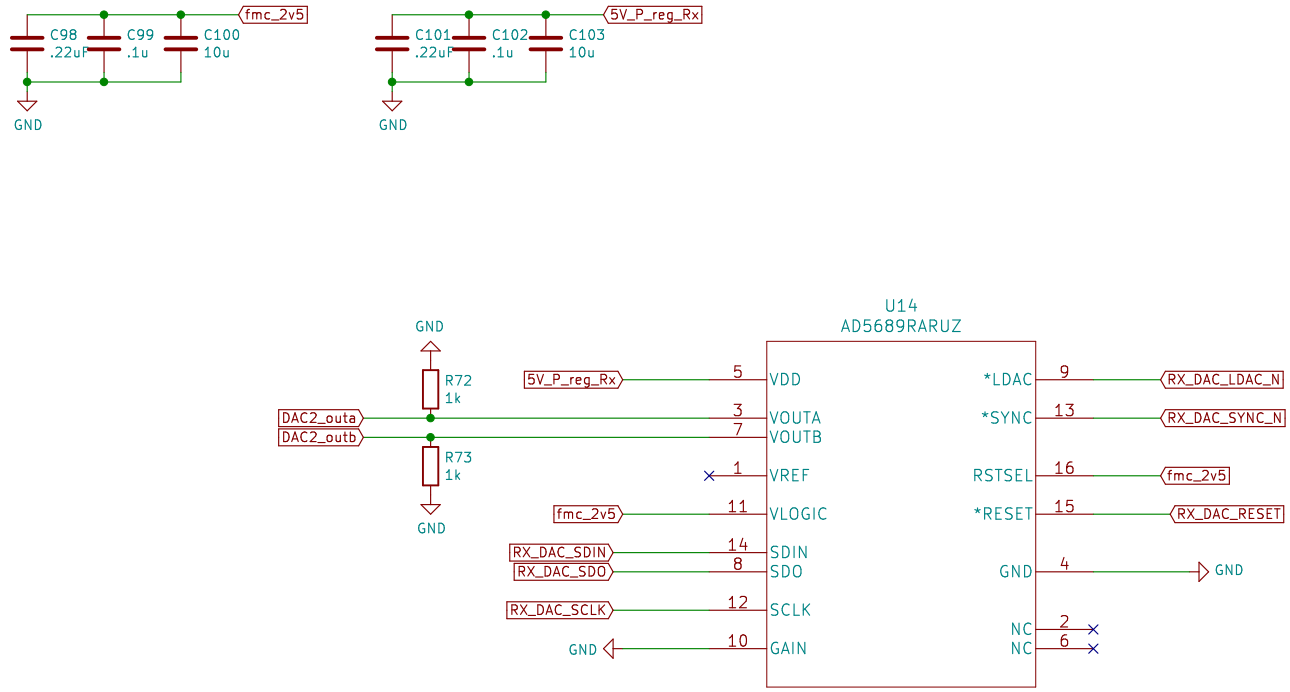
LDO supplies CLK and ADC

Sheet: /ADC_ps/
File: ADC_ps.sch

Title: ADC and CLK power supply

Size: A4	Date:	**Rev: A**
KiCad E.D.A. kicad (5.1.5)-3		Id: 11/16

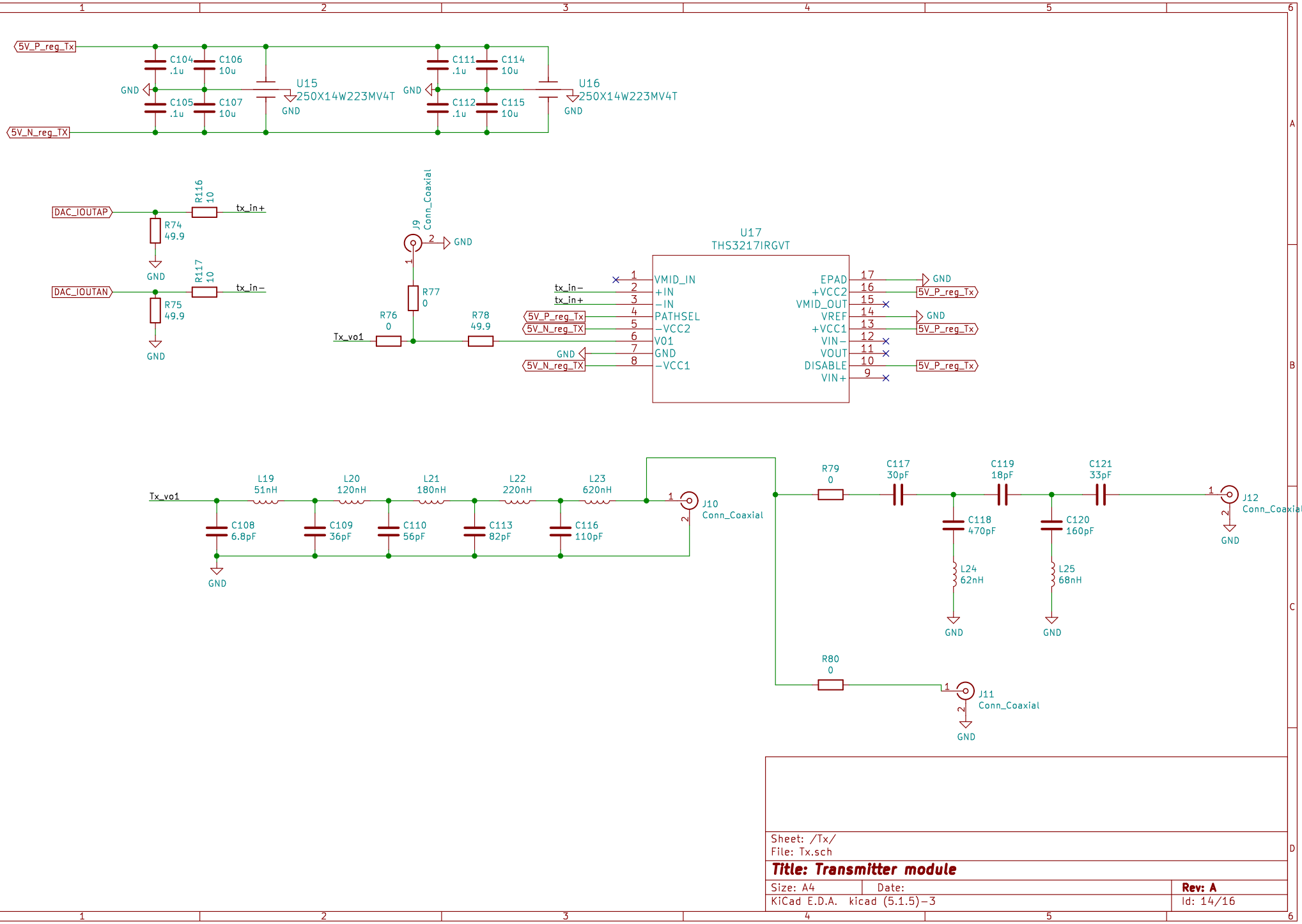

ADC_1v8_VA
C202 10nF/201
C203 10nF/201
C204 10nF/201
C205 10nF/201
C206 10nF/201
C207 10nF/201
GND
CLKGEN_VCC_VOUT
C92 0.1u
C94 10u
GND
CLKGEN_VCC_VOUT
R68 130
R70 130
C96 .1u
C97 .1u
clk1P
clk1N
ADC_CLKP
ADC_CLKN
R69 82
R71 82
GND
GND
C90 10nF/201
U13
ADS4129IRGZT
ADC_1v8_VD
GND
ADC_OVR
ADC_CLKOUTN
ADC_CLKOUTP
ADC_1v8_VA
GND
ADC_CLKN
ADC_CLKP
GND
ADC_VCM
GND
ADC_INP
ADC_INN
GND
ADC_1v8_VA
GND
ADC_1v8_VA
ADC_1v8_VA
1 DRGND
2 DRVDD
3 OVR_SDOUT
4 CLKOUTM
5 CLKOUTP
6 DFS
7 OE
8 AVDD
9 AGND
10 CLKP
11 CLKM
12 AGND
13 VCM
14 AGND
15 INP
16 INM
17 AGND
18 AVDD
19 AGND
20 AVDD
21 NC
22 AVDD
23 RESERVED
24 AVDD
49 EPAD
48 D10_D11_P
47 D10_D11_M
46 D8_D9_P
45 D8_D9_M
44 D6_D7_P
43 D6_D7_M
42 D4_D5_P
41 D4_D5_M
40 D2_D3_P
39 D2_D3_M
38 D0_D1_P
37 D0_D1_M
36 DRGND
35 DRVDD
34 NC
33 NC
32 NC
31 NC
30 RESET
29 SCLK
28 SDATA
27 SEN
26 AVDD
25 AGND
GND
GND
ADC_10_11_P
ADC_10_11_N
ADC_8_9_P
ADC_8_9_N
ADC_6_7_P
ADC_6_7_N
ADC_4_5_P
ADC_4_5_N
ADC_2_3_P
ADC_2_3_N
ADC_0_1_P
ADC_0_1_N
GND
C93 10nF/201
ADC_1v8_VD
ADC_SCLK
ADC_SEN
ADC_1v8_VA
GND
J6 txenable_active_h
ADC_1v8_VA
GND
ADC_1v8_VA
R66 10k
J8 txenable_active_h
R67 10k
GND
R56 75
R60 10
S2D_OUTN
ADC_INP
R58 25
R62 25
C91 100p
R59 25
R63 25
R57 75
R61 10
S2D_OUTP
ADC_INN
ADC_1v8_VA
R65 100
J7 txenable_active_h
ADC_SDATA
R64 10k
GND
Sheet: /ADC/
File: ADC.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.5)-3
Id: 12/16



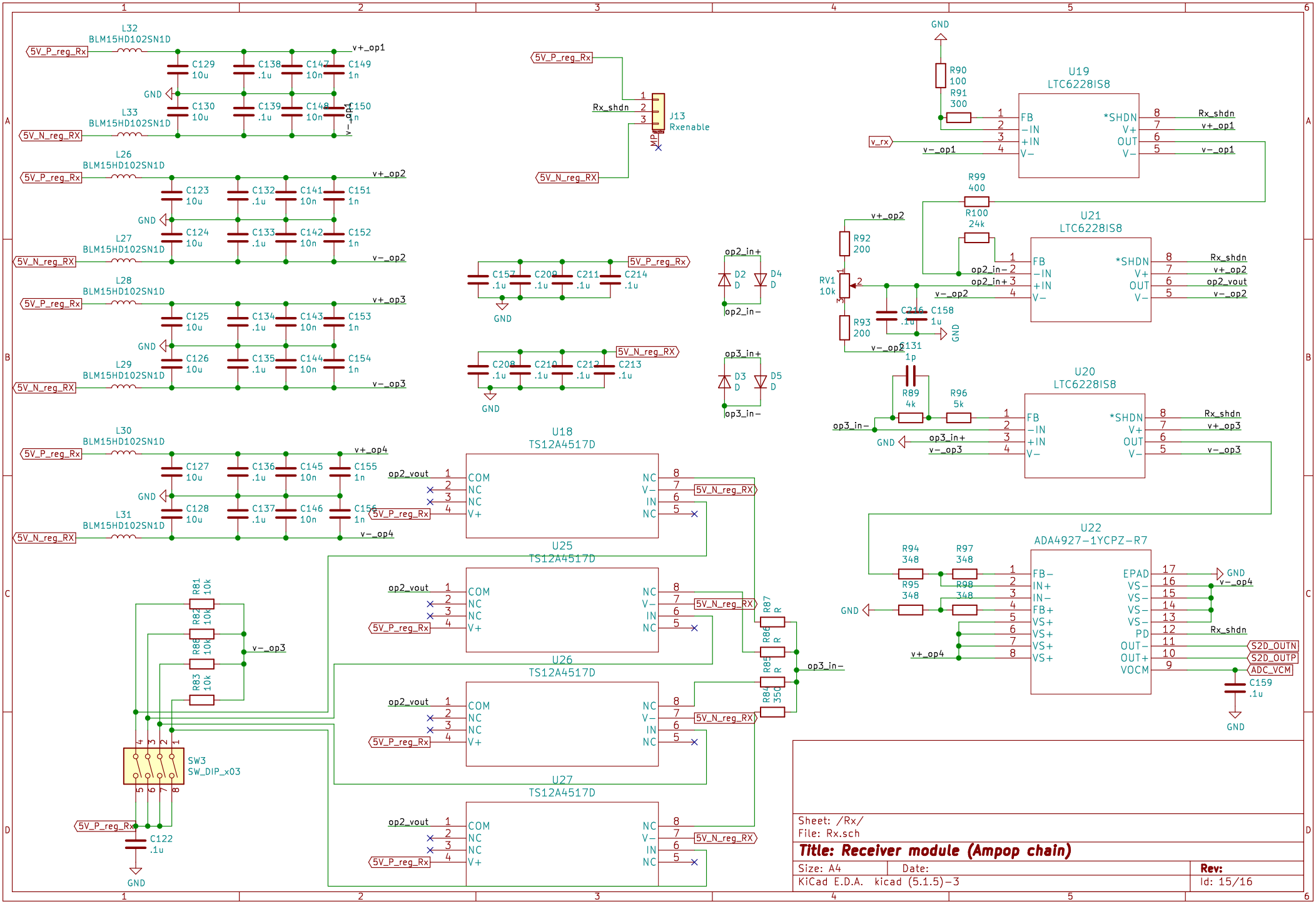
Sheet: /dac2/
File: dac2.sch

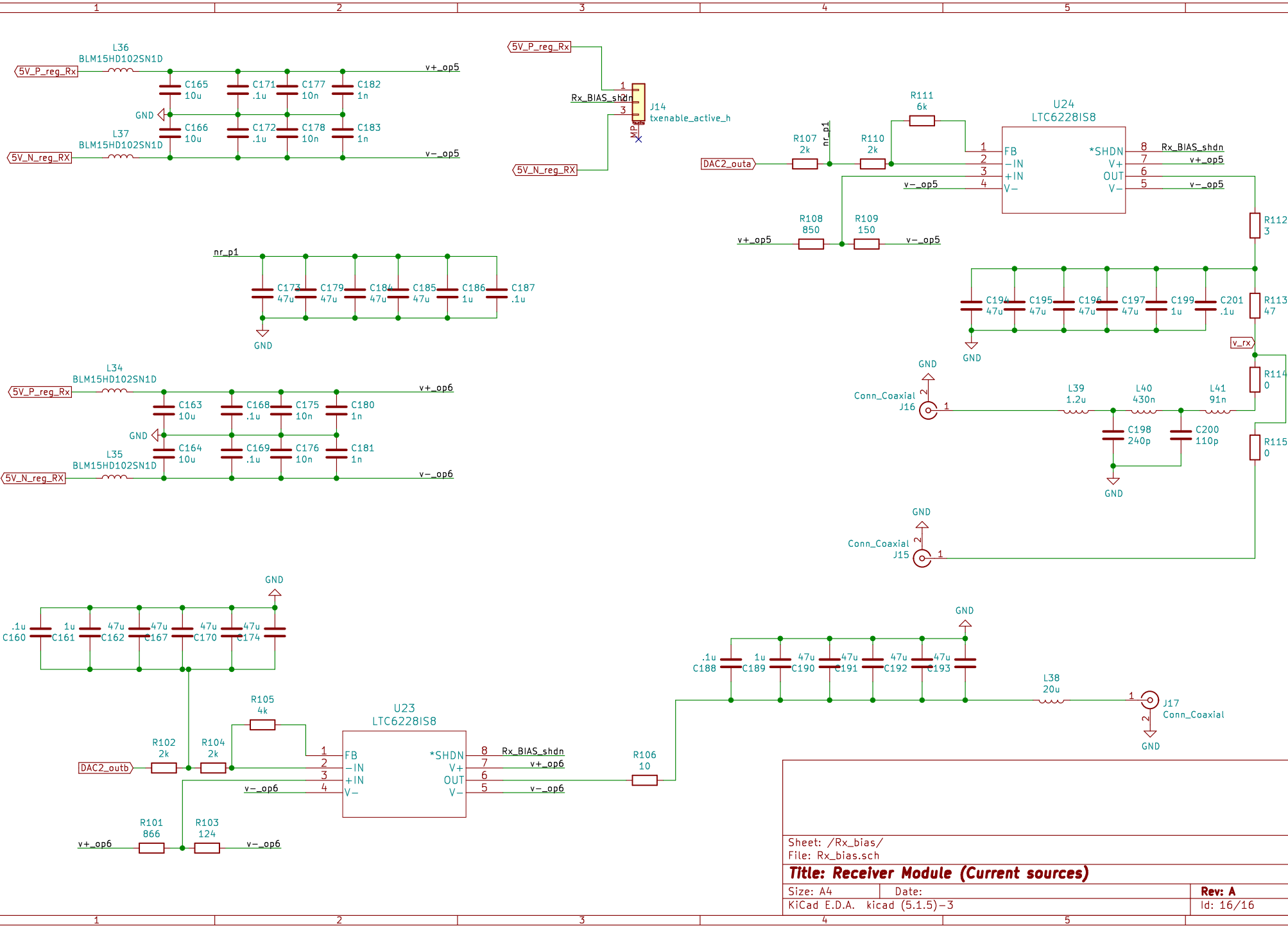
Title: DAC for RX current sources

Size: A4	Date:	**Rev: A**
KiCad E.D.A. kicad (5.1.5)-3		Id: 13/16



Sheet: /Tx/		
File: Tx.sch		
Title: Transmitter module		
Size: A4	Date:	**Rev: A**
KiCad E.D.A. kicad (5.1.5)−3		Id: 14/16

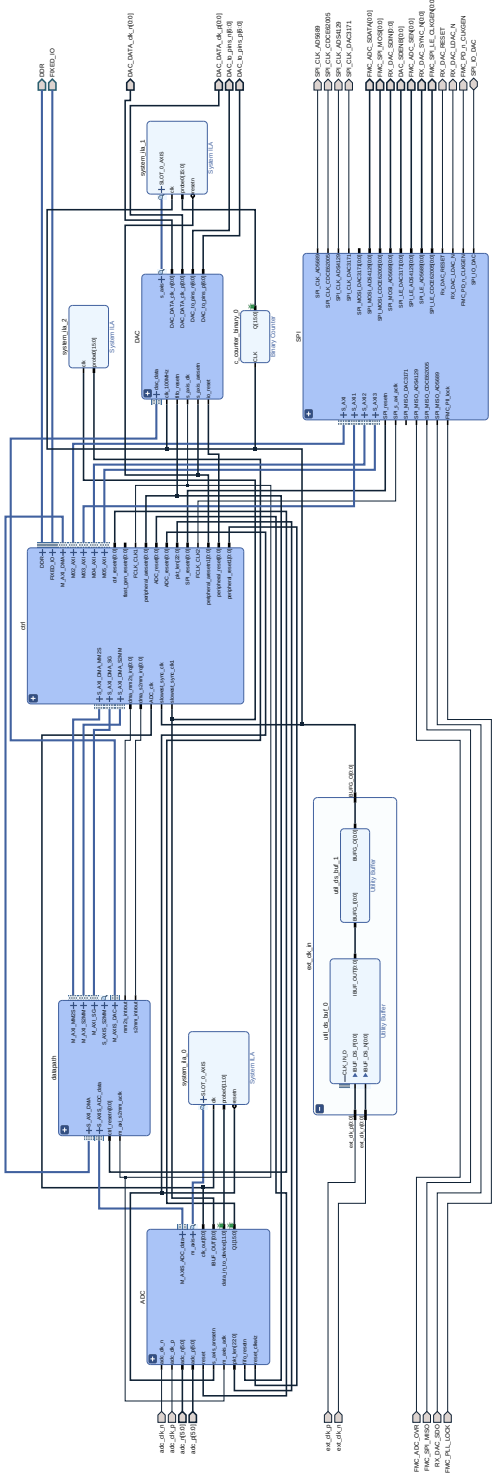

L32
BLM15HD102SN1D
5V_P_reg_Rx
v+_op1
C129
10u
C138
.1u
C147
10n
C149
1n
GND
C130
10u
C139
.1u
C148
10n
C150
1n
L33
BLM15HD102SN1D
5V_N_reg_RX
v-_op1
L26
BLM15HD102SN1D
5V_P_reg_Rx
v+_op2
C123
10u
C132
.1u
C141
10n
C151
1n
GND
C124
10u
C133
.1u
C142
10n
C152
1n
L27
BLM15HD102SN1D
5V_N_reg_RX
v-_op2
L28
BLM15HD102SN1D
5V_P_reg_Rx
v+_op3
C125
10u
C134
.1u
C143
10n
C153
1n
GND
C126
10u
C135
.1u
C144
10n
C154
1n
L29
BLM15HD102SN1D
5V_N_reg_RX
v-_op3
L30
BLM15HD102SN1D
5V_P_reg_Rx
v+_op4
C127
10u
C136
.1u
C145
10n
C155
1n
GND
C128
10u
C137
.1u
C146
10n
C156
1n
L31
BLM15HD102SN1D
5V_N_reg_RX
v-_op4
5V_P_reg_Rx
Rx_shdn
J13
Rxenable
5V_N_reg_RX
C157
.1u
C209
.1u
C211
.1u
C214
.1u
5V_P_reg_Rx
GND
C208
.1u
C210
.1u
C212
.1u
C213
.1u
5V_N_reg_RX
GND
op2_in+
D2
D
D4
D
op2_in-
op3_in+
D3
D
D5
D
op3_in-
GND
R90
100
R91
300
v_rx
v-_op1
U19
LTC6228IS8
FB
-IN
+IN
V-
*SHDN
V+
OUT
V-
Rx_shdn
v+_op1
v-_op1
R99
400
R100
24k
v+_op2
R92
200
RV1
10k
R93
200
v-_op2
U21
LTC6228IS8
op2_in-
op2_in+
v-_op2
C216
.1u
C158
1u
GND
C131
1p
R89
4k
R96
5k
op3_in-
GND
op3_in+
v-_op3
U20
LTC6228IS8
Rx_shdn
v+_op3
v-_op3
U18
TS12A4517D
op2_vout
COM
NC
NC
V+
NC
V-
IN
NC
5V_N_reg_RX
5V_P_reg_Rx
U25
TS12A4517D
U26
TS12A4517D
U27
TS12A4517D
R81
10k
R82
10k
R88
10k
R83
10k
v-_op3
R87
R
R86
R
R85
R
R84
350
op3_in-
SW3
SW_DIP_x03
5V_P_reg_Rx
C122
.1u
GND
R94
348
R97
348
R95
348
R98
348
GND
v+_op4
U22
ADA4927-1YCPZ-R7
FB-
IN+
IN-
FB+
VS+
VS+
VS+
VS+
EPAD
VS-
VS-
VS-
VS-
PD
OUT-
OUT+
VOCM
GND
v-_op4
Rx_shdn
S2D_OUTN
S2D_OUTP
ADC_VCM
C159
.1u
GND
Sheet: /Rx/
File: Rx.sch
Title: Receiver module (Ampop chain)
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.5)-3
Id: 15/16


L36
BLM15HD102SN1D
5V_P_reg_Rx
C165 10u
C171 .1u
C177 10n
C182 1n
GND
C166 10u
C172 .1u
C178 10n
C183 1n
L37
BLM15HD102SN1D
5V_N_reg_RX
v+_op5
v−_op5
5V_P_reg_Rx
Rx_BIAS_shdn
J14
txenable_active_h
5V_N_reg_RX
R111 6k
U24
LTC6228IS8
R107 2k
nr_p1
R110 2k
DAC2_outa
FB
−IN
+IN
V−
*SHDN
V+
OUT
V−
Rx_BIAS_shdn
v+_op5
v−_op5
R108 850
R109 150
v+_op5
v−_op5
R112 3
nr_p1
C173 47u
C179 47u
C184 47u
C185 47u
C186 1u
C187 .1u
GND
C194 47u
C195 47u
C196 47u
C197 47u
C199 1u
C201 .1u
R113 47
GND
v_rx
L34
BLM15HD102SN1D
5V_P_reg_Rx
v+_op6
C163 10u
C168 .1u
C175 10n
C180 1n
GND
C164 10u
C169 .1u
C176 10n
C181 1n
L35
BLM15HD102SN1D
5V_N_reg_RX
v−_op6
GND
Conn_Coaxial
J16
L39 1.2u
L40 430n
L41 91n
R114 0
C198 240p
C200 110p
R115 0
GND
GND
Conn_Coaxial
J15
GND
.1u C160
1u C161
47u C162
47u C167
47u C170
47u C174
R105 4k
U23
LTC6228IS8
R102 2k
R104 2k
DAC2_outb
FB
−IN
+IN
V−
*SHDN
V+
OUT
V−
Rx_BIAS_shdn
v+_op6
v−_op6
v−_op6
R106 10
R101 866
R103 124
v+_op6
v−_op6
GND
.1u C188
1u C189
47u C190
47u C191
47u C192
47u C193
L38 20u
J17
Conn_Coaxial
GND
Sheet: /Rx_bias/
File: Rx_bias.sch
Title: Receiver Module (Current sources)
Size: A4
Date:
Rev: A
KiCad E.D.A. kicad (5.1.5)−3
Id: 16/16

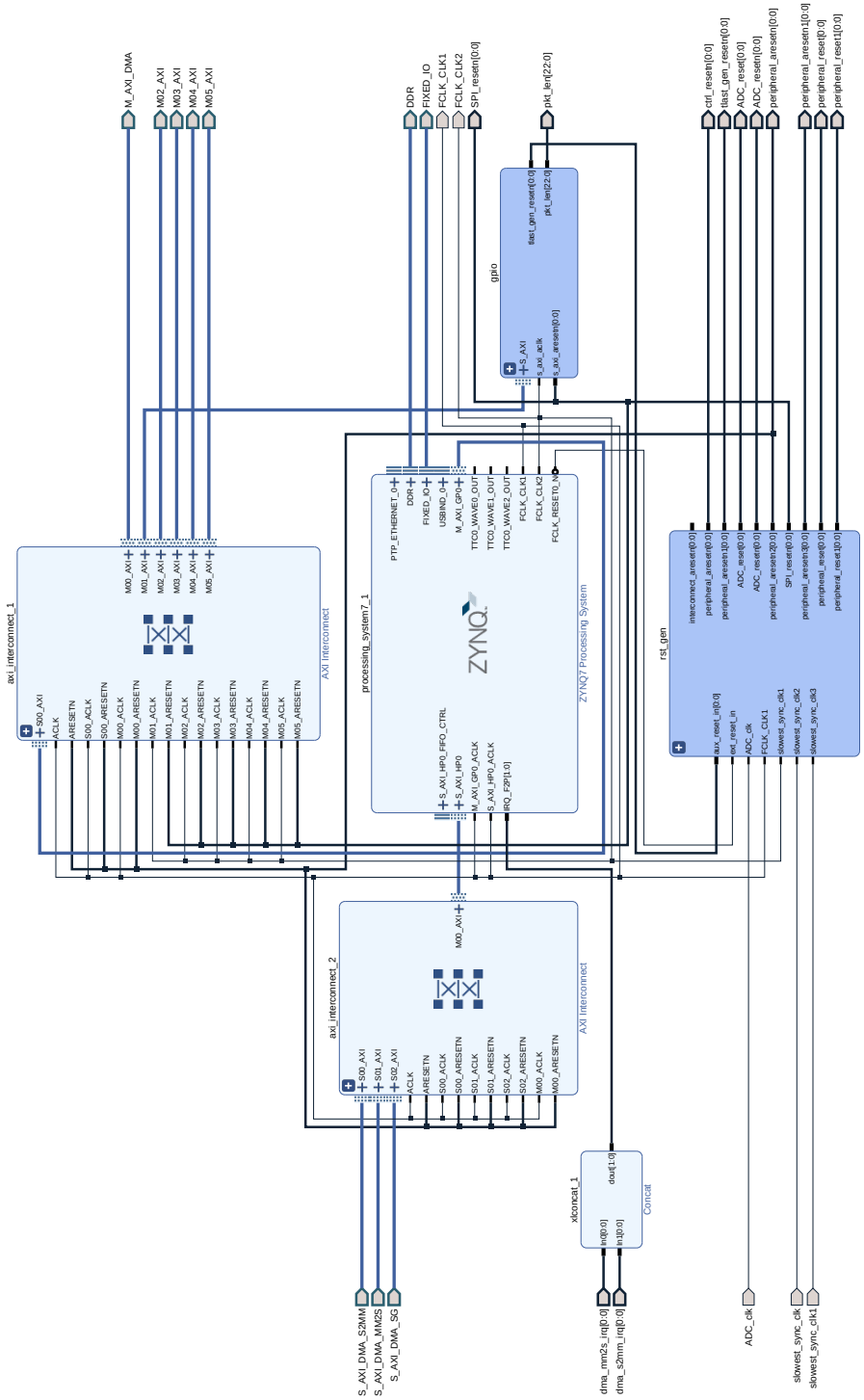
Appendix B

Vivado: Implemented block design

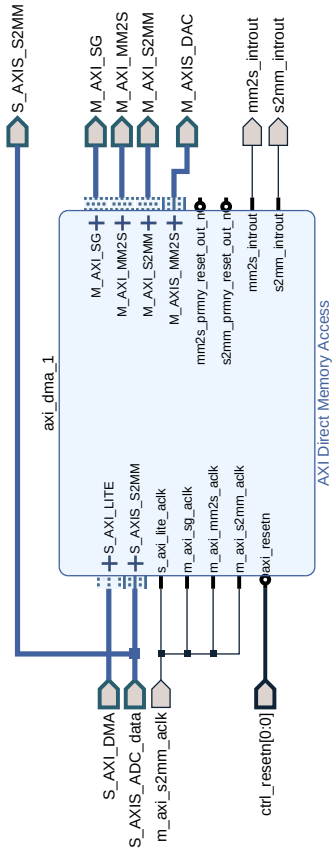
B.1 Overall block design



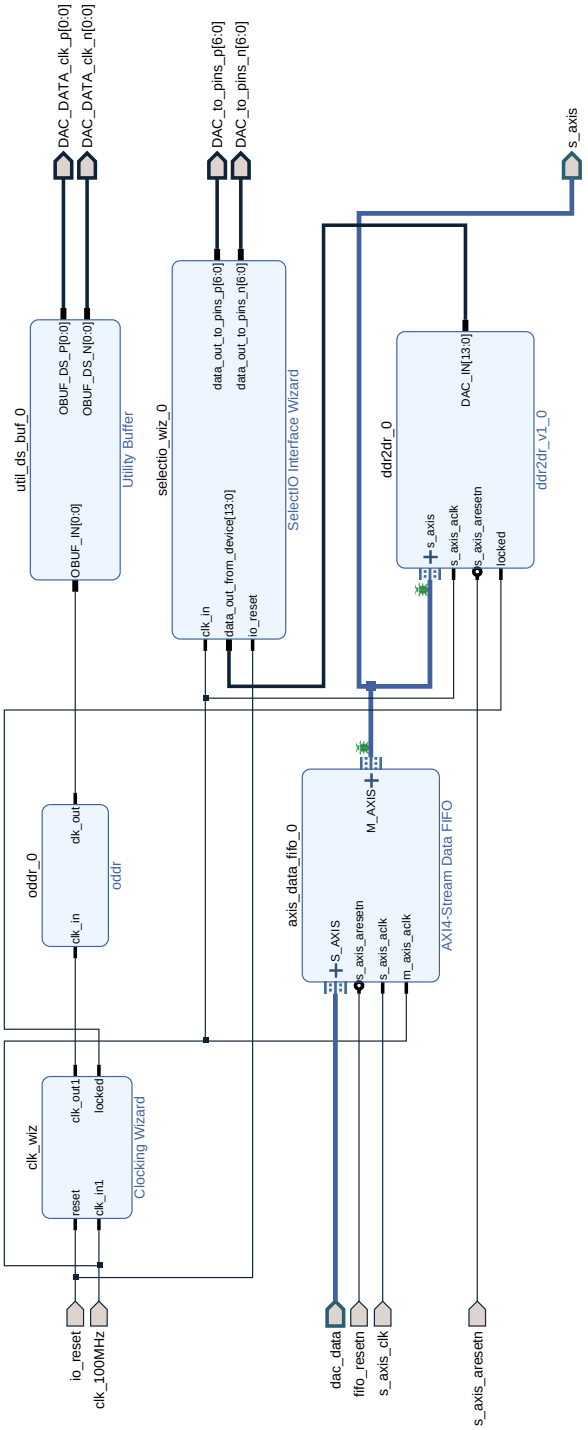
B.2 Block design: ctrl



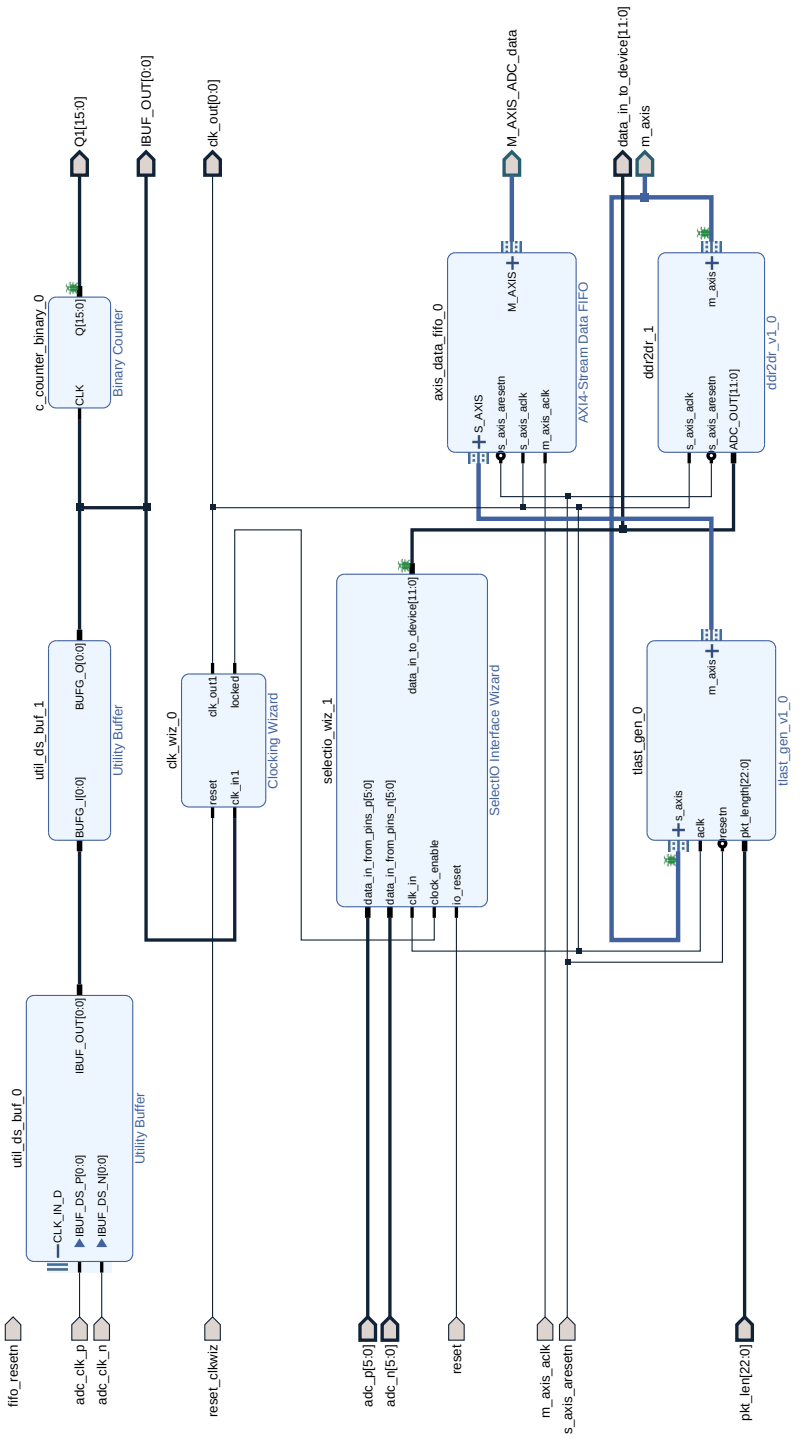
B.3 Block design: datapath



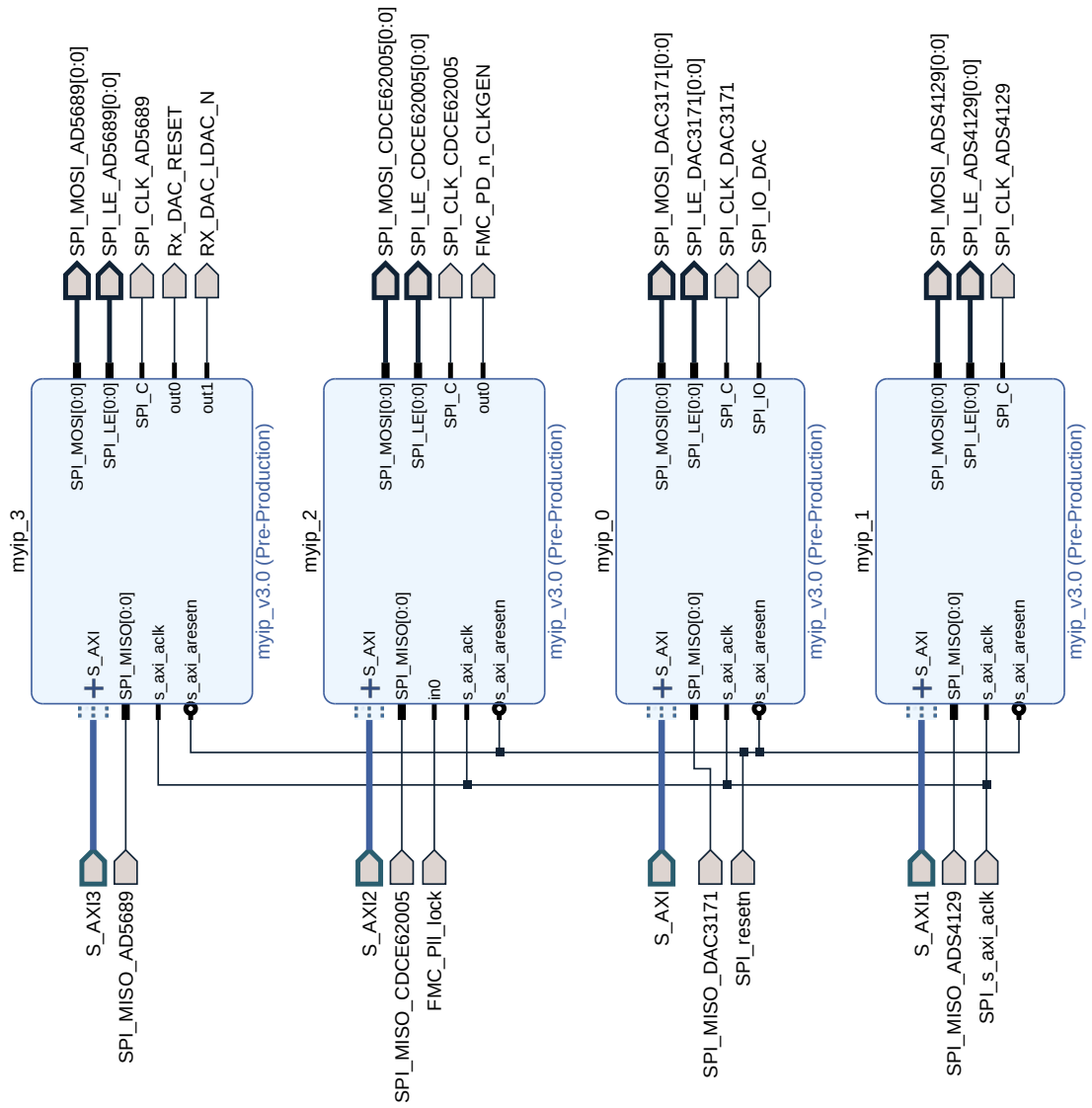
B.4 Block design: DAC



B.5 Block design: ADC



B.6 Block design: SPI



Appendix C

SPI IP core: Interface with each IC

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////

// Company:
// Engineer:
//
// Create Date: 12.08.2020 16:49:24
// Design Name:
// Module Name: myip_v3_0_spi
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////



module myip_v3_0_spi #
    (
        parameter integer DATA_LEN      = 32,
        parameter DEVICE = "DAC3171"
    )
    (
        input wire  S_AXI_ACLK,
        input wire  S_AXI_ARESETN,
        input wire [DATA_LEN-1:0] SPI_DATA,
        input wire [0:0] SPI_MISO,
        output reg [0:0] SPI_MOSI,
```

```
    output reg [0:0] SPI_LE,
    output wire SPI_C,
    output reg spi_clk_en,
    output reg [DATA_LEN-1:0] SPI_ANS,
    output reg [0:0] ready,
    input wire [0:0] start,
    inout wire SPI_IO
);

reg [DATA_LEN-1:0] spi_counter;
reg [DATA_LEN-1:0] SPI_DATA_R;
reg read;
//

if(DEVICE == "DAC3171")
begin
    wire data_in;
    wire data_out;
    reg data_enable;
    reg MOSI;

    assign data_out = MOSI;
    IOBUF u_iobuf_dq
        (
            .I  (data_out),
            .T  (data_enable),
            .IO (SPI_IO),
            .O  (data_in)
    );
    integer SPI_DATA_LEN = 24; // 8 + 16
    integer SPI_ADDR_LEN = 8;
    reg rd_dly;
    assign SPI_C = (spi_counter > 0)? spi_clk_en : 1'b0;
    always @( posedge S_AXI_ACLK )
    begin
        spi_clk_en <= spi_clk_en + 1;
        if ( S_AXI_ARESETN == 1'b0 )
        begin
            ready <= 1'b1;
            spi_counter <= 'b0;
            SPI_MOSI <= 'b0;
            MOSI <= 'b0;
            SPI_LE <= 'b1;
            spi_clk_en <= 1'b0;
            read <=0;
            data_enable<=1'b0;
            rd_dly <=1;
        end
        else
```

```
            begin
                if(!spi_clk_en)
                begin
                    if(ready == 1)
                    begin
                        //SPI_MOSI <= 1'b1;
                        SPI_LE <= 'b1;
                        spi_counter <= 0;
                        data_enable <= 0;
                        read <=1'b0;
                    end

                    if(!ready)SPI_ANS[SPI_DATA_LEN - spi_counter] <= data_in;
                end
                else
                begin
                    if(start == 1'b1)
                    begin
                        ready <= 1'b0;
                        spi_counter <= 'b0;
                        SPI_DATA_R <= SPI_DATA;
                        if(SPI_DATA[SPI_DATA_LEN-1]==1)
                            read <= 1;
                    end
                    else if(ready == 1'b0 && spi_counter < SPI_DATA_LEN)
                    begin
                        SPI_MOSI <= SPI_DATA_R[SPI_DATA_LEN -1 - spi_counter];
                        MOSI <= SPI_DATA_R[SPI_DATA_LEN -1 - spi_counter];
                        spi_counter <= spi_counter + 1;
                        SPI_LE <= 1'b0;
                    end
                    if(read && spi_counter > SPI_ADDR_LEN)
                        data_enable <= 1;
                    if(spi_counter == SPI_DATA_LEN)
                    begin
                        ready <= 1'b1;
                        SPI_MOSI <= 1'b0;
                        MOSI <= 1'b0;

                    end
                end
            end
        end
    end
    else if(DEVICE == "ADS4129")
    begin
        integer SPI_DATA_LEN = 16; // 8 + 8
        integer SPI_ADDR_LEN = 8;
        reg [3:0] clock_en_1_16;
```

```
assign SPI_C = (spi_counter > 0)? spi_clk_en : 1'b1;

always @( posedge S_AXI_ACLK )
begin
    clock_en_1_16 <= clock_en_1_16 + 1;
    if(clock_en_1_16 == 4'h0 || clock_en_1_16 == 4'h7)spi_clk_en <=
        spi_clk_en + 1;
    if ( S_AXI_ARESETN == 1'b0 )
    begin
        ready <= 1'b1;
        spi_counter <= 'b0;
        SPI_MOSI <= 'b0;
        SPI_LE <= 'b1;
        spi_clk_en <= 1'b0;
        read <=0;
        clock_en_1_16<=0;
    end
    else
    begin
        if(clock_en_1_16 == 4'h7)
        begin
            if(ready == 1)
            begin
                SPI_LE <= 'b1;
                spi_counter <= 0;
            end
            if(ready == 1'b0 && spi_counter < SPI_DATA_LEN)
                SPI_ANS[SPI_DATA_LEN -1 - spi_counter] <= SPI_MISO;
        end
        else if(clock_en_1_16 == 4'h0)
        begin
            if(start == 1'b1)
            begin
                ready <= 1'b0;
                spi_counter <= 'b0;
                SPI_DATA_R <= SPI_DATA;
            end
            else if(ready == 1'b0 && spi_counter < SPI_DATA_LEN)
            begin

                SPI_MOSI <= SPI_DATA_R[SPI_DATA_LEN -1 - spi_counter];
                spi_counter <= spi_counter + 1;
                SPI_LE <= 1'b0;
            end
            if(spi_counter == SPI_DATA_LEN)
            begin
                ready <= 1'b1;
                SPI_MOSI <= 1'b0;
                SPI_LE <= 'b1;
```

```
                end
            end
            else if(clock_en_1_16 == 4'hB)
            begin
                if(spi_counter == SPI_DATA_LEN)
                begin
                    SPI_LE <= 'b1;
                end
            end
        end
    end

end
else if (DEVICE == "CDCE62005")
begin
    integer SPI_DATA_LEN = 32; // 28 + 4
    integer SPI_ADDR_LEN = 4;
    reg read_dly;
    assign SPI_C = (spi_counter > 0)? spi_clk_en : 1'b0;
    always @( posedge S_AXI_ACLK )
    begin
        spi_clk_en <= spi_clk_en + 1;
        if ( S_AXI_ARESETN == 1'b0 )
        begin
            ready <= 1'b1;
            spi_counter <= 'b0;
            SPI_MOSI <= 'b0;
            SPI_LE <= 'b1;
            spi_clk_en <= 1'b0;
            read<=0;

        end
        else
        begin
            if(!spi_clk_en)
            begin
                if(ready == 1)
                begin
                    SPI_LE <= 'b1;
                    spi_counter <= 0;
                end
                if(read == 1 && SPI_LE == 0)
                begin
                    SPI_ANS[spi_counter-1] <= SPI_MISO;
                end
            end
            else
            begin
                if(start == 1'b1)
```

```
                    begin
                        ready <= 1'b0;
                        spi_counter <= 'b0;
                        SPI_DATA_R <= SPI_DATA;
                        read<=0;
                    end
                    else if(ready == 1'b0 && spi_counter < SPI_DATA_LEN)
                    begin
                        //SPI_ANS[SPI_DATA_LEN -1 - spi_counter] <= SPI_MISO;
                        SPI_MOSI <= SPI_DATA_R[spi_counter];
                        spi_counter <= spi_counter + 1;
                        SPI_LE <= 1'b0;
                    end
                    if(spi_counter == SPI_DATA_LEN)
                    begin
                        if(SPI_DATA[3:0] == 4'hE && read == 0)
                        begin
                            read <= 1;
                            SPI_MOSI <= 1'b0;
                            SPI_LE <= 'b1;
                            spi_counter <= 0;
                        end
                        else
                        begin
                            ready <= 1'b1;
                            SPI_MOSI <= 1'b0;
                            SPI_LE <= 'b1;
                            spi_counter <= 0;
                        end


                    end
                end

            end
        end
    end
    else if (DEVICE == "AD5689R")
    begin
        integer SPI_DATA_LEN = 24; // 16 + 4 +4
        integer SPI_ADDR_LEN = 8; // 4 + 4

        assign SPI_C = (spi_counter > 0)? spi_clk_en : 1'b0;
        always @( posedge S_AXI_ACLK )
        begin
            spi_clk_en <= spi_clk_en + 1;
            if ( S_AXI_ARESETN == 1'b0 )
            begin
                ready <= 1'b1;
```

```
                spi_counter <= 'b0;
                SPI_MOSI <= 'b0;
                SPI_LE <= 'b1;
                spi_clk_en <= 1'b0;

            end
            else
            begin
                if(spi_clk_en)
                begin
                    if(ready == 1)
                    begin
                        SPI_LE <= 'b1;
                        spi_counter <= 0;
                    end
                end
                else
                begin
                    if(start == 1'b1)
                    begin
                        ready <= 1'b0;
                        spi_counter <= 'b0;
                        SPI_DATA_R <= SPI_DATA;
                    end
                    else if(ready == 1'b0 && spi_counter < SPI_DATA_LEN)
                    begin
                        SPI_ANS[SPI_DATA_LEN -1 - spi_counter] <= SPI_MISO;
                        SPI_MOSI <= SPI_DATA_R[SPI_DATA_LEN -1 - spi_counter];
                        spi_counter <= spi_counter + 1;
                        SPI_LE <= 1'b0;
                    end
                    if(spi_counter == SPI_DATA_LEN)
                    begin
                        ready <= 1'b1;
                        SPI_MOSI <= 1'b0;
                        SPI_LE <= 'b1;
                        spi_counter <= 0;
                    end
                end
            end
        end
    end
endmodule
```

Appendix D

DDR2DR IP core: Interface with each IC

```
module  ddr2dr
# (parameter RESOLUTION = 12,
   parameter OUT_WIDTH = 32,
   parameter IC = "ADS4129",
   parameter DATA_WIDTH = 32,
   parameter TDATA_WIDTH = 8,
   parameter INV = "FALSE" )
(
 input s_axis_aclk          , // Clock Input
 input s_axis_aresetn       , // reset sync posedge

   // Slave interface
   input   wire                          s_axis_tvalid,
   output  wire                          s_axis_tready,
   input  wire [DATA_WIDTH-1:0]          s_axis_tdata,

   // Master interface
   output  wire                          m_axis_tvalid,
   input   wire                          m_axis_tready,
   output wire [DATA_WIDTH-1:0]          m_axis_tdata,

   output wire [RESOLUTION-1:0] DAC_IN,
   input wire [RESOLUTION-1:0] ADC_OUT,
   input wire locked
 );



// converts a double data rate input signal:
// data_in = d0,d2,d4,... @ posedge
```

```
// data_in = d1,d3,d5,... @ negedge
// into:
// dataout = d0,d1,... delayed by 1 clock cycle

integer i; // aux variable



if(IC == "ADS4129")
begin


    reg [DATA_WIDTH-1:0] data_out;
    reg [DATA_WIDTH-1:0] reg_;

    // Pass through control signals
    assign s_axis_tready = 1'b1;
    assign m_axis_tvalid = 1'b1;
    assign m_axis_tdata = data_out;

    always @(posedge s_axis_aclk) // handle data @ negedge
    begin
        if(s_axis_aresetn == 1'b0)
           begin
                  data_out <= 0;
           end
           else
           begin
            for(i = 1; i < RESOLUTION; i = i + 2)
                        data_out[i] <= ~ADC_OUT[RESOLUTION/2+(i-1)/2];
                  for(i = 0; i < RESOLUTION; i = i + 2)
                  data_out[i] <= ~ADC_OUT[(i)/2];
                  data_out[DATA_WIDTH-1:RESOLUTION] = {DATA_WIDTH-RESOLUTION{~
                      ADC_OUT[(RESOLUTION-1)]}};
            end
    end
end
else if (IC == "DAC3171")
begin

    reg [RESOLUTION-1:0] data_out;

    // Pass through control signals
    assign s_axis_tready = 1'b1;
    assign m_axis_tvalid = 1'b1;

    assign DAC_IN = (locked)? data_out : 0;

    always @(negedge s_axis_aclk) // handle data @ negedge
```

```
    begin
        if(s_axis_aresetn == 1'b0)
           begin
                  data_out <= {RESOLUTION-1{1'b0}};
           end
           else if(s_axis_tvalid)
           begin
            data_out[RESOLUTION-1:RESOLUTION/2] <= s_axis_tdata[RESOLUTION
                /2-1:0];
            data_out[RESOLUTION/2-1:0] <= s_axis_tdata[RESOLUTION-1:RESOLUTION
                /2];
           end
    end
end

endmodule
```

Appendix E

ZC706 Evaluation board: Constraining the design

```
set_property DIFF_TERM TRUE [get_ports adc_clk_p]
set_property DIFF_TERM TRUE [get_ports adc_clk_n]
set_property IOSTANDARD LVDS_25 [get_ports {DAC_DATA_clk_p[0]}]
set_property IOSTANDARD LVDS_25 [get_ports {DAC_DATA_clk_n[0]}]
set_property DIFF_TERM FALSE [get_ports {DAC_to_pins_p[5]}]
set_property DIFF_TERM FALSE [get_ports {DAC_to_pins_n[5]}]
set_property DIFF_TERM TRUE [get_ports {adc_p[5]}]
set_property DIFF_TERM TRUE [get_ports {adc_n[5]}]
set_property DIFF_TERM TRUE [get_ports {adc_p[4]}]
set_property DIFF_TERM TRUE [get_ports {adc_n[4]}]
set_property DIFF_TERM TRUE [get_ports {adc_p[3]}]
set_property DIFF_TERM TRUE [get_ports {adc_n[3]}]
set_property DIFF_TERM TRUE [get_ports {adc_p[2]}]
set_property DIFF_TERM TRUE [get_ports {adc_n[2]}]
set_property DIFF_TERM TRUE [get_ports {adc_p[1]}]
set_property DIFF_TERM TRUE [get_ports {adc_n[1]}]
set_property DIFF_TERM TRUE [get_ports {adc_p[0]}]
set_property DIFF_TERM TRUE [get_ports {adc_n[0]}]
set_property IOSTANDARD LVDS_25 [get_ports ext_clk_n]
set_property IOSTANDARD LVDS_25 [get_ports ext_clk_p]
set_property DIFF_TERM TRUE [get_ports ext_clk_p]
set_property DIFF_TERM TRUE [get_ports ext_clk_n]

set_property PACKAGE_PIN AD23 [get_ports {DAC_to_pins_p[0]}]
set_property PACKAGE_PIN AF23 [get_ports {DAC_to_pins_p[1]}]

set_property PACKAGE_PIN AJ23 [get_ports {DAC_to_pins_p[2]}]
set_property PACKAGE_PIN AF19 [get_ports {DAC_to_pins_p[3]}]
set_property PACKAGE_PIN AJ20 [get_ports {DAC_to_pins_p[4]}]
set_property PACKAGE_PIN AH19 [get_ports {DAC_to_pins_p[5]}]
set_property PACKAGE_PIN AK17 [get_ports {DAC_to_pins_p[6]}]
set_property PACKAGE_PIN AF20 [get_ports {DAC_DATA_clk_p[0]}]
```

```
set_property PACKAGE_PIN T30 [get_ports {adc_p[0]}]
set_property PACKAGE_PIN R25 [get_ports {adc_p[1]}]
set_property PACKAGE_PIN P30 [get_ports {adc_p[2]}]
set_property PACKAGE_PIN N29 [get_ports {adc_p[3]}]
set_property PACKAGE_PIN P23 [get_ports {adc_p[4]}]
set_property PACKAGE_PIN N26 [get_ports {adc_p[5]}]
set_property PACKAGE_PIN AE22 [get_ports adc_clk_p]

set_property IOSTANDARD LVDS_25 [get_ports adc_clk_p]

create_clock -period 8.000 -name adc_clk_p -waveform {0.000 4.000} [get_ports
    adc_clk_p]
create_clock -period 8.000 -name ext_clk_p -waveform {0.000 4.000} [get_ports
    ext_clk_p]




set_input_delay -clock [get_clocks clk_fpga_2] -min -add_delay 20.000 [
    get_ports FMC_ADC_OVR]
set_input_delay -clock [get_clocks clk_fpga_2] -max -add_delay 40.000 [
    get_ports FMC_ADC_OVR]
set_input_delay -clock [get_clocks clk_fpga_2] -min -add_delay 20.000 [
    get_ports FMC_SPI_MISO]
set_input_delay -clock [get_clocks clk_fpga_2] -max -add_delay 40.000 [
    get_ports FMC_SPI_MISO]
set_input_delay -clock [get_clocks clk_fpga_2] -min -add_delay 20.000 [
    get_ports RX_DAC_SDO]
set_input_delay -clock [get_clocks clk_fpga_2] -max -add_delay 40.000 [
    get_ports RX_DAC_SDO]


set_input_delay -clock [get_clocks adc_clk_p] -clock_fall -min -add_delay 0.600
     [get_ports {adc_n[*]}]
set_input_delay -clock [get_clocks adc_clk_p] -clock_fall -max -add_delay 2.000
     [get_ports {adc_n[*]}]
set_input_delay -clock [get_clocks adc_clk_p] -min -add_delay 0.600 [get_ports
    {adc_n[*]}]
set_input_delay -clock [get_clocks adc_clk_p] -max -add_delay 2.000 [get_ports
    {adc_n[*]}]
set_input_delay -clock [get_clocks adc_clk_p] -clock_fall -min -add_delay 0.600
     [get_ports {adc_p[*]}]
set_input_delay -clock [get_clocks adc_clk_p] -clock_fall -max -add_delay 2.000
     [get_ports {adc_p[*]}]
set_input_delay -clock [get_clocks adc_clk_p] -min -add_delay 0.600 [get_ports
    {adc_p[*]}]
```

```
set_input_delay -clock [get_clocks adc_clk_p] -max -add_delay 2.000 [get_ports
    {adc_p[*]}]



create_generated_clock -name {DAC_DATA_clk_p[0]} -source [get_pins design_1_i/
    DAC/oddr_0/inst/ODDR_inst/C] -divide_by 1 [get_ports {DAC_DATA_clk_p[0]}]
set_output_delay -clock [get_clocks {DAC_DATA_clk_p[0]}] -clock_fall -min -
    add_delay -1.000 [get_ports {DAC_to_pins_n[*]}]
set_output_delay -clock [get_clocks {DAC_DATA_clk_p[0]}] -clock_fall -max -
    add_delay 0.500 [get_ports {DAC_to_pins_n[*]}]
set_output_delay -clock [get_clocks {DAC_DATA_clk_p[0]}] -min -add_delay -1.000
     [get_ports {DAC_to_pins_n[*]}]
set_output_delay -clock [get_clocks {DAC_DATA_clk_p[0]}] -max -add_delay 0.500
    [get_ports {DAC_to_pins_n[*]}]
set_output_delay -clock [get_clocks {DAC_DATA_clk_p[0]}] -clock_fall -min -
    add_delay -1.000 [get_ports {DAC_to_pins_p[*]}]
set_output_delay -clock [get_clocks {DAC_DATA_clk_p[0]}] -clock_fall -max -
    add_delay 0.500 [get_ports {DAC_to_pins_p[*]}]
set_output_delay -clock [get_clocks {DAC_DATA_clk_p[0]}] -min -add_delay -1.000
     [get_ports {DAC_to_pins_p[*]}]
set_output_delay -clock [get_clocks {DAC_DATA_clk_p[0]}] -max -add_delay 0.500
    [get_ports {DAC_to_pins_p[*]}]

set_property PACKAGE_PIN U26 [get_ports ext_clk_p]
set_property IOSTANDARD LVCMOS25 [get_ports SPI_CLK_ADS4129]
set_property IOSTANDARD LVCMOS25 [get_ports SPI_CLK_CDCE62005]
set_property IOSTANDARD LVCMOS25 [get_ports SPI_CLK_DAC3171]
set_property IOSTANDARD LVCMOS25 [get_ports {DAC_SDENB[0]}]
set_property IOSTANDARD LVCMOS25 [get_ports {FMC_ADC_SDATA[0]}]
set_property IOSTANDARD LVCMOS25 [get_ports {FMC_ADC_SEN[0]}]
set_property IOSTANDARD LVCMOS25 [get_ports {FMC_SPI_LE_CLKGEN[0]}]
set_property IOSTANDARD LVCMOS25 [get_ports {FMC_SPI_MOSI[0]}]
set_property IOSTANDARD LVCMOS25 [get_ports {RX_DAC_SDIN[0]}]
set_property IOSTANDARD LVCMOS25 [get_ports {RX_DAC_SYNC_N[0]}]
set_property IOSTANDARD LVCMOS25 [get_ports FMC_ADC_OVR]
set_property IOSTANDARD LVCMOS25 [get_ports FMC_SPI_MISO]
set_property IOSTANDARD LVCMOS25 [get_ports RX_DAC_SDO]
set_property IOSTANDARD LVCMOS25 [get_ports SPI_CLK_AD5689]
set_property PACKAGE_PIN W28 [get_ports {RX_DAC_SDIN[0]}]
set_property PACKAGE_PIN V27 [get_ports {RX_DAC_SYNC_N[0]}]
set_property PACKAGE_PIN T29 [get_ports {FMC_ADC_SEN[0]}]
set_property PACKAGE_PIN U29 [get_ports FMC_ADC_OVR]
set_property PACKAGE_PIN T25 [get_ports SPI_CLK_AD5689]
set_property PACKAGE_PIN W30 [get_ports SPI_CLK_ADS4129]
set_property PACKAGE_PIN W29 [get_ports {FMC_ADC_SDATA[0]}]
set_property PACKAGE_PIN AE21 [get_ports SPI_CLK_CDCE62005]
set_property PACKAGE_PIN AA22 [get_ports {FMC_SPI_MOSI[0]}]
set_property PACKAGE_PIN AA23 [get_ports FMC_SPI_MISO]
```

```
set_property PACKAGE_PIN AH24 [get_ports {DAC_SDENB[0]}]
set_property PACKAGE_PIN AG25 [get_ports {FMC_SPI_LE_CLKGEN[0]}]
set_property PACKAGE_PIN AG22 [get_ports SPI_CLK_DAC3171]
set_property PACKAGE_PIN V29 [get_ports RX_DAC_SDO]

set_property PACKAGE_PIN V28 [get_ports RX_DAC_RESET]
set_property PACKAGE_PIN T24 [get_ports RX_DAC_LDAC_N]
set_property PACKAGE_PIN AG24 [get_ports FMC_PD_n_CLKGEN]
set_property PACKAGE_PIN AD21 [get_ports FMC_PLL_LOCK]

set_property IOSTANDARD LVCMOS25 [get_ports FMC_PD_n_CLKGEN]
set_property IOSTANDARD LVCMOS25 [get_ports FMC_PLL_LOCK]
set_property IOSTANDARD LVCMOS25 [get_ports RX_DAC_LDAC_N]
set_property IOSTANDARD LVCMOS25 [get_ports RX_DAC_RESET]




set_property PACKAGE_PIN AH23 [get_ports SPI_IO_DAC]
set_property IOSTANDARD LVCMOS25 [get_ports SPI_IO_DAC]
set_property SLEW SLOW [get_ports SPI_IO_DAC]

set_property DRIVE 16 [get_ports SPI_CLK_ADS4129]
set_property SLEW FAST [get_ports SPI_CLK_ADS4129]

set_property DRIVE 16 [get_ports {FMC_ADC_SDATA[0]}]
set_property DRIVE 16 [get_ports {FMC_ADC_SEN[0]}]

set_property OFFCHIP_TERM NONE [get_ports FMC_PD_n_CLKGEN]
set_property OFFCHIP_TERM NONE [get_ports RX_DAC_LDAC_N]
set_property OFFCHIP_TERM NONE [get_ports RX_DAC_RESET]
set_property OFFCHIP_TERM NONE [get_ports SPI_CLK_AD5689]
set_property OFFCHIP_TERM NONE [get_ports SPI_CLK_ADS4129]
set_property OFFCHIP_TERM NONE [get_ports SPI_CLK_CDCE62005]
set_property OFFCHIP_TERM NONE [get_ports SPI_CLK_DAC3171]
set_property OFFCHIP_TERM NONE [get_ports SPI_IO_DAC]
set_property OFFCHIP_TERM NONE [get_ports DAC_SDENB[0]]
set_property OFFCHIP_TERM NONE [get_ports FMC_ADC_SDATA[0]]
set_property OFFCHIP_TERM NONE [get_ports FMC_ADC_SEN[0]]
set_property OFFCHIP_TERM NONE [get_ports FMC_SPI_LE_CLKGEN[0]]
set_property OFFCHIP_TERM NONE [get_ports FMC_SPI_MOSI[0]]
set_property OFFCHIP_TERM NONE [get_ports RX_DAC_SDIN[0]]
set_property OFFCHIP_TERM NONE [get_ports RX_DAC_SYNC_N[0]]
set_false_path -from [get_clocks clk_fpga_2] -to [get_clocks -of_objects [
    get_pins design_1_i/ADC/clk_wiz_0/inst/mmcm_adv_inst/CLKOUT0]]
set_property C_CLK_INPUT_FREQ_HZ 300000000 [get_debug_cores dbg_hub]
set_property C_ENABLE_CLK_DIVIDER false [get_debug_cores dbg_hub]
set_property C_USER_SCAN_CHAIN 1 [get_debug_cores dbg_hub]
```

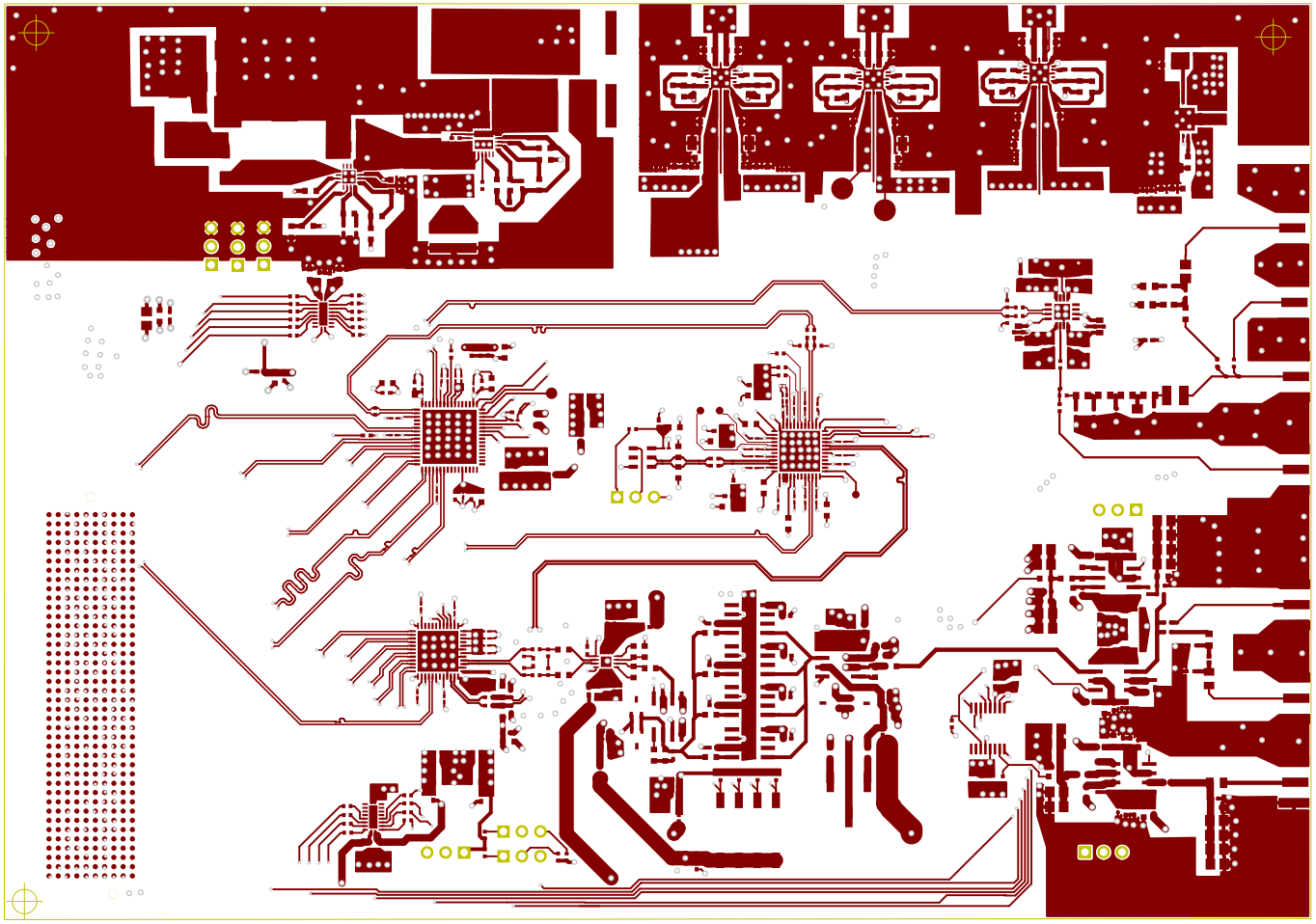
```
connect_debug_port dbg_hub/clk [get_nets design_1_i/ctrl/processing_system7_1/
    inst/FCLK_CLK1]
```

Appendix F

Board Layout

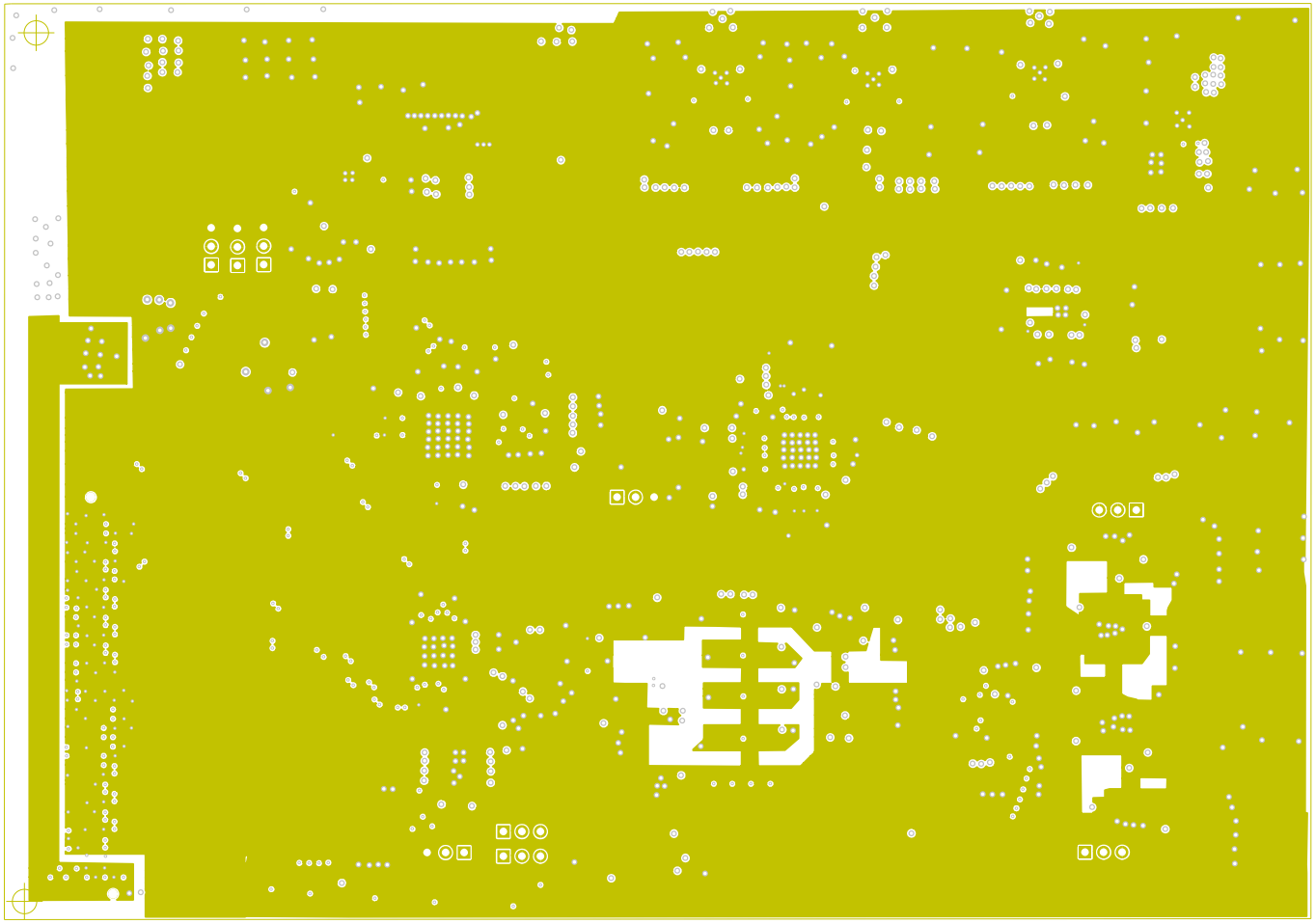
F.1 Board Layout

TOP COPPER



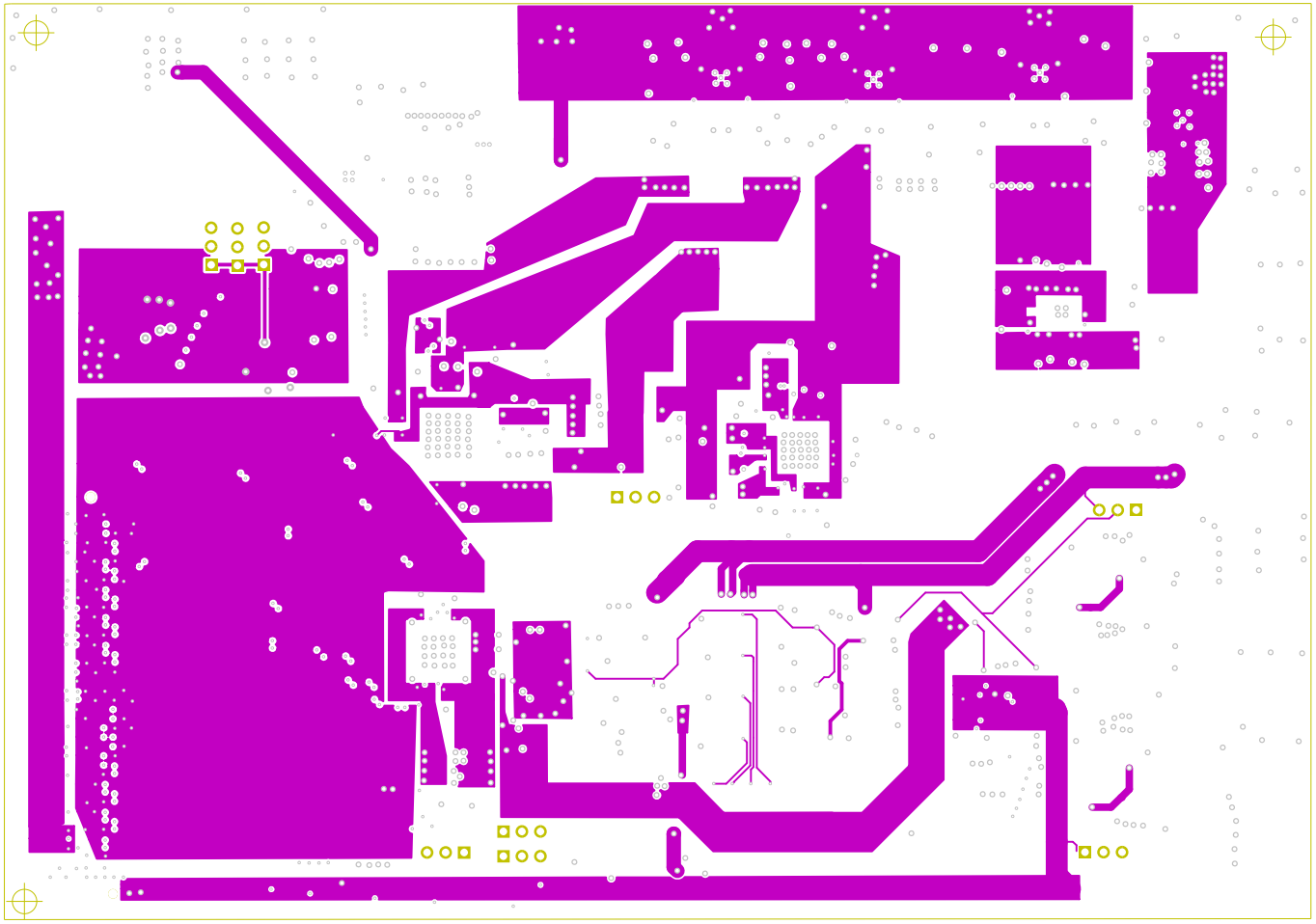
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Title: Implemented PCB		
Size: A4	Date: 2020-11-20	Rev:
KiCad E.D.A. kicad (5.1.5)-3		Id: 1/1

Inner Layer 1



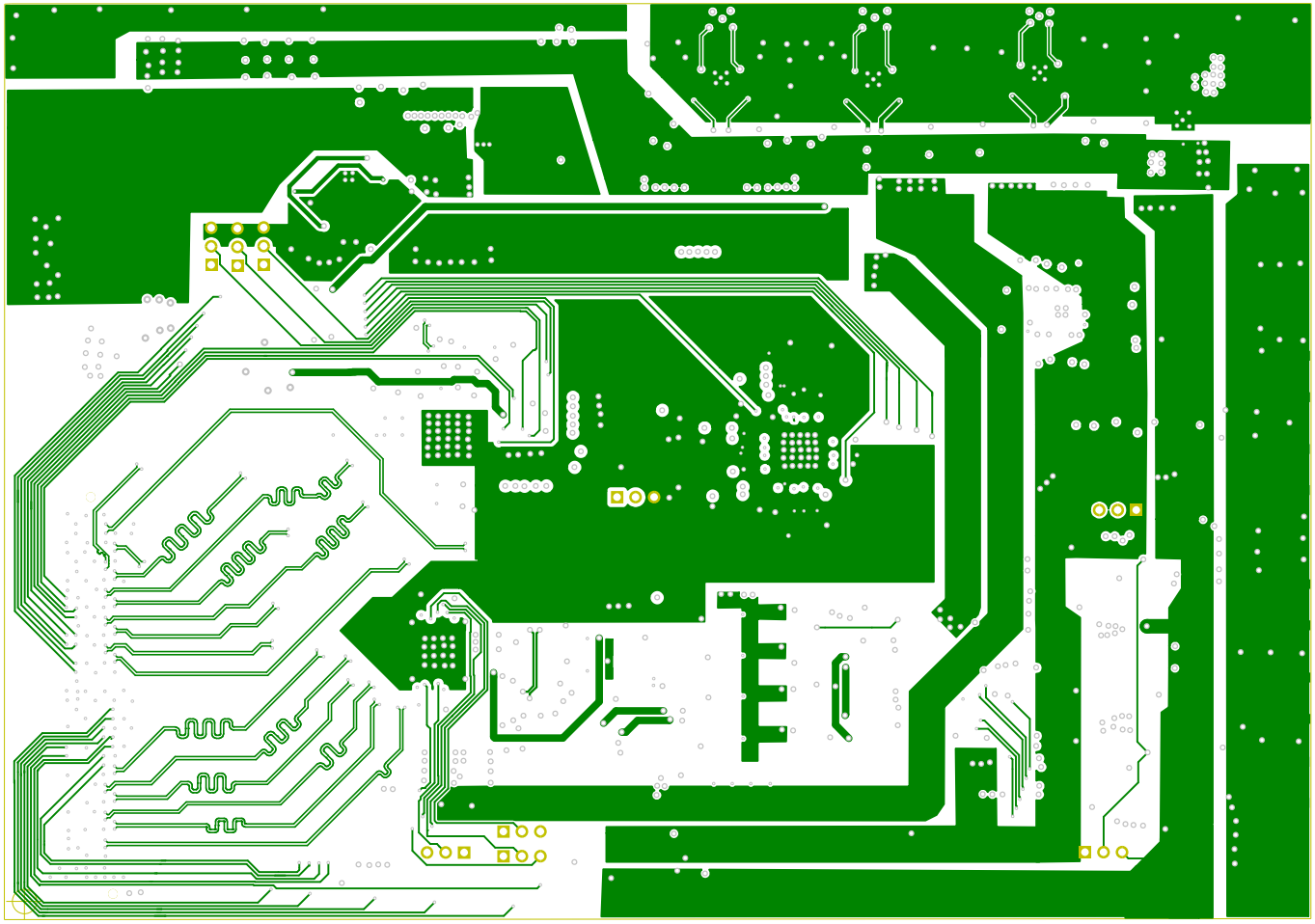
João Presa		
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Size: A4	Date: 2020-11-20	Rev:
KiCad E.D.A. kicad (5.1.5)-3		Id: 1/1

Inner Layer 2



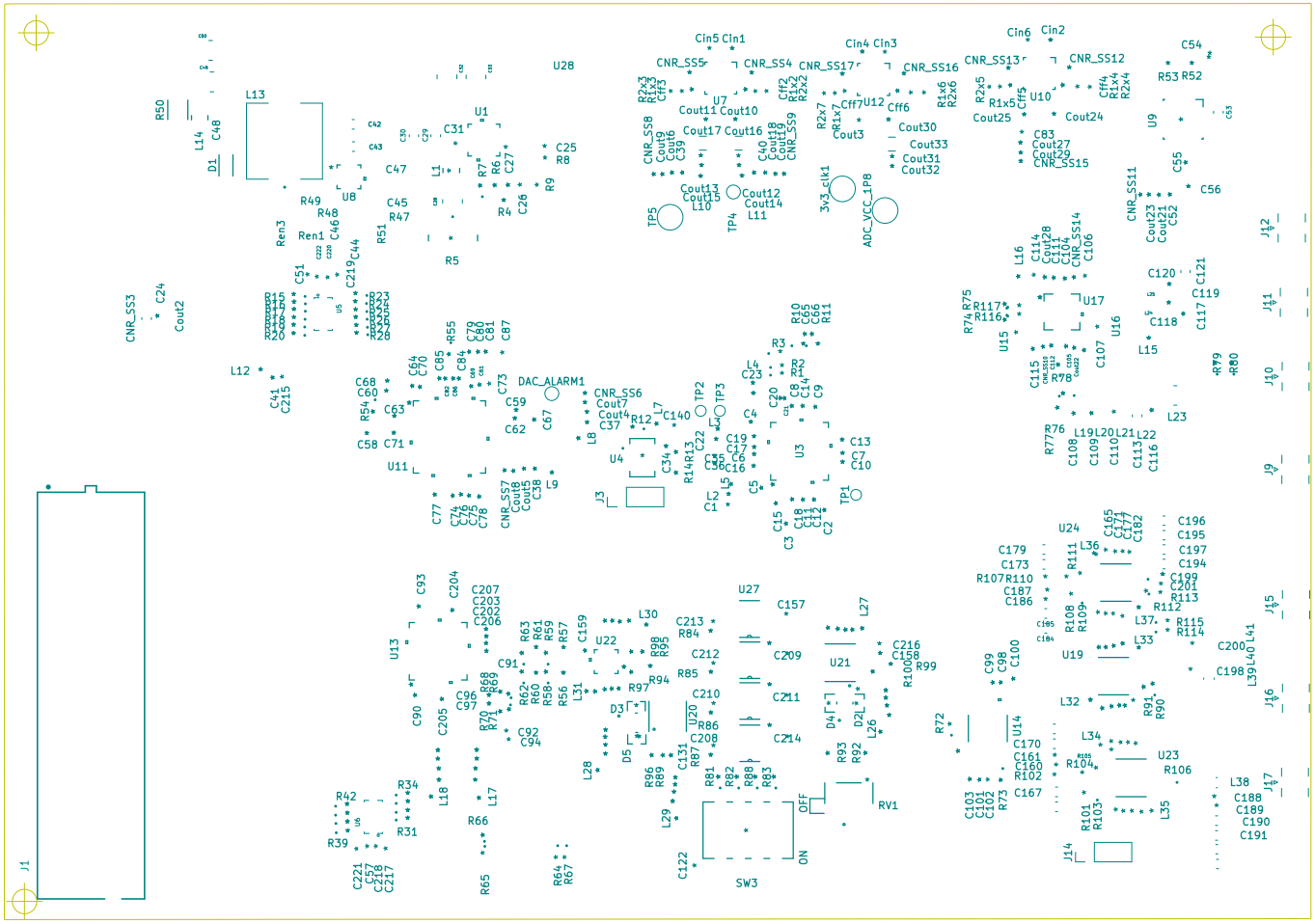
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KiCad E.D.A. kicad (5.1.5)-3		Id: 1/1

BACK COPPER



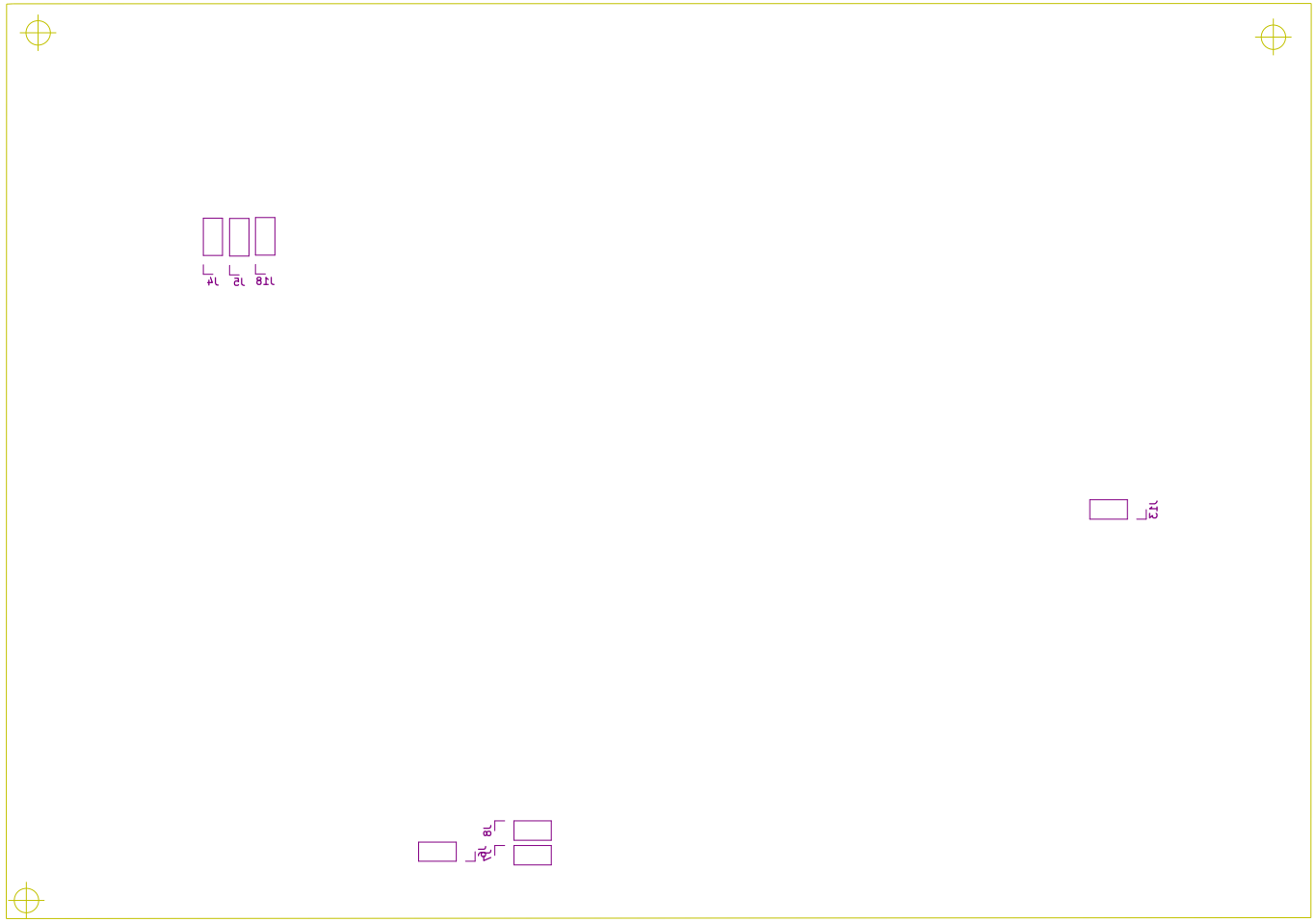
João Presa		
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Title: Implemented PCB		
Size: A4	Date: 2020-11-20	Rev:
KiCad E.D.A. kicad (5.1.5)-3		Id: 1/1

Front SilkS



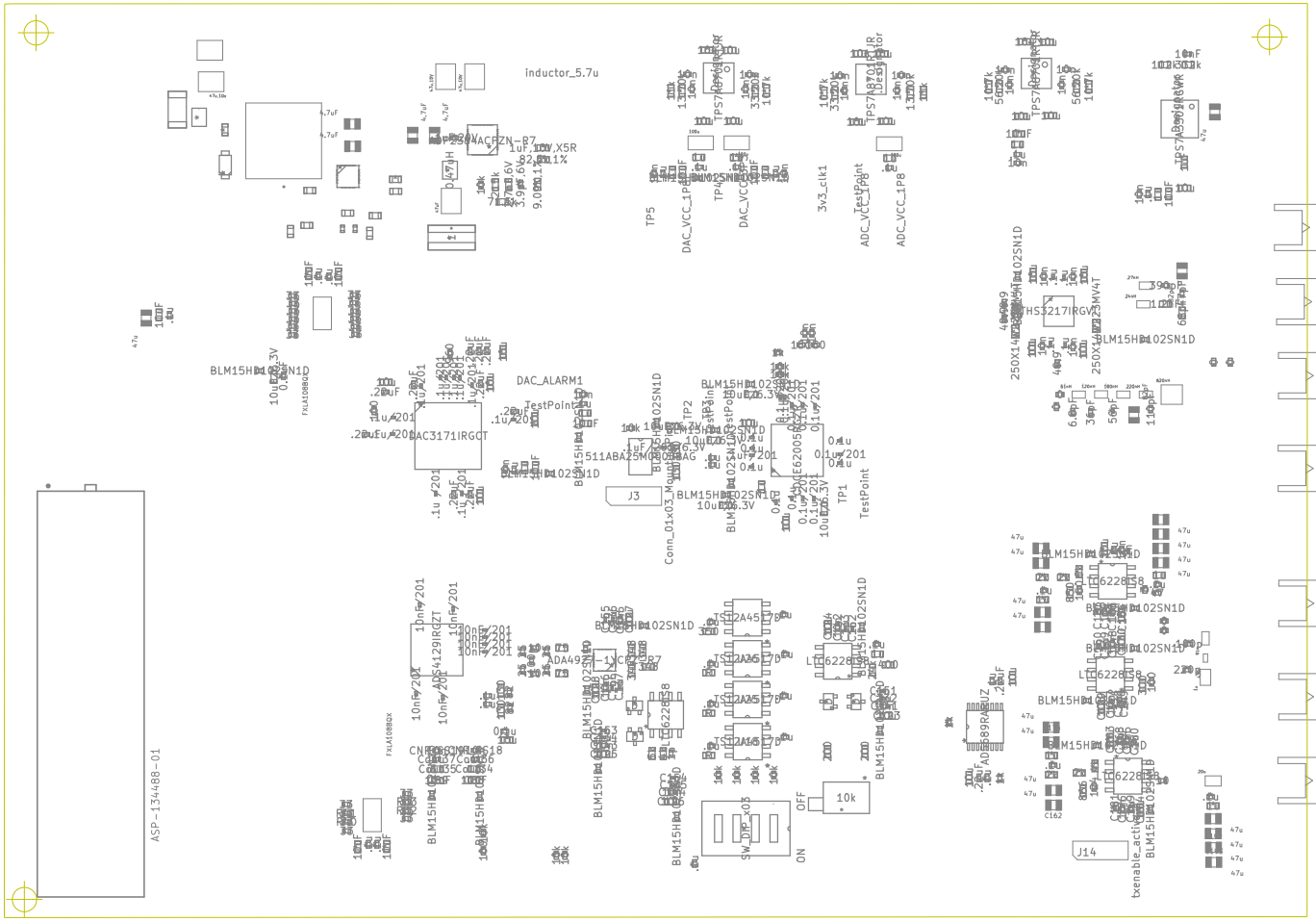
João Presa	
Sheet:	
File: pcb_rf_v0.kicad_pcb	
Title: Implemented PCB	
Size: A4	Date: 2020-11-20
KiCad E.D.A. kicad (5.1.5)-3	Rev: Id: 1/1

Back SilkS



João Presa		
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Size: A4	Date: 2020-11-20	Rev:
KiCad E.D.A. kicad (5.1.5)-3		Id: 1/1

Front Fab



João Presa		
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KiCad E.D.A. kicad (5.1.5)-3		Id: 1/1

References

[1] SA Wolf, DD Awschalom, RA Buhrman, JM Daughton, S Von Molnar, ML Roukes, A Yu Chtchelkanova, and DM Treger. Spintronics: a spin-based electronics vision for the future. *science*, 294(5546):1488–1495, 2001.

[2] John C Slonczewski et al. Current-driven excitation of magnetic multilayers. *Journal of Magnetism and Magnetic Materials*, 159(1):L1, 1996.

[3] S Il Kiselev, JC Sankey, IN Krivorotov, NC Emley, RJ Schoelkopf, RA Buhrman, and DC Ralph. Microwave oscillations of a nanomagnet driven by a spin-polarized current. *nature*, 425(6956):380–383, 2003.

[4] Sining Mao, Yonghua Chen, Feng Liu, Xingfu Chen, Bin Xu, Puling Lu, Mohammed Patwari, Haiwen Xi, Clif Chang, Brad Miller, et al. Commercial tmr heads for hard disk drives: characterization and extendibility at 300 gbit 2. *IEEE transactions on magnetics*, 42(2):97–102, 2006.

[5] Tetsuo Endoh and Hiroaki Honjo. A recent progress of spintronics devices for integrated circuit applications. *Journal of Low Power Electronics and Applications*, 8(4):44, 2018.

[6] U Ebels, J Hem, A Purbawati, A Ruiz Calafora, C Murapaka, L Vila, K Jaimes Merazzo, E Jimenez, M-C Cyrille, R Ferreira, et al. Spintronic based rf components. In *2017 Joint Conference of the European Frequency and Time Forum and IEEE International Frequency Control Symposium (EFTF/IFCS)*, pages 66–67. IEEE, 2017.

[7] Abbass Hamadeh. *Synchronization of spin trasnsfer nano-oscillators*. PhD thesis, Paris 11, 2014.

[8] Romain Lebrun. *Vortex magnétiques couplés dans des oscillateurs à transfert de spin: de l'excitation résonante à la synchronisation mutuelle*. PhD thesis, 2015.

[9] E Grimaldi, R Lebrun, A Jenkins, A Dussaux, J Grollier, V Cros, A Fert, H Kubota, K Yakushiji, A Fukushima, et al. Spintronic nano-oscillators: Towards nanoscale and tunable frequency devices. In *2014 IEEE International Frequency Control Symposium (FCS)*, pages 1–6. IEEE, 2014.

[10] JD Costa, S Serrano-Guisan, B Lacoste, AS Jenkins, T Böhnert, M Tarequzzaman, J Borme, FL Deepak, E Paz, J Ventura, et al. High power and low critical current density spin transfer torque nano-oscillators using mgo barriers with intermediate thickness. *Scientific reports*, 7(1):1–9, 2017.

[11] A Dussaux, E Grimaldi, B Rache Salles, AS Jenkins, AV Khvalkovskiy, P Bortolotti, J Grollier, H Kubota, A Fukushima, K Yakushiji, et al. Large amplitude spin torque vortex oscillations at zero external field using a perpendicular spin polarizer. *Applied Physics Letters*, 105(2):022404, 2014.

[12] Joo-Von Kim. Spin-torque oscillators. In *Solid State Physics*, volume 63, pages 217–294. Elsevier, 2012.

[13] Luc Berger. Emission of spin waves by a magnetic multilayer traversed by a current. *Physical Review B*, 54(13):9353, 1996.

[14] Hyun Seok Choi, Sun Yool Kang, Seong Jun Cho, Inn-Yeal Oh, Mincheol Shin, Hyuncheol Park, Chaun Jang, Byoung-Chul Min, Sang-Il Kim, Seung-Young Park, et al. Spin nano–oscillator–based wireless communication. *Scientific reports*, 4(1):1–7, 2014.

[15] Steven Louis, Vasyl Tyberkevych, Jia Li, Ivan Lisenkov, Roman Khymyn, Elena Bankowski, Thomas Meitzler, Ilya Krivorotov, and Andrei Slavin. Low power microwave signal detection with a spin-torque nano-oscillator in the active self-oscillating regime. *IEEE Transactions on Magnetics*, 53(11):1–4, 2017.

[16] S Miwa, S Ishibashi, H Tomita, T Nozaki, E Tamura, K Ando, N Mizuochi, T Saruya, H Kubota, K Yakushiji, et al. Highly sensitive nanoscale spin-torque diode. *Nature materials*, 13(1):50–56, 2014.

[17] K Yu Guslienko. Magnetic vortex state stability, reversal and dynamics in restricted geometries. *Journal of nanoscience and nanotechnology*, 8(6):2745–2760, 2008.

[18] A Dussaux, AV Khvalkovskiy, P Bortolotti, J Grollier, V Cros, and A Fert. Field dependence of spin-transfer-induced vortex dynamics in the nonlinear regime. *Physical Review B*, 86(1):014402, 2012.

[19] AA Thiele. Steady-state motion of magnetic domains. *Physical Review Letters*, 30(6):230, 1973.

[20] Jiadong Zang, Vincent Cros, and Axel Hoffmann. *Topology in Magnetism*, volume 192. Springer, 2018.

[21] A Litvinenko, P Sethi, C Murapaka, A Jenkins, V Cros, P Bortolotti, R Ferreria, B Dieny, and U Ebels. Analog and digital phase modulation of spin torque nano-oscillators. *arXiv preprint arXiv:1905.02443*, 2019.

[22] A Purbawati, F Garcia-Sanchez, LD Buda-Prejbeanu, and U Ebels. Enhanced modulation rates via field modulation in spin torque nano-oscillators. *Applied Physics Letters*, 108(12):122402, 2016.

[23] R Sharma, P Dürrenfeld, M Ranjbar, RK Dumas, Johan Åkerman, and PK Muduli. Modulation rate study in a spin-torque oscillator-based wireless communication system. *IEEE Transactions on Magnetics*, 51(11):1–4, 2015.

[24] Alex S Jenkins, Lara Alvarez, San Emeterio, Roberta Dutra, Rubem L Sommer, Paulo P Freitas, and Ricardo Ferreira. A multi-band analogue frequency sensor with sub-mhz resolution based on a vortex nano-oscillator. *arXiv preprint arXiv:1806.06002*, 2018.

[25] AS Jenkins, R Lebrun, E Grimaldi, S Tsunegi, P Bortolotti, H Kubota, K Yakushiji, A Fukushima, G De Loubens, Olivier Klein, et al. Spin-torque resonant expulsion of the vortex core for an efficient radiofrequency detection scheme. *Nature nanotechnology*, 11(4):360, 2016.

[26] Author. *ZC706 Evaluation Board for the Zynq-7000 XC7Z045 SoC: User Guide*. XILINX.

[27] Author. *Zynq-7000 SoC Packaging and Pinout: Product Specification UG865*. XILINX.

[28] Author. *7 Series FPGAs SelectIO Resources: User Guide 471*. XILINX.

[29] Texas Instruments. *DAC31x1 Single-Channel, 14-,12-, and 10-Bit, 500-MSPS, Digital-to-Analog Converters*, 2013. Rev. D.

[30] Texas Instruments. *12-/14-Bit, 160/250MSPS, Ultralow-Power ADC*, 2009. Rev. G.

[31] Texas Instruments. *THS3217 DC to 800-MHz, Differential-to-Single-Ended, DAC Output Amplifier*, 2016. Rev. B.

[32] Texas Instruments. *THS3215EVM and THS3217EVM User's Guide, Differential-to-Single-Ended, DAC Output Amplifier*, 2016. Rev. A.

[33] RF Tools. Lc filter design tool, 2020. URL: https://rf-tools.com/lc-filter/.

[34] ANALOG DEVICES. *Dual, 16-/12-Bit nanoDAC+ with SPI Interface*, 2013. Rev. B.

[35] ANALOG DEVICES. *Op Amp Noise Relationships: 1/f Noise, RMS Noise, and Equivalent Noise Bandwidth*, 2008. Rev. 0.

[36] ANALOG DEVICES. *0.88nV/Hz 730MHz, 500V/µs, Low Distortion Rail-to-Rail Output Op Amps with Shutdown*, 2019. Rev. B.

[37] ANALOG DEVICES. Ltspice. URL: https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html.

[38] Per Magnusson. Voltage and current noise sources in ltspice .noise simulations, 2017. URL: https://axotron.se/blog/voltage-and-current-noise-sources-in-ltspice-noise-simulations/.

[39] On Semiconductor. *MMBD330T1G, SMMBD330T1G, MMBD770T1G, SMMBD770T1G - Schottky Barrier Diodes*, 2011. Rev. 6.

[40] Texas Instruments. *CDCE62005 3:5 Clock Generator, Jitter Cleaner with Integrated Dual VCOs*, 2008. Rev. G.

[41] Wayne Green Rob Reeder and Robert Shillito. Analog-to-digital converter clock optimization: A test engineering perspective. *Analog Dialogue 42-02*, 2008.

[42] Kal Mustafaa and Chris Sterzik. Ac-coupling between differential lvpecl, lvds, hstl, and cml. *High Performance Analog*, 2003.

[43] Kal Mustafaa and Chris Sterzik. Adc-coupling between differential lvpecl, lvds, hstl, and cml. *High Performance Analog*, 2003.

[44] Texas Instruments. *TPS7A87 Dual, 500-mA, Low-Noise (3.8 VRMS), LDO Voltage Regulator*, 2016. Rev. A.

[45] Texas Instruments. *TPS7A33 –36-V, 1-A, Ultralow-Noise Negative Voltage Regulator*, 2011. Rev. D.

[46] ANALOG DEVICES. Ad-fmcdaq2-ebz user guide, 2019. URL: https://wiki.analog.com/resources/eval/user-guides/ad-fmcdaq2-ebz.

[47] JLCPCB. Jlcpcb, 2020. URL: https://jlcpcb.com/.

[48] Texas Instruments. *High-Speed Layout Guidelines for Signal Conditioners and USB Hubs*, 2018.

[49] XILINX. *Vivado Design Suite Vivado AXI Reference Guide*, 2017. Rev. 4.

[50] XILINX. *AXI DMA v7.1 LogiCORE IP Product Guide*, 2019.

[51] Texas Instruments. *LM4140 High Precision Low Noise Low Dropout Voltage Reference*, 2000. Rev. F.

[52] ANALOG DEVICES. *Precision Wide Supply High Output Drive Low Noise Reference*, 2020. Rev. 1.

[53] Texas Instruments. *0.05V/°C max, SINGLE-SUPPLY CMOS OPERATIONAL AMPLIFIERS Zero-Drift Series*, 2003. Rev. 1.

[54] Texas Instruments. *REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference*, 2007. Rev. H.

[55] Estelle M. Philips and Derek S. Pugh. *How to Get a PhP*. Open University Press, Fourth edition, 2005.

[56] José Diogo Teixeira Barbosa Costa. Spin-transfer-torque nano-oscillators: fabrication, characterization and dynamics. 2017.