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OPTIMIZATION AND SCALING-UP OF PEROVSKITE SOLAR CELLS DEPOSITION

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Abstract

Renewable energy sources contribution to global energy demand has increased in the past few years, with solar photovoltaic among the most promising alternatives for replacing fossil fuels. In this field, perovskite solar cells (PSCs) have emerged with an unparalleled performance evolution in the photovoltaic field. However, this technology is still not available at commercial level due to some technological limitations, as it is typical in emergent technologies, particularly related to stability, upscaling and environmental impact. This thesis aims at contributing to PSC upscaling, forecasting the preparation of 5 cm^2 individual PSC devices with 9 % power conversion efficiency (PCE) for posterior assembling of a 10 x 10 cm^2 module. This module configuration was simulated using the software tool LAOSS, able to optimize electrical interconnection in perovskite modules.

After experimental optimization of the perovskite deposition step in 5 cm^2 devices, the best performing PSC cell reached a power conversion efficiency of 8.95 %. Then, this characteristic curve was used as input performance curve of the software for the electrical design study of the 10x10 cm^2 module and its interconnections The simulation results showed that the total gap width plays a big role in the module performance, with power conversion efficiency and fill factor being especially harmed with increasing gap width. In terms of interconnection segments, the simulations demonstrated that P1 and P3 should be as narrow as possible (50 μm is enough), only needing to be wide enough to avoid short-circuits. Concerning the division of a module in sub-cells, the simulation output also showed a reduction in the ideal number of sub-cells for increasing gap width, which is also translated in a larger individual sub-cell width. The series resistance between the contact of the back-contact of a sub-cell with the front-contact of the following, in the P2 zone, also proved to have a strong impact on the module performance, with higher resistances leading to significant power losses.

In parallel with the simulation work, the most recent reported upscaling strategies have been investigated, which allowed to contribute to a review paper that is now under submission process.

In conclusion, for producing efficient large-scale perovskite modules, it is very important to have a very precise laser ablation process to minimize the scribe dimensions for the interconnections, minimizing dead areas and creating smooth scribes, avoiding electrical losses. It is also important to complement laboratorial developments with theoretical predicting tools, allowing to know beforehand the dimensions that better suit the module fabrication.

Keywords: Perovskite Solar Cell; Module; Upscaling; Optimization; Simulation.

Resumo

A contribuição das fontes de energia renováveis para o consumo energético mundial tem vindo a aumentar nos últimos anos, com a energia fotovoltaica entre os mais promissores candidatos para substituir a utilização de combustíveis fósseis. Nesta área, as células solares de perovskita têm ganho extraordinário destaque, com uma evolução de desempenho sem paralelo no setor fotovoltaico. No entanto, esta tecnologia ainda não está disponível a nível comercial, devido a algumas limitações tecnológicas, como é habitual em tecnologias emergentes, particularmente relacionadas com a estabilidade, aumento de escala e impacto ambiental. Esta tese tem como objetivo contribuir para o aumento de escala, considerando a preparação de células de 5 cm^2 com 9 % de eficiência para posterior fabrico de um módulo com 10 x 10 cm^2. A configuração deste módulo foi simulada com recurso ao software LAOSS, capaz de otimizar o desempenho elétrico em módulos de perovskita.

Após otimização experimental da deposição de perovskita para células com 5 cm^2, a melhor célula fabricada registou uma eficiência de 8,95 %. A respetiva curva característica foi usada como base para o estudo do dimensionamento de um módulo com 10 x 10 cm^2 e as suas interconexões. Os resultados das simulações mostraram que a largura total do intervalo entre duas sub células tem uma grande influência no desempenho do módulo, tendo-se verificado um decréscimo sobretudo da eficiência e do fator de preenchimento com o aumento desta largura. Em termos dos segmentos da interconexão, as simulações mostraram que o P1 e o P3 deviam ser o mais estreitos possível (50 μm são suficientes), estreitos o suficiente apenas para evitar curto-circuitos. No que toca à divisão do módulo, as simulações também mostraram um número ideal de sub células decrescente com o aumento da largura total da interconexão, o que também se traduz num aumento da largura individual de cada sub célula. A resistência em série entre o contra elétrodo de uma sub célula e o foto elétrodo da seguinte, na zona do P2, também demonstrou ter um impacto significativo no desempenho módulo.

Em paralelo com os trabalhos de simulação, foram também estudados os mais recentes trabalhos sobre estratégias para o aumento de escala, tendo resultado numa contribuição para um artigo de revisão, presentemente em processo de submissão.

Concluindo, para produzir módulos de perovskita com bom desempenho, é de elevada importância que se tenha ao dispor uma ferramenta laser de corte e remoção muito precisa, permitindo reduzir a largura da interconexão, reduzindo as áreas inativas do dispositivo, e criando cortes suaves e uniformes para evitar perdas resistivas. É também fundamental que se complemente desenvolvimentos laboratoriais com ferramenta teóricas de previsão, permitindo adquirir o conhecimento prévio das dimensões mais adequadas para o fabrico de um módulo com um bom desempenho.

Declaration

I hereby declare, under word of honor, that this work is original and that all non-original contributions are indicated, and due reference is given to the author and source.

6 / 7 / 2020

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Notation and Glossary

FF	Fill factor	
GFF	Geometric fill factor	
I	Output current	A
I_D	Diode current	A
I_L	Photo-generated current	A
I_{SC}	Short-circuit current	A
I_{SH}	Shunt current	A
J_{SC}	Short-circuit current density	$mA \cdot cm^{-2}$
R_S	Series resistance	Ω
R_{SH}	Shunt resistance	Ω
V	Voltage	V
V_{OC}	Open-circuit voltage	V
w_{P1}	P1 width	μm
w_{P2}	P2 width	μm
w_{P3}	P3 width	μm

Greek symbols

η	Power conversion efficiency

Acronym list

AZO	Aluminum-doped Zinc Oxide
CAD	Computer Aided Design
CdTe	Cadmium-telluride
CIGS	Copper-indium-gallium-selenide
DMF	Dimethylformamide
DMSO	Dimethyl sulfoxide
dxf	Drawing eXchange Format
EBL	Electron Blocking Layer
ETL	Electron Transport Layer
FA	Formamidinium
FK209	tris(2-(1H-pyrazol-1-yl)-4-tert-butylpyridine)cobalt(III) tri[bis(trifluoromethane)sulfonimide]
FTO	Fluorine-doped Tin Oxide
HTL	Hole Transport Layer
I-V	Current-Voltage
ITO	Indium-doped Tin Oxide
LED	Light-emitting diode
LEPABE	Laboratory for Process Engineering, Environment, Biotechnology and Energy
LEPAE	Laboratory for Process Engineering, Environment and Energy
LiTFSI	Lithium bis(trifluoromethanesulfonyl)imide
MA	Methylammonium
P3HT	Poly(3-Hexylthiophene-2,5-Diyl)
PCBM	Phenyl-C61-Butyric-Acid-Methyl Ester
PCE	Power Conversion Efficiency
PEDOT:PSS	Poly(3,4-Ethylenedioxythiophene) Polystyrene Sulfonate
PSC	Perovskite Solar Cell
PTAA	Poly(triarylamine)
PV	Photovoltaic
R2R	Roll-to-roll
Spiro-OMeTAD	2,2′,7,7′-tetrakis(N,N-di-p-methoxyphenylamine) 9,9′-spirobifluorene
THG-YAG	Third Harmonic Generation - Yttrium Aluminium Garnet
TCO	Transparent Conducting Oxide
UV	Ultraviolet

1 Introduction

1.1 Framing and presentation of the work

With growing world population and industrialization, the energy demand over the past years has immensely increased. In just 40 years, the global primary energy consumption has almost duplicated, ranging from 81 339 TWh in 1978 to more than 155 000 in 2018 [6]. Especially since the industrial revolution, mankind has been attracted to the apparent abundancy and easy processing of coal and crude oil (and its derivatives), making them the most used energy source, as the local biomass utilization was not enough for answering the industrial needs. However, these reserves demonstrated that they were not so abundant as expected, along with an even more serious issue: environmental impact. The burning of coal, fuels derived from crude oil (such as diesel, gasoline, kerosene) and most natural gas streams emit large quantities of CO_2, responsible to the greenhouse effect. Besides, these combustion reactions produce large amounts of small particles, NO_x, SO_x, and carbon monoxide, all very harmful to human health.

For these reasons, the need for finding truly abundant and non-polluting energy sources and its large-scale implementation is imperative. Actually, since the first hydropower units in the XIX century, energy harvesting from renewable sources is increasing, reaching 26 % contribution for global electricity generation in 2018 [7]; hydropower, wind power and solar photovoltaic (PV) are the major contributors for this increase. In particular, solar PV has had an enormous grow in the last decade, and the International Energy Agency predicts that it is going to be the greatest electricity source by 2035 [8].

The photovoltaic phenomenon was first discovered in France in 1839, by Edmond Becquerel, who first noticed the production of an electrical current when assembling two plates of platinum or gold in an acid, neutral or alkaline solution when exposed to solar radiation [9]. Notably, this remarkable discovery gave the name to the “European Becquerel Prize for Merits in Photovoltaics”, an annual prize that distinguishes the best researchers in PV science around the world. Later, in 1883, Charles Fritts built the first solid-state PV device, by coating the semiconductor selenium with a transparent gold layer [9]. It should be noted that only in 1897 the existence of the electron was proven, so the scientific mechanism behind current photogeneration was not fully understood by the time. In 1930, Walter Schottky – doctoral student of Max Planck – provided an interpretation of the PV effect in semiconductor/metal contacts, but only years later Russell Ohl presented an understanding of the p-n junction, and built a PV cell with semiconductor doping. While working at Bell Laboratories in United States, in 1941 he filled the patent for the modern solar cell, that would be granted five years later. These cells were already fabricated with silicon, and many others soon followed Ohl steps at

Bell Labs, and finally in 1953 the first practical solar cell was built, using boron doping [9], giving birth to the first generation of photovoltaic solar cells.

The first generation of PV devices is composed by single-junction cells of monocrystalline or polycrystalline silicon devices, assembled by wafer connecting. These are the most common photovoltaic installations worldwide and represent about 85 % of the PV market share [10]. These cells usually have better efficiencies and stability than other types, but the fabrication cost is also high [10].

The second generation of photovoltaics is also constituted by single-junction cells, but the materials used are amorphous silicon, cadmium-telluride (CdTe), gallium-arsenide, and copper-indium-gallium-selenide (CIGS). Except for gallium-arsenide, the cells are now built with thin film technology, and not with the wafer connection used in the crystalline silicon devices. This generation cells offer cheaper processing methods but falls short on efficiency when compared to the first generation devices. Moreover, some of the materials used are rare or toxic [11].

Although some authors claim that there is a fourth generation on the way, consisting of composite materials [12], it is the third generation that has been on the spotlight for emerging PV research. This new generation consists of organic-based solar cells, such as dye-sensitized solar cells, quantum dot–sensitized solar cells, hybrid solar cells, polymer-based solar cells, perovskite solar cells and multi-junction solar cells [13]. So, this generation is basically divided in organic-based and multi-junction solar cells. Multi-junctions provide outstanding efficiencies despite still at very costly and complex fabrication processes, but are certainly a technology to keep in mind for the future. Organic materials, on the other hand, are cheaper than the common 1st and 2nd generation feedstocks, very promising for a large scale, cheap and efficient PV fabrication, along with the benefit; these organic compounds allow different and nicer colors than those of blue silicon or dark grey/black typical of 2nd generation devices, which facilitates building integration. Also, these organic devices are easier to incorporate in flexible substrates [10].

In particular, **perovskite solar cells** (PSCs) are among the most promising technologies in the PV field in the last few years. Perovskite is a class of materials with an ABX_3 crystallographic structure. A and B refer to cations (A larger than B), and X is an anion: usually a halogen or oxide. Perovskite discovery goes back to 1839, when the Russian mineralogist Perovski identified a sample of calcium titanate, $CaTiO_3$ [14]. Soon, the great properties of these materials such as high-absorption coefficient, long-range ambipolar charge transport, low exciton-binding energy, high dielectric constant or ferroelectric properties caught scientific attention, especially for optoelectronic and photovoltaic applications [14]. Figure 1.1.1 shows a typical chemical configuration for a cubic crystal structure perovskite. Crystal structure may change, according to the tolerance factor, which depends on the radius of each element.

The first PSC was fabricated in 2009, and the researchers reached a power conversion efficiency (PCE) of 3.8 % [15]. Just ten years later, in early 2019, a record of 25.2 % PCE was obtained at a joint work between Korea University and MIT [1]. This quick evolution has no parallel in the PV field, which can be proved by the PCE evolution plot – Figure 1.1.2. Perovskite precursors are cheap, abundant, and easily solution processed [14]. Another advantage of this semiconductor material is the widely tunable band gap. This is not only due to the intrinsic tuning of composition, derived from the choice and relative quantities of the precursors in a perovskite, but also a result of the ease in controlling their dimensionality.

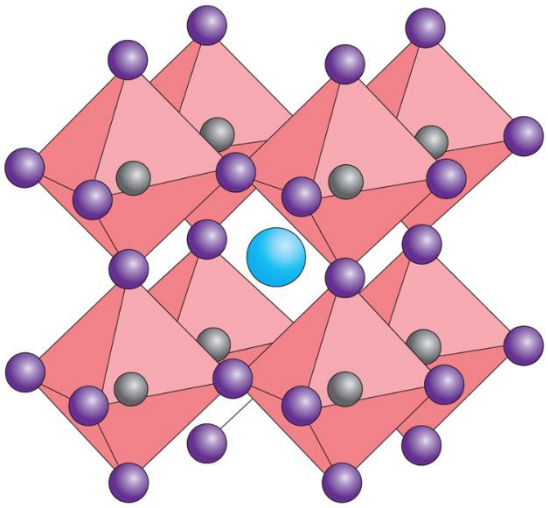

Figure 1.1.1 - Cubic perovskite structure. Blue dot represents A cation, grey dots B cation and X is the anion [2].

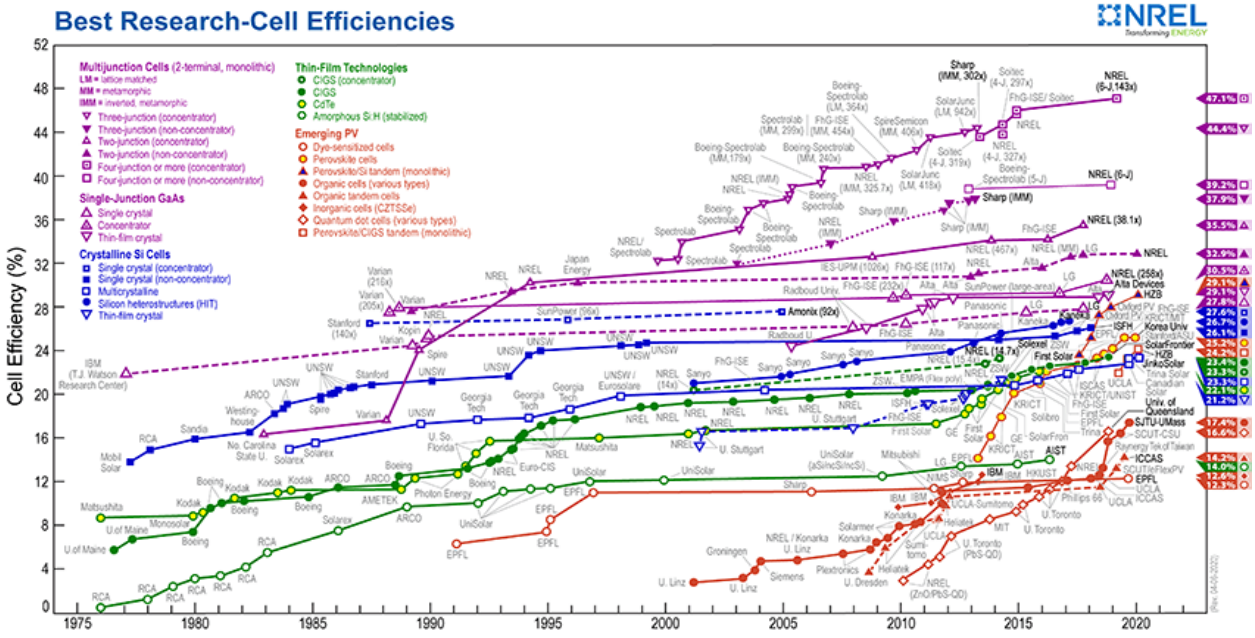

Figure 1.1.2 – PV technologies efficiency evolution [1].

Besides that, perovskite harvests diffuse light with a rather high efficiency [16]. All these factors certainly make very interesting the investigation in developing this PV technology, and that is why perovskite-based PV devices have been one of the leaders in the race for finding a true alternative to silicon technology. Figure 1.1.3 shows an example of a PSC device.

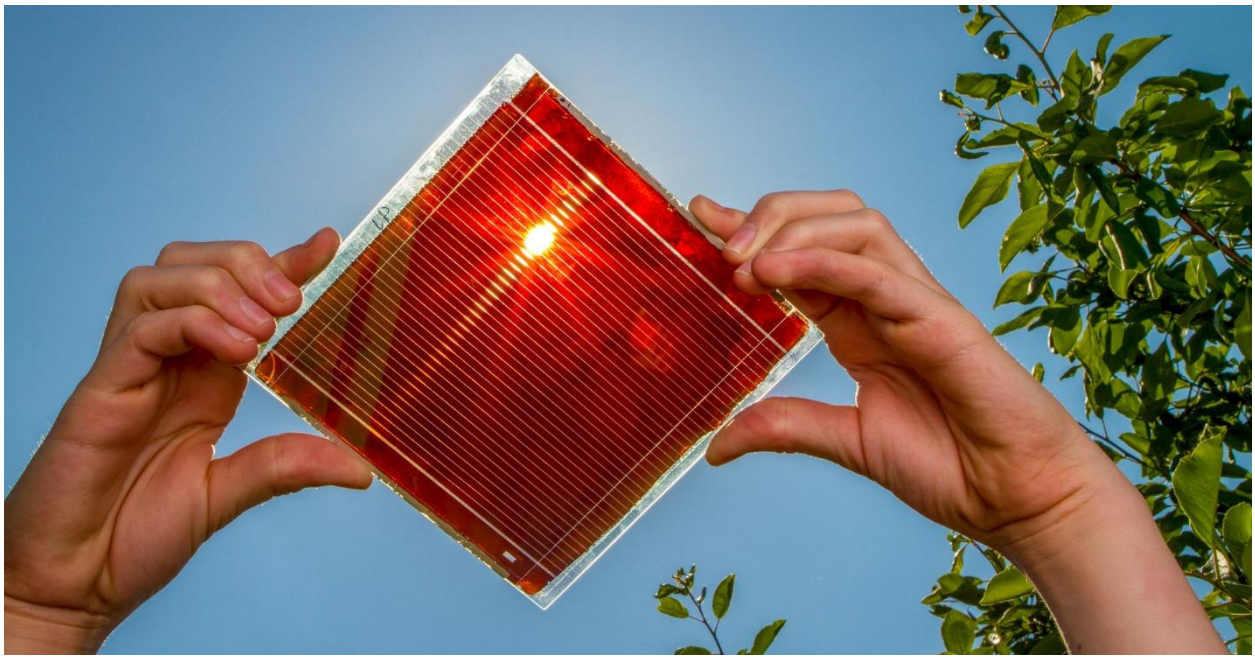

Figure 1.1.3 - Perovskite device [3].

Besides all the advantageous characteristics mentioned before, PSCs are still not available at commercial level. This quick evolution is naturally related to small size devices (< 1 cm^2), while works on larger areas and module configuration still need further studies. For the upscaling of perovskite devices, two main limiting factors must be considered: defective perovskite deposition in large scale and glass substrates series resistance impact on large devices. Other important limiting factors when considering commercialization are stability, economical output, architectural integration and environmental safety.

Since engineering is also synonym of building large-scale and human-useful resources, the main goal of this work is to contribute to tackle challenges found upon upscaling the perovskite devices. More specifically, the first objective of this work was to build, in the laboratory, a PSC module with an active area of 50 cm^2, optimizing the necessary parameters along the fabrication process, as well as to optimize the perovskite film deposition by slot-die technique. Due to laboratory closure upon covid-19 epidemic directives, the thesis objectives were redefined, focusing in a more theoretical work. First, a complete bibliographic overview of the most promising deposition techniques for addressing upscaling purposes, challenges of the glass substrates series resistance and module configurations was conducted, resulting in the participation of a review paper on PSC [17]. Then, a software to design and optimize large area semiconductor devices – LAOSS by FLUXiM AG [18] - was used for assessing the optimized electrical parameters for preparing an efficient module design of 100 cm^2. Several sizes, number of individual cells and shapes, distance between contacts and dead-areas were simulated.

1.2 Presentation of the lab

LEPABE, Laboratory for Process Engineering, Environment, Biotechnology and Energy was founded in 1997 by professor Carlos Costa (under the name of LEPAE), with the aim to "develop fundamental and applied knowledge in complex systems by using methodologies both from the systems engineering and social sciences areas, like case study based research, and from meso scale chemical engineering", on the words of its founder. The lab is a research unit of the Chemical Engineering Department of the Faculty of Engineering of the University of Porto and has approximately 220 research members.

The mission of LEPABE is to reinforce the excellence in science and investigation, increasing knowledge in technologies and procedures, through focusing on advanced manufacturing and processing, advanced materials, nanotechnologies, and biotechnology. The laboratory and its elements also aim to enhance regional competitiveness of industry of the Northern region of Portugal, always providing solutions to help address major concerns shared by society: making renewable energy more affordable, ensuring food safety, solving emergent problems affecting water and air quality and efficiently recycling industrial residues.

LEPABE's activity is divided into five groups: Processes, Products and Energy; Process Systems Engineering; Biotechnology; Supramolecular Assemblies; and Environmental Sciences and Technologies. Seven spin-off companies have been born form LEPABE: SYSADVANCE, Advanced Cyclone Systems, BioMode, VisBlue, Amnis Pura, Pixel Voltaic and OFRTECH [19].

1.3 Contribution of the author to the work

For this work, I have fabricated and characterized all the cells. The dimensions I used were not used before in the host laboratory, so that I had to adjust some details along the fabrication proceedings. Also, I performed all the simulations mentioned. Although many simulation works have previously been reported on perovskite module fabrication, this is, as far as my research goes, the first work performed using LAOSS. For that reason, the methodology applied in the simulations was defined by me, since I learnt to use the software by myself, with help from the tutorial and manual provided by the FLUXiM, whose support team also cleared a few doubts along the way.

1.4 Organization of the thesis

This first chapter of **introduction** presented the motivation behind this work and the main objectives to be followed. The next chapter, **context and state of the art**, gives a comprehensive analysis of the issues to be addressed within the thesis, as well as an overview of the most important works reported on the development of perovskite devices into a

commercial technology. The third chapter, **materials and methods**, will provide a detailed explanation of the experimental procedure followed to carry out the work on this thesis. **Results and discussion**, fourth chapter, is going to show the results of the experiments and simulations carried out, as well as some debate concerning the importance of the work, the reasons behind the data obtained and further meaning for future development. In the **conclusion**, a brief sum up of the results obtained and its contribution to the issues stated. Further, in the **assessment of the work done**, will be built a retrospective analysis of the author, in which will be analyzed the assessment of the objectives proposed, as well as other contributions that this work may have.

2 Context and State of the art

Perovskite solar cells work basically through a n-i-p junction, where “n” stands for an electron acceptor, “i” is the semiconductor, and “p” is a hole accepting material. In PSCs, the semiconductor is a perovskite class of compounds and when absorbing light matching the respective band gap, it will lift an electron from the valence band to the conduction band, creating an electron-hole pair. In order to create electrical current as desired in a photovoltaic device, the hole and the electron should be properly separated and driven to opposite sides of the cell. The electrons must then travel to the n-type material (ETL – electron transport layer) and the holes to the p-type (HTL – hole transport layer). Each charge will then be collected by the respective electrical contacts. Electrons flow through the external circuit, performing electrical work and at the interface of the HTL with its contact, they recombine with holes, closing the circuit and regenerating the system [20]. The band gap of each component of the cell must be energetically aligned in order to obtain an efficient charge extraction, *i.e.* the valence band edge of the HTL should be higher than that of perovskite, and the ETL conduction band edge should be lower [20] - Figure 2.1 a).

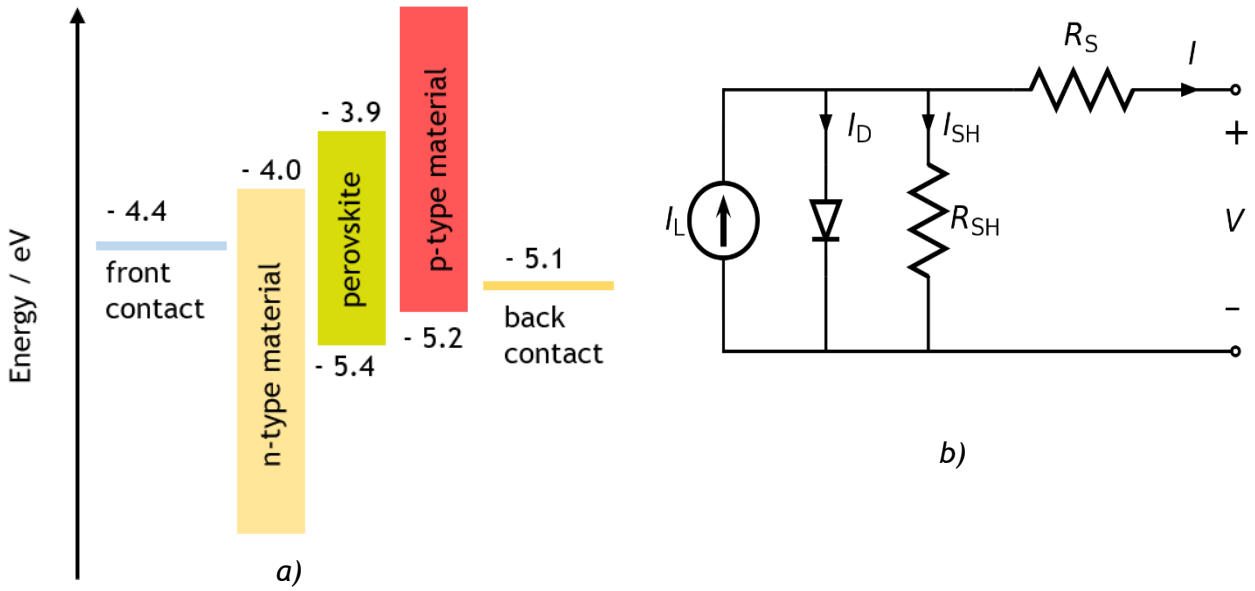

Figure 2.1 - a) Energy diagram of a PSC; b) Electrical circuit of a photovoltaic cell.

Figure 2.1 b) shows a generic representation of the electrical circuit of a photovoltaic cell. I_L is the photogenerated current, I_D the diode current, I the output current and V is the voltage across both terminals. The index “SH” stands for shunt and R_S is the series resistance. The shunt resistance is the resistance for electrons to recombine with holes, so it must be high. The series resistance is the resistance for the charges to travel to the external circuit, so it should be the lowest possible, to achieve a good performance.

When evaluating the PV cell performance, some parameters must be taken into consideration. Power conversion efficiency, η, is the percentage of electrical power produced from that which reaches the cell. This PCE can either regard to active area or aperture area. Active area is the working area of the cell, while the aperture area is the total area, considering both active and dead area (due to interconnections, shading, etc.). The open circuit voltage, V_{OC}, is the output voltage of the cell when the photocurrent generated is null. The short circuit current, I_{SC}, is the current obtained when the voltage applied is null. J_{SC} has the same meaning but refers to current density. Fill factor, *FF*, is the quotient between the maximum power point and the product of the V_{OC} and I_{SC}.

The most common used PSC architectures are: mesoporous, planar, HTL-less and inverted. The mesoporous structure is composed into 6 layers, not including the glass substrate: front-contact, electron blocking layer (EBL), mesoporous layer, perovskite, HTL, and back-contact. The EBL is an electron selective layer responsible for preventing electrons in the TCO (transparent conductive oxide) to recombine with holes. The mesoporous layer can be either conducting or insulating, acting as a scaffold for the perovskite, providing greater contact area for the perovskite adhesion. In case it is a conducting material, it also helps conducting the photo injected electrons onto the EBL. Planar structure is identical, but it does not use mesoporous layers. So, the electrons have to travel directly from the perovskite to the EBL, which can be less efficient, but the fabrication is certainly simpler and cheaper. HTL-less structure, as the name tells, is when a cell is built without the specific p-type layer, so that the perovskite itself works as p-type material as well. Again, this structure presents benefits in terms of processing and cost, but harms the cell performance. Inverted architecture places the HTL near the front-contact and the ETL on the opposite, next to the back-contact. This structure still lacks in performance when comparing to other configurations but presents great advantages in terms of long-term stability and ease of fabrication [20, 21]. Figure 2.2 provides a schematic drawing of a mesoporous architecture.

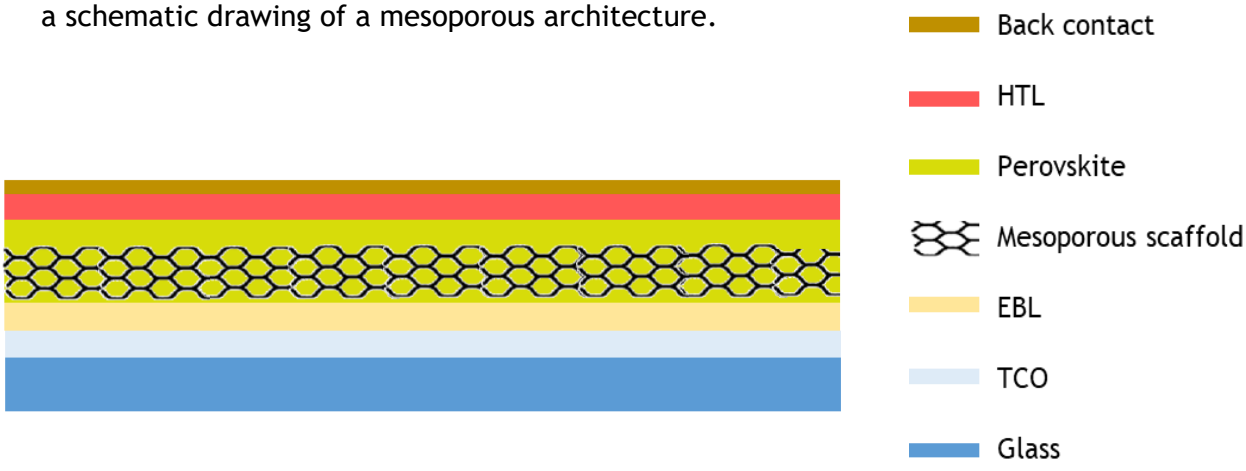

Figure 2.2 – Mesoporous architecture of perovskite solar cells.

Recalling the ABX_3 structure, the most commonly used A cations in PSCs are methylammonium (MA), formamidinium (FA) and cesium (Cs) or a mixture of them. B cation is usually lead (Pb^{2+}), but can eventually be replaced by another species with equivalent charge, for example tin (Sn^{2+}). X anion in PV applications is usually a halogen, such as bromide (Br^-), iodide (I^-) or chlorine (Cl^-) or a mixture [22]. For example, with no particular meaning, a perovskite material can be $MA_{0.4}FA_{0.4}Cs_{0.2}Pb(I_{0.5}Br_{0.5})_3$. This possibility constitutes itself as a great advantage in terms of materials synthesis, providing a wide band of different perovskites with tunable properties.

The front-contact is a TCO deposited in a glass substrate, allowing most of the light to pass but also able to conduct electricity. The most commonly used are indium-doped tin oxide (ITO) and fluorine-doped tin oxide (FTO), although some authors also used aluminum-doped zinc oxide (AZO) [23]. The back-contact is usually made of a noble metal like Au or Ag, quite expensive and so cheaper alternatives such as Ni or Al are being studied, as well as carbon materials [24]. When it comes to the EBL, a very thin and compact TiO_2 is the most common material, although some studies also used other compact materials such as SnO_2, ZnO or phenyl-C61-butyric-acid-methyl ester, known as PCBM [25]. For the mesoporous layer, TiO_2, SnO_2 or ZnO may also be used, but assembled as a scaffold for the perovskite solution to fill its pores [25]. When it comes to insulating mesoporous layer, Al_2O_3 and ZrO_2 are the most frequent used materials [20]. The HTL is usually made of 2,2′,7,7′-tetrakis(N,N-di-p-methoxyphenylamine) 9,9′-spirobifluorene, commercially known as spiro-OMeTAD. This material enabled the record PSC efficiencies, but it is expensive and unstable, and therefore researchers have been dedicated to test other materials as potential candidates, from which can be highlighted PEDOT:PSS (poly(3,4-ethylenedioxythiophene) polystyrene sulfonate, especially used in inverted architecture), P3HT (poly(3-hexylthiophene-2,5-diyl)), X-60 and PTAA (poly(triarylamine)). Besides these, hybrid HTL containing carbon materials may also provide be an alternative, as they present enhanced conductivity at lower cost [20, 26].

As mentioned before, stability is one important factor for feasible commercialization of a photovoltaic technology. Unfortunately, stability is one of the major drawbacks of PSCs, even if several works have been conducted in order to overtake this obstacle. The major degradation factors in a PSC are [20, 27]:

- Moisture: water makes perovskite to hydrolyze back to its precursors. The excess of water may cause irreversible damage, obliging to prepare PSC devices under controlled humidity. The HTL spiro-OMeTAD is also strongly hydrophilic, degrading from moisture and allowing it to pass to the perovskite layer;
- UV light: ultra violet radiation is absorbed at the TiO_2 mesoporous layer, and through a complex mechanism involving oxygen presence, free spots are created for the photo

injected electrons to allocate, creating a pathway for them to recombine with holes, leading the cell to lose current;

- High temperature: the permanently incoming solar light will increase the device temperature, which can be harmful for perovskite since it degrades with long exposition to high temperatures and has low thermal conductivity. High temperatures also affect spiro-OMeTAD, inducing crystallization, which harms the charge transportation;
- Intrinsic: interfacial degradation and corrosion, particularly with iodide and Au diffusion into the adjacent layers;
- Oxygen: oxygen is easily adsorbed in the perovskite structure, diffusing through its vacancies, allocating near the valence band. When light hits the PSC, a photogenerated electron may be trapped by the oxygen molecule, a O_2^- superoxide is formed, which is going to react with the perovskite cations, causing it to degrade.

Another important feature for all photovoltaic technologies is its environmental friendliness. Unfortunately, most perovskite materials contain Pb, a toxic element, that brings many dangers to the environment [28]. So far, tin has been the most trialed material for replacing lead, but germanium and bismuth are also among the candidates. However, none of these materials has yet been able to provide the same results as Pb based PSCs [29]. Nevertheless, lead amount in a PSC device is lower than 1 %, which is really low when compared to other commercialized technologies such as lead-acid batteries, widely used in automobile vehicles. Assuming a PSC with a maximum perovskite layer thickness of 400 nm, it should contain roughly 0.4 g of lead per square meter; this is equivalent to one-fiftieth of lead solder used in commercial silicon modules [30]. The calculated amount of added lead to the environment in case of catastrophic module failure should take into account: i) the full degradation of its perovskite absorber material when exposed to ambient, followed by ii) the dissolution of the decomposition products in water. For both cases, the added amount of lead to the ambient is very small compared to the natural occurrence of lead in soils; 1 m^2 PSC module has the equivalent amount of lead to 1 cm-thick natural soil with the same area [31]. Other studies have also shown that the direct impact of lead leaking from damaged panels will be much less when compared to other anthropogenic lead sources such as coal-burning power stations.

These environmental and stability issues may be minimized if an adequate PV device encapsulation is used. A good encapsulation will allow not only to protect the inner-components to degrade by inclusion of water and oxygen from the exterior, but also protecting the environment from potential hazards caused by leakage of PSC materials. Most works on PSC encapsulation have focused in using suitable polymers that do not need high temperature processing, because this is known to degrade the PSC performance. A detailed review on some

of the encapsulation works developed so far can be found on the work of Uddin *et al.*, published in 2019 [32].

Finally, another major step for commercialization of PSC is the upscaling. In conventional chemical engineering, this term usually refers to a process, in which a team or enterprise dedicates to develop a scientifically proven method (reaction, separation process, etc.) into a large-scale operation, rentable and steady. In other words, it is shifting from a goblet to a reactor, from grams a day to tonnes a day, from a laboratory to a big industrial plant. The same goes for devices. PV panels commercialization is only possible through the assembling of devices with few dead areas, low series resistance in interconnections, stable and long lasting energy production, be independent of maintenance as long as possible, easy link to the electrical network, whether being a PV park sourcing high-tension cables or a single panel supplying a house, and be safe, robust and protected against surrounding environment, without harming the electrical performance.

In crystalline silicon technology, the cells are built in wafer style, posteriorly interconnected with bus bars. But within thin film technologies, many sub-cells are assembled in a sub-module, and sub-modules are then connected to form a full panel [33].

The first recorded solid state perovskite module was fabricated in 2014 by Matteocci *et al*. [34]. They reached a maximum 5.10 % PCE for a 5 sub-cell series interconnected module with a FTO/b-TiO_2/m-TiO_2/$CH_3NH_3PbI_{3-x}Cl_x$/P3HT/Au configuration (b- and m- stand for blocking layer and mesoporous, respectively), with a *FF* of 0.526 and an active area of 16.8 cm^2. Great upgrades were made in only one year, since in 2015 a module with a 12.9 % PCE (for a 40 cm^2 active area) was fabricated by Heo *et al*. [35]. This module had 10 sub-cells series interconnected in an inverted architecture, using the materials ITO/PEDOT:PSS/$MAPbI_3$/ PCBM/Au. Then in 2017 a great improvement was achieved with Microquanta producing a 6 sub-cell series interconnected module with 16.0 % PCE corresponding to 16.29 cm^2 of aperture area [36]. The current record belongs to the french Commissariat à l'énergie atomique et aux énergies alternatives, that earlier this year has claimed to fabricate a module with 20.3 % PCE for a 11.2 cm^2 active area, on a 8 series connected sub-cell device [37].

The chart in Appendix 1 shows the evolution of certified module efficiencies, with respect to aperture area.

Even if some advances have been made in terms of PSC modules construction, there are two main aspects contributing for efficiency loss when going from small devices (< 0.1 cm^2) to large cells (~ 1 cm^2) and to modules (> 10 cm^2): emergence of defects on the materials deposition over big areas and the impact of series resistance in the substrate conduction ability. Now, will be reviewed each of them in more detail, and provided a lookout on the most frequent module configurations.

2.1 Scalable deposition methods[1]

The deposition method plays a big role in the performance of PSC modules. The active layers should be compact, uniform and robust, and its processing should allow to easily obtain the desired thickness. In general, except for perovskite, the other active layers can be easily deposited by spray techniques, screen printing or thermal evaporation [38]. A well working PSC should have a pin-hole free and smooth surface film, with large grain-size with few defects, and therefore a slow crystal-growth process should be provoked [39]. A list of some of the most used deposition methods will be presented next.

Spin-coating. On laboratory scale, this is the most used and successful deposition method [40]. It works by dropping a few droplets of solution on the substrate that is vacuum stick to a chuck. The chuck will then rotate, and the fluid will be driven radially outwards due to centrifugal force. The viscous forces and surface tension trigger the flat deposition on the surface, and after the evaporation of the solvent, a film is formed. This evaporation step depends on the specifics of each process. The angular speed, density of the volatile liquid, solution viscosity and rate of the evaporation determine the film thickness [41]. A two-step deposition may be applied, where each of the precursors is sequentially spin-coated [4]. This method has the advantage of the great know-how acquired in small scale, but it is hard to guarantee a uniform deposition in large areas and may lead to solution waste. An example of a module built with this technique is the work developed by Han *et al*. that fabricated a 11 series connected sub-cell module achieving 13.8 % for a 25 cm^2 aperture area, having deposited ETL, perovskite and HTL via spin-coating [42].

Blade-coating. This method works by continuously supplying ink onto the substrate, and a blade over the rolling substrate forms a meniscus, as shown in Figure 2.1.1 a). The gap between the blade and the substrate will determine the amount of fluid that is deposited in the substrate, with the roll speed and ink properties also influencing the formed film thickness [43]. This method is applied in roll-to-roll (R2R) processes, and grants better reproducibility and control over the film in large areas when compared to spin-coating [4]. Deng *et al*. fabricated a 60 cm^2 aperture area module using N_2 knife assisted blade coating for HTL and perovskite layers deposition, obtaining 16.4 % PCE [44].

Slot-die coating. In this method, the ink is deposited onto the substrate through a head, which is formed by two blades separated by a shim, creating the space for the ink to flow from the head to the substrate, with the desired pattern and gap, illustrated in Figure 2.1.1 b). This gap

[1] Adapted from [17] C. Teixeira, D. Castro, L. Andrade, A. Mendes, *Selection of the ultimate perovskite solar device for feasible commercialization: A review*, to be submitted to Renewable and Sustainable Energy Reviews, (2020)., under submission.

width, the gap between the head and the substrate, along the ink viscosity and deposition speed determine the layer thickness. This method is versatile, being possible to achieve many thicknesses and process different solutions, with high uniformity [45]. Using slot-die coating, Giacomo *et al*. fabricated a 13.8 % PCE module corresponding to a 144 cm^2 aperture area [46].

Printing methods. In these methods, the ink is continuously supplied to the substrate through nozzles (inkjet printing – Figure 2.1.1 c)) or a screen mesh (screen printing – Figure 2.1.1 d)). This technique is cheap and may be easily adapted to flexible substrates; though, it may have complex operation optimization and, specially, in inkjet printing, there is the risk of the ink particles dissolve the ones already on the substrate [47]. A promising result has been obtained by Panasonic, that fabricated a 16.09 % PCE module corresponding to a 802 cm^2 aperture area, using inkjet printing [48].

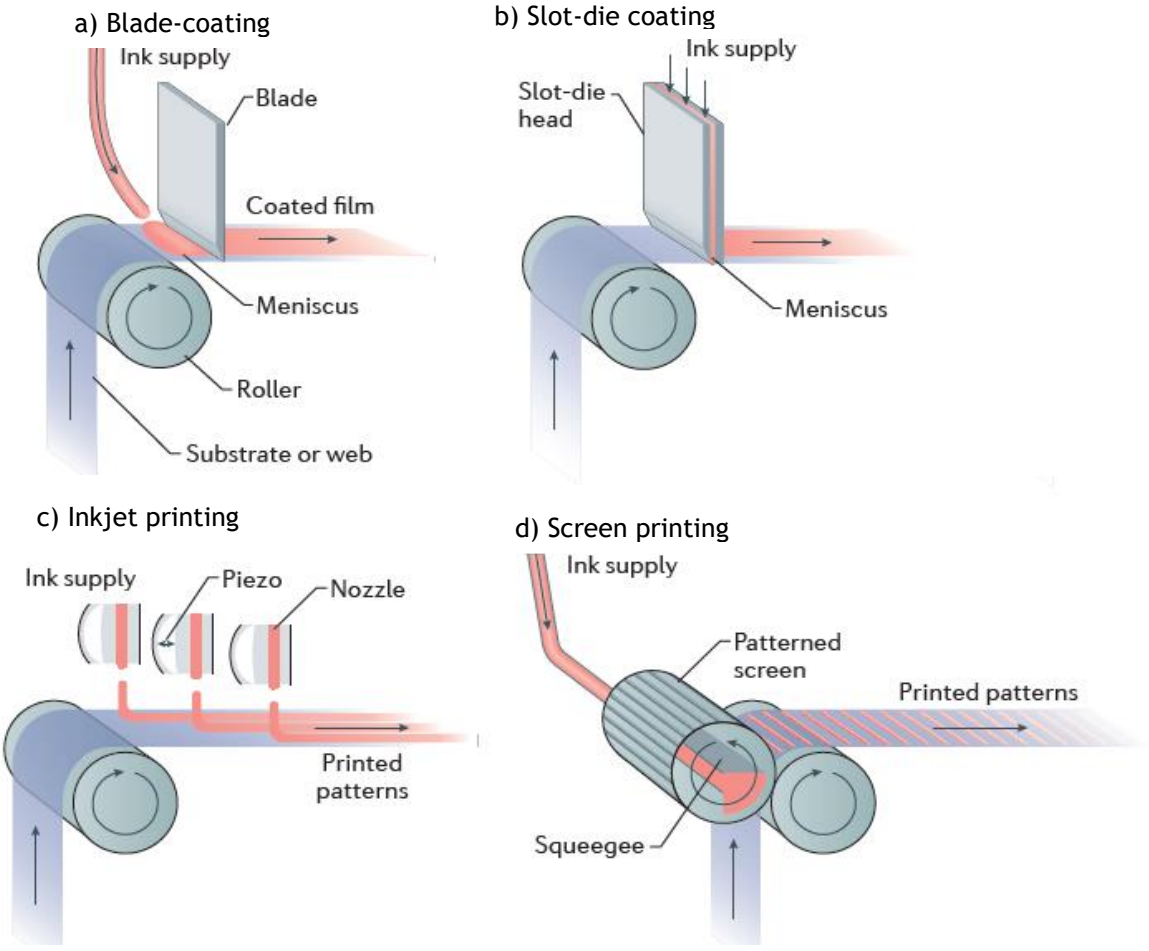

Figure 2.1.1 – Scalable deposition methods: a) blade-coating, b) slot-die coating, c) inkjet printing and d) screen printing (adapted from [4]).

Some other methods may be also good alternatives, but they are not, to date, as explored as the already mentioned ones. **Spray coating** has shown promising results in assembling other active layers, but it still has not been fully tested in perovskite large area deposition and may require high temperature for working [4]. **Electrodeposition** is a solvent-free method (except

for the electrolytes used but these are not toxic nor expensive) that has also been tested for perovskite deposition but has not shown great results so far. Although it dispenses the use of vacuum or high temperature processing, it is a technique difficult to apply to flexible substrates [49]. Another technique frequently used for the deposition of the active layers other than the semiconductor layer is **vapor deposition**. This method is used in other PV technologies such as crystalline silicon, CIGS or CdTe, and therefore there is already an immense know-how. However, this technique requires high-vacuum operation conditions and so it is expensive [4].

2.2 Substrate resistance[2]

PSCs, as other PV technologies, deeply depend on the use of a TCO coated on a glass substrate. This is the first component of a PSC right after the glass, serving as the front-contact of the cell. A good performing TCO means maximum transparency and conductivity, minimizing optical losses by reflection and electrical losses through the series resistance [50].

The most used TCOs in perovskite devices are FTO and ITO. FTO works by doping tin oxide with fluorine atoms; the fluorine ions (F^-) replace some oxygen atoms within the oxide structure and occupy vacancies, and the charge difference creates "pathways" for the electrons to flow [51]. On the other hand, ITO is an alloy with ternary composition and is "naturally" conductive, although its properties change according to the relative content of each component: indium, tin, and oxygen [52]. Both materials have similar transmittance, with ITO usually delivering best electrical performance. However, indium is toxic, and FTO is cheaper to produce and more easily deposited in substrates [50]. Hence, there is not a clear best option for PSC application and the TCO choice depends on the desired characteristics.

The TCO is a major performance limiting factor because it is a semiconductor. Since it is not metallic, the maximum limit of charges that can travel at the same time in the TCO is more reduced than in a conductor, but all charges that leave/enter the cell have to travel through the TCO. J_{SC} is one of the parameters affected, because more series resistance will result in less speed in driving charges. With high series resistance, electrons with tend to prefer the shunt path, recombining with holes and reducing the power output of the cell. This phenomenon also traduces in a poor *FF* [53]. This TCO resistance is often called as sheet resistance and is classified in units of ohm per square ($\Omega \cdot sq^{-1}$).

Many strategies can be used to reduce the series resistance of the TCO substrate but they will still impact the final device performance. TCO thickness can be increased, resulting in higher conductivity, but it will reflect in a reduction of the light that reaches the perovskite, as reflection and absorption phenomena raise. Additional doping also enhances TCO electrical

[2] Adapted from [17] ibid. , under submission.

conductivity, but it also means lower transparency [23]. There is also the possibility of reducing individual sub-cell width so that the distance that charges have to travel in TCO would be smaller, but reducing sub-cell width also means having more interconnections between sub-cells in order to reach the same device dimension. The consequence is the increase of the dead area of the module due to interconnections, and in extreme cases of small width, difficulties in industrial processing [23]. So, for the ideal module building, there should be a careful optimization process of each of these variables.

In 2016, Galagan *et al*. [54] used the software COMSOL to study the role of the TCO in a PSC module performance. The results showed that soft changes in sheet resistance may translate in important aspects for the design of the module. For a TCO sheet resistance of 10 $\Omega \cdot sq^{-1}$, the data showed that the sub-cell width should be between 3 and 7 mm, but if the resistance was 60 $\Omega \cdot sq^{-1}$, the width should be lower than 3 mm. When using ITO, the team also found that high temperature processing of active layers damaged this TCO, increasing the series resistance, alerting to special precaution upon assembling the devices. This simulation work results were then corroborated by experimental data, confirming the predictions. Kaminski *et al*. [23], also using software tools, studied the TCO influence in a PSC module. The results showed an improvement in performance when using AZO, with increased front-contact thickness not harming the light reaching the absorber, also with benefits from using an anti-reflective coating and a reduced TiO_2 thickness in the EBL. In 2017, Shi *et al*. [55] optimized a sol-gel method for the production of FTO by adjusting the F/Sn molar ratios. A F/Sn molar ratio of 14 % delivered the best electrical performance for the FTO, corresponding to a surface resistance of 14.7 $\Omega \cdot cm^{-1}$ and 74.4 % of light transmittance. In another study in 2017, Koo *et al*. [51] fabricated FTO electrodes via ultrasonic spray pyrolysis, varying the $O_2/(O_2 + N_2)$ ratio on the carrier gas used during the process. The results showed that the optimal value was 50 %, which allowed a sheet resistance of only 4 $\Omega \cdot sq^{-1}$ and optical transmittance of 85 %, along with a faster substitution of the O atoms by F atoms in FTO structure, reducing the vacancy concentration. More recently, in 2019, Mouhamad and his team [53] built a PSC module with three mesoporous layers, HTL-free, and with a carbon back electrode to study the interference of the limiting conductivity of both electrodes (FTO and carbon) on the cell performance. They suggested that sub-cells should be no wider than 5 mm to achieve a *FF* of 0.70, and highlighted that, although still lacking in performance, this design costs are low when compared with other more frequent ones, and that this architecture also provided a gain in stability.

2.3 Module fabrication[3]

The challenges debated in sections **2.1** and **2.2** are the present main obstacles for module-level development of perovskite technologies. In the past few years, an increasing number of researchers are being dedicated to overcome these challenges and, indeed, be able to provide the best solution for future perovskite PV panel large-scale fabrication. There have been mainly two module configurations studied: monolithic and grid interconnected.

Monolithic interconnection. In this configuration, many sub-cells are connected in series, and hence the voltage is the sum of each individual voltage and the current is limited by the lowest current sub-cell. The sub-cells share a common substrate. The first step is the TCO deposition. Then, scribe lines, called P1, remove thin lines of the TCO, electrically insulating each sub-cell. Then, all the active layers are deposited, and the next scribe, called P2, removes the active layers just a bit further from the P1, so that the sub-cells are, again, separated. This scribe should stop just before reaching the TCO. The next step is the back-contact deposition. It will fill the gap created by P2, connecting the top of a sub-cell with the bottom of the next one, thus creating the electrons path. The final step is the P3, scribe lines that remove both back contact and active layers (or only the back contact) just a bit further from P2. These scribe lines can either be executed mechanically or by laser. The goal of this configuration is to connect many cells without having to use excessive conductive contacts [5]. Figure 2.3.1 helps to understand the design of a monolithic module.

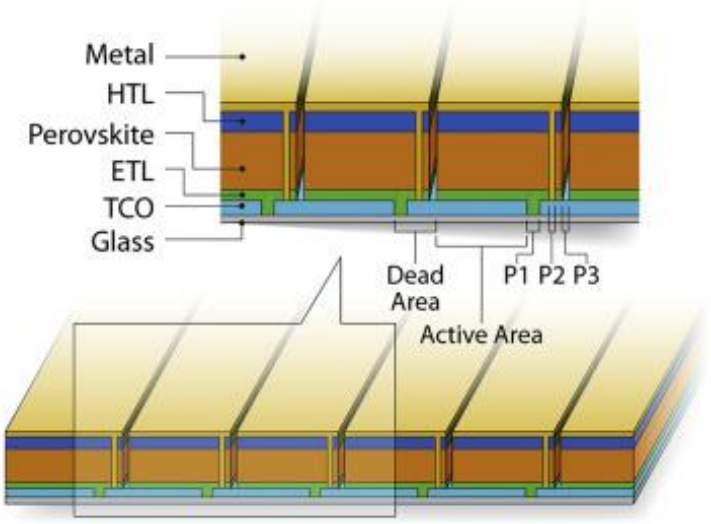

Figure 2.3.1 – Monolithic module (adapted from [5]).

[3] Adapted from [17] ibid., under submission.

Grid interconnection. With this configuration, the sub-cells within a module are now connected in parallel, so that the output voltage is limited by the lowest producing one. This arrangement works by building what basically is a large area singe cell, but the difference is that the TCO is impregnated with thin conducting lines, called fingers, that collect the current from the front contact. A sub-cell can be defined as the space between two consecutive grid lines, since all charges generated within those grid lines will travel to one of them (either electrons or holes, depending on the architecture). The fingers then drive the charges to bigger lines, called busbars, that finally drive the charges to the external circuit [5]. Each busbar usually collects charges from many modules, as can be seen in Figure 2.3.2.

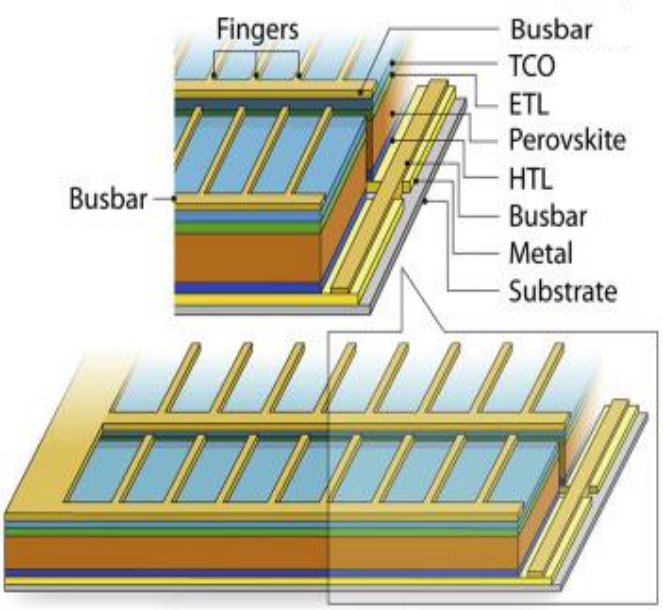

Figure 2.3.2 – Grid module (adapted from [5]).

Both configurations aim to reduce the path that the charges travel within the TCO, as that is known to improve the performance by reducing series resistance. So, an important parameter to analyze in a module is the geometric fill factor, *GFF*, which is the fraction of active area divided by the total aperture area. A *GFF* close to 95 % is achievable in both configurations, but it may be easier to reach this in the grid configuration, with careful grid design. In monolithic modules, since there are multiple interconnections, a more careful work is needed to minimize dead and interconnection area losses [56]. These interconnections should be narrow and as close as possible to minimize these losses. However, an over narrow P2 will imply greater series interface resistance, since charges must travel to the back contact of a sub-cell to the TCO of the following one, in the pathway created by P2. This clearly is a matter of optimization to obtain the maximum performance of the cell. P1 and P3 are less sensitive scribes, since they only have to be narrow enough to isolate the sub-cells front and back-contacts, respectively [38]. The back contact filling the P2 scribe will be in touch with the active layers, which may be an additional degradation mechanism, but this also happens with grid modules, since the fingers impregnated in the TCO may also harm the active layers [57]. The main drawback of grid module is the high costs of all the contact material used, along with the challenges of depositing the respective fingers and to coat the active layers on it. Also, additional shading can be generated [5]. One final comparative observation is that in a monolithic module, if one of the cells stop working, current will not pass, so the whole module stops working, while on a

grid device, a local failure does not imply on other sub-cells. Overall, due to the reasons mentioned, monolithic configuration has suffered deeper progress in the last years.

In 2017, Palma *et al*. [58] fabricated the first as-claimed fully laser-processed PSC module, with a thorough optimization of all scribes. They obtained a 9.3 % PCE with respect to a 14.5 cm^2 aperture area, and an incredible *GFF* of 95 %. Chen *et al*. [59] tested a method based on a solid film applying pneumatic driven pressure to distribute the perovskite uniformly through all the substrate, having achieved large grain size with few defects. The champion device has 15.8 % PCE, corresponding to a 10 sub-cells monolithic module with 17.6 cm^2 aperture area. Later in 2018, Higuchi and his team [60] dedicated to minimizing the heat damage on FTO provoked by laser scribing, having used mechanical etching. They came across evidence of TiO_2 residues in the P2 gap, that increased the interconnection series resistance. To overcome this, the team used THG-YAG (third harmonic generation - yttrium aluminum garnet) laser treatment to remove the residues, having obtained a 34 % PCE improvement when compared to those modules without this laser treatment. Fill factor also increased from 0.546 to 0.692. Yang *et al*. [61] also worked on the TiO_2 residues interference, but the solution applied was a reduction in the ETL layer thickness to only 10 nm, fabricating a 10.36 cm^2 area four sub-cell monolithic module with 15.6 % PCE and 87.3 % *GFF*. Regarding degradation due to iodide diffusion, Bi *et al*. [57] developed a work where multiple diffusion barriers are studied and incorporated into the module building. This required an extra scribe, an additional step to shape the diffusion barrier into the module design. However, the devices showed improved PCE when applying the diffusion barrier, achieving 15.6 % PCE. In terms of stability, the modules retained 95 % of their initial PCE after 1 000 h under heating (in the dark), and 91 % after 1 000 h under AM 1.5 G simulated solar light. Earlier this year, Schultz *et al*. [62] investigated if changing from nano to picosecond pulse duration presented improvements in the modules, and the results showed that the use of picosecond laser not only exhibited better electrical performance, but resulted in better morphology of the scribe walls, elimination of PbI_2 in the scribe path and largely reduced damage in the TCO when compared to the use of nanosecond laser. Wang *et al*. [63] developed a similar work and confirmed the benefits in using picosecond pulse laser.

In what concerns grid interconnected modules, there are also some progresses. In august 2017, Kim *et al*. [64] fabricated a grid module with 16 cm^2 (unspecified if its active or aperture area), with a corresponding 12.1 % PCE. The authors performed a careful optimization of the grid lines design to maximize the performance, and achieved a *FF* of 0.619. With a different approach, Wilkinson and his team [65] developed a thorough simulation study on grid modules. The results showed that the material used as TCO (whether FTO or ITO) in a grid module does not significantly affect its performance. Also, a potential PCE of 21 % was recorded for a 200 cm^2 active area device, with an optimized metal grid display. The same PCE was registered as

achievable for a hybrid monolithic-grid module, with the possibility to have 2 mm for each interconnection.

A throughout overview of the most relevant works in the module fabrication field was performed in the first month of this master thesis to be included in a review paper entitled "Selection of the ultimate perovskite solar device for feasible commercialization: A review" and submitted to the journal *Renewable and Sustainable Energy Reviews*.

3 Materials and Methods

This work is divided in two different parts due to the laboratory closure, following covid-19 safety measures. So, the first five weeks were dedicated to laboratory development of cells towards module fabrication, and then the following time to simulation for module design optimization.

3.1 PSC fabrication: experimental procedure

For the experimental part of this thesis, the general methodology used followed the previous developments in host lab. So, the devices were prepared as described elsewhere [66]. Then, after being familiarized with the procedure for small area devices, the size of the cells was subsequently increased. The assembling of cells with a "strip" design and dimensions of 3 cm x 1.9 cm (0.8 cm width for active area) was optimized. For that, 2.2 mm glass substrate coated with FTO with a 7 $\Omega \cdot sq^{-1}$ sheet resistance (TEC7, Solaronix) were used. The FTO glass substrates were laser scribed (VersaLaser, VLS 2.30, Universal Laser Systems, USA), on the conductive side, 4 millimeters away from the edge. Then, the samples were washed using a Hellmanex solution (HellmaGmbH, Germany), and sonicated in ethanolic KOH and then distillate water, 5 min in each. The next step was the EBL deposition. After being plasma-treated for 10 mins, the FTO substrates were placed in a heating plate (inside a hotte), with thin glass strips covering the opposite side from scribing, which was going to be the photo electrode. While the plate heated to 450 ºC, the spray solution for the deposition was prepared, containing 7 mL of anhydrous isopropanol 99.8 % (AcroSeal Acros), 0.4 mL of acetylacetone (<< 99 %, Sigma), and 0.6 mL of titanium diisopropoxide bis(acetylacetone) 75 wt.% (Sigma-Aldrich). The reagents were mixed in this order, inside the glove box: isopropanol was the solvent used and acetylacetone works as stabilizer. When the plate was ready, the solution was sprayed onto the substrates. Then, for 45 min, the substrates remained in the plate with the hotte exhaustion turned off, and after that period the exhaustion was turned on, the substrates were covered with aluminum foil and the temperature switched off. The next step was the TiO_2 mesoporous layer deposition. The solution used was 1 g of TiO_2 for 6 g of absolute ethanol and should be kept always under stirring. Before the deposition, the space where there was no EBL should be covered with tape. The deposition took place inside the glove box, where 80 μL of the solution were spin coated onto the substrate. After the deposition, the tape was removed and the substrates were placed in a heating plate at 100 ºC for *ca.* 10 min and then transferred to an oven for performing the complete annealing process at 500 ºC during 30 min. Then, followed the perovskite deposition. The perovskite used is $Cs_{0.05}(MA_{0.17}FA_{0.83})_{99.95}Pb(I_{0.83}Br_{0.17})_3$, a tri-cationic structure. The solution precursor is composed by PbI_2 (1.1 M - Sigma-Aldrich 99.999% trace metal basis), $PbBr_2$ (0.2 M -Sigma-Aldrich 99.999 % trace metal basis),

methylammonium bromide (MABr, 0.2 M - Dyesol) formamidinium iodide (FAI, 1.0 M - Dyesol). These solids were dissolved in 0.8 mL of dimethylformamide (Sigma-Aldrich,99.8 %) and 0.2 mL of dimethyl sulfoxide (DMSO, Sigma-Aldrich, 99.9 %). Then, 0.95 mL of this solution were pipetted and mixed with 0.05 mL of 1.5 M CsI solution (Sigma-Aldrich 99.999 % trace metal basis). The perovskite solution was also deposited by spin coating. For each cell, 60 μL of perovskite solution were deposited. 25 s after the program started, 150 μL of chlorobenzene (Sigma-Aldrich, 99.8 %), the anti-solvent, were poured onto the spinning substrate. After the deposition, each cell should be 40 min in a hot plate at 100 ºC. The deposition and sintering processes took place inside the glove box, such as the next step, the HTL deposition, also by spin coating. The solution was composed by 0.1020 g of spiro-OMeTAD (Chemborun, 99.7 % sublimed grade), dissolved in 1116 μL of chlorobenzene, 40 μL of 4-tert-butylpyridine (Sigma-Aldrich, 96 %), 23 μL of lithium bis(trifluoromethanesul fonyl)imide (LiTFSI) solution (520 mg of LiTFSI in 1 mL of acetonitrile) and 10 μL of FK209 (tris(2-(1H-pyrazol-1-yl)-4-tert-butylpyridine)cobalt(III)tri[bis(trifluoromethane)sulfonimide]) solution (40 μg in 100 μL of acetonitrile). For each cell, 50 μL of HTL solution were deposited. Then, the cells were removed from the glove box but should be protected from light and moisture as possible. The space that was under the tape during the mesoporous TiO_2 layer, would then be covered with perovskite and HTL. So, the next step was to manually remove the active layers on that part, with the use of a swab soaked with acetonitrile and a scalpel. The swap with acetonitrile was also used to clean the non-conducting side of the glass. Next, the back-contact was deposited by thermal evaporation. The equipment was a VaporStation 4, from Oxford Vacuum Science, U.K.. The target gold thickness was 60 nm, and for the first 4 nm the deposition rate was 0.1 $nm \cdot s^{-1}$ and the remaining time at a 1.25 $nm \cdot s^{-1}$ rate.

The next cell dimensions were 5 cm x 2 cm (1 cm width for active area). The procedure was the same as described above, but the volume of mesoporous for each cell was adjusted to 150 μL, as well as 60 μL of perovskite solution per cell and the volume of anti-solvent in the perovskite deposition was alternated. The cells fabricated may be seen in Figure 3.1.1.

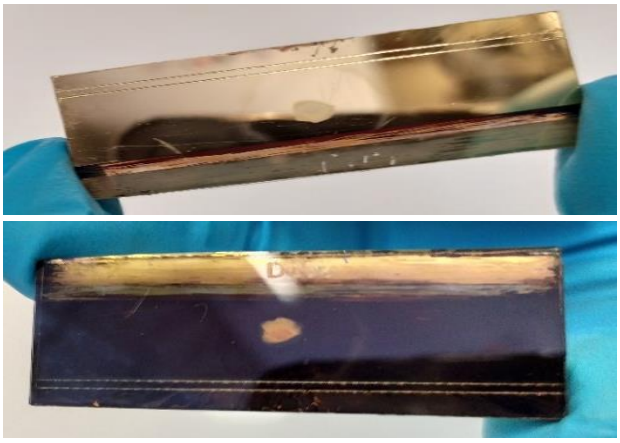

Figure 3.1.1 – 5 cm^2 active area cells.

Were the circumstances “normal”, the next step would be a two sub-cell series module assembly. Its fabrication methodology was also studied. Starting with the same substrate, coated with FTO, cut in the dimensions of 5 cm x 4 cm. The first step is the FTO scribing, breaking the substrate electrical conduction between the two sub cells and in the counter-electrode zone of the second sub cell. Then, the EBL is deposited, also with thin glass masks preventing from the deposition in the interconnection and the photoelectrode spots. The same goes with the mesoporous layer, but using scotch tape prior to deposition and removing it afterwards. The perovskite and HTL take place in all the substrate, but once again it should be removed with a scalpel and cleaned with acetonitrile in the zones where there is not EBL and mesoporous TiO_2. Next, is the gold deposition. A Kapton tape strip is placed in the boundary between the photoelectrode and the active layers in the first cell, so that only a line of gold is placed in the photoelectrode. Another strip is placed in the boundary between the interconnection and the active layers of the second sub-cell, so that the gold connects the top of the first sub-cell with the bottom FTO of the next one, but not making contact with its back electrode nor its active layers. Figure 3.1.2 helps to better understand the mechanism and the expected design.

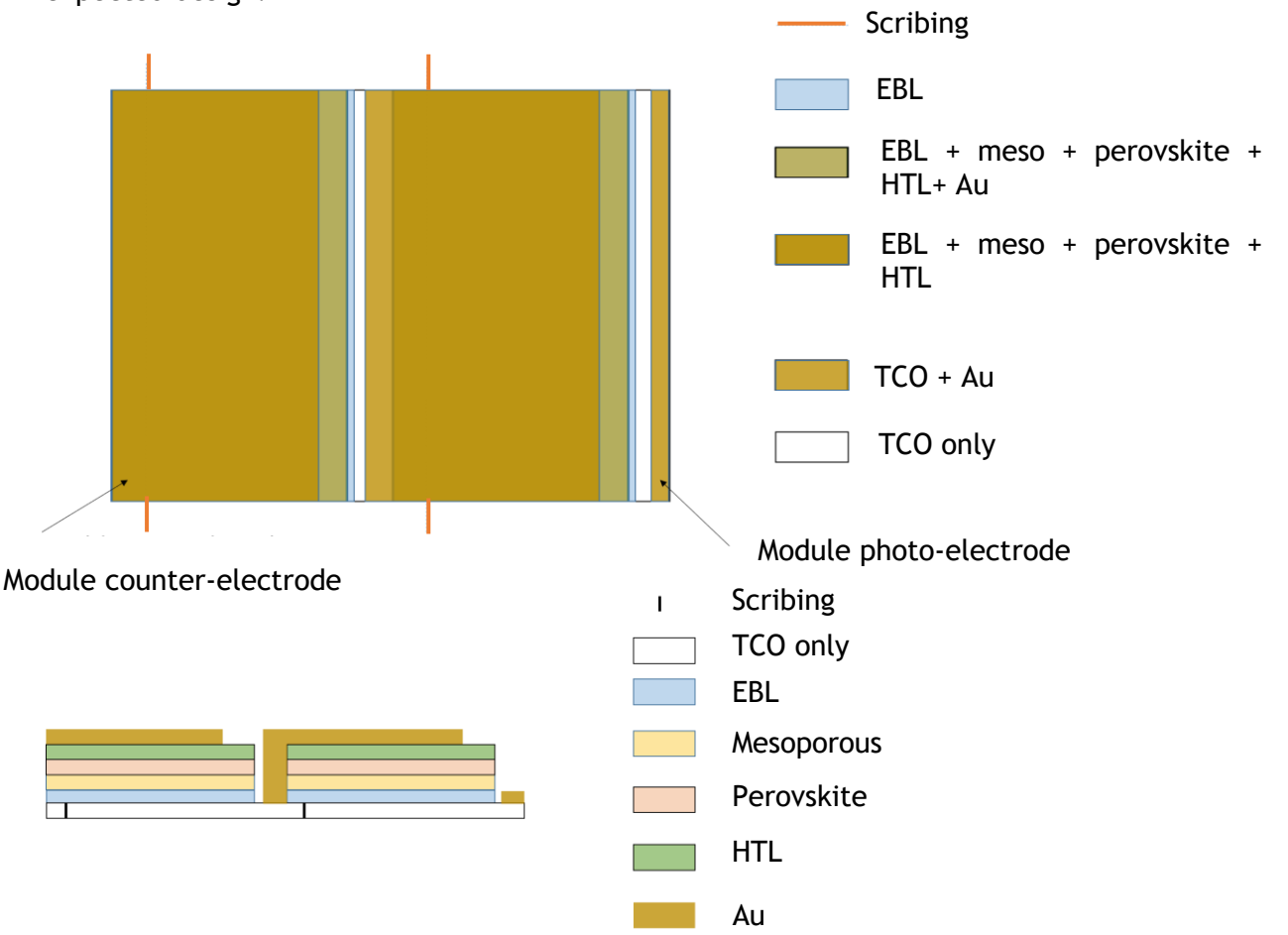

Figure 3.1.2 – Top and side view of the proposed module.

The devices were characterized approximately 24 hours after their preparation, at room temperature and ambient air. During night, the devices were kept in the dark and in desiccator to prevent degradation from moisture. The solar simulator was calibrated using a single crystal Si photodiode (Newport, USA). The current-voltage (*I-V*) curves were obtained by applying an external potential load and measuring the generated photocurrent using a Zennium (Zahner Elektrik, Germany) workstation, controlled by the Thales software package (Thales XT 5.1.4).

3.2 PSC electrical simulation

The software used for the simulations was LAOSS (which is inspired by for "large area organic semiconductor simulation"), developed by the swiss company FLUXiM AG. LAOSS was developed in 2015, and allows one to simulate electrical, thermal and optic properties of organic solar cells and LED's, using finite element method modelling. The software has a user-friendly interface, allows to use .dxf files (CAD drawings) and has also a set of geometries included [18].

The information input for each simulation will be described in the next chapter, specified individually for each of the simulations run. However, some of the inputs are always the same and will be referred here:

- Meshing tool is NetGen with 0.1 minimum and maximum edge size;
- No thermal coupling (this work is only about electrical properties);
- Convergence type is absolute residual with root mean square norm, with a 1×10^{-10} tolerance and 20 maximum iterations.

All the procedures generally follow the advice given in the software manual [67].

Following the objectives mentioned, the parameters studied within the software were devices dimensions (sub-cell width, interconnection gap), electrodes resistance and sub-cell number.

4 Results and discussion

4.1 PSC fabrication

The fabrication of PSC devices with active area of 2.4 cm^2 (3 cm x 0.8 cm) was optimized, after being familiarized with the preparation of small-size cells (~0.1 cm^2). A total of 26 cells was fabricated, and the following Figure 4.1.1 shows the *I-V* curve for the best performing cell.

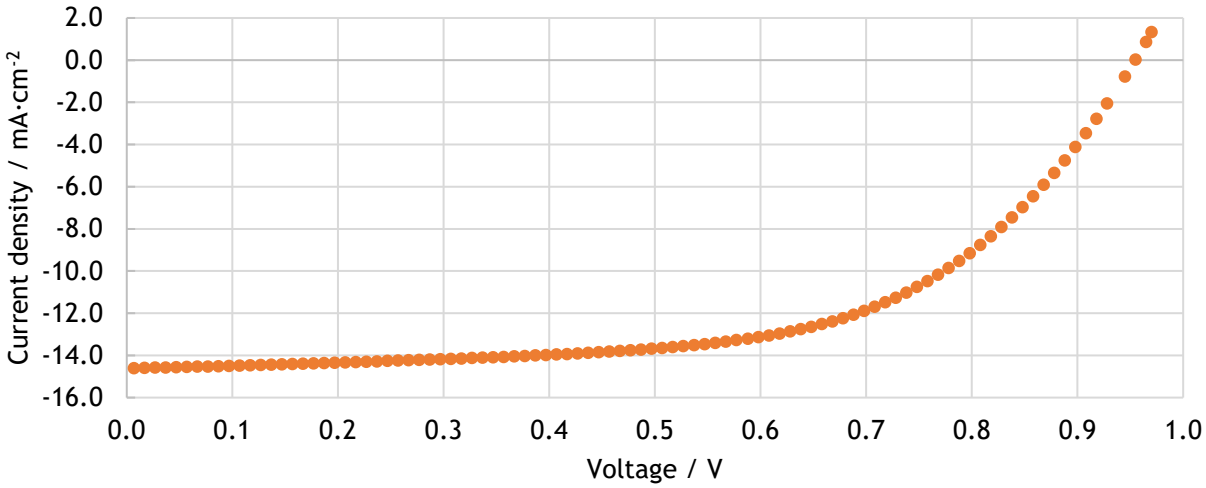

Figure 4.1.1 - Characteristic I-V curve of the 2.4 cm^2 active area best performing PSC (PCE = 8.30 %; FF = 0.598; Jsc = 14.61 $mA \cdot cm^{-2}$; V_{OC} = 0.955 V).

The next goal was to increase gradually the active area optimizing the deposition parameters. So, a total of 18 cells with 5 cm x 1 cm active area were prepared. Again, several batches of cells were prepared for optimization purposes. In this case, various anti-solvent volumes were tested, but it was verified that 150 μL were enough. What proved to be very important was to clean the interior of the spin-coater after each deposition, since due to great amounts of anti-solvent used, it would stick into the inner-walls, interfering with the annealing process. The Figure 4.1.2 shows the *I-V* curve of the best performing PSC device and Table 4.1.1 the average photovoltaic performance comparison between 2.4 and 5 cm^2 active area cells.

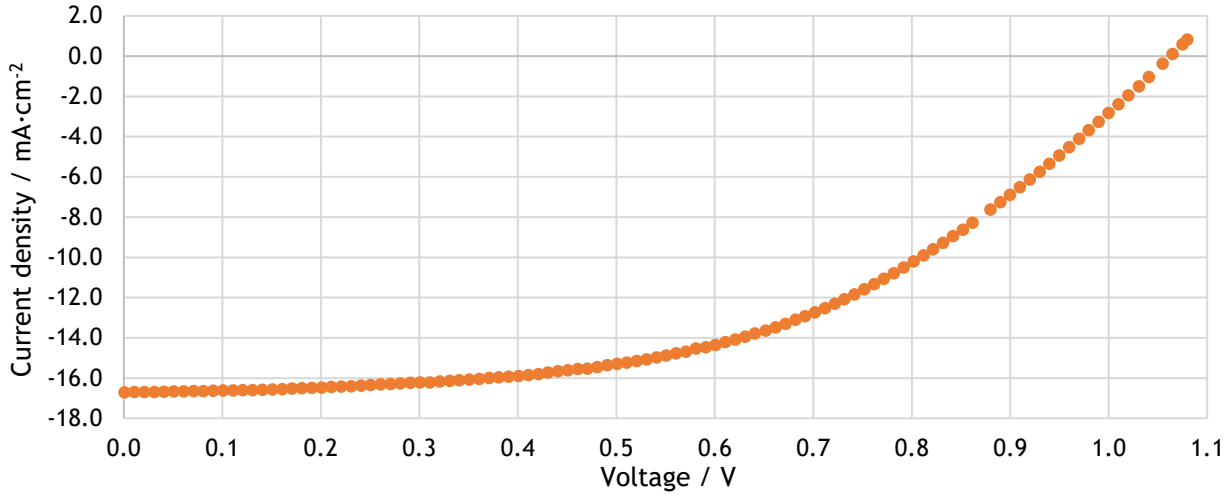

Figure 4.1.2 – Characteristic I-V curve of the 5 cm² active area best performing PSC (PCE = 8.95 %; FF = 0.505; Jsc = 16.72 mA·cm⁻², V_{OC} = 1.068 V).

Table 4.1.1 – Average photovoltaic parameters comparison of the 2.4 and 5 cm² active area cells.

Active area (cm²)	2.4	5.0
PCE (%)	5.95 ± 1.22	6.48 ± 1.50
V_{OC} (V)	0.845 ± 0.052	0.943 ± 0.088
J_{SC} (mA·cm⁻²)	12.08 ± 1.93	12.47 ± 2.51
Fill factor	0.511 ± 0.056	0.493 ± 0.048

Some improvement can be verified in the PCE and in the V_{OC} obtained, which largely depends on the layers used [68] and therefore is natural to increase with growing laboratorial procedures handling experience. Constant performance outputs were observed for 2.4 and 5 cm², demonstrating that the length of the cell, up to these values, does not provide an obstacle to PSC upscaling. This is also supported by the improvement verified for the J_{SC}, which is affected by series resistance in the substrate. Nevertheless, a slight decrease in the *FF* starts to appear, demonstrating the TCO influence.

However, the results obtained for these dimensions fall short to the best PCE previously obtained in this lab for cells with 0.2 cm², reported in [66], which is over 15 %. A loss of performance is inevitable when depositing the materials in larger scale and increasing the cell width, as previously stated in this thesis.

4.2 PSC electrical simulation

Before moving forward to single-cells interconnection into a PV module, the best cell geometry as well as electrical contacts optimization, for avoiding increased dead areas, should be assessed.

LAOSS software was used to predict the theoretical losses due to TCO resistance when upscaling the cell from the 0.2 cm^2 up to 5 cm^2. Then, interconnections geometry as well as scribing optimization were studied for the modules configuration.

The geometry input in the software was a simple rectangle with 5 cm length and 1 cm width, the same size of the mask used for PSC characterization. The software input needed to be provided is a correlation between the bottom and top electrodes, i.e. information about how efficiently charges are generated and transported to allow the PV effect. For this study, the correlation provided was the *I-V* curve file corresponding to a standard cell with 15.22 % PCE fabricated in the host laboratory (from now on, called reference curve) - Figure 4.2.1. The bottom and top electrodes sheet resistances also have to be provided, and 7 $\Omega \cdot sq^{-1}$ was selected for the top electrode, as it corresponds to the sheet resistance of the used FTO, and 0.407 $\Omega \cdot sq^{-1}$ for the bottom electrode, which corresponds to a layer of gold with 60 nm and 2.44×10^{-8} $\Omega \cdot m$ resistivity (value at 20 ºC [69]) – Figure 4.2.2. Both figures show the input information as displayed in LAOSS interface.

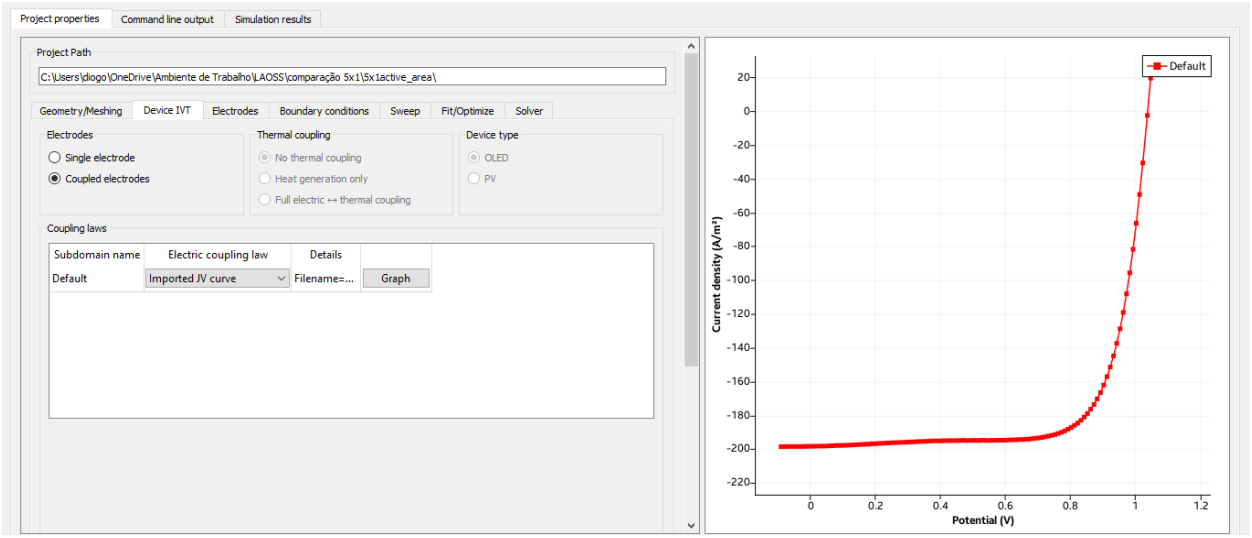

Figure 4.2.1 – Imported I-V reference curve.

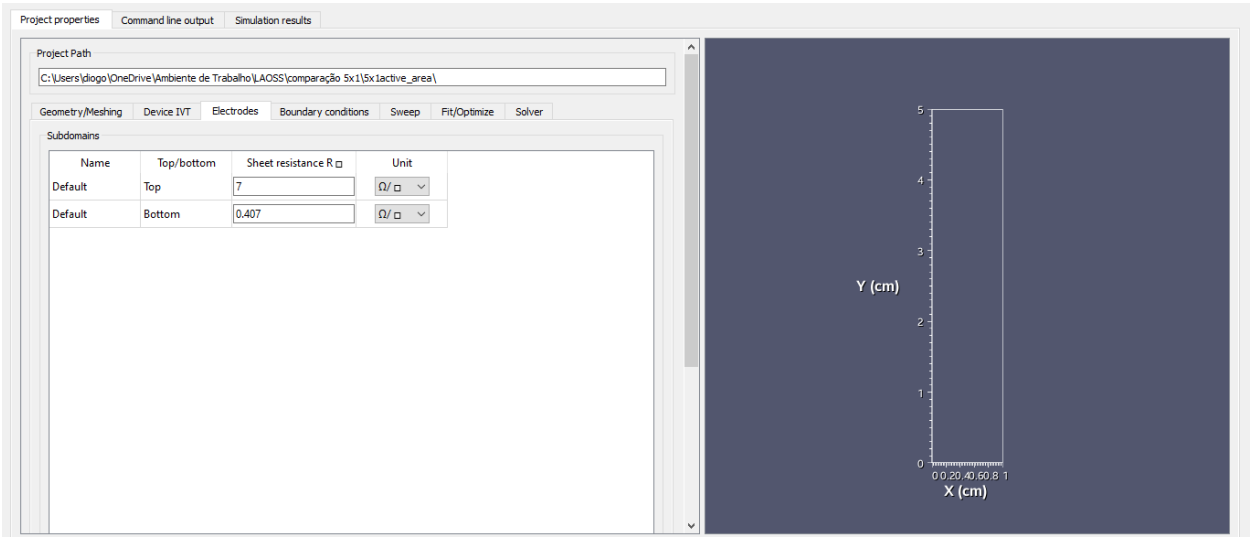

Figure 4.2.2 – Sheet resistance input.

The next step is the establishment of the boundary conditions. In this case, the voltages in both electrical contacts are set to 0. Then, the sweep parameters are defined. A sweep ranging from 0 to 1.06 V was performed (the V_{OC} of the reference cell), with a step of 0.01 V. The simulation was run in approximately 72 s – Figure 4.2.3 – and the correspondent photovoltaic parameters are compared in table 4.2.1.

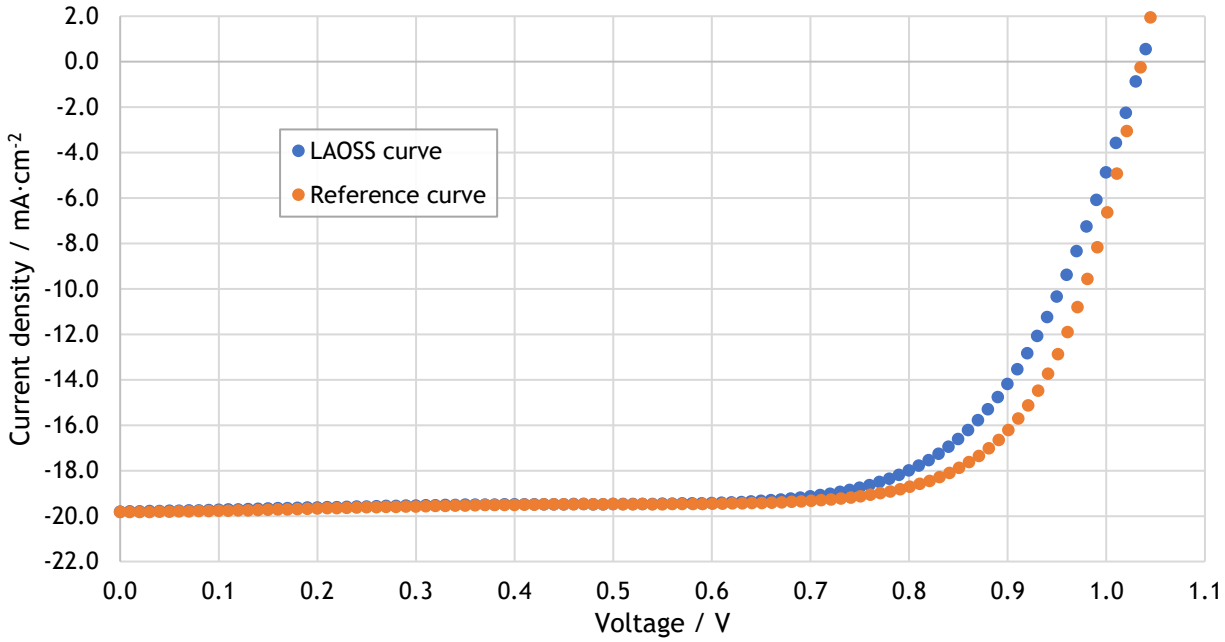

Figure 4.2.3 – Comparison between LAOSS and reference curve.

Table 4.2.1 – Comparison between LAOSS and reference cell photovoltaic parameters.

	Reference	LAOSS
PCE (%)	15.22	14.40
V_{OC} (V)	1.036	1.036
J_{SC} (mA·cm^{-2})	19.83	19.81
Fill factor	0.738	0.702

The input *I-V* curve is the coupling law between top and bottom electrode, which the software considers to be constant over all the device area. Therefore, the slight differences in performance of both cells, verified in Figure 4.2.3 and Table 4.2.1, are only due to the TCO, and prove that these dimensions of the cell almost do not provide limitations to the electrical power output.

Then, the laboratorial *I-V* curve of the best PCE device with 5 cm^2 was compared with the simulated 5 cm^2 *I-V* curve – Figure 4.2.4.

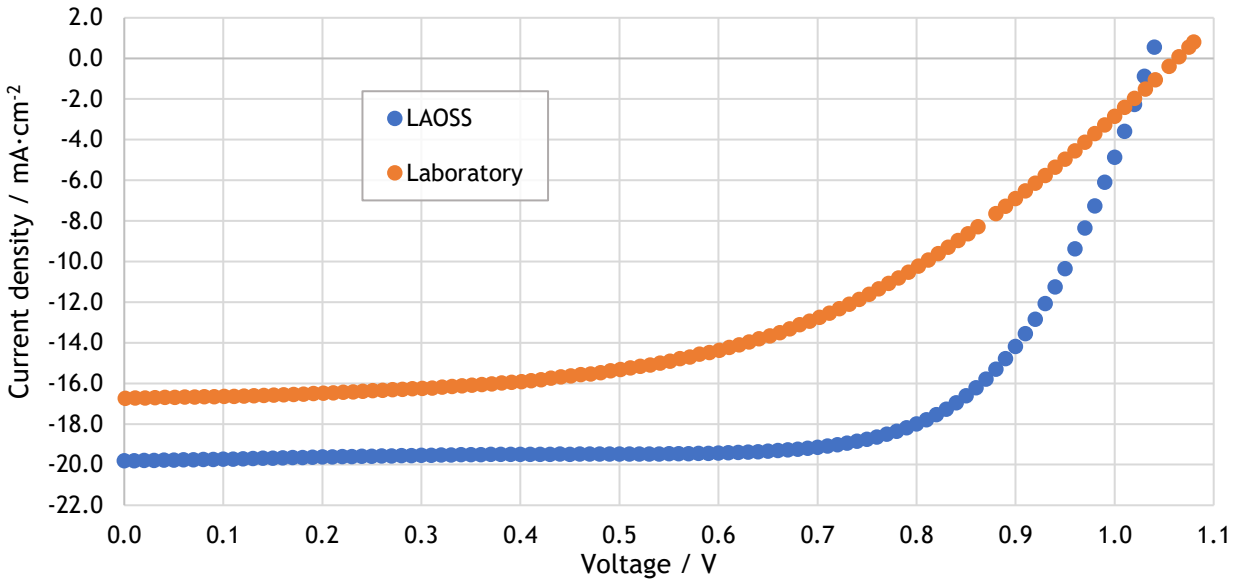

Figure 4.2.4 – Comparison between LAOSS and laboratory 5 cm^2 active area cells.

The corresponding photovoltaic parameters of the laboratory cell are:

- 8.95 % PCE;
- 0.505 fill factor;
- 1.065 V open-circuit voltage;
- J_{SC} of 16.73 mA·cm^{-2}.

In this case, there is a large difference between the two curves, only narrowed in the voltage limit zone. Actually, laboratory produced 5 cm^2 cell has a higher V_{OC} than the reference one, but the difference is small and it is within experimental error. However, the remaining parameters such as the PCE, short-circuit current density and fill factor all register big downgrades. This may be explained by several different reasons. First, as stated before, LAOSS only takes into account the electrode resistance losses, whereas in a real scenario all factors will influence the cell performance, as uneven deposition in large area (further laboratorial deposition optimization is needed), existence of pinholes or interfacial defects occurring during the cell fabrication. Besides that, the simulation in LAOSS only contemplates active area but, as described in section 3.1, additional space for the photo and counter electrodes connection to external circuit is fabricated in the laboratory. One of the major differences is in *FF*, which goes from 0.702 in the simulation to 0.505 in the best performing cell. A loss in *FF* is natural when up-scaling, due to substrate resistance and it is also largely correlated to the quality of the perovskite layer and the recombination pathways, so it is natural that laboratorial deposition will lead to poorer *FF*, especially when it comes to the absorber layer [53]. This conclusion also draws attention to the importance of establishing a large-scale deposition method that allows to create thin, uniform and crystalline perovskite layer.

Therefore, the 5 cm^2 laboratorial *I-V* curve corresponding to the 8.95 % will be used for the upcoming simulations, since it represents the real performance obtained when upscaling in laboratory environment, and it is affected by the defects in large-scale deposition. Further optimization in the host laboratory could improve this result but, still, it would never reach the 15 % corresponding to a small scale cell. For that reason, using the 15 % PCE cell as coupling law would be incorrect since it is not true to the laboratorial outcome.

The next step is a PSC module simulation. The device will be a monolithic module, with P1, P2 and P3 configuration previously described. For this module, it is important that the gap caused by the scribes (*i.e.* gap is the sum of the width of P1, P2 and P3) should be as narrow as possible to maximize the active area of the device, and the sub-cell width should also be adjusted in order to minimize the resistive losses in the TCO substrate.

First, it is important to establish a gap width. For a more realistic simulation, the gap width should be established as the best obtained in the host laboratory, but since that has not yet been tested, it will be based in a published work. Schultz *et al*. [62] reported, earlier this year, a laser-fabricated PSC module with optimized laser parameters dedicated to enhance the P2 scribe line, resulting in a better performance associated with low resistance between contacts in the P2 zone. The team reported a gap of 500 μm, and a series resistance in the P2 connection between electrodes of 0.01 $\Omega \cdot cm^2$. These values will be used in the simulations.

Then, a simulation-based optimization of the width of each of the scribe zones, P1, P2 and P3 was performed. Since the target is to build a 10 cm x 10 cm module, for the optimization of each scribe width was designed a "mini-module" consisting only of two sub-cells, each with 10 cm height and 1 cm width, since this width should be close to the ideal width to be posteriorly obtained. Although the work reported does not mention individual widths of any of the scribes, in this work it will be considered a minimum width of 50 μm for each of the scribes, since it can become difficult to perform narrower scribes.

In the P3 zone, the charges flow solely through the TCO substrate, which is the component with the higher sheet resistance (7 $\Omega \cdot sq^{-1}$). Therefore, this was established to 50 μm width, and the optimization consisted in adjusting the P1 and P2 widths. In the P1 zone, the charges flow through the back contact, which in this work is a gold layer, with a sheet resistance of 0.407 $\Omega \cdot sq^{-1}$, and the P2 zone has both top electrode sheet resistance as 7 $\Omega \cdot sq^{-1}$ and 0.407 $\Omega \cdot sq^{-1}$ for the bottom electrode, along with a coupling law that assumes ohmic behavior in the contact between both electrodes, with a series resistance of 0.01 $\Omega \cdot cm^2$, as previously mentioned. The following Figure 4.2.5 shows the maximum power generated per area in each mini-module as a function of P2 width. Considering that the total gap is 500 μm, the P1 width will be 500 μm minus the P3 width (50 μm), minus the P2 width (simulated): $w_{P1} = 500 - w_{P3} - w_{P2}$.

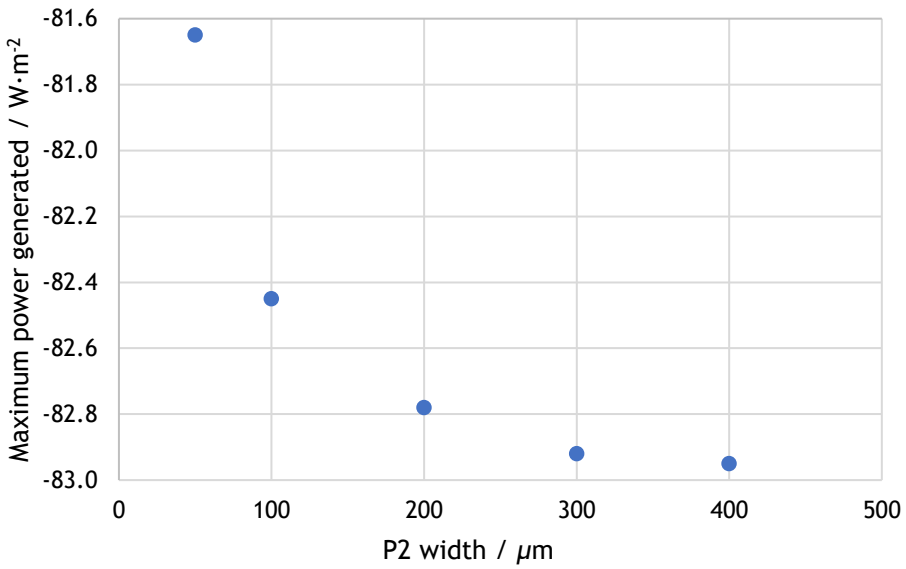

Figure 4.2.5 – Maximum power generated as a function of P2 width.

Although the variation is soft, the case in which the P2 has 400 μm width and the P1 and P3 both have 50 μm is the one that has the better performance, and therefore will be used in simulation.

In the next step, should be determined the ideal number of sub-cells for a 10 x 10 cm^2 module. For that, it is used the *Full module handling* tool from LAOSS. For using this tool, it has to be

defined only the gap width, which was set to 500 μm, and the cell count range (in this case, was performed a simulation between 1 and 20 sub-cells). The software then considers that there are no electrical losses in the interconnection area, simulating the performance for an individual sub-cell. Hence, with increasing number of sub-cells, individual sub-cell width is progressively reduced, giving raise to dead area caused by interconnections, since the total length and height are kept constant: the aperture area is always 100 cm^2. Figure 4.2.6 shows the simulation results obtained.

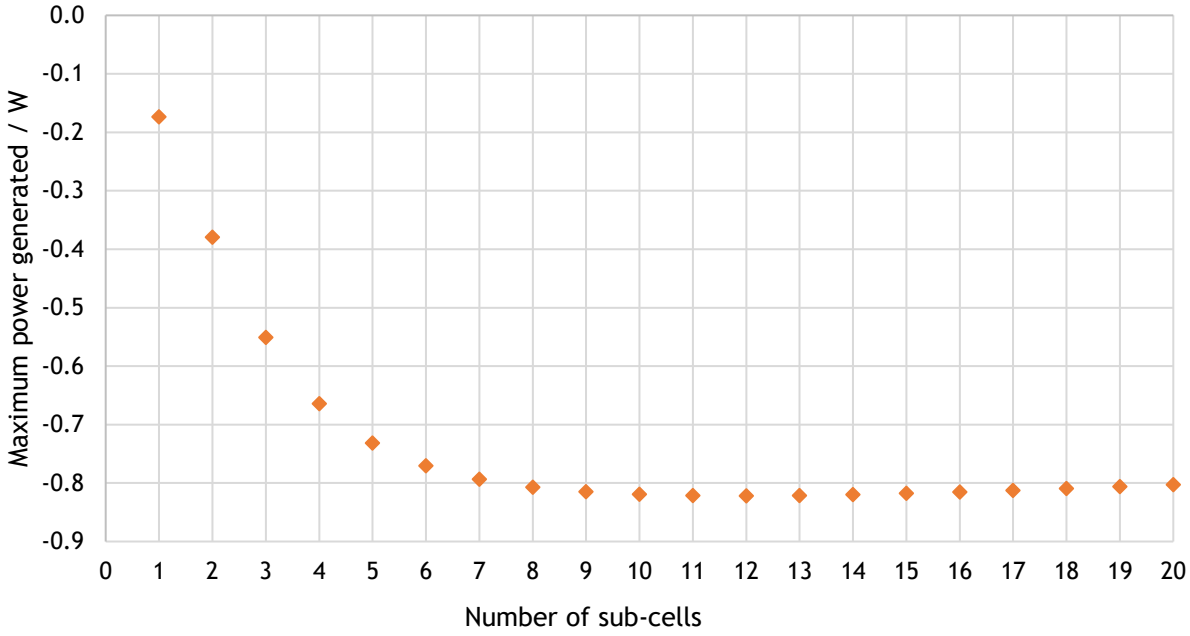

Figure 4.2.6 – Maximum power generated as a function of the sub-cell count (500 µm gap).

The maximum power was registered for a 12 sub-cell module, which corresponds to a 7.875 mm width for each sub-cell. However, it should be highlighted that between the 8 and 20 sub-cell division, the maximum power generated little changed. This may have a special meaning for laboratorial module fabrication, since it is much easier to assemble a module with 8 sub-cell than with 12; the reduction in the number of cells of the module will result in cells with higher width but without severe performance losses.

In the next step, it was drawn a full module using LibreCAD, with the parameters already mentioned: 10 cm height, 10 cm width, 12 sub-cells with 7.875 mm each, and the corresponding gap with 500 μm width. P1 and P3 both have a width of 50 μm and P2 with 400 μm. The Figure 4.2.7 shows the module and an interconnection detail.

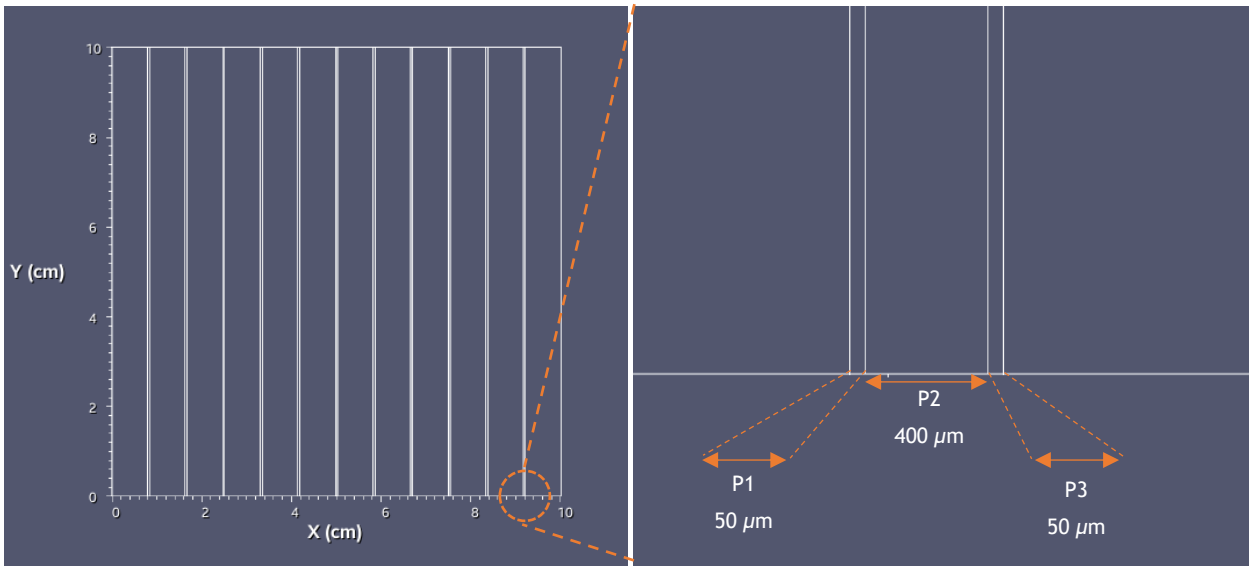

Figure 4.2.7 – Full module and interconnection detail (as seen in LAOSS interface).

Then, a simulation was run to evaluate the performance of the module. As coupling for bottom and top electrodes was used the 8.95 % PCE curve, and all the other parameters were the same as mentioned. The Figure 4.2.8 shows the electrode information input in the software. The value $1x10^{7}$ Ω·sq^{-1} sheet resistance (signaled as 1e+07 Ω/□ in the software) means that in those domains, there is no electrical conductivity. This value is used since it is advised by the software manual.

Geometry/Meshing | Device IVT | Electrodes | Boundary conditions | Sweep | Fit/Optimize | Solver

Subdomains

Name	Top/bottom	Sheet resistance R□	Unit
Default	Top	7	Ω/□
Default	Bottom	0.407	Ω/□
P1	Top	1e+07	Ω/□
P1	Bottom	0.407	Ω/□
P2	Top	7	Ω/□
P2	Bottom	0.407	Ω/□
P3	Top	7	Ω/□
P3	Bottom	1e+07	Ω/□

Figure 4.2.8 – Sheet resistance values for the module sections.

A simulation was then run with a voltage sweep between 0 and 12.84 V (which is the number of sub-cells multiplied by the V_{OC} of the single sub-cell). The Figure 4.2.9 shows the *I-V* curve obtained and the power generated as a function of the voltage of the simulated module.

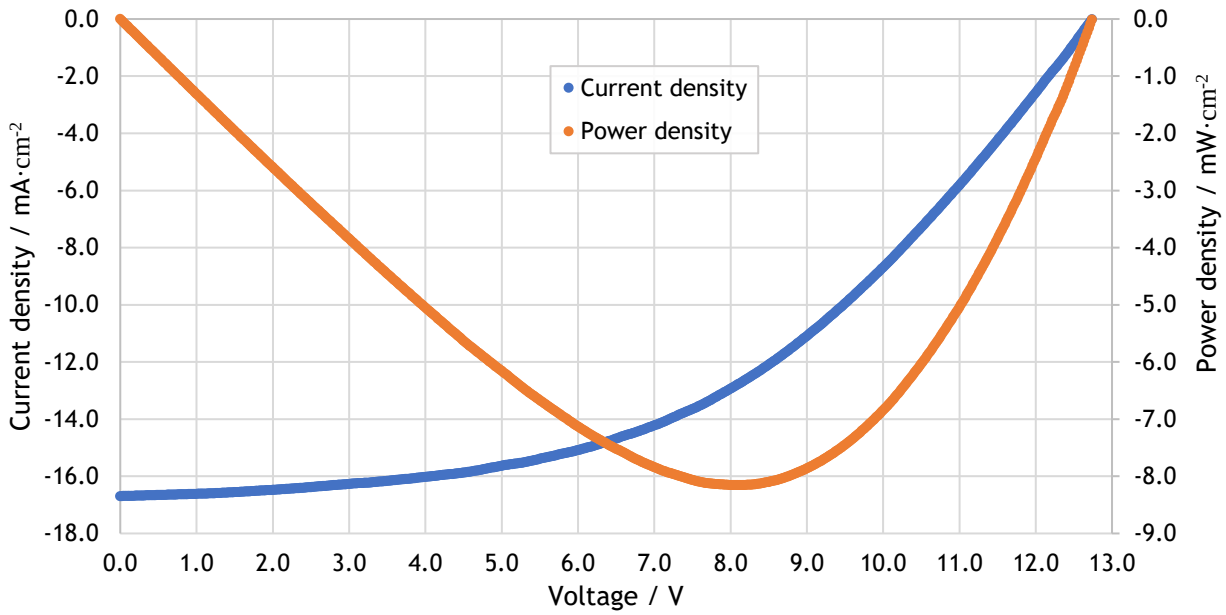

Figure 4.2.9 – Full module current and power density.

The module exhibited:

- 8.16 % PCE (relative to aperture area);
- 0.487 fill factor;
- 12.7 V open-circuit voltage;
- J_{SC} of 16.70 mA·cm^{-2}.

In general, the module results show residual performance losses when comparing to the individual cell. A small downgrade in *FF* from 0.505 to 0.487 is verified, indicating minor losses due to the TCO substrate sheet resistance. However, the J_{SC} kept almost the same (from 16.73 to 16.70 mA·cm^{-2}). These results show that it is possible, with careful optimization, to up-scale PSC devices into large modules without suffering severe losses due to sheet resistance in the TCO substrate. However, must always be kept in mind that it is very important to have a reliable large-scale deposition process, as the perovskite layer quality heavily influences the cell performance. Not only that, but it is also very important to minimize electrical losses in the interconnections, by making them as narrow as possible and not damaging the cell with the laser ablation.

As suggested in Figure 4.2.6, for these interconnection dimensions, a small reduction in the number of sub-cells, resulting in a larger individual width, presents a significant simplification for device fabrication without severely harming the performance of the module. In another simulation, a module with 8 sub-cell was built, resulting in an individual width of 1.206 cm per cell. All the other parameters were kept the same. Figure 4.2.10 shows the resulting *I-V* curve.

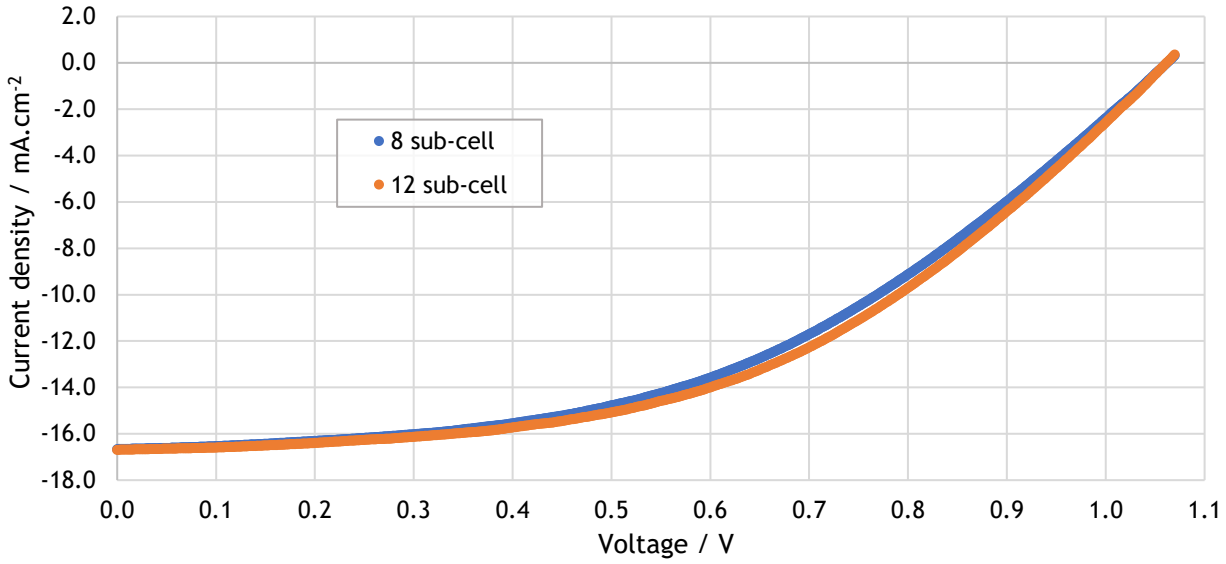

Figure 4.2.10 - Comparison between 8 and 12 sub-cell module. Note: the voltage is divided by the number of the cells of each module.

The voltage was normalized for the voltage of an individual cell (total voltage divided by the number of sub-cells); the modules have great performance similarity, and in fact the PCE only dropped from 8.15 % in the best module for 8.00 % in the 8 sub-cell module, which is an easier-processing alternative for a slight decrease in performance.

Following a more realistic analysis, it will be now shown an analogue simulation where the minimum width for each scribe was considered to be 100 μm instead of 50 μm. The total gap width is still 500 μm and the resistance at the interconnection 0.01 $\Omega \cdot cm^2$. While the *Full module handling* tool, used in LAOSS to determine the ideal number of sub-cells, only considers the total gap width, no additional simulation was needed to determine the ideal division for a 10 cm x 10 cm module. Following the evolution showed in Figure 4.2.5, the P1 and P3 widths were set to 100 μm and P2 width to 300 μm, as shown in Figure 4.2.11.

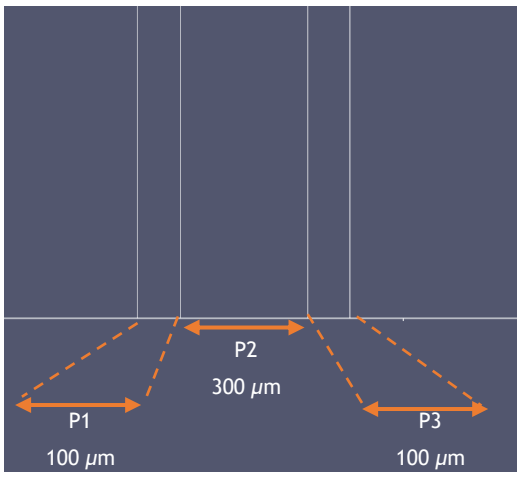

Figure 4.2.11 – Module interconnection zone.

All the remaining parameters for the simulation were the same. The Figure 4.2.12 shows the *I-V* curve and power density as a function of voltage.

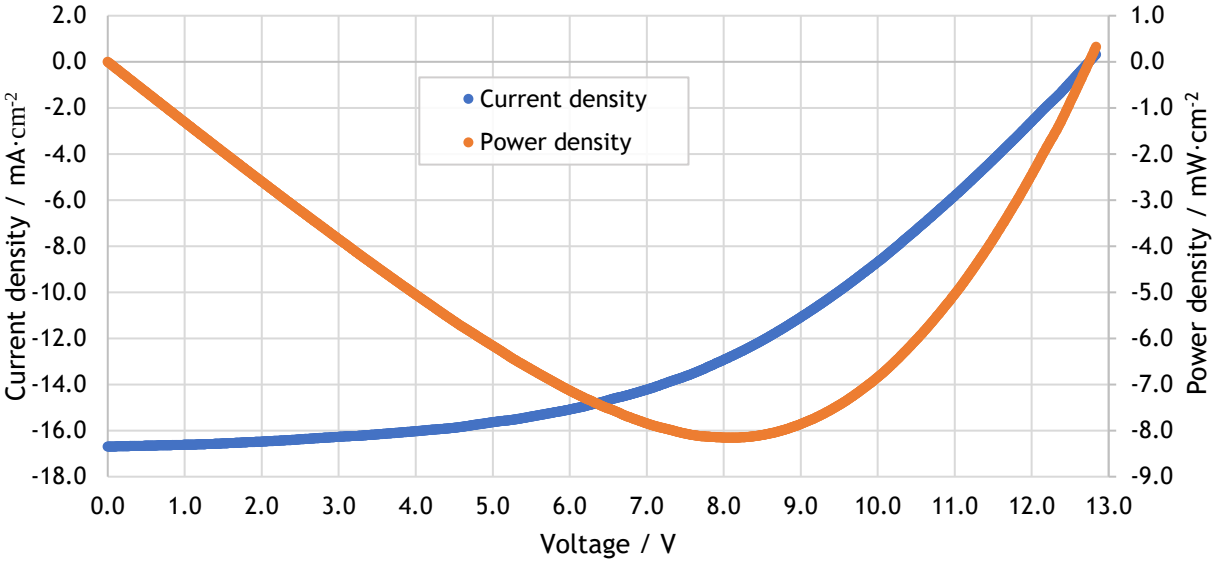

Figure 4.2.12 – Full module current and power density (500 µm gap and 300 µm P2 width).

The parameters obtained are:

- 8.15 % PCE;
- 0.486 fill factor;
- 12.7 V open-circuit voltage;
- J_{SC} of 16.70 mA·cm^{-2}.

The results show that there are almost no losses in the module electrical performance when shifting the minimum scribe width from 50 to 100 µm.

However, on a laboratory scale, it may not be easy to obtain such narrow gaps. High precision laser is required to perform the most accurate scribes. For that reason, in the next step was simulated a module performance considering a minimum gap width of 1 mm. The interconnection resistance in the P2 zone is considered to be 0.01 Ω·cm^2 and, as shown in Figure 4.2.5, the case considered is the maximum P2 width. A simulation with the *Full module handling* tool was performed to assess the ideal number of sub-cells for this 1 mm gap width. The results are shown in Figure 4.2.13.

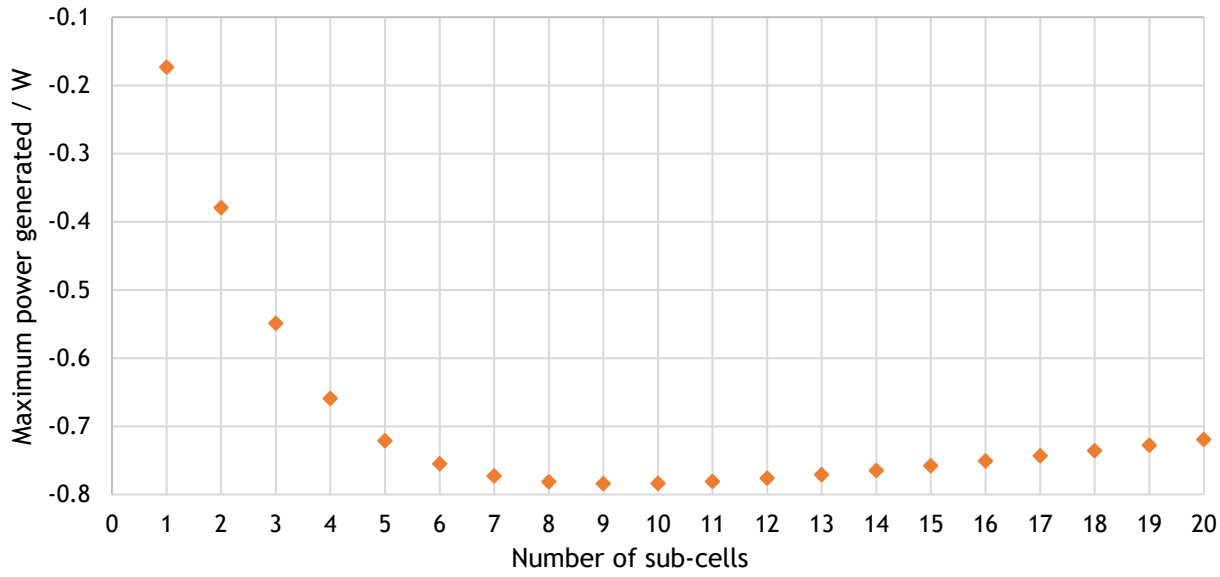

Figure 4.2.13 - Maximum power generated as a function of the sub-cell count (1 mm gap).

The simulation output shows that 9 is the ideal sub-cell number for the module, with a corresponding 0.78 W of maximum power. Again, it is important to note that, between 7 and 12 cells does not seem to exist major performance losses, which can present as an important indicator for device building, since the simplicity in fabrication is an important factor either for laboratorial and industrial mass production.

Then, a module was drawn in LibreCAD according to the ideal number of sub-cells, considering a minimum scribe width of 100 μm for P1 and P3. In this case, w_{P2} = 800 μm. The simulation was run, and the Figure 4.2.14 shows the results obtained.

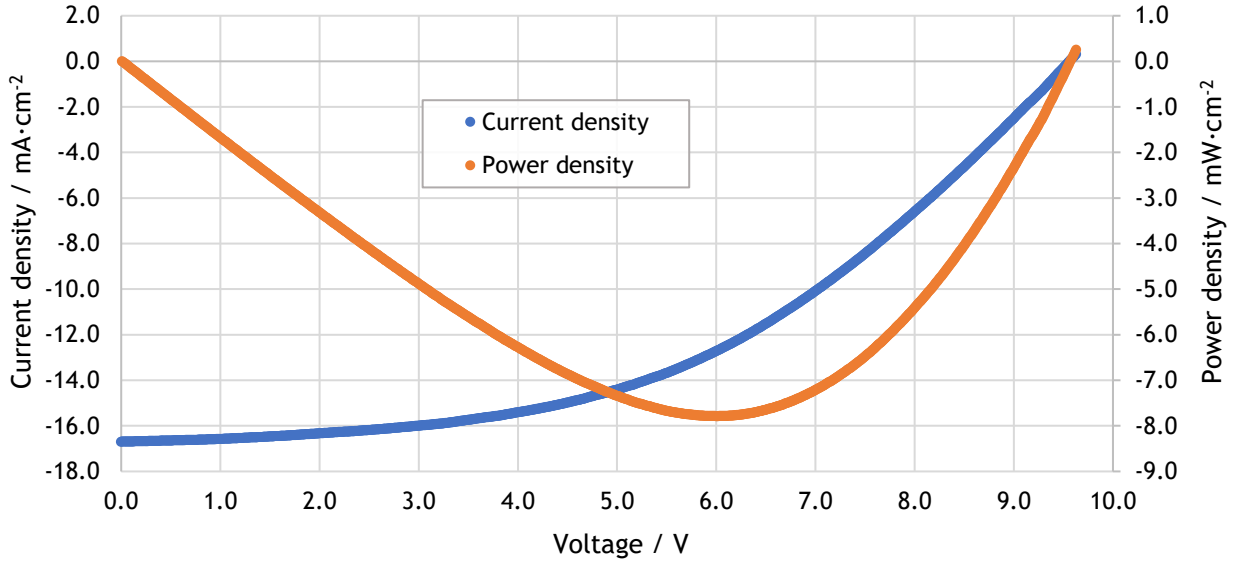

Figure 4.2.14 - Full module current and power density (1 mm gap and 800 µm P2 width).

The module exhibited:

- 7.79 % PCE (relative to aperture area);
- 0.478 fill factor;
- 9.56 V open-circuit voltage;
- J_{SC} of 16.70 mA·cm^{-2}.

In this case, a slight fall on the *FF* is verified. PCE drops 5 % from the best case scenario for a 500 μm total gap width. In short, some downgrades in performance are starting to be noticed. It should be noted that the decrease in V_{OC} is due to the reduction of the number of sub-cells: voltage generated per cell remains similar, as well as the J_{SC}. So, the number of cells selected for each module should also take into account the desired final power output of a module.

Again, in the next step, was evaluated the influence of a limitation in the minimum scribe width. Hence, P1 and P3 width were set to 200 μm and P2 width to 600 μm. Figure 4.2.15 shows the characteristic and power curves obtained.

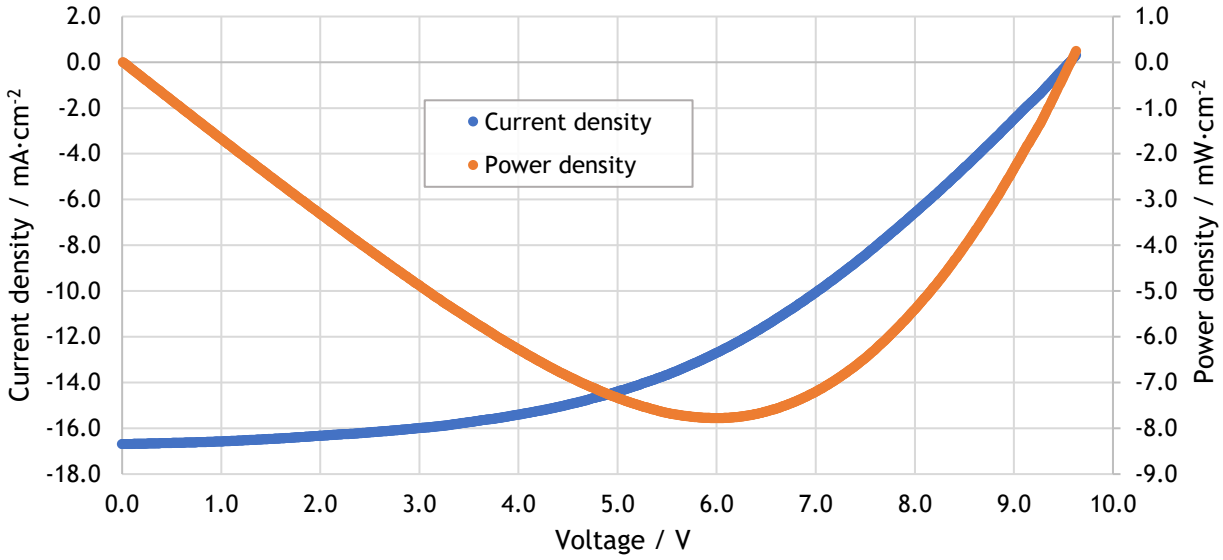

Figure 4.2.15 - Full module current and power density (1 mm gap and 600 µm P2 width)

The parameters obtained are:

- 7.78 % PCE;
- 0.477 fill factor;
- 9.56 V open-circuit voltage;
- J_{SC} of 16.7 mA·cm^{-2}.

Again, great similarity was shown between the performances of modules with different minimum scribe widths. Should also be mentioned that in laboratory scale, what happens in the interconnection zone is true to the widths mentioned for each scribe. In fact, P1 and P3 should be narrow enough to isolate both sub-cells, whereas in the P2 zone there has to be a

successful deposition of the back contact in order to the charges flow from one sub-cell to the next with the minimal resistive losses possible. Also, as shown in Figure 2.3.1, the scribes are not immediately followed, and rather have a small space between them, for avoiding short-circuits. Since that space is not considered for the simulations, it can be deemed as a small fraction of the P2 widths mentioned in this thesis. This means that the greater impact of the scribes in the module performance is related with its effectiveness in avoiding short-circuit between electrodes in individual cells and between cells in a module.

Further simulations were run to evaluate more widely the effect of the total gap width in interconnections. For a total gap width of 1.5 mm (with a 150 μm minimal scribe width), a *Full module handling* simulation was executed to determine the ideal number of 8 sub-cells for a 10 cm x 10 cm module, and another similar simulation for a 2 mm gap (with a 200 μm minimal scribe width), having obtained the best performance for a module with 7 sub-cells. The following Figure 4.2.16 shows the variation of the PCE and fill factor for each of the modules.

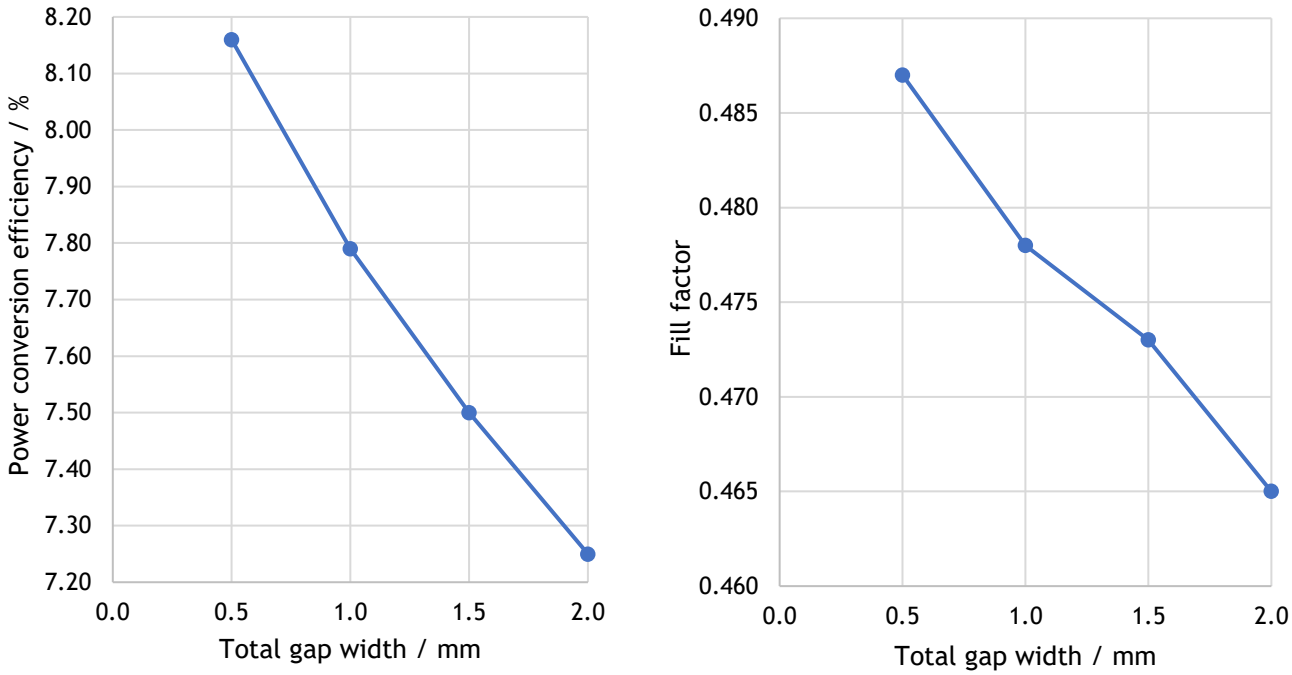

Figure 4.2.16 – PCE and fill factor variation with total gap width.

The graphs show that there is, in fact, some losses in performance when increasing the total interconnection width between the sub-cells in a module. This brings focus to the importance of developing skilful laser ablation processes, being able to perform precise and narrow scribes, maximizing the active area of the cell. However, with increasing gap width, the suitable number of sub-cells decreases (12 → 9 → 8 → 7), which means more ease in the fabrication process. Hence, the design of the module always depends on the application desired. To obtain the ideal module, nonetheless, a previous careful optimization via a simulation software may

be really helpful in order to determine the suitable dimensions for each case, having the profit of using both practical capabilities and theoretical predictions.

Other than geometrical parameters, the resistance at the P2 interconnection, between the back contact of a sub-cell and the front contact of the other, is also an important constraint for an efficient module performance. For the previous performed simulations it was considered a resistance of 0.01 Ω·cm^2, but this value may be dependent on the quality of the scribing process, as well as of an eventual cleaning process on the P2 scribe zone, which is benefit for the charge travelling [60]. To assess this topic multiple simulations were run varying the resistance between 0.01 and 0.15 Ω·cm^2. The PSC module simulated considered 12 sub-cells with 500 μm total gap width, w_{P1} = w_{P3} = 50 μm and w_{P2} = 400 μm - Figure 4.2.17. All the other parameters (*I-V* input correlation, sheet resistance and sweep range) were used as mentioned for the previous simulations.

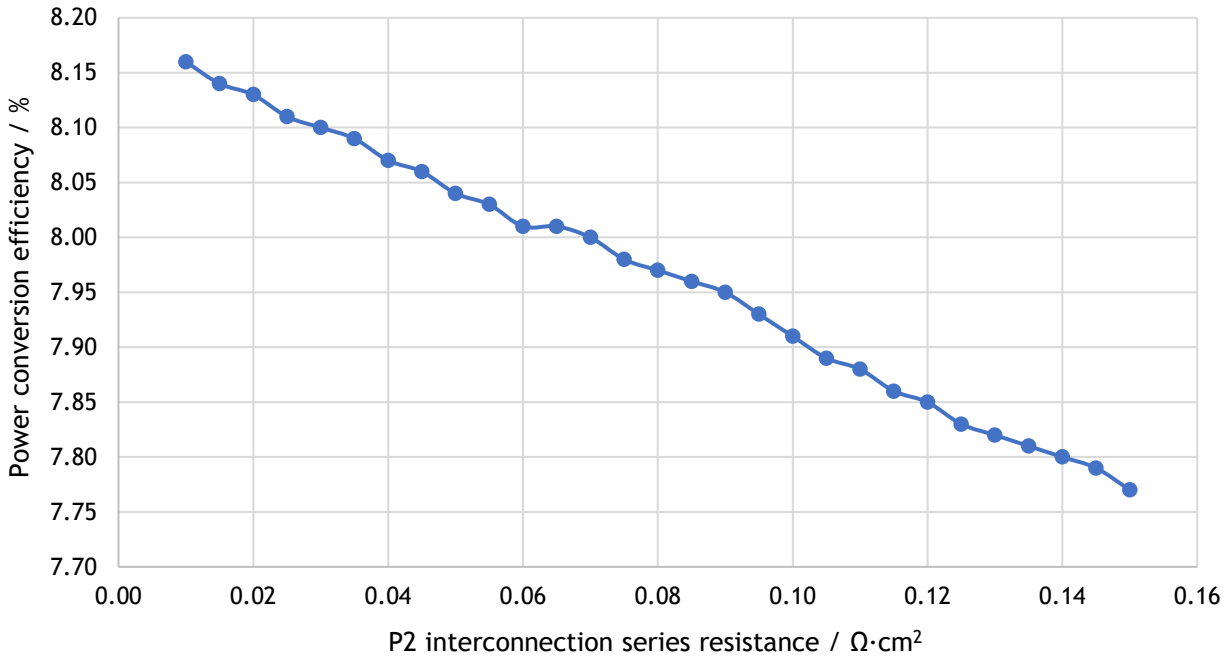

Figure 4.2.17 – PCE obtained as a function of the P2 interconnection resistance.

The results show that there is a steady loss on performance when increasing the resistance. Therefore, additional precaution must be taken when scribing the P2 zone. Residuum or heat damage may harm the charges flow at the interconnection, resulting in a performance decrease [60].

5 Conclusion

Upscaling PSC devices into modules is an important step towards commercialization of this technology. However, some challenges must be addressed, namely the deposition methods over large area and the increasing substrate resistance. In this work, PSCs were fabricated in the laboratory and then the software LAOSS was used to assess the impact of the substrate resistance on the cell dimensions increase. For laboratorial cells, the maximum PCE obtained was 8.95 %, for a 5 cm^2 cell. When comparing experimental work with equivalent results obtained from simulations, the outcomes reveal that the losses solely due to the substrate resistance in TCO are short and therefore there must be a careful optimization of the laboratorial procedure for large area devices.

The results shown that the total gap width and the series resistance at the P2 interconnection were the most important factors for performance losses, and the power conversion efficiency and fill factor are the parameters most affected, with the V_{OC} and J_{SC} remaining almost unchanged with small sub-cell widths. The simulations revealed a loss of approximately 5 % in efficiency for an increase of 500 μm on the interconnection width. For a 10 cm x 10 cm module with an interconnection gap width of 500 μm, the PCE obtained was 8.16 %, having decreased to 7.25 % for a 2 mm gap, and the *FF* reduced from 0.487 To 0.465. Increasing from 0.01 to 0.15 $\Omega \cdot cm^2$ resistance at the interconnection between two sub-cells also showed to provoke a drop of 5 % in the PCE. It was concluded that P1 and P3 should be as narrow as possible, avoiding short-circuits in the interconnection zone, whereas P2 width should be maximized. The conclusions show that it is important to adopt very precise and efficient laser ablation processes to perform the scribes in the modules, always aiming to minimize the scribe width and the damage in the devices. However, for laboratorial fabrication and mass production at industry level, simplifying the fabrication process means cost reduction. In this thesis, it has been shown that a slight reduction in the number of sub-cells of a module, thus simplifying its design, may result in an unimportant performance loss, giving advantage for the manufacturer.

All in all, it may be concluded that practical capabilities and theoretical predictions complement each other, since a simulation work can only be performed based on experimental values for physical limitations, and the simulation tool gives very important inputs on what options to take when building a module. Combining both approaches it is very important to effectively build a large module with minimized electrical losses, allowing to shift the outstanding PCEs from small cells to large, commercial-sized perovskite devices.

6 Assessment of the work done

6.1 Objectives Achieved

As for the initial objective defined, due to unfortunate circumstances, it was not possible to build a module on laboratory, nor to test and optimize perovskite deposition by slot-die technique. Nevertheless, these objectives were adapted to a more theoretical approach by performing the simulation of PSC module design in terms of dead-areas, interconnections and sub-cell number, allowing to obtain important know-how for future modules fabrication. A solid base theoretical predicting knowledge was acquired, allowing to foresee the best options to adopt when building modules in laboratorial environment – which, in fact, is the most important information to be obtained, since this work was developed within a laboratorial perspective and background. The redefined objectives have been, therefore, achieved.

6.2 Other Work Carried Out

During the course of this semester, I also had the opportunity to participate in a review paper concerning the commercialization of PSC technology. In that paper, I wrote a detailed section concerning the evolution of PSC modules over the past few years and of the major challenges faced upon upscaling PSC devices.

6.3 Final Assessment

From my personal view, I would be really happy to contribute to the upscaling works that are being carried out in the host laboratory at a module-level but, unfortunately, it was not possible. Working from home for so long and in a project of this dimension was something new for me, and really challenging at times. However, with the constant communication and great support I have received, especially from my supervisor, it has been developed – what I believe to be – a good work, with important prospects that enabled a solid understanding of the software. In fact, in this period I have been able to produce not only both laboratorial and simulation work, but also written a part of a review paper, which demanded great bibliographic research and correspondent understanding of the topic. But the greatest novelty for me was the use of the software: not me, nor anyone else at the host laboratory had used this software before, and so it was totally up to me to learn how to use it, skillfully enough to produce results worthy for a master thesis, in a relatively short period of time, with little more than the tutorials to help me. I hope that this understanding can be a very important tool for a more accurate module building for future developments at laboratory scale, aiming to make PSC a rentable, industrial-fit technology, ready to revolutionize the photovoltaic market, offering a better alternative to the conventional products currently in use.

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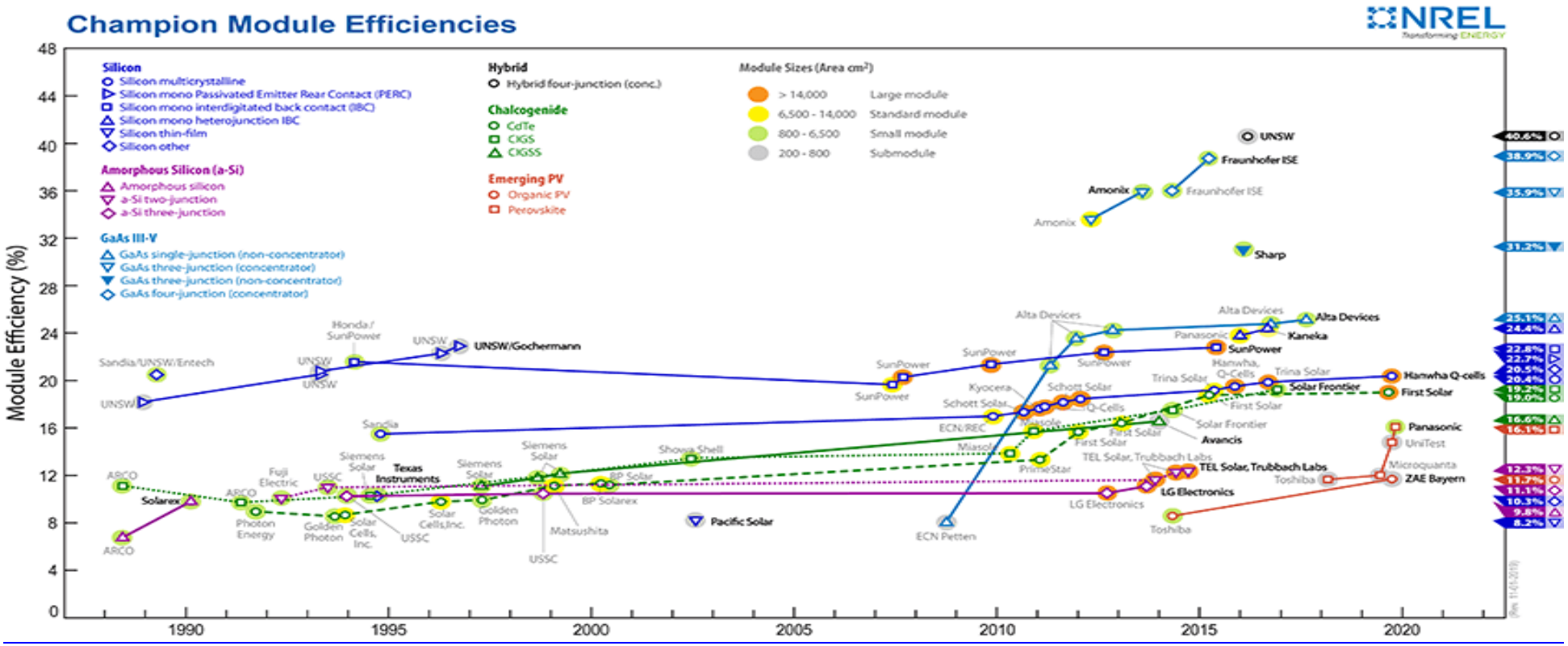
Appendix 1: National Renewable Energy Laboratory: Champion Photovoltaic Module Efficiency Chart



Champion Photovoltaic Module Efficiency Chart, NREL; consulted on 1/7/2020. Available from https://www.nrel.gov/pv/module-efficiency.html