The two main goals of the development of digital filter architectures and hardware implementations are arguably the achievement of higher processing speeds and of higher integration levels, in particular the integration of filters into VLSI packages. Of particular interest are architectures that lead naturally to pipelined implementations, as the speed-up potential of pipelines is fully realized in the processing of the very long streams of data typically encountered in digital filtering.

Wave Digital Filters were proposed by Fettweis as an alternative to conventional digital filter structures. The main motivation for the use of this class of filters is their lower sensitivity to the values of the filter coefficients. Their main disadvantage is perhaps a higher circuit complexity when compared with conventional digital filter implementations. The lower sensitivity to the filter coefficients, however, can be exploited to simplify the hardware, by reducing the filter coefficient word size, which not only reduces the multiplier complexity but may also lead to a speed increase. One particular type of WDF structure, the unit element chain, is particularly interesting from the point of view of achieving high processing speeds via pipelining, as it consists of a number of processing units separated by registers. Furthermore, the segments of this pipeline are identical, which simplifies its integration. Another interesting characteristic is that the structure can be used to implement all-pass responses, and can therefore be used to provide group delay equalization.
In the work summarized here, the unit element chain wave digital filter design and hardware implementation are considered. The proposed design technique uses a direct search method to perform a discrete optimization. With this design technique the filter coefficients can be obtained directly from the specifications of the amplitude or the phase frequency responses of the filter.

Two architectures are proposed for the hardware implementation of this type of filter. In both of them, a fast computation time is made possible by implementing the required multiplications using shifts. The values of the filter coefficients are therefore restricted to simple combinations of powers of 1/2. The two proposed structures differ in the hardware complexity they require and in their computation speed. The computation rates of these two architectures are approximately given by the inverse of the time required to perform two or three additions.

Several sample designs are given, and their scaling and noise performance are discussed. Measurements of the characteristics of these sample designs, implemented on a general purpose DSP chip are also given.