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SINGLE-STAGE, BIDIRECTIONAL AC-DC MATRIX CONVERTER FOR ENERGY STORAGE SYSTEMS

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Single-stage, Bidirectional AC-DC Matrix Converter for Energy Storage Systems

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Abstract

The integration of more renewable energy sources (RES) in the electric power grid is raising huge challenges for the transmission and distribution system operators. Balancing consumption and generation is becoming more difficult due to the intermittency and unpredictability of the RES. In addition, the arising of new loads such as the electric vehicles (EV) is pushing the limits of the conventional power grid. Energy storage is seen as a key solution to mitigate the intermittency of the renewable generation, to reduce the need for grid reinforcement and expansion, and to provide more flexibility and security to the power grid. Inserting energy storage systems in the low voltage (LV) grid and in the proximity of the *prosumers* is becoming a trend with several pilot projects being concluded in the last few years. Due to the proximity to the costumers, this system is commonly named community energy storage (CES). The use of batteries seems to be the more promising technology for these systems enabling both energy and power storage functionalities.

The battery energy storage systems (BESS) need a bidirectional AC-DC power conversion system (PCS) to interface a battery pack with the electric power grid. The aim of this work is to increase the power density of the power electronics converter and keep simultaneously the same reliability of traditional solutions. These goals are pursued through the reduction of the conversion stages and utilization of design methodologies to reduce the volume of the passive components. The matrix converter is a key element of the system, since it performs a direct AC to AC conversion between the grid and the high-frequency transformer (HFT) dispensing the traditional DC-link capacitors. Therefore, the circuit volume and weight are reduced and a longer service life is expected when compared to the existing technical solutions. The interface between the HFT and the battery pack is then performed by a full-bridge (FB) converter. The resulting power circuit is the commonly known high-frequency link matrix converter (HFLMC). A new modulation for the HFLMC is proposed in this thesis featuring controllable power factor in the grid interface as well as voltage and current regulation for a battery energy storage device.

A prototype was built to verify the feasibility and performance of the proposed modulation. An electromagnetic interference (EMI) filter for differential-mode and common-mode filtering was designed for compliance with CISPR 11 Class B standard. Regarding the

magnetic components, analytic and software tools were employed for the optimized design of the high-frequency transformer and link-inductor. The control system is composed by a digital signal processor (DSP) plus a field-programmable gate array (FPGA) for the signal acquisition and generation of the sixteen command signals. Silicon carbide (SiC) MOSFETs are used in order to allow high switching frequency with low losses. The respective gate driver circuit was developed to allow safe and reliable commutations up to 100 kHz. This research was conducted in the Smart Grids and Electric Vehicles (SGEV) laboratory of INESC TEC. The experimental tests show the capability to control the grid currents in the synchronous reference frame in order to provide grid services. Simultaneously, the battery current is well regulated with a small ripple which makes this converter suitable for battery charging of electric vehicles and energy storage applications.

Resumo

A integração de mais fontes de energia renovável na rede elétrica está a colocar enormes desafios para os operadores das redes de transmissão e distribuição de energia. O balanceamento do consumo e geração tem-se tornado mais difícil devido à intermitência e imprevisibilidade das fontes de energia renovável. Além disso, o aparecimento de novas cargas no sistema, como por exemplo os veículos elétricos, está a puxar pelos limites da rede elétrica convencional. O armazenamento de energia é por isso visto como uma solução chave para mitigar a intermitência da produção renovável, reduzir a necessidade de reforço e expansão da rede, bem como fornecer mais flexibilidade e segurança à rede elétrica. A introdução de sistemas de armazenamento de energia na rede de baixa tensão, e junto aos chamados *prosumers*, está a tornar-se uma tendência com diversos projetos piloto realizados nos últimos anos. Dada a proximidade com os clientes, estes sistemas são habitualmente chamados de armazenamento de energia comunitário. As baterias parecem ser a tecnologia mais promissora para estes sistemas, uma vez que permitem fornecer tanto funcionalidades de armazenamento de energia como de potência.

Os sistemas de armazenamento de energia com baterias precisam de um conversor de potência AC-DC bidirecional para fazer a interface com o *pack* de baterias e a rede elétrica. A principal motivação deste trabalho é aumentar a densidade de potência do conversor mantendo simultaneamente a mesma fiabilidade das soluções convencionais. Estes objetivos são perseguidos através da redução dos andares de conversão e da utilização de métodos de design para reduzir o volume dos componentes passivos. O conversor matricial é por isso um elemento chave do sistema, uma vez que realiza diretamente a conversão AC-AC entre a rede e o transformado de alta frequência, dispensando os tradicionais condensadores de barramento DC. Desta forma, o peso e o volume circuito de potência são reduzidos e o tempo de serviço é estendido quando comparado com as soluções atuais de conversão. A interface entre o transformador e o *pack* de baterias é por sua vez realizado por um conversor em ponte completa. O resultante circuito de potência designa-se habitualmente por conversor matricial com ligação de alta frequência (HFLMC). Nesta tese é proposta uma nova modulação para o HFLMC que permite controlar o fator de potência na rede bem como a regulação da tensão e da corrente nas baterias.

Foi projetado e construído um protótipo para verificar a viabilidade e desempenho da modulação proposta. Foi também desenhado um filtro de interferência eletromagnética para as componentes de modo comum e modo diferencial de forma a cumprir com a norma CISPR 11 Class B. Relativamente aos componentes magnéticos, foram utilizadas ferramentas analíticas e de *software* para a otimização do desenho do transformador de alta frequência e da bobine de ligação. O sistema de controlo é composto por uma DSP e uma FPGA para a aquisição dos sinais e geração dos dezasseis sinais de comando. São utilizados SiC MOSFETs uma vez que permitem a comutação a alta-frequência com baixas perdas. O respetivo circuito de comando foi desenvolvido para permitir comutações seguras e com fiabilidade para frequências de comutação até 100 kHz. Este trabalho de investigação foi desenvolvido no Laboratório de Redes Inteligentes e Veículos Elétricos do INESC TEC. Os testes experimentais revelaram a capacidade de controlar as correntes no referencial síncrono de forma a serem fornecidos serviços de redes. Simultaneamente, a corrente na bateria é regulada corretamente com baixo oscilação o que torna este conversor adequado para o carregamento de veículos elétricos e para aplicação em sistemas de armazenamento de energia.

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DIOGO ANDRÉ CERQUEIRA PINTO BEZERRA VARAJÃO

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"If things are not failing, you are not innovating enough."

Elon Musk

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List of Abbreviations

ADC	Analog to Digital Converter
AMI	Advanced Metering Infrastructure
AVG	Average
AWG	American Wire Gauge
BBB	Bidirectional Buck-boost
BESS	Battery Energy Storage System
BMS	Battery Management System
BP	Balancing Power
BSO	Branch Switch Over
BSW	Bidirectional Switch
CAES	Compressed Air Energy Storage
CBC	Current-based Commutation
CCM	Continuous Conduction Mode
CE	Conducted Emissions
CES	Community Energy Storage
CHB	Cascaded H-bridge
CISPR	International Special Committee on Radio Interference
CM	Common-mode
CPES	Centre for Power and Energy Systems
CSC	Current Source Converter
CSR	Current Source Rectifier

CSVM	Conventional SVM
DAB	Dual Active Bridge
DCM	Discontinuous Conduction Mode
DER	Distributed Energy Resources
DG	Distributed Generation
DM	Differential-mode
DMC	Direct Matrix Converter
DSO	Distribution System Operator
DSP	Digital Signal Processor
DSVM	Direct Space Vector Modulation
DUT	Device Under Test
EES	Electrical Energy Storage
EM	Electric Motor
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EMS	Energy Management System
EPS	Electric Power System
ESS	Energy Storage Systems
EV	Electric Vehicle
FB	Full-bridge
FCV	Fuel-Cells vehicles
FIR	Finite Impulse Response
FLC	Flying Capacitor
FNN	Forum Network Technology/network operation in the VDE
FPGA	Field-programmable Gate Array
FWD	Freewheel Diodes
GaN	Gallium Nitride
GM	Gain-margin

GUI	Graphical User Interface
HC	Hybrid Commutation
HDC	DC Premagnetization
HEV	Hybrid Electric Vehicles
HF	High-frequency
HFL	High-frequency Link
HFLMC	High-frequency Link Matrix Converter
HFT	High-frequency Transformer
HS	Hard Switching
IAP	Interoperability Architecture Perspective
IC	Integrated Circuit
ICE	Internal Combustion Engine
IEA	International Energy Agency
IEC	International Electrotechnical Commission
IGBT	Insulated-Gate Bipolar Transistor
IL	Insertion Loss
IMC	Indirect Matrix Converter
ISVM	Indirect Space Vector Modulation
LF	Low-frequency
LFT	Low-frequency Transformer
LISN	Line Impedance Stabilizing Network
LUT	Lookup tables
LV	Low Voltage
LVRT	Low-voltage Ride Through
MC	Matrix Converter
MCU	Microcontroller Unit
MIMO	Multiple Input, Multiple Output
MKP	Metallized Polypropylene Capacitor

MLC	Multilevel Converter
MLS	MATLAB/Simulink
MLT	Mean Length Turn
MMC	Modular Multilevel Converter
MMF	Magnetic Flux
MOSFET	Metal–oxide–semiconductor Field-effect transistor
MV	Medium Voltage
NPC	Neutral-point Clamped
PCB	Printed Circuit Board
PCC	Point of Common Coupling
PCS	Power Conversion System
PE	Protective Earth
PFC	Power Factor Correction
PHEV	Plug-in Hybrid Electric Vehicles
PHS	Pumped Hydro Storage Systems
PI	Proportional-Integral controller
PLL	Phase-locked Loop
PM	Phase-margin
POHC	Partial Odd Harmonic Current
PSM	Phase-shift Modulation
PV	Photovoltaic
PWM	Pulse-width Modulation
QP	Quasi-peak
RB-IGBT	Reverse Blocking IGBT
RES	Renewable Energy Sources
SC	Supercapacitor
SGEV	Smart Grids and Electric Vehicles
SGIRM	Smart Grid Interoperability Reference Model

Si	Silicon
SiC	Silicon Carbide
SISO	Single Input, Single Output
SM	Submodules
SMPS	Switched-Mode Power Supply
SNR	Signal-to-Noise Ratio
SOC	State of Charge
SOH	State of Health
SPI	Serial Peripheral Interface
SPWM	Sinusoidal Pulse-width Modulation
SRF	Self Resonant Frequency
SSV	Switching Space Vectors
SVM	Space Vector Modulation
SwC	Switching Cell
TCM	Triangular Current Mode
TDD	Total Demand Distortion
THD	Total Harmonic Distortion
TMU	Trigonometric Math Unit
TR	Test Receiver
TRL	Technology Readiness Level
TSO	Transmission System Operator
UPS	Uninterruptible Power Supply
UVLO	Under Voltage Lockout
VBC	Voltage-based Commutation
VDE	Association for Electrical, Electronic & Information Technologies
VNA	Vector Network Analyzer
VRE	Variable Renewable Electricity
VSC	Voltage Source Converter

VSI	Voltage Source Inverter
WBG	Wide-bandgap semiconductors
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

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Chapter 1

Introduction

1.1 Research Motivation

The increased penetration of renewable energy sources (RES) along with the integration of electric vehicles into the utility grid is creating a need for more distributed energy storage [1, 2]. The recent International Energy Agency (IEA) outlook [3] presents up to date projections of energy trends through to 2035. It projects that the world electricity demand increases by more than two-thirds over the period 2011-2035, and nearly half of the net increase in generation comes from variable renewable electricity (VRE). In this way, the share of renewables in total power generation rises from 20 % in 2011 to 31 % in 2035 [3]. Another interesting projections for photovoltaic (PV) and wind contribution to final European Union (EU) 27 electricity demand are shown in Figure 1.1. It is expected a combined penetration of 45 % for these two major variable renewables to final EU 27 demand in the year 2030 [4].

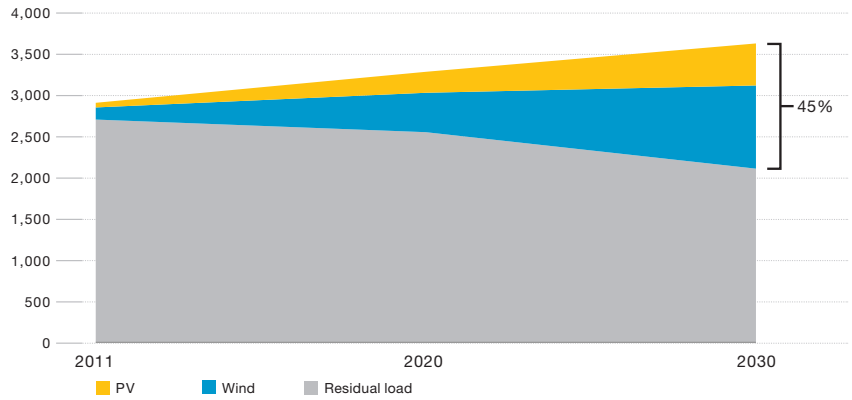


Figure 1.1: Projected PV and wind contribution to final EU 27 electricity demand until 2030 (TWh) [4].

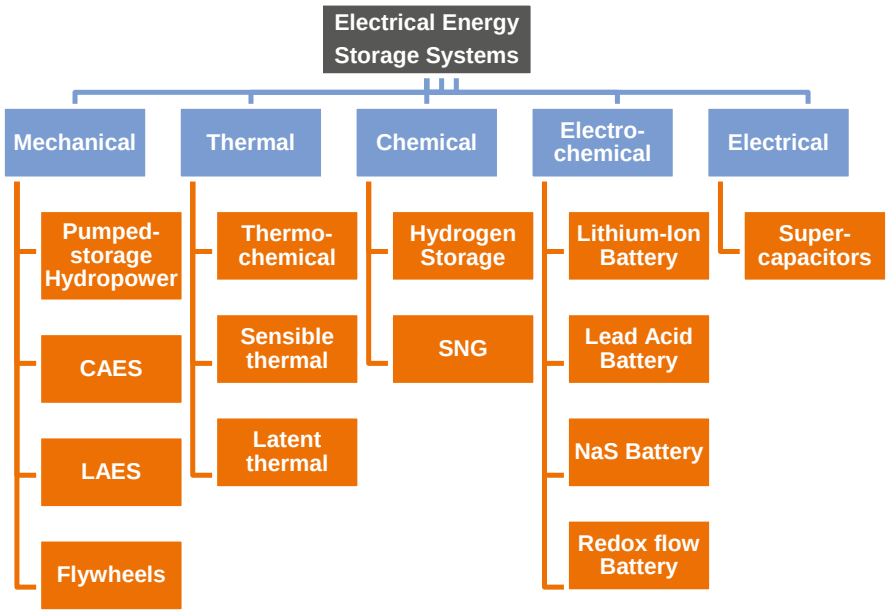


Figure 1.2: Classification of electrical energy storage systems according to energy form [13].

In addition to the rapidly increasing electricity demand, the dramatically escalate of oil prices, the aging of the grid infrastructure, and the need to reduce CO_2 emissions are factors that offer a new set of challenges in balancing consumption and generation [5]. As concluded in [6], the use of decentralised battery energy storage systems (BESS) is a technical and economical alternative to curtail PV systems and wind turbines for the provision of balancing power (BP). The IEA estimates that 500GW of energy storage capacity is required in 2050 [7]. Energy storage is seen as a solution since it can be used to mitigate the intermittency of RES, reduce the need for grid reinforcement and expansion, and supply more flexibility and security to the grid [1, 8–11].

1.1.1 Energy Storage at the different grid levels

Since electrical energy is a form of energy that cannot be effectively stored in bulk, it needs to be converted into a different form for storage [8]. The electrical energy storage (EES) systems can be classified according to the form of energy used. In Fig. 1.2 EES systems are classified into mechanical, thermal, chemical, electrochemical, and electrical energy storage systems [12].

According to International Electrotechnical Commission (IEC), almost 99 % of world-wide storage capacity is provided by large-scale Pumped Hydro Storage Systems (PHS) [12]. The original intent of these plants was to provide demand levelling at a transmission level, but was further expanded to provide ancillary service functions such as frequency regulation in both pumping and generation mode [1]. Another technology for bulk storage is

Compressed Air Energy Storage (CAES). By compressing air during off-peak periods it allows simultaneously increase the efficiency of gas turbines and produces electricity during peak periods at lower costs [1, 9]. Fig. 1.3 shows the worldwide installed capacity of EES systems where is patent the predominance of PHS and CAES. Since PHS and CAES are connected to the transmission lines and generally located faraway from load centers, they can do little to handle potential congestion issues that affect transmission and distribution networks [1].

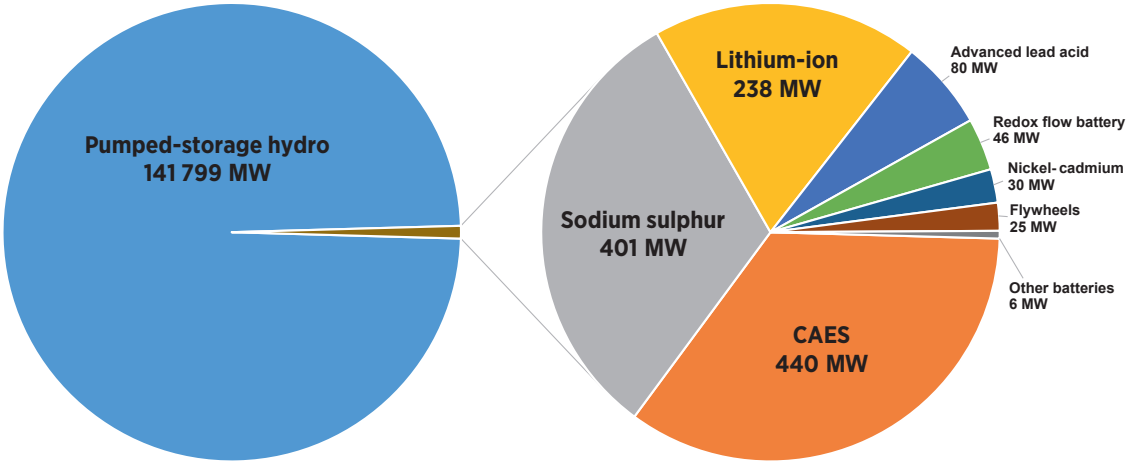


Figure 1.3: Worldwide installed storage capacity for electrical energy in 2015 [14].

Since in the future, intermittent generation will provide the majority of consumed energy, the grid will need more storage capacity as well as more flexible and more dynamic reaction [9]. In this way, it is important to distinguish "energy storage" from "power storage" since they have different and unique capabilities. The "energy storage" has the capability of time shifting and so is mainly used to leveling the load diagram. On the other hand, "power storage" is focused on speed of response capability, that is used for frequency regulation and spinning reserve [1]. Studies were conducted and it was stated in [15] that the fast response (4 second to achieve full power) is worth twice as much as slower response (20-min ramp-up for generation assets) [1]. Systems like batteries and flywheels have very fast response time, and consequently they can affect frequency control with less energy as compared with fossil fuel plants [1], since the interface is implemented using power electronic converters. Thus, the dynamic reaction associated to "power storage" is even more important than its long term capacity associated to "energy storage" [9]. The energy to power ratio (E2P) describes the ratio of installed capacity (energy) and installed power[16]. Storage systems with a high E2P can deliver energy for a longer time than storage systems with a small E2P. Table 1.1 presents a comparison between energy storage and power storage, with the description of the operation modes, technologies and functionalities.

Table 1.1: Comparison between energy storage and power storage.

	Energy storage	**Power storage**
E2P	1 – 10h	$<$ 0,5 h
Capability	time shifting	speed of response
Operation	operation takes place for long periods and uses a significant part of total stored energy	operation during short periods with up to the maximum available power rating
Technologies	pumped hydro storage, compressed air energy storage, thermal energy storage and most battery types	capacitors, superconducting magnetic energy storage, electrochemical batteries, flywheels, and variable speed pumped hydro storage
Functionalities	peak shaving, load leveling, buffer and smooth RES intermittency (capacity firming), avoid reverse power flow to MV, grid upgrade deferral	voltage support, frequency regulation, spinning reserve, power factor correction and harmonic filtering, uninterruptible power supply (UPS)

It is foreseen that the market for flywheels and supercapacitors will be focused more on selling ancillary services to distribution grids, like voltage and frequency stabilization [9]. Due to its higher energy density, batteries have the unique potential to provide energy storage services at all levels of the grid, while also providing several pure power storage services [9, 11]. Fig. 1.4 shows the potential contribution of the BESS in the energy transition until 2030. These systems can be fitted to either high power or high energy applications, and typically range from 2 kW (5 kWh – 20 kWh) up to 50 MW (MWh scale) [11]. With the availability of more advanced battery technologies, utilities are deploying more distributed batteries (several MWs) at the substation level for peak load management and reliability improvement [1]. It was estimated that storage systems can help defer capacity upgrades of utility substations for two to three years to accommodate short-term localized growth [8]. In the electromobility sector, EVs are becoming competitive when compared with equivalent ICE versions. In a decade, the EVs will have an important role in the provision of grid services through the vehicle-to-grid (V2G) concept [18–20]. Nowadays, the V2G operation can significantly affect the state of health (SOH) of the lithium batteries due to cycling operation [21]. In the future, with the expected price drop of the batteries and further advancements in the cell materials, a full range of V2G services become possible by the aggregation of EV fleets [17]. Several pilot projects have been exploring the V2G concept. For example, BMW and California-based utility provider PG&E successfully tested demand response charging of EVs for load shifting during high usage times of day [22]. The Parker project join the automotive manufactures Nissan, Mitsubishi,

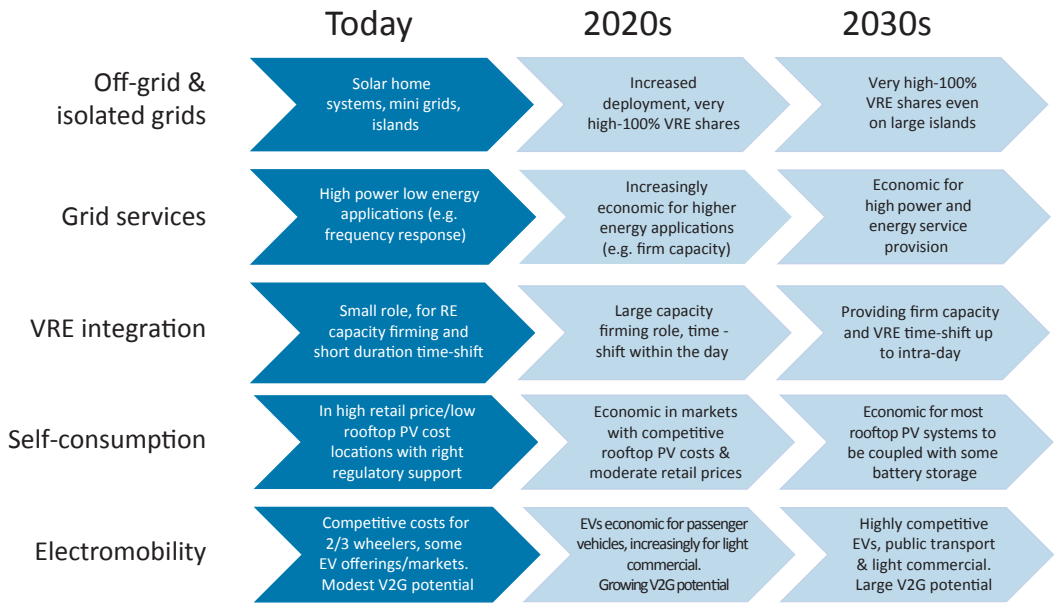


Figure 1.4: Potential contribution of the BESS in the energy transition by sector [17].

and Groupe PSA, the energy company Enel, and the technology provider Nuvve to validate that series-produced electric vehicles as part of an operational vehicle fleet which can support the power grid by becoming a vertically integrated resource [23].

1.1.2 Community Energy Storage

The energy storage needs to follow the generation move towards the new paradigm based on distributed energy resources (DER). Inserting energy storage systems in the low voltage (LV) grid, and in the proximity of the *prosumers*, increases the global value of the storage solution [24]. Due to the proximity with the customers, this system is commonly named Community Energy Storage (CES) [25]. Figure 1.5 shows an integration example of a CES unit in the low voltage distribution grid and near the customers. This EES system location is defined in IEC 62933-5-1 standard as 'residential including group of households' [26]. Based on the reasons explained in section 1.1.1, the application of batteries seems to be the more promising technology for these systems, enabling both energy and power capabilities [11].

Economics of storage will be a major driver of how quickly distributed storage solutions are adopted in electricity grids [27]. The economic value of the storage devices is directly related to the difference between on-peak and off-peak power price, since it makes possible to do electric energy price arbitrage [8, 28]. If services are added to CES, then the solution could become even more cost beneficial and make it largely adopted. A recent report from Mckinsey & Company [29] has shown the economic value of BESS for utility and customer applications. Figure 1.6 represent the economic value of the battery storage for utility and

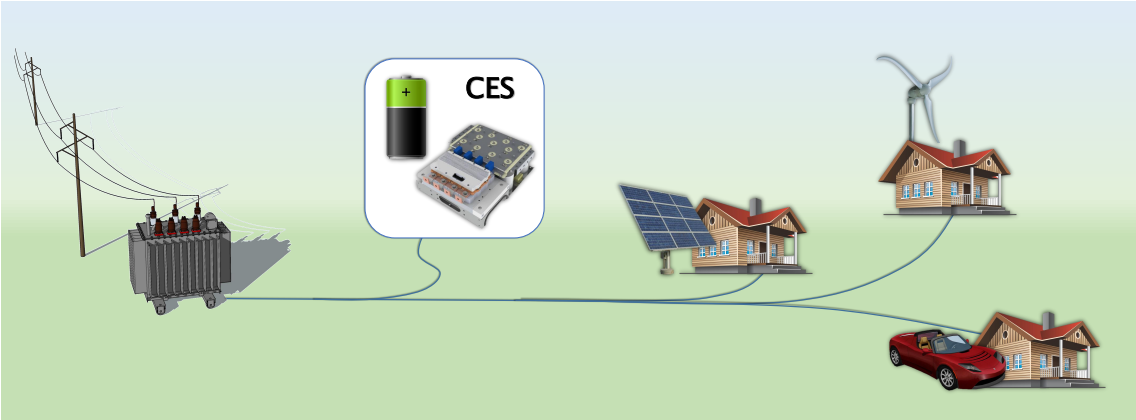


Figure 1.5: Integration of the community energy storage unit inside low voltage distribution grid.

customer applications. In 2020, the renewable energy technology firming and smoothing will play an important role for the utility along with the capability to contribute for frequency regulation. At the customer and business level, the reduction in demand charge and the increase of solar self-consumption will provide the highest economic value. This presents a risk for the grid operation, since the customers choose to stay connected to the grid in order to have access to 24/7 reliability, but generate 80 to 90 % of their own energy by incorporating CES systems [29]. Therefore, there will be fewer bill payors to cover the fixed investment in the grid, which still provides backup reliability for the solar customers. The solar customers are paying for their own energy but not paying for the full reliability of being connected to the grid [29].

1.1.3 Functionalities and benefits of CES

Locating storage near loads and distributed generation (DG) opens up opportunities to use this storage for many more applications than the bulk storage resources could address [27]. CES can offer a wide range of functionalities and ancillary services for the grid operator, allowing simultaneously the increase of flexibility and reliability of the network [1, 2, 11, 27, 29]. The operation of several CES units as a fleet, controlled from a central location, can provide the same benefits of a MW scale substation battery [24, 30]. Aggregation of CES units, through advanced metering infrastructure (AMI), will enable the grid operator to participate in the electricity market and dispatch the energy more efficiently [8, 31].

In terms of energy storage, the CES can operate as an energy source in a daily cycle base. This type of operation takes place for long periods and uses a significant part of total stored energy. CES can store energy in periods of low demand, and release it at high demand periods, implementing in this way peak shaving and peak shifting functionalities [32]. The peak shaving consists in the reduction of the total energy amount that is provided by utility at peak load demand periods, taking advantage of the energy storage capacity of CES. This reduces peak demand in LV electric power grids, and allows

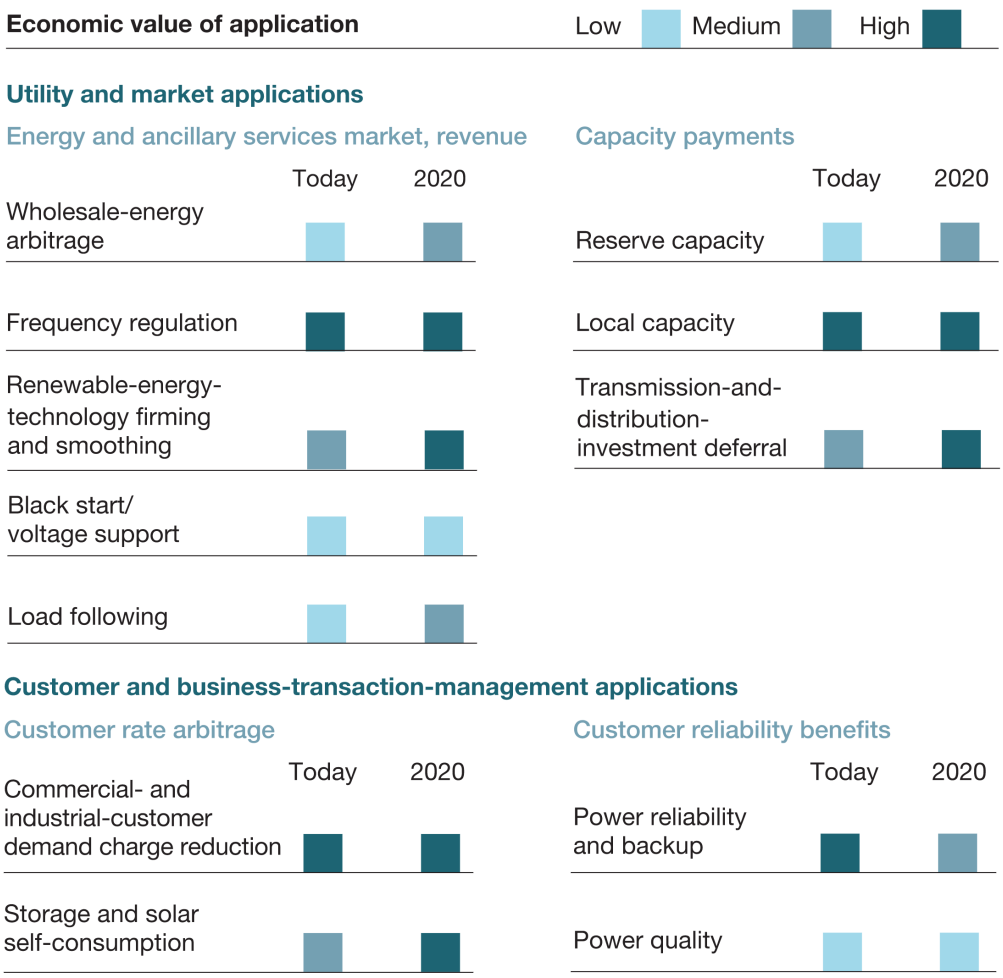


Figure 1.6: Battery storage economic value for utility and customer applications [29].

grid operators to offset a growing cost for generating extra power to meet very short period of demand [4, 5, 25]. Peak shifting has a very similar definition and is also know as load leveling. Since the peak of photovoltaic generation precedes the customer load peak by two to three hours each work day, the CES can store and shift the same amount of demand from the generation to be consumed later when the load grows [1, 4, 25]. By shifting load from peak to base load periods, the CES can help the grid operator to reduce the maximum currents flowing from the transmission and distribution grid through constrained utility infrastructure. This allows the grid operator to defer investment into upgrading their network capacity, being this one of the richest opportunities for distributed energy storage since the benefit can be very high [11, 27]. Moreover, since the CES is located very close to the loads, this would allow that excess energy be captured locally with less line losses and send back to the same customers when needed [1]. Then, power losses during transmission are greatly reduced and the system efficiency is improved [28]. Therefore, the effectiveness of energy storage operation with CES is much higher than other methods [25].

CES can also be a solution to the variability in the amount of renewable energy generation and uncertainty in the generation time [25]. This system can act as a buffer and smooth RES intermittency by absorbing and delivering power to limit fluctuations of feed-in electricity in the low voltage grid [11, 33]. In certain moments, when the power consumed in a LV grid is lower than the power produced by local DGs, a reverse flow occurs to medium voltage (MV) through distribution transformer. This can rise voltage above the limits, principally in rural grids due to longer cables, and overload equipment if the power flow exceeds the capacity of the transformer or the lines [4]. The presence of CES in these LV grids can store the excess of produced DG energy and avoid the technical operation issues provoked by the reverse power flow. Moreover, the CES can dynamic mitigate the neutral current and neutral voltage rise problems created by varying load and PV unbalance in LV networks [34]. Therefore, the hosting capacity of the distribution grids is increased allowing the integration of even more distributed power generation [35].

In terms of power storage, the CES can operate as a power source using the maximum available power rating and with a faster response. This type of operation takes place for short periods and uses a small energy amount of total stored energy. Voltage support is an important functionality that can be provided by CES in order to maintain the voltage within a defined range, with the aim to guarantee standard of supply [4, 11]. The lower voltages can be provoked by momentary loss of microgeneration due to variations in climatic conditions. Another concern is related to the expected appearance of heavy loads, such as electric vehicle battery chargers, that will stress the network [36]. Such loads can originate an unpredictable power unbalance during short periods that affect feeder voltage. In island operation mode, the frequency may also be affected and should be regulated [37]. Due to its high ramp-up response, the CES can locally provide a momentary power boost to compensate the power unbalance. This primary control may be implemented in the storage unit for load sharing among others controllable and dispatchable fast-response DER units in that area [37]. Further, secondary control should correct the voltage and frequency deviation caused by primary control.

Other additional features may also be provided by the CES to improve electric service reliability and power quality [8, 27]. CES can take advantage of its physical location and advanced technology to provide significant benefit with limited charging/discharging and relatively short discharge durations (from seconds to couple of minutes) [27]. Seeing that CES has energy stored in its batteries, during charging or in standby mode this unit can also provide spinning reserve capacity for the grid operator [25]. Active power filtering is another feature that could be implemented to perform power factor correction and harmonic filtering [38]. The power electronic converter used in this system has the ability to act as instantaneous capacitive or inductive VAR compensator to correct the power factor and reduce the cable power losses [39]. This feature is a concurrent objective faced to the voltage support discussed above, because the two depend on the reactive current. However, the control algorithm can be configured in order to allow both features

to operate in a weighted form [40]. Another interesting feature is the harmonic filtering due to proliferation of non-linear loads which increases non-sinusoidal currents that flow into the power grid [41]. In a weak LV network, the grid voltage could be seriously affected by these currents, and therefore the CES can be a solution for this problem without significant additional cost.

Due to its closeness to the customer, the CES can act as an UPS when the grid is under fault or maintenance modes. In this case, the storage units combined with the load and the distributed generation forms a microgrid, which permits the operation in island mode until the power be restored [42]. In this way, CES allow for increased power safety and reliability in areas with weaker low voltage grid [27].

1.1.4 Reference pilot projects of CES

There are several pilot projects of community energy storage currently in the field. The Department of Energy of United States has an up-to-date database of global energy storage projects [43]. Table 1.2 shows a very short list of some operational CES pilot projects. It is important to point that both energy and power functionalities have been explored by these systems. It is important to stress that part of this Ph.D. research work was integrated and developed within the framework of the European research project SENSIBLE - Storage-Enabled Sustainable Energy for Buildings and Communities (Grant Agreement 645963).

1.2 Power Conversion System

A modern storage unit for utility grid connection can be split in three primary components [44]: storage medium, power conversion system (PCS), and balance of plant. Figure 1.7 depicts the block diagram of a typical grid-connected Energy Storage System specified by IEEE 2030.2-2015 standard. For the present work, the storage medium is assumed to be based on batteries, since it seems to be the most promising technology for the BESS [11, 25]. The balance of plant includes all the devices that are used to support the equipment, including communications, monitoring and control. This component will only be briefly addressed in section 4.3 regarding the P-Q control functionality. Further details about this topic are available in IEEE 2030.2-2015 standard [44]. This thesis is focused on the energy conversion module that consists in a bidirectional power conversion system. The main requirements and features that must be provided by the PCS are discussed in section 1.2.1. Then, a revision of the essential applicable standards is presented in section 1.2.2. Finally, the resulting specifications are listed in section 1.2.3 in order to guide the project of the PCS.

Table 1.2: List of some reference pilot projects of community energy storage [43].

Location	Functionalities	kW/kWh	Battery	Owner	Manufacturer
Irvine, USA	microgrid capability, energy time shift, resiliency	250 / 1500	Lithium-Ion	Irvine Company	Dynapower, Tesla
Ohio, USA	backup power, voltage support, renewables capacity firming	25 / 25	Lithium-Ion	AEP Ohio	S&C Electric
Michigan, USA	grid upgrade deferral, energy time shift	25 / 50	Lithium-Ion	General Motors	LG Chemical, ABB
Ontario, Canada	energy time shift, reliability, renewables capacity firming, resiliency	150 / 300	Lithium-Ion	Oshawa Power	Tabuchi Electric
Évora, Portugal	voltage support, reliability, energy time shift, renewables capacity firming, UPS	10 / 40	Lithium NCA	EDP Distribuição	GTE Seville University, INESC TEC
Évora, Portugal	voltage support, energy time shift, renewables capacity firming	3.3 / 9.2	Lead-acid VRLA	EDP Distribuição	INESC TEC
Côte d'Azur, France	grid upgrade deferral, renewables capacity firming, energy time shift	33 / 85	Lithium-Ion	ERDF	SOCOMEC, SAFT
L'Aquila, Italy	voltage support, power factor correction, load leveling	32 / 32	Lithium-Ion	ENEL	Samsung SDI, Loccioni Group
Berkshire, United Kingdom	renewables capacity firming, energy time shift, grid upgrade deferral	50 / 100	Lithium-Ion	Northern Powergrid	ABB, NEC
Island Pellworm, Germany	electric supply capacity, renewables capacity firming, energy time shift	200 / 1600	Vanadium Redox Flow Battery	Northern Powergrid	Gildemeister, DMG Mori Seiki
Falkoping, Sweden	grid upgrade deferral, electric supply capacity, renewables capacity firming	75 / 75	Lithium-Ion	Falbygden Energi	ABB
Shanghai, China	frequency regulation	50 / 50	Lithium Iron Phosphate	-	BYD

1.2.1 Requirements and Features

Within the concept of community energy storage, some design constraints should be addressed in order to implement an effective solution for the market. Regarding the PCS, reliability and maintenance issues are critical, since this kind of storage systems are intended to be installed in remote locations, especially outdoor or in the distribution transformer rooms. If the maintenance intervals can match the ones used for the existing equipment (several months to few years), the operational costs of the system can be significantly reduced. These requirements can be fulfilled avoiding the use of components which performance depends strongly on environmental conditions (temperature, humidity, etc.) and the running time of the converter. Currently, the two main components of a PCS with such problems are the electrolytic capacitors and the active cooling systems (forced air or liquid).

Passive cooling represents typically a significant part of the volume and also the weight

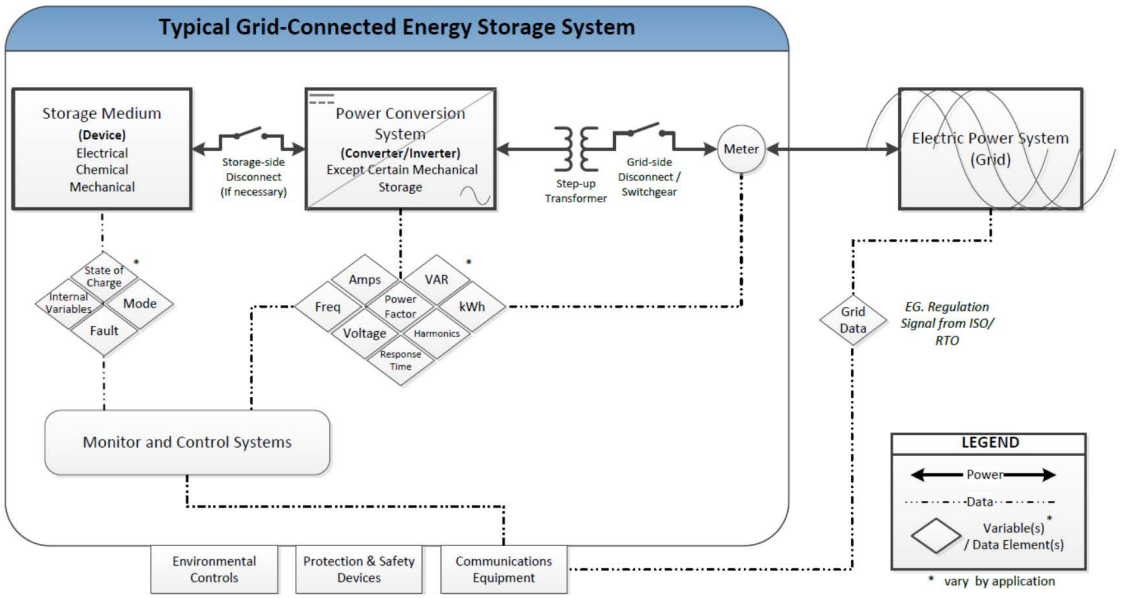


Figure 1.7: Block diagram of a typical grid-connected Energy Storage System specified by IEEE 2030.2-2015 standard. [44].

of the converter, which makes this cooling technique reasonable only for converters with low losses. For an outdoor installation it is also desirable for the system to be hermetic, which is another limitation for the power losses since all the heat must be conducted through the enclosure. For indoor installations the hermetic characteristic is less critical, and it is also desirable since it makes the converter much more immune to external physical interactions.

In the grid interface, the power quality requirements are well defined on international standards, as described in the section 1.2.2. For batteries, these requirements should come from the battery supplier, since it is related to many aspects such as cell technology, capacity, temperature, etc. In any case, waveforms with low ripple and low harmonic content are always desirable since they ensure that the capacitors and the inductors operate with low temperatures, which results in a significant increase in service life.

Safety is always a major concern for equipment, specially when it is installed close to residential areas. If the voltage level for the battery bank is under 50 volts it is widely accepted that the human safety is ensured, and the work performed may usually be considered to be de-energized work [45]. Therefore, installation and maintenance are also benefited with this voltage limit, because they can be made in energized circuits, without major safety concern. If the system is also galvanically isolated and double-grounded, one can say that there is no risk of exposure to dangerous potentials.

Together with the electrical features discussed previously, other physical constraints like weight and volume must be discussed. They are not as critical as electric vehicle on-board chargers for example, but a large size and weight will result in a cost increase for

the transportation, handling and installation of the equipment. For the installation in the distribution transformer rooms, a reasonable power density is necessary to ensure that the CES doesn't exceed the effective available volume. In order to provide galvanic isolation to the converter, prevent dc current injection to the grid and perform some voltage level adaptation between grid and batteries, a power transformer should be employed. The use of a low frequency transformer is typically a major penalty to reach low weight and volume designs. Thus, a demand for high frequency isolation techniques should be made if the low weight and volume are pursued [46].

Due to the limited available space, the energy storage technology used in this edge-of-grid application could take advantage of higher power density battery technology commonly used in electric vehicles [25]. A possible synergy with automotive industry is envisioned as leverage for strong CES development and adoption. Used electric vehicle battery packs could be reassembled to obtain a second-life in distributed energy storage applications [47, 48]. This cooperation can offer a low-cost, compact and high-reliable battery for CES, and simultaneously avoid recycling cost for the vehicle owner or manufacturer (in case of leasing battery pack) [24].

1.2.2 Standards

The storage systems are connected to the electric power grid so they must meet applicable interconnection requirements. The IEEE 1547 is the most relevant existing standard applicable to energy storage systems interconnected to electric power grid [49]. It is a result of an effort by the IEEE SCC21 committee to develop a single interconnection standard that applies to all DER [50]. The interconnection requirements related to synchronization, power quality (harmonics, dc injection, etc.) and unintentional islanding are specified in this standard. The current total harmonic distortion (THD) shall not exceed a limit of 5 %. In terms of dc current injection, the system shall not exceed 0.5 % of the full rated output current at the point connection [51]. Moreover, according to [52] the storage units must always generate symmetrical, three-phase rotary currents. The approaches for intentional islanding operation were further defined in IEEE 1547.4, where the separation and reconnection with the distribution grid was established [53]. In order to the CES act as an UPS, the operation in island mode is required to continuously supply the load demand and absorb energy from a local distributed generation. Anyway, in the close future, the operation in island mode may not be allowed by specific countries legislation. Therefore, an automatic disconnection device should ensure that the CES is separated from the grid to prevent unintentional island. Currently, PV systems have this requirement, specified in standards as VDE 0126-1-1, IEC 61727 or IEEE 1547. Other disconnection requirements in case of frequency or voltage deviation are also specified in these standards.

The IEEE 2030 series of standards is helping to further realize greater implementation of communications and information technologies that provide interoperability solutions for

enhanced integration of DER and loads with the grid [54]. In particular, the IEEE 2030-2011 defines the smart grid interoperability reference model (SGIRM) that organizes all the functions and interconnections of a Smart Grid in terms of three separate interoperability architecture perspectives (IAPs): power system, communications, and information technology [55]. It is intended to present interoperable design and implementation alternatives for systems that facilitate data exchange between smart grid elements, loads, and end-use applications. The communications technology perspective of the SGIRM supports a broad set of networks. Figure 1.8 provides a graphical view of the relationship of various networks to the smart grid bulk generation, transmission, distribution, and customer domains. Even though the public Internet may not be commonly used, the IEEE 2030 SGIRM allows use of the public Internet [55].

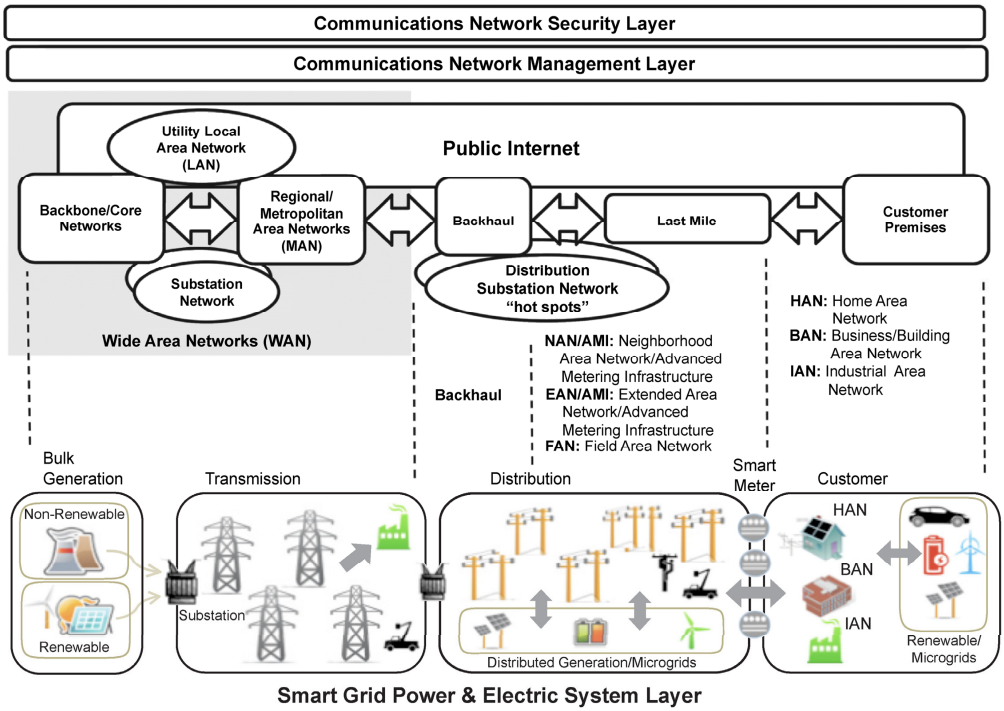


Figure 1.8: End-to-end smart grid communications model specified by IEEE 2030-2011 standard [55].

The IEEE 2030.2-2015 was specifically developed to address the interoperability of energy storage systems (ESS) with electric power infrastructure. It is applicable to ESS applications located on customer premises, at the distribution level, and on the transmission level (i.e., bulk storage) [44]. The standard protection practices for an BESS are also listed in IEEE 2030.2 and typically consists of overcurrent/short-circuit protection, frequency deviation protection, undervoltage/overvoltage protection, and anti-islanding protection. The test procedures of electric energy storage equipment and systems are defined by the IEEE 2030.3-2016 standard [56]. Testing items and procedures, including

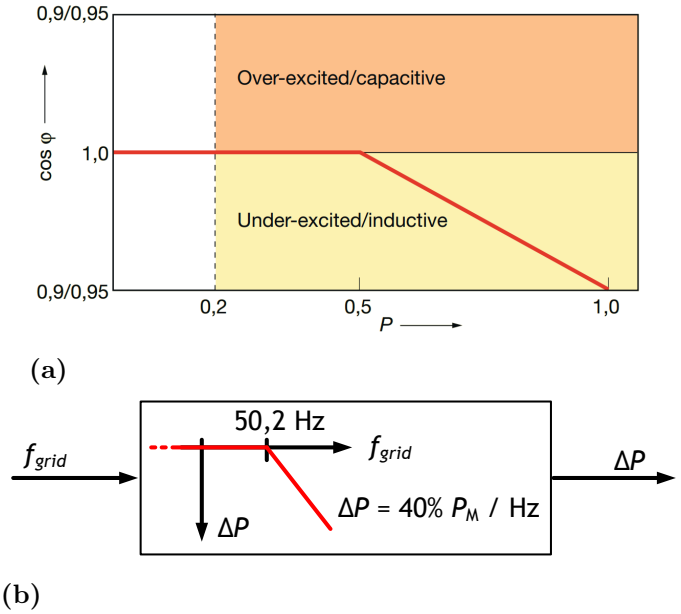


Figure 1.9: Some requirements from VDE-AR-N 4105. (a) Reactive power curve. (b) Frequency-dependent active power control.

type test, production test, installation evaluation, commissioning test at site, and periodic test, are provided in order to verify whether ESS applied in electric power systems (EPSs) meet the safety and reliability requirements. The type test is mainly used to verify the design principle and ratings of the ESS. The following are examples of type tests defined by the IEEE 2030.3-2016 standard: state of charge test, energy conversion efficiency test, discharging response time, charging response time, synchronization test, reconnection after abnormal condition test, open-phase test, overcurrent test, DC injection test, unintentional islanding test, and low-voltage ride through (LVRT) test.

Recently, the technical requirements for the connection of the generators to the LV distribution network were updated in Germany, through the application guide VDE-AR-N 4105. Generators feeding into the low-voltage distribution network have to be involved in maintaining static voltage stability by providing reactive power, according to the curve represented in Fig. 1.9(a). The generators also need to stay connected during frequency deviations, in order to guarantee the stability of the power system [57]. Particularly, the VDE application rule specifies a frequency-dependent active power control as represented in Fig. 1.9(b). The generator should reduce the active power in the event of overfrequency instead of automatic disconnect from the grid, solving for example the "50.2 Hz problem" [4].

A technical information namely "Connecting and operating storage units in low voltage networks" was also published by VDE (FNN) [52]. It specifies that the storage unit should implement the requirements depicted in Fig. 1.9 during "Energy supply" (discharge) mode. No reactive power should be provided in "Energy consumption" (charge) mode, so $cos\varphi = 1$ applies. CES design should take this into account and leverage their

Table 1.3: List of standards applicable to the power conversion system for CE mark.

Electromagnetic Compatibility - Directive 2014/30/EU
• IEC 61000-6-3:2011 - Emission standard for residential, commercial and light-industrial environments environments • CISPR 11:2015 - Radio-frequency disturbance characteristics - Limits and methods of measurement • IEC 61000-3-2:2014 - Limits for harmonic current emissions ($\leq$16 A) • IEC 61000-3-3:2013 - Limitation of voltage changes, voltage fluctuations and flicker in public low-voltage supply systems ($\leq$16 A) • IEC 61000-6-1:2016 - Immunity standard for residential, commercial and light-industrial environments • IEC 61000-4-2:2008 - Electrostatic discharge immunity test • IEC 61000-4-3:2006 - Radiated, radio-frequency, electromagnetic field immunity test • IEC 61000-4-4:2012 - Electrical fast transient/burst immunity test • IEC 61000-4-5:2014 - Surge immunity test • IEC 61000-4-6:2013 - Immunity to conducted disturbances, induced by radio-frequency fields • IEC 61000-4-8:2009 - Power frequency magnetic field immunity test • IEC 61000-4-11:2004 - Voltage dips, short interruptions and voltage variations immunity tests

potential to guarantee safety and reliability in the power system operation.

The International Electrotechnical Commission (IEC) considers that the energy storage is a major element of Smart Grid [58]. Following this conviction, IEC created the TC-120 committee – Electrical Energy Storage (EES) Systems – to develop the necessary efforts to the standardization in the field of grid EES systems. Some standards are already concluded. For example, IEC 62933-5-1:2017 specifies safety considerations applicable to EES systems integrated with the electrical grid [26]. Other standards are still in development, such as the IEC 62933-3-1 and the IEC 62933-5-2.

Special attention must be paid regarding the electromagnetic interference in order to ensure compliance with the EMI standards [59]. Table 1.3 has a list of standards that must be taken in account to issue the CE mark declaration. These standards can be split in two types according if are related with emission or immunity of the system.

1.2.3 Specifications

Considering the applicable standards and the requirements discussed in the previous section, it was possible to establish the same requirements and specifications for the power conversion system. Within this thesis, it is intended to build and demonstrate a TRL 4 prototype of a PCS for a CES system. Table 1.4 has a list of the main specifications and requirements to be implemented.

Table 1.4: Specifications and requirements for the power conversion system.

Property	**Value**
Line-to-line voltage ($V_{AC,ll,nom}$)	$3 \times 400\ V_{rms}\ \pm\ 10\ \%$
Input frequency (f_i)	50 Hz
Battery voltage (V_{batt})	380 V (320 to 490 V)
Output power (P_{nom})	$\pm$ 10 kW
Switching frequency (f_s)	20 kHz
AC current ($I_{AC,P,nom}$)	$3 \times 15\ A_{rms}$
Nominal charging current ($I_{batt,nom}$)	26 A
Maximum charging current ($I_{batt,max}$)	31 A
Battery current ripple (I_{batt_ripple})	$\leq$ 5 % (40 to 100 % $I_{batt,nom}$)
Power factor (PF)	$>$ 0.9 (40 to 100 % $I_{AC,P,nom}$)
Total Harmonic Distortion (THD)	$\leq$ 5 % (40 to 100 % $I_{AC,P,nom}$)
Efficiency (η)	$>$ 95 % (50 to 100 %P_{nom})
Additional requirements	
• Bidirectional power flow • Galvanic isolation • P - Q control • DC voltage and current control • Battery connection according to battery manufacturer	

1.3 Research Goals

As previously discussed in Section 1.2, a bidirectional and isolated PCS to make the interface of the batteries with the electric power grid is required. In this way, the main focus of this work is in the advancement of the power conversion system to provide the necessary functionalities. A deep review of DC-DC and AC-DC conversion topologies is presented in Chapter 2. From this analysis, it was concluded that the High-frequency Link Matrix Converter (HFLMC) has important features that can be explored in the CES, such as the inherit bidirectional power flow, and the single-stage power conversion architecture that avoids the conventional DC-link. Figure 1.10 shows the power electronics topology of the HFLMC that is the scope of this research.

From the state of the art review presented in Section 2.6, it was concluded the available modulations for the HFLMC were not able to provide the required control functionalities for the CES. In this way, the development of a new modulation for this topology that allows to fulfill simultaneously the requirements on the grid side and from the batteries is one of the main objectives of this research. The provision of advanced functionalities to support the grid operation is also a topic for investigation. Experimental demonstration of the proposed power conversion system is one of the main outcomes of this thesis.

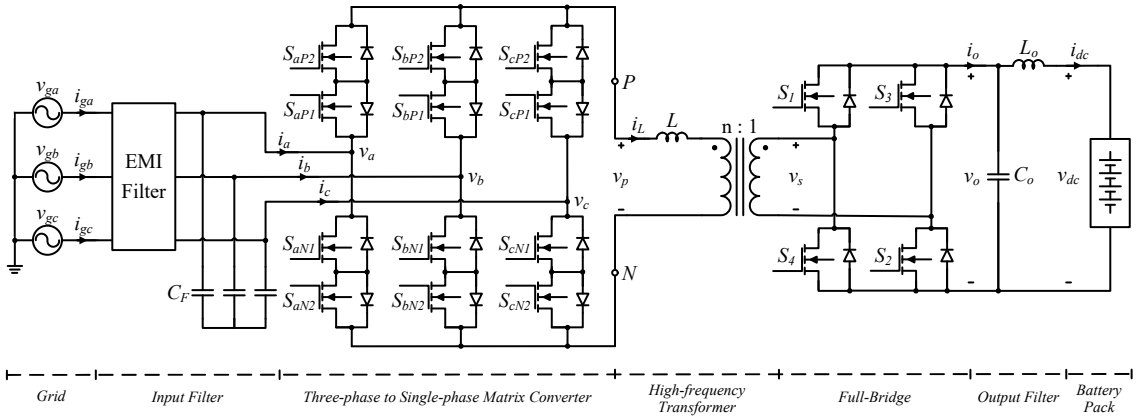


Figure 1.10: Circuit schematic of the high-frequency link matrix converter (HFLMC).

The introduction of energy storage in the low voltage distribution grid can provide several benefits and advanced services for the network operation. The advancement of new solutions for the power conversion system of the CES unit is an actual and challenging research topic. The development of a new modulation and control strategies for the HFLMC topology is by far the core of this work. Considering the requirements and features to be implemented in the CES unit, and focusing on the power conversion system development, the general objective of this thesis was defined as:

> *Investigate if and how the high-frequency link matrix converter (HFLMC) can be used as the power conversion system (PCS) for community energy storage (CES), complying with the grid interconnection requirements and also with the requirements for the batteries, targeting to obtain a higher power density than conventional solutions while keeping the same reliability.*

Based on this general objective, three main research questions have been formulated:

RQ 1 *Is it possible to create a new modulation to operate the HFLMC with sufficient low losses and high switching frequency that allows to reduce the volume of the heat sink and passive components, resulting in high power density solution for the PCS?*

RQ 2 *Could this new modulation allow to control simultaneously the active and reactive power in the grid and the current in the batteries, complying with the respective requirements imposed by the grid interconnection and the batteries operation?*

RQ 3 *Is it possible to formulate a P-Q controller for the HFLMC to allow the CES unit to be involved in maintaining static voltage stability by proving reactive power, and to keep connected during frequency deviations in order to contribute for the stability of the power system?*

1.4 Contributions

This research focused on different areas of power electronics: compliance with electromagnetic compatibility standards and respective filter design, optimized project of magnetic components, project of gate drivers for fast switching of SiC MOSFETs, implementation of commutation strategies for the bidirectional switches of the MC, development of controllers with the respective signal acquisition circuits for precise measurement of voltages and currents, simulation and experimental validation.

In order to provide the HFLMC topology with the necessary control functionalities for a CES system, a new modulation was invented as documented in Chapter 4. A comprehensive explanation of the modulation principle is supported with several figures and diagrams. A detailed deduction of the duty-cycles along with the resulting average currents at the grid side and the battery side is also provided in Appendix A. A controller for the grid currents was formulated in the synchronous reference frame for decoupled grid current regulation. By adding an external control layer, it is also possible to perform P-Q control. The voltage and current in the battery pack can also be regulated by a different controller that sets the references for the active and reactive component of the grid currents. A simulation framework was implemented in the GeckoCIRCUITS software including thermal modeling, conducted emission measurement, magnetic coupling, and loss model of the MOSFETs and other components. Then, extensive simulations were performed to validate the modulation, the different controllers, the EMI filter effectiveness, the magnetic components, and the cooling system.

An international patent application was submitted in order to protect the intellectual property associated to this research [60]. The claimed subject matter is mainly associated with the proposed modulation and the respective controllers to properly manage the interface with the battery pack and the grid. The patent was already granted in the United States with the reference US 9,973,107 B2. The examiner attested the novelty, usefulness, and non-obviousness of this technology. The regional processes are still ongoing in other places including Europe (EP 3180849 A1) and Japan (JP 2017528102 A). This technology was named 'ACDC CUBE' by INESC TEC and has the reference number 14-02022. The Technology Licensing Office of INESC TEC is currently developing efforts to license the technology for the industry.

An EMI filter was designed to ensure that the PCS is compliant with the CISPR 11 Class B standard. A step-by-step design process was established and systematized for the HFLMC that can be extended to other current source converters. Conducted emissions are estimated through extended simulation and take into account the effect of the measurement apparatus. Since the input of the converter is symmetric, differential-mode and common-mode filtering stages are projected separately and then integrated in a synergistic way in order to reduce volume and weight. A prototype of the filter was constructed and tested in the SGEV laboratory. Experimental results with the characterization of the insertion

losses and the attenuation capability following the CISPR 17 standard are provided. The implementation of this testbench for the experimental characterization of the filter is an important contribution of this thesis, since it provides the accumulated experience and the baluns for further testes at the SGEV laboratory of INESC TEC.

A functional prototype was developed to test and validate the modulation and the respective controllers proposed for the HFLMC. The circuits for accurate measurement of voltages and currents at the grid and battery side were designed to ensure a proper isolation and measurement range. Then, additional conditioning circuits to adapt the signal to the ADCs of the DSP were implemented. With the information provided by the sensors, the control algorithms are executed by the DSP that calculates the required duty-cycles and phase-shift. Due to the complexity associated with the modulation, it was necessary to add a FPGA to implement the commutation strategy for the bidirectional switches of the MC. A comprehensive review about the commutation strategies for the MC is provided in Section 3.4. The VHDL source code of the Variable-step VBC strategy embedded in the FPGA is reproduced in Appendix C and can be used in further developments at the SGEV laboratory. This control system based on DSP plus FPGA was developed from the ground up, and constitutes an important output of this thesis. The command signals for the 16 SiC MOSFETs are sent to the gate drivers which in turn are responsible for providing the appropriate current to turn-on and turn-off the power switches. The gate driver circuit includes short-circuit protection, a Miller Clamp circuit, under voltage lockout (UVLO) protection, and a current buffer for fast switching. This gate driver circuit is another important output of this research work, since the Silicon Carbide semiconductors are now replacing the Si technology in several power electronics converters. Each bidirectional switch is formed by two SiC MOSFETS mounted aligned side-by-side on the heatsink. This approach was effective in the minimization of the loop parasitic inductance and reduction of the PCB footprint area of the MC. This approach is documented in Chapter 6 and Appendix H and constitutes other relevant contribution of this thesis. The methodology to design the magnetic devices using analytic and software tools is described in Appendix E. The implementation of the power transformer and the link-inductor using this methodology is also detailed. The complete assembly of all parts described above resulted in a TRL 4 functional prototype presented in Chapter 6.

Several experimental tests were performed to validate the different control layers that run from the ns up to the ms time frame. It was demonstrated the capability to commutate the current in the bidirectional switches of the MC in a safe and reliable way using the variable VBC strategy. To the best of my knowledge, this is the first three-phase MC to be implemented and successfully operated at FEUP and INESC TEC, after a single-phase version had been tested in 2012 [61]. The high quality of the impressed grid currents was verified through the measurement of the harmonics, which are in compliance with the IEC 61000-3-2 standard. Decoupled control of the grid currents in the dq reference frame is possible and was well demonstrated in Chapter 4 and Chapter 6. Above this internal

control layer, other controllers were proposed and tested such as: the battery voltage and current controllers and the PQ controller. A journal paper was published with the description of the proposed modulation and the respective experimental demonstration using the developed prototype [62].

Within the scope of this research and also as a result of my participation on national and international projects at INESC TEC, the following papers and patent were published:
PATENT

1. D. Varajão, L. M. Miranda, and R. E. Araujo, "AC/DC Converter with Three To Single Phase Matrix Converter, Full-Bridge AC/DC Converter and HF Transformer," Granted Patent USA US 9,973,107 B2, Pending Patent Europe EP 3180849 A1, Pending Patent Japan JP 2017528102 A, International Patent Application (PCT) WO 2016024223 A1, 18 February 2016 [Priority Date: 13 August 2014].

JOURNAL PAPERS

2. D. Varajão, R. E. Araújo, L. M. Miranda, and J. P. Lopes, "Modulation Strategy for a Single-stage Bidirectional and Isolated AC-DC Matrix Converter for Energy Storage Systems," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 4, pp. 3458-3468, April 2018.

3. D. Varajão, R. E. Araújo, L. M. Miranda, J. P. Lopes, and N. D. Weise, "Control of an Isolated Single-Phase Bidirectional AC-DC Matrix Converter for V2G applications," in *Electric Power Systems Research*, vol. 149, pp. 19-29, Aug. 2017.

4. C. Gouveia, C. L. Moreira, J. A. P. Lopes, D. Varajão and R. E. Araujo, "Microgrid Service Restoration: The Role of Plugged-in Electric Vehicles," in *IEEE Industrial Electronics Magazine*, vol. 7, no. 4, pp. 26-41, Dec. 2013.

CONFERENCE PAPERS

5. D. Varajão, L. M. Miranda, R. E. Araújo and J. P. Lopes, "Power Transformer for a Single-stage Bidirectional and Isolated AC-DC Matrix Converter for Energy Storage Systems," *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, Florence, 2016, pp. 1149-1155.

6. D. Varajão, L. M. Miranda and R. E. Araújo, "Towards a new technological solution for Community Energy Storage," *EPE 2014 - 16th European Conference on Power Electronics and Applications*, Lappeenranta, 2014, pp. 1-10.

7. L. M. Miranda, D. Varajão, B. dos Santos, R. E. Araújo, C. L. Moreira and J. A. P. Lopes, "Power flow control with bidirectional dual active bridge battery charger in low-voltage microgrids," *EPE 2013 - 15th European Conference on Power Electronics and Applications*, Lille, 2013, pp. 1-10.

8. B. dos Santos, R. E. Araújo, D. Varajão and C. Pinto, "Rapid Prototyping Framework for Real-Time Control of Power Electronic Converters Using Simulink," *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*, Vienna, 2013, pp. 2303-2308.

9. D. Varajão, R. E. Araújo, C. Moreira and J. Peças Lopes, "Impact of phase-shift modulation on the performance of a single-stage bidirectional electric vehicle charger," *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, Montreal, QC, 2012, pp. 5215-5220.

1.5 Outline

This document is divided in two parts: *State of the Art* with two chapters, and the *Implemented Design* with four chapters and ten appendixes. The first part presents a detailed revision of the state of the art in terms of conversion topologies, paying special attention for the family of matrix converters. The second part, proposes a new modulation for the HFLMC and deals with all the implementation details for experimental validation. A further description of the contents available in each chapter is presented bellow.

Part I - State of the Art

Chapter 2, **Bidirectional and Isolated AC-DC Converters**, presents a revision of the main conversion topologies for the PCS. Voltage and current source converters are analysed and compared regarding their applicability for grid interface. A review of bidirectional DC-DC converters for voltage adaptation inside the PCS is also included. Finally, the combination of voltage and current source converters with the isolated and bidirectional DC-DC topologies is provided.

Chapter 3, **Review of Matrix Converters**, introduces the main topologies of matrix converters, namely the Direct Matrix Converter (DMC) and the Indirect Matrix Converter (IMC). An overview of the modulations proposed for these conversion topologies are presented with a special focus on the switching pattern generation in order to reduce the number of switching commutations. Implementation issues regarding the construction of the bidirectional switch is also discussed. Finally, a comprehensive revision of current-based and voltage-based commutation strategies is also presented in the end of the chapter.

Part II - Implemented Design

Chapter 4, **High-frequency Link Matrix Converter**, introduces the topology that is the subject of study and proposes a new modulation strategy. A detailed deduction of the main equations to define the voltages and currents in the grid side, battery side, and also in the HF-link is carried out. Active and reactive power control method at the

grid side, and voltage and current regulation at the battery side are also developed and validated through extensive simulations.

Chapter 5, **EMI Filter**, discusses the project of the differential-mode and common-mode filtering stages for CISPR 11 Class B pre-compliance. A systematization of the EMI filter design process with estimation of the conducted emissions by taking into account the effect of the measurement apparatus is presented. Then, an experimental characterization of the insertion losses and attenuation capability of the EMI filter following the CISPR 17 standard is performed.

Chapter 6, **Prototype and Experimental Results**, details the construction of the TRL 4 prototype and presents the experimental results obtained at the SGEV laboratory of INESC TEC. Despite being a complex conversion topology that requires a special commutation strategy, the feasibility for its application on battery-based applications was demonstrated, being this the main contribution of this chapter.

Chapter 7, **Conclusions and Future Work**, reports the final remarks and establish perspectives for future research work.

Appendix A, **Supplement to Chapter 4**, provides a detailed derivation of the average currents and the duty-cycles that result from the proposed modulation.

Appendix B, **Switching states of the Variable-step VBC**, the switching states for each normal and critical interval of the Variable-step VBC strategy are provided for each sector and the bidirectional switches S_{aX}, S_{bX}, and S_{cX}.

Appendix C, **Variable-step VBC strategy**, details the source code in VHDL for the Variable-step VBC strategy employed in the functional prototype.

Appendix D, **Four-step CBC strategy**, details the source code in VHDL for the Four-step CBC strategy described in Section 3.4.1.

Appendix E, **Power Transformer and Link-inductor**, details the high-frequency transformer and link inductor design process.

Appendix F, **DC Filter**, report the project of the DC filter that interfaces the battery pack in order to reduce the current ripple.

Appendix G, **Simulation Model**, shows the implementation details of the power circuit, the control algorithms, and the thermal circuit in GeckoCIRCUITS software.

Appendix H, **PCB Design**, shows the schematic, layout, and image of the PCBs designed for the functional prototype.

Appendix I, **Testbench at the SGEV Laboratory**, includes photos of the test-bench at the Smart Grids and Electric Vehicles laboratory of INESC TEC, along with a description of the infrastructure.

Appendix J, **HFLMC vs VSC-DAB**, presents an extensive comparison between the HFLMC and the traditional solution based on a VSC and a DAB.

Part I

State of the Art

Chapter 2

Bidirectional and Isolated AC-DC Converters

Power electronics is making profound changes from the transportation sector to the electric power system [63, 64]. The development of new wide bandgap power semiconductors [65] combined with enhanced modulations [66] and control techniques are contributing for the miniaturization and efficiency improvement of the power electronics converters.

Bidirectional AC-DC converters are required for several applications, such as BESS [64], chargers for electric vehicles (EVs) [67], UPS [46], solid-state transformers (SST) [68], and DC microgrids [69]. Each of these applications has different requirements and features for the PCS. However, galvanic isolation is relevant to ensure safety, prevent DC current injection to the grid and perform voltage level adaptation between the grid and the DC side [70].

As previously discussed in Section 1.2, a bidirectional PCS to make the interface of the batteries with the electric power grid is required. Several solutions have been proposed for the PCS of battery energy storage systems [64, 71–73]. Typically, the PCS is composed by an AC-DC converter to do the interface with the grid, and a DC-DC converter to manage the voltage and current at the battery pack. Through this thesis, the term "converter" is employed to highlight the bidirectional power flow capability, making a distinction from the "inverter" and "rectifier" topologies.

The control system synchronizes the AC-DC converter with the grid using a phase-locked loop (PLL) algorithm. By employing appropriate command strategies for the power semiconductors, the AC-DC converter modulates the grid currents with low THD and minimum common-mode (CM) voltage in order to reduce the electromagnetic interference (EMI). The AC-DC converter can be divided into voltage source and current source topologies, depending on the dc-link energy storage element. The current source converters (CSC) employ inductors in the dc circuit, whereas the voltage source converters (VSC) have capacitors in the dc-link. The later is used more often and therefore a large variety

of topologies is available. Section 2.1 and Section 2.2 present a list of possible topologies of VSC and CSC, respectively. It is important to stress that only 3-wire topologies are considered for this analysis because the PCS is intended to operate with balanced AC three-phase currents.

If the voltage range of the battery pack is not compatible with the DC-link voltage required for the AC-DC converter, a DC-DC conversion stage needs to be included in the PCS. The DC-DC stage can operate as boost or buck converter in order to adapt the different DC voltage levels inside the PCS. Additionally, the DC-DC converter is also responsible for the charging process of the battery through voltage and current regulation respecting the limits imposed by the BMS. A review of the bidirectional DC-DC converters is given in Section 2.3.

The combination of AC-DC and DC-DC stages allows to obtain several possible topologies for the isolated and bidirectional PCS. Conventional solutions based on the use of low-frequency transformer (LFT) are discussed in Section 2.4. Galvanic isolation can also be provided by incorporating the power transformer in the bidirectional DC-DC converter stage. A distinction between dual and single-stage AC-DC converters based on the high-frequency link (HFL) concept is represented in Fig. 2.1.

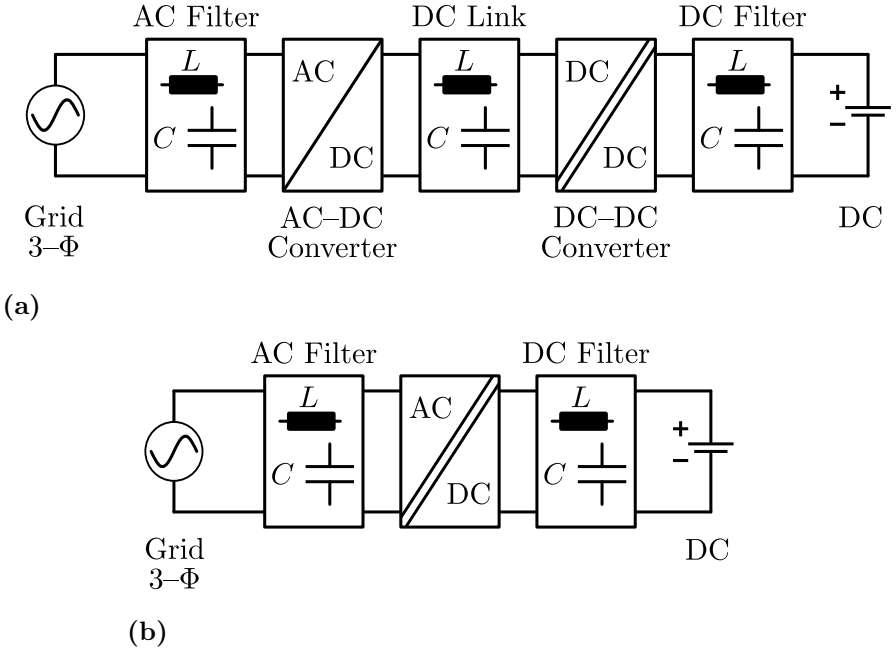


Figure 2.1: Block diagram of (a) Dual-stage AC-DC Converters with HFL and (b) Single-stage AC-DC Converters with HFL (adapted from [74]).

Dual-stage architectures have a DC-link energy storage element to decouple the AC-DC and DC-DC converters. As a result, both systems can be optimized independently within narrow specifications [74]. Contrarily to what happens in a single-phase system, the instantaneous power is perfectly constant in a symmetric three-phase power supply system. Thus, the DC current at the battery is also constant in single-stage converters.

As a result, they only require storage at the switching frequency which makes the filtering design easier. In single-stage architectures, the galvanic isolation is incorporated in the AC-DC converter. By removing one conversion stage and the DC-link energy storage element, they have the potential to improve efficiency and power density while reducing the number of components, weight and costs. The main disadvantage is that all functionalities are performed by a single conversion stage that consequently needs to be designed and optimized within wide specifications [74]. Diverse dual and single-stage converter topologies with high-frequency link are detailed in Section 2.5 and Section 2.6, respectively.

2.1 Voltage Source Converters

There are several possible topologies for the VSC. In low voltage grids, the two-level (2L) converter represented in Fig. 2.2 is widely used mainly due to its simplicity, reliability, and availability in integrated power modules which results in a cheap and compact solution with small footprint. This topology only requires six switches, and the corresponding modulation strategies are also simple and easy to implement in a microcontroller unit (MCU) [66]. However, the 2L VSC has limited power and voltage range and has relatively high switching losses [75].

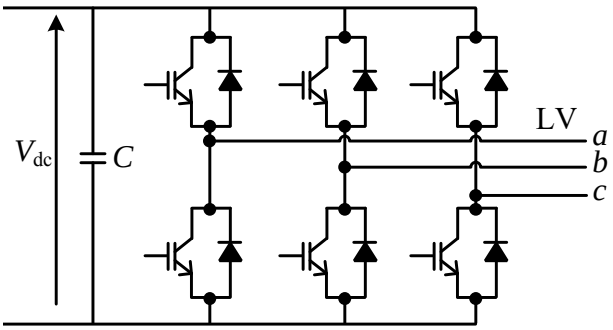


Figure 2.2: 2L VSC for LV grid applications (adapted from [76]).

The 2L VSC can be enhanced with an active, bidirectional switch connected to the dc-link midpoint, as illustrated in Fig. 2.3. The resulting topology is named T-type converter due to the format of each bridge leg. The connection to the dc-link midpoint enables the generation of AC voltages with three-levels. As a result, the voltage stress at the semiconductors is reduced while the output voltage quality improves significantly [77]. The bidirectional switch has to block only half of the dc-link voltage. Therefore, it can be implemented with power semiconductors having a lower voltage rating when compared with the high-side and low-side switches. As an example, for a dc-link with V_{dc}=700 V, the bidirectional switches can be rated at 600 V while the high-side and low-side switches need to be rated at 1000 V or 1200 V. The main benefit of the T-type converter comes from the switching losses reduction due to the commutation voltage of the 1200 V devices which is

only 350 V instead of 700 V in the two-level VSC. Regarding the practical implementation, only one additional isolated gate driver supply is necessary, when compared to the two-level topology, if the bidirectional switches are mounted in common-collector configuration. As experimentally demonstrated in [78], a motor drive with the T-type converter can reduce the harmonic machine losses approximately by a factor of 4 compared to standard 2-L VSC.

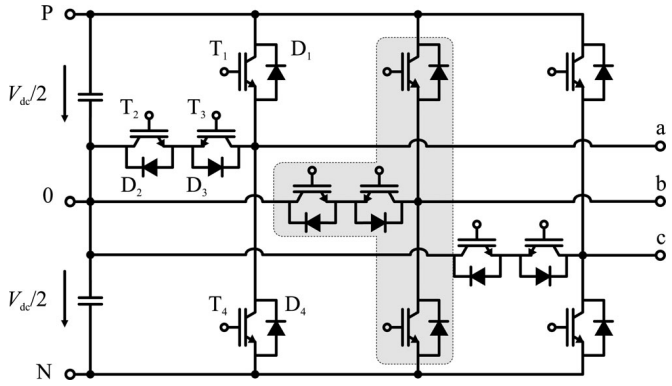


Figure 2.3: Three-level T-type converter (3L-T-type VSC). [77].

Equipment in the megawatt range is usually connected to the MV grid (6 kV to 30 kV). With the available technology, it is hard to connect a single power semiconductor switch directly to the MV grid. Despite some solutions start to be available in the market, its switching characteristics are much inferior when compared to, for example, a 1200 V SiC MOSFET. To overcome this difficulty, multiple switching devices are connected in series in the 2L VSC, as represented in Fig. 2.4. A specific design of the gate driver for the power semiconductors is necessary to ensure each device is synchronously turned on/off. The operation of this topology requires low switching frequency to achieve acceptable switching losses, which results in expensive and bulky DC link capacitor and AC-side filter [76]. Moreover, this approach also results in high voltage stress and harmonic distortion [75].

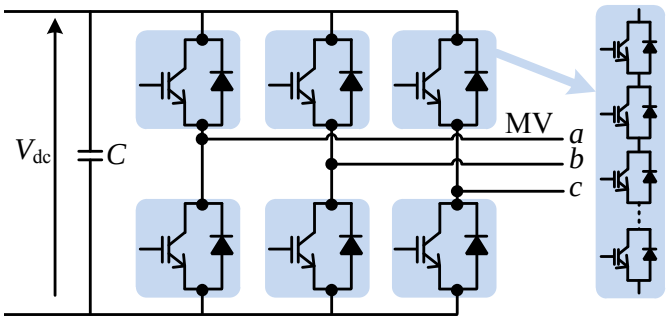


Figure 2.4: 2L VSC formed by the series connection of IGBTs for direct connection to MV grid [76].

The family of multilevel converters (MLC) has emerged as the solution to overcome the voltage limit capability of the semiconductor devices [79]. By combining an array of power semiconductors and capacitor voltage sources, MLCs can generate high voltages, while the power semiconductors must withstand only a fraction of the output voltages [80]. The generation of voltages with three-levels (3L) or more, in contrast to the traditional 2L-VSC, allows to obtain a better harmonic spectrum and smaller voltage stress with low switching frequencies [81, 82].

The diode-clamped converter is also known as neutral-point clamped (NPC) converter because the mid-voltage level is defined as the neutral point [83]. Fig. 2.5 shows the topology of the three-level NPC. As can be seen, the 3L-NPC VSC only requires half the voltage blocking capability of a 2L VSC, which reduces the necessary installed switch power in about 20 % [84]. Advanced modulation strategies have been developed for balancing the neutral-point voltage for all load power factors with the minimum output-voltage switching-frequency distortion [85]. The main drawback of the 3L-NPC converter is to be limited to only three voltage levels. Additional levels can be implemented but require extra components.

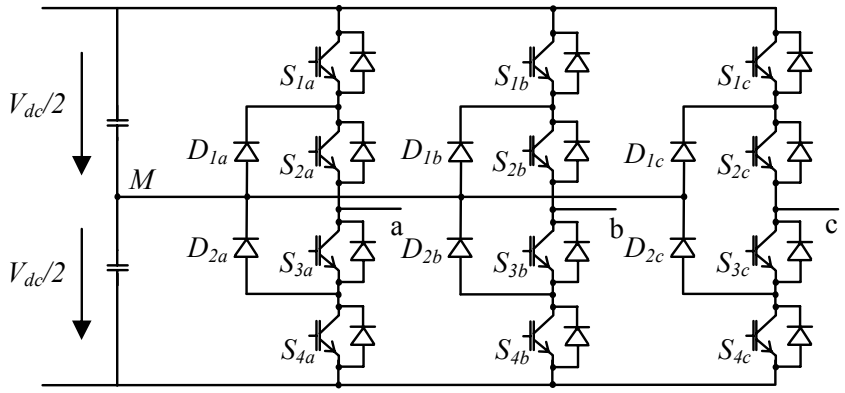


Figure 2.5: Three-level neutral point-clamped voltage source converter (3L-NPC VSC) [84].

The flying capacitor (FLC) converter represented in Fig. 2.6(b) is another MLC. The load current charges and discharges every capacitor, which results in voltage variation that must be within the permissible limits. Thus, the required capacitance decreases approximately as the switching frequency increases [79]. The need of a capacitors voltage balancing strategy and a pre-charge approach at the start-up makes this topology more complex to operate. However, the resulting high first carrier band frequency of the output voltage make this topology attractive fo applications with very low current ripple requirements [86].

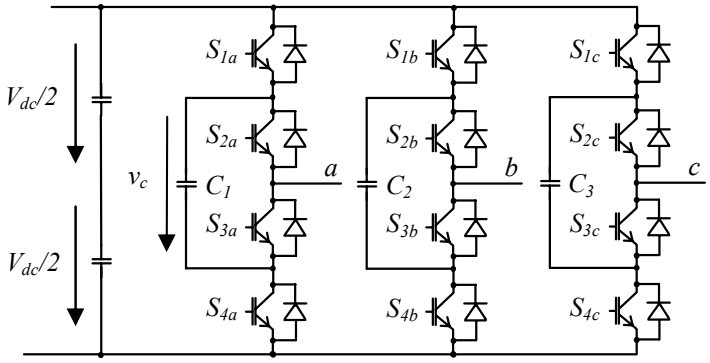


Figure 2.6: Three-level flying capacitor voltage source converter (3L-FLC VSC) [84].

Direct connection of the BESS to the MV grid can also be achieved through the use of cascaded modular converters such as the cascaded H-bridge (CHB) converter or the modular multilevel converter (MMC) [76]. By series-connecting converter submodules higher voltage levels can be achieved, offering modularity and higher degree of redundancy. Additionally, any voltage level requirements can be fulfilled with superior harmonic performance, reduced rating values of the converter components and improved efficiency [87].

The CHB is composed by three phase-legs, each having multiple H-bridge cells connected in series, as illustrated in Fig. 2.7. Typically, dozens or even hundreds of modules are combined in series and parallel to form the BESS. Therefore, the battery modules can be equally distributed to each cell as a small battery pack. Every H-bridge is responsible to generate the required output voltage and simultaneously regulate the power flow of the battery modules connected to its dc-link [88]. This topology is a modular structure, scalable, and has a high degree of redundancy. The optimal number of converter cells is a compromise between conduction losses, total harmonic distortion, efficiency and voltage level of the batteries [73]. A high number of levels can significantly reduce the AC filter requirements and the voltage rating of the power switches [89]. The main disadvantage of this converter is the resulting complex control scheme.

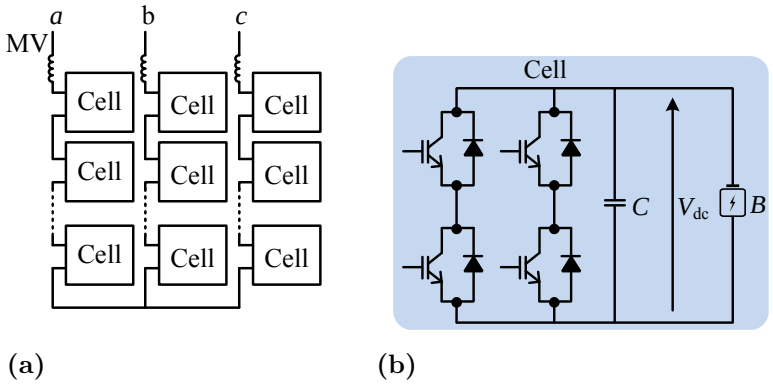


Figure 2.7: Three-phase cascaded H-bridge converter and H-bridge cell [76].

The MMC consists of two arms per phase-leg where each arm is composed by multiple series-connected, nominally identical submodules (SM), and a series inductor L_o, as depicted in Fig. 2.8. The SMs in each arm are controlled to generate the required ac phase voltage, while the arm inductor suppresses the high-frequency components in the arm current [87]. Compared with the CHB, the MMC topology provides additional freedom in dealing with SOC unbalances particularly for operations with grid imbalances [87], which are of particular importance for the BESS. This converter is a modular structure, scalable, and well-suited for high voltage and high power applications. High quality AC voltage waveforms with low harmonics are produced by the MMC which reduces the filtering requirements. However, this converter is still more complex and expensive when compared with to other conventional multilevel VSC.

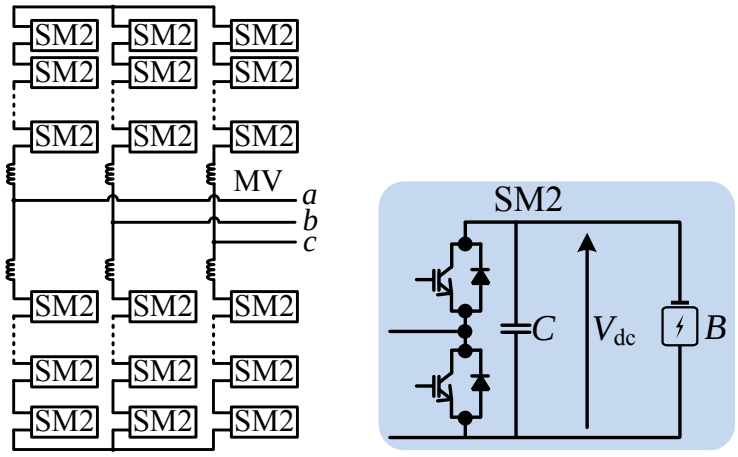


Figure 2.8: Modular multilevel converter with distributed batteries in submodules [76].

2.2 Current Source Converters

Contrary to the VSC, the CSC are not so commonly used for bidirectional interface with the electric power grid. Nevertheless, the application of matrix converters has the potential to achieve higher power densities when compared with the conventional VSC solutions [90–92].

The bidirectional buck–boost matrix converter is represented in Fig. 2.9. By combining six bidirectional switches and a link-inductor, this topology allows to control the dc voltage in a wider range [93]. This characteristic is of particular importance in battery applications, where the voltage of each cell can vary significantly according to the SOC. Recent modulations and control strategies have been developed to reduce the dc current ripple and enable active and reactive power regulation [94, 95]. An experimental comparison of the performance of several modulation strategies in terms of THD of input and output

currents, and efficiency can be found in [96]. Using high-frequency switching results in size reduction of the ac filter and the link-inductor which allows a fast dynamic response of this converter. As the other matrix converters, the main drawback is the need of a commutation strategy for the bidirectional switches to avoid short-circuits and open-loops that can destroy the power semiconductors.

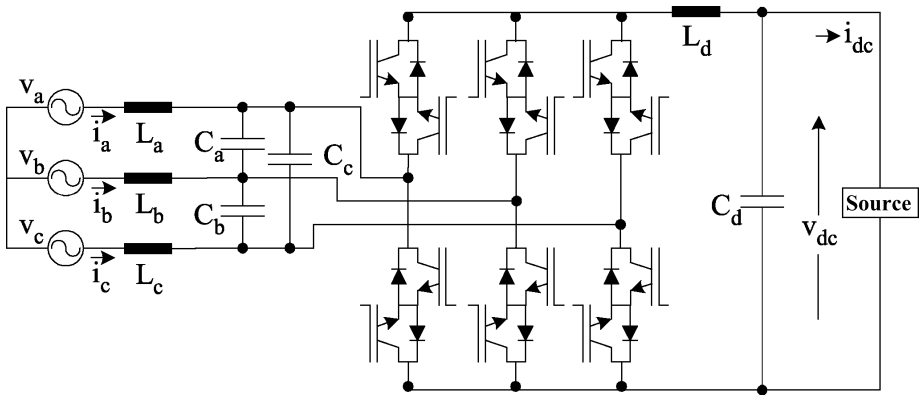


Figure 2.9: Bidirectional buck–boost Matrix Converter [93].

The AC-link configuration has been explored since the 80's as an alternative to the conventional DC-link [97]. Fig. 2.10 shows the bidirectional parallel AC-link matrix converter. The same six bidirectional switches (BSW) of the buck-boost MC are used to make the interface between the electric power grid and the AC-link. Four additional BSW do the interface between the AC-link with the DC power source. By combining an inductor with a parallel capacitor, the resonance of this second order circuit allows bidirectional power flow in buck and boost modes. All switches turn-on under ZVS and the AC-link capacitance ensures soft-switching in all operating conditions [98]. Moreover, a completely indirect energy transfer between the source and the power grid is enabled by this topology. During the first part of the modulation period, the DC input charges the link-inductor. Then, the stored inductive energy is discharged to the electric power grid. Reverse power flow occurs by simply reversing this process. By exploring several patents, this technology is being commercialized by Ideal Power. The company claims that the "embedded firmware and safety sense mechanisms ensure that the PCS DC and AC power ports are never directly connected to one another via both-on power switches", eliminating the need for an isolation transformer [99]. As a result, high efficiency can be

achieved in a compact and light weight converter. The main drawback is the high number of power semiconductors required to form the 10 BSW.

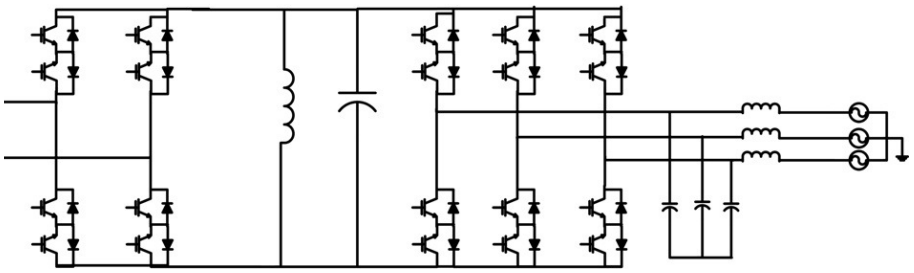


Figure 2.10: Bidirectional parallel AC-link Matrix Converter [98].

2.3 Bidirectional DC-DC Converters

Voltage adaptation between the different subsystems of a PCS is typically required. The bidirectional buck-boost (BBB) DC-DC converter is widely used to perform this task. With two power transistors and one inductor, both buck and boost operating modes can be implemented. This converter can work in discontinuous conduction mode (DCM), continuous conduction mode (CCM), or triangular current mode (TCM) [100]. The main advantage of this converter is to require few components and to be simple to control. However, high electric and thermal stress on the inductor and on both switches occurs, which results in large power losses [101]. Moreover, a bulky inductor is expected if low switching frequency is employed to reduce the power losses.

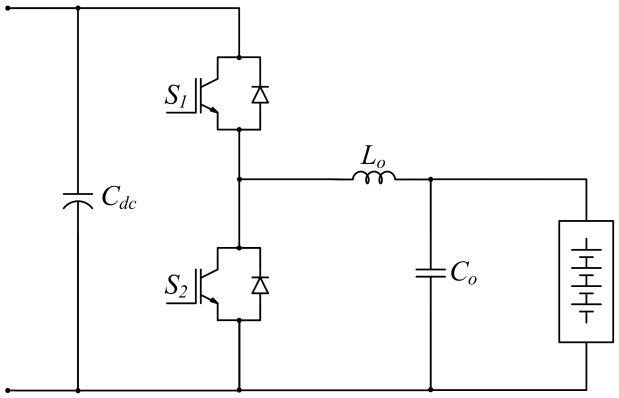
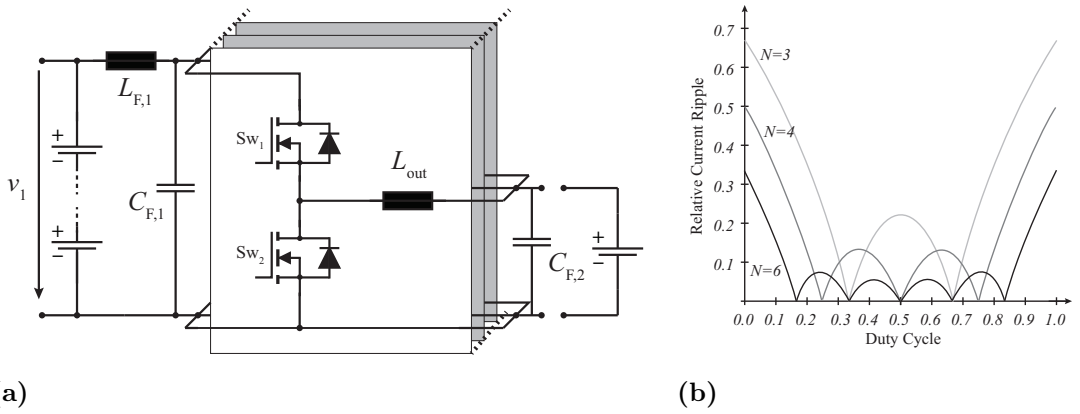


Figure 2.11: Bidirectional buck-boost (BBB) DC-DC Converter.

The interleaved DC-DC converter results as a combination of N modules of the bidirectional buck-boost DC-DC converter, as represented in Figure 2.12. By interleaving the

phase currents of the different modules, a smooth output current can be achieved [102]. The fundamental frequency of the voltage and current ripples at the high and low voltage DC-links is N times the switching frequency, reducing the ripple current for both DC-link capacitors by 1/N [103]. The total volume of the inductors is also reduced by a factor of 1/N due to the small ripple current involved in the conversion process. The modularity of this system allows to achieve high efficiencies under partial load conditions by adapting the number of active phases, which is also known by power shedding. Moreover, continuity of service in case of faults could also be possible by using the interleaved DC-DC converter. However, a high number of phases also requires several power switches, gate driver circuits and more current sensors for phase current balancing. Experimental implementations of the interleaved DC-DC converter have demonstrated that high power densities can be achieved: a 100 kW converter prototype with 25 kW/dm^3 is designed in [103]; a modular SiC-based prototype with 43 kW/dm^3 is proposed in [104].



(a) **(b)**

Figure 2.12: (a) Multi-phase Interleaved DC-DC Converter. (b) Dependency of the output current ripple on the duty cycle and the number of phases (N) for the interleaved DC-DC Converter operated with TCM modulation [102].

The dual active-bridge (DAB) is composed by two full-bridges, a high-frequency transformer (HFT), and optionally a link-inductor, as shown in Fig. 2.13. This topology was originally proposed in [105] (1988) and patented in [106] (priority date: September 29th 1989). By applying high-frequency voltages at the transformer windings, the magnetic circuit can be significantly reduced, which increases the power density of the DC-DC converter while provides galvanic isolation. The DAB uses a principle similar to the power transmission in traditional ac power system. By adjusting the phase-shift between AC square wave voltages v_{T1} and v_{T2}, the direction and magnitude of the inductor current i_L can be changed, allowing the direction and magnitude control of the power flow between both full-bridges bridges [107]. This approach is named single-phase-shift or simply phase-shift modulation (PSM) since only one degree of freedom is available. The extended-phase-shift (EPS), dual-phase-shift (DPS), and triple-phase-shift (TPS) modulations were proposed to decrease current stress, improve efficiency, expand the ZVS operation range,

and minimize the output capacitance, by generating three-level AC voltages at the HFT terminals [108]. Another approach to generate three or five-level AC voltages is by replacing one of the full bridges by a multilevel bridge [109]. The possibility to operate in buck and boost mode associated with the high-efficiency and the fast dynamic response makes the DAB an attractive topology for bidirectional and isolated DC-DC power conversion.

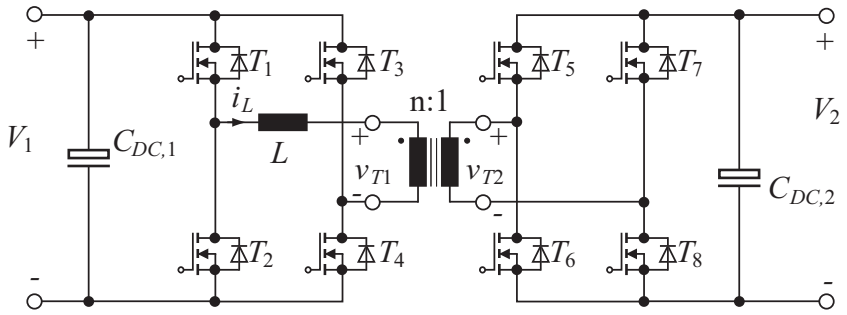


Figure 2.13: Dual Active Bridge Converter (DAB) [110].

Recently, there has been a growing interest in the area of soft-switching resonant topologies. The series resonant converter (SRC) is a topology that allows bidirectional and isolated DC-DC power conversion. As can be seen in Fig. 2.14, the power circuit is very similar to the DAB. Two full-bridges are connected through a series LC resonant tank and a HFT. Maximum efficiency can be achieved by operating the SRC in discontinuous conduction mode (DCM) [111]. A self-sustained oscillation close to the resonance frequency of the resonant tank is obtained with the switching frequency equal or slightly below the resonance frequency [110]. As a result, the DCM-SRC behaves as a "DC transformer" by providing isolation and fixed voltage transfer ratio with a gain around V_2=V_1/n. Very low switching losses can be achieved because the primary-side semiconductors turn-ON in ZVS and turn-OFF in ZCS, while the secondary-side switches operate under ZCS during turn-ON and turn-OFF [111]. Since the current at the high-frequency transformer is practically sinusoidal, low EMI emissions are expected. The reduced voltage range of the DCM-SRC converter is the main disadvantage. However, this converter can be combined with a bidirectional buck-boost DC-DC to optimize the operation range of the PCS in a wide voltage range [110].

The SRC can also be operated in CCM by setting the switching frequency higher than the LC resonance frequency [112]. The phase-shift between the two bridges controls the power flow direction and magnitude. All the switches work with 50 % duty cycle to generate symmetric AC voltages at the HFT windings. However, a dc current component arising from any asymmetric voltages drops in the power circuit which may induce magnetic flux saturation of the transformer [113]. The series capacitor used in the resonant tank blocks this dc component of the magnetizing current which prevents the transformer from saturation [112]. C_R can be split into two parts and placed on both sides of the transformer

to promote symmetric operation [114]. Low switching losses can be achieved because the primary-side semiconductors turn-ON in ZVS, while the secondary-side switches operate under ZCS during turn-OFF for all load and input/output voltage conditions [112]. The main disadvantage of CCM-SRC is the size of resonant capacitor, which results in extra size and cost when compared with the DAB.

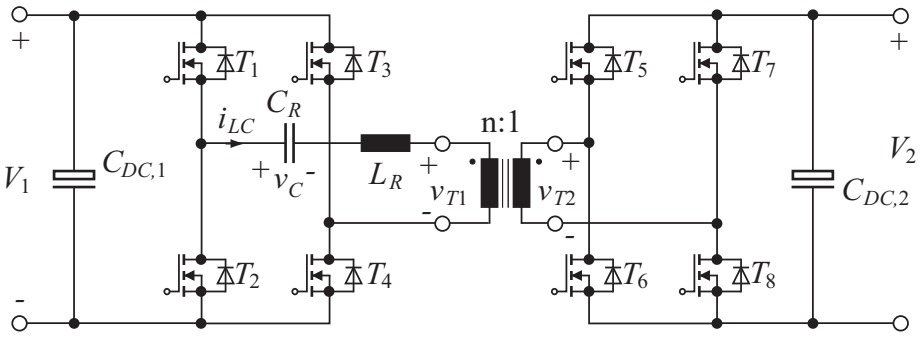


Figure 2.14: Series Resonant Converter (SRC) [110].

The efficiency of SRC drops considerably as the operating switching frequency drifts away from the resonant frequency, making it unsuitable for a very wide input and output voltage range applications [115]. The LLC resonant converter has been investigated due to soft-switching features as the ZVS for primary power switches and soft commutation for output rectifiers [116]. However, the LLC can only operate under unidirectional power conversion. The CLLC-type resonant converter is similar to the LLC-type resonant network with an extra inductor and capacitor in the secondary side, as represented in Fig. 2.15. The resulting topology is symmetric and allows bidirectional power flow between the two DC ports. Other variants of the CLLC topology were proposed in [118, 119]. The design procedure described in [115] can ensure soft-switching in all switches without additional snubber or clamp circuitry: ZVS operation can be achieved on primary side power MOSFETs and ZCS operation on secondary side rectifiers. As a result, very high-frequency

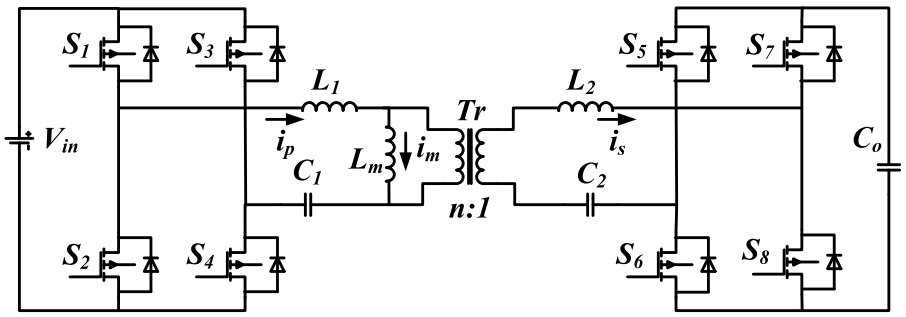


Figure 2.15: CLLC Resonant Converter [117].

operation is possible which enables size reduction of the magnetics and filter capacitors. The design and control complexity of the CLLC converter is higher when compared with the DAB. Instead of an almost linear relation for the gain, the CLLC is controlled by the switching frequency following a nonlinear function that is dependent of the loads. Hence, the required operating frequency can be very large in the case of a wide output voltage range. For the CLLC converter, the output current is sinusoidal, whereas for the DAB converter, the output current has more high-order harmonic components which requires an extra current filter [117].

The DC-DC topologies described above can be combined with the AC-DC converters presented in Section 2.1 and 2.2 to form the bidirectional PCS. In the following sections, conventional solutions based on LF transformer along with dual and single-stage topologies based on the HFL are presented.

2.4 Conventional Isolated AC-DC Converters

The classical solution for the isolated PCS consists in the combination of the 2L VSC with the bidirectional buck-boost converter [64]. The transformer is placed in the low-frequency side such as depicted in Fig. 2.16. The VSC is controlled to keep a constant voltage in the DC-link and providing simultaneously a proper power quality in the grid interface [120]. On other hand, the buck-boost converter is responsible for the voltage and current regulation in the batteries. The galvanic isolation between the grid and the battery pack is provided by the LFT. This solution has the advantages of a low complexity due to a reduced number of components, a well-known control and design techniques, and a wide availability of integrated components. However, the use of a LFT, which is heavy and bulky, is not suitable to obtain a high-power density conversion system.

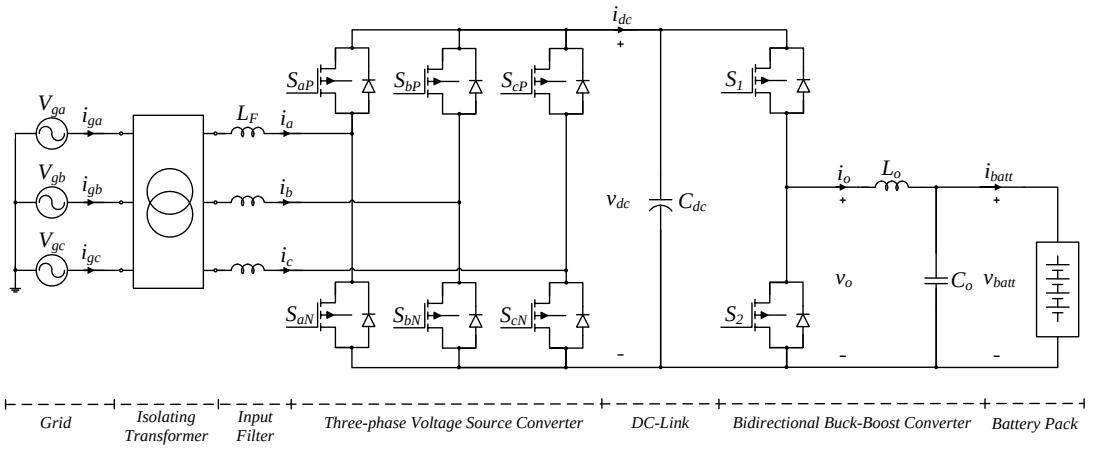


Figure 2.16: Topology based on three-phase Voltage Source Converter and bidirectional buck-boost converter (VSC-BBB).

Alternatives for this topology can be obtained by employing a HFT in the DC-DC conversion stage in order to significantly reduce the size and volume of the transformer [46]. These high-frequency link converters, performing AC to DC energy conversion can be classified as dual-stage (2-S) or single-stage (1-S) ones [121].

2.5 Dual-stage AC-DC Converters with HFL

The traditional 2-S converters are composed by a three-phase VSC in series with a HFL DC-DC converter. The VSC controls the power factor (PF) and modulates the grid currents with low THD. Galvanic isolation and output voltage regulation are then provided by the DC-DC converter [110]. Several topologies based on DAB, dual half-bridge (DHB) and SRC have been proposed for the 2-S HFL [110, 118, 122–124].

Fig. 2.17 shows a topology with a high-frequency transformer in a Dual Active-Bridge configuration. The power circuit comprises a three-phase VSC connected to the grid with an LCL filter. Voltage adaptation and galvanic isolation are provided by the power transformer. The DAB is used to regulate the voltage and current in the battery pack. Hereafter this topology will be called by VSC-DAB. The VSC is commonly controlled by pulse-width modulation (PWM) or by space vector modulation (SVM) [125]. On other hand, the DAB is normally controlled by conventional PSM [126]. The active power flow from primary bridge to secondary bridge over one switching period can be expressed by:

$$P_{DAB} = \frac{V_p V_s}{\omega_s L} n\phi \left(1 - \frac{|\phi|}{\pi}\right). \tag{2.1}$$

where ω_s is the switching frequency in radians per second, L is the primary-referred leakage inductance, n is the transformer turns ratio, and ϕ is the phase-shift between square voltages V_p and V_s.

Nevertheless, the needed for a DC-bus to decouple the operation of the three-phase VSC from the DC-DC converter is also a limitation in terms of volume and shorter life

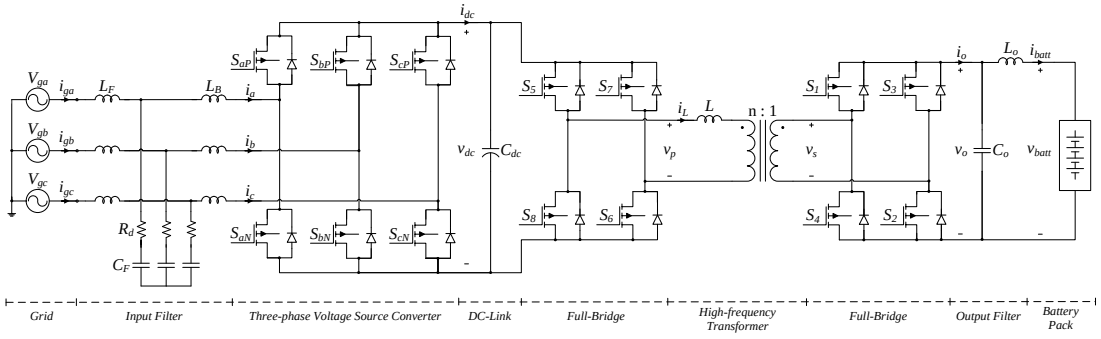


Figure 2.17: Topology based on three-phase Voltage Source Converter and Dual Active Bridge converter (VSC-DAB).

of the capacitors. Several single-stage power converters were proposed to perform bidirectional AC-DC power conversion as a possible alternative for the traditional dual-stage solutions. Possible alternatives based on 1-S structures will be presented in the next section.

2.6 Single-stage AC-DC Converters with HFL

In 2-S conversion structures, capacitors are necessary in order to minimize voltage variation in the DC-link due to instantaneous power difference between the VSC and the HFL DC-DC converter [127]. Capacitors are one kind of the most vulnerable power electronic components in terms of failure rate in field operation [128]. Therefore, several 1-S solutions have been developed to reduce the required capacitance in the conversion chain [60, 91, 129–145]. The use of a full-bridge (FB) converter connected to the secondary winding of the HFT is common to practically all these 1-S solutions. Although, there are different options regarding the grid side converter, such as the synchronous rectifier followed by a DAB [129], the multi-port converter [130], the half-bridge resonant converter [131], and other solutions based on matrix converters [60, 91, 132–145].

The use of a 3×2 matrix converter (MC) for the front-end is an interesting solution due to its capability to perform a direct AC to AC conversion without a DC-link [146]. As described in section 2.2, the matrix converter is an array of controlled bidirectional power switches that connect the voltage source directly to the load without using any DC-link or large energy storage elements. Presently, these characteristics are the main reason for the tremendous interest in this topology, since they allow to obtain a compact solution for a four-quadrant converter. Chapter 3 presents a revision of the traditional matrix converter topologies along with respective modulations.

Fig. 2.18 shows the topology of the high-frequency link matrix converter (HFLMC). Each bidirectional switch S_{xy} is composed by two transistors S_{xy1} and S_{xy2} ($x = a, b, c$ and $y = P, N$) in a common-source configuration, requiring only one floating power supply. The simultaneous commutation of the controlled bidirectional switches used in MCs is difficult to achieve without generating overcurrent or overvoltage spikes that can destroy the power semiconductors. This fact affected negatively the interest in matrix converters for several years until advanced multistep commutation strategies appeared, that allowed safe operation of the switches [147–150]. Precise timing is needed in order to achieve high frequencies. Furthermore, the accurate detection of the current direction or relative voltage magnitude is essential to ensure a proper commutation of the power switches. A review of the commutation strategies is elaborated in Chapter 3.3. The MC works as a current source converter and applies voltage v_p to the HFT. In order to simplify the explanation, the transformer is modeled by a primary-referred leakage inductance L, and an ideal transformer with turns ratio n. Naturally, other elements must then be considered for modeling the transformer, such as the magnetizing inductance, the primary

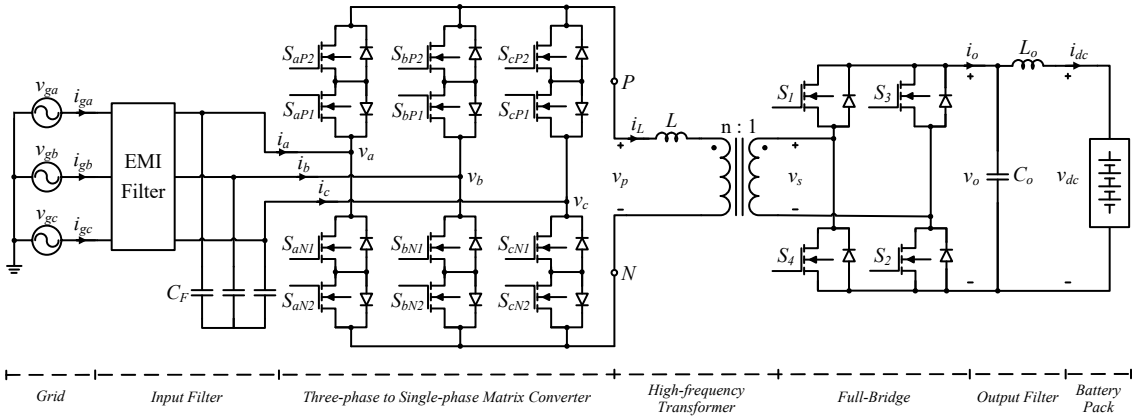


Figure 2.18: Topology based on 3x2 matrix converter with a high-frequency link (HFLMC).

and secondary windings resistance, inter-winding capacitance, and the core losses. Since the HFT operates under a non-conventional voltage and current waveforms, the design of this part should ensure a proper operation of the transformer even if a small DC voltage component appears. Moreover, special attention to the core losses and their impact on the temperature of the material should be taken during the design process. Further details about the modeling and project of the HFT are discussed in Appendix E. The FB works as a current source in its output, producing i_o, by impressing voltage v_s in the HFT. DC voltage v_o is held almost constant through a small film capacitor. The output filter reduces the ripple in DC current i_{dc}. Due to the harmonic content present in the input currents of the MC itself, an EMI filter is required to allow compliance with the electromagnetic compatibility (EMC) standards [151, 152]. A careful dimensioning of the filter is essential to ensure the adequate power factor in all operating range and to achieve a good power quality without penalizing the efficiency, volume and cost. A single-stage LC filter with damping resistor connected in parallel with the inductance is the most common solution and allows the minimization of the power losses [151, 153–155]. The design of process of the HFLMC's EMI filter for CISPR 11 Class B pre-compliance is presented in Chapter 5.

The apparent power flow from the matrix converter to the full-bridge over one switching period is given by:

$$S_{HFLMC} = \frac{3}{4}\frac{V_p V_s}{\omega_s L} n\phi \left(1 - \frac{|\phi|}{\pi}\right). \tag{2.2}$$

where ω_s is the switching frequency in radians per second, L is the primary-referred leakage inductance, n is the transformer turns ratio, and ϕ is the phase-shift between voltages V_p and V_s.

The main drawbacks of the matrix converter are the lack of an intrinsic free-wheeling path and the higher number of gate drivers and isolated power supplies. Although, comparing the HFLMC topology with the VSC-DAB topology only two more transistors are

necessary. Yet, many advantages can be referred, being the first the absence of a DC capacitor bank, which is a key enabler for long life and reliability. Moreover, a pre-charge circuit for the capacitor bank and for the transformer inrush currents is unnecessary, because there is no uncontrolled current path between the grid and the primary winding of the high-frequency transformer. Furthermore, only one floating supply is needed to drive both switches of each cell, in a common source configuration. The VSC-DAB topology also needs more magnetic cores due to the use of an LCL filter instead of the LC filter used in the HFLMC.

There are high-frequency link topologies that act as a current source at its input, such as the HFLMC which is considered in this work, or topologies that act as voltage source. In [135, 139, 140], modulations for the HFL topologies that act as voltage source at its input were proposed. These modulations are based in sinusoidal pulse-width modulation (SPWM) and in SVM. However, issues such as current and voltage regulation in the DC side are not addressed. Differently, modulations for the HFL topologies that act as current source at its input were proposed in [138, 141, 156]. These modulations are different from each other but all employ, at some extent, the same phase-shift principle of the DAB. This approach consists in introducing a phase-shift between the voltages applied by both bridges to the transformer. In this way, bidirectional power flow is enabled and controlled by this variable. These modulations provide current regulation capability in the storage device but do not allow power factor control, keeping it near unitary. From this analysis, it can be concluded that the state of the art modulations proposed for the HFLMC are not capable to regulate current and voltage in the DC side and simultaneously adjust the power factor at the AC side. This gives origin to the first and second Research Questions listed in Section 1.3 regarding the possibility to create a new modulation for the HFLMC. The third Research Question is dependant from the other two, and is related to the formulation of a P-Q controller for the HFLMC.

2.7 Conclusion

After an extensive review of bidirectional AC-DC and DC-DC topologies, the main power converter solutions for the PCS were presented. It can be concluded that the HFLMC has the potential to achieve higher power density with longer service life when compared with conventional topologies. In order to provide deep knowledge about the matrix converter technologies, an extended review is provided in Chapter 3. Then, a new modulation for the HFLMC is developed in Chapter 4 along with the controllers for grid currents, the controller for the battery voltage and current, and also the P-Q controller.

Chapter 3

Review of Matrix Converters

One of the most interesting families of converters is the so-called matrix converters [157]. The matrix converter (MC) is an array of controlled bidirectional power switches that connect the voltage source directly to the load without using any DC-link or large energy storage elements [158], and therefore it is called the "all-silicon" solution. The development of this converter started in 1980 with the work of Venturini and Alesina [159, 160]. They first introduced the name "matrix converter" and presented the power circuit along with a rigorous mathematical analysis to describe the low-frequency behaviour of the converter [158]. An extensive review of the milestones in research on matrix converters is presented in [161]. This converter has some very attractive characteristics [157, 158]:

- compact power circuit;
- generation of output voltage with frequency not coupled to the AC input;
- sinusoidal input and output currents;
- operation with adjustable input power factor;
- full regenerative operation.

These characteristics are the reason for the present tremendous interest in this topology, since they allow to obtain a compact solution for a four-quadrant frequency converter [162]. Since the 1980s, several modulation methods were developed to control this converter, that is also known as Direct Matrix Converter (DMC). Therefore, in this work the Matrix Converter and the Direct Matrix Converter designations will be used indistinctly. More recently, the Indirect Matrix Converter (IMC) has been gaining recognition since maintain the same input–output performance of the conventional matrix converter but with a simpler topology [162]. Figure 3.1 shows the classification of the main force commutated three-phase AC-AC converter topologies, where the DMC and the IMC are obviously included.

In this chapter it will be presented the Direct Matrix Converter and the Indirect Matrix Converter along with a review of the respective actual and most important modulations. In the last part of this chapter are also presented the possible constructive approaches for

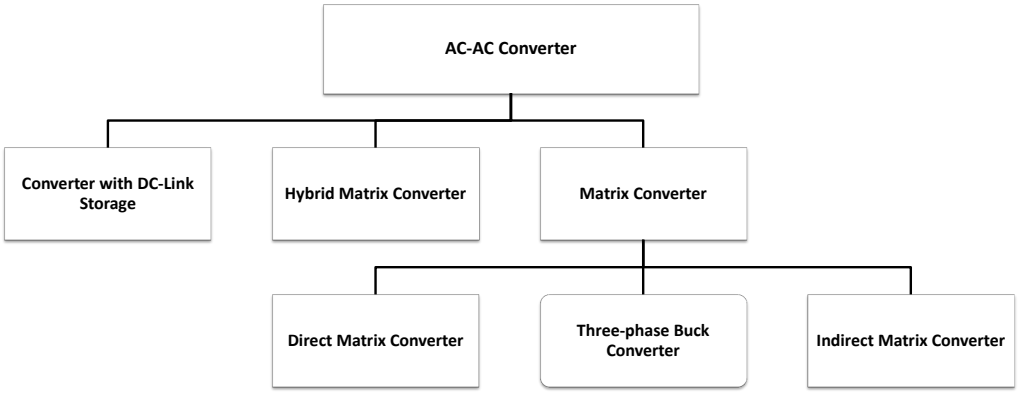


Figure 3.1: Classification of three-phase AC-AC converter topologies (adapted from [163]).

the bidirectional switch along with the current commutation strategies for the MC based on current direction and/or relative voltage magnitude. This review work is fundamental to provide solid knowledge to the reader before the introduction of the high-frequency link matrix converter in Chapter 4.

3.1 Direct Matrix Converter

The Direct Matrix Converter [36] is a single-stage converter which has an array of $m \times n$ bidirectional power switches to directly connect an m-phase voltage source to an n-phase load [146]. The 3×3 matrix converter (3Φ-3Φ MC) has the highest practical interest because it connects a three-phase voltage source with a three-phase load, typically a motor. This converter consists of nine bidirectional switches arranged in three groups of three, each group being associated with an output line [164]. Each group can also be designated as a switching cell (SwC). Therefore, with this arrangement it is possible to connect any of the input line *a*, *b*, or *c* to any of the output line *A*, *B*, or *C*, as it is shown in Figure 3.2(a). The converter diagram is similar to a matrix, with the rows consisting of the three input lines (*a*, *b*, *c*), the columns consisting of the three output lines (*A*, *B*, *C*), and the bidirectional switches connecting each row to each column, which are symbolized with circles in Figure 3.2(b).

The matrix converter operation can be expressed mathematically using the concept of switching function [165]. The switching function, S_{jK}, is defined as the representation of the switch connecting input line j to output line K. When the switch is *closed*, the value of the switching function is *1*, and when the switch is *open*, the value of the switching function is *0*. Therefore, the switching function of a single switch is defined as [166]:

$$S_{jK}(t) = \begin{cases} 1, & \text{switch } S_{jK} \text{ closed} \\ 0, & \text{switch } S_{jK} \text{ open} \end{cases} \qquad j = \{a, b, c\}, \qquad K = \{A, B, C\} \tag{3.1}$$

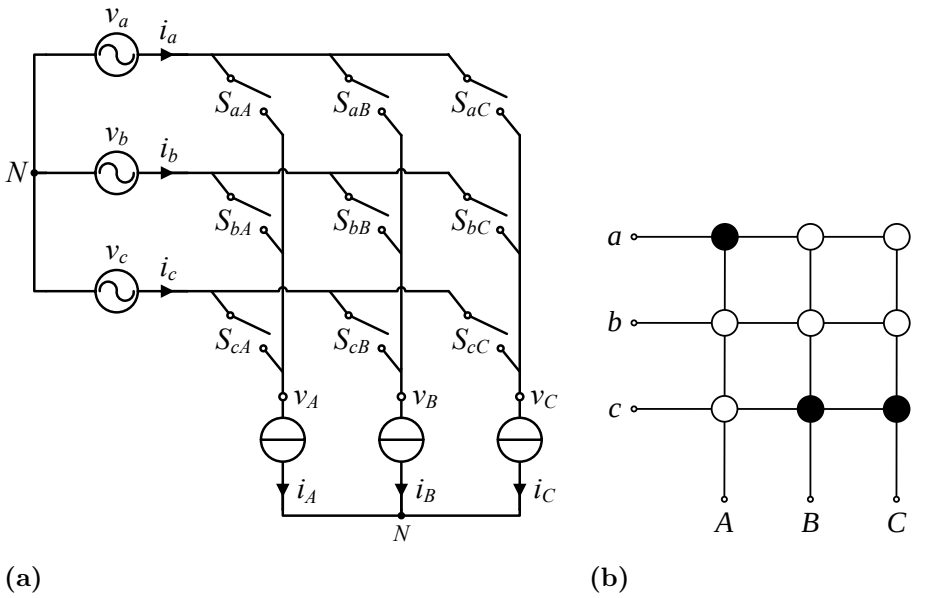


Figure 3.2: Direct Matrix Converter topology. (a) Schematic diagram. (b) Symbol.

3.1.1 Mathematical Model

The procedure used to generate the appropriate firing pulses to each of the nine bidirectional S_{jK} switches is denominated by "Modulation" [146]. In order to develop a modulation strategy for the MC, it is necessary to develop a mathematical model that will be presented thereafter.

The source and load voltages are referenced to the supply neutral, "n" in Figure 3.2a, and can be expressed as vectors defined by

$$\mathbf{v_i} = \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}, \qquad \mathbf{v_o} = \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix}. \tag{3.2}$$

Because of the instantaneous power transfer of the matrix converter, due to absence of a DC-link capacitor, the electrical parameters (voltage and current) on one side may be reconstructed from the corresponding parameters on the other side, at any instant [164]. Using this principle, the relationship between load and input voltages can be expressed as

$$\left.\begin{array}{c} \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} = \begin{bmatrix} S_{aA} & S_{bA} & S_{cA} \\ S_{aB} & S_{bB} & S_{cB} \\ S_{aC} & S_{bC} & S_{cC} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \\ \mathbf{v_o} = \mathbf{T}\left(S_{jK}\right)\mathbf{v_i} \end{array}\right\} \tag{3.3}$$

where $\mathbf{T}(S_{jK})$ is the instantaneous transfer matrix that represents the state of the converter switches [146], and is defined as

$$\mathbf{T}(S_{jK}) = \begin{bmatrix} S_{aA} & S_{bA} & S_{cA} \\ S_{aB} & S_{bB} & S_{cB} \\ S_{aC} & S_{bC} & S_{cC} \end{bmatrix}. \tag{3.4}$$

Each row of $\mathbf{T}(S_{jK})$ shows the state of the switches connected on the same output line and each column shows the state of the switches connected on the same input line [164].

Using the same principle, the following relationship is valid for the input and output currents:

$$\left.\begin{array}{c} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} S_{aA} & S_{aB} & S_{aC} \\ S_{bA} & S_{bB} & S_{bC} \\ S_{cA} & S_{cB} & S_{cC} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} \\ \mathbf{i_i} = \mathbf{T}(S_{jK})^T \mathbf{i_o} \end{array}\right\} \tag{3.5}$$

where $\mathbf{T}(S_{jK})^T$ is the transpose matrix of $\mathbf{T}(S_{jK})$.

By considering that the bidirectional power switches work with a switching frequency much higher than the frequencies of the input voltages and output currents, the high-frequency (HF) components of the variables in (3.3) and (3.5) can be neglected [166]. Then, a low-frequency (LF) output voltage of variable amplitude and frequency can be generated by modulating the duty cycle of the switches using their respective switching functions [146]. The LF or local-averaged value of a switching function S_{jK} is the duty cycle of the corresponding switch, and it is defined as d_{jK}, which can have the following values:

$$0 \leq d_{jK} \leq 1, \qquad j = \{a, b, c\}, \qquad K = \{A, B, C\} \tag{3.6}$$

The low-frequency equivalents of (3.3) and (3.5) are

$$\overline{\mathbf{v}}_\mathbf{o} = \overline{\mathbf{T}}(d_{jK})\, \mathbf{v_i} \tag{3.7}$$

$$\bar{\mathbf{i}}_\mathbf{i} = \overline{\mathbf{T}}(d_{jK})^T \mathbf{i_o} \tag{3.8}$$

respectively, where

$$\overline{\mathbf{T}}(d_{jK}) = \begin{bmatrix} d_{aA} & d_{bA} & d_{cA} \\ d_{aB} & d_{bB} & d_{cB} \\ d_{aC} & d_{bC} & d_{cC} \end{bmatrix} \tag{3.9}$$

is the LF instantaneous transfer matrix that represents the duty cycle of the converter switches. The $\overline{\mathbf{T}}(d_{jK})^T$ is the transpose matrix of $\overline{\mathbf{T}}(d_{jK})$.

Equations (3.3) and (3.5) give the instantaneous relationships between input and output quantities and are the basis of all modulation methods [146, 167]. Specifying the input

voltages, the load parameters, and the switching states, that are given by the modulation strategy, the output voltages and the input currents are determined. This is a simple method of solving a matrix converter system in a simulation program [164]. In the same way, Equations (3.7) and (3.8) can be used to compute the low-frequency components of input and output quantities and modeling the matrix converter operation.

3.1.2 Possible switching states

There are no intrinsic freewheeling paths in the matrix converter as there are in the conventional VSCs. For this reason, a safe transition between the allowed states of a switching cell is more complex to achieve. Ideally, the commutation between the bidirectional switches should occur instantaneously and simultaneously in order to satisfy the restriction in (3.10). However, in practice, this is not possible due to propagation delays in the command circuits and finite switching times of the power semiconductors. For a more clear explanation, the basic commutation circuit of a switching cell is illustrated in Figure 3.3. Three bidirectional switches connect ideal voltage sources to the output phase K that feeds an RL load.

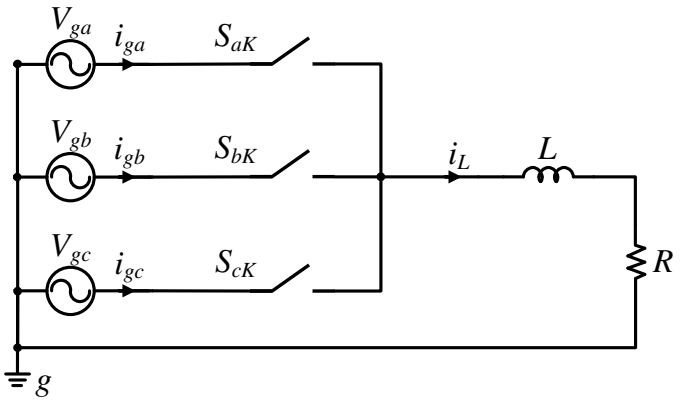


Figure 3.3: Basic commutation circuit of a switching cell with an RL load.

There are two basic rules for the safe commutation between the switches in the switching cell:

- to avoid a short circuit of the input voltage sources, a simultaneous connection of two switches to the same output phase must be strictly avoided;
- the inductive nature of the load makes it impossible to interrupt the current suddenly, and therefore, at least one switch must be closed.

If these rules are not followed, line-to-line short circuits or overvoltages can destroy the converter. These constraints can be expressed by:

$$S_{aK} + S_{bK} + S_{cK} = 1, \qquad K = \{A, B, C\}. \tag{3.10}$$

With these constraints, the 2^9 different switch combinations that the 3Φ-3Φ matrix converter appears to have, are reduced to only 27 allowed switching states [166]. Table 3.1 summarizes the allowed switch states that are subdivided into three groups. Each of these switch combination is characterized by a three letters code that denotes to which input phase the respective output phase is connected (see Figure 3.2b). For example, "*abb*" means that the output phases A, B, and C are respectively connected to input lines a, b, and b.

Table 3.1: The 27 allowed switch states in a matrix converter [168].

Rotating vectors		Stationary vectors						Zero vectors
abc	cba	abb (+1)	baa (-1)	bab (+4)	aba (-4)	bba (+7)	aab (-7)	aaa
cab	acb	bcc (+2)	cbb (-2)	cbc (+5)	bcb (-5)	ccb (+8)	bbc (-8)	bbb
bca	bac	caa (+3)	acc (-3)	aca (+6)	cac (-6)	aac (+9)	cca (-9)	ccc

Each switching state of the matrix converter specifies one output voltage and one input current space vector. These vectors can be called voltage (current) Switching Space Vectors (SSV) [169]. Therefore, the MC synthesize the output voltage (input current) vector from the input voltages (output currents). According to the characteristics of the SSVs associated with each switching state, the 27 allowed switching states are classified into three groups as shown in Table 3.1:

- ***Group I***: six switching states provide a direct connection of each output phase to a different input phase. These SSVs have constant amplitudes. Voltage SSVs rotate at the input frequency ω_i, and current SSVs rotate at the output frequency ω_o [170];

- ***Group II***: eighteen switching states where two output phases are connected to one input phase, and the third output phase is connected to one of the other input phases. These voltage (current) SSVs have fixed directions, occupying one of six positions, regularly spaced 60° apart in the $\alpha\beta$ frame [146]. For this reason, these SSVs will be named "stationary vectors". The magnitude of these voltage (current) SSVs vary with the input voltage phase angle and the output current phase angle, respectively [171]. The maximum length of output voltage vectors is $2/\sqrt{3} \cdot V_{env}$ where V_{env} is the instantaneous value of the rectified input voltage envelope [146];

- ***Group III***: three combinations where all three output phases are connected to the same input phase. These SSVs produce null output voltage and input current vectors (i.e., located at the origin of the $\alpha\beta$ frame) and for this reason they will be named "zero vectors".

3.1.3 Review of modulation techniques for DMC

The performance of the matrix converters is strictly related to the adopted modulation strategy [172]. Several modulation techniques were proposed for the MC since the original control theory proposed by Gyugyi and Pelly in 1976 [173]. The modulation of the matrix converter has evolved from complicated modulation expressions based on transfer function approaches to modern space vector modulation [174]. Figure 3.4 shows a summary of modulation techniques for MCs.

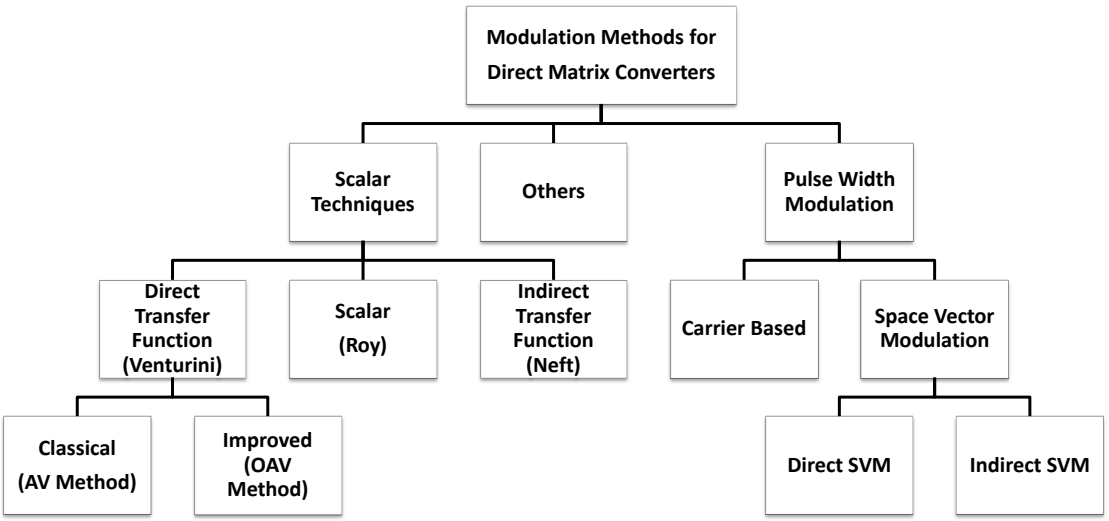


Figure 3.4: Classification of MC modulation techniques.

The first and highly relevant method is called the direct transfer function approach, also known as the Venturini modulation (or also AV Method). This method was proposed in 1980 by Alesina and Venturini in works [159, 160]. Here, the output voltage is obtained by the product of the input voltage and the instantaneous transfer matrix that represents the state of the converter switches (see (3.3)). Although this technique was more effective than traditional control techniques, still having a maximum output voltage equal to half of the input voltage, which corresponds to a voltage transfer ratio of $q = 0.5$. By the end of 1980s, these two researchers proposed in [175, 176] an improved control algorithm by adding a harmonic component to the output reference voltage. This optimum AV modulation, also known as the OAV Method, raised the maximum voltage transfer ratio to 0.866 (or $\sqrt{3}/2$), which was demonstrated to be the theoretical limit under the constraint of sinusoidal input and output waveforms, and provided full input power factor control [177].

In 1983, Rodriguez introduced a conceptually different control technique based on the "fictitious DC-link" idea [178]. With this method, the matrix converter is separated in a rectifier part and an inversion part, which are modulated so that each output line is switched between the most positive and most negative input lines [146]. This concept is also known as the indirect transfer function approach and belongs to the category of indirect methods. These methods aim to increase the maximum voltage transfer ratio above the 0.866 limit of other methods. In 1985–1986, Ziogas et al. published [179] and [180], where the maximum voltage transfer ratio was increased to 1.053. This improvement is obtained at the expense of low frequency harmonic distortion in the output and/or the input current compared to another methods with maximum voltage transfer ratio of 0.866 [146]. The experimental validation of the indirect modulation principle can be found in work [181].

In 1989, Roy developed the scalar modulation algorithm [182], which uses the instantaneous voltage ratio of specific input phase voltages to generate the switch command signals. The main disadvantage of this algorithm is that it needs an accurate measuring of the instantaneous input voltages to do a comparison between their relative magnitudes [146].

Apart from the scalar techniques presented above, the PWM techniques are a very important solution for the control of the MCs. The carrier-based modulation is the simplest approach of this category and came from the modulation of conventional converts [167]. Some works with this modulation technique are reported for example in [183] and [184].

The application of the space vector modulation to matrix converter is conceptually the same as the well-established SVM for voltage source inverters (VSI). However, it is more complicated since SVM has to be applied simultaneously to the output voltage and to the input current modulation. In 1989, Huber and Borojevic proposed in [185] the first control technique for matrix converters based on space vector modulation. This was accomplished by combining the principles of indirect transfer function approach with the principles of space vector modulation, resulting in the Indirect Space Vector Modulation (ISVM). The matrix converter is considered as an imaginary two-stage converter: a rectification stage that provides a fictitious DC-link and an inverter stage that produces the reference output voltages. Each of these stages is controlled using the space vector modulation procedures. The final modulation can then be obtained by merging the two independent space vector modulations. The ISVM was further investigated and is among others treated in [166, 186].

In 1993, Casadei et al. proposed in [187] a different approach to SVM for MCs. Instead of looking to the matrix converter as a two-stage converter with fictitious DC-link, the authors represent all the switch combinations in the stationary $\alpha\beta$ frame and then apply the known space vector approach to modulate simultaneously the input current and output voltage. For this reason, is commonly known as Direct Space Vector Modulation (DSVM). This approach yields a more physical connection and an immediate comprehension of the direct power conversion process [177]. The DSVM was further investigated and is among

others treated in [188, 189].

Other modulation techniques, such as model predictive control [190], sliding mode vector control [191], and direct torque control [192] were proposed for the control of MCs.

Nowadays, the SVM approach is probably the most used and investigated modulation strategy for the MCs [172]. Although the direct and indirect SVM approaches are apparently different, it has been proved in [193] that both can be regarded as one unified SVM method. Therefore, in this work will be explored the DSVM and it will be simply named by SVM since it is the conventional space vector modulation approach.

3.1.4 Space Vector Modulation for DMC

The space vector modulation approach has advantages [187, 193] with respect to other modulation strategies such as:

- immediate comprehension of the required commutation process;
- achieve the maximum voltage transfer ratio without utilizing third harmonic component injection method;
- the input and output power factor are independently controlled;
- minimize the effective switching frequency in each cycle, which reduce the switching losses;
- minimize harmonic content;
- is particularly suitable for digital implementation.

Switching Space Vectors

The space vector approach is based on the instantaneous space vector representation of input and output voltages and currents [189]. In an output $\alpha\beta$ reference frame, the instantaneous voltage space vector of the output is

$$\overline{v}_o = \frac{2}{3}\left(v_{AB} \; + \; \underline{a}v_{BC} \; + \; \underline{a}^2 v_{CA}\right) = v_o e^{j\alpha_o} \tag{3.11}$$

where $\underline{a} \equiv e^{j\frac{2\pi}{3}}$, v_o and α_o are the amplitude and angle of the voltage space vector of the output. In an input $\alpha\beta$ reference frame, the instantaneous input current space vector is

$$\overline{i}_i = \frac{2}{3}\left(i_a \; + \; \underline{a}i_b \; + \; \underline{a}^2 i_c\right) = i_i e^{j\beta_i} \tag{3.12}$$

where i_i and β_i are the amplitude and angle of the current space vector of the input. Using the same transformation, the voltage space vector of the input is

$$\overline{v}_i = \frac{2}{3}\left(v_a \; + \; \underline{a}v_b \; + \; \underline{a}^2 v_c\right) = v_i e^{j\alpha_i} \tag{3.13}$$

where v_i and α_i are the amplitude and angle of the voltage space vector of the input.

Since output voltage and input current SSVs of Group I are rotating in the $\alpha\beta$ frame they cannot be usefully used to synthesize the reference vectors [189]. For this reason, in a SVM strategy, only the stationary and zero vectors are used. Table 3.2 summarizes the switching configurations of 3Φ-3Φ matrix converter used in direct SVM. It is important to note that two switching states with the same number and opposite signs have two voltage/current SSVs with the same magnitude, but opposite directions [169].

Table 3.2: Switching configurations of 3Φ-3Φ matrix converter used in Direct SVM.

Switch Config.	A	B	C	v_{AB}	v_{BC}	v_{CA}	i_a	i_b	i_c	v_o	α_o	i_i	β_i
$+1$	a	b	b	v_{ab}	0	$-v_{ab}$	i_A	$-i_A$	0	$2/\sqrt{3}\cdot v_{ab}$	0	$2/\sqrt{3}\cdot i_A$	$-\pi/6$
-1	b	a	a	$-v_{ab}$	0	v_{ab}	$-i_A$	i_A	0	$-2/\sqrt{3}\cdot v_{ab}$	0	$-2/\sqrt{3}\cdot i_A$	$-\pi/6$
$+2$	b	c	c	v_{bc}	0	$-v_{bc}$	0	i_A	$-i_A$	$2/\sqrt{3}\cdot v_{bc}$	0	$2/\sqrt{3}\cdot i_A$	$\pi/2$
-2	c	b	b	$-v_{bc}$	0	v_{bc}	0	$-i_A$	i_A	$-2/\sqrt{3}\cdot v_{bc}$	0	$-2/\sqrt{3}\cdot i_A$	$\pi/2$
$+3$	c	a	a	v_{ca}	0	$-v_{ca}$	$-i_A$	0	i_A	$2/\sqrt{3}\cdot v_{ca}$	0	$2/\sqrt{3}\cdot i_A$	$7\pi/6$
-3	a	c	c	$-v_{ca}$	0	v_{ca}	i_A	0	$-i_A$	$-2/\sqrt{3}\cdot v_{ca}$	0	$-2/\sqrt{3}\cdot i_A$	$7\pi/6$
$+4$	b	a	b	$-v_{ab}$	v_{ab}	0	i_B	$-i_B$	0	$2/\sqrt{3}\cdot v_{ab}$	$2\pi/3$	$2/\sqrt{3}\cdot i_B$	$-\pi/6$
-4	a	b	a	v_{ab}	$-v_{ab}$	0	$-i_B$	i_B	0	$-2/\sqrt{3}\cdot v_{ab}$	$2\pi/3$	$-2/\sqrt{3}\cdot i_B$	$-\pi/6$
$+5$	c	b	c	$-v_{bc}$	v_{bc}	0	0	i_B	$-i_B$	$2/\sqrt{3}\cdot v_{bc}$	$2\pi/3$	$2/\sqrt{3}\cdot i_B$	$\pi/2$
-5	b	c	b	v_{bc}	$-v_{bc}$	0	0	$-i_B$	i_B	$-2/\sqrt{3}\cdot v_{bc}$	$2\pi/3$	$-2/\sqrt{3}\cdot i_B$	$\pi/2$
$+6$	a	c	a	$-v_{ca}$	v_{ca}	0	$-i_B$	0	i_B	$2/\sqrt{3}\cdot v_{ca}$	$2\pi/3$	$2/\sqrt{3}\cdot i_B$	$7\pi/6$
-6	c	a	c	v_{ca}	$-v_{ca}$	0	i_B	0	$-i_B$	$-2/\sqrt{3}\cdot v_{ca}$	$2\pi/3$	$-2/\sqrt{3}\cdot i_B$	$7\pi/6$
$+7$	b	b	a	0	$-v_{ab}$	v_{ab}	i_C	$-i_C$	0	$2/\sqrt{3}\cdot v_{ab}$	$4\pi/3$	$2/\sqrt{3}\cdot i_C$	$-\pi/6$
-7	a	a	b	0	v_{ab}	$-v_{ab}$	$-i_C$	i_C	0	$-2/\sqrt{3}\cdot v_{ab}$	$4\pi/3$	$-2/\sqrt{3}\cdot i_C$	$-\pi/6$
$+8$	c	c	b	0	$-v_{bc}$	v_{bc}	0	i_C	$-i_C$	$2/\sqrt{3}\cdot v_{bc}$	$4\pi/3$	$2/\sqrt{3}\cdot i_C$	$\pi/2$
-8	b	b	c	0	v_{bc}	$-v_{bc}$	0	$-i_C$	i_C	$-2/\sqrt{3}\cdot v_{bc}$	$4\pi/3$	$-2/\sqrt{3}\cdot i_C$	$\pi/2$
$+9$	a	a	c	0	$-v_{ca}$	v_{ca}	$-i_C$	0	i_C	$2/\sqrt{3}\cdot v_{ca}$	$4\pi/3$	$2/\sqrt{3}\cdot i_C$	$7\pi/6$
-9	c	c	a	0	v_{ca}	$-v_{ca}$	i_C	0	$-i_C$	$-2/\sqrt{3}\cdot v_{ca}$	$4\pi/3$	$-2/\sqrt{3}\cdot i_C$	$7\pi/6$
0_a	a	a	a	0	0	0	0	0	0	0	–	0	–
0_b	b	b	b	0	0	0	0	0	0	0	–	0	–
0_c	c	c	c	0	0	0	0	0	0	0	–	0	–

Output voltage and input current SSVs are represented in the output and input $\alpha\beta$ frame, as shown in Figure 3.5(a) and 3.5(b), respectively. Sector numbers 1 to 6 are assigned for the vector spaces between the two adjacent SSVs in both the input and the output $\alpha\beta$ frames.

Vector synthesis

The SVM algorithm for MCs has the inherent capability to achieve full control of both the output voltage vector and the instantaneous input current displacement angle [166, 186, 187]. In order to explain the modulation algorithm, reference will be made to Figure 3.6(a) and 3.6(b).

At any given sampling instant, the output voltage vector $\overline{v}_o$ and the input current displacement angle φ_i are known as reference quantities. The input line-to-neutral voltage vector $\overline{v}_i$ is imposed by the source voltages and is recognized by its measurements. Then, the control of the input side can be achieved, controlling the phase angle β_i of the input

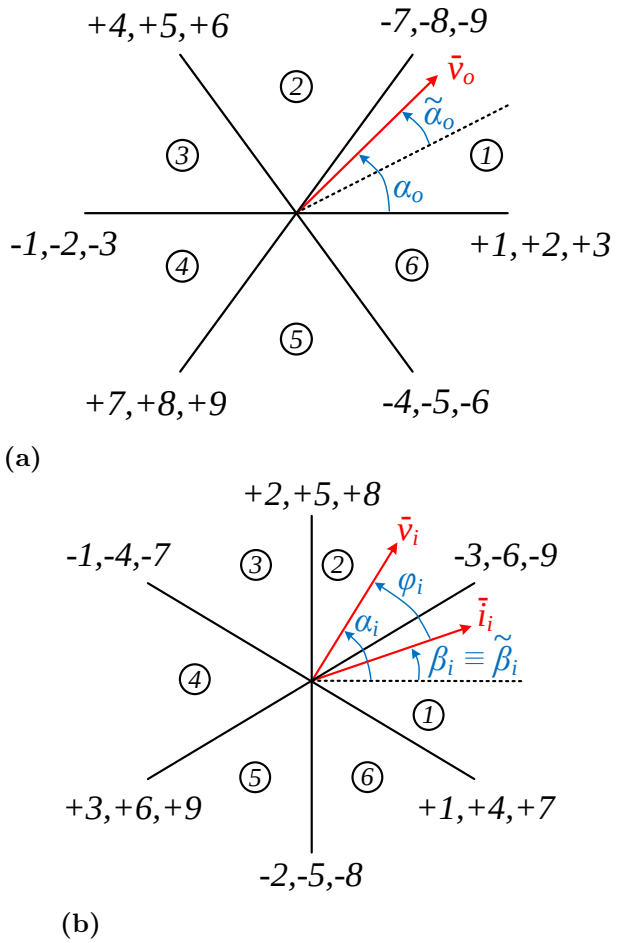


Figure 3.5: Stationary vectors representation in $\alpha\beta$ frame. (a) Output voltage SSVs. (b) Input current SSVs.

current vector [167]. Therefore, the desired phase angle β_i of the input current $\bar{i}_i$ is

$$\beta_i = \alpha_i - \varphi_i. \tag{3.14}$$

Obviously, in order to obtain unity input power factor, the direction of the input current space vector $\bar{i}_i$ has to be the same of $\bar{v}_i$.

The SVM algorithm is based on the selection of four stationary vectors that are applied for suitable time intervals within each cycle period T_s. Vectors $\bar{v}_o$ and $\bar{i}_i$ are then generated through time averaging by choosing the time spent in each of the four stationary vectors during the switching sequence. The switching states whose SSVs are adjacent to the reference output voltage (input current) vector, are selected. Then, the zero vectors are applied to complete the switching period.

It will be assumed that both output voltage and input current space vectors are lying in sector 1 without loss of generality. In Figure 3.6(a), $\bar{v}_o{}^1$ and $\bar{v}_o{}^2$ represent the components of $\bar{v}_o$ along the two adjacent voltage SSVs. In Figure 3.6(b), $\bar{i}_i$ is also resolved into components $\bar{i}_i{}^1$ and $\bar{i}_i{}^2$ along the two adjacent current SSVs. Possible switching states

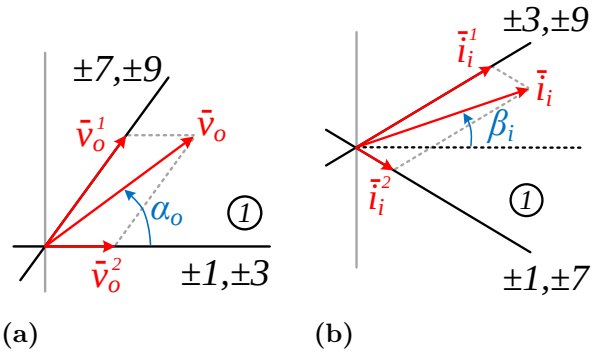


Figure 3.6: Modulation principle. (a) Output voltage vector synthesis. (b) Input current vector synthesis.

that can be utilized to synthesize the components of voltage and current space vectors are

$$\overline{v}_o{}^1: \quad \pm 7, \pm 8, \pm 9; \qquad \overline{v}_o{}^2: \quad \pm 1, \pm 2, \pm 3; \tag{3.15}$$

$$\overline{i}_i{}^1: \quad \pm 3, \pm 6, \pm 9; \qquad \overline{i}_i{}^2: \quad \pm 1, \pm 4, \pm 7. \tag{3.16}$$

To simultaneously synthesize the output voltage and the input current space vectors, common switching states ±7, ±9, ±1, ±3 are selected. From two switching states with the same number but opposite signs, only one should be used since the corresponding voltage or current SSVs are in opposite directions [169]. The ones that have the higher voltage values are selected [187]. Using the same procedure, it is possible to determine the four switching configurations related to any possible combination of output voltage sector (K_V) and input current sectors (K_I), leading to the results summarized in Table 3.3 [171, 189, 194]. Four symbols (I, II, III, IV) are also introduced in the last row of Table 3.3 to identify the four general switching states, valid for any combination of input and output sectors.

As mentioned above, both input current and output voltage vectors are synthesized by considering the proper duty cycles. The duty cycles for the four general switching states are calculated based on the phase of output voltage and input current vector references using the following relationships [188]:

$$\delta^I = \frac{2}{\sqrt{3}}\, q\, \frac{cos(\tilde{\alpha}_o - \pi/3)\; cos(\tilde{\beta}_i - \pi/3)}{cos\varphi_i} \tag{3.17}$$

$$\delta^{II} = \frac{2}{\sqrt{3}}\, q\, \frac{cos(\tilde{\alpha}_o - \pi/3)\; cos(\tilde{\beta}_i + \pi/3)}{cos\varphi_i} \tag{3.18}$$

$$\delta^{III} = \frac{2}{\sqrt{3}}\, q\, \frac{cos(\tilde{\alpha}_o + \pi/3)\; cos(\tilde{\beta}_i - \pi/3)}{cos\varphi_i} \tag{3.19}$$

$$\delta^{IV} = \frac{2}{\sqrt{3}}\, q\, \frac{cos(\tilde{\alpha}_o + \pi/3)\; cos(\tilde{\beta}_i + \pi/3)}{cos\varphi_i} \tag{3.20}$$

where $q = |\overline{v}_o|/(\sqrt{3}|\overline{v}_i|)$ is the voltage transfer ratio. In (3.17)-(3.20) $\tilde{\alpha}_o$ and $\tilde{\beta}_i$ are

Table 3.3: Selection of switching states for each combination of output voltage and input current [194].

		K_V													
		1 or 4					2 or 5					3 or 6			
K_I	1 or 4	(1,1) (4,4)	+9	-7	-3	+1	(4,2) (1,5)	+6	-4	-9	+7	(1,3) (4,6)	+3	-1	-6	+4
		(4,1) (1,4)	-9	+7	+3	-1	(1,2) (4,5)	-6	+4	+9	-7	(4,3) (1,6)	-3	+1	+6	-4
	2 or 5	(5,1) (2,4)	+8	-9	-2	+3	(2,2) (5,5)	+5	-6	-8	+9	(5,3) (2,6)	+2	-3	-5	+6
		(2,1) (5,4)	-8	+9	+2	-3	(5,2) (2,5)	-5	+6	+8	-9	(2,3) (5,6)	-2	+3	+5	-6
	3 or 6	(3,1) (6,4)	+7	-8	-1	+2	(6,2) (3,5)	+4	-5	-7	+8	(3,3) (6,6)	+1	-2	-4	+5
		(6,1) (3,4)	-7	+8	+1	-2	(3,2) (6,5)	-4	+5	+7	-8	(6,3) (3,6)	-1	+2	+4	-5
			I	II	III	IV		I	II	III	IV		I	II	III	IV

the output voltage and input current phase angle measured regarding the bisecting line of the corresponding sector (see Figure 3.5) and differ from α_o and β_i according to the output voltage and input current sectors [188]. In these equations, the following angle limits apply:

$$-\frac{\pi}{6} < \tilde{\alpha}_o < +\frac{\pi}{6}, \qquad -\frac{\pi}{6} < \tilde{\beta}_i < +\frac{\pi}{6}. \tag{3.21}$$

The duty cycle of the zero vectors, δ^{0a}, δ^{0b}, and δ^{0c}, is such that the total duty cycle must be equivalent to the unit, in order to complete the switching period, i.e., at a fixed sampling

$$\delta^{0a} + \delta^{0b} + \delta^{0c} = 1 - (\delta^{I} + \delta^{II} + \delta^{III} + \delta^{IV}). \tag{3.22}$$

It should be noted that the duty cycles for the switching states at any time instant are limited by the following constraints:

$$\begin{aligned} \delta^{0a}, \delta^{0b}, \delta^{0c} &\geq 0 \\ \delta^{I}, \delta^{II}, \delta^{III}, \delta^{IV} &\geq 0. \end{aligned} \tag{3.23}$$

Considering these constraints and (3.17)-(3.22), in the particular case of balanced supply voltages and balanced output voltages, the maximum voltage transfer ratio is given by [189]:

$$q <= \frac{\sqrt{3}}{2}|cos\varphi_i|. \tag{3.24}$$

Assuming unity input power factor, (3.24) gives the well-known maximum voltage transfer ratio of matrix converters [175] under the constraint of sinusoidal input and output waveforms.

Switching pattern

The four general switching states along with the zero vectors can be organized within the switching period T_s. This switching configuration sequence that defines the turn-on and turn-off sequence of the switches is commonly named switching pattern [189]. Different switching patterns have different influence on the performance and efficiency of the matrix converter. This way, the arrangement of the three zero voltage vectors introduces a degree of freedom that can be used to improve the modulation strategy [172, 193].

In the first papers regarding space vector modulation only one zero vector placed at the end of the switching period was used [187]. For this reason, this switching pattern is considered a single-sided modulation. At the expense of only a slight increase in the number of Branch-Switch-Over (BSO) per switching period, double sided modulation has become the prevalent method, since it allows a better harmonic performance at the input and output side of MC [168]. From the use of three zero vectors in each cycle period arises a switching pattern with 12 BSOs [189]. It can be verified that among all possible switching sequences there is only one sequence characterized by only one switching commutation for each change of the output voltage. Table 3.4 shows the switching sequence for the first half of the period in function of the sum of K_V and K_I. In the other half of the period the sequence order is reversed. δ^{01}, δ^{02} and δ^{03} are the duty cycles of the three zero states that are used in the switching pattern.

Table 3.4: Switching sequence for the first half of the switching period T_s.

$\boldsymbol{K_V + K_I}$	**Switching sequence**						
Even	δ^{01}	δ^{III}	δ^{I}	δ^{02}	δ^{II}	δ^{IV}	δ^{03}
Odd	δ^{01}	δ^{I}	δ^{III}	δ^{02}	δ^{IV}	δ^{II}	δ^{03}

These zero states correspond to different zero vectors that should be selected according to the input current sector as represented in Table 3.5.

Table 3.5: Zero states to select according the input current sector.

$\boldsymbol{K_I}$	$\boldsymbol{\delta^{01}}$	$\boldsymbol{\delta^{02}}$	$\boldsymbol{\delta^{03}}$
1, 4	δ^{0c}	δ^{0a}	δ^{0b}
2, 5	δ^{0b}	δ^{0c}	δ^{0a}
3, 6	δ^{0a}	δ^{0b}	δ^{0c}

The resultant switching sequence of output voltages in the time domain is shown in Table 3.6, where it can be noted that the sequence varies with the input current sector.

Assuming that both the output voltage and input current vectors are in sector 1, the corresponding general double-sided switching pattern is as shown in Figure 3.7.

Table 3.6: Switching sequence of output voltages in the time domain.

K_I	Output voltages					
1, 4	c	a	b	b	a	c
2, 5	b	c	a	a	c	b
3, 6	a	b	c	c	b	a

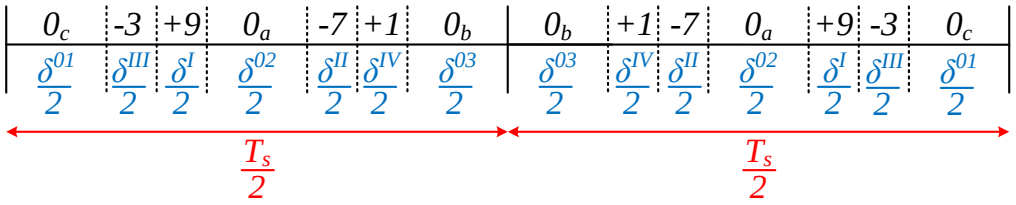


Figure 3.7: General double-sided switching pattern in a switching period T_s with $K_V = K_I = 1$.

The input current ripple depends on the switching frequency seen from the input and on the values of the input filter parts [195]. For a given input filter the only way to reduce the input current ripple is to increase the switching frequency seen from the input of the MC. The input switching frequency can be determined by the number of breaks in the MC input current which corresponds to a zero-vector [195]. Since the three zero switching states can be chosen there exists two degrees of freedom in the switching pattern definition. These two degrees of freedom might be used to eliminate one or two zero states, which affects the number of commutations in each switching period, leading to two zero or one zero switching pattern. The different switching patterns were assessed in [172] in order to investigate their effect in the power losses and in the quality of the input and output current. Table 3.7 shows the different switching strategies and their switching frequencies according to the zero states represented in Figure 3.7.

Strategies 1-3 are characterized by a single zero state for each half of the switching

Table 3.7: Strategies for zero switching states and respective switching frequencies.

Strategy number	Defining equation	Switching frequency
1	$\delta^{01} = \delta^{03} = 0$	$f_s = 8/T_s$
2	$\delta^{01} = \delta^{02} = 0$	$f_s = 8/T_s$
3	$\delta^{02} = \delta^{03} = 0$	$f_s = 8/T_s$
4	$\delta^{01} = \delta^{03}, \delta^{02} = 0$	$f_s = 10/T_s$
5	$\delta^{01} = \delta^{02}, \delta^{03} = 0$	$f_s = 10/T_s$
6	$\delta^{02} = \delta^{03}, \delta^{01} = 0$	$f_s = 10/T_s$
7	$\delta^{01} = \delta^{02} = \delta^{03}$	$f_s = 12/T_s$

pattern and thus have eight BSOs [196]. Strategy 1 was proposed in [197] and is commonly known as Low Distortion modulation method. This strategy uses only the zero configuration in the middle of the half period (δ^{02} in Figure 3.7), and in this way, the switches of one branch of the MC do not change their states (in this case, the first branch of Figure 3.2a).

Strategies 4-6 use two zero configurations for each half of the switching pattern and have 10 BSOs. Strategy 4 was proposed in [195] and takes advantage of the switching sequence to increase the switching frequency seen from the grid side. This strategy increase the switching frequency on the input side in 60% compared to strategies 2 and 3. Among all different strategies, the best quality of the input current is obtained with Strategy 4.

Strategy 7 utilizes all the three zero configurations in each switching period, with equal duty cycles, and thus have 12 BSOs. In the same way, a three zero switching pattern can increase the switching frequency seen from the grid side in 25 % compared to a two zero switching pattern. Among these seven strategies, the best quality of the output current is obtained with Strategy 7.

An optimal modulation strategy in terms of output current ripple was proposed in [172]. This strategy is based on the calculation of the optimal duty cycles of the zeros vectors in order to achieve the minimum *rms* value of the load current ripple in each switching period. Since the efficiency is also better than the Strategy 7, the optimal modulation should be preferred when the output current quality is a necessity.

In sum, Strategy 4 should be chosen if the input current quality or efficiency are the most important requirements. Conversely, if the output current quality is a priority then optimal modulation should be preferred [172].

3.1.5 Simulation of the SVM for DMC

In order to validate the theoretical analysis and to get a deep insight about the SVM implementation, a simulation workbench was developed. The space vector modulation with the respective switching pattern generator was implemented in MATLAB / Simulink (MLS) [198]. The power circuit was modeled using the circuit simulator GeckoCIRCUITS [199]. Using the available interface between these two simulators, it was possible to perform a complete simulation in both the control/modulation and circuit domains. The parameters used in the simulation are listed in Table 3.8.

Table 3.8: Parameters used in the simulation.

Parameter	Value	Parameter	Value
V_i	325 V	R	10 Ω
f_i	50 Hz	f_o	100 Hz
f_s	10 kHz	L	30 mH

An *RL* load is connected to the DMC output as represented in Figure 3.8. As is commonly known, the matrix converter acts as a voltage source at its output and as a current source at its input. For this reason, and due to the high harmonic content of their input current, an input filter is necessary to allow the connection with the grid and fulfil the standards of electromagnetic compatibility and harmonics. Although, for this first validation it was decided to use the same conditions of the theoretical analysis presented above. Thus, an ideal voltage source was directly connected to the DMC input with waveform as depicted Figure 3.9(a).

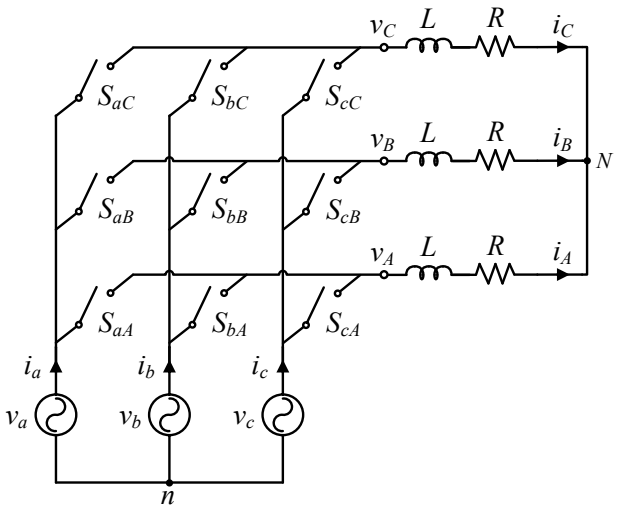
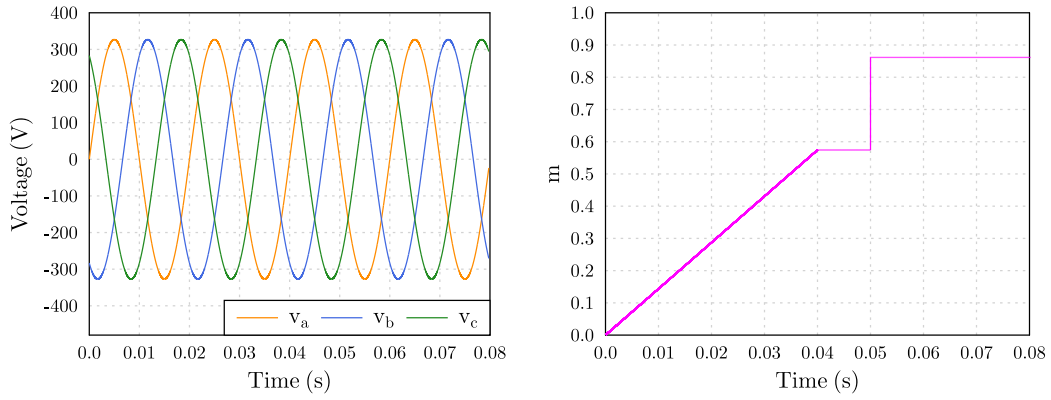


Figure 3.8: Power circuit of the DMC modeled for simulation.

The reference output frequency was kept constant at 100 Hz and the modulation index was changed according to the curve presented in Figure 3.9(b). The maximum voltage transfer ratio q_{ref} involved in this test is 0.75 which is bellow the limit stated in (3.24). As a result, the maximum modulation index m used in this simulation is 0.866.



(a) **(b)**

Figure 3.9: (a) Input voltages of the DMC controlled by SVM. (b) Modulation index.

Figure 3.10 shows the input currents of the DMC that are supplied by the ideal input voltage source. The magnitude of these currents evolve as a function of the variation in the modulation index. If an appropriately dimensioned low-pass filter is connected between the input voltage source and the DMC, these currents would be nearly sinusoidal.

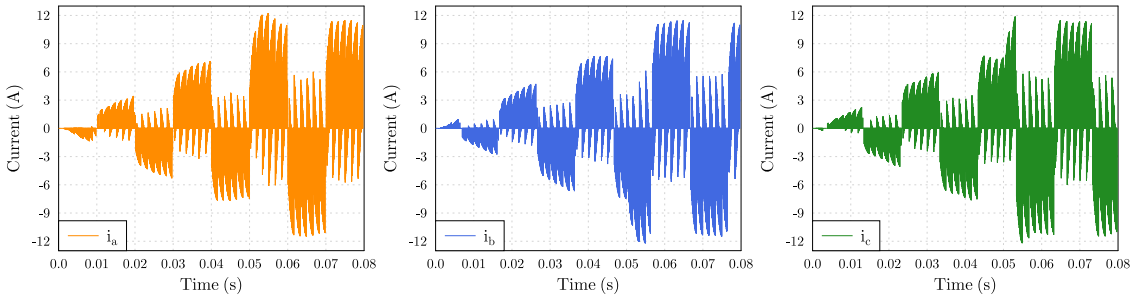


Figure 3.10: Input currents of the DMC controlled by SVM.

The line and phase voltages at the DMC output are presented in Figures 3.11 and 3.12, respectively.

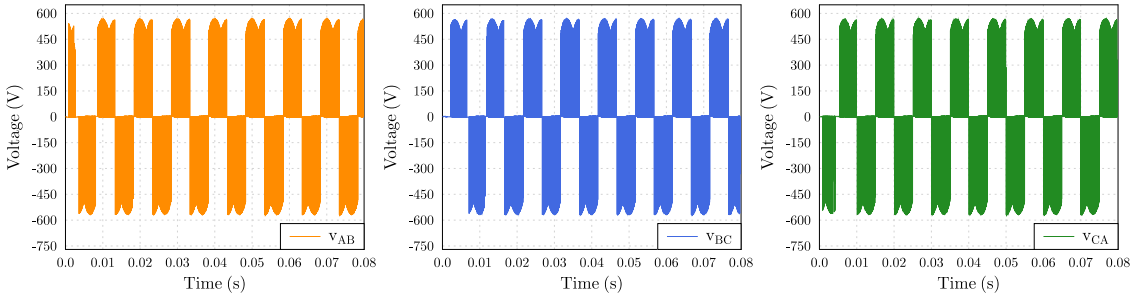


Figure 3.11: Output line voltages of the DMC controlled by SVM.

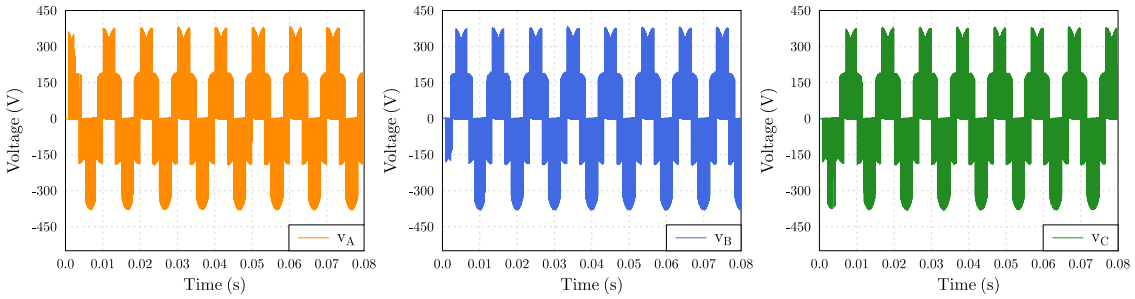


Figure 3.12: Output phase voltages of the DMC controlled by SVM.

Figure 3.13 shows the output currents of the matrix converter that circulate in the load. The magnitude of these currents evolve accordingly to the modulation index variation presented in Figure 3.9(b). This load acts as a low-frequency filter and, as a result, the

high-frequency components of the output voltages are not present in the output currents. The magnitude of these currents is a function of the load impedance ($2\pi f_o L + R$), the input voltage and the voltage transfer ratio.

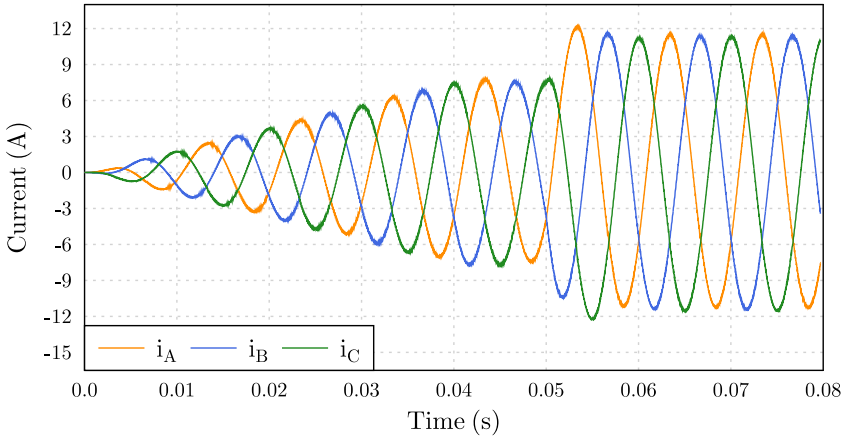


Figure 3.13: Output currents of the DMC controlled by SVM.

The implementation of the SVM in the developed workbench was very useful to validate the theoretical analysis and to observe the operation of the direct matrix converter.

3.2 Indirect Matrix Converter

The "fictitious DC-link" idea was introduced in 1983 by Rodriguez for the control of the Direct Matrix Converter [178]. Considering this idea, Holtz and Boelkens [200] proposed in 1989 a new topology of a AC-AC converter without DC energy storage elements. This topology physically implements the direct MC with indirect modulation to explore the "fictitious DC-link" idea through the reorganization of the DMC switches [201, 202]. For this reason, it is known as Indirect Matrix Converter and may replace the DMC since it offers the same benefits and disadvantages [162]. A circuit topology of the IMC is illustrated in Figure 3.14.

The IMC is divided into two parts that separate the AC-AC conversion into two stages, such as the source and the load side converter [203]. The source converter is a three-phase to single-phase matrix converter that is composed of six bi-directional switches built with 12 unidirectional switches. This converter works as a Current Source Rectifier (CSR) with the purpose of generating sinusoidal input currents as well as maintaining a constant local-averaged voltage at the DC bus. The load side converter is a conventional three-phase voltage source inverter composed of six unidirectional switches that is used to form output voltages. The dual bridges together employ 18 IGBTs and 18 diodes similar to those in the direct matrix converter. However, the physical realisation is much easier, because the inverter stage could be realised by a conventional six-pack power module when compared to fully employment of bidirectional switches in the direct MC. The IMC

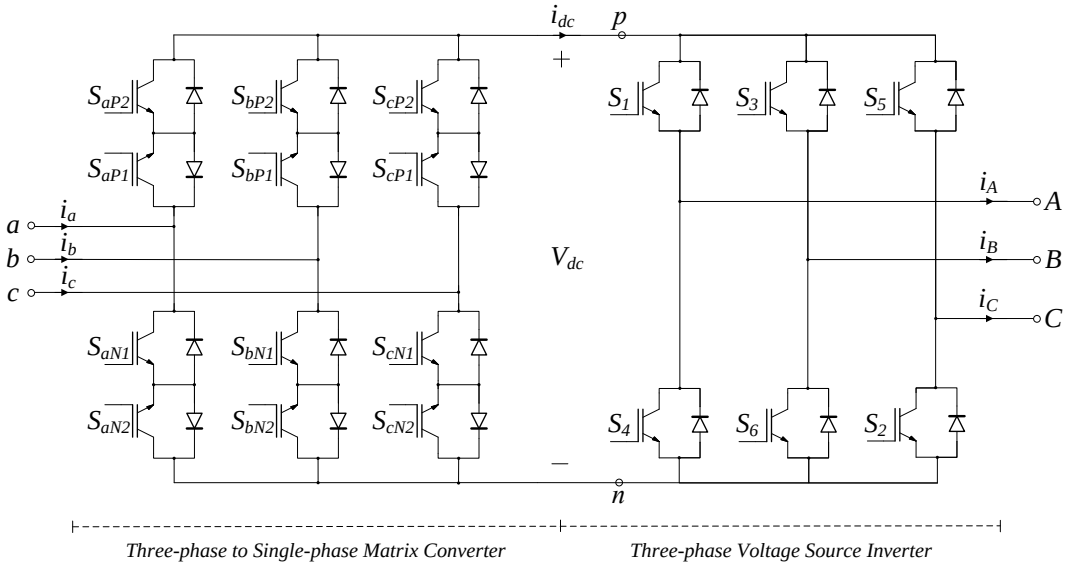


Figure 3.14: Indirect Matrix Converter topology.

also turns possible a reduction in the number of active switches of the source bridge to three if no bidirectional power flow is needed [204].

3.2.1 Review of modulation techniques for IMC

The existence of two stages in the IMC allows the employment of conceptually different control techniques that take advantage of the decoupling present in the conversion process. The synchronization of the modulation process of CSR and VSI is necessary to maintain the power balance with sinusoidal supply currents, since there are not any energy storage element between the dual bridges [205].

Several modulation techniques were proposed for the indirect MC, but most research on IMC has been done using pulse width modulation [206], space vector modulation [207] or predictive control [208].

In 1995, Huber et. al [166] formulated the Indirect Space Vector Modulation for the DMC. Then, Jussila in [209] extensively investigated and applied the indirect space vector modulation to the indirect matrix converter.

Due to the current interest in this modulation and its high performance, in this work it will be presented in the next section the main aspects of the ISVM for the control of the indirect MC.

3.2.2 Space Vector Modulation for IMC

The indirect space vector modulation for the IMC is based on the instantaneous space vector representation of input and output voltages and currents. Since the indirect MC has two conversion stages, the modulation for the source and load bridges can be done

separately. Then, the duty cycles that result from this analysis can be combined to complete the modulation. In the following, the switching frequency is presumed to be so high that the input current and output voltage reference vectors remain constant during one switching period. In addition, the ideal sinusoidal and symmetric input and output quantities with constant frequencies and magnitudes are also assumed.

Space Vector Modulation of Source Bridge

The switching states of the input phases a, b and c of the source bridge can be described by switching functions sw_a, sw_b and sw_c, respectively. As described by the restriction in (3.10), the short-circuiting of the input phases is not allowed. In this way, these switching functions can assume only three-values:

- 1: connection of the input phase to the DC-link bar p through the on-state of the upper switch;
- 0: unconnected state when both switches are off;
- -1: connection of the input phase to the DC-link bar n through the on-state of the lower switch.

Since only one input phase may be connected to each bar at a time, the input switching functions should satisfy

$$sw_a \; + \; sw_b \; + \; sw_c = 0. \tag{3.25}$$

The input currents can be expressed through the switching functions: $i_a = sw_a i_{dc}$, $i_b = sw_b i_{dc}$ and $i_c = sw_c i_{dc}$. Considering this result, (3.12) can be rewritten to express the instantaneous input current space vector as follows:

$$\bar{i}_i = \frac{2}{3}\left(i_a \; + \; \underline{a} i_b \; + \; \underline{a}^2 i_c\right) = \frac{2}{3}\left(sw_a \; + \; \underline{a} sw_b \; + \; \underline{a}^2 sw_c\right) i_{dc} = \overline{sw}_i i_{dc} \tag{3.26}$$

where i_{dc} is the DC-link current and $\overline{sw}_i$ is the space vector of the source bridge switching functions:

$$\overline{sw}_i = \frac{2}{3}\left(sw_a \; + \; \underline{a} sw_b \; + \; \underline{a}^2 sw_c\right). \tag{3.27}$$

If permissible value combinations of sw_a, sw_b and sw_c are substituted into (3.27), it is possible to derive the input current vectors presented in Figure 3.15(a) when $i_{dc} > 0$ and in Figure 3.15(b) when $i_{dc} < 0$. Each current vector in Figure 3.15 is denoted by $i_x\left(sw_a, sw_b, sw_c\right)$.

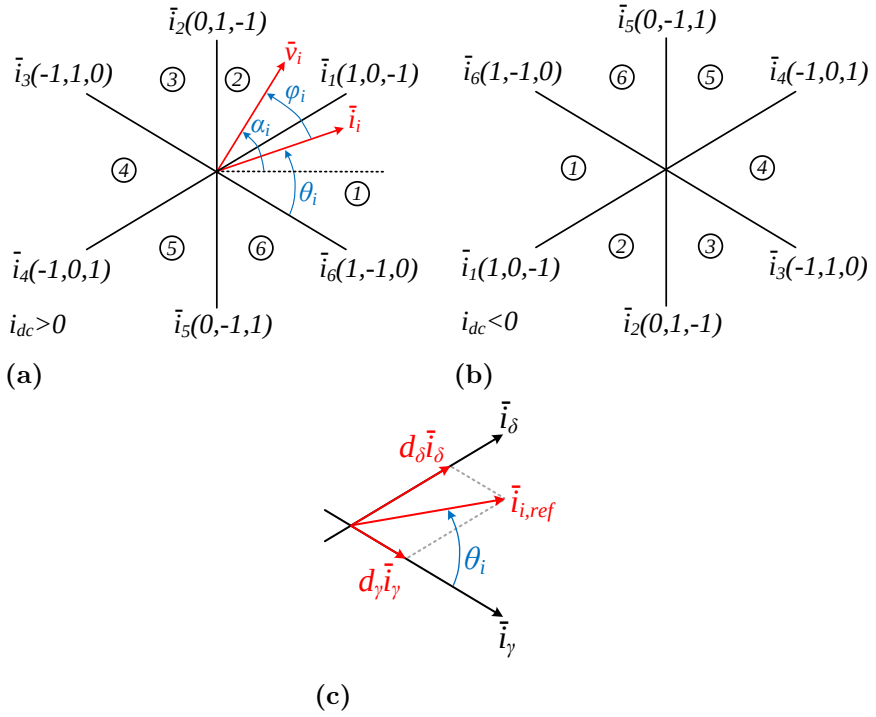


Figure 3.15: Input current SSVs in $\alpha\beta$ frame when (a) i_{dc} ¿ 0 and (b) i_{dc} ¡ 0. (c) Synthesis of the input current reference vector $i_{i,ref}$.

As shown in Figure 3.15(c), the current reference vector $i_{i,ref}$ can be synthesised in one switching period by means of the two adjacent current vectors:

$$\bar{i}_{i,ref} = d_\gamma \bar{i}_\gamma \; + \; d_\delta \bar{i}_\delta \tag{3.28}$$

where the duty cycles of the current vectors $\bar{i}_\gamma$ and $\bar{i}_\delta$ are d_γ and d_δ, respectively. The angle of the reference current vector within the actual sector is θ_i. As proved in [209], the duty cycles d_γ and d_δ are

$$d_\gamma = \frac{|\bar{i}_{i,ref}|}{|i_{dc}|} \sin\left(\frac{\pi}{3} - \theta_i\right) = \sin\left(\frac{\pi}{3} - \theta_i\right) \tag{3.29a}$$

$$d_\delta = \frac{|\bar{i}_{i,ref}|}{|i_{dc}|} \sin\left(\theta_i\right) = \sin\left(\theta_i\right) \tag{3.29b}$$

since the current ratio $|\bar{i}_{i,ref}|/|i_{dc}|$ is set at unity to not limit the link current i_{dc} that is dependent of the load.

Space Vector Modulation of Load Bridge

The switching states of the output phases A, B and C of the load bridge can be described by switching functions sw_A, sw_B and sw_C, respectively. As described by the restriction in (3.10), the open circuit of the load is not allowed. In this way, these switching functions can assume only two-values:

- 1: connection of the output phase to the DC-link bar p through the on-state of the upper switch;
- -1: connection of the output phase to the DC-link bar n through the on-state of the lower switch.

Since at least one output phase may be connected to each bar at a time, the output switching functions should satisfy

$$sw_A \; + \; sw_B \; + \; sw_C \neq 0. \tag{3.30}$$

The output phase voltages with respect to the virtual midpoint of the DC-link can be expressed through the switching functions: $v_A = sw_A V_{dc}/2$, $v_B = sw_B V_{dc}/2$ and $v_C = sw_C V_{dc}/2$. Considering this result, the instantaneous output voltage space vector is

$$\overline{v}_o = \frac{2}{3}\left(v_A \; + \; \underline{a} v_B \; + \; \underline{a}^2 v_C\right) = \frac{2}{3}\left(sw_A \; + \; \underline{a} sw_B \; + \; \underline{a}^2 sw_C\right)\frac{V_{dc}}{2} = \overline{sw}_o \frac{V_{dc}}{2} \tag{3.31}$$

where V_{dc} is the DC-link voltage and $\overline{sw}_o$ is the space vector of the load bridge switching functions:

$$\overline{sw}_o = \frac{2}{3}\left(sw_A \; + \; \underline{a} sw_B \; + \; \underline{a}^2 sw_C\right). \tag{3.32}$$

If permissible value combinations of sw_A, sw_B and sw_C are substituted into (3.32), it is possible to derive the output voltage vectors presented in Figure 3.16(a). The zero vectors $\overline{v}_{0+}$ and $\overline{v}_{0-}$ are produced by connecting all output phases to the bar p or to the bar n, respectively. Each voltage vector in Figure 3.16 is denoted by $v_x\,(sw_A, sw_B, sw_C)$.

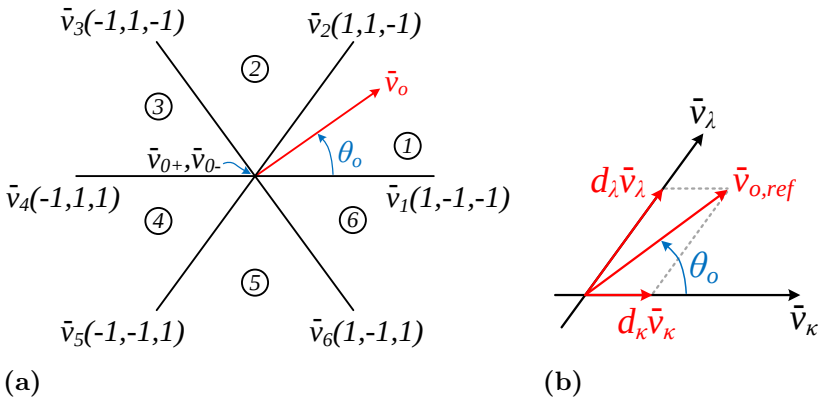


Figure 3.16: (a) Output phase voltage SSVs in $\alpha\beta$ frame. (b) Synthesis of the output voltage reference vector $v_{o,ref}$.

As shown in Figure 3.16(b), the output phase voltage reference vector $v_{o,ref}$ can be synthesised in one switching period by means of the two adjacent voltage vectors:

$$\overline{v}_{o,ref} = d_\kappa \overline{v}_\kappa \; + \; d_\lambda \overline{v}_\lambda \tag{3.33}$$

where the duty cycles of the voltage vectors $\overline{v}_\kappa$ and $\overline{v}_\lambda$ are d_κ and d_λ, respectively. The angle of the reference voltage vector within the actual sector is θ_o. As proved in [209], the duty cycles d_κ and d_λ are

$$d_\kappa = \frac{|\overline{v}_{o,ref}|\sqrt{3}}{V_{dc}} \sin\left(\frac{\pi}{3} - \theta_o\right) = m \sin\left(\frac{\pi}{3} - \theta_o\right) \tag{3.34a}$$

$$d_\lambda = \frac{|\overline{v}_{o,ref}|\sqrt{3}}{V_{dc}} \sin\left(\theta_o\right) = m \sin\left(\theta_o\right) \tag{3.34b}$$

where m denotes the modulation index that ranges from zero to unity.

Combination of Source and Load Bridges

As presented in Figure 3.14, the source and load bridges are connected to each other through the fictitious DC-link. As proved in [209], the output voltage is synthesised by applying the load bridge states during source bridge states. In this way, the resulting four active voltage vectors $\overline{v}_{\gamma\kappa}$, $\overline{v}_{\delta\kappa}$, $\overline{v}_{\gamma\lambda}$ and $\overline{v}_{\delta\lambda}$ are used to synthesise the output voltage in the modulation period T_s. The duty cycles of the active voltage vectors are:

$$d_{\gamma\kappa} = d_\kappa d_\gamma = m \sin\left(\frac{\pi}{3} - \theta_o\right) \sin\left(\frac{\pi}{3} - \theta_i\right), \tag{3.35a}$$

$$d_{\delta\kappa} = d_\kappa d_\delta = m \sin\left(\frac{\pi}{3} - \theta_o\right) \sin\left(\theta_i\right), \tag{3.35b}$$

$$d_{\gamma\lambda} = d_\lambda d_\gamma = m \sin\left(\theta_o\right) \sin\left(\frac{\pi}{3} - \theta_i\right), \tag{3.35c}$$

$$d_{\delta\lambda} = d_\lambda d_\delta = m \sin\left(\theta_o\right) \sin\left(\theta_i\right). \tag{3.35d}$$

The zero vectors $\overline{v}_{0(+,-)}$ are used to complete the modulation period T_s, whose duty cycle is:

$$d_0 = 1 - (d_{\gamma\kappa} + d_{\delta\kappa} + d_{\gamma\lambda} + d_{\delta\lambda}). \tag{3.36}$$

The modulation index m can also be expressed as a direct relation between the output and input voltages of the IMC. For that, it is necessary to express the average DC-link voltage V_{dc} by the input quantities as follows:

$$V_{dc} = \frac{3}{2}|\overline{v}_{i,1}| cos\varphi_{i,1} \tag{3.37}$$

which can be substituted into (3.34) to obtain

$$m = \frac{2}{\sqrt{3}} \frac{|\overline{v}_{o,ref}|}{|\overline{v}_{i,1}| cos\varphi_{i,1}} = \frac{2}{\sqrt{3}} \frac{q_{ref}}{cos\varphi_{i,1}} \tag{3.38}$$

where q_{ref} is the reference of the input-to-output voltage transfer ratio, $\varphi_{i,1}$ is the fundamental displacement angle between the input current and phase voltage, and it is assumed that $\overline{v}_{o,ref}$ and $\overline{v}_{i,1}$ contain only the fundamental component. In the linear modulation range $m = [0, 1]$ and thus, the maximum value of the voltage transfer ratio reference q_{ref}

is $\sqrt{3}/2 = 0.866$, which is attained when $cos\varphi_{i,1}$ is unity. This result is coherent with the previously obtained in (3.24) for the DMC controlled by direct SVM.

With the present modulation, the DC-link voltage v_{dc} produced by the source bridge is always positive. In this way, the diodes of the load bridge are always reverse-biased and the DC-link is not short-circuited. Furthermore, considering that the same performance of the DMC is achieved, it is clear the advantages of the IMC controlled by the indirect SVM.

Switching pattern

The duty cycles presented in (3.35)-(3.36) can be organized in several ways to form the switching pattern. Works [163, 166, 196, 210] present alternatives and comparison of modulation methods that intend to minimize the common-mode voltage, the number of commutations or the output voltage distortion. The different switching patterns have different influence on the performance and efficiency of the indirect matrix converter.

Two alternatives for the switching pattern are presented in [163]. The first strategy allows a zero current switching (ZCS) of the input bridge, and the second strategy allows a zero voltage switching (ZVS) of the output bridge. Considering the higher number of switches in the input bridge and the higher complexity involved in the second strategy, the first strategy is preferable for practical purposes.

In [210] is proposed the Conventional SVM (CSVM) that is very similar to the first strategy presented in [163]. In the CSVM, the duty cycles are arranged in order to minimize the number of commutations. As a result, only one commutation for each duty cycle change occurs within this switching pattern. Thus, whereas the ZCS result in eight BSOs, the CSVM produces only six BSOs. Considering the high number of switches of the IMC, this is an important approach to reduce the switching losses and improve the overall conversion efficiency. Moreover, the CSVM has the advantage that can be implemented with simpler logic. For this reason, the CSVM was chosen for this work and will be presented as follows.

The CSVM switching pattern can be defined for all the 36 combinations of input and output sectors, through the following rules:

- The pattern on the source bridge is always $\gamma - \delta - \gamma$;
- The pattern of the load bridge is $\kappa - \lambda - 0 - \lambda - \kappa$ if the sum of K_V and K_I is even;
- The pattern of the load bridge is $\lambda - \kappa - 0 - \kappa - \lambda$ if the sum of K_V and K_I is odd;
- If K_I is even the output zero vector must be $\overline{v}_{0+}$, i.e. (1,1,1) as presented in Figure 3.16;
- If K_I is odd the output zero vector must be $\overline{v}_{0-}$, i.e. (-1,-1,-1) as presented in Figure 3.16.

Similarly to the switching pattern for the DSVM (see section 3.1.4), a double-sided symmetric pattern with the zero vector $\overline{v}_0$ in the middle of the modulation period T_s is used. The resulting duty cycle patterns of the CSVM for the first half of the modulation period are shown in Table 3.9. To achieve a symmetric switching pattern the sequence order of the active vectors is reversed in the other half of the period.

Table 3.9: Duty cycle patterns of the CSVM for the first half of the switching period T_s.

$K_V + K_I$	Duty cycle sequence				
Even	$d_{\gamma\kappa}/2$	$d_{\gamma\lambda}/2$	$d_{\delta\lambda}/2$	$d_{\delta\kappa}/2$	$d_0/2$
Odd	$d_{\gamma\lambda}/2$	$d_{\gamma\kappa}/2$	$d_{\delta\kappa}/2$	$d_{\delta\lambda}/2$	$d_0/2$

The number of zero states during a modulation period could be increased by dividing the zero duty cycle into several parts. This strategy can improve the output voltage distortion mainly at low modulation indexes at the cost of higher switching losses, which is an important drawback [209]. A common solution involves the change of the modulation method according to the current operation requirements, as investigated for example in work [195].

Table 3.10 shows the switching pattern of the CSVM during a switching period. The zero output voltage state is generated by employing the zero vector $\overline{v}_0$ in the load bridge, producing a null DC-link current and $v_{AB} = v_{BC} = v_{CA} = 0$. This output voltage is independent of the DC-link voltage so, in order to avoid unnecessary switchings, the state sw_δ is taken for the source bridge during the zero output voltage state. The sequence for the output bridge vary in function of the input and output sector numbers.

Table 3.10: Switching pattern of the CSVM for the switching period T_s.

		Switching state								
		1	2	3	4	5	6	7	8	9
Input state		sw_γ		sw_δ					sw_γ	
Output state	Even ($K_V + K_I$)	sw_κ	sw_λ		sw_κ	sw_0	sw_κ	sw_λ		sw_κ
	Odd ($K_V + K_I$)	sw_λ	sw_κ		sw_λ	sw_0	sw_λ	sw_κ		sw_λ

3.2.3 Simulation of the SVM for IMC

In order to validate the theoretical analysis and to get a deep insight about the SVM implementation for the IMC, a simulation workbench was developed using the same approach as section 3.1.5. An *RL* load is connected to the IMC output as represented in Figure 3.17. The parameters used in this simulation are the same listed in Table 3.8. The same ideal voltage source was directly connected to the IMC input (see Figure 3.9(a)). The reference output frequency was kept constant at 100 Hz and the modulation index

was changed according the curve presented in Figure 3.9(b), which is equal to the one used for the DMC simulation.

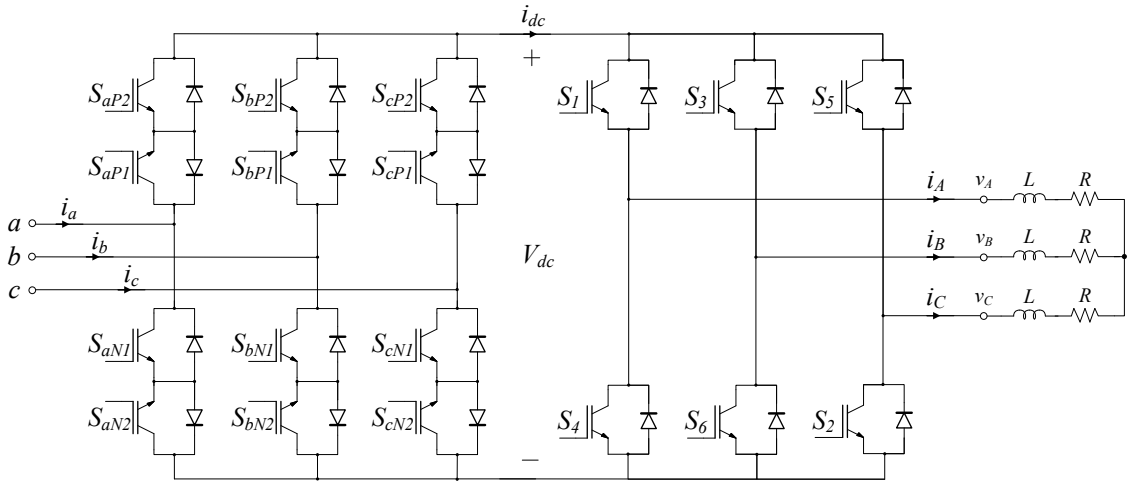


Figure 3.17: Power circuit of the IMC modeled for simulation.

Figure 3.18 shows the IMC input currents that are supplied by the ideal input voltage source. The magnitude of these currents evolve as a function of the modulation index variation. As it is possible to see, a high harmonic content is present in the input current, so an input filter is necessary to allow the connection with the grid. If an appropriately dimensioned low-pass filter is connected between the input voltage source and the IMC, these currents would be nearly sinusoidal.

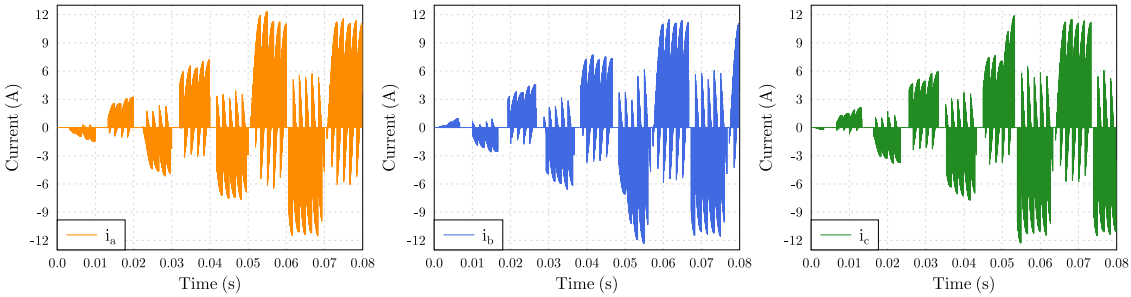
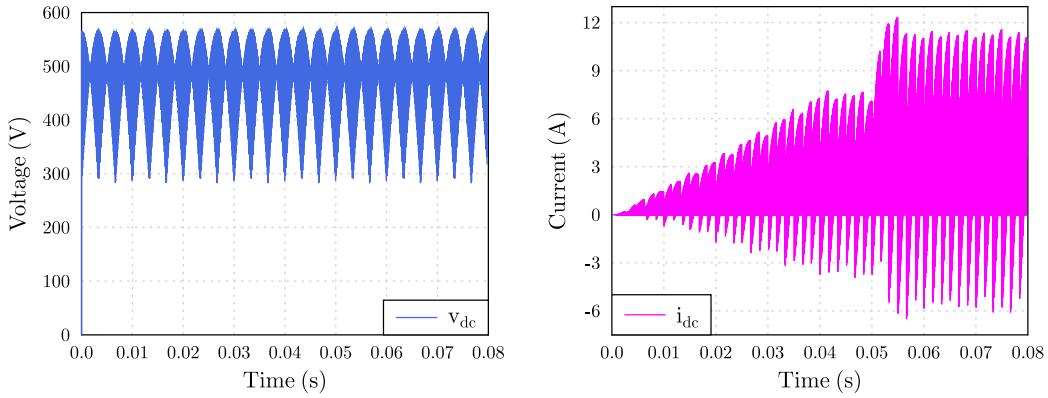


Figure 3.18: Input currents of the IMC controlled by SVM.

The DC-link voltage and current are shown in Figure 3.19. Since there is not a capacitor in the DC-link, a fictitious voltage is generated from the IMC input voltage rectification. The average value of this voltage is around 500 V that is very near the value that results from (3.37).

The output line and phase voltages at the IMC output are presented in Figures 3.20 and 3.21, respectively. For this simulation, the same *RL* load used previously in section 3.1.5 was connected in the IMC output.



(a) **(b)**

Figure 3.19: DC-link (a) voltage and (b) current.

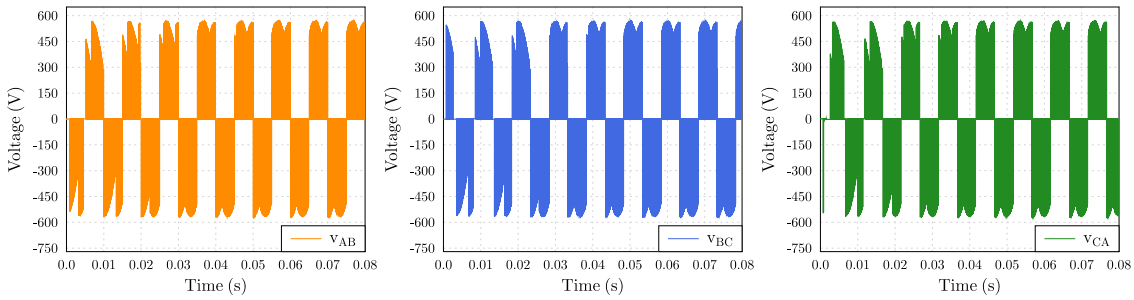


Figure 3.20: Output line voltages of the IMC controlled by SVM.

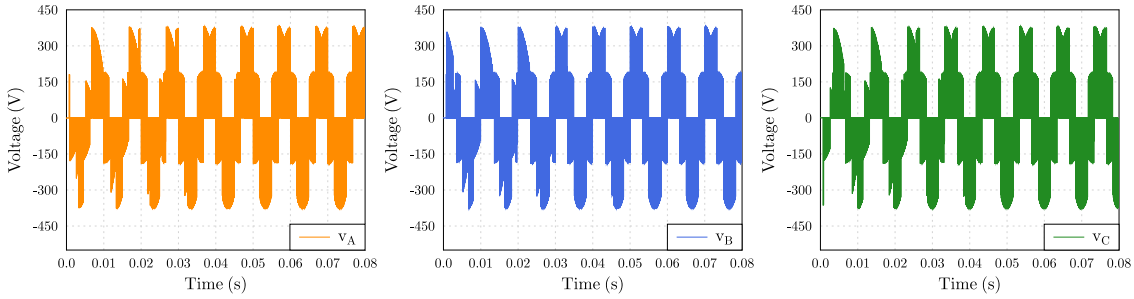


Figure 3.21: Output phase voltages of the IMC controlled by SVM.

Figure 3.22 shows the output currents of the matrix converter that circulate in the load. The magnitude of these currents change accordingly to the modulation index variation presented in Figure 3.9(b). The output current is very similar to the previously obtained in Figure 3.13.

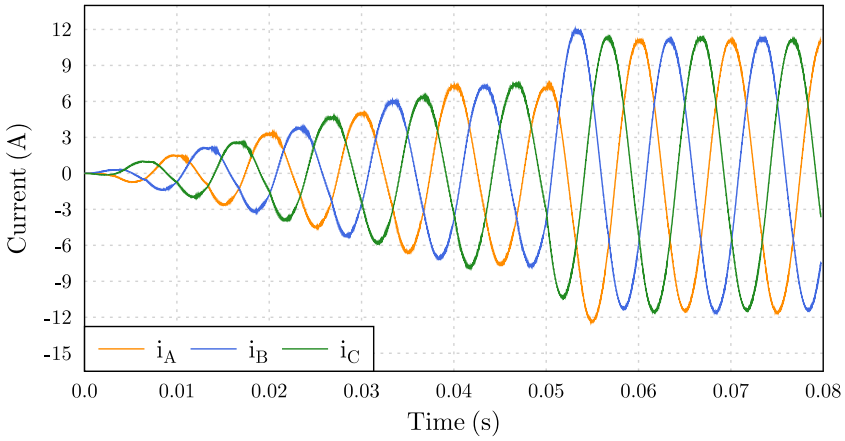


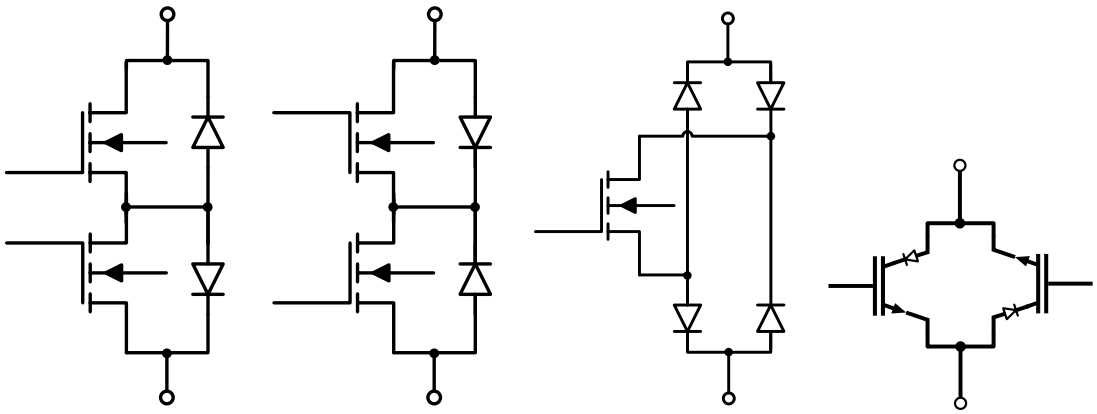
Figure 3.22: Output currents of the IMC controlled by SVM.

The implementation of the SVM in the developed workbench was very useful to validate the theoretical analysis and to get deep knowledge about the operation of the indirect matrix converter.

3.3 Bidirectional switch

The matrix converter is composed by fully-controlled bidirectional switches with the capability to operate in the four-quadrants of the voltage-current plane. In this way, a bidirectional switch is capable of blocking voltage and conducting current in both directions with turn-on and turn-off controllability [146, 211, 212]. Unfortunately, there are no such devices currently available, so discrete power semiconductors need to be used to construct a proper bidirectional switch. The main drawback are the parasitic inductances associated with the connections between the transistors [213]. A modular integrated design and construction of a bidirectional switch in a custom-package was proposed in [214]. It was demonstrated that low stray inductance can be obtained in a compact design.

Due to its large current rating, IGBTs have been extensively applied in matrix converters for high-power applications [215]. Wide-bandgap semiconductors (WBG) are semiconductor materials which have a relatively large band gap compared to silicon. This feature permit devices to operate at much higher voltages, switching frequencies and junction temperatures than conventional semiconductor materials [216]. Emerging technologies, such as Silicon Carbide (SiC) and Gallium Nitride (GaN) power devices are examples of WBG semiconductor. SiC power devices have been investigated extensively in the past two decades, and there are many devices commercially available now [217]. These devices are becoming closer to “ideal” switches, which can have a huge impact in the miniaturization of power electronic converters for the transportation and renewable energy sectors [65, 216–220].



(a) Common-source configuration. **(b)** Common-drain configuration. **(c)** Diode bridge with a controlled switch. **(d)** Reverse voltage blocking switches.

Figure 3.23: Example of possible configurations to build the bidirectional switch.

There are several possibilities to build the bidirectional switch by combining diodes and transistors. The more commonly used configurations are represented in Figure 3.23. The anti-series connection of two MOSFETs in common-source or common-drain configuration is shown in Figure 3.23(a) and Figure 3.23(b) respectively. The intrinsic body diode of each MOSFET creates a path for the backward current and simultaneously block the reverse voltage applied to the opposite transistor [221]. An advantage of the common-source arrangement is requiring only one isolated power supply for both gate driver circuits of the bidirectional switch. Eventually, the common-drain configuration could require even less isolated power supplies if combined at the converter topology level.

Another approach is to associate a diode bridge with a controllable switch as depicted in Figure 3.23(c). In this configuration, the current flows forward an reverse using the same transistor which is an interesting solution considering the costs and complexity [212]. Nevertheless, the simultaneous conduction of two diodes and one transistor result in higher conduction losses when compared with the previous solutions. Moreover, it is not possible to control the direction of the current which is required by some commutation.

The reverse blocking IGBT (RB-IGBT) was created with the aim of obtain a bidirectional switch with a smaller voltage drop when compared with the previously presented solutions [222]. The RB-IGBT has a symmetrical blocking voltage characteristic and is capable to control the forward current. A bidirectional switch can be arranged with the anti-parallel connection of two RB-IGBTs, as depicted in Figure 3.23(d). Since there is no external diode connected in series, a small voltage drop is obtained reducing in this way the conduction losses. However, the reverse recovery current of the internal diode is greater when compared to standard fast freewheeling diodes (FWD) [223]. Discrete bidirectional RB-IGBTs are not commonly available in the market. Typically this type of semiconductors are provided in power modules in the dozens or hundreds of kWs range. For example, Fuji Electric has RB-IGBT based three-level NPC power modules in its

portfolio [224].

Ideal Power has developed a patented technology to implement the bidirectional switch known as B-TRAN: Bi-directional Bi-polar Junction Transistor. According to the manufacturer, the B-TRAN has the same three-layer PNP or NPN structure of the IGBT, but has a control switch on each side [225]. This double-sided switch arrangement has identical behaviour in each direction, enabling it to block voltage or conduct current in each direction with equal performance.

Considering the alternatives described above, the common-source configuration is typically preferred to build the bidirectional switches for matrix converters [146, 212].

3.4 Commutation strategies

Ideally, the commutation among possible states of power electronics converters should occur instantaneously and simultaneously. In practice, such conditions are impossible to achieve due to nonzero switching times, delays, and differences between rise and fall times of the power semiconductors. To illustrate the commutation problems in matrix converters, a simple circuit with three bidirectional switches is shown in Figure 3.24. S_{aX}, S_{bX}, and S_{cX} connect, respectively, voltage sources V_{ga}, V_{gb}, and V_{gc} with a RL load. These bidirectional switches are composed by two MOSFETs in common-source configuration but the following analysis is equivalent for the other constructive approaches discussed in Section 3.3. Proper current commutation in matrix converters requires that one, and only one, bidirectional switch on each output leg be ON at any given time [226]. Overcurrents due to short-circuit between voltages sources or overvoltages due to current interruption in inductive loads can occur due to incorrect command sequence.

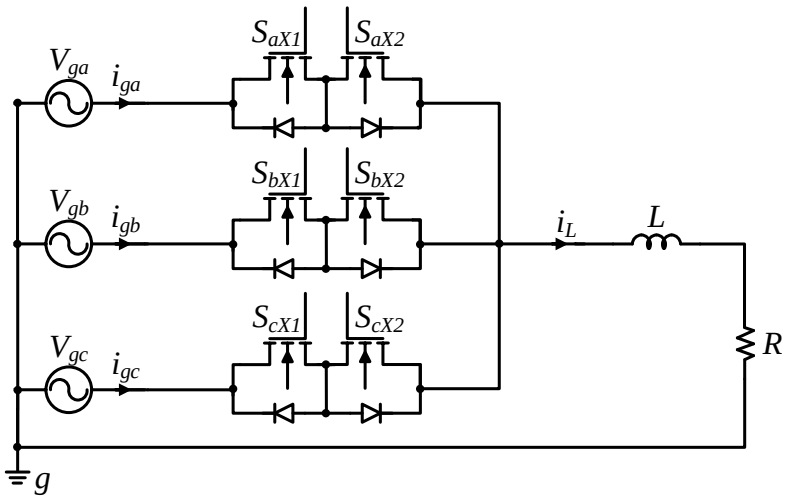


Figure 3.24: Basic commutation circuit with three bidirectional switches and an RL load.

Suppose that S_{aX} (S_{aX1}, S_{aX2}) is *ON* and conducts the load current i_L. It is intended to commutate the current to S_{bX}. Since there is no freewheeling path for the current, it is difficult to perform a commutation without generating overvoltages or overcurrents [227]. For example, if S_{bX} is *ON* before S_{aX} be completely *OFF*, a short-circuit will occur between voltage sources V_{ga} and V_{gb}. The resulting peak current can potentially destroy the power semiconductors [211, 228]. An approach to limit the current rise can be implemented by adding extra inductances between the bidirectional switches and the voltage sources [146]. However, the additional volume occupied by the inductances and the higher switching losses make this approach not practical. In other way, if S_{aX} is turned off before S_{bX} start conducting, there will be not a path for i_L. The sudden interruption of the inductive current will generate an overvoltage that can also lead to the destruction of the power semiconductors [211, 228]. In order to mitigate the problems originated by the current commutation, snubber or clamping circuits can be inserted at the switches terminals. Nevertheless, this method rise the energy lost during each commutation and also increase the volume of the converter [146].

In order to construct a reliable matrix converter it is important to overcome the problem of commutating the current path between the bidirectional switches [226, 229]. Several methods have been proposed to solve the commutation problem by generating a proper switching sequence for the four-quadrant switches of the matrix converter. These methods rely on knowledge of either the relative magnitude of the input voltages or the current direction in each output leg of the converter [226]. Basically, a multi-step strategy avoid the conditions that can generate overvoltages or overcurrents by complying with the two fundamental rules previously defined in Section 3.1.2.

Table 3.11 enumerate the safe states of the bidirectional switches based on current direction. Regarding the state of switches, *1* is used to represent the *ON* mode and *0* to represent the *OFF* mode. State 1, 2, and 3 are unconditional states, which means that can be activated at any time. For that reason, each switching sequence begins and ends at one unconditional state. In other way, state 4 to 15 are conditional states and can only be activated when the current direction is in accordance with the signal of the last column of Table 3.11. A direct transition between unconditional states is not possible due to the commutation problem. Nevertheless, by combining the conditional states with the unconditional states in a proper sequence, it is possible to create a current commutation strategy.

The same analysis can be done regarding Figure 3.24 but now considering the relative magnitude of voltage sources V_{ga}, V_{gb}, and V_{gc}. For simplicity, only S_{aX} and S_{bX} are considered but the same analysis can be extended to include S_{cX}. Table 3.12 enumerate the safe states of the bidirectional switches based on relative voltage magnitude. State 1 and 2 are unconditional states, which means that can be activated at any time. For that reason, each switching sequence begins and ends at one unconditional state. In other way, state 3 to 8 are conditional states and can only be activated when the relative voltage

Table 3.11: Safe states of the bidirectional switches based on current direction [230].

State	S_{aX1}	S_{aX2}	S_{bX1}	S_{bX2}	S_{cX1}	S_{cX2}	$\mathbf{sgn}(i_L)$
1	1	1	0	0	0	0	$\pm$
2	0	0	1	1	0	0	$\pm$
3	0	0	0	0	1	1	$\pm$
4	1	0	0	0	0	0	$+$
5	0	1	0	0	0	0	$-$
6	0	0	1	0	0	0	$+$
7	0	0	0	1	0	0	$-$
8	0	0	0	0	1	0	$+$
9	0	0	0	0	0	1	$-$
10	1	0	1	0	0	0	$+$
11	0	1	0	1	0	0	$-$
12	0	0	1	0	1	0	$+$
13	0	0	0	1	0	1	$-$
14	1	0	0	0	1	0	$+$
15	0	1	0	0	0	1	$-$

Table 3.12: Safe states of the bidirectional switches (S_{aX} and S_{bX} only) based on relative magnitude of the input voltages [228].

State	S_{aX1}	S_{aX2}	S_{bX1}	S_{bX2}	$\mathbf{sgn}(V_{ga} - V_{gb})$
1	1	1	0	0	$\pm$
2	0	0	1	1	$\pm$
3	1	1	1	0	$+$
4	1	1	0	1	$-$
5	0	1	1	1	$+$
6	1	0	1	1	$-$
7	0	1	1	0	$+$
8	1	0	0	1	$-$

magnitude is in accordance with the signal of the last column of Table 3.12.

In the following sections, some commutation strategies based on current direction or relative magnitude of the input voltages are detailed.

3.4.1 Current-based commutation strategies

The first current-based commutation (CBC) strategy was proposed by Burány in 1989 [228]. Each commutation sequence is composed by two unconditional and three conditional states. This method was named "four-step" commutation strategy because there are four transitions between the states.

The direction of output current can be difficult to measure, particularly at zero crossing areas where traditional current sensors such as Hall effect probes are prone to producing uncertain results. The misjudgement of output-current direction in the commutation process will lead to an open circuit of the inductive load current and then cause overvoltage on the matrix converter [226, 229]. Two main approaches were proposed to deal with the uncertainties associated with the current direction detection. The first approach consists to add a clamp circuit to absorb the overvoltage spikes. This circuit is typically composed by one or two diode bridges, a crowbar, and a clamp capacitor as detailed in [231, 232]. By continuously measuring the voltage across the clamp capacitor it is possible to detect that the failure has occurred [226]. With this information, the converter can be safely turned-off to prevent damages to the system. If the energy stored in the inductive load is not so high, one simple and low-cost solution can be implemented by placing varistors across the input and output phases of the MC. A carefully selected varistor is able to stand the stress for more than 1 million pulse-off cycles which is enough compared to the lifetime of the converter [233]. In [234], the authors propose to implement an hysteresis function in the controller to detect the current direction for the IMC. The second approach to deal with the low current-direction uncertainty is to measure the voltage drop of each power transistor. This function can be incorporated within the gate driver circuit of each bidirectional switch and by establishing a communication link with the other drivers. However, this analog circuitry is complex and expensive. With this additional information, only the switch carrying the current has command signal at any given time. Once the precise output-current direction is obtained, fast and reliable two-step CBC is possible to accomplish [147, 235].

If the turn-off delay time of the devices used for the bidirectional switches is greater than the turn-on delay under all possible operating conditions then the commutation time, t_c, can be reduced to zero for one conditional state of the switching sequence. Following this idea, a three-step commutation strategy was introduced by Wheeler et al. [226] in order to minimize the output-voltage distortion. Therefore, the required commutation time is always considerably lower than the corresponding t_c for a relative input voltage magnitude based commutation strategy. This is a very significant advantage of input-current-direction-based commutation strategies [226]. Following the same approach, the corresponding two-step current commutation strategy can be reduced to a single-step current commutation strategy.

An extensive review of commutation strategies can be found in [146, 149]. A comparative analysis of the different strategies is presented in [150] using the total harmonic distortion (THD), the converter efficiency, the maximum commutation frequency and the necessary hardware requirements for the implementation as comparison criterion.

Four-step commutation strategy or Semi-soft Commutation

The four-step commutation was the first strategy to be proposed for the MC. It is probably the most used and reliable current-based commutation strategy. By having additional switches with command signal, it is possible to provide a path for the load current without short circuiting the input phases [147].

Please refer to Figure 3.24. If S_{aX1} and S_{aX2} are *ON*, current i_L will flow through one of the MOSFETs accordingly to the current direction. Supposing that it is intended to transfer the current to S_{bX} (S_{bX1} and S_{bX2}), the commutation problem described before will occur. Since it is not possible to simultaneously turn-off S_{aX1} and S_{aX2}, and turn-on S_{bX1} and S_{bX2}, a proper switching sequence need to be implemented. It will be considered that $i_L > 0$, thus the current is flowing through S_{aX1} and the body diode of S_{aX2}. When a commutation is required the non-conducting device, S_{aX2}, is switched off as represented in Figure 3.25. Then, the transistor that will carry the current after commutation, S_{bX1}, is then switched on. This allows that both switches are *ON* without provoking a short-circuit between voltage source A and B while provide a path for the load current. A short time later S_{aX1} is turned off and the current immediately commutates to S_{bX1}. Finally, S_{bX2} is turned on to complete the switching sequence. Commutation time, t_c, should be defined considering the switching characteristics of the transistor in use and the delays in the command circuits [146, 236]. Typically, t_c is higher than the rise and fall time of the MOSFET and also includes the turn-on and turn-off delay.

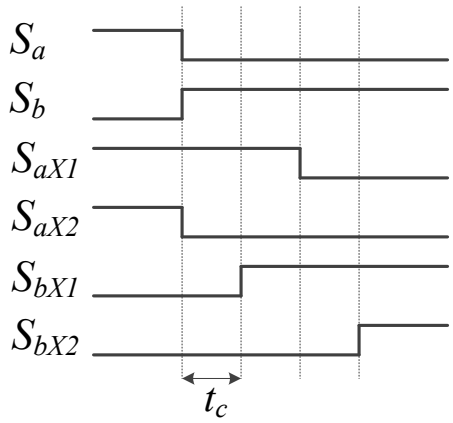


Figure 3.25: Timing diagram for the *four-step* commutation strategy with $i_L > 0$.

This logic sequence is also valid when the current has the inverse direction being only required to select the respective transistors. Figure 3.26 shows the state diagram for the commutation between S_{aX} and S_{bX} as a function of the current direction.

This commutation strategy allows ZCS of the transistors if the outgoing device is reverse biased by the turning on of the incoming device. This situation will occur when the phase voltage of the incoming switch is greater than the phase voltage of the outgoing

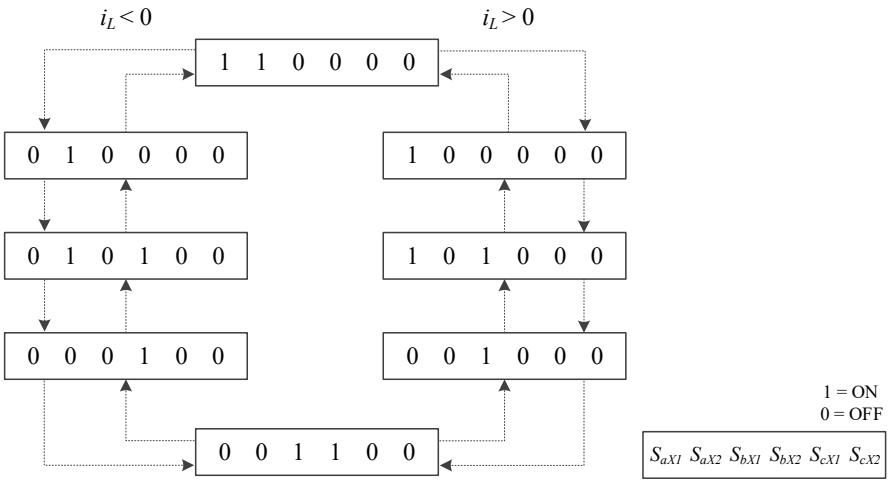


Figure 3.26: State diagram for the *four-step* commutation strategy.

transistor in the conduction path [236]. Since there is a 50% chance of occurring a reverse bias, the switching losses are reduced by half using this method. For this reason, the four-step commutation is also known as 'semi-soft current commutation' since half the switching operations are achieved by natural or soft-switching. This method was also experimentally validated in a high-frequency three-phase bi-directional rectifier [230].

3.4.2 Voltage-based commutation strategies

Voltage-based commutation (VBC) strategies rely on the knowledge of the relative magnitude of input voltages [229]. The philosophy is to provide a freewheeling path by keeping transistors with command signal except those required for voltage blocking [226].

The basic four-step VBC strategy was proposed by Mahlein *et al.* [149] and is similar to the current-based one. If the relative voltage between two input phases is unclear, this method can ensure a safe and reliable commutation by implementing two two-step commutations via the third phase. Moreover, neither the average value of input current nor the average value of the output voltage is influenced [237]. However, it will double the commutation time and the switching loss and lead to output-voltage/current distortion, particularly at low-output-voltage conditions [229].

Another VBC strategy was proposed by Ziegler and Hofmann [213], which was named METZI commutation. It is based on the basic operating principle of providing a freewheeling path for both output current directions at any given time [238]. This can be accomplished by using more active devices in either steady or transient states. As a result, this method forms a fast two-step commutation strategy and enables semi-soft switching. For these reasons, the METZI method is considered one of the best commutation strategies [239]. Other two-step commutation approaches were proposed by Youm and Kwon [148], and Wei et al. [240].

The voltage sign measurement is typically done before the input filter for better voltage sampling and reducing the influence caused by transistors switching [237]. However, the relative magnitude of the input voltages can be difficult to measure, particularly at zero crossing areas of the line-to-line voltage [229]. Therefore, the sign detection circuit has to meet high demands and must be very precise, making it difficult to design specially if connected directly at the input of the MC. If the relative magnitude of the input voltages is misjudged and a commutation failure occurs then a short circuit between the input lines of the converter will occur, which can lead to destruction of the converter [226].

To prevent problems in the critical interval, Ziegler and Hofmann proposed an alternative method that modifies the main and commutation switching states [241]. The new switching patterns allow the operation as a two-step commutation strategy. A similar approach was proposed by Ecklebe *et al.* [242] and by Wang *et al.* [237, 243]. Nevertheless, the main disadvantage is that the input current will differ from the ideal sinusoidal since the calculated pulse patterns will not be executed.

An improved method to solve the problems related with current commutation in critical intervals was proposed by She *et al.* in [239] and further detailed in [229]. In every critical interval, the basic four-step strategy is employed for commutation between two input phases with unclear relative voltage. In normal intervals, the two-step METZI method is utilized for commutation between two input phases with clear relative voltage. This method enables the commutation between any two of the input phases in any intervals, and for this reason it is suitable for any kinds of modulation algorithms [229].

METZI commutation strategy

As previously discussed, the METZI commutation ensures that at each moment the maximum number of switches is turned on. With this approach, a fast two-step commutation with semi-soft switching is achieved.

This method is based on the detection of the six 60° intervals (I, II, III, IV, V, VI) of the three-phase grid voltages where the line-to-line voltages do not change their relative magnitude. Figure 3.27 depicts the normal intervals along with the voltages over one period of the grid. In every interval, one phase has the highest voltage V_P, one the lowest V_N, and one the middle V_M. For example, in interval III the highest voltage V_P corresponds to V_b, the lowest V_N to V_a, and the middle V_M to V_c.

Six switching states are defined by this commutation strategy: three major states (P, M, N) and three intermediate states (PM, MN, NP) for each output phase, as shown in the state diagram in Figure 3.28. A commutation from one major state to another target major state is accomplished in two steps:

Step 1: turn off all switches which will not be switched on in the target major state; the intermediate state will be reached;

Step 2: turn on the switches of the target major state; the target state will be reached.

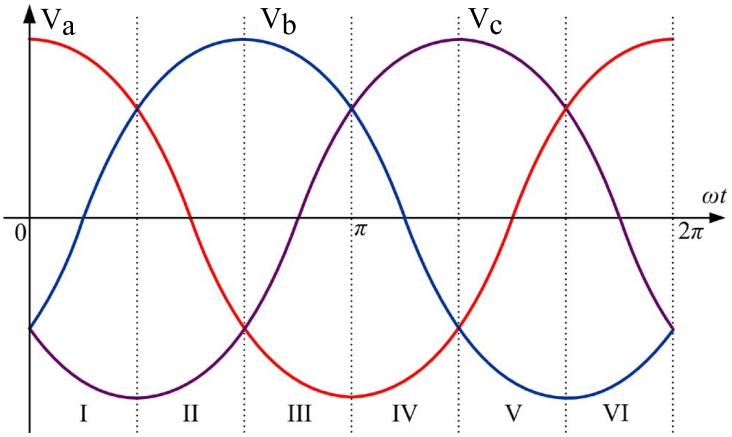


Figure 3.27: Normal intervals of the three-phase grid voltages [229].

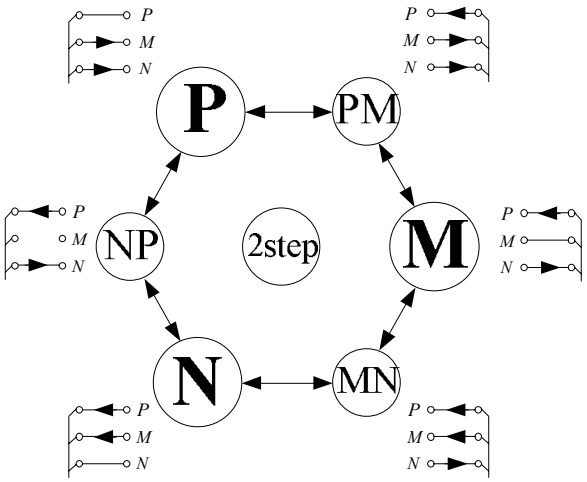


Figure 3.28: METZI commutation sequence [239].

As can be seen, four of the six switches are turned on in every major state. Two switches are turned on to ensure a bi-directional path for the load current, and the redundant two switches are turned on for two-step commutation. Table B.1 and Table B.2 from Appendix B detail the command signals for each bidirectional switch S_{aX}, S_{bX}, and S_{cX}.

The METZI commutation could work reliably if the relative magnitude of input voltages is accurately known, as shown in Figure 3.28. However, problems may arise near the boundary of two adjacent normal intervals, in which two of the input voltages are similar. If the relative magnitude of input voltages is misjudged, a line-to-line short circuit path is established through the redundant switches, even if no commutation happens [229]. Table 3.13 shows a detailed short circuit analysis when the relative magnitude of input voltages is misjudged in the critical intervals.

The possibility of misjudgement becomes amplified at zero crossing areas of input line-to-line voltage, since the input voltages of the matrix converter may be distorted because

Table 3.13: Short circuit analysis when the relative magnitude of input voltages is misjudged in the critical intervals. [237].

State	$V_P \approx V_M$	$V_M \approx V_N$
P	short circuit in phase P and M	do not lead to short circuit
PM	short circuit in phase P and M	do not lead to short circuit
M	short circuit in phase P and M	short circuit in phase M and N
MN	do not lead to short circuit	short circuit in phase M and N
N	do not lead to short circuit	short circuit in phase M and N
NP	do not lead to short circuit	do not lead to short circuit

of the high-frequency switching of the power semiconductors. Therefore, the VBC strategy should be improved in these intervals to ensure reliable and safe commutations.

Variable-step VBC strategy

To overcome the limitations of the METZI commutation strategy near the boundary of two adjacent normal intervals, an improved method was proposed by She *et al.* in [239] and further detailed in [229]. This method inserts six critical intervals (I-II, II-III, ..., VI-I) between the six normal intervals, as shown in Figure 3.29. In each critical interval, two of the input voltages are similar and their relative magnitude is difficult to be distinguished. Critical intervals can be classified in two types: H-type and L-type. In H-type critical intervals, two input voltages are similar and are both higher than the third one (I-II, III-IV, and V-VI). In other way, in L-type critical intervals, two input voltages are close and are both lower than the third one (II-III, IV-V, and VI-I). The variable-step VBC strategy applies the two-step METZI method in normal intervals for the commutation between two input phases with clear relative voltage. In every critical interval, the basic four-step strategy is employed for commutation between two input phases with unclear relative voltage. With this approach, the critical sequence is replaced by two uncritical sequences which will perform a commutation to the remaining third input phase and then to the desired target major state, as represented in Figure 3.30.

Comparing this diagram with the one in Figure 3.28, it can be concluded that less transistors have command signal within the critical intervals. Basically, some of the redundant switches that can create a short circuit for the other phase are not activated. Table B.3 and Table B.4 from Appendix B detail the command signals for each bidirectional switch S_{aX}, S_{bX}, and S_{cX} within critical intervals. Lets analyse in detail the four-step commutation from P to M major state in H-type critical interval [229, 239]:

Initial state P: the two unidirectional switches in input phase P are both on, and the two unidirectional switches in phase M are both off. With this arrangement, there will no short circuits even if the voltage of phase M is higher than that of phase P.

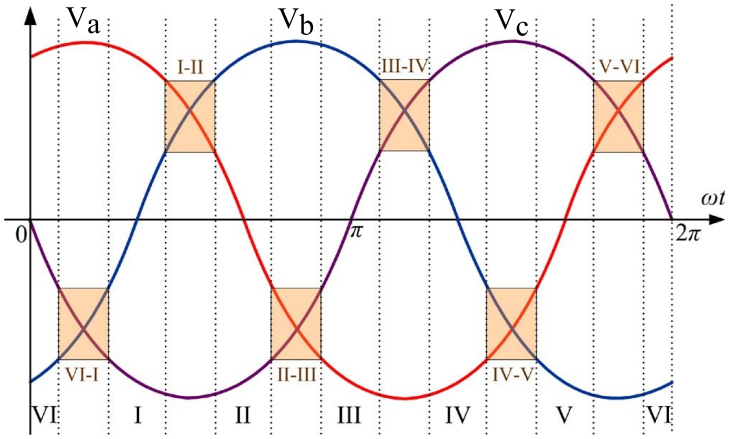


Figure 3.29: Normal and critical intervals of the three-phase grid voltages [229].

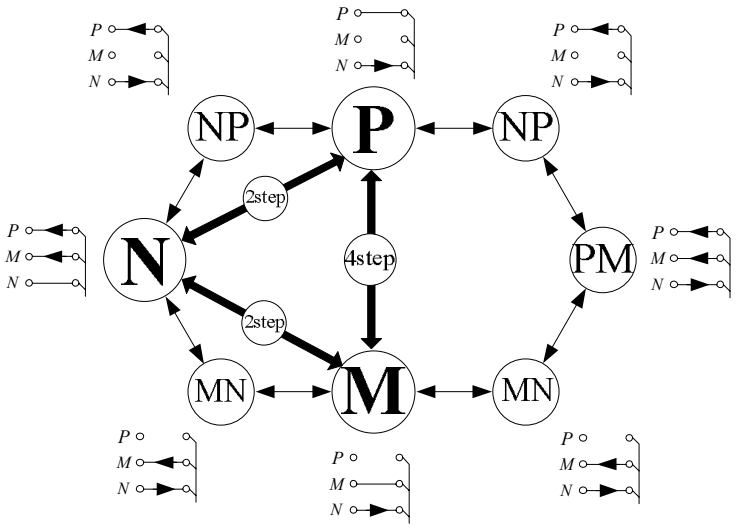


Figure 3.30: Variable-step commutation sequence in H-type critical interval [239].

The forward switch of phase N is on to provide a positive load current freewheeling path;

Step 1, intermediate state NP: the forward switch of phase P is turned off;

Step 2, intermediate state PM: the reverse switch of phase M is turned on;

Step 3, intermediate state MN: the reverse switch of phase P is turned off;

Step 4, target state M: the forward switch of phase M is turned on. Thus, the unidirectional switches in input phase M are both on, the unidirectional switches in input phase P are both off, and the forward switch of input phase N is still on to provide positive load current freewheeling path.

If the load current is positive, the load current is freewheeled by the forward switch of phase N, from the first step to the fourth step and then commutated to the target phase. Otherwise, if the load current is negative, the load current will commutate to the target phase in the second or third step upon the actual relative magnitude of phase P and phase M. This is an improvement with respect to the two two-step commutation approaches since the probability of the third phase freewheeling is reduced by half [229]. The critical intervals should be wide enough to cover the uncertain areas. However, the number of four-step critical commutations will be increased with the widening of the critical intervals and thus results in increase of the output-voltage distortion and switching losses.

The critical four-step commutation diagram in L-type critical intervals could be obtained by a similar approach. In this case, the reverse switch of the third phase should be switched on for negative load current freewheeling. Therefore, the variable-step VBC strategy can be implemented with any kinds of modulation algorithms for matrix converters, without the need of explicit input-voltage measurement [229]. By properly changing between the two-step uncritical commutation and four-step critical commutation methods, a safe VBC strategy with minimum switching losses is ensured.

3.4.3 Hybrid commutation strategies

The hybrid commutation (HC) strategies rely on both information about the relative magnitude of input voltages and information about the output-current direction.

Sun *et al.* proposed a two-step HC strategy based on the explicit output current and input voltage detection by measuring the voltage drop on each bidirectional switch [244]. The main disadvantage of this method is the complex measurement hardware requirement similar to the two-step current-based approach [147, 235].

A fast one-step HC strategy was also proposed by Ziegler and Hofmann [245]. However, it is very difficult to be implemented since explicit measurements of the output current and input voltage are both required.

3.5 Conclusion

In this chapter was presented a detailed review of the Direct Matrix Converter and Indirect Matrix Converter along with the implementation issues associated with the current commutation.

The Space Vector Modulation is probably the most used modulation strategy for the DMC and IMC due to its low computation requirements and high flexibility.

Considering the constructive approaches to build the bidirectional switch, the common-source configuration seems to be the right choice since allows to reduce the number of isolated power supplies.

Regarding current commutation, the voltage-based commutation seems to be the more practical solution for the matrix converter since it just requires simple and low-cost measurement hardware. Moreover, the variable-step VBC strategy is more attractive for practical matrix-converter implementation since allows to perform safe commutations in the critical intervals.

Part II

Implemented Design

Chapter 4

High-frequency Link Matrix Converter

4.1 Introduction

The high-frequency link matrix converter (HFLMC) represented in Figure 4.1 is the scope of this chapter. As discussed in Section 2.6, the HFLMC has the potential to achieve higher power density with longer service life when compared with conventional topologies. However, the state of the art modulations proposed for the HFLMC are not capable to regulate current and voltage in the DC side and simultaneously adjust the power factor at the AC side, which are essential for the operation of a CES unit.

In this chapter, a new modulation strategy for the HFLMC based on SVM and PSM is proposed. This modulation allows to simultaneously control the power factor in the grid interface, and the voltage and current in the battery pack. Active and reactive power (PQ) control method can also be implemented to provide services for the grid operator. The grid currents controller is formulated in the *dq* reference frame for decoupled grid currents regulation. Finally, a detailed simulation is performed to test and validate the modulation and the controllers proposed for the HFLMC.

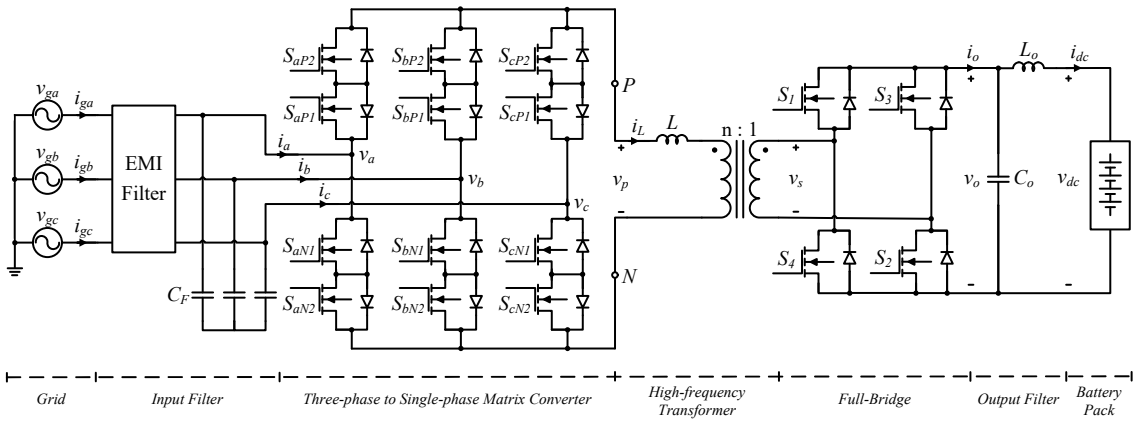


Figure 4.1: Circuit schematic of the high-frequency link matrix converter (HFLMC).

Table 4.1: Feasible switching states of the 3×2 MC.

State	S_{aP}	S_{bP}	S_{cP}	S_{aN}	S_{bN}	S_{cN}	v_p	i_a	i_b	i_c	SSV
1	1	0	0	0	1	0	V_{ab}	i_L	-i_L	0	I_1
2	1	0	0	0	0	1	-V_{ca}	i_L	0	-i_L	I_2
3	0	1	0	0	0	1	V_{bc}	0	i_L	-i_L	I_3
4	0	1	0	1	0	0	-V_{ab}	-i_L	i_L	0	I_4
5	0	0	1	1	0	0	V_{ca}	-i_L	0	i_L	I_5
6	0	0	1	0	1	0	-V_{bc}	0	-i_L	i_L	I_6
7	1	0	0	1	0	0	0	0	0	0	I_7
8	0	1	0	0	1	0	0	0	0	0	I_8
9	0	0	1	0	0	1	0	0	0	0	I_9

4.2 Proposed Modulation

Since the MC is fed by a voltage source, only one input phase may be connected to each P or N bar in Figure 4.1 at a time. On the other hand, the inductive nature of the transformer makes it impossible to interrupt the i_L current suddenly, and therefore, at least one switch must be connected to each bar. Considering these constraints, the 3×2 MC has only nine feasible switching states which are summarized in Table 4.1. Regarding the state of the switches S_{xy}, *1* is used to represent the *ON* mode and *0* is used to represent the *OFF* mode. Each switching state of the MC specifies one input current switching space vector. The current SSVs have fixed directions and are $\pi/3$ radians evenly spaced in the $\alpha\beta$ reference frame. Sector numbers 1 to 6, represented by K, are assigned for the spaces between two adjacent SSVs. Figure 4.2 shows the SSVs along with the instantaneous representation of the input voltage ($\bar{v}_i$) and input current ($\bar{i}_i$) space vectors in the $\alpha\beta$ reference frame. Each complex space vector is obtained through multiplication of respective *abc* components by a proper unitary complex phase shifter [166]. A symmetric three-phase voltage system with angular frequency ω_i and amplitude V_i is assumed as defined by (4.1). The instantaneous input voltage space vector $\bar{v}_i$ with angle $\alpha_i = \omega_i t$ is obtained from (4.1) using (4.2). In the following analysis, the input filter dynamic is considered negligible. Additionally, the grid is modeled by an ideal three-phase AC voltage source.

$$\begin{aligned} v_a(t) &= V_i \cos(\omega_i t) \\ v_b(t) &= V_i \cos\left(\omega_i t - \frac{2\pi}{3}\right) \\ v_c(t) &= V_i \cos\left(\omega_i t + \frac{2\pi}{3}\right) \end{aligned} \tag{4.1}$$

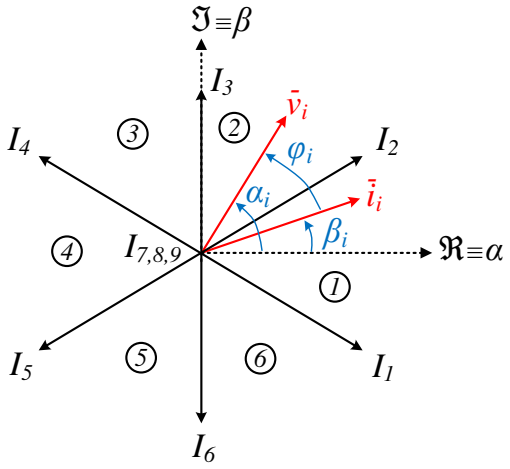


Figure 4.2: Representation of the input current SSVs in the $\alpha\beta$ reference frame along with the instantaneous voltage and current space vectors.

$$\bar{v}_i = \frac{2}{3}\left(v_a(t) + v_b(t)e^{j\frac{2\pi}{3}} + v_c(t)e^{j\frac{4\pi}{3}}\right) = V_i e^{j\alpha_i} \tag{4.2}$$

At any given sampling instant, the displacement angle φ_i between $\bar{i}_i$ and $\bar{v}_i$ is a reference for the modulation. Therefore, power factor can be controlled by the phase angle β_i of the desired input current vector $\bar{i}_i^*$, as in (4.3).

$$\beta_i = \alpha_i - \varphi_i \tag{4.3}$$

Input current $\bar{i}_i$ is formed by the local average, over a modulation period T_s, of each input phase current as represented in (4.4). The SVM is then based on the selection of space vectors in order to approximate $\bar{i}_i$ to $\bar{i}_i^*$ as described by (4.5).

$$\begin{aligned}
\langle i_a\rangle_{Ts} &= I_i \cos\left(\omega_i t - \varphi_i\right) \\
\langle i_b\rangle_{Ts} &= I_i \cos\left(\omega_i t - \frac{2\pi}{3} - \varphi_i\right) \\
\langle i_c\rangle_{Ts} &= I_i \cos\left(\omega_i t + \frac{2\pi}{3} - \varphi_i\right)
\end{aligned} \tag{4.4}$$

$$\bar{i}_i^* = \frac{2}{3}\left(\langle i_a\rangle_{Ts} + \langle i_b\rangle_{Ts}e^{j\frac{2\pi}{3}} + \langle i_c\rangle_{Ts}e^{j\frac{4\pi}{3}}\right) = I_i e^{j\beta_i} \tag{4.5}$$

The two adjacent nonzero SSVs (I_K) are selected as represented in Fig 4.3. θ_i is the angle of $\bar{i}_i^*$ within the actual sector, which can be calculated by (4.6). Vector $\bar{i}_i^*$ is decomposed into components $\bar{i}_\gamma$ and $\bar{i}_\sigma$ along the two adjacent current SSVs (4.7). θ_i is measured with respect to the SSV associated with the $\bar{i}_\gamma$ vector. For this example, space vectors I_1 and I_2 are used to synthesize $\bar{i}_\gamma$ and $\bar{i}_\sigma$ by considering the proper duty cycles d_γ and d_σ respectively. This is valid for sector 1 but can be derived by symmetry for the other

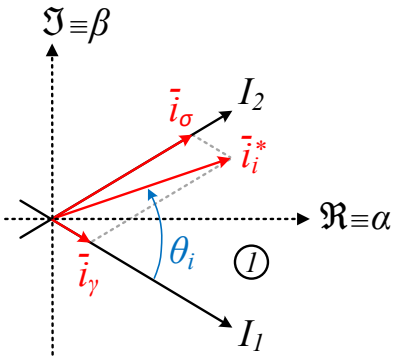


Figure 4.3: Synthesis of the desired current space vector $\bar{i}_i^*$ in sector 1.

sectors in the $\alpha\beta$ reference frame without loss of generality.

$$\theta_i = \beta_i - K\frac{\pi}{3} + \frac{\pi}{2} \tag{4.6}$$

$$\begin{aligned} \bar{i}_i^* &= \bar{i}_\gamma + \bar{i}_\sigma \\ \bar{i}_\gamma &= d_\gamma I_1 \\ \bar{i}_\sigma &= d_\sigma I_2 \end{aligned} \tag{4.7}$$

Duty cycles for the two general switching states are calculated using the relationships in (4.8a) and (4.8b), where $m_{\gamma\sigma}$ is the basic modulation index used to adjust the amplitude I_i of $\bar{i}_i^*$. The zero space vectors (I_z=I_7, I_8 or I_9) are used to complete the modulation period, whose duty cycle is calculated by (4.8c). Since $d_{0\gamma\sigma} \geq 0$, $d_\gamma \geq 0$, and $d_\sigma \geq 0$, the maximum basic modulation index is limited to 1, so $0 \leq m_{\gamma\sigma} \leq 1$.

$$\begin{aligned} d_\gamma &= m_{\gamma\sigma} \sin\left(\frac{\pi}{3} - \theta_i\right) \\ d_\sigma &= m_{\gamma\sigma} \sin\left(\theta_i\right) \\ d_{0\gamma\sigma} &= 1 - d_\gamma - d_\sigma \end{aligned} \tag{4.8}$$

The HFL operation requires an AC voltage with a balanced positive and negative volt-seconds at the transformer terminals. Small mismatches in inductor applied volt-seconds can have significant impact on circuit operation, including the saturation of magnetic components, loss of regulation, and decrease in converter efficiency [246]. Several techniques have been proposed to deal with DC offset of the magnetizing flux in high-frequency transformers [246–248]. For this analysis, it is considered that the amplitude of v_p and v_s is constant during one period of modulation, $T_s = 1/f_s$. In practice, this can be approximately achieved if the switching frequency is sufficiently higher when compared to the grid frequency, ω_i. Following this requirement, the proposed modulation for the HFLMC

combines the space vector approach with the phase-shift modulation. The MC applies the nonzero SSVs of Table 4.1 in a square wave fashion in order to ensure a proper flux balance in the HFT. The modulation period of v_p can be divided into five intervals as represented in Figure 4.4(a). First and second intervals have the same duration ($d_1 T_s/2$) and apply the SSV associated to the $\bar{i}_\gamma$ component. These pulses have amplitude V_1 which has correspondence to voltage v_p in Table 4.2. For example, if the current reference $\bar{i}_i^*$ is in sector 1, then I_1 and I_4 space vectors are selected. In the following analysis will be considered $t_0 = 0$. Space vector I_1 is applied until instant t_2, and then space vector I_4 is applied until instant t_4, as defined in (4.9). The third and fourth intervals are symmetric ($d_2 T_s/2$) and apply the SSV associated to the $\bar{i}_\sigma$ component. For sector 1, space vector I_2 is applied between instant t_4 and t_6, and space vector I_5 is applied between instant t_6 and t_8. Finally, one of the zero SSVs (I_z=I_7, I_8 or I_9) is applied during the fifth interval, between instant t_8 and T_s, to complete the modulation period. There are several possibilities from where to choose the zero vectors, since all apply the same voltage to the transformer. Table 4.2 shows the zero vectors to be used in each sector in order to minimize the number of commutations.

$$\begin{aligned} t_2 &= \frac{d_1}{2} T_s \\ t_4 &= d_1 T_s \\ t_6 &= \left(d_1 + \frac{d_2}{2} \right) T_s \\ t_8 &= (d_1 + d_2)\, T_s \end{aligned} \tag{4.9}$$

FB impresses a voltage v_s in the transformer winding with a phase-shift, ϕ, respecting to v_p. The phase-shift is limited by (4.10), and can be normalized as (4.11) by making $\delta = \phi / \frac{\pi}{2}$.

$$-\frac{\pi}{2} \leq \phi \leq \frac{\pi}{2} \tag{4.10}$$

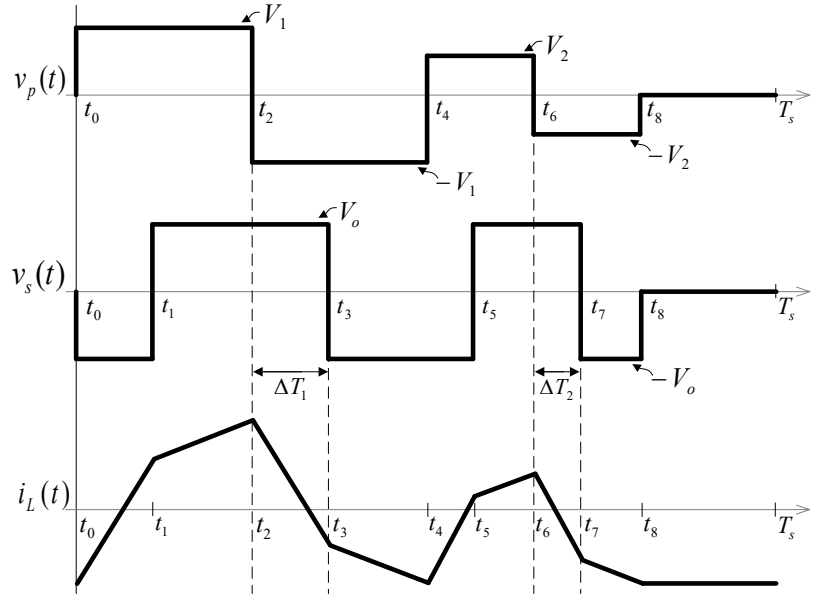
$$-1 \leq \delta \leq 1 \tag{4.11}$$

Table 4.3 shows the four feasible switching states of the FB converter. Positive pulse between instant t_1 and t_3 (4.14) is phase-shifted by ΔT_1 (4.12) relatively to the first positive pulse of v_p. State 11 ($S_1, S_2 = 1$) is used to apply $v_s = V_o$, which corresponds to the average output voltage. The same approach is employed for the second positive pulse between instant t_5 and t_7, which is phase-shifted by ΔT_2 (4.13) relatively to the second positive pulse of v_p.

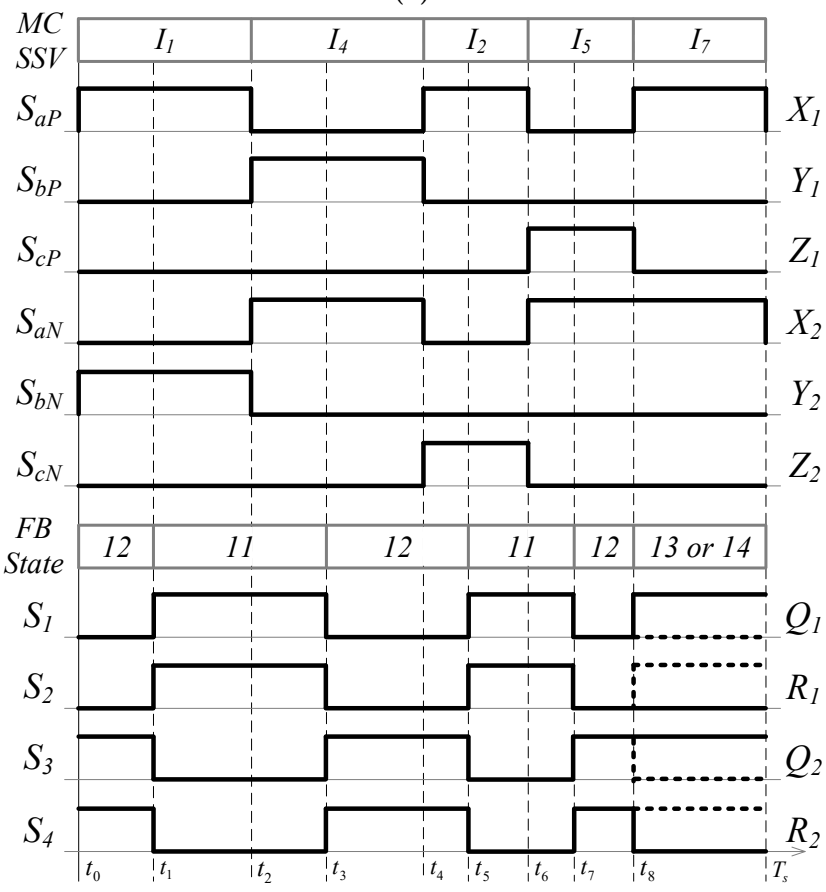
$$\Delta T_1 = \frac{\delta}{2} \frac{d_1}{2} T_s \tag{4.12}$$

$$\Delta T_2 = \frac{\delta}{2} \frac{d_2}{2} T_s \tag{4.13}$$

Negative pulses are applied during intervals $[t_0, t_1]$, $[t_3, t_5]$ and $[t_7, t_8]$ using state 12



(a)



(b)

Figure 4.4: (a) Modulation principle in charger mode: voltages v_p, v_s, and transformer primary current (i_L). (b) Example of command signals for the MC and FB under positive phase-shift and sector 1.

Table 4.2: SSVs and corresponding voltage v_p applied by the MC.

Sector	Duty cycle	Positive pulse		Negative pulse		Zero
		SSV	$\boldsymbol{v_p}$	**SSV**	$\boldsymbol{v_p}$	**SSV**
1	d_1	I_1	V_{ab}	I_4	$-V_{ab}$	I_7
	d_2	I_2	$-V_{ca}$	I_5	V_{ca}	
2	d_1	I_2	$-V_{ca}$	I_5	V_{ca}	I_9
	d_2	I_3	V_{bc}	I_6	$-V_{bc}$	
3	d_1	I_3	V_{bc}	I_6	$-V_{bc}$	I_8
	d_2	I_4	$-V_{ab}$	I_1	V_{ab}	
4	d_1	I_4	$-V_{ab}$	I_1	V_{ab}	I_7
	d_2	I_5	V_{ca}	I_2	$-V_{ca}$	
5	d_1	I_5	V_{ca}	I_2	$-V_{ca}$	I_9
	d_2	I_6	$-V_{bc}$	I_3	V_{bc}	
6	d_1	I_6	$-V_{bc}$	I_3	V_{bc}	I_8
	d_2	I_1	V_{ab}	I_4	$-V_{ab}$	

Table 4.3: Feasible switching states of the FB converter.

State	$\boldsymbol{S_1}$	$\boldsymbol{S_2}$	$\boldsymbol{S_3}$	$\boldsymbol{S_4}$	$\boldsymbol{v_s}$	$\boldsymbol{i_o}$
11	1	1	0	0	V_o	ni_L
12	0	0	1	1	$-V_o$	$-ni_L$
13	1	0	1	0	0	0
14	0	1	0	1	0	0

$(S_3, S_4 = 1)$ of the FB. Zero voltage is then applied during $d_0 T_s$ to complete the modulation period. States 13 $(S_1, S_3 = 1)$ and 14 $(S_2, S_4 = 1)$ can be selected for example to reduce the number of commutations. Figure 4.4(b) shows an example of possible command signals for the MC and the FB under positive phase-shift and sector 1. X_1, Y_1, Z_1, X_2, Y_2, Z_2 are intermediate signals of the modulation that have always the specific pattern represented in Figure 4.4(b). For each sector, these intermediate signals can then be routed to the command signals S_{xy} using Table 4.4. On other hand, intermediate signals Q_1, R_1, Q_2, R_2 can only have slight variations across the sectors due to the choice between

Table 4.4: Intermediate signals routing for the MC.

Sector	S_{aP}	S_{bP}	S_{cP}	S_{aN}	S_{bN}	S_{cN}
1	X_1	Y_1	Z_1	X_2	Y_2	Z_2
2	Y_2	Z_2	X_2	Y_1	Z_1	X_1
3	Z_1	X_1	Y_1	Z_2	X_2	Y_2
4	X_2	Y_2	Z_2	X_1	Y_1	Z_1
5	Y_1	Z_1	X_1	Y_2	Z_2	X_2
6	Z_2	X_2	Y_2	Z_1	X_1	Y_1

the two zero states.

$$\begin{aligned} t_1 &= t_0 + \Delta T_1 = \frac{\delta}{2}\frac{d_1}{2}T_s \\ t_3 &= \left(\frac{\delta}{2}+1\right)\frac{d_1}{2}T_s \\ t_5 &= t_4 + \Delta T_2 = d_1 T_s + \frac{\delta}{2}\frac{d_2}{2}T_s \\ t_7 &= d_1 T_s + \left(\frac{\delta}{2}+1\right)\frac{d_2}{2}T_s \end{aligned} \tag{4.14}$$

The modulation principle for negative phase-shift operation is equivalent to the positive phase-shift with ΔT_1 and ΔT_2 taking the negative values as shown in Figure 4.5(a). The negative pulse of v_s between instant t_{11} and t_{13} (4.14) is phase-shifted by ΔT_1 relatively to the first negative pulse of v_p. The same approach is used for the second negative pulse of v_s between instant t_{15} and t_{17}, which is phase-shifted by ΔT_2 relatively to the second negative pulse of v_p. Positive pulses are applied during intervals $[t_0, t_{11}]$, $[t_{13}, t_{15}]$ and $[t_{17}, t_8]$ using state 11. Zero voltage is then applied between instant t_8 and T_s. Figure 4.5(b) shows an example of possible command signals for the MC and the FB where they are under negative phase-shift and when the current reference vector is in sector 1. Intermediate signals X_1, Y_1, Z_1, X_2, Y_2, Z_2 are exactly the same presented in Figure 4.4(b). Such as for the positive phase-shift case, H_1, L_1, H_2, L_2 can only have slight variations across the sectors due to the choice between the two zero states.

$$\begin{aligned} t_{11} &= t_3 = \left(\frac{\delta}{2}+1\right)\frac{d_1}{2}T_s \\ t_{13} &= \left(\frac{\delta}{4}+1\right)d_1 T_s \\ t_{15} &= d_1 T_s + \left(\frac{\delta}{2}+1\right)\frac{d_2}{2}T_s \\ t_{17} &= d_1 T_s + \left(\frac{\delta}{4}+1\right)d_2 T_s \end{aligned} \tag{4.15}$$

The voltage difference between v_s and v_p is applied to the transformer which stores

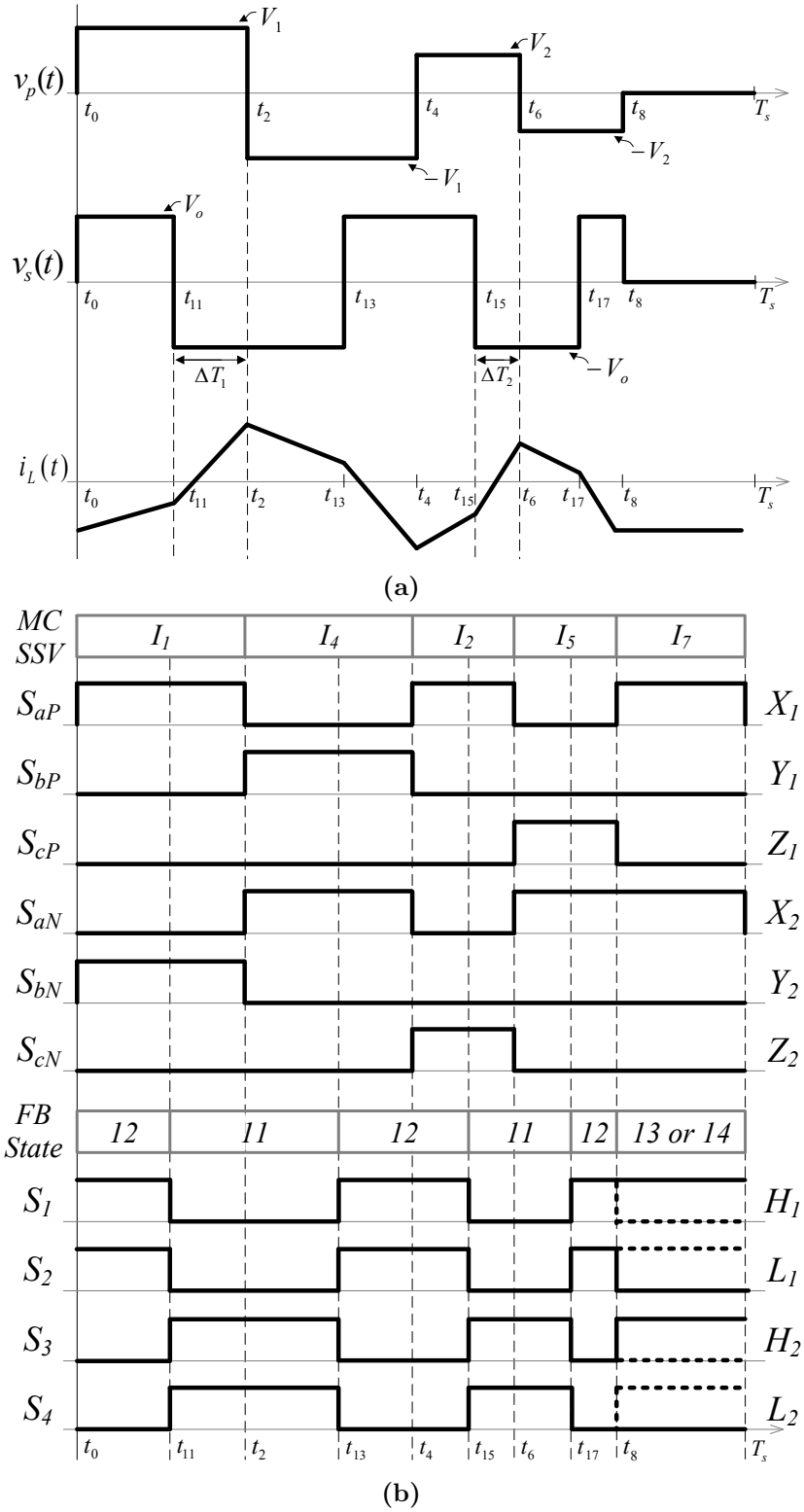


Figure 4.5: (a) Modulation principle in inverter mode: voltages v_p, v_s, and transformer primary current (i_L). (b) Example of command signals for the MC and FB under negative phase-shift and sector 1.

energy in leakage inductance L. The power transfer between the two voltage sources (MC and FB) can be controlled by the amplitude and phase-shift of v_s and v_p. The resulting current, i_L, is reflected in the MC input as well as in the FB output producing i_i and i_o respectively. Averaging these currents in the MC input over one modulation period results for sector 1:

$$\begin{aligned}
\langle i_a \rangle_{Ts} &= \frac{V_o}{\omega_s L} n\phi \left(1 - \frac{|\phi|}{\pi}\right) \left(d_1^2 + d_2^2\right) \\
\langle i_b \rangle_{Ts} &= -\frac{V_o}{\omega_s L} n\phi \left(1 - \frac{|\phi|}{\pi}\right) d_1^2 \\
\langle i_c \rangle_{Ts} &= -\frac{V_o}{\omega_s L} n\phi \left(1 - \frac{|\phi|}{\pi}\right) d_2^2
\end{aligned} \tag{4.16}$$

where $\omega_s = 2\pi f_s$ is the modulation frequency in radians per second. A detailed derivation of the average currents defined in (4.16) can be found in Appendix A. In order to modulate the reference input current vector (4.4)-(4.5), duty cycles d_1 and d_2 must be calculated using (4.17), where m is the modulation index. The modulation period is then completed through the duty cycle d_0. Since $d_0 \geq 0$, $d_1 \geq 0$, and $d_2 \geq 0$, the modulation index is limited to $1/\sqrt{2}$, thus $0 \leq m \leq 1/\sqrt{2}$. As I_i is controlled by ϕ, m can be set to its maximum value to do not limit the transferred power. In the following description $m = 1/\sqrt{2}$ will be considered without loss of generality. Further details about the derivation of duty-cycles defined in (4.17) can be found in Appendix A.

$$\begin{aligned}
d_1 &= m\sqrt{\sin\left(\frac{\pi}{3} - \theta_i\right)} \\
d_2 &= m\sqrt{\sin\left(\theta_i\right)} \\
d_0 &= 1 - d_1 - d_2
\end{aligned} \tag{4.17}$$

Taking the space vector transformation (4.5) and combining it with (4.16)-(4.17), the value of I_i is obtained as (4.18). Due to symmetry, this result is also valid for the other sectors in the $\alpha\beta$ reference frame. Moreover, this result proves that (4.16) and (4.4) are equivalent and allow the precise modulation of $\bar{i}_i$. Assuming zero power losses in the conversion system, the average output current over one modulation period, $\langle i_o \rangle_{Ts}$, can be expressed by (4.19).

$$I_i \equiv \langle \bar{i}_i \rangle_{Ts} = \frac{1}{2} \frac{V_o}{\omega_s L} n\phi \left(1 - \frac{|\phi|}{\pi}\right) \tag{4.18}$$

$$I_o \equiv \langle i_o \rangle_{Ts} = \frac{3}{4} \frac{V_i}{\omega_s L} n\phi \left(1 - \frac{|\phi|}{\pi}\right) \cos\left(\varphi_i\right) \tag{4.19}$$

Considering (4.2)-(4.4) and (4.18), the active and reactive power are given respectively by (4.20) and (4.21). Similarly, taking (4.19), the average output power in the DC side can

be defined as (4.22).

$$P_i = \frac{3}{2}\Re\{\bar{v}_i \cdot (\bar{i}_i)^*\} = \frac{3}{4}\frac{V_i V_o}{\omega_s L} n\phi \left(1 - \frac{|\phi|}{\pi}\right) \cos(\varphi_i) \tag{4.20}$$

$$Q_i = \frac{3}{2}\Im\{\bar{v}_i \cdot (\bar{i}_i)^*\} = \frac{3}{4}\frac{V_i V_o}{\omega_s L} n\phi \left(1 - \frac{|\phi|}{\pi}\right) \sin(\varphi_i) \tag{4.21}$$

$$P_o = V_o I_o = \frac{3}{4}\frac{V_i V_o}{\omega_s L} n\phi \left(1 - \frac{|\phi|}{\pi}\right) \cos(\varphi_i) \tag{4.22}$$

As expected, the input active power (4.20) is equal to the output power (4.22) since zero power losses were considered. The MC impresses an AC voltage in the transformer by selecting the two highest line-to-line voltages (cf. Table 4.2). As a consequence, only the SSVs in the half-plane defined by the direction of $\bar{v}_i$ can be used. Therefore, the input current displacement angle has to be restricted to

$$-\frac{\pi}{6} \leq \varphi_i \leq \frac{\pi}{6}\,. \tag{4.23}$$

Reactive power generation or consumption is then limited as a function of the active power and the maximum apparent power. However, this constraint is not significant since in most applications a unitary power factor is preferred. Moreover, the reactive power curve requirement from VDE-AR-N 4105 (Figure 1.9) can still be implemented. Additionally, the limit in (4.23) allows compensation of the reactive power drawn by the input filter.

4.3 Controllers

4.3.1 Grid currents controller

By controlling the grid current through the adjustment of $\bar{i}_i$, several control strategies can be implemented and combined as power factor control, DC voltage and current regulation and active and reactive power control (PQ control). An equivalent single-phase circuit of the grid, the input filter, and the HFLMC is shown in Figure 4.6. The mathematical model of this grid interface in the stationary reference frame is described by (4.24) [249], with $L_e = L_g + L_d + L_F$, $R_e = R_g$, and $C_e = C_F$. It is clear from this relationship that the grid current, $i_g(t) = [i_{ga}\ i_{gb}\ i_{gc}]^T$, can be controlled by the modulated current $i_i(t) = [i_a\ i_b\ i_c]^T$. The grid voltage $v_g(t) = [v_{ga}\ v_{gb}\ v_{gc}]^T$ can be seen as the perturbation variable. It is assumed $v_i(t) \approx v_g(t)$ in steady-state operation.

$$i_i(t) = i_g(t) + L_e C_e \frac{d^2}{dt^2} i_g(t) + R_e C_e \frac{d}{dt} i_g(t) - C_e \frac{d}{dt} v_g(t) \tag{4.24}$$

The controller can be formulated in the synchronous reference frame (SRF) using the dq transformation, as shown in Figure 4.7. Assuming a balanced three-phase grid, the state variables under steady-state conditions are represented by DC quantities in the SRF. The

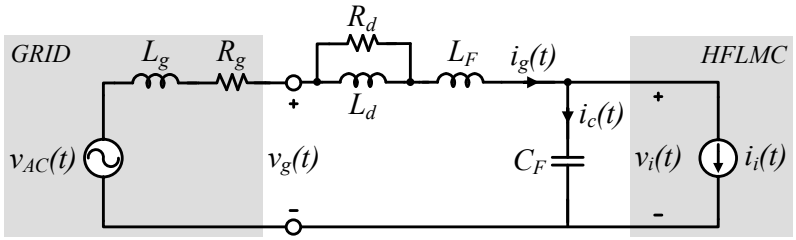


Figure 4.6: Simplified equivalent circuit of the grid interface.

phase angle of the grid voltage, α_i, is not only necessary to synchronize the modulation but also for the dq transformation. The SRF phase-locked loop (PLL) has proven to be robust against phase unbalancing, harmonics and voltage distortions [250, 251]. Using this PLL structure, the phase angle is estimated by synchronizing the $v_g(t)$ along the q-axis, resulting in $v_{gd} = 0$. Considering this result, active and reactive power in the grid can be expressed respectively by (4.25) and (4.26). Active power can be controlled with the q-axis component and the reactive power with the d-axis component of the grid current space vector [252].

$$P_g = \frac{3}{2} v_{gq} i_{gq} \tag{4.25}$$

$$Q_g = -\frac{3}{2} v_{gq} i_{gd} \tag{4.26}$$

The transformation of model (4.24) to the SRF results in (4.27). There are cross coupled terms that should be decoupled in order to individually control i_{gd} and i_{gq} by adjusting i_{id} and i_{iq} [253]. As described in [252], the reactive power drawn by the input filter can be compensated by adding an additional term to the input current reference i_{id}^*. Proportional-integral (PI) controllers are implemented to track i_{gd}^* and i_{gq}^*.

$$\begin{aligned} i_{id} &= i_{gd} + L_e C_e \left[\frac{d^2}{dt^2} i_{gd} - 2\omega_i \frac{d}{dt} i_{gq} - \omega_i^2 i_{gd} \right] + \\ &+ R_e C_e \left[\frac{d}{dt} i_{gd} - \omega_i i_{gq} \right] - C_e \left[\frac{d}{dt} v_{gd} - \omega_i v_{gq} \right] \\ i_{iq} &= i_{gq} + L_e C_e \left[\frac{d^2}{dt^2} i_{gq} + 2\omega_i \frac{d}{dt} i_{gd} - \omega_i^2 i_{gq} \right] + \\ &+ R_e C_e \left[\frac{d}{dt} i_{gq} + \omega_i i_{gd} \right] - C_e \left[\frac{d}{dt} v_{gq} + \omega_i v_{gd} \right]. \end{aligned} \tag{4.27}$$

Input current vector $\bar{i}_i^*$ can be modulated through control of the respective magnitude I_i, and phase φ_i in the polar frame. Thus, components i_{iq}^* and i_{id}^* are transformed from the dq reference frame to the polar frame. In order to calculate the required ϕ to produce I_i, the inverse function of (4.18) must be found. Since I_i is a non-linear function of phase-shift, approximation $\phi \left(1 - \frac{|\phi|}{\pi}\right) \approx 0.691\phi$ is considered for the domain of interest. The resulting

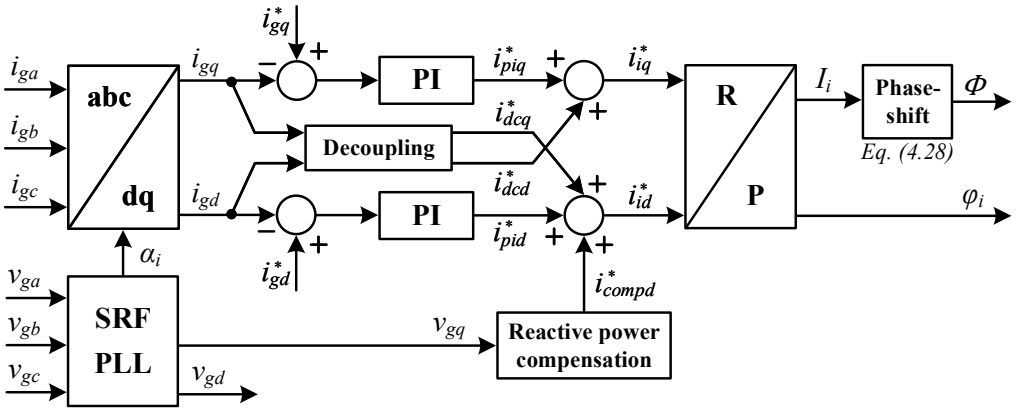


Figure 4.7: Control diagram for decoupled grid currents regulation in the SRF frame.

control variables are determined by:

$$\phi = sgn(i^*_{iq})\frac{k_g}{V_o}\sqrt{{i^*_{id}}^2 + {i^*_{iq}}^2} \tag{4.28}$$

$$\varphi_i = tan^{-1}\left(\frac{i^*_{id}}{i^*_{iq}}\right) \tag{4.29}$$

where $sgn()$ is the sign function and $k_g = \frac{2\omega_s L}{0.691n}$. Due to the nature of the output filter, V_o has practically the same value of the measured DC voltage, v_{dc}. For this reason, v_{dc} is considered for calculating phase-shift instead of v_o. Consequently, for the given reference currents, i^*_{gq} and i^*_{gd}, control variables ϕ and φ_i can be determined in order to feed the modulation. Using a positive phase-shift, the power is transferred from the grid to the battery pack. A negative phase-shift inverts the power flow from the battery to the grid. From the control perspective, the transition between these operation modes is seamless.

The stability and bandwidth of the proposed control scheme need to be analyzed. The time-domain model of the converter connected to the grid through an LC filter (4.24) to a frequency-domain model. The transfer function model simplify the analysis and design process, and provides interesting information about the controller, such as bandwidth, overshoot, settling time and stability. Frequency response method is selected here for the clearly graphical representation with user-friendly software, such as MATLAB. The average model of the converter is a classical modeling method for PWM converter systems, where the switching frequency is assumed to be much higher than the converter dynamics for the averaging model to be accurate. In this specific case, the HFLMC has also two main dynamics: one associated with the proposed modulation that is updated at T_s, and the other associated with the grid currents control that is much slower than the previous one. Based on this assumption, the AC current control loop is designed separately from the modulation one by the use of averaging technique [254]. It is considered that the power converter with the modulation generates the reference currents i^*_{iq} and i^*_{id} almost

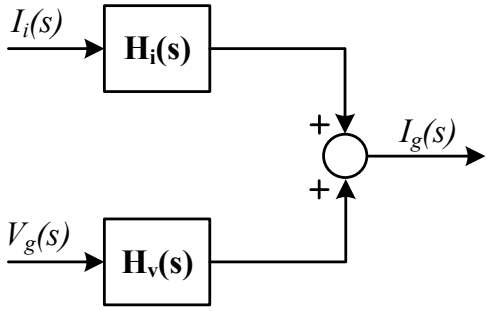


Figure 4.8: Transfer functions that establish the relation between $I_g(s)$, $I_i(s)$ and $V_g(s)$.

instantaneously when compared with the dynamics of the current control loop. However, some delay exist due to the processing of all the computations in the DSP and FPGA (T_s) and due to the modulation (0.5 T_s). This delay can be modeled by the following transfer function:

$$G_d(s) = \frac{I_i(s)}{I_i^*(s)} = e^{-s1.5T_s} \tag{4.30}$$

The input filter of the converter is based on the LC filter with a damping network composed by the parallel of L_d and R_d, as represented in Figure 4.6. The damping is important to avoid resonances near the natural frequency of the LC filter. For frequencies a decade below the resonant frequency, the impedance of the damping network is practically defined by L_d. Therefore, equation (4.24) is still valid for the formulation of the control architecture in the SRF.

As previously discussed, the grid current $i_g(t)$ can be controlled by the modulated current $i_i(t)$. So, $H_i(s)$ is the transfer function that represents this relation. The current in the grid can also be perturbed by voltage $v_g(t)$ according the transfer function $H_v(s)$. Figure 4.8 and (4.31) represent these relations that define how $I_g(s)$ changes as a function of $I_i(s)$ and $V_g(s)$.

$$I_g(s) = I_i(s)H_i(s) + V_g(s)H_v(s) \tag{4.31}$$

Transfer functions $H_i(s)$ and $H_v(s)$ can be obtained by analyzing the equivalent circuit presented in Figure 4.6 based on the superposition theorem. The respective transfer functions are defined in (4.32) and (4.33).

$$H_i(s) = \frac{I_g(s)}{I_i(s)} = \frac{sL_d + R_d}{s^3C_FL_FL_d + s^2C_FR_d(L_d + L_F) + sLd + R_d} \tag{4.32}$$

$$H_v(s) = \frac{I_g(s)}{V_g(s)} = \frac{sC_F}{s^3C_FL_FL_d + s^2C_FR_d(L_d + L_F) + sLd + R_d} \tag{4.33}$$

For the definition of the current controller, only the relation between $I_i(s)$ and $I_g(s)$ is explored, while $V_g(s)$ is seen as a perturbation for the control loop. Then, the transfer function of the equivalent circuit of the grid interface (i.e. the plant of the control loop)

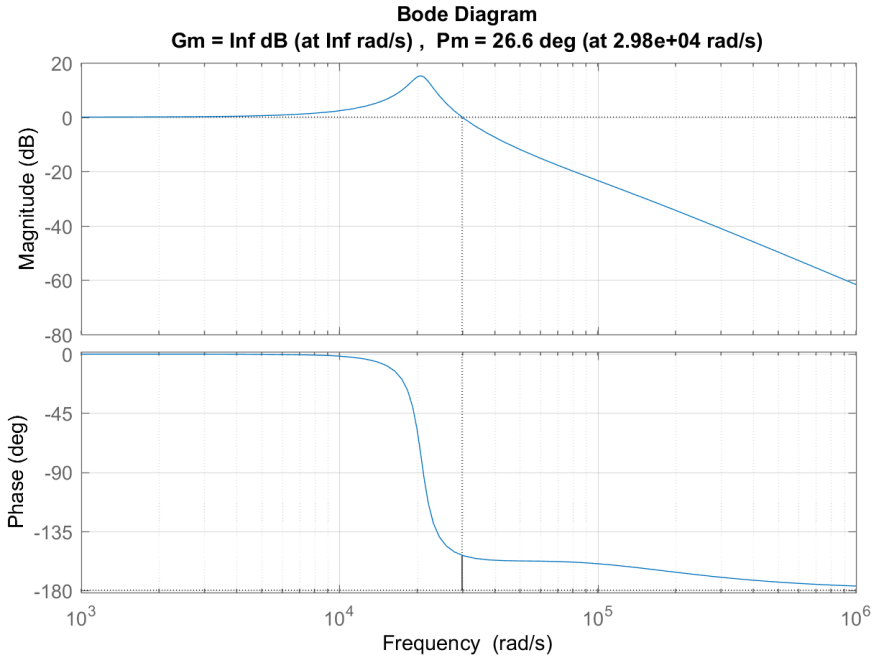


Figure 4.9: Bode plot of the transfer function $G_p(s)$ between $i_i(t)$ and $i_g(t)$.

can be defined as:

$$G_p(s) = \frac{I_g(s)}{I_i(s)} \equiv H_i(s) \tag{4.34}$$

Now, it is important to analyze the transfer function $G_p(s)$ to verify its stability and the requirements for the linear controller. The parameters considered for the grid model are $R_g = 50$ mΩ and $L_g = 50$ μH, following the reference network defined in IEC 61000-3-3 standard [255]. Regarding the input filter, $C_F = 20$ μF, $L_F = 60$ μH, $L_d = 60$ μH, and $R_d = 3.3$ Ω are employed in both simulation and experimental tests. Figure 4.9 shows the Bode plot for the equivalent circuit of the grid interface. As can be seen, the damping network reduces the magnitude of the resonant peak. The natural frequency of this circuit is around 3279 Hz. If the linear controller were a simple unitary gain, the phase-margin (PM) of the closed-loop would be only 26.6°. This shows the need to add a controller to improve the PM in order to provide robustness to the closed-loop system.

In order to stabilize the closed-loop it is necessary to introduce a controller to increase the PM, as represented by $G_c(s)$ in Figure 4.10. The PI controller described by (4.35) is commonly employed for this task. A linear design and the MATLAB/Simulink (MLS) environment were used to define the parameters of the controller. The proportional and integral gains tuned for this case are K_p=0.05 and K_i=125. To prevent saturation, due to the integrative component, the clamping anti-windup method is added to the PI controller.

$$G_c(s) = K_p + \frac{K_i}{s} \tag{4.35}$$

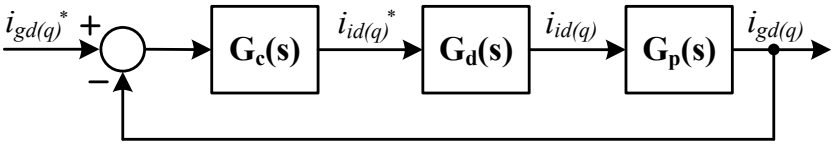


Figure 4.10: Simplified control loop of the grid currents in the synchronous reference frame.

Figure 4.11 shows the Bode plot of the current control system highlighting the bandwidth of the control loop. As can be seen, the PM is increased significantly to 92.3°. The resulting bandwidth of the system is around 20 Hz which is well below the resonant peak of the $G_p(s)$. Now all the poles are in the left hand side of the s-plane. This was expected considering the 11.3 dB gain-margin (GM) from the Bode plot. Therefore, the closed loop system is stable.

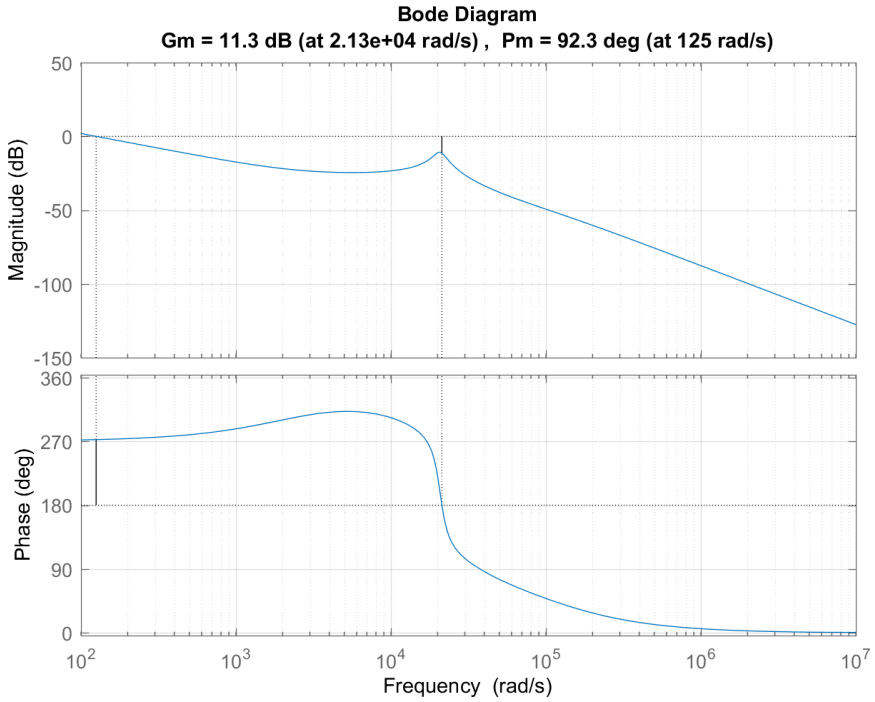


Figure 4.11: Bode plot of the current control loop composed by $G_c(s)$, $G_d(s)$, and $G_p(s)$.

The formulation of the grid interface model in the SRF makes appear the cross coupled terms in (4.27). In order to individually control i_{gq} and i_{gd}, the decoupling terms are added to the diagram in Figure 4.7. In this way, the two PI controllers that regulate i_{gq} and i_{gd} in the grid interface can be formulated independently. Thus, the same gains deduced above are used for both PI regulators, ensuring the stability and robustness of the controller.

4.3.2 Battery voltage and current controllers

With these control variables there is flexibility to implement several control strategies for the PCS. One possibility consists in having a current controller that imposes the proper i^*_{gq} in order to regulate the output current i_{dc}, as shown in Figure 4.12. An additional PI controller gives the set-point for i^*_{gd} to adjust the power factor in the grid side according to the reference PF^*. Furthermore, the regulation of the output voltage v_{dc} can be accomplished by adding an outer control loop to the previous strategy. The voltage controller sets the reference for i_{dc}, which in turn is adjusted by the internal current controller.

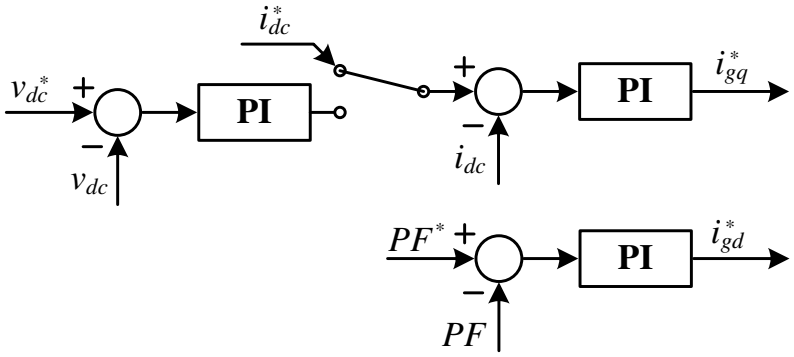


Figure 4.12: Battery voltage and current controllers with power factor adjustment.

4.3.3 PQ controller

Active and reactive power can also be controlled to provide services for the grid operator or to comply with the power quality standards [256, 257]. The required references i^*_{gq} and i^*_{gd} for the internal loop are set by the PQ controller presented in Figure 4.13. The

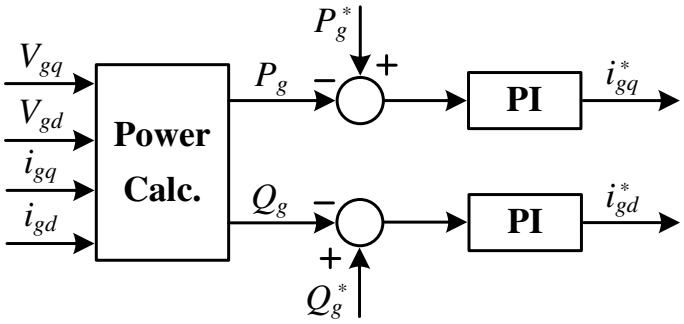


Figure 4.13: PQ controller.

grid currents are then regulated in the dq reference frame by the controller projected in Section 4.3.1. As a consequence, the active and reactive power level in the grid interface

Table 4.5: Specifications and parameters of the HFLMC.

Parameter	Value	Parameter	Value	Parameter	Value
V_i	325 V	$V_{dc,nom}$	380 V	L	44 μH
f_i	50 Hz	$I_{dc,max}$	31 A	n	1
P_{nom}	10 kW	C_F	20 μF	C_o	75 μF
$I_{g,max}$	16 A	f_s	20 kHz	L_o	55 μH

is adjusted to follow the references P_g^* and Q_g^*. The instantaneous values for the active and reactive power are determined using (4.25) and (4.26). The amplitude of the output current i_{dc} in the energy storage device is a result of the active power exchanged with the grid.

4.4 Simulation Results

A simulation model of the HFLMC is implemented in GeckoCIRCUITS [199] software to verify and validate the proposed modulation and the controllers. Figure G.1 from Appendix G show the implementation details of the power circuit and the control algorithms in this software. The specifications and parameters used in simulation are listed in Table 4.5. The transformer's turns ratio and the leakage inductance are designed for a DC voltage range operation from 320 V to 490 V. The SiC MOSFET of type C2M0025120D [258] with a typically on-resistance of 25 mΩ was selected for the MC and the FB. Switching and conduction losses are modeled using information provided by the manufacturer, as represented in Figure G.2. A first-order thermal model is also incorporated considering an ambient temperature of 40°C. The heatsink is designed for a maximum junction temperature of 155°C at nominal operating conditions. Figure G.3 from Appendix G show the implementation details of the thermal circuit and losses measurement in GeckoCIRCUITS. As previously discussed in Section 3.4, the simultaneous commutation of the bidirectional switches is very difficult to achieve without generating overcurrent or overvoltage spikes that can destroy the power semiconductors. To overcome this difficulty, the variable-step VBC strategy presented in Section 3.4.2 was employed. By properly changing between the two-step uncritical commutation and the four-step critical commutation approaches a safe VBC with minimum switching losses is ensured. The grid was modelled by an ideal three-phase AC voltage source in series with a line impedance of 478 μH (150 mΩ at 50 Hz) and 240 mΩ. These values follow the reference network defined in IEC 61000-3-3 [255]. On other hand, the battery is modeled by a DC voltage source in series with a resistance of 0.5 Ω, as an approximation for the battery internal impedance [71]. A DC filter is added between the FB and the battery pack in order to reduce the current ripple present in i_o due to the high-frequency link operation.

4.4.1 High-frequency Link operation

The high-frequency link operation is illustrated in Figure 4.14. The single-stage conversion is noticeable through the low-frequency envelope that appears on v_p. Since there is no intermediate DC-link, the grid voltage peak appears directly applied to the primary winding of the transformer. In other way, the FB applies an AC voltage with the same amplitude of the battery voltage. The phase-shift introduced on v_s respecting to v_p generates the current i_L that circulates in the transformer primary winding. This current is then reflected to the secondary winding as a function of the turns-ratio of the transformer.

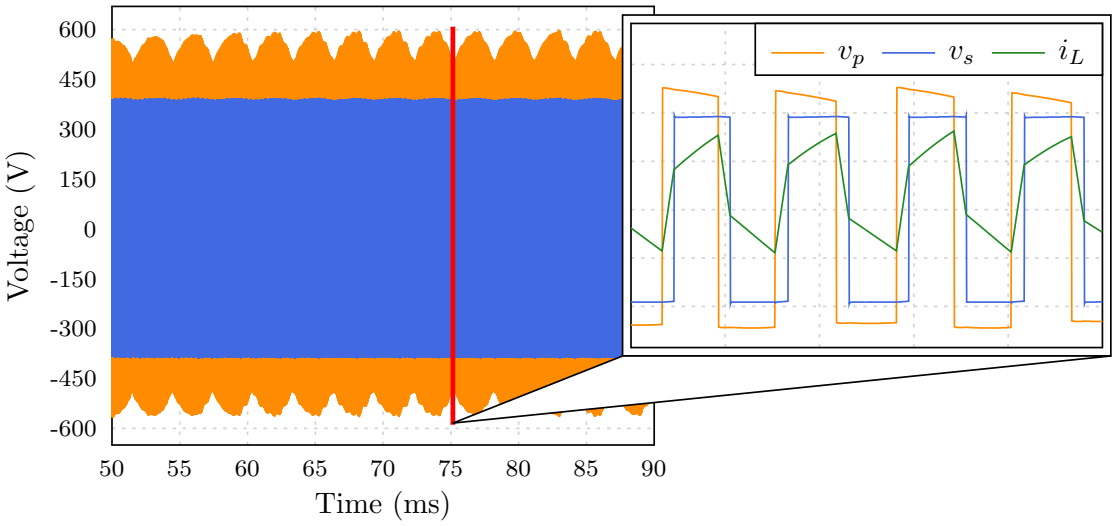
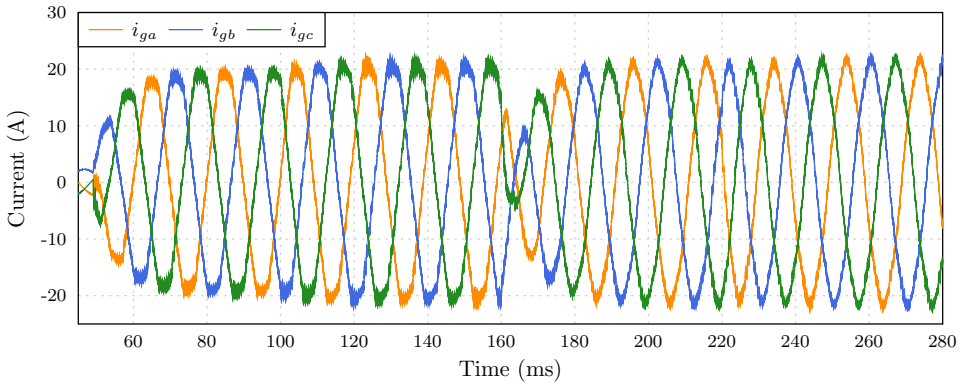


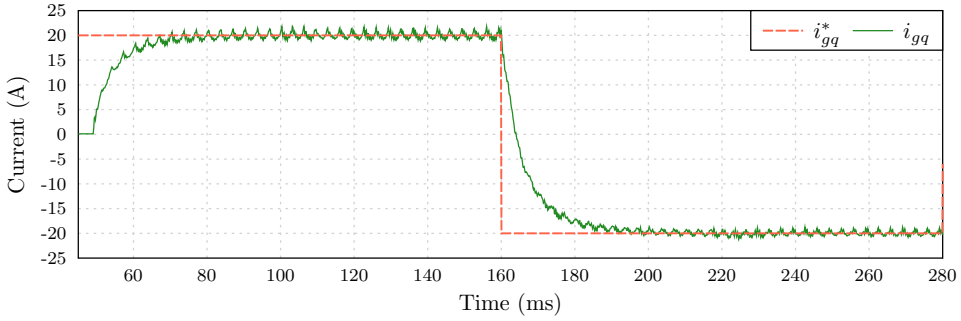
Figure 4.14: HFL operation: voltages impressed at the transformer primary and secondary windings (v_p, v_s), and current in the link-inductor (i_L).

4.4.2 Grid currents controller

The feasibility and performance of the controller proposed in Figure 4.7 was verified through simulation. Both PI controllers were tuned with gains K_{p,i_g}=0.050 and K_{i,i_g}=2500. The current references, i^*_{gq} and i^*_{gd}, are varied in order to test the step response of the current controller. Figure 4.15 shows the operation of the HFLMC in the four-quadrants (4Q). As can be seen in Figure 4.15(b) and Figure 4.15(c), d and q components are perfectly decoupled and follow the given references. The transition from charger to inverter mode at 160ms is performed transparently and with perfect control of the grid currents as shown in Figure 4.15(a). This abrupt step introduced a perturbation at i_{gd} that is quickly compensated by the controller. The step response has a rise time lower than 15ms and a settling time under two cycles of the grid voltage. The power factor was also alternated between -0.94 and +0.94 by changing i_{gd}. Regarding to the DC side, the current i_{dc} is an image of the q component of the grid current which was expected considering (4.18)-(4.22).



(a)



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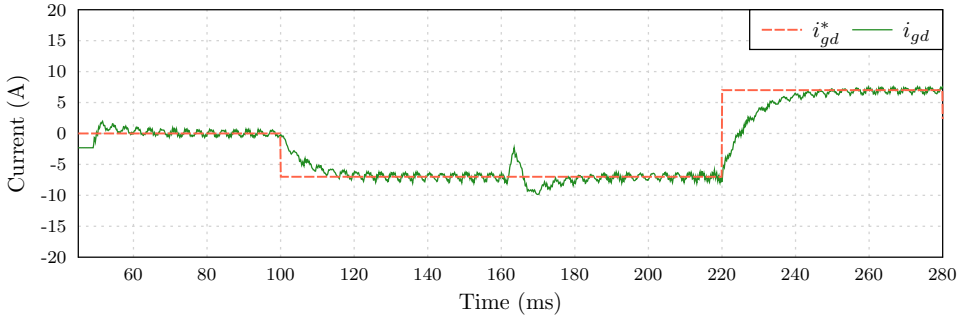

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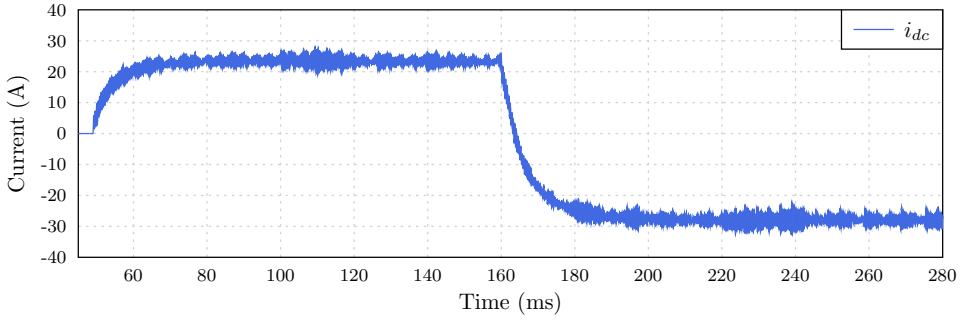


(d)

Figure 4.15: Simulation results of the HFLMC operation in the 4Q. (a) Grid currents ($i_{ga,b,c}$). (b) q reference (i^*_{gq}) and actual q grid current (i_{gq}). (c) d reference (i^*_{gd}) and actual d grid current (i_{gd}). (d) Battery current (i_{dc}).

4.4.3 Battery voltage and current controllers

The voltage and the current in the battery pack can be regulated by changing the currents i_{gq} and i_{gd} at the grid interface. The controller proposed in Figure 4.12 was tested in simulation by changing the references for i_{dc}, v_{dc}, and PF. The gains of the PI controller for i_{dc} are $K_{p,i_{dc}}$=0.5 and $K_{i,i_{dc}}$=200. Regarding the PI controller for PF the gains are set as $K_{p,PF}$=30 and $K_{i,PF}$=300. Finally, the gains of the PI controller for v_{dc} are $K_{p,v_{dc}}$=1.5 and $K_{i,v_{dc}}$=150.

Figure 4.16 shows the simulation results of the operation with the Idc and PF controllers. It is clear the effectiveness of the controller to regulate i_{dc}. The step response has a rise time around 18 ms and a settling time under two cycles of the grid voltage. This is achieved by modifying the reference i^*_{gq} that in turn feeds the grid current controller. As expected, i_{gq} has the shape of i_{dc}. Regarding the PF, the respective controller is enabled at t=170 ms. The process of adjusting the PF starts immediately by setting the reference i^*_{gd}. Then, the grid current controller adjust the control variables for the modulation in order to follow this reference. With this strategy the PF is corrected in less than 30 ms. As expected, the battery current is not affected by this change in the PF.

The outer control layer for v_{dc} can be tested since the the capability to regulate i_{dc} was already validated. The additional PI controller proposed in Figure 4.12 was included in the simulation. The main signals from the controller during this experiment are represented in Figure 6.32. During the first part of the test, v^*_{dc} is set to 370 V. Since the battery voltage is at 380 V, the converter starts operating in inverter mode by changing the reference i^*_{dc}. Then, v^*_{dc} is set to 390 V and the converter changes its operation to charger mode in order to increase the battery voltage up to the reference. From this experiment, it is clear that the proposed control architecture is able to regulate both the current and voltage in the batteries. In respect to the capability of adjusting the power factor, the PF controller is enabled at instant t=159 ms. The process to adjust the power factor to 0.90 starts immediately by changing the reference i^*_{gd}. As can be seen, the step response has a rise time below 15ms and a settling time around one cycle of the grid voltage. As expected, the battery voltage is not affected by this change in the PF.

4.4.4 PQ controller

The controller proposed in Figure 4.13 was tested in simulation to verify its capability to adjust independently the active and reactive power by changing the references of P^*_g and Q^*_g. The gains of both PI controllers for P_g and Q_g are $K_{p,PQ}$=0.001 and $K_{i,PQ}$=300.

Figure 4.18 shows the simulation results. As can be seen, both P_g and Q_g follow the references and are well controlled. A change in the reactive power set-point does not disturb the P_g regulation. At t=160 ms is made an abrupt change in the active power reference from charging at 10 kW to the inverter mode. A negligible perturbation appears at Q_g but it is promptly extinguished. The step response has a rise time lower than 20 ms

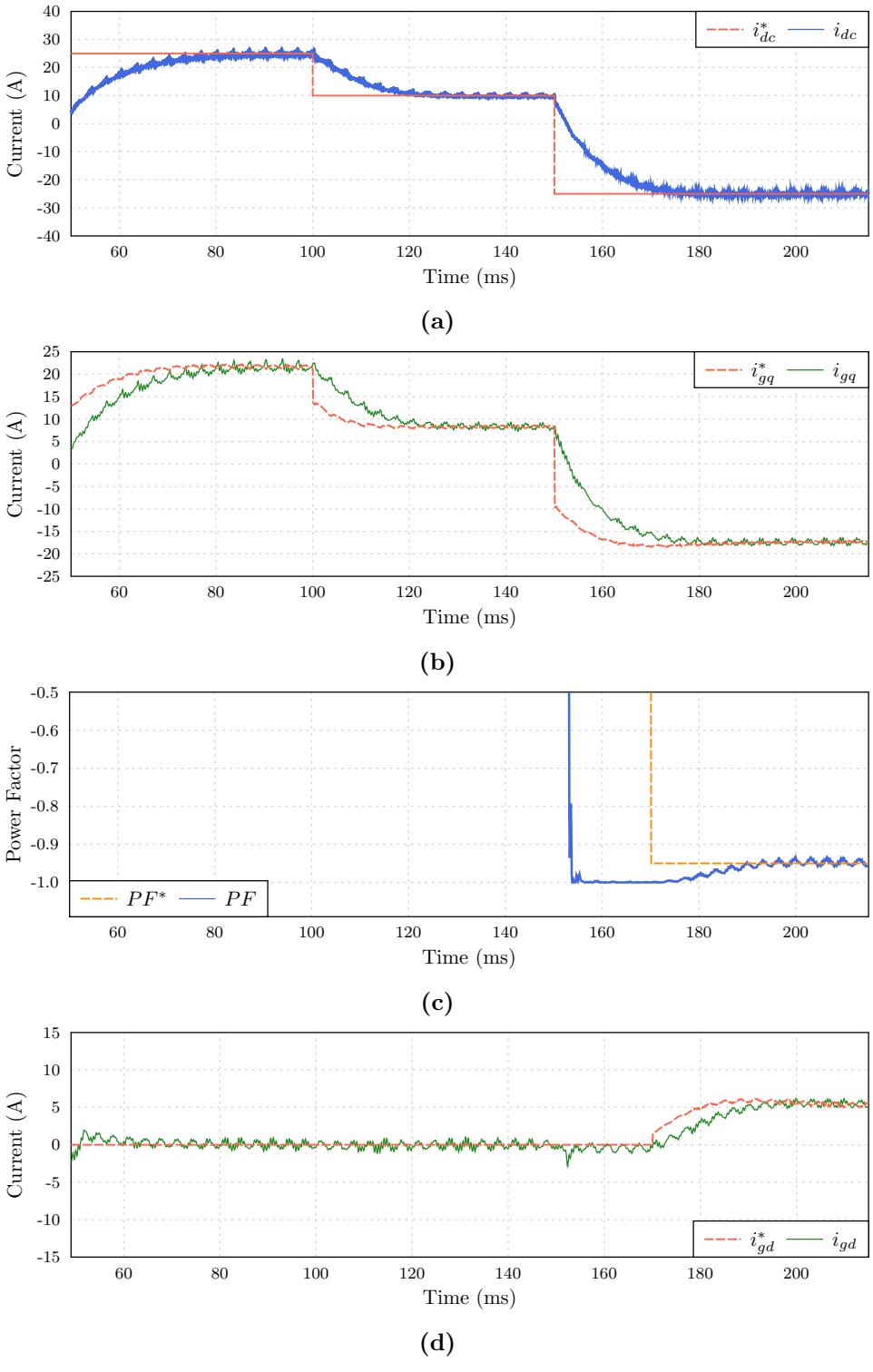


Figure 4.16: Simulation results of the HFLMC operating with the Idc and PF controllers. (a) Battery current (i_{dc}). (b) q grid current (i_{gq}). (c) Power factor and set-point (PF^*). (d) d grid current (i_{gd}).

and a settling time under two cycles of the grid voltage. Regarding the interface with the battery pack, i_{dc} is a result of the active power exchanged with the grid. When P_g

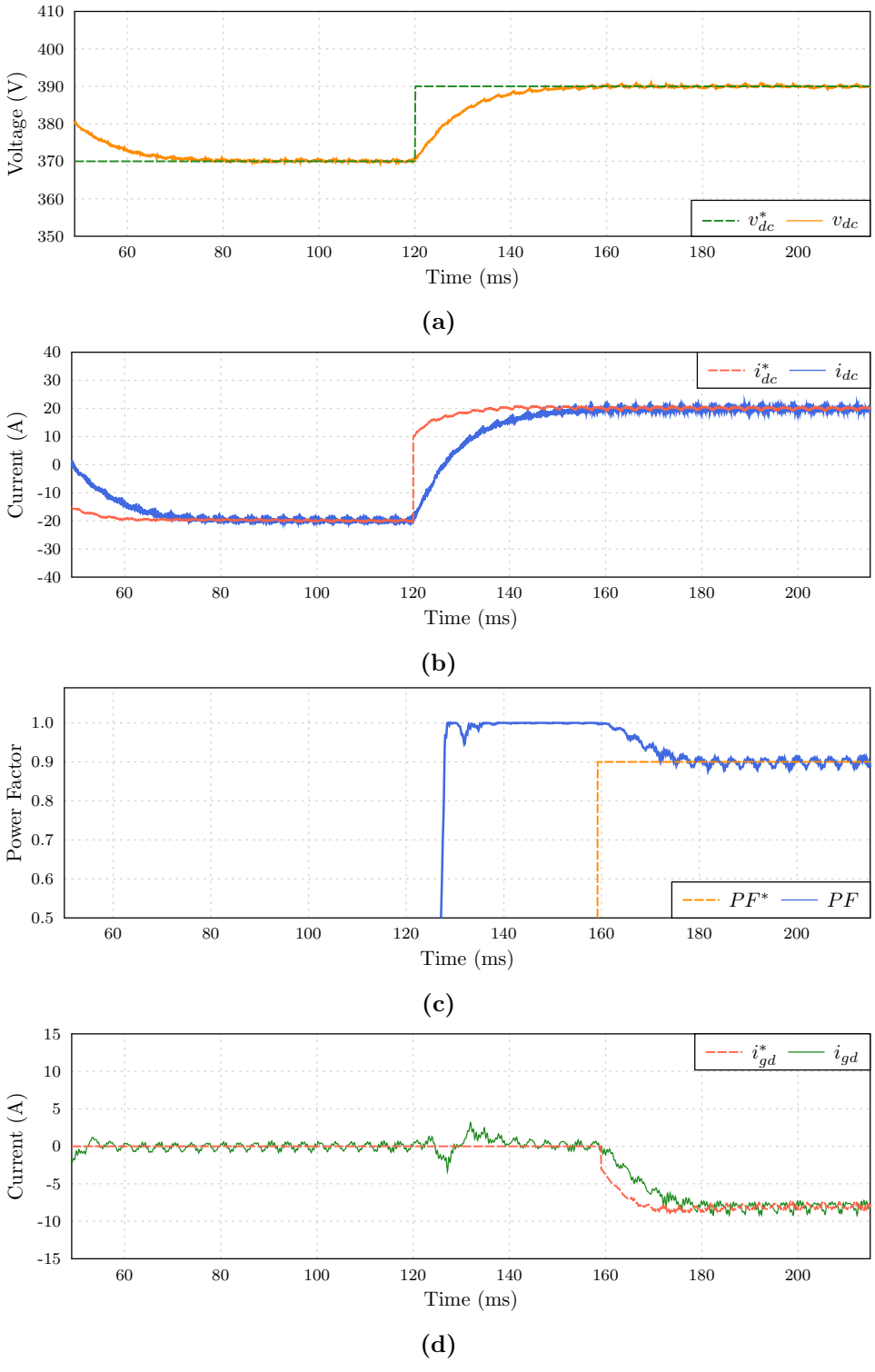


Figure 4.17: Simulation results of the HFLMC operating with the Vdc and PF controllers. (a) Battery voltage and set-point (v^*_{dc}). (b) Battery current (i_{dc}). (c) Power factor and set-point (PF^*). (d) d grid current (i_{gd}).

changes to -10 kW the current i_{dc} slightly increases to compensate the voltage drop in the impedance of the battery pack. It is also interesting to note that, as expected, the

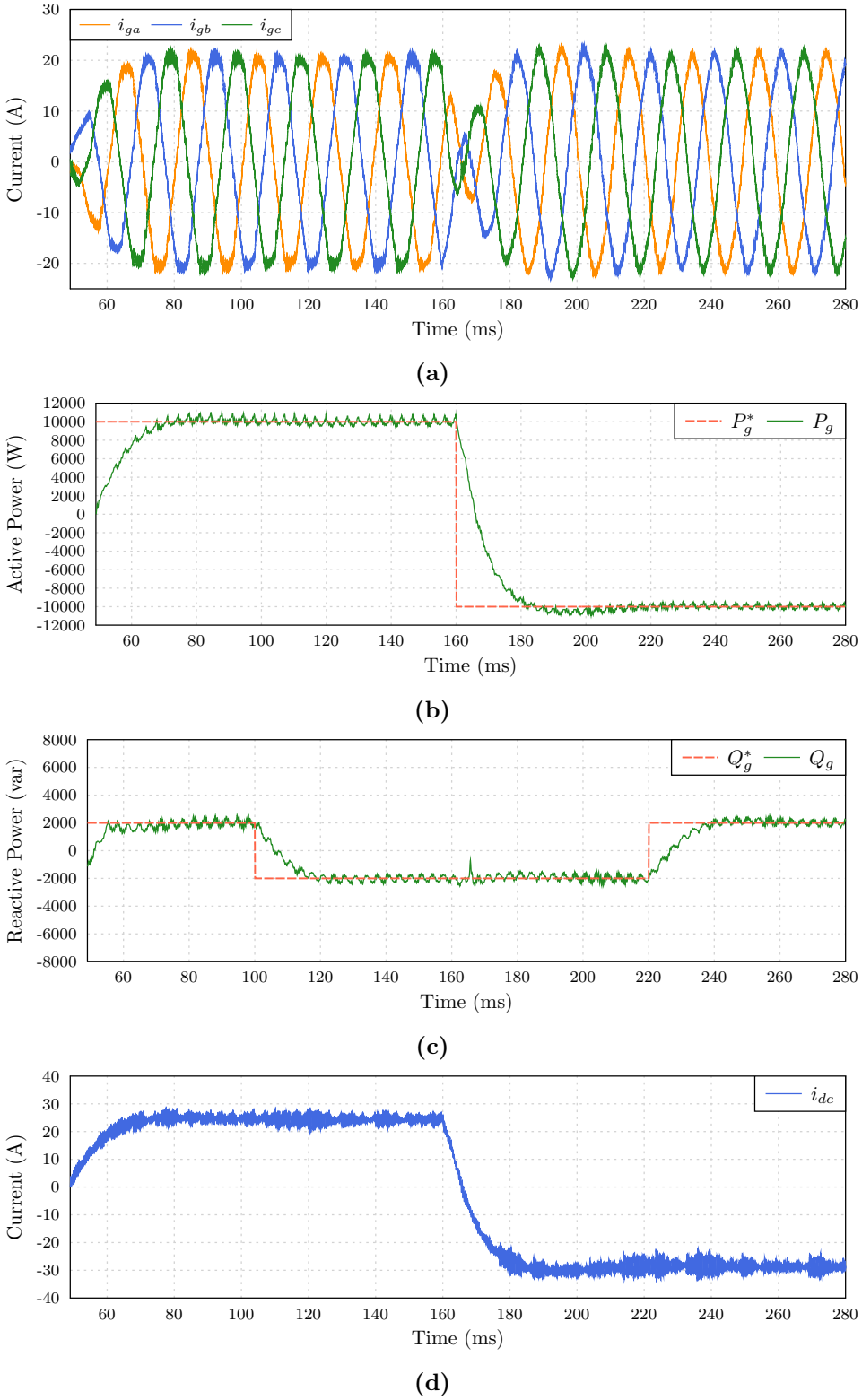


Figure 4.18: Simulation results of the HFLMC operating with the PQ controller. (a) Grid currents ($i_{ga,b,c}$). (b) Active power and set-point P_g^*. (c) Reactive power and set-point Q_g^*. (d) Battery current (i_{dc}).

variation of the reactive power does not affect the current at the batteries. With this simulation, it was successfully verified the operation of the HFLMC in the 4Q.

4.5 Conclusion

A new modulation for the HFLMC was proposed and validated through extensive simulation and experimental tests. The transition from charger to inverter mode occurs smoothly due to the essence of the modulation. The controller for the grid currents ensure a proper regulation in the d-q reference frame with very fast dynamics. Proof of stability was provided in order to ensure robustness of the proposed control scheme. Additional control layers can be implemented to perform voltage and current regulation in the battery pack making this converter a perfect solution for battery based applications that require bidirectional power flow and galvanic isolation in a compact design. Alternatively, a PQ controller can also be implemented in order to provide additional services to the grid operator.

Chapter 5

EMI Filter

5.1 Introduction

The development of new wide bandgap power semiconductors allow the increase of the switching frequency of the power converters. As a result, conducted emissions (CE) with higher intensity are generated in the measurement range of the EMC standards. Therefore, additional effort is necessary in the design of the EMI filter included in the input of the power converters to comply with the standards. A careful dimensioning of the EMI filter is essential to ensure the adequate power factor in all operating range and to achieve a good power quality without penalizing the efficiency, volume and cost of the system. Several approaches for the design of differential-mode (DM) and common-mode (CM) filtering stages for direct and indirect matrix converters were proposed in [90, 151–155, 236, 259–265].

In this chapter is described a method that aims to systematize the design process of the HFLMC's EMI filter for CISPR 11 Class B pre-compliance. This approach can be extended to other current source converters which allows time-savings during the project of the filter. Conducted emissions are estimated through extended simulation and take into account the effect of the measurement apparatus. Differential-mode and common-mode filtering stages are projected separately and then integrated in a synergistic way in order to reduce volume and weight. A prototype of the filter was constructed and tested in the laboratory. Experimental results with the characterization of the insertion losses following the CISPR 17 standard are provided. The attenuation capability of the filter was demonstrated in the final part of the chapter.

This chapter is organized as follows: in section 5.2 the applicable standards and the measurement approach of CE are described. The detailed design of DM and CM filters is explained in section 5.3 and section 5.4 respectively. Section 5.5 presents the integration strategy of both filters. Finally, the experimental results are shown in section 5.6.

5.2 Standards and CE Measurement

The CE are generated by harmonics present in the input current of the MC, $i_i = [i_a, i_b, i_c]$, where i_a, i_b and i_c are the phase currents. EMC standards classify the CE according to the frequency range [266]. Low-frequency harmonics are typically measured up to 2 kHz (40th harmonic) as defined by IEC 61000-3-2 [267]. In section 5.5 are presented the LF harmonics measured for this converter and compared with IEC 61000-3-2 Class A limits. Regarding the HF conducted emissions, CISPR 11 [268] specifies the limits for frequencies from 150 kHz to 30 MHz. These emissions can be estimated by simulating the converter operation without any input filter at nominal conditions: $P_{nom} = 10$ kW, line-to-neutral grid voltage $V_{g,ln} = 230$ V, grid frequency $f_g = 50$ Hz and output voltage $V_{dc} = 380$ V. A simulation model of the HFLMC was implemented in GeckoCIRCUITS [269]. This software has a measure block that performs analysis according to the CISPR 16 [270] standard using the time domain simulation data. Similar to a test receiver (TR), it is possible to select different signal processing options: average (AVG), quasi-peak (QP) or peak detection. The first step of the filter design is to specify the maximum admissible CE levels. Due to the type of application, the QP limits of CISPR 11 Class B curve will be considered. A line impedance stabilizing network (LISN) is connected between the grid and the device under test (DUT) in order to provide a known impedance and ensure the reproducibility of the measurements [271]. A TR calculates the CE in "dBμV" through the measurement of the voltage at the LISN output port, V_{TR}. An equivalent impedance of $50\,\Omega/50\,\mu$H is specified by CISPR 16 for the TR/LISN. The LISN's transfer function from V_{TR} to the DUT's input current is:

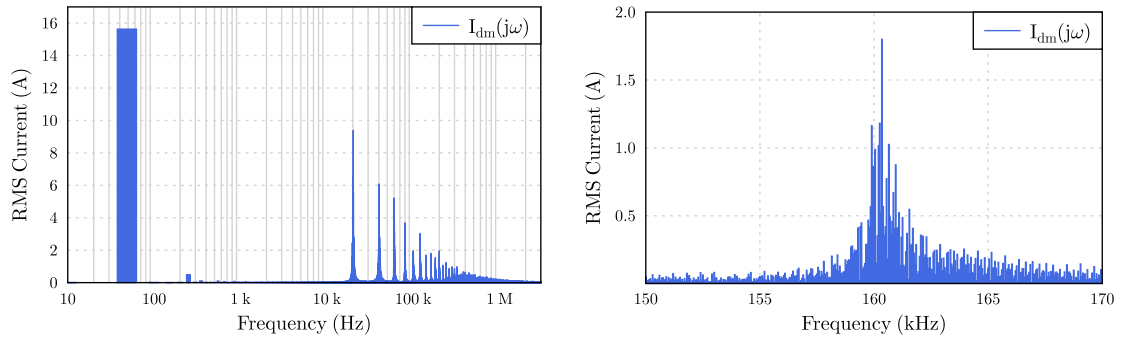
$$G_{LISN}(s) = \frac{V_{TR}(s)}{I_{dut}(s)} = \frac{s^2 L_{LISN} C_{LISN} R_{TR}}{s^2 L_{LISN} C_{LISN} + s R_{TR} C_{LISN} + 1} \tag{5.1}$$

where $R_{TR} = 50\,\Omega$, $L_{LISN} = 50\,\mu$H and $C_{LISN} = 250\,$nF.

5.3 Design of Differential-Mode Filter

5.3.1 Spectrum of the converter input current

Due to the symmetry of the converter and the measurement system, the DM input filter can be projected considering a single-phase equivalent circuit [262]. Fig. 5.1(a) shows the spectrum of the input current of one phase, $I_{dm}(j\omega)$, obtained from simulation. Since no circuit element is connected between the lines and the protective earth (PE), only DM current is present at $I_{dut}(s)$. As can be seen, the first significant harmonic content appears around the switching frequency, $f_s = 20$ kHz. Other harmonics are also present at frequencies multiple of f_s. The first switching frequency harmonic inside the measurement range appears at 160 kHz. A zoom around this frequency is depicted in Fig. 5.1(b).



(a) (b)

Figure 5.1: (a) Frequency spectrum of the converter input current $I_{dm}(j\omega)$. (b) Zoom around the first switching frequency harmonic above 150 kHz.

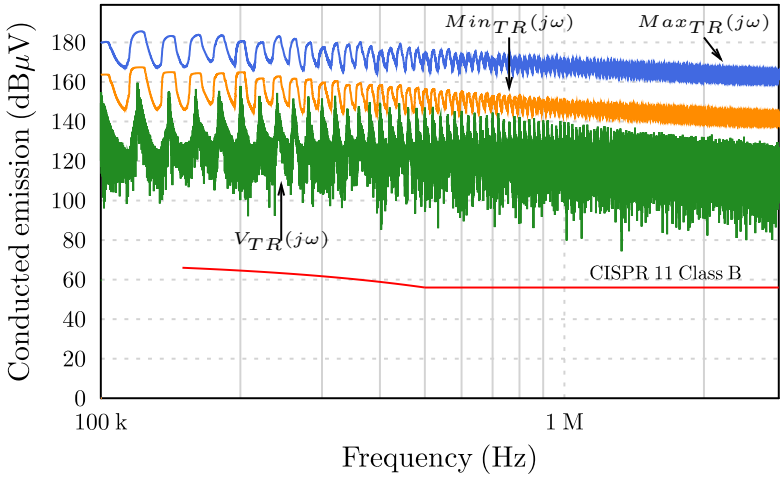


Figure 5.2: TR measurement without DM filter: maximum and minimum estimation of CE along with the spectrum of $V_{TR}(j\omega)$.

5.3.2 Spectrum of the measured voltage

The spectrum of V_{TR} can be determined by the multiplication of $I_{dm}(j\omega)$ with (5.1). Fig. 5.2 depicts the spectrum of $V_{TR}(j\omega)$ at the LISN's output terminals along with the maximum and minimum estimation of CE levels using QP detection. The exact QP values will be between the Max_{TR} and Min_{TR} curves. Further details about the modeling of the TR and the determination process of these curves are described in [260].

5.3.3 Required attenuation

The required attenuation for the DM filter can be estimated without the need of calculating the exact QP values. The predicted CE level at 160 kHz by Max_{TR} curve is 182.9 dBμV. By analysing this curve, the next switching frequency harmonic appears at 180 kHz and requires lower attenuation. Thus, the filter design will focus in the emissions at 160 kHz.

The limit specified at this frequency by CISPR 11 is $Limit_{CISPR,160kHz} = 65.5$ dBμV. A margin of 6 dB is added in order to account for possible inaccuracies in CE estimation, and also for the parasitics of the inductive and capacitive components [272]. In this way, the design process can be faster since the parasitic effects are not considered in the first step. Finally, the required attenuation of the DM filter at 160 kHz is:

$$\begin{aligned} Att_{req,DM} =& Max_{TR,160kHz} - Limit_{CISPR,160kHz} + \\ &+ Margin = 123.4 \ dB. \end{aligned} \tag{5.2}$$

5.3.4 Topology

In theory, there are a large number of filter topologies that can be employed for EMI filtering. Although, a low number of topologies are used due to cost and complexity reasons [272]. The second-order LC circuit is a very common topology employed as the input filter of MC [164]. In order to minimize the resonance that occurs at the filter natural frequency, active and passive damping solutions were proposed in [236, 259, 273]. Passive damping is achieved by adding a resistor in series or parallel with an inductor or capacitor. Considering the simple LC circuit, it was demonstrated in [153] that the minimum power losses are obtained with a resistor connected in parallel with the inductor. Moreover, this solution also reduces the global cost and volume of the input filter [146]. More complex damping networks can be obtained by adding an additional inductor or capacitor in series or parallel with the damping resistor [259]. The objective of these damping networks is to provide passive damping to a filter without increasing excessively the power dissipation. By modifying the peak output impedance, this damping aims to facilitate the controller design and avoid large oscillations during transients [272]. Fig. 5.3 shows two LC filter topologies with single resistor damping networks. Both have a high frequency attenuation asymptote given by $1/(\omega^2 L_f C_f)$, that is identical to the original undamped LC filter. For the shunt RC damping network, C_{fd} blocks the dc current in order to avoid significant power losses in R_d. However, the large total capacitance reduces the power factor for low-power operation making this solution unattractive. Regarding the series RL damping network, L_{fd} provides a dc bypass to avoid significant power dissipation

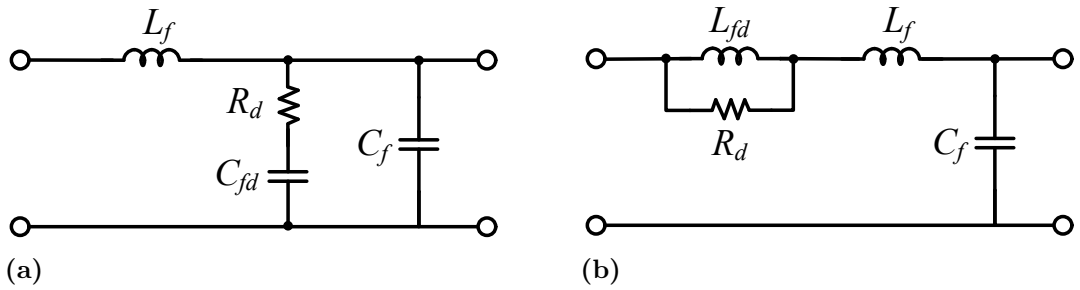


Figure 5.3: Two LC filter topologies with single resistor damping networks. (a) Shunt RC damping network. (b) Series RL damping network.

in R_d. Therefore, both inductors must be rated for the peak dc current. The output impedance of the LC filter is dominated by the inductor impedance at low frequency and by the capacitor impedance at high frequency [274]. Both asymptotes intersect at the filter resonant frequency:

$$f_0 = \frac{1}{2\pi\sqrt{L_f C_f}}. \tag{5.3}$$

As previously discussed, $V_{TR}(j\omega)$ is dependent of the DUT's input current. Therefore, $I_{dm}(j\omega)$ must be reduced in order to generate CE within the imposed limits. Transfer function $H_{lcrl}(s)$ which relates I_{dm} with I_i is defined in (5.4). The magnitude of $H_{lcrl}(s)$ characterizes the attenuation capability of a single-stage LC filter with series RL damping network (cf., Fig. 5.3(b)).

$$H_{lcrl}(s) = \frac{sL_{fd} + R_d}{s^3 C_f L_f L_{fd} + s^2 C_f R_d (L_f + L_{fd}) + sL_{fd} + R_d} \tag{5.4}$$

A compromise between damping and the size of L_{fd} must be done during the design process [274]. The damping ratio n_d defines the relation between inductor L_{fd} and L_f as:

$$n_d = \frac{L_{fd}}{L_f}. \tag{5.5}$$

For practical purposes, a unitary damping ratio is interesting since only one type of inductor needs to be built/purchased. According to [272], this solution also results in acceptable losses on R_d. As demonstrated in [259], the optimum damping resistance for the series RL damping network can be calculated as:

$$R_d = \sqrt{\frac{L_f}{C_f}} \frac{1 + n_d}{n_d} \sqrt{\frac{2(1 + n_d)(4 + n_d)}{(2 + n_d)(4 + 3n_d)}}. \tag{5.6}$$

Fig. 5.4 shows the impact of different damping factors in terms of resonance of $H_{lcrl}(s)$ for $C_f = 20\,\mu$F and $L_f = 60\,\mu$H. As expected, the peak in the magnitude is reduced

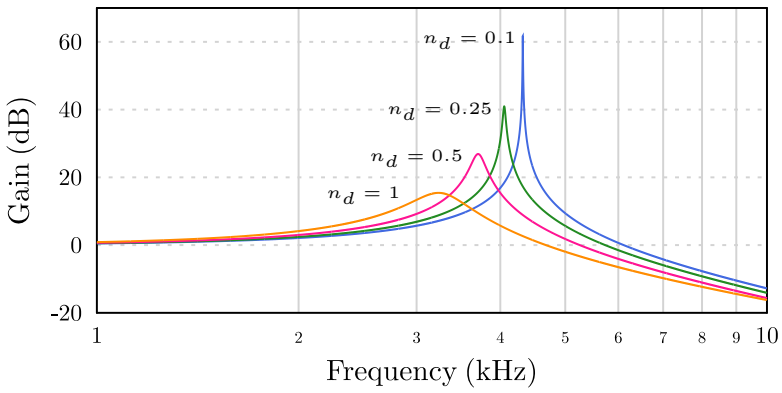


Figure 5.4: Impact of different damping factors in transfer function $H_{lcrl}(s)$.

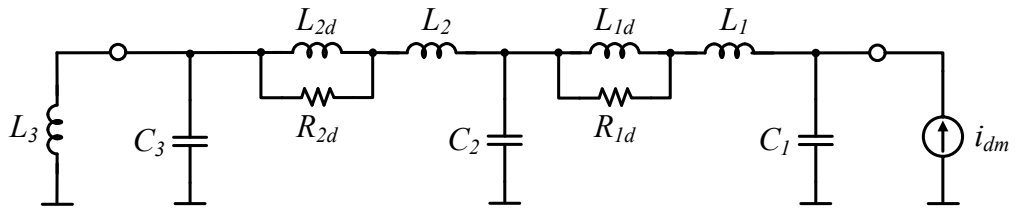


Figure 5.5: Equivalent single-phase circuit of the DM filter.

as damping is increased. Simultaneously, the frequency at which this peak occurs also decreases as damping rises. Nevertheless, the low and high frequency asymptotes are not affected by the damping factor. For a given attenuation, the cascade connection of multiple LC filter stages allows the reduction of volume and weight when compared with a single-stage LC filter [274]. This is achieved by increasing the cutoff frequencies of the multiple stages resulting in smaller inductance and capacitance values. Nevertheless, the interaction between cascaded LC filter stages can provoke additional resonances and increased output impedance. An approach to reduce this interaction is by selecting gradually smaller cutoff frequencies as it nears the filter output [259]. In other words, higher attenuation is required for the stages near the filter output to improve system stability.

5.3.5 Components

In order to provide the required attenuation a three-stage filter as shown in Fig. 5.5 is employed. Stage 1 and Stage 2 are formed by LC filters with series RL damping networks, and Stage 3 is formed by an undamped LC filter formed by C_3 and L_3. The DM capacitors drawn reactive current from the grid which decreases the operating PF. In order to have a minimum power factor during light load operation, the total capacitance must be limited according to the converter nominal power. In [232] the authors suggest that the PF must be at least 0.9 for operation at 10 % of P_{nom}. Other authors consider that a 0.8 power factor for the same operating conditions is reasonable [155]. The capacitance limitation can also be specified in terms of the absolute value for the reactive power. For instance, in [90] it is proposed that the reactive power drawn by the input filter must be restricted to 15 % of P_{nom}. Assuming a small voltage drop for the fundamental component across the filter inductors, the total reactive power absorbed can be calculated by (5.7). Considering this last criteria, the maximum capacitance per phase must be restricted to $C_{f,total} \leq 30\,\mu$F.

$$Q_{C_f} \approx 3 \cdot 2\pi \cdot f_g \cdot C_{f,total} \cdot V_{g,ln}^2 \tag{5.7}$$

Stage 1

The matrix converter is a voltage-fed topology and behaves as a current source at its input. Capacitor C_1 (C_F in Figure 4.1) is placed at the MC input in order to limit the voltage

ripple and ensure a correct system operation. For the worst operating conditions, the peak current at the MC input is $\hat{I}_i = 37\,A$. By defining $\delta_{vCf,pp}$ as the maximum peak-to-peak voltage ripple, the minimum required capacitance can be calculated as [275]:

$$C_1 \geq \frac{\hat{I}_i}{1.1 \cdot V_{g,ln} \cdot 2\pi \cdot f_s \cdot \delta_{vCf,pp}}. \tag{5.8}$$

By limiting $\delta_{vCf,pp}$ to about 5-10 % of the nominal input voltage [272, 275], the minimum required capacitance must be between 11.6 μF and 23.2 μF. Due to the discrete availability of capacitance values and also for practical implementation reasons, C_1 is selected to 20 μF.

The magnitude of the LF current harmonics can be affected if the resonant frequency (f_0) of the different filter stages is near the measurement range (up to 2 kHz). Although, the resonant frequency must be significantly lower than the switching frequency in order to provide sufficient attenuation at $f = f_s$. Therefore, it is common to choose a resonant frequency between 20 times the grid frequency and about one-third of the switching frequency [154]. Considering this criteria, the resonant frequency for Stage 1 must be between 1 kHz and 6.66 kHz. As previously discussed, the attenuation for this stage must be higher than the other stages, resulting in a lower resonant frequency for Stage 1 when compared to Stage 2. The attenuation for Stage 1 is selected as $Att_{Stage1} = 0.5 \cdot Att_{req,DM}$, which by the following:

$$f_{0,Stage1} = \frac{160kHz}{\sqrt{10^{\frac{Att_{Stage1}}{20}}}} \tag{5.9}$$

results in $f_{0,Stage1} = 4588$ Hz. Considering C_1 and (5.3), L_1 is calculated as 60 μH. For $n_{1d} = 1$, the damping network is composed by $L_{1d} = 60\,\mu$H and $R_{1d} = 3.4\,\Omega$ according to (5.5) and (5.6) respectively.

Stage 2

For practical reasons, L_2 and L_{2d} are selected to be equal to L_1 and L_{1d}. By defining $Att_{Stage2} = 0.35 \cdot Att_{req,DM}$, the resonant frequency of Stage 2 needs to be $f_{0,Stage2} = 13316$ Hz. Considering L_2 and (5.3), C_2 is calculated as 2.3 μF. Due to the discrete availability of capacitance values, C_2 is selected to be 2.2 μF. Finally, the unitary damping ratio results in $R_{2d} = 10\,\Omega$.

Stage 3

The third stage of the filter is composed by C_3 in combination with L_3. During test experiments, L_3 corresponds to the inner inductance of the LISN, L_{LISN}. For normal operation, L_3 coincide with the grid inductance, L_g. Although the grid inductance can vary significantly depending of the PCC, for this analysis $L_g = 50\,\mu$H is considered, following the reference network defined in IEC 61000-3-3 [255]. This stage must provide the remainder attenuation, which can be written as $Att_{Stage3} = Att_{req,DM} - Att_{Stage1} -$

Att_{Stage2}. Therefore, the resonant frequency of Stage 3 needs to be $f_{0,Stage3} = 53204$ Hz. Considering $L_3 = 50\,\mu$H, the respective capacitor is chosen to be $C_3 = 180\,n$F.

5.3.6 Evaluation of the DM filter

By combining all three stages, the complete transfer function H_{dm} from I_i to I_{dm} can be obtained. Fig. 5.6 depicts the frequency response of the DM filter. As required, a 123 dB attenuation is provided at 160 kHz. The effect of the damping networks is perceptible by comparing the gain at $f_{0,Stage1}$ and $f_{0,Stage2}$ with the gain at $f_{0,Stage3}$.

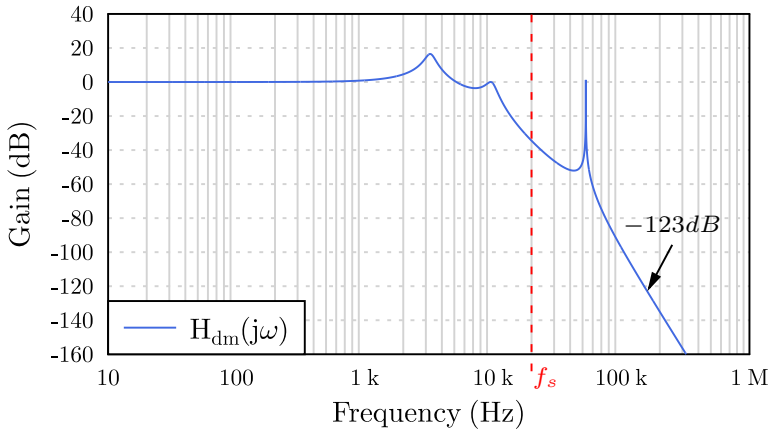


Figure 5.6: Frequency response of the DM filter: magnitude of H_{dm}.

Fig. 5.7 depicts Max_{TR} and Min_{TR} for the converter operation with the DM filter. As can be seen, the maximum curve for the predicted QP values is below the limits specified by CISPR 11 Class B curve and the selected margin of 6 dB can be observed. Thus, the DM filter design is considered to be concluded.

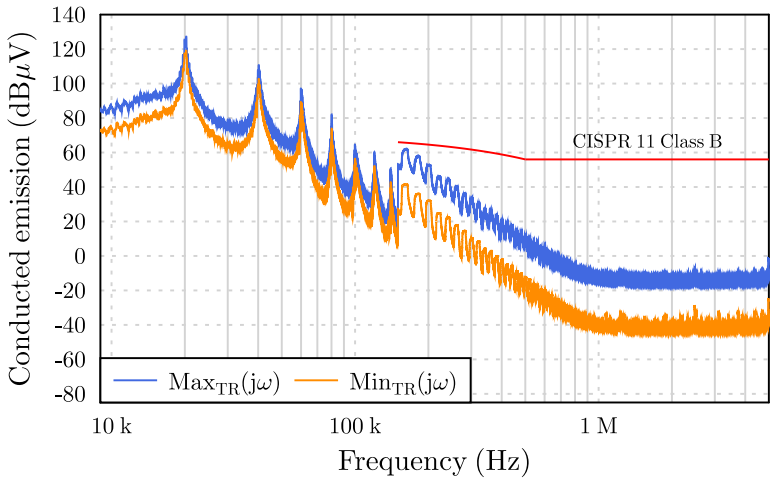


Figure 5.7: TR measurement with DM filter: maximum and minimum estimation of CE.

5.4 Design of Common-Mode Filter

5.4.1 Common-mode voltage

The CM voltage generated by the matrix converter induces a circulating current, i_{cm}, through the converter and the ground (see Fig. 5.10). This current closes the loop through the TR/LISN impedance resulting in CE that must be within the limits specified by CISPR 11. SiC MOSFET C2M0025120D [258] is used for the converter implementation. The parasitic capacitance from the semiconductor to the heat sink per unit area is approximated by $20\,pF/cm^2$ [265]. Considering this reference value, the parasitic capacitance of all the matrix converter's semiconductors is $C_{gh} = 600\,pF$. Regarding the transformer interwinding capacitance and the stray primary side wiring capacitance it is difficult estimate these values without making measurements. For this reason, a $1.2\,nF$ capacitance is added to the simulated circuit in order to take into account these parasitics. Thus, a total parasitic capacitance to ground $C_g = 1.8\,nF$ is considered. The resulting CM voltage, v_{cm}, impressed by the MC is represented in Fig. 5.8. This voltage has approximately 110 V_{rms} and a peak equal to $\hat{V}_{g,ln}$.

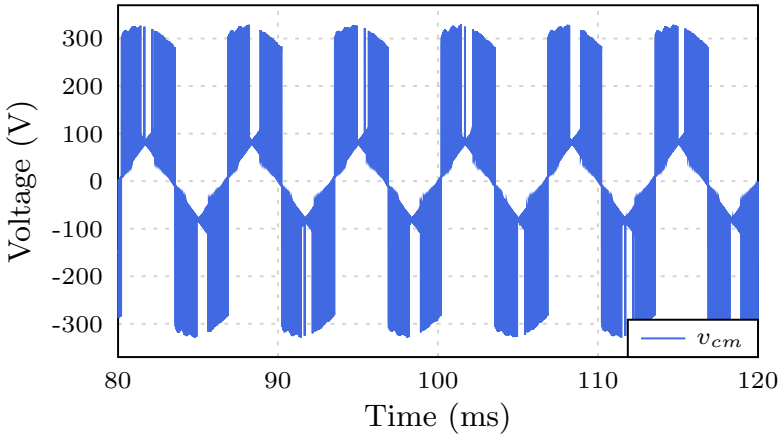


Figure 5.8: Common-mode voltage impressed by the matrix converter.

5.4.2 Spectrum of the measured voltage

The converter and the measurement system can be reduced to its single-phase equivalent CM circuit as represented in Fig. 5.10. It is important to note that, from the CM point of view, the three line-to-ground capacitors of each stage are in parallel. Thus, the effective common-mode capacitance is equal to the sum of the three capacitor values [276]. The LISN and the TR are modeled by its equivalent CM impedance. v_{cm} is modeled by an ideal voltage source. The C_g connected to the ground represents the parasitic capacitance. The spectrum of V_{TR} can be determined by the multiplication of $I_{cm}(j\omega)$ with the LISN's

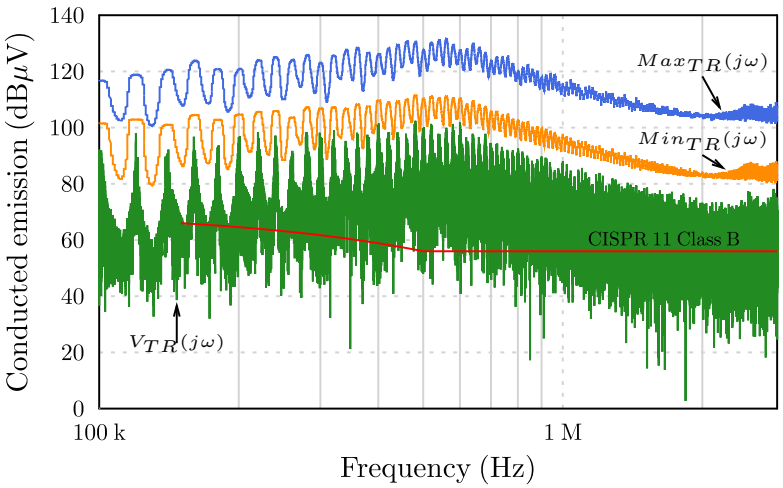


Figure 5.9: TR measurement without CM filter: maximum and minimum estimation of CE along with the spectrum of $V_{TR}(j\omega)$.

transfer function $G_{LISN,CM} = G_{LISN}/3$. Fig. 5.9 depicts the spectrum of V_{TR} at the LISN output terminals along with the Max_{TR} and Min_{TR} using QP detection.

5.4.3 Required attenuation

The required attenuation for the CM filter can be estimated without the need of calculating the exact QP values. The predicted CE at 160 kHz by $Max_{TR}(j\omega)$ curve is 123.7 $dB\mu$V. The limits specified in CISPR 11 Class B for CM are equal to the DM. Considering the limit at 160 kHz and including a margin of 6 dB, the required attenuation of the CM filter at 160 kHz is $Att_{req,CM} = 64.2\,dB\mu$V.

5.4.4 Topology

In order to limit i_{cm}, the EMI filter must maximize the mismatch between the power source and the converter impedances [277]. LC circuits are usually employed for the common-mode filter [278]. In contrast with the DM filter, no additional damping need to be added by external elements. The CM inductors are connected in series with the lines in order to provide a high-impedance for the common-mode noise. The three windings of the inductor are wound on the same core, which forms a common-mode choke. Because the power line currents are symmetrically displaced in each winding, the magnetic flux produced in the core by these currents cancels.

5.4.5 Components

In order to provide the required attenuation a two-stage CM filter is employed (see Fig. 5.10). Stage 1 and Stage 2 are formed by undamped LC filters that make the connection between the lines and the PE. The maximum value of the line-to-ground capacitance

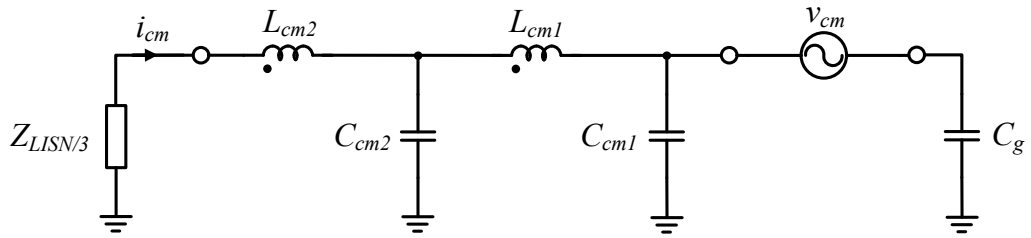


Figure 5.10: Equivalent single-phase circuit of the CM filter.

is limited by the leakage requirements imposed by several safety agencies [276]. This safety measure is necessary for protection of personnel against electric shock under fault conditions. According to IEC 60950, the ground leakage current for Class I equipments must be limited to $I_{leak,max} = 3.5\,mA$ at 50 Hz. This requirement has a great impact on the CM filter design. Considering the upper limit of the grid RMS voltage, a maximum total CM capacitance per phase of $C_{cm,max} = 44\,nF$ is calculated by:

$$C_{cm,max} = \frac{I_{leak,max}}{1.1 \cdot V_{g,ln} \cdot 2\pi \cdot f_g}. \tag{5.10}$$

According to [272], for maximum attenuation given a minimum total capacitance each stage shall present the same value. In order to provide some margin to the imposed limit of $C_{cm,max}$, a total capacitance per phase of 20 nF is chosen. Therefore, capacitors C_{cm1} and C_{cm2} must be 10 nF. Considering this capacitance, the value of the CM choke of each stage is then chosen to provide half of the required CM attenuation ($Att_{Stage1-2,CM} = 0.5 \cdot Att_{req,CM}$). The cut-off frequency is calculated by the following:

$$f_{0,Stage1-2,CM} = \frac{160kHz}{\sqrt{10^{\frac{Att_{Stage1-2,CM}}{20}}}} \tag{5.11}$$

resulting in $f_{0,Stage1-2,CM} = 25.2$ kHz. Taking into account this frequency, inductor L_{cm1} and L_{cm2} is selected to 1.3 mH.

5.4.6 Evaluation of the CM filter

By combining the two stages, the complete transfer function H_{cm} from I_i to I_{cm} is obtained. Fig. 5.11 depicts the gain of the CM input filter. As required, a 64 dB attenuation is provided at 160 kHz.

Fig. 5.12 depicts the maximum and minimum estimation of the CE for the converter operation with the CM filter. As can be seen, the maximum curve for the predicted QP values is below the limits specified by CISPR 11. Thus, the CM filter design is considered to be concluded.

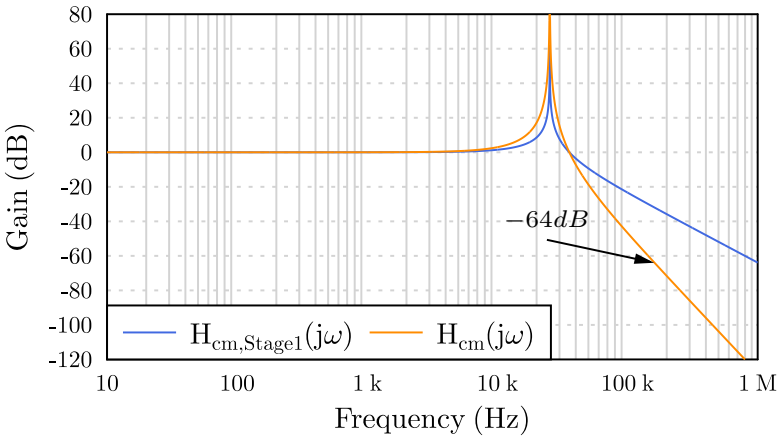


Figure 5.11: Frequency response of the CM filter: magnitude of H_{cm}.

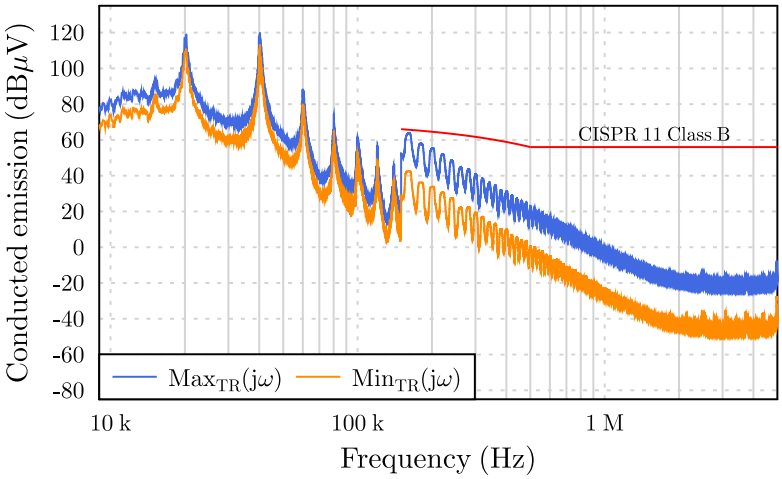


Figure 5.12: TR measurement with CM filter: maximum and minimum estimation of CE.

5.5 Integration of DM and CM filter

The final step for the design of the EMI filter is the integration of the DM and CM stages. There are several ways to perform this integration. Due to the imperfect coupling between the three windings of a CM choke, some leakage inductance is present in L_{cm1} and L_{cm2}. The inductors of both DM and CM filters can be combined in each stage, so that this leakage inductance can be employed as part of the required DM inductance. Using this strategy, a small DM inductor can be employed reducing the volume and weight of the filter. Fig. 5.13 shows the complete circuit of the EMI filter. All the components are listed in Table 5.1.

Toroidal cores are preferred for the DM inductors (L_1, L_{d1}, L_2, L_{d2}) since they create a low external magnetic field, reducing the magnetic coupling with other elements in the circuit. Iron powder material is selected since it presents a much higher saturation flux

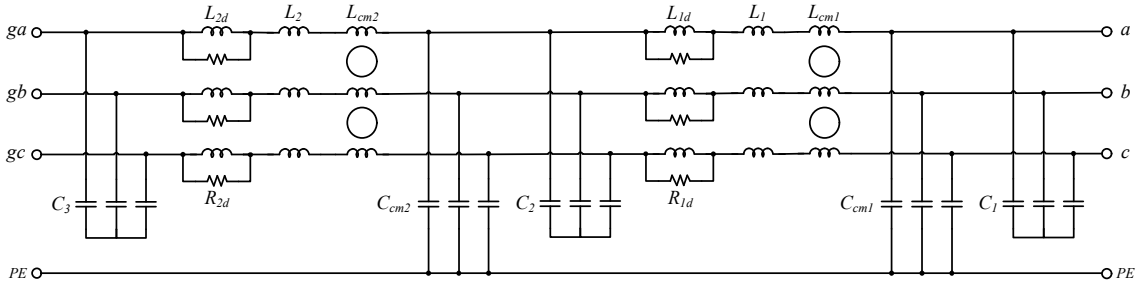


Figure 5.13: Complete circuit of the EMI filter comprising the DM and the CM filtering stages.

Table 5.1: Components for the EMI filter.

Component	Specification
C_1	EPCOS, MKP B32928C3206K, X2, 20 μF, 305 V_{ac}
C_2	EPCOS, MKP B32924C3225K, X2, 2.2 μF, 305 V_{ac}
C_3	Murata, GA3 GB563K, X7R, 56 nF, 250 V_{ac} ($\times$3)
L_1, L_{1d}	Micrometals, Iron Powder T184-52, 21 turns, 12 AWG
L_2, L_{2d}	Micrometals, Iron Powder T184-52, 21 turns, 12 AWG
R_{1d}	Bourns, SMD CRS, 3.3 Ω, 2 W
R_{2d}	Bourns, SMD CRS, 10 Ω, 2 W
C_{cm1}, C_{cm2}	Murata, Ceramic DE2F3KY, Y2, 10 nF, 250 V_{ac}
L_{cm1}, L_{cm2}	Schaffner, RB8532-16-1M3, 1.3 mH, 16 A

density than ferrites, resulting in a more compact inductor [272]. The distributed air-gap is also a constructive advantage when compared with ferrites. Cores from Micrometals [279] were chosen mainly due to its low-cost and availability in the market. The -52 material is suitable to be used in differential-mode filter applications. Core size T184 was selected in order to maintain inductance for the required energy storage. The inductor was constructed in a single layer in order to reduce the winding parasitic parallel capacitances. Furthermore, a solid round conductor is employed in order to take advantage from the increased resistance with frequency [272]. Using GeckoMAGNETICS [269] software, the required number of turns was projected in order to obtain the nominal inductance at half of the peak current. This criteria takes in account the 9.1 μH leakage inductance of the CM chokes (L_{cm1}, L_{cm2}). The losses for the designed DM inductors are estimated at 2.1 W with a 15°C temperature rise at P_{nom}.

Voltage surges due to electrical discharges and under voltages during load steps can appear at the MC input. Since the aforementioned voltages are usually high, metallized polypropylene capacitors (MKP) are selected for C_1 and C_2 due to its higher ripple current capacity and lower ageing compared with electrolytic capacitors [232]. Moreover,

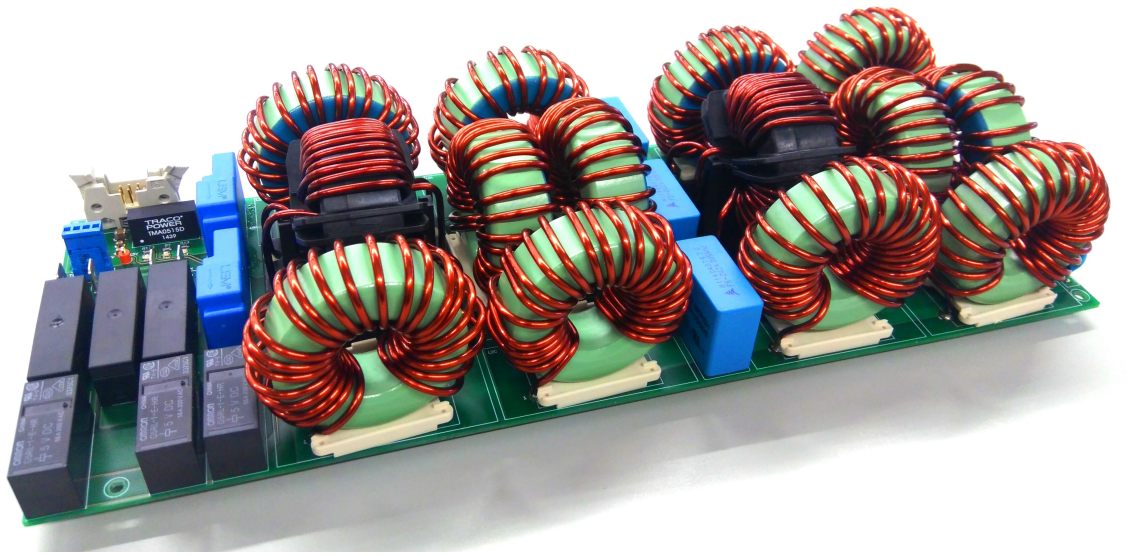


Figure 5.14: Photo of the EMI filter implementation.

capacitors from class X2 need to be chosen since they are specific for "across-the-line" applications. Capacitors from class X2 can withstand pulse peak voltages up to 2.5 kV in accordance with IEC 60664. Ceramic capacitors for C_3, C_{cm1} and C_{cm2} are preferred since a small capacitance is required, leading to a compact construction and low parasitics. Due to safety reasons, CM capacitors are from class Y2 that is specific for "line-to-ground" applications. These CM capacitors increase the total DM capacitance. However, since the CM capacitance is typically much smaller than the required DM capacitance little influence is to be expected [272]. Thus, no additional adjustments in the values of capacitances are necessary.

According to IEC 60950 standard, the capacitors connected across the lines should be discharged to a voltage lower than 60 V in less than 10 seconds after a supply disconnection. This is required since both DM and CM capacitors remain charged to the value of the mains supply voltage at the instant of disconnection. If a hand or other body part touch two pins of the mains supply plug at the same time, the capacitors will discharge through that body part. This discharge can be quite painful and for this reason, resistors of large value are connected across the lines in parallel with such capacitors. In this EMI filter, a 130 kΩ and 2 W SMD resistors are employed.

Fig. 5.14 shows a photo of the implemented filter. The PCB also includes current sensors, relays and fuses for protection. C1 capacitors are mounted in another board near the SiC MOSFETS in order to reduce the parasitic inductances.

As discussed in section 5.2, low-frequency current harmonics are generated by the converter and are mainly dependent of the employed modulation. Although, the resonant frequencies of the EMI filter could make interference in this measurement range. A final simulation with the integration of DM and CM filters was performed. Fig. 5.15 shows the

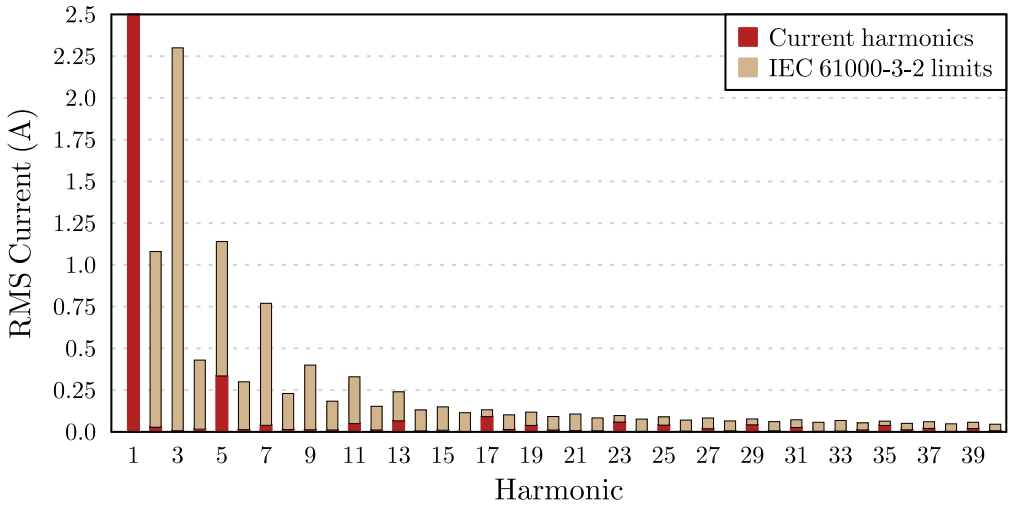


Figure 5.15: Low-frequency harmonics of grid current compared to IEC 61000-3-2 limits: simulation with the EMI filter comprising the DM and CM filters.

measured low-frequency harmonics of the grid current and compare with the IEC 61000-3-2 [267] Class A limits. As can be seen, the limits were not exceeded and the effectiveness of the EMI filter is verified.

5.6 Experimental Results

EMI filters are usually characterized by the insertion loss (IL) that is a measure of the interference suppression capability of a filter [266]. IL can be determined using the scattering s-parameters defined for the 2-port network circuits. The most accurate way to measure s-parameters is using a vector network analyzer (VNA) [280]. The test procedure is specified in CISPR 17 [281] standard. Fig. 5.16 shows the test circuits used for measuring the IL for the DM and CM stages. The VNA generates a signal with a pre-defined power and variable frequency at its port 1. This signal is then propagated through the DUT and measured at the VNA port 2. CISPR 17 specifies that the source and load impedances of the VNA must be equal to $Z_0 = 50\,\Omega$. Since the impedances are matched, IL coincide with the magnitude of the forward transmission coefficient S_{21}, as defined by (5.12).

$$IL = -20 \cdot log_{10}|S_{21}|, dB \tag{5.12}$$

Balanced-unbalanced transformers, also known as "baluns", must be connected to the VNA ports in order to isolate the DUT from the ground plane during DM measurements, as represented in Fig. 5.16(a). Moreover, the baluns are essential to provide very high CM rejection. The Coilcraft PWB1010LB [282] wideband transformer was mounted in a shielded housing with BNC receptacles as shown in Fig. 5.17, resulting in a $50\,\Omega : 50\,\Omega$ balun with a 3.5 kHz to 125 MHz bandwidth. A Rohde-Schwarz ZVL 3 with an operating

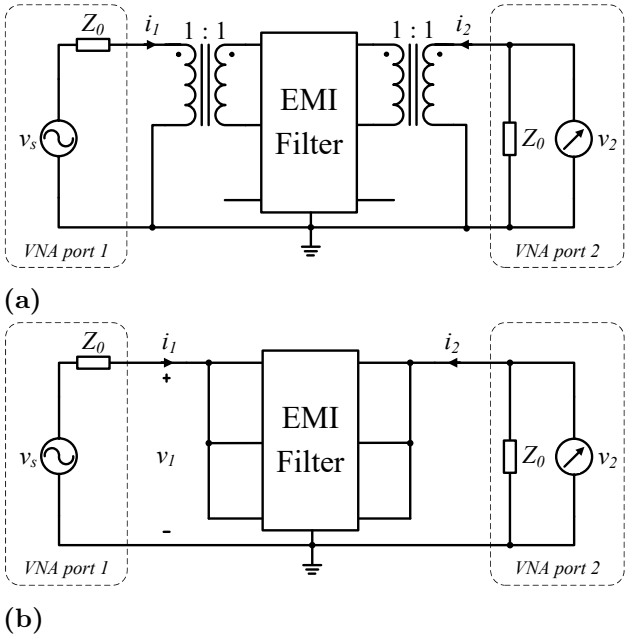


Figure 5.16: Test circuits for measuring the insertion losses in EMI filters: (a) differential-mode (symmetrical), (b) common-mode (asymmetrical).

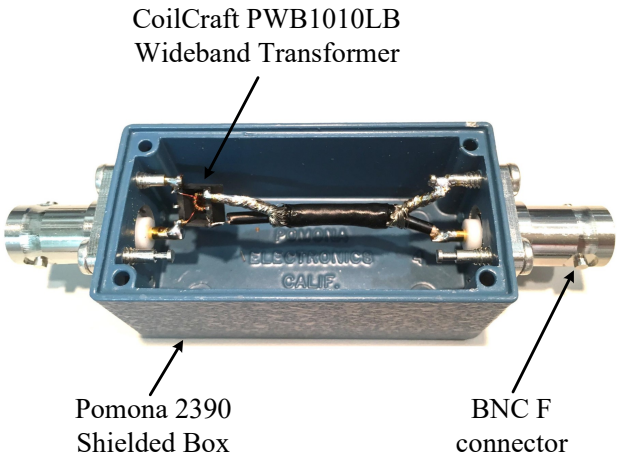


Figure 5.17: Photo of the constructed balun for DM S_{21} parameter measurement.

frequency range from 9 kHz to 3 GHz was employed for the measurements. Coaxial cables with a characteristic impedance of 50 Ω were used to connect the DUT to the measurement equipment. The test bench with the baluns and the VNA is shown in Fig. 5.18.

The DM S_{21} parameter was measured between phase A and B with the other lines remaining unconnected. Fig. 5.19(a) depicts the obtained results for the DM Stage 2 and also for the series of Stage 1 and Stage 2. As measured by the R&S ZVL 3, $S_{21,dm,Stage2} = -50.2\,dB$ for Stage 2 and $S_{21,dm,Stage1-2} = -92.4\,dB$ for Stage 1 and 2. The former result is inferior compared with the expected $104.9\,dB$. This is justified since the measurements are performed with a power of 20 dBm (equivalent to 100 mW). For this power level, the

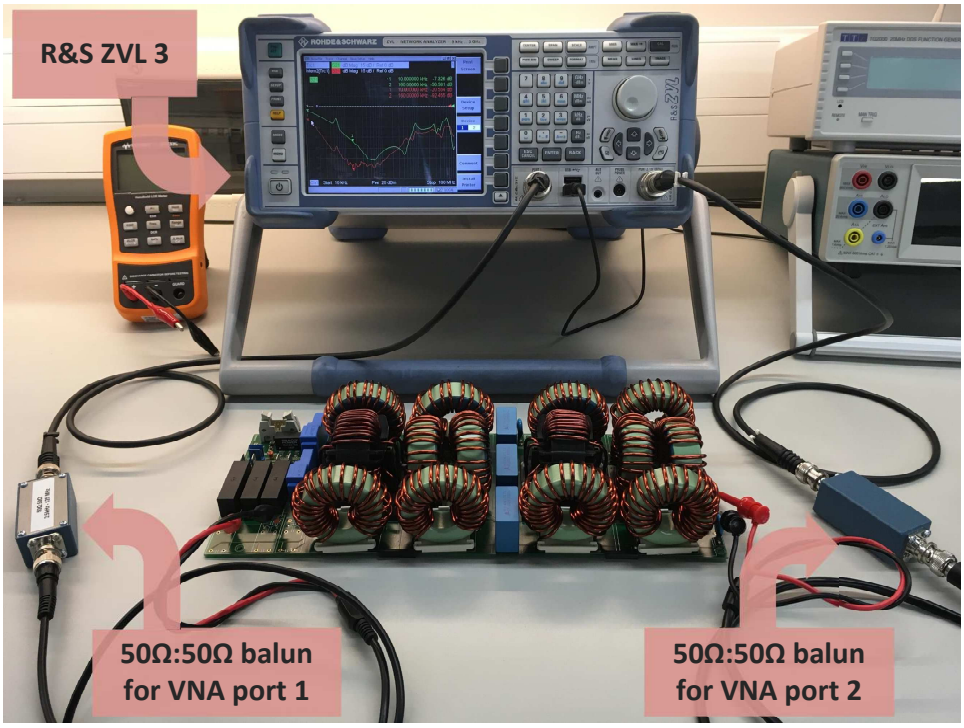
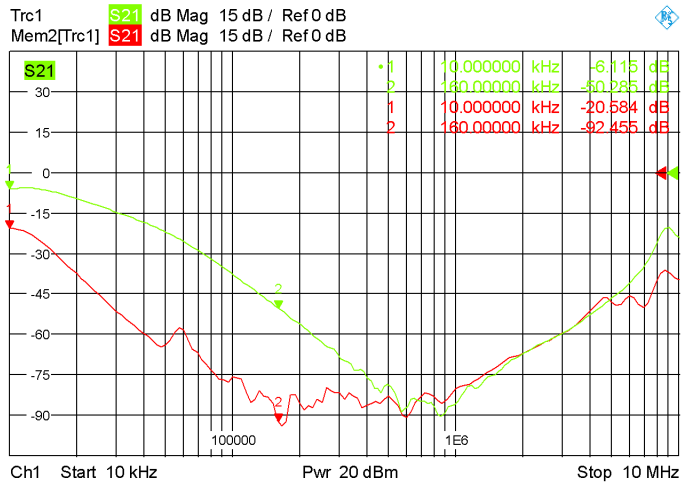


Figure 5.18: Photo of the test bench for measuring the DM insertion losses.

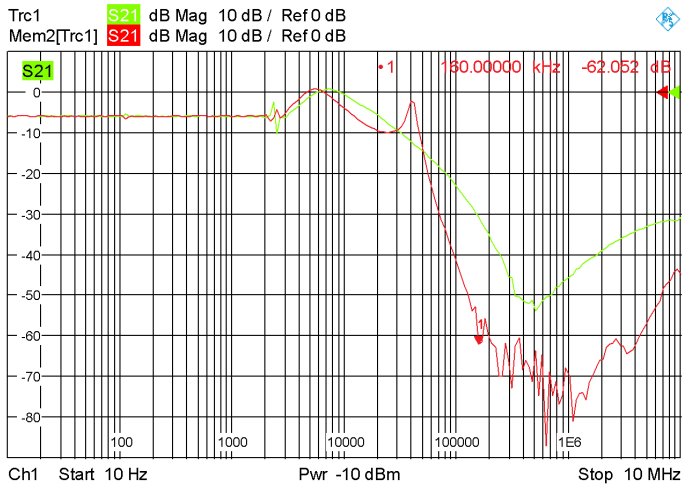
DM inductors have a higher inductance as explained in section 5.5. Consequently, a shift in the resonant frequency occurs resulting in a smaller attenuation. However, this is not a problem since for higher currents the effective inductance is within the expected range.

For the CM S_{21} parameter measurement, the baluns are not needed since the ground plane of the VNA is directly connected to the PE terminal of the EMI filter. Fig. 5.19(b) depicts the obtained results for the CM Stage 1 and also for the series of Stage 1 and Stage 2. As specified in section 5.4, each stage must provide half of the required attenuation, more specifically 32.1 dB. As can be seen, $S_{21,cm,Stage1} = -31.2\,dB$ for one stage and $S_{21,cm,Stage1-2} = -62.0\,dB$ for the complete CM filter. These values are clearly aliened with the predicted ones.

With the results exported by the R&S ZVL 3, the insertion losses were computed using (5.12) and depicted in Fig. 5.20. It is clearly noticed that parasitic effects limit the achievable insertion losses and degraded the EMI filter performance for frequencies above 1 MHz. This can be explained by the parasitic series inductance of capacitors and the capacitance across the choke coils [283]. However, the required attenuation at these high-frequencies is lesser than the attenuation required at 160 kHz. This margin can be observed at the curves represented in Fig. 5.7 and Fig. 5.12. Therefore, the performance of the filter is not compromised and complies with the specifications.



(a)



(b)

Figure 5.19: S_{21} parameter of the EMI filter measured with R&S ZVL 3 VNA: (a) differential-mode $S_{21,dm,Stage2}$ (Trc1) and $S_{21,dm,Stage1-2}$ (Mem2), (b) common-mode $S_{21,cm,Stage1}$ (Trc1) and $S_{21,cm,Stage1-2}$ (Mem2).

5.7 Conclusion

This chapter details a step-by-step design method for the DM and CM filters of the HFLMC. Each filtering stage is projected based on the required attenuation for CISPR 11 Class B pre-compliance. Both filters are integrated in a synergistic way in order to reduce volume and weight. A prototype of the filter was constructed and tested in the laboratory. An experimental test bench was mounted to determine the insertion losses according to the CISPR 17 standard. The obtained results confirm that the attenuation capability of the filter is within the expected range. This filter will be integrated in the final prototype at the input of the matrix converter, as detailed in Chapter 6.

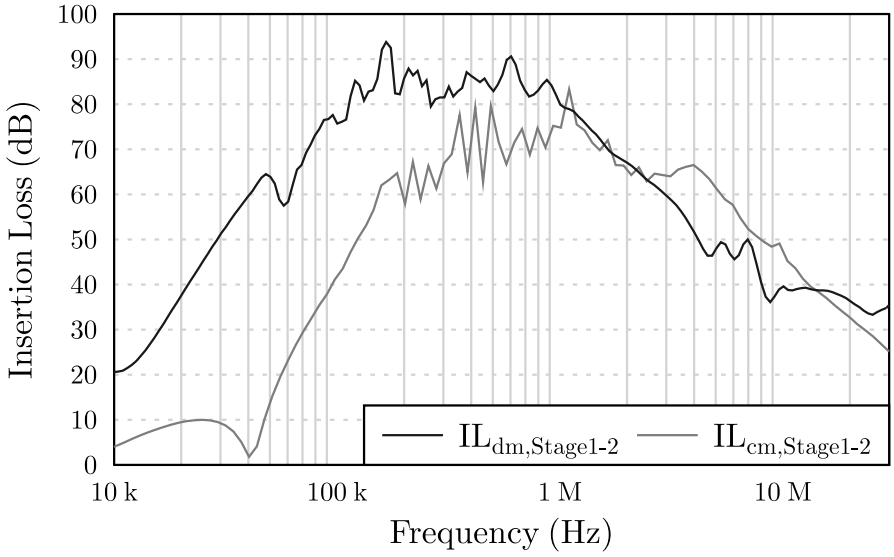


Figure 5.20: Measured insertion losses for DM filter ($IL_{dm,Stage1-2}$) and CM filter ($IL_{cm,Stage1-2}$).

Chapter 6

Prototype and Experimental Results

6.1 Introduction

This chapter describes the efforts to construct a prototype according to the parameters in Table 4.5 in order to validate the proposed modulation and the control architecture. Firstly, the main components and the different subsystems of the prototype are described in detail. Secondly, the several experiments that were performed are described along with the obtained results. It is also presented the commutation of the bidirectional switches, the high-frequency link operation, the harmonics of the grid current, the grid currents controller, the battery voltage and current controllers, and the PQ controller.

6.2 Description of the Prototype

The block diagram of the constructed prototype is represented in Figure 6.1. As can be seen, there are five main blocks: EMI Filter, 3x2 Matrix Converter, Transformer and Link-inductor, Full-bridge, and Control. The EMI Filter was already detailed in Chapter 5. It is only important to refer that the grid currents are measured directly at the PCC, right at the input of the EMI filter. Regarding the Transformer and Link-inductor, the respective project and construction is described in Appendix E. The 3x2 Matrix Converter block includes the gate drivers for the 12 SiC MOSFETs that are mounted on the heatsink and bellow the PCB. The three-phases that came from the EMI filter are connected to the C_1 capacitors at the MC input. The single-phase output of the 3x2 MC is then connected to the power transformer and link-inductor. The transformer's secondary is linked to the FB which in turn makes the interface with the battery. This PCB has the gate drivers for the four SiC MOSFETS, the voltage and current sensors, and also includes the DC filter and relay. Control PCB has a DSP and a FPGA, and the circuits for signal conditioning of voltages and currents measurement.

To implement the different parts of the functional prototype, four PCBs were designed as documented in Appendix H. The first step was to create a schematic with all the

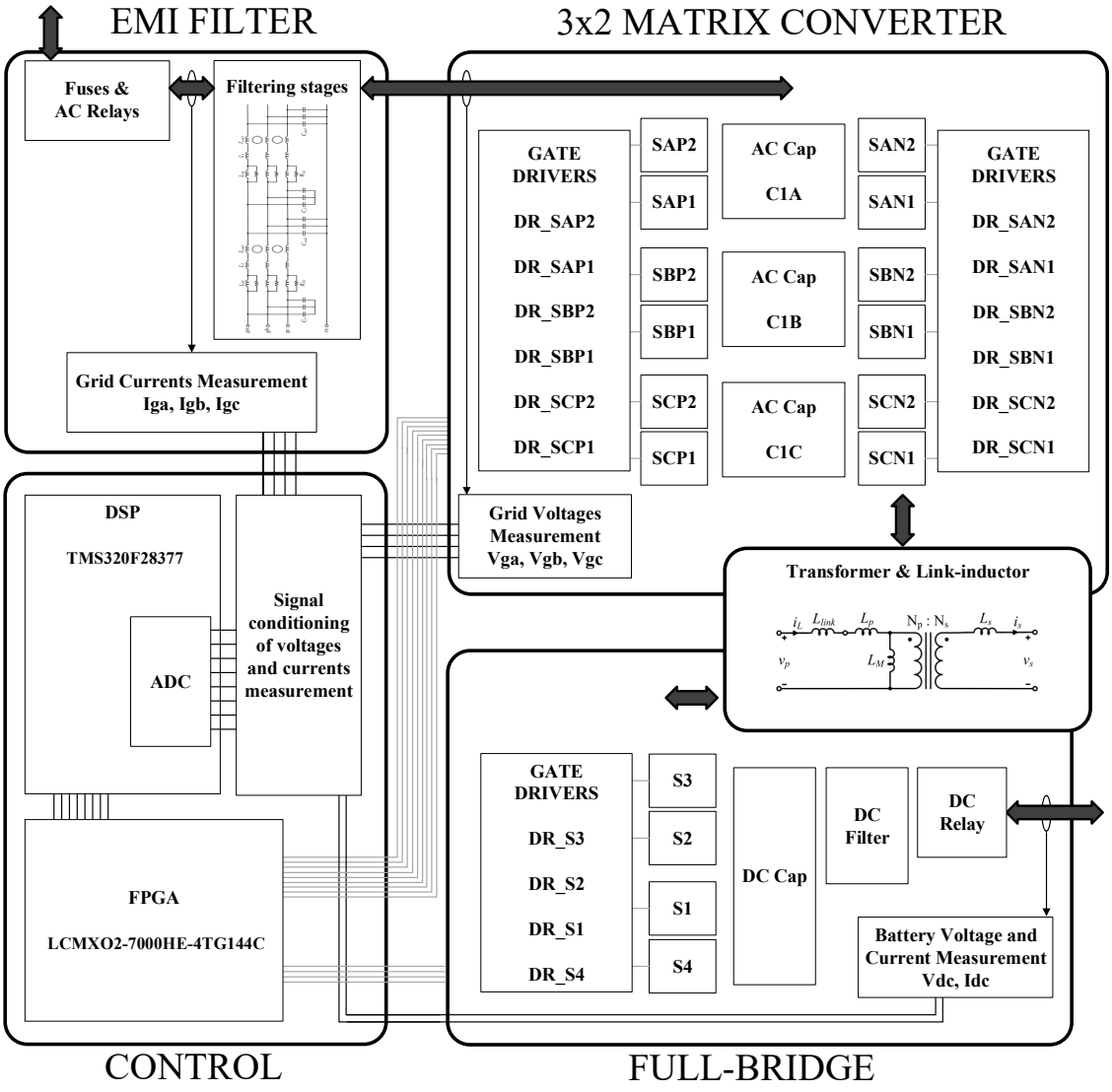


Figure 6.1: Block diagram of the functional prototype.

components, including the circuits for voltages and currents measurement, gate driver for the MC and FB, analogue circuits for signal conditioning, and the interfaces with DSP and FPGA. The PCB schematics are represented in Figure H.1 - Figure H.4, and Figure H.8. The layout of the PCBs is composed by 2 layers, as illustrated in Figure H.5 and Figure H.9. In order to ensure the required current carrying capacity, a copper trace width of 95 μm was selected for the PCBs production. The PCB images submitted for production are represented in Figure H.6, Figure H.7, Figure H.10, and Figure H.11. The PCBs were produced externally by a manufacturer. All the components were then soldered on the four PCBs at the SGEV laboratory of INESC TEC. Following, the main components and the different subsystems of the prototype are described in detail.

6.2.1 Voltage and current measurement

Accurate measurements of voltages and currents are essential to ensure a proper control of the converter. For safety reasons, galvanic isolation between the control system and the grid/battery pack must be provided by the measurement circuit. Additionally, high common-mode transient immunity, low signal-to-noise ratio (SNR), low offset, high gain accuracy, and stability are also crucial for the measurements. An additional circuit for signal conditioning is also necessary to adapt the voltage to the 0-3 V range of the analog to digital converters (ADC) of the digital signal processor (DSP).

Typically, optical isolation amplifiers are employed as voltage sensors due to its performance and availability in a compact package. The grid and battery voltages are measured using respectively the ACPL-C79B and the ACPL-C87B isolation amplifiers. Both have ±0.5 % gain tolerance, 15 kV/μs common-mode transient immunity, and less than 0.1 % non-linearity. Figure 6.2 shows the circuit used for the measurement and signal conditioning of grid voltages ($v_{ga,b,c}$). The voltage divider is composed by *R3*, *R5*, and *R7* to create a voltage at the primary of isolation amplifier. The 8.2 V/V gain of the ACPL-C79B amplifies this voltage to the secondary side. Since the grid voltage is bipolar, an offset must be added to do the adjustment of the signal to the ADC range. An offset of 1.65 V is generated through resistors *R254* and *R244*. Finally, the operational amplifier OPA2350 provides the necessary attenuation to represent the signal in the remainder ±1.35 V voltage range. The power supply is provided by isolated 1W DC-DC converter TMA0505S.

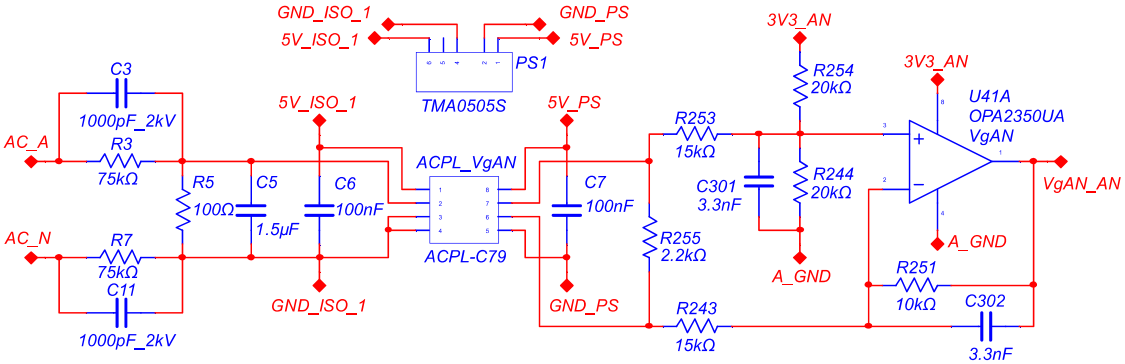


Figure 6.2: Circuit for the measurement and signal conditioning of grid voltages ($v_{ga,b,c}$).

Figure 6.3 shows the circuit used for the measurement and signal conditioning of battery voltage (v_{dc}). The same principle presented before for the measurement of grid voltages is applied. Although, the ACPL-C87B with its 1 V/V gain was preferred since v_{dc} is always positive.

There are several methods for currents measurement, such as the resistive shunt, inductive sensors, magneto-resistive, and hall effect sensors. In this work, the hall effect

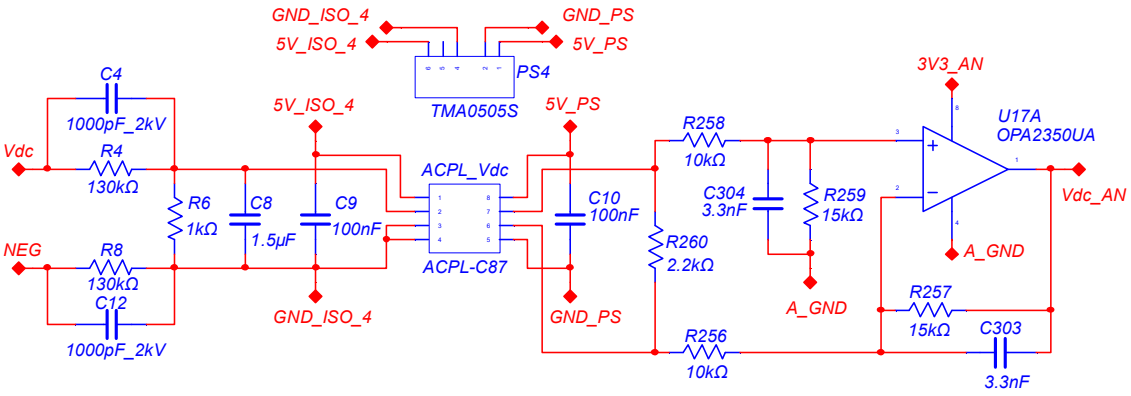


Figure 6.3: Circuit for the measurement and signal conditioning of battery voltage (v_{dc}).

measuring principle was preferred. The magnetic flux created by the current that circulates in the sensor's primary winding is concentrated in a magnetic circuit and measured in the air gap using a Hall device. The output signal from the Hall device is then conditioned to provide an exact representation of the primary current. This method ensures galvanic isolation and features low insertion losses. For the grid currents measurement the LEM HY15-P was employed due to its high sensitivity and extended measuring range. Figure 6.4 shows the circuit used for the measurement and signal conditioning of grid currents ($i_{ga,b,c}$). This circuit was designed to measure ±25 A peak which produces a voltage in the range ±6.67 V at the sensor output. Since this voltage is bipolar it is necessary to add an offset and also attenuate the signal to adapt the voltage to the ADC's 0-3 V range.

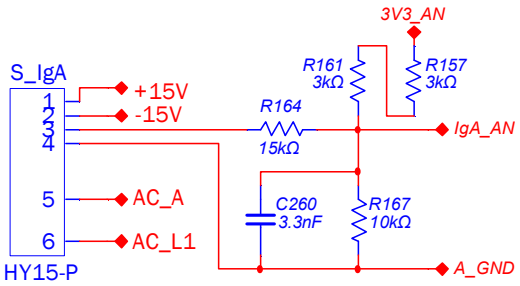


Figure 6.4: Circuit for the measurement and signal conditioning of grid currents ($i_{ga,b,c}$).

Regarding the measurement of the battery current, the ACS712-ELCTR-30A-T sensor from Allegro was preferred due to its compactness. This sensor also present the following features: low power loss, 2.1 kV isolating voltage, ratiometric output from the supply voltage, and 66 mV/A output sensitivity. This is an economical, easily, and implementable solution taking into account that the sensor can be supplied with unipolar voltage (0-V_{CC}). Therefore, no offset needs to be added to the sensor output since it produces half of V_{CC}

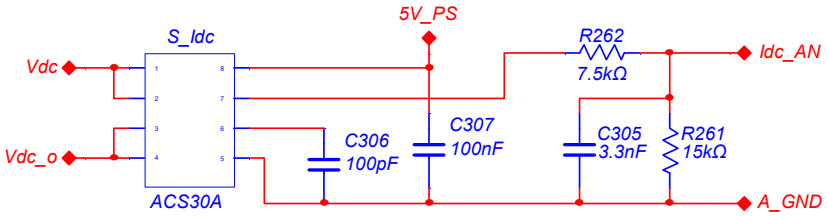


Figure 6.5: Circuit for the measurement and signal conditioning of battery current (i_{dc}).

for zero current. The signal only needs to be attenuated for the voltage range of the ADC, which is done through *R261* and *R262*.

Figure 6.6 shows a photo of the PCB with the implemented circuits for signal conditioning of voltages and currents described above. These circuits are placed near the pins of the ADC of the DSP to reduce the noise interference after the signal conditioning.

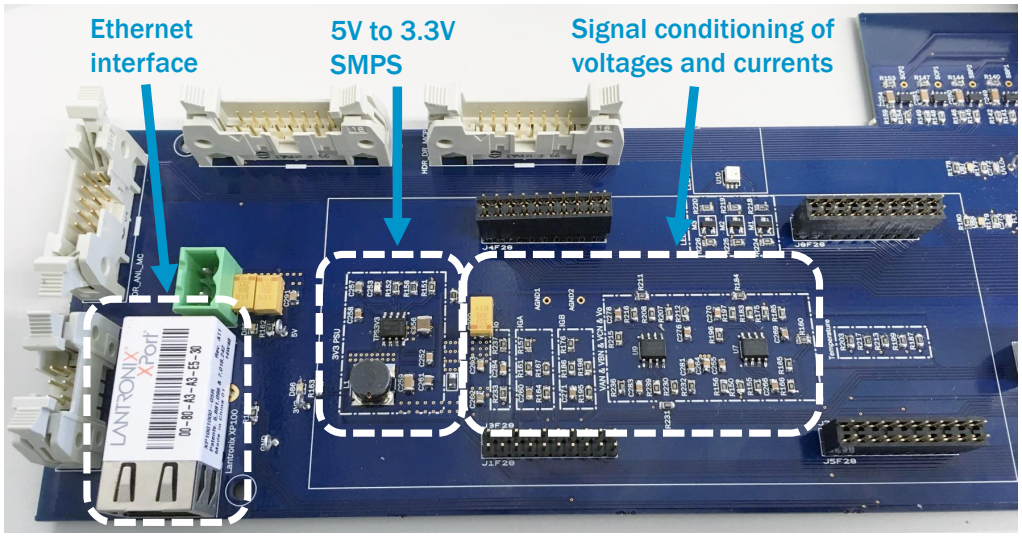


Figure 6.6: Photo of the circuits for signal conditioning and the Ethernet interface.

6.2.2 Control system based on DSP plus FPGA

The proposed modulation requires a non-standard PWM peripheral for the generation of all 16 command signals. The more advanced PWM peripherals typically available in DSP, such as the ePWM Type 4 from Texas Instruments, do not have enough compare events to implement the modulation. Therefore, a more flexible platform is necessary for this application.

Considering the computational requirements, a control system based on DSP plus FPGA was designed as represented in the architecture of Figure 6.7. The TMS320F28377

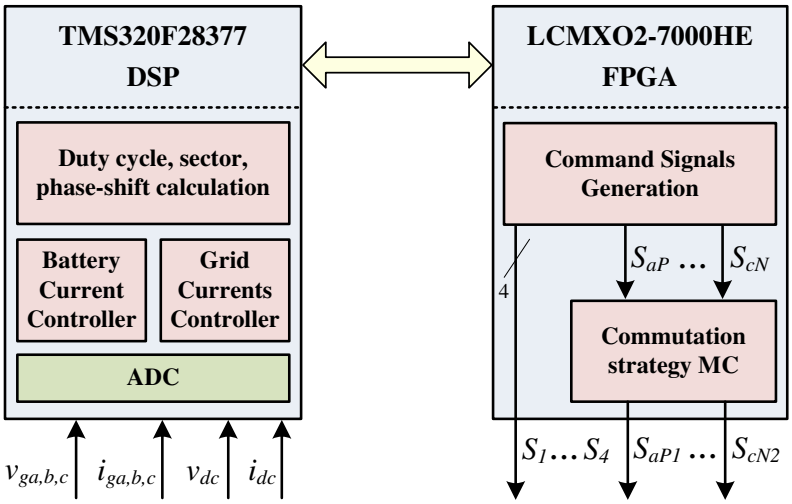


Figure 6.7: Architecture of the control system based on DSP plus FPGA.

DSP from Texas Instruments is a powerful 32-bit floating-point microcontroller with 200 MHz clock, 12-bit ADCs, and a trigonometric math unit (TMU). This DSP is responsible for the acquisition of the voltages and currents measurements previously discussed. The sampling is performed four times by each modulation period which corresponds to a sampling rate of 80 kHz. A moving average algorithm, based on a 3rd-order FIR filter, is implemented to weigh all the samples. The control algorithms presented in Section 4.3 are also implemented in the DSP. Figure 6.8 shows the implementation structure of part of the modulation in the DSP. The control loop is executed at 20 kHz in order to update the command variables at every cycle of the modulation. As can be seen, the sector detection and the duty-cycle calculation are processed by using the angle information from the PLL. Following the architecture described in [250], the PLL was implemented in a synchronous reference frame. Using the symmetrical optimum method, the gains for the loop filter were tuned as $K_{p,PLL}$=0.3 and $K_{i,PLL}$=1.74.

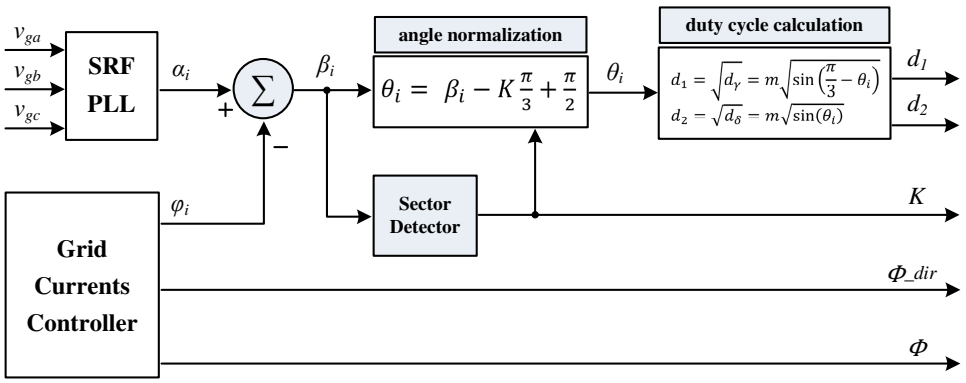


Figure 6.8: Implementation structure of part of the modulation in the DSP.

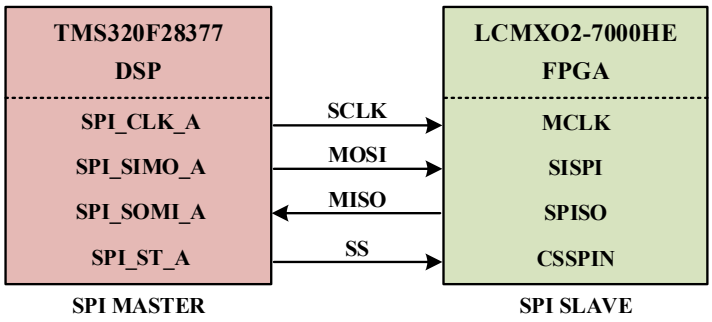


Figure 6.9: Communication bus between DSP and FPGA through SPI in a single master to single slave architecture.

In turn, the MachXO2 LCMXO2-7000HE-4TG144C FPGA from Lattice implements the current commutation strategy for the MC and generates the command signals for the 16 SiC MOSFETs. This FPGA has up to 114 user I/Os and offers embedded Flash technology for instant-on, non-volatile operation in a single chip. To provide a precise clock for the control logic, the 200 MHz crystal oscillator FXO-HC736R-200 was added to the breakout board at pin 27. Besides the MachXO2 includes two inter-integrated circuit (I2C) bus, communication by serial peripheral interface (SPI) was chosen since has complete protocol flexibility. Furthermore, the full-duplex capability makes SPI very simple and efficient for single master/single slave applications. Therefore, both control platforms communicate through SPI in a single master to single slave architecture, as represented in Figure 6.9. The SPI bus specifies four logic signals:

- SCLK: Serial Clock (output from master)
- MOSI: Master Output Slave Input (data output from master)
- MISO: Master Input Slave Output (data output from slave)
- SS: Slave Select (output from master)

Communication is initiated by the bus master that configures the clock, using a frequency supported by the slave device. In this applications, the SCLK was defined as 1.35 MHz in the DSP configuration. The master then selects the slave device through the SS line that is active low. During each clock cycle, a full duplex data transmission occurs. The master sends a bit on the MOSI line and the slave reads it, while the slave sends a bit on the MISO line and the master reads it. This FPGA includes a hard SPI core that can save several Lookup tables (LUTs) when compared to the implementation in FPGA logic. The SPI module has a 8-bits architecture that is used to access the data and control registers.

A 20 kHz frequency corresponds to a modulation period $T_s = 50$ μs. This cycle can be generated inside the FPGA using a counter that increments with the 200 MHz clock from the crystal oscillator. Therefore, the 50 μs modulation period corresponds to a counting value of 10000. Duty-cycles d_1 and d_2 are calculated by the DSP and need to

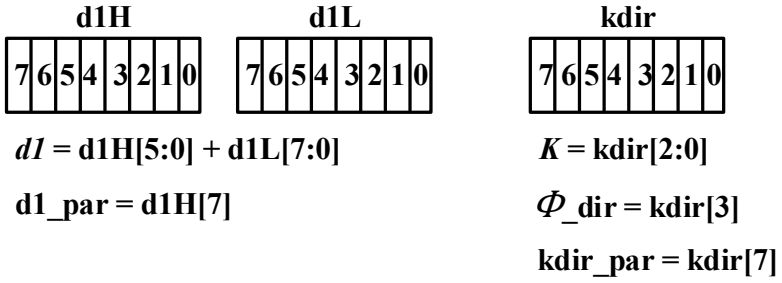


Figure 6.10: Data codification for SPI transmission.

be transmitted to the FPGA. These duty-cycles are float variables and take values in the range [0, 1]. Since duty-cycles need to be in the range [0, 10000] inside the FPGA, a scaling factor of 10000 is applied inside the DSP before being transmitted by SPI. Therefore, only 14-bits are necessary to represent values in this range. Taking in account that the frame should be constructed using data blocks of 8-bits, two bytes are necessary for each duty-cycle and the phase-shift. For example, d_1 is represented by the two bytes d1H and d1L. Bits [5:0] of d1H are the most significant bits of d1 whereas byte d1L has the least significant bits of d_1. By concatenating d1H[5:0] with d1L[7:0] it is possible to obtain duty-cycle d_1. In order to check if some error occurred during data transmission, a parity bit is included in the SPI frame for each variable. The parity bit is determined by the XOR operation between all bits of d_1, which is inserted in d1H[7] by the DSP. Then, the FPGA checks if the parity is even: d1H[7] is logic high if d1 has odd number of 1's. Duty-cycle d_2 is encoded using the same approach. Figure 6.10 shows how these variables are codified to be transmitted by SPI. Phase-shift Φ is a float variable and take values in the range [-1, 1]. In order to transmit this information to the FPGA as an unsigned value, the phase-shift modulo is encoded using the same method as d_1 and d_2 except for the scale factor that is 8192 (2^{13}). The signal of Φ is sent in byte kdir along with information about the sector of SVM. If $\Phi \geq 0$ then kdir[3] is 1 and if $\Phi \leq 0$ then kdir[3] is 0. The sector of SVM is an unsigned int variable and take values in the range [1, 6]. This information is encoded in kdir[2:0]. The parity bit of kdir is inserted in kdir[7] using the same approach described above. As a result, the SPI frame is divided in seven blocks of 8-bits, as depicted in Figure 6.11. MOSI line has the variables transmitted by the DSP. Then, the FPGA

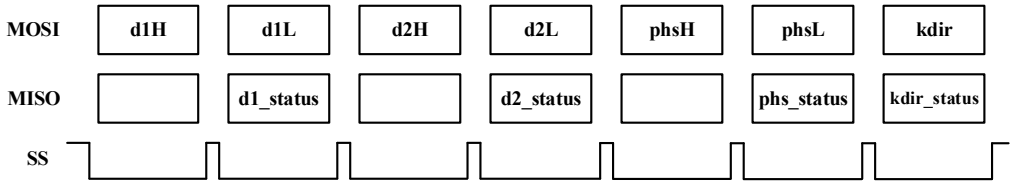


Figure 6.11: SPI frame to transmit d_1, d_2, Φ, K and Φ_{dir}.

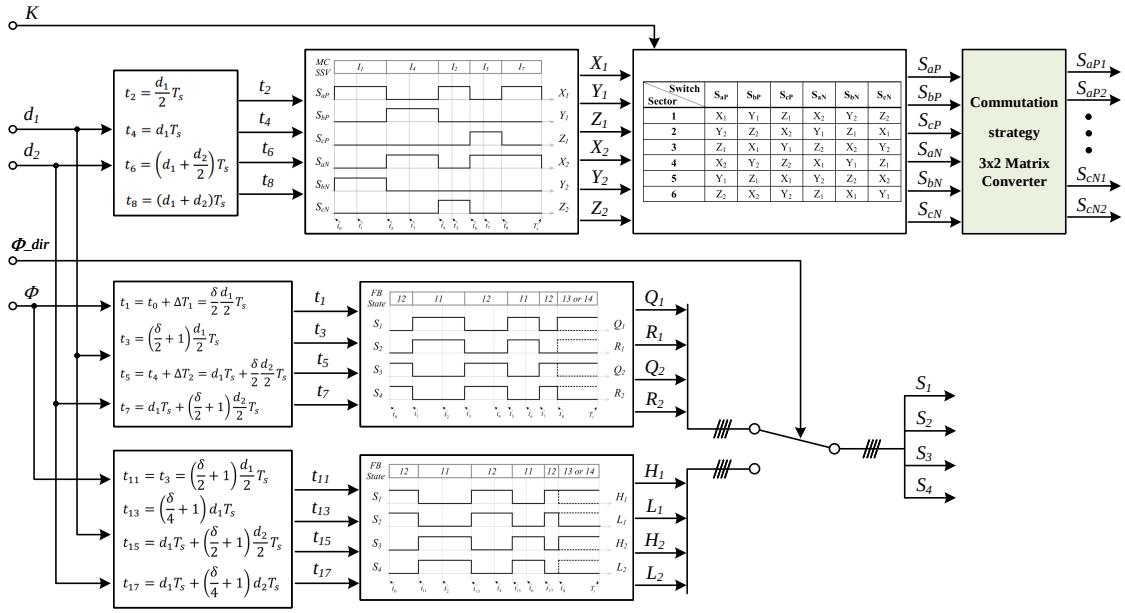


Figure 6.12: Implementation structure of part of the modulation in the FPGA.

has a state machine that receives this information using the SS signal to know the actual byte number inside the SPI frame. The FPGA provides feedback through the MISO line regarding possible transmission errors that are detected using the parity bits. After a sequence of error messages, the DSP can interrupt the operation and safely shut-down the converter.

The values of duty-cycles, sectors, and the phase-shift provided by the DSP are used by the FPGA to implement the modulation following the implementation structure represented in Figure 6.12. In a first stage, the whole timing instants are calculated using the duty-cycles and the phase-shift values. These timing instants are then compared with a counter to generate the intermediate signals (X_1, Y_1, Z_1, ..., Q_1, R_1, ..., H_2, L_2). These intermediate signals are routed to the input of the commutation strategy block as a function of the sector K. Finally, the command signals to the matrix converter (S_{aP1}, S_{aP2}, ..., S_{cN1}, S_{cN2}) are generated by the commutation strategy. Regarding the full-bridge, the intermediate signals are routed according to the phase-shift direction. It is important to note, that an active-high complementary dead time is incorporated in the command signals of the FB to avoid short circuits during the commutation.

Taking in account the review of current commutation strategies presented in Section 3.4, the Variable-step VBC strategy was selected for this implementation. By properly alternating between the two-step uncritical commutation and the four-step critical commutation approaches a safe VBC with minimum switching losses is ensured by this strategy. Figure 6.13 shows the switching state machine diagram for commutation in normal (I, II) and critical (I-II, II-III) intervals. The thick solid lines show the paths for commutations within each normal or critical interval, and the dashed lines with arrows

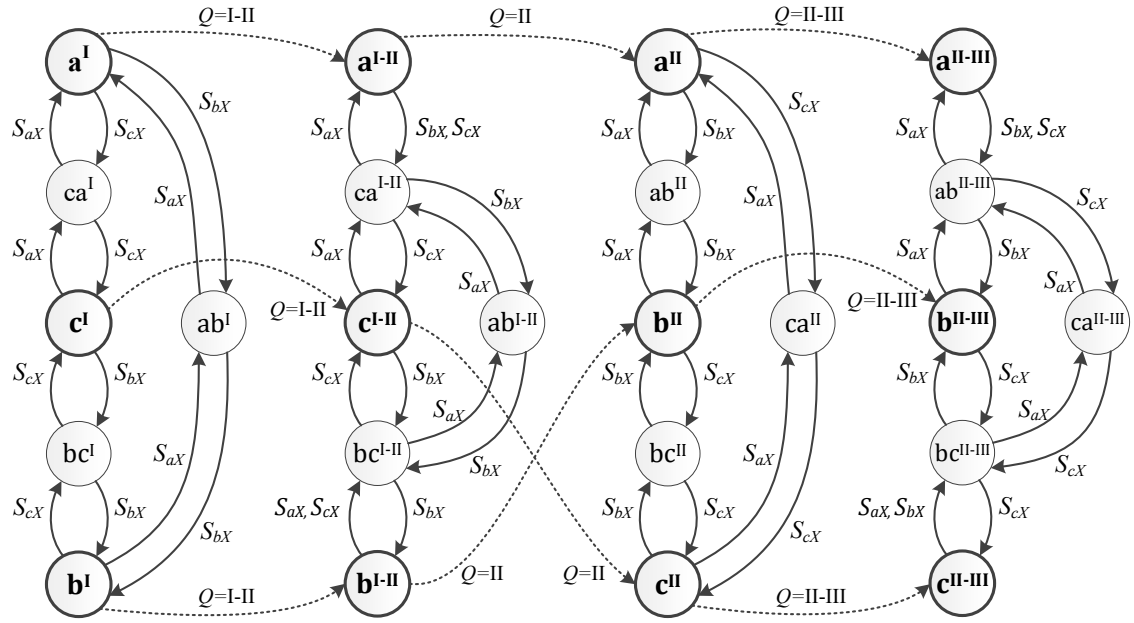


Figure 6.13: Switching state machine diagram for commutation in normal (I, II) and critical (I-II, II-III) intervals.

show the paths for switching state transitions between the intervals. This switching state machine can be extended to the whole input-voltage fundamental cycle. The complete switching state machine of the Variable-step VBC strategy was codified in VHDL code and programmed in the MachXO2 FPGA. The source code is reproduced in Appendix C.

To validate the command signals generation by the FPGA, a simulation was done in the Lattice Diamond software. Fig 6.14 shows the signals for one period of modulation (50 μs) in sector 1 for δ=0.5, d_1=0.4 and d_2=0.2. As can be seen, the pulses are correctly generated and have the specified width and phase-shift.

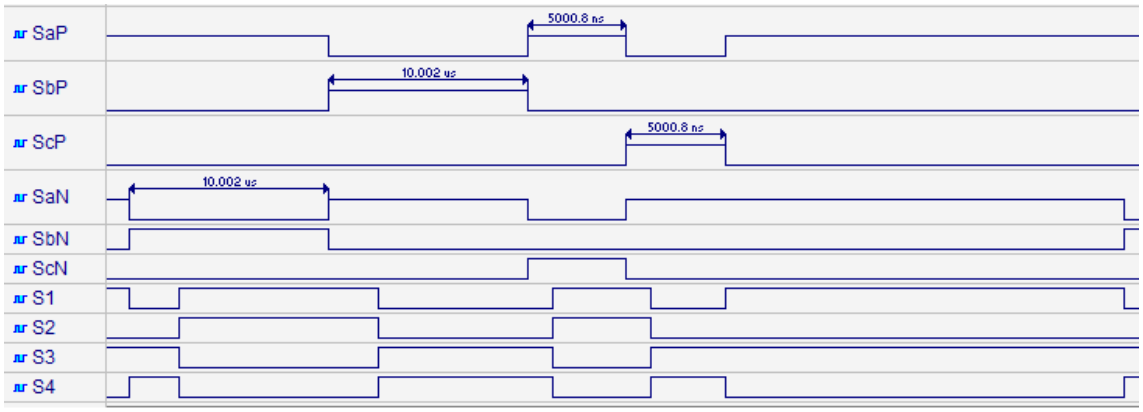


Figure 6.14: Simulated command signals generated by the FPGA for sector 1 and δ=0.5.

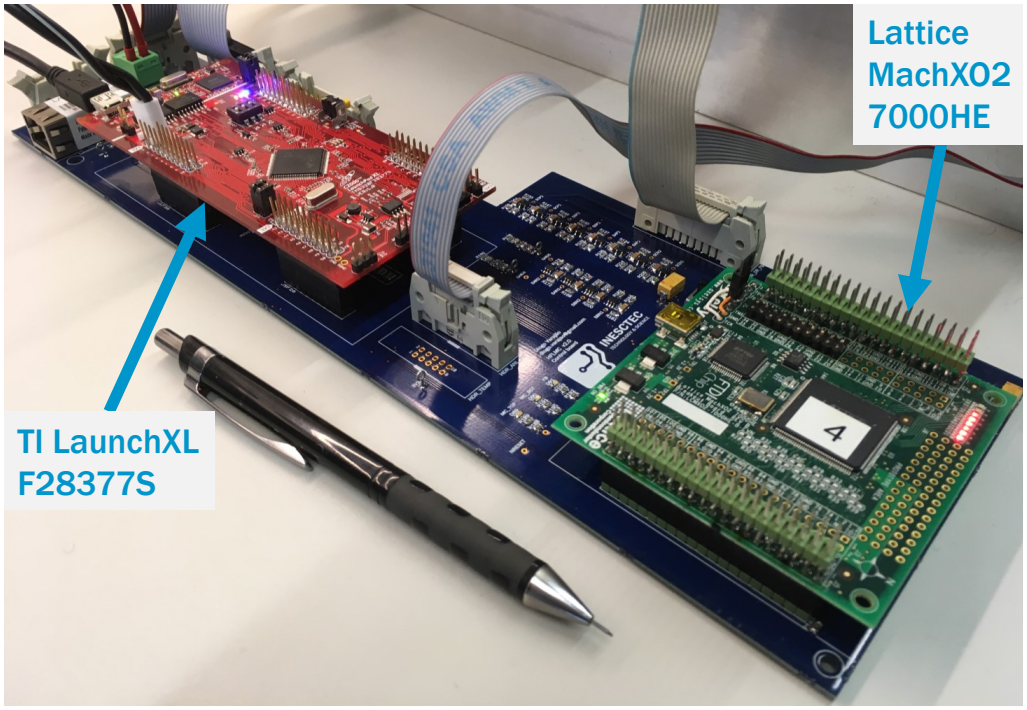


Figure 6.15: Photo of the control system based on DSP plus FPGA.

Figure 6.15 shows a photo of the PCB with the control system based on DSP plus FPGA. This is the same board presented before in Figure 6.6 with the zoom around the circuits for signal conditioning. A data bus in the middle of the PCB connects both control cards. Using digital probes it is possible to measure all the 16 command signals generated by the FPGA as represented in Figure 6.16. The similarity with the previous results presented in Figure 4.4 and Figure 6.14 is evident. As can be noticed, there are small differences in the width of the pulses of the same bidirectional switch. This appears due to the time step introduced by the commutation strategy.

6.2.3 Gate driver

In order to drive the SiC MOSFETs it is necessary to provide an appropriate command signal between the gate and source of the transistor. The 3x2 MC is composed by six bidirectional switches. In turn, each bidirectional switch is formed by two transistors in anti-series connected by the sources terminals. This approach has the advantage that only one isolated voltage source is required to drive each bidirectional switch. Isolation between the control system and the transistor is mandatory for the HFLMC. Typically, the gate drivers available in the market use optical isolation or galvanic isolation. Regarding protection features, short-circuit detection and feedback is important to ensure robustness of the power converter against external faults.

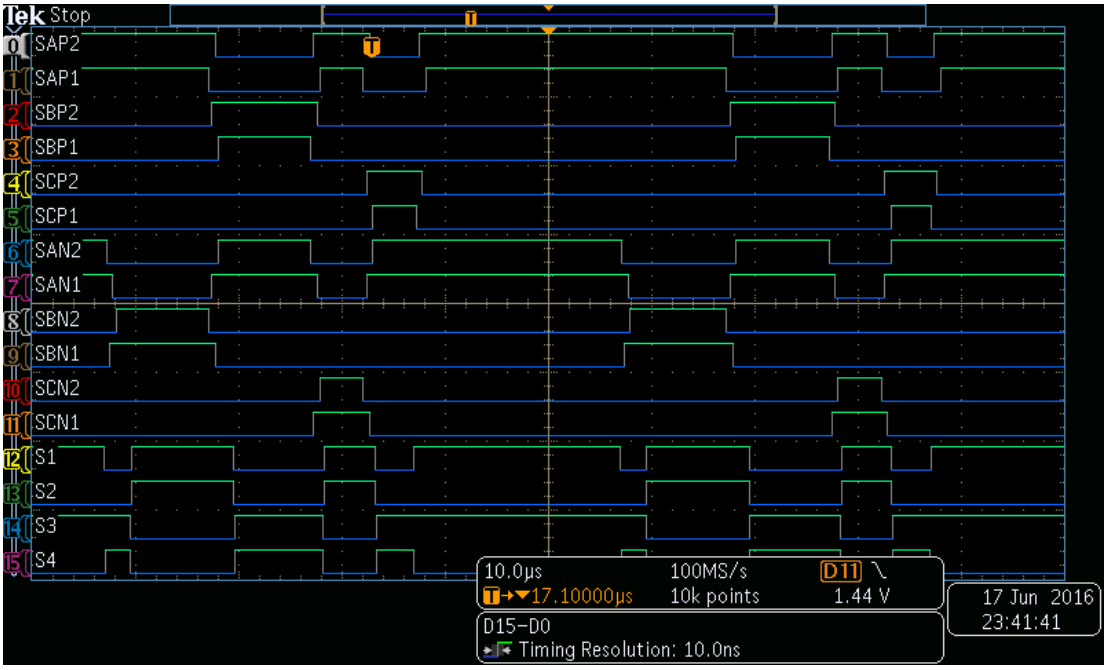


Figure 6.16: Command signals generated by the FPGA for sector 1 and δ=0.5.

For this application, the driver ACPL-337J-000E from Avago that features fast propagation delay, 4.0 A maximum peak output current, Miller Clamp circuit, under voltage lockout (UVLO) protection, and desaturation detection for short-circuit protection with feedback was selected. Figure 6.17 shows the implemented gate drive circuit based on ACPL-337J. In the low-voltage side (primary side) of the integrated circuit there is an optocoupler circuit to provide isolation. In the secondary side there are two main circuits: 1) measurement of the drain to source voltage, v_{DS}, for short-circuit protection; 2) application of gate signal to command the SiC MOSFET.

The short-circuit protection monitors the voltage at pin 14 (DESAT) of the driver. There is a constant current of 1 mA flowing through *R21*, *D5*, and the MOSFET. If the total voltage drop surpasses 7 V, the short-circuit protection is activated and the gate signal is inhibited. A blanking time can be adjusted by capacitor *C26* to keep the protection disabled for a short time period following the turn-on of the MOSFET. Additionally, a Schottky diode *D8* is connected across pin 14 and the source to avoid detection of false fault signals, that can happen if the reverse recovery spikes coming from the MOSFET freewheeling diodes, brings the DESAT pin below ground.

The turn-on of one transistor can induce a Miller current to circulate in other transistor due to the path created through the Miller capacitance, C_{GD}. This current can be calculated by the following formula:

$$I_{gd} = C_{gd} \times \frac{dv}{dt}. \tag{6.1}$$

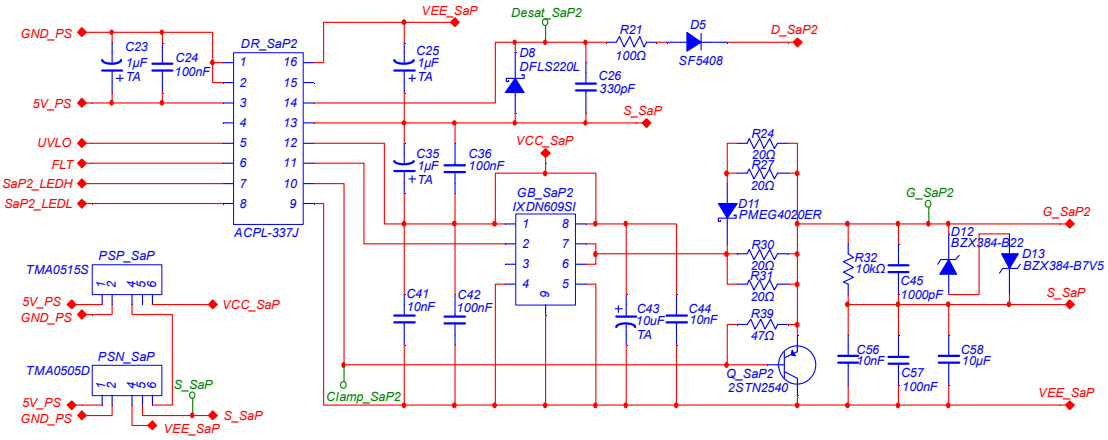


Figure 6.17: Gate driver circuit for SiC MOSFETs based on ACPL-337J.

With the increase of the switching speed high dv/dt appears which leave current I_{gd} to generate oscillations in the gate voltage, V_{gs}. If the threshold voltage is surpassed the transistor starts conducting current. This can originate a short-circuit in conjunction with other transistors that are already turned-on. In order to continue operating the converter at high speed, a Miller clamp circuit must be implemented to bypass the induced current. Despite the ACPL having an internal Miller clamp feature, the internal MOSFET has a resistance between 1.1 Ω and 3.5 Ω which may not be sufficient to avoid the untimely turn-on of the transistor. Therefore, a PNP transistor Q_S_{aP2} is connected between the gate and the negative voltage (VEE) to perform the current bypass. This transistor is activated when the MOSFET has been commanded to be turned-off. In this way, the gate voltage is clamped below the transistor threshold voltage. This protection is particularly important in the case of the MC due to the association in anti-series of two MOSFETs to form a bidirectional switch. An additional 1 nF ceramic capacitor ($C45$) is added between gate and the source terminals to shunt the miller current and reduce the ringing on the gate.

A bipolar gate voltage of +20 V/-5 V is supplied by isolated DC/DC converters from Traco Power. In this case, the TMA-0515S is connected in series with the TMA-0505D. The negative voltage is also useful to keep the MOSFET in off state since it increases the difference to the threshold voltage. Regarding the C2M0025120D, the minimum threshold voltage is 1.8 V.

The ACPL-337J can provide a maximum peak output current of 4 A. Depending of the gate resistances, this current can limit the turn-on and turn-off speed. Therefore, the IXDN609SI current buffer was added to the circuit in order to provide up to 9 A peak source/sink current. This IC has low propagation delay and less than 25 ns rise and fall times.

Typically, the turn-off of a MOSFET takes longer time than the turn-on. In this case, different resistance values were employed: 10 Ω for the turn-on and 5 Ω for the turn-off.

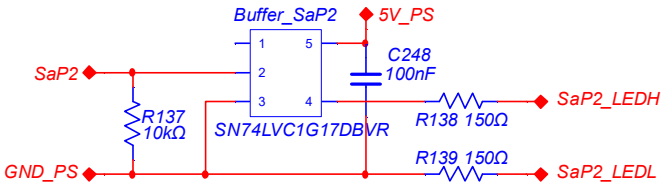


Figure 6.18: LED driver implemented in the control system PCB to increase the noise immunity.

This is accomplished by inserting the PMEG4020ER Schottky Diode (*D11*) in the return path to put resistances *R24* and *R27* in parallel with *R30* and *R31*.

To protect the gate of the MOSFET against both positive and negative voltage peaks, the BZX384-B22 (*D12*) and the BZX384-B7V5 (*D13*) were added between the gate and the source terminals. A gate shunt resistor of 10 kΩ (*R32*) is also connected across the gate and the source in order to decrease the impedance and make the pull-down.

Three de-coupling ceramic capacitors with values of 10 nF, 100 nF, and 10 uF (*C56*, *C57*, *C58*) are placed close to the SiC MOSFET to reduce the high frequency switching loop and bypass noise within this loop. The 74270012 ferrite bead was also placed on the gate pin of the TO-247 to introduce high impedance on the gate path for high frequencies in the MHz range and reduce the V_{gs} ringing.

The ACPL-337J has a direct LED input that allows flexible logic configuration and differential current mode driving with low input impedance. The command signals that come from the control system PCB (Figure 6.15) are the inputs of the LED at pins 7 and 8 of the ACPL-337J. In order to increase the noise immunity, a LED driver is implemented in the control system PCB as represented in Figure 6.18. The Schmitt-trigger buffer can provide up to 24 mA source/sink current, which is sufficient to drive the LED. Both *SaP2_LEDH* and *SaP2_LEDL* signals are then carried to the MC PCB through a flat-cable.

Finally, a photo of the gate driver circuits for the S_{cP1} and S_{cP2} SiC MOSFETs implemented in the MC PCB is shown in Figure 6.19. As can be seen, a layout with high component density was achieved making the MC PCB very compact.

6.2.4 SiC MOSFETs and the bidirectional switches

Despite the modulation frequency being 20 kHz, the transistors switch four or five times for each period of the modulation. Therefore, the effective switching frequency of the transistors is 80 kHz or 100 kHz. As discussed previously, the SiC devices are more suitable to operate at these frequencies than other technologies. The SiC MOSFET of type C2M0025120D [258] with a typically on-resistance of $R_{DS(ON)}$=25m Ω was selected for the MC and the FB. This transistor has a Drain-Source breakdown voltage V_{DS}=1200 V and can conduct currents up to $I_{D(25°C)}$=90 A. The LA-9-150 heat-sink from Fischer Elektronik was selected for this application. The four transistors of the FB were mounted

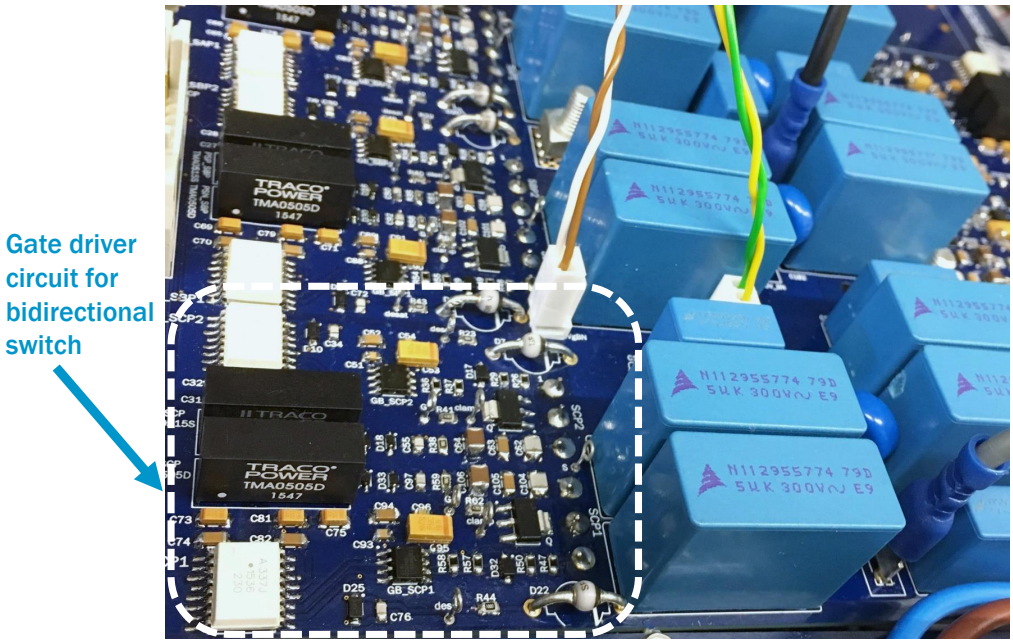


Figure 6.19: Photo of the gate driver circuits for the S_{cP1} and S_{cP2} SiC MOSFETs.

in one heat-sink. The other 12 MOSFETs of the MC were mounted in another heatsink as depicted in Figure 6.20. One of the MOSFET that forms the bidirectional switch is mounted at the top of the heat-sink and the other is on the side. This disposition allows to put both transistors aligned side-by-side in order to reduce the distance between the sources and consequently minimize the parasitic inductance between the sources. The MOSFETs are electrically isolated from the heat-sink by the 4180G thermal interface pad developed by Aavid Thermalloy.

If for some reason there happens a fault during the commutation of the bidirectional switches, dangerous overvoltages can appear at the terminals of the MC. To protect the SiC MOSFETs, S10K625 varistors were added to the input and output of the MC.

6.2.5 EMI Filter and AC supply

The two-stage EMI filter presented in Section 5 for CISPR 11 Class B pre-compliance was integrated in the prototype. The first validation tests were performed with reduced input voltage. The connection to the grid was made through an autotransformer to adjust the voltage to 100 $V_{l-l,rms}$.

6.2.6 Power Transformer and Link-inductor

The link-inductor projected in Appendix E was connect between the MC and the FB. The power transformer is only necessary to provide galvanic isolation since the turns ratio is unitary. For this reason, these validation tests were performed without the power

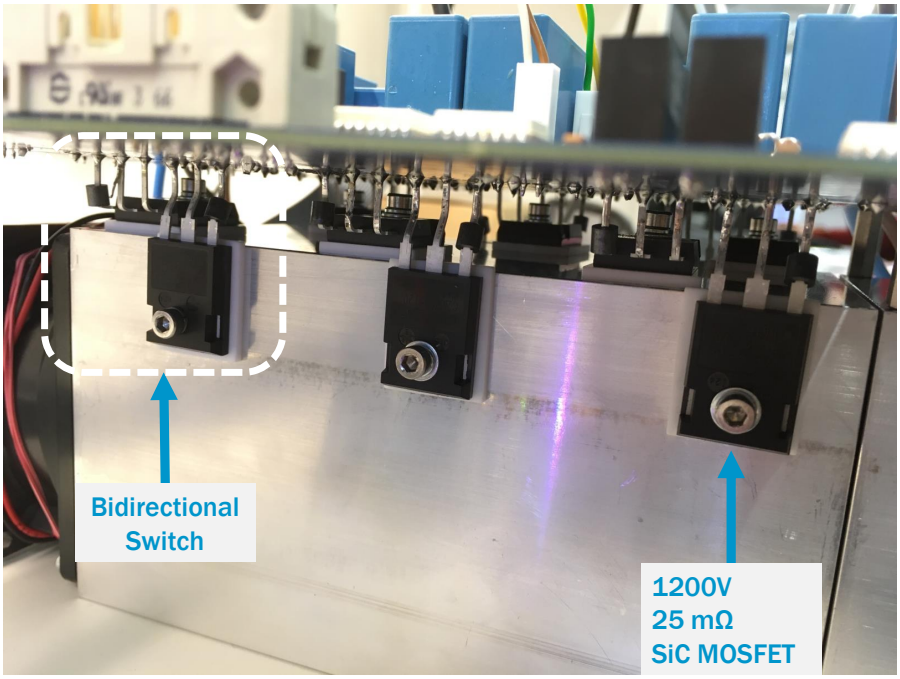


Figure 6.20: Photo of the mounting of the SiC MOSFETs to form the matrix converter.

transformer. For safety reasons, a conventional low frequency transformer was connected in series to the autotransformer that is connected to the grid.

6.2.7 DC Filter

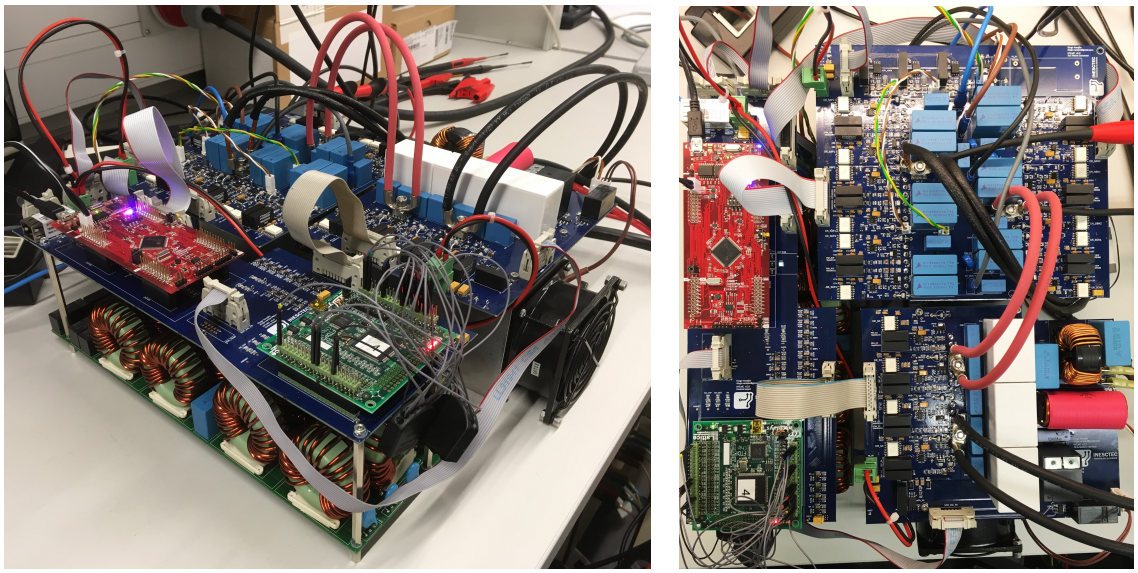
The output current from the FB has significant ripple components due to the high-frequency link operation. In order to attenuate the ripple components, a DC filter can be implemented by 90 μF capacitance and 60 μH inductance. The filter was constructed with three C4AEHBW5300A3JJ capacitors from Kemet and the IHV28BZ60 inductor from Vishay. The project of the DC filter is detailed in Appendix F.

6.2.8 Battery and DC supply

For safety reasons and to ensure a constant DC supply, the open-loop tests were performed using the EA-PSI-9750-60 power supply plus the EA-ELR-9750-66 electronic load. Using this strategy, it was possible to test the converter with the certainty that the battery did not influence the tests. The battery voltage and current controllers were then tested with a battery pack of 2.3 kWh capacity and 192 V nominal voltage. This pack is composed by 16 cells of UL12-12 connected in series.

6.2.9 Complete assembly of the prototype

All the parts described above were assembled altogether to form the functional prototype. Figure 6.21 shows two photos with different perspectives of the prototype.



(a) (b)

Figure 6.21: Photos of the complete assembly of the prototype. (a) Side view. (b) Top view.

The complete assembly of the functional prototype has the following dimensions: 305 x 350 x 140 mm, corresponding to a boxed volume of 14.95 dm^3. The total weight of the prototype is 11.89 kg. Considering a rated power of 10 kW, the power density of this functional prototype is 669 W/dm^3 while the specific power is 841 W/kg. It is important to stress that this prototype was merely utilized to validate the technology. A full enclosure design has not yet been designed and optimized but it is expected that a significant increase in the power density and reduction in weight would be achieved.

6.3 Experimental Results

The prototype described above was integrated in the testbench shown in Appendix I. Several experimental tests were performed to validate the different control layers: the commutation of the bidirectional switches and the high-frequency link operation; measurement of the grid current harmonics; then the grid currents controller; finally the battery voltage and current controllers and the PQ controller.

6.3.1 Commutation of the bidirectional switches

The proper commutation of the bidirectional switches is crucial for the HFLMC operation. An overview of S_{aP2} commutation over two grid cycles is depicted in Figure 6.22. v_{ds} exhibits an envelope that appears due to the evolution of the line-to-line voltages within

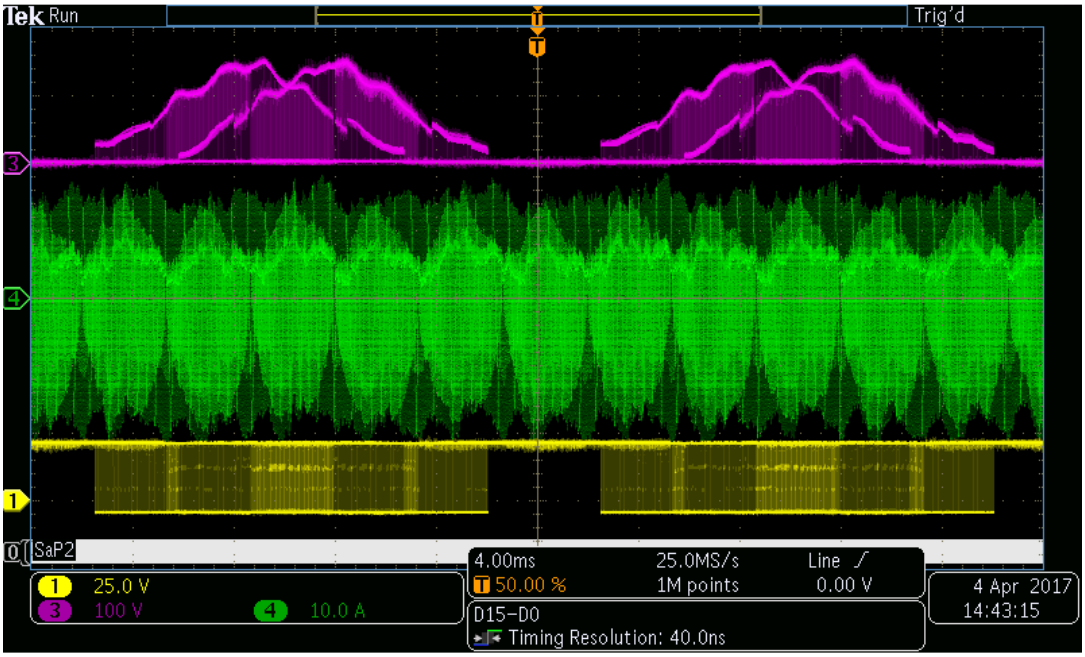
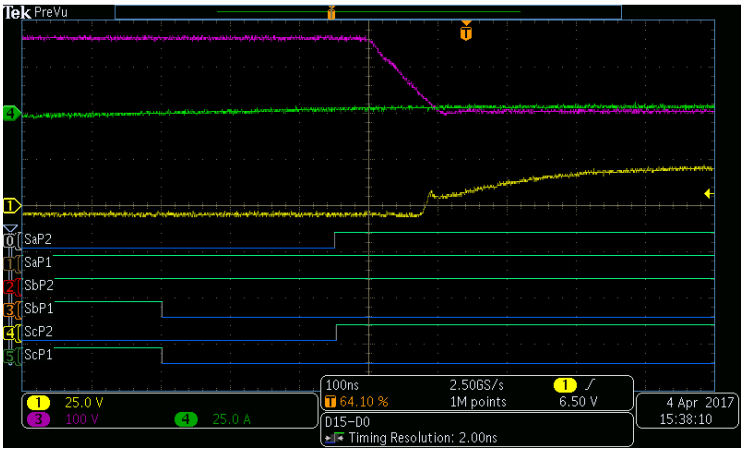


Figure 6.22: Overview of S_{aP2} commutation over two grid cycles: gate voltage v_{gs} [CH1], drain voltage v_{ds} [CH3], current i_L [CH4], and command signal from FPGA [D0].

the sectors. As a consequence, the switching losses in each MOSFET change within the grid cycle. As was previously discussed, each transistors is kept in *ON* mode by the VBC strategy during one sector. This is also clear from the waveform of v_{gs}. By avoiding these unnecessary commutations, the switching losses are reduced. As can be seen, the waveform of current i_L is repeated in each sector. Moreover, a low frequency variation in the amplitude of i_L is also evidenced within the sector. This is due to the single-stage operation of the converter and nature of the proposed modulation.

The detailed analysis of the commutation of BS S_{aP}, S_{bP}, and S_{cP} is represented in Figure 6.23. The command signals for the P bar of the MC, along with the v_{gs}, and v_{ds} of S_{aP2} are also depicted. The VBC strategy ensures a path for the current by keeping some of the transistors in *ON* mode. As can be seen in Figure 6.23(a), for this sector 3 the S_{aP1} and S_{bP2} are permanently *ON*. It is intended to do a commutation from S_{bP} to S_{aP}. Initially, the BS S_{bP} is conducting the current i_L since both transistors S_{bP1} and S_{bP2} are *ON*. Additionally, S_{cP1} has also a command signal to be turned-on. Then, S_{bP1} and S_{cP1} are turned-off. Since i_L is negative and $V_b > V_a$, the current continues flowing through S_{bP2} and D_{bP1}, the body diode of S_{bP1}. When the current i_L inverts its direction, the commutation to S_{aP} is initiated. Firstly, the current flows through S_{aP1} and D_{aP2}, the body diode of S_{aP2}. When the command signal of S_{aP2} changes to *ON* mode, the transistor starts conducting with zero voltage. The ZVS occurs because the output capacitance of the MOSFET, C_{oss}, is discharged. Thus, this commutation occurs with zero switching losses which increases the conversion efficiency.



(a)

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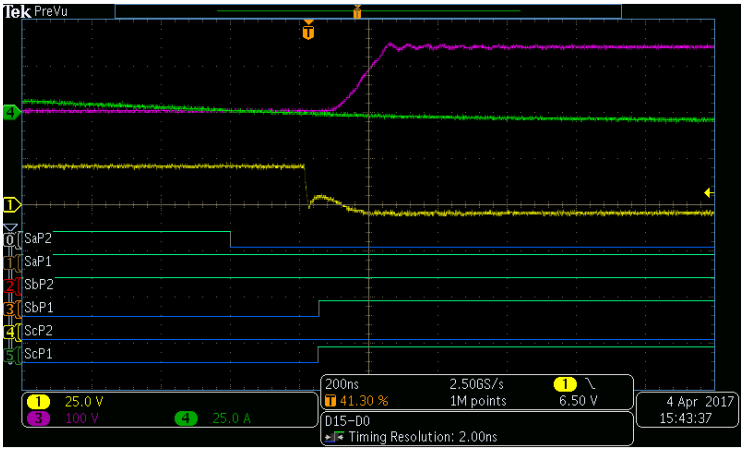


(c)

Figure 6.23: Commutation of bidirectional switches S_{aP}, S_{bP}, and S_{cP}: gate voltage v_{gs} [CH1], drain voltage v_{ds} [CH3], current i_L [CH4], and command signals for the P bar of MC [D0-D5]. (a) Turn-on of S_{aP2} under ZVS. (b) Turn-on of S_{aP2} under HS. (c) Turn-off of S_{aP2} under HS.

Figure 6.23(b) shows the commutation from S_{cP} to S_{aP} in the critical interval from sector 4 to sector 5. The switching sequence is similar to the one previously presented.

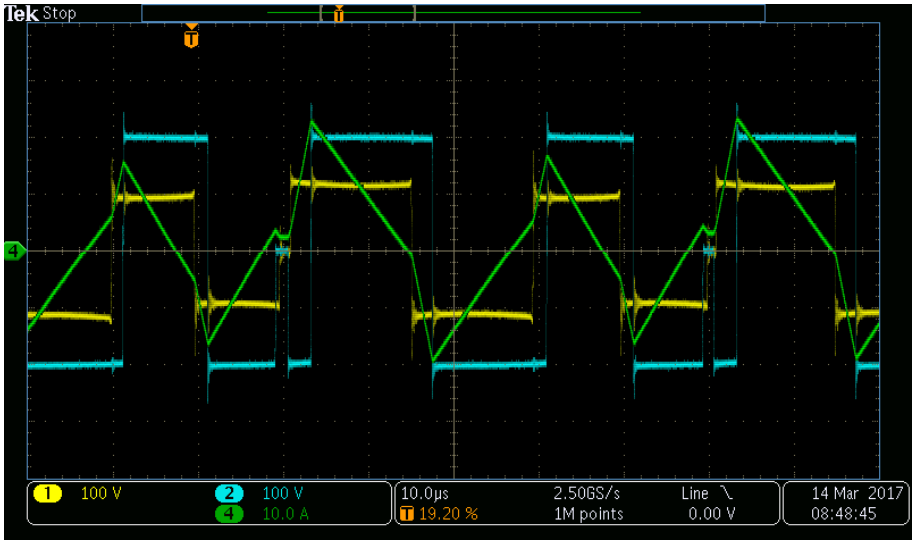
Initially, the BS S_{cP} is conducting the current i_L since both transistors S_{cP1} and S_{cP2} are *ON*. Additionally, S_{bP1} has also a command signal to be turned-on. S_{bP2} is kept turned-off since this is a critical interval. Then, S_{cP1} and S_{bP1} are turned-off. Since i_L is negative and $V_c > V_a$, the current continues flowing through S_{cP2} and D_{cP1}, the body diode of S_{cP1}. When the command signal of S_{aP2} changes to *ON* mode, the transistor starts conducting current with non-zero voltage. v_{ds} only starts decreasing when i_L is completely flowing through S_{aP2}. This hard switching occurs because i_L does not invert its direction before the change in the command signal of S_{aP2}. Thus, not all commutations occur under ZVS. The soft-switching conditions will vary inside the modulation period and during the grid voltage cycle. As explained in Section 3.4, only half of the commutations of the MC occur with soft-switching when operating with 4-step strategy.

Figure 6.23(c) illustrate the commutation from S_{aP} to S_{bP} in the critical interval from sector 2 to sector 3. Initially, the BS S_{aP} is conducting the current i_L since both transistors S_{aP1} and S_{aP2} are *ON*. Additionally, S_{bP2} has also a command signal to be turned-on. S_{cP2} is kept turned-off since this is a critical interval. When the current i_L inverts its direction, the commutation to S_{bP} is initiated. Firstly, the current flows through S_{bP2} and D_{bP1}, the body diode of S_{bP1}. When the command signal of S_{aP2} changes to *OFF* mode, the transistor is already not conducting current and it is with zero voltage. Therefore, this commutation occurs with zero switching losses. Similarly, S_{bP1} is also turned-on under ZVS because its body diode is already conducting.

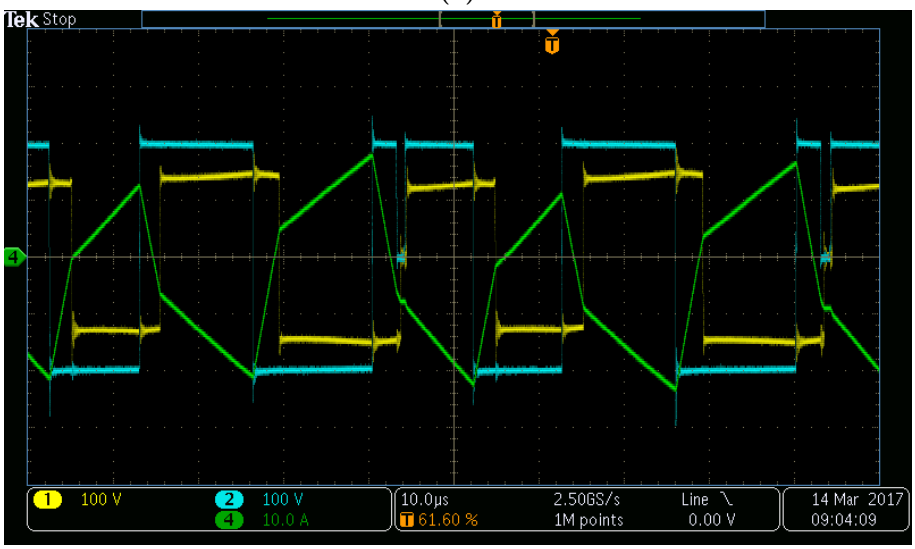
6.3.2 High-frequency link operation

The operation of the HFL in charger mode and inverter mode over two periods of the modulation is illustrated in Figure 6.24. These results are in agreement with the description illustrated in Figure 4.4 and the simulation results presented in Figure 4.14. The MC and the FB impress v_p and v_s according to the modulation principle. The current in the link inductor then evolves according the magnitude and phase-shift between these voltages. In charger mode, i_L has predominantly the same signal of v_p and v_s. This results on a power flow from the grid to the battery since i_g has the same direction of v_g. The opposite occurs in inverter mode, as i_L has predominantly the inverse signal of v_p and v_s. During the application of the zero SSV, i_L is kept constant until the end of the modulation period.

Figure 6.25 represents two cycles of the grid current in charger mode along with the HFL operation. The grid voltage at the input of the converter exhibits some distortion. This appears due to additional impedance, introduced by the autotransformer plus the LF transformer, in series with the EMI filter. In charger mode, the voltage at the input of the converter decreases in order to impose this transit of power. On other way, the HFLMC supports the input voltage during inverter mode operation. As can be seen, i_{ga} is almost purely sinusoidal and in phase with v_{ga}. It is interesting to see the envelop that



(a)



(b)

Figure 6.24: HFL operation: voltage v_p [CH1], voltage v_s [CH2], current i_L [CH4]. (a) Charger mode with $\delta = 0.4$. (b) Inverter mode with $\delta = -0.4$.

appears at v_p due to the single-stage operation. This is consistent with the simulation results presented before in Figure 4.14.

6.3.3 Harmonics of the grid current

The three grid currents as well as the battery current in charger mode are depicted in Figure 6.26. It is clear that the grid currents are perfectly symmetric and have low distortion. Moreover, the battery current is constant and features low ripple. This is crucial to ensure that additional losses are not produced in the battery pack.

The low-frequency harmonics of the grid current were measured in the laboratory using the PA1000 Power Analyzer from Tektronix. This experiment was performed by

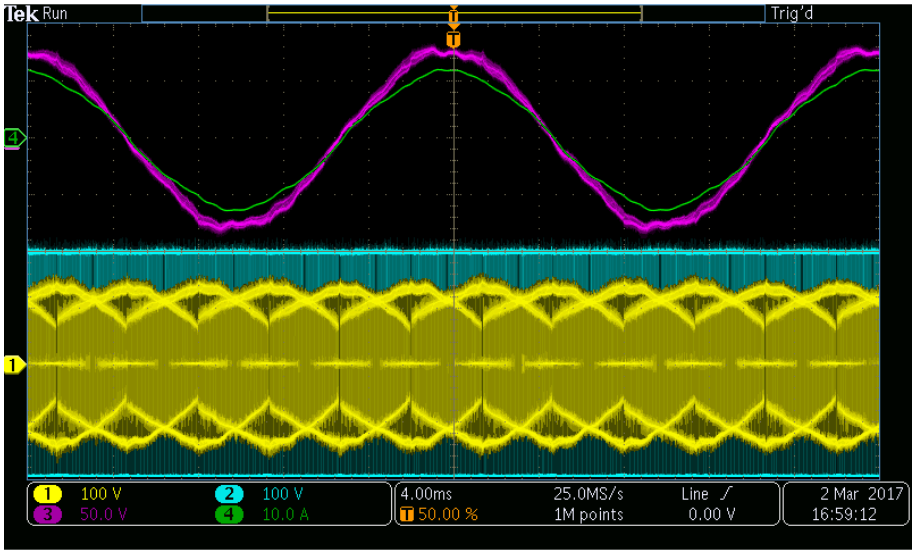


Figure 6.25: Grid current modulation and the HFL operation in charger mode: voltage v_p [CH1], voltage v_s [CH2], grid voltage v_{ga} [CH3], and grid current i_{ga} [CH4].

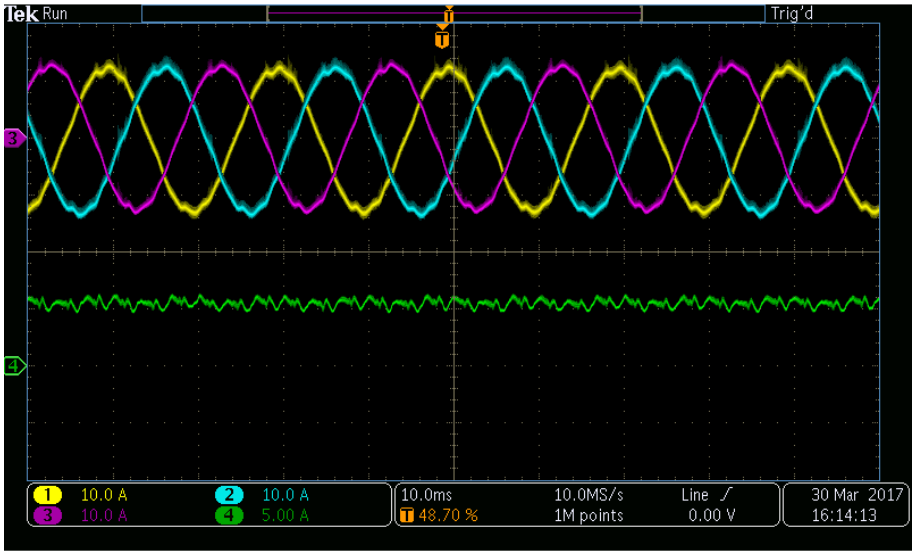


Figure 6.26: Experimental results of the HFLMC operation in charger mode: grid currents ($i_{ga,b,c}$) [CH1,CH2,CH3] and battery current (i_{dc}) [CH4].

measuring i_{ga}, but considering Figure 6.26 the results should be identical for the other phase currents. Figure 6.27 shows the low-frequency harmonics of the grid current and the THD measurement according the IEC 61000-3-2 standard for charger and inverter mode. The Partial Odd Harmonic Current (POHC) was measured as 27.6 mA for charger mode and 21.2 mA for inverter mode which means that the high-order harmonics from the 21^{st} to the 39^{th} are almost negligible. From this figure, the 5^{th} harmonic is the most significant. However, all the harmonics are within the limits specified by the standard with a THD of

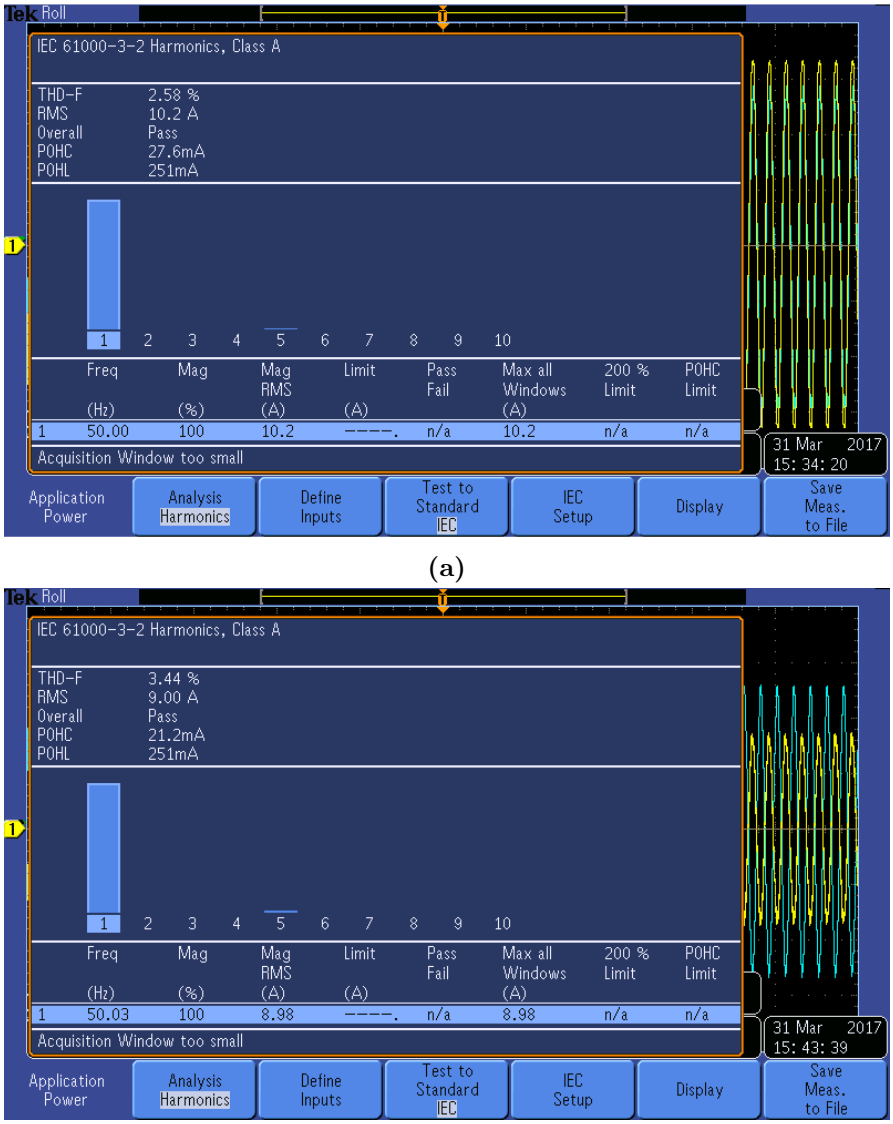
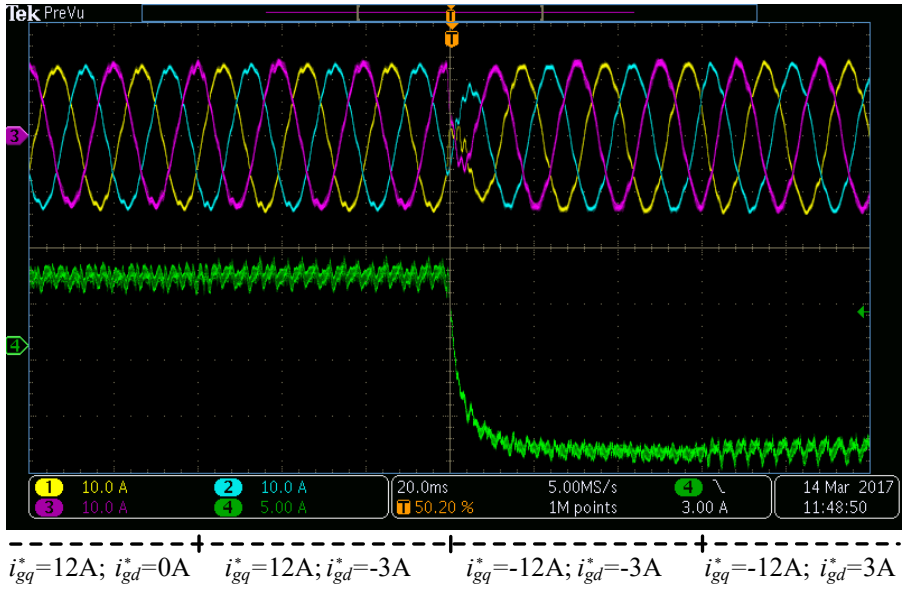


Figure 6.27: Low-frequency harmonics of the grid current and THD measurement according the IEC 61000-3-2 standard. (a) Charger mode. (b) Inverter mode.

2.58 % at 10.2 Arms for charger mode and 3.44 % at 9.0 Arms for inverter mode. It can be concluded that the proposed modulation together with the EMI filter can ensure that the grid currents are in compliance with the IEC 61000-3-2 standard.

6.3.4 Grid currents controller

The grid currents controller gives the main command variables for the modulation: the phase-shift ϕ and the displacement angle φ_i. By adjusting these variables, it is possible to control the magnitude and phase of the modulated grid currents. As described in Section 4.3, the currents are controlled in the synchronous reference frame. Both PI controllers of Figure 4.7 were tuned with gains K_{p,i_g}=0.050 and K_{i,i_g}=2500. The operation



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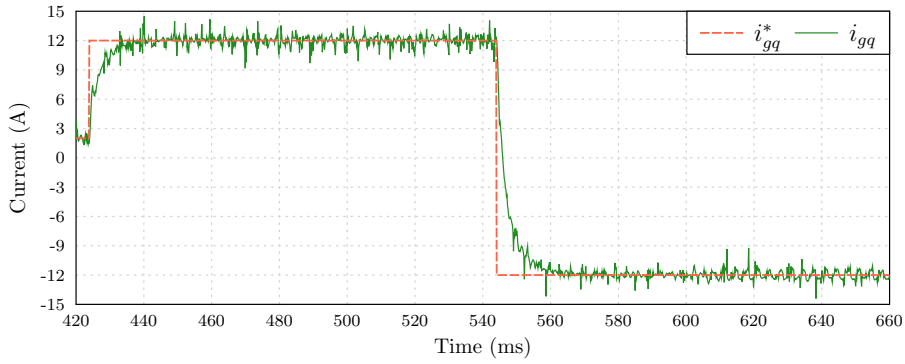

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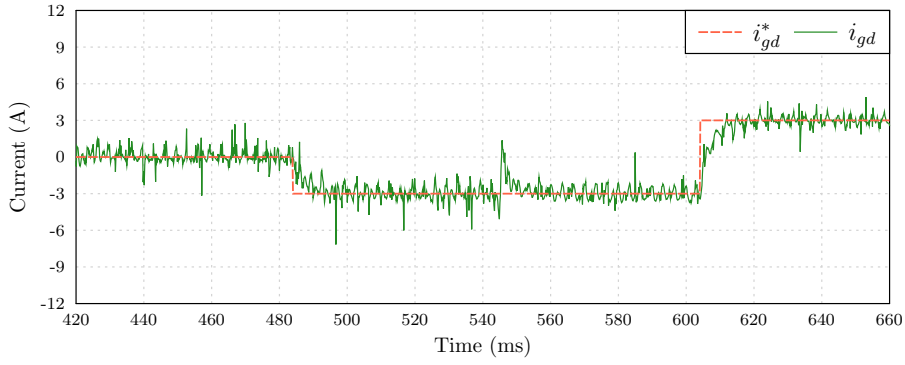

(c)

Figure 6.28: Experimental results of the HFLMC operation in the 4Q. (a) Grid currents ($i_{ga,b,c}$) [CH1,CH2,CH3] and battery current (i_{dc}) [CH4]. (b) q reference (i^*_{gq}) and actual q grid current (i_{gq}). (c) d reference (i^*_{gd}) and actual d grid current (i_{gd}).

in the 4Q was verified by performing a test where i^*_{gq} and i^*_{gd} are cyclically changed. As can be seen in Figure 6.28, the grid currents are perfectly controlled and decoupled. When i_{gq}

changes from 12 A to -12 A, a perturbation appears at i_{gd} but it is quickly compensated by the controller. The step response has a rise time lower than 10ms and a settling time under two cycles of the grid voltage. Due to the impedance of the autotransformer, the magnitude of V_i changes depending on the power flow direction. Considering (4.19), that explains the difference in the magnitude of i_{dc} noticeable in Figure 6.28(a). As expected by the mathematical analysis and the simulation results, the waveform of i_{dc} has the same shape of i_{gq}.

6.3.5 Battery voltage and current controllers

By changing the currents i_{gq} and i_{gd} at the grid interface, it is possible to regulate the voltage and the current in the battery pack. The controller proposed in Figure 4.12 was added to the control loop implemented in the DSP. The gains of the PI controller for i_{dc} are $K_{p,i_{dc}}$=0.5 and $K_{i,i_{dc}}$=200. Regarding the PI controller for PF the gains are set as $K_{p,PF}$=10 and $K_{i,PF}$=300.

The capability to regulate the current at the battery pack was verified by doing a test where i^*_{dc} is cyclically changed. Figure 6.29 shows the experimental results where it is clear the effectiveness of the controller to adjust i_{dc}. The amplitude of the grid currents

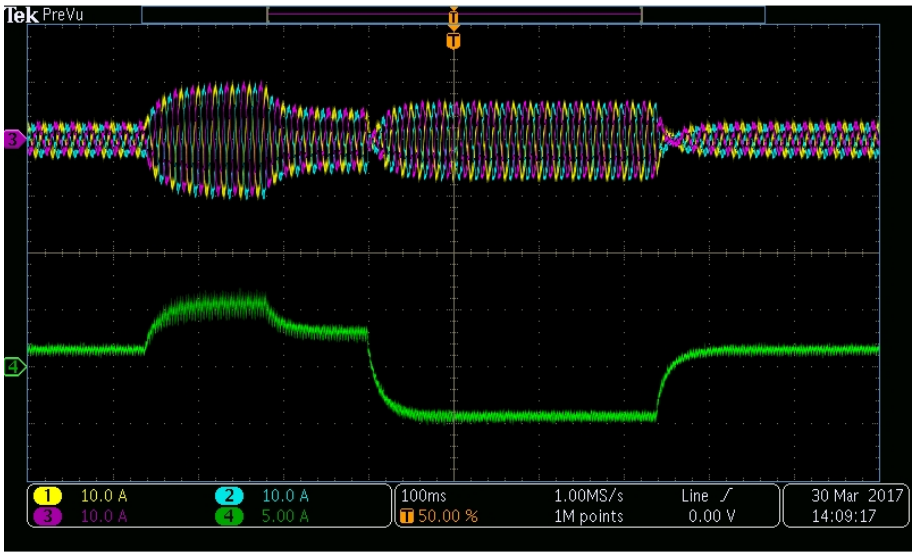

Figure 6.29: Experimental results of the HFLMC operating with the Idc and PF controllers: Grid currents ($i_{ga,b,c}$) [CH1,CH2,CH3] and battery current (i_{dc}) [CH4].

changes according to the power that is being exchanged with the battery. The transition from charger to inverter mode occurs smoothly as can be seen when i_{dc} becomes negative. At this instant, the phase of the grid currents steps by 180° due to the power flow inversion. Figure 6.30 gathers the main signals from the controller during this experiment. As can be seen, i_{dc} follows the reference with a rise time around 40ms and a settling time under four cycles of the grid voltage. This controller modifies the reference i^*_{gq} that in turn feeds

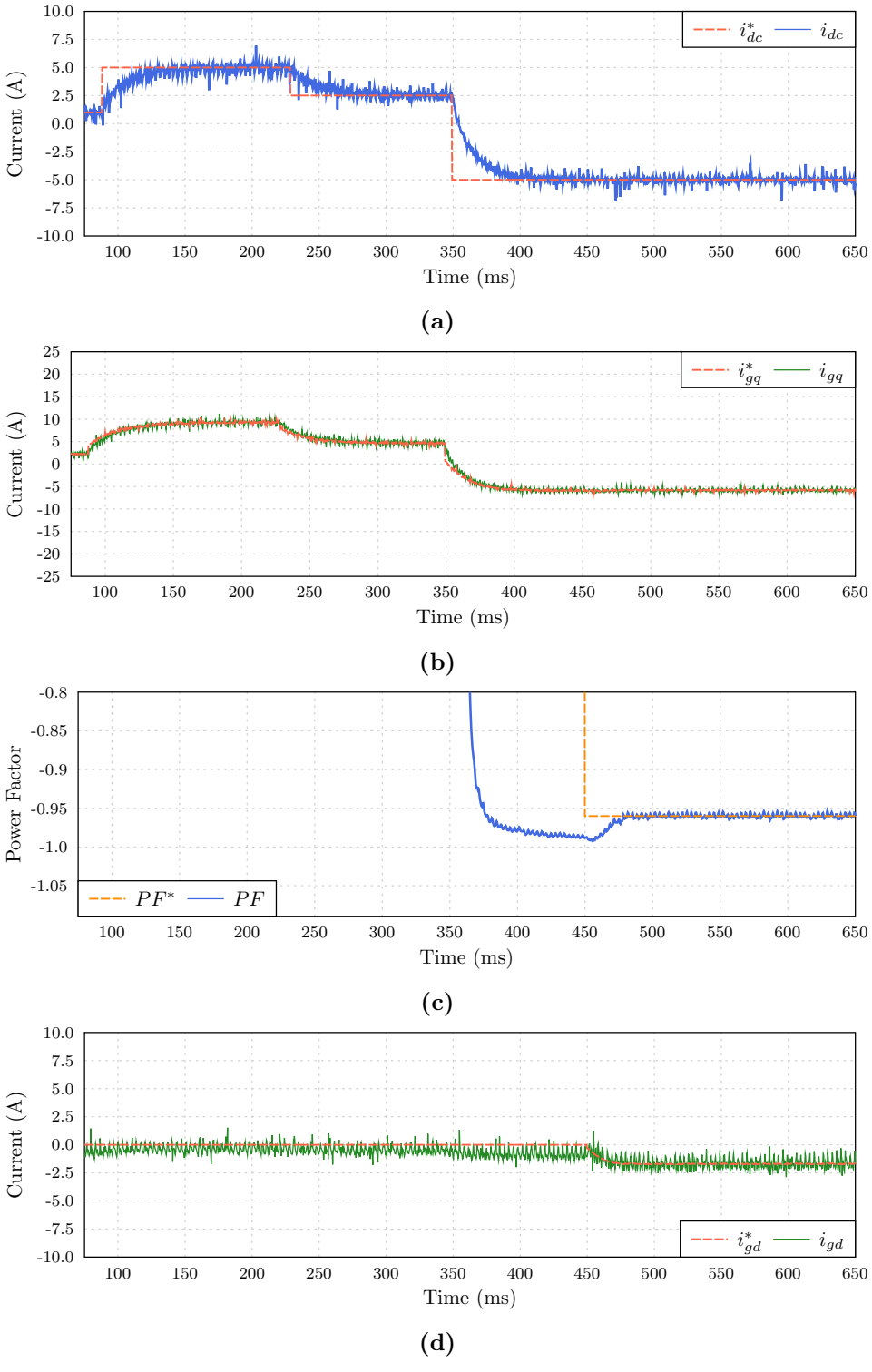

Figure 6.30: Experimental results with the Idc and PF controllers. (a) Battery current (i_{dc}). (b) q grid current (i_{gq}). (c) Power factor and set-point (PF^*). (d) d grid current (i_{gd}).

the grid current controller. As expected, i_{gq} has the same shape of i_{dc}. Regarding the PF, the respective controller is enabled at t=450 ms. The process of adjusting the PF starts

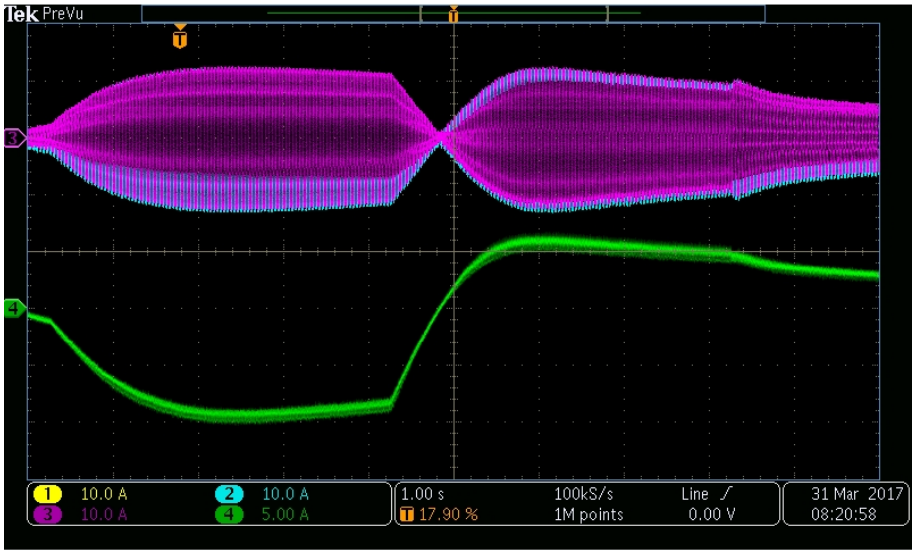

Figure 6.31: Experimental results with the Vdc and PF controllers: Grid currents ($i_{ga,b,c}$) [CH1,CH2,CH3] and battery current (i_{dc}) [CH4].

immediately by setting the reference i^*_{gd}. With this strategy the PF is corrected in less than 30 ms. The battery current is not affected by this change in the PF.

After validating the capability to regulate i_{dc}, the additional control layer for v_{dc} was tested by cyclically changing v^*_{dc}. The PI controller for v_{dc} proposed in Figure 4.12 was implemented in the DSP with gains $K_{p,v_{dc}}$=0.004 and $K_{i,v_{dc}}$=200. These gains are significantly different than the ones used in the simulation because the internal impedance of the battery pack is not just a resistance as modeled in the simulation. Figure 6.31 shows the grid currents and the battery current during the test of the v_{dc} controller. Similarly to the previous test, the amplitude of the grid currents changes according to the power that has been exchanged with the battery. Moreover, it is clear from this experiment that the transition from inverter to charger mode occurs smoothly. The main signals from the controller during this experiment are represented in Figure 6.32. At the first part of the test, v^*_{dc} is set to 180 V. Since the battery voltage is above that level, the converter starts operating in inverter mode by changing the reference i^*_{dc}. As the current increases and the energy is taken from the battery pack, the voltage goes down until achieve the reference. At the second part of the test, v^*_{dc} is set to 200 V. Then, the converter switches to charger mode in order to increase the battery voltage up to the reference. At instant t=28.8 s, the PF controller is enabled and the process to adjust the power factor to 0.96 starts immediately. By changing the reference i^*_{gd}, the PF is corrected in less than 30 ms. As expected, the battery voltage is not affected by this change in the PF.

Additional experiments were done to evaluate the performance of the PF controller. The set-point for the power factor is kept unitary during the test. The Fluke 1760 Three-phase Power Quality Analyzer was used to measure the voltages and currents at the PCC.

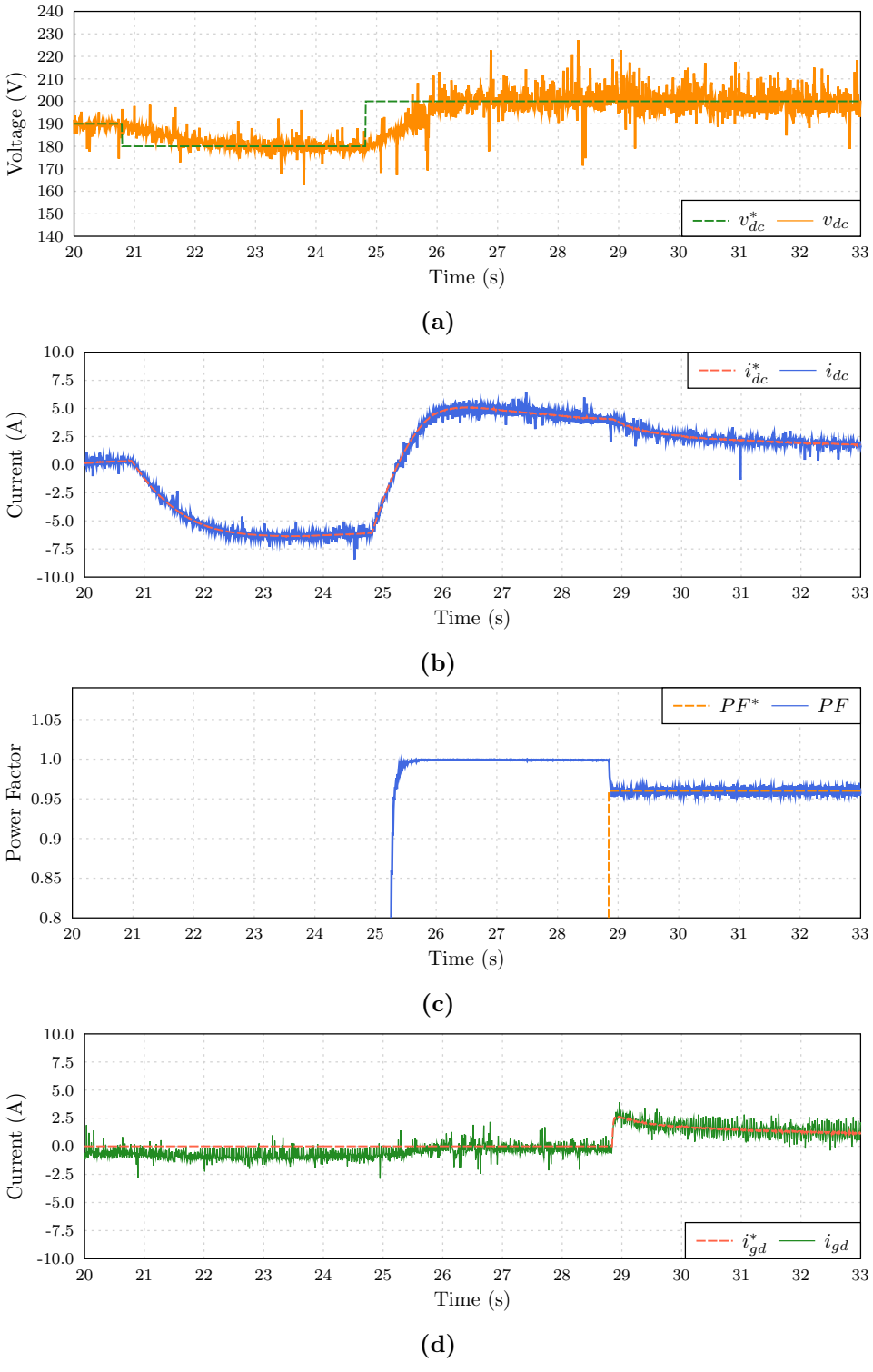

Figure 6.32: Experimental results with the Vdc and PF controllers. (a) Battery voltage and set-point (v^*_{dc}). (b) Battery current (i_{dc}). (c) Power factor and set-point (PF^*). (d) d grid current (i_{gd}).

During this test, the power was varied from 500 VA up to 1.75 kVA. Figure 6.33 shows the measurements of the apparent power in each phase along with the PF. As can be seen,

the PF is kept near unitary for different power levels. This allows to prove the capability of the proposed modulation to effectively control the reactive power at the grid interface.

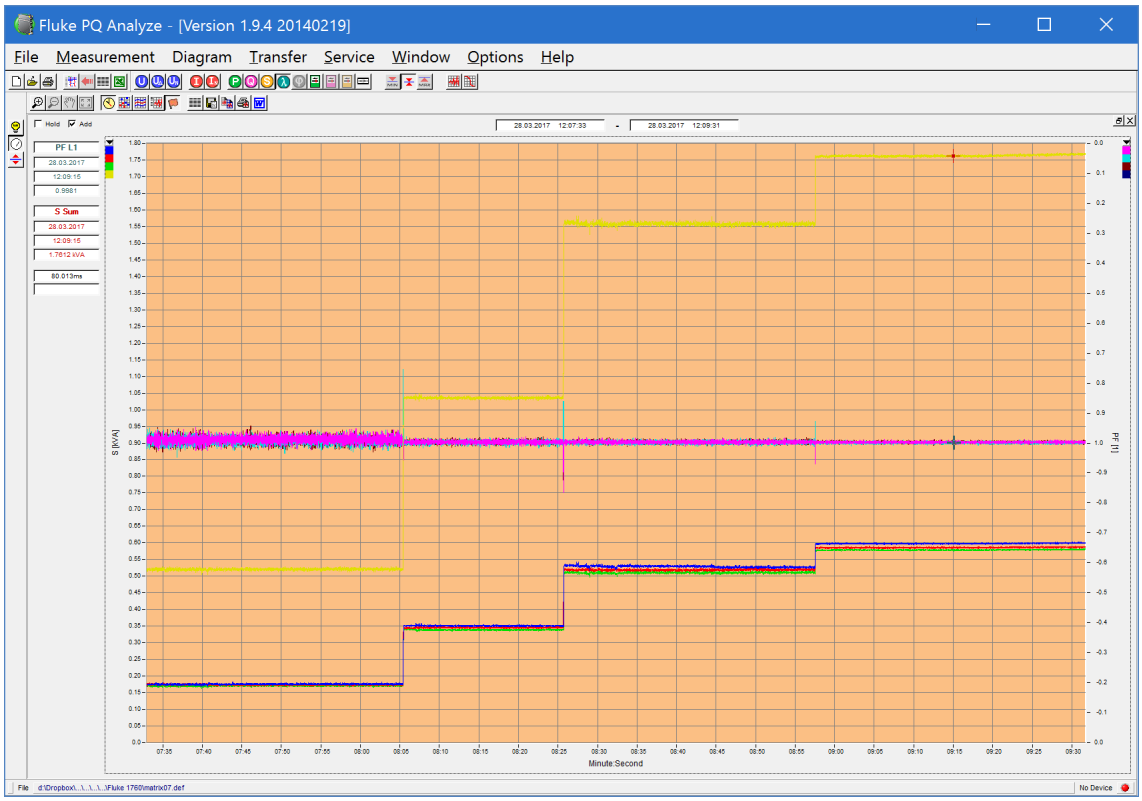

Figure 6.33: Experimental results with the PF controller obtained from the Fluke 1760 Three-phase Power Quality Analyzer. [blue] Apparent power phase-A; [red] Apparent power phase-B; [green] Apparent power phase-C; [yellow] Total apparent power; [magenta] PF.

6.3.6 PQ controller

Some services can be provided to the grid operator by adjusting the active and reactive power that is being exchanged with the electric power grid. By changing the currents i_{gq} and i_{gd} it is possible to control the active and reactive power at the grid interface. The controller proposed in Figure 4.13 was implemented in the DSP. The gains of both PI controllers for P_g and Q_g are $K_{p,PQ}$=0.002 and $K_{i,PQ}$=300. An experiment to verify the performance of this controller was performed by cyclically changing the references of P_g^* and Q_g^*. Figure 6.34 shows the grid currents and the battery current during this test. Additional signals from the PQ controller are also depicted in Figure 6.35. As can be seen, both P_g and Q_g follow the references and are well controlled. The step response has a rise time lower than 25ms and a settling time under three cycles of the grid voltage. When Q_g changes to -400 VA the current i_{gq} slightly increases to compensate the voltage drop at the input of the converter. Comparing with the simulation results of Figure 4.13, this did not occur because V_i was kept constant. When P_g steps from 1250 W to -1250 W a

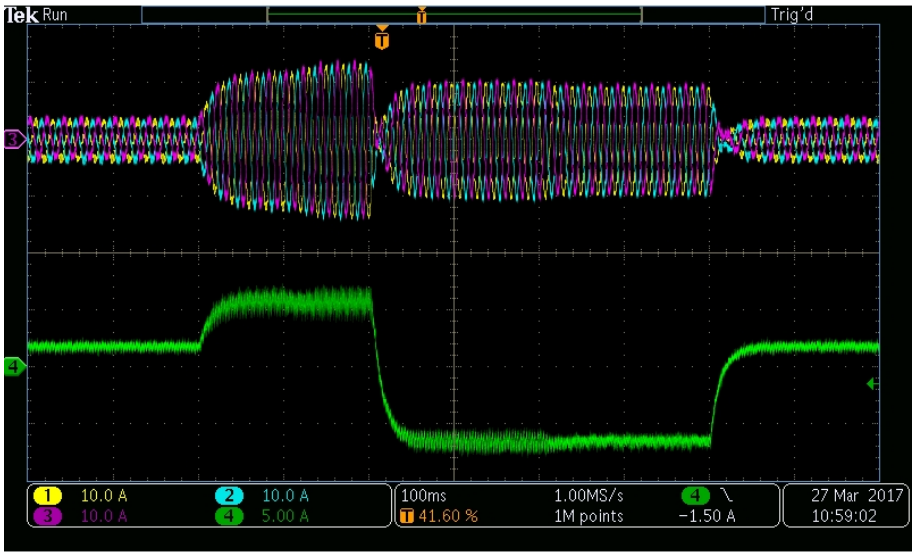

Figure 6.34: Experimental results of the HFLMC operating with the PQ controller: Grid currents ($i_{ga,b,c}$) [CH1,CH2,CH3] and battery current (i_{dc}) [CH4].

perturbation appears on Q_g. Compared with the simulation, it was necessary more time to correct Q_g because the control variable φ was near saturation due to the correction of the reactive power of C_f. Regarding the interface with the battery pack, i_{dc} is a result of the active power exchanged with the grid. With this experiment, it was successfully verified the operation of the HFLMC in the 4Q.

6.4 Conclusion

A detailed description of the prototype and the testbench was presented in the first part of this chapter. The prototype allowed to perform all the experimental tests to verify the capabilities of the proposed modulation and the control architecture. As demonstrated, the grid currents can be decoupled and controlled in the synchronous reference frame. The flexibility to adjust the phase of the grid currents allied with the capacity to regulate the current and voltage in the batteries was experimentally verified. Moreover, it was demonstrated that the grid currents are modulated with low distortion and in compliance with the IEC 61000-3-2 standard. Finally, a PQ control strategy can be implemented to provide additional services to the grid operator.

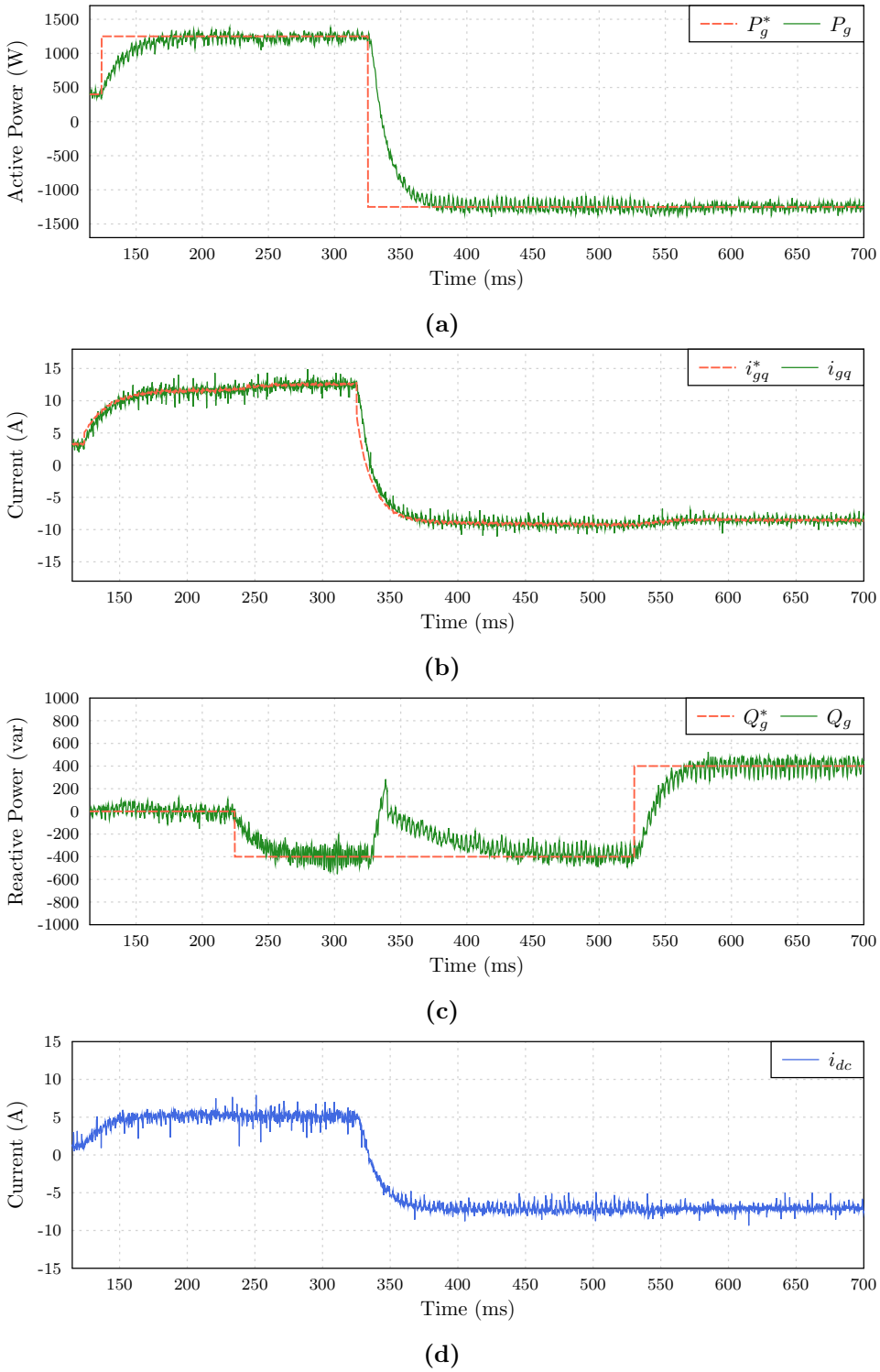

Figure 6.35: Experimental results of the HFLMC operating with the PQ controller. (a) Active power and set-point P_g^*. (b) q reference (i_{gq}^*) and actual q grid current (i_{gq}). (c) Reactive power and set-point Q_g^*. (d) Battery current (i_{dc}).

Chapter 7

Conclusions and Future Work

7.1 Final Remarks

This work has investigated a new modulation and additional controllers for a bidirectional and isolated AC-DC power conversion topology, namely the HFLMC. Due to the key features of the resulting PCS, battery energy storage systems seems to have the perfect fit with the proposed technology. The exploration of the functionalities offered by this power electronics converter were evaluated under the CES concept. On-board charger for EVs is also a possible application due to the potential for volume and weight reduction along with the provision of galvanic isolation.

The generation of sinusoidal currents in the grid interface can be ensured by the invented modulation. By combining the space vector approach with the phase-shift principle it was possible to formulate a new modulation for the HFLMC topology. Due to the essence of the modulation, transition from charger to inverter mode occurs smoothly. This simplifies the formulation of closed-loop controllers and the respective firmware implementation. Grid currents can be properly regulated in the d-q reference frame with very fast dynamics. Additional control layers can be implemented to perform voltage and current regulation in the battery pack with simultaneous adjustment of the power factor in the grid interface. The extensive simulations presented in Chapter 4 evidence the effectiveness of the developed control architecture. Therefore, this power electronics converter seems to be suitable for battery based applications that require bidirectional power flow and galvanic isolation in a compact design.

The use of a voltage-based commutation strategy for the matrix converter enables soft-switching commutations. As a consequence, the switching losses are reduced and the converter operates with lower temperatures. Moreover, the heatsink used to extract the heat from the power semiconductors can be smaller enabling a compact design. The developed gate driver circuit for the 1200 V/25 mΩ SiC MOSFETS has been proved to effectively command the bidirectional switches while keeping the safety of the converter through the embedded protections.

The developed prototype allowed to perform several experimental tests in order to validate the theoretical analysis and the simulation results. The proposed algorithms to control the grid currents in the *d-q* frame and also the voltage and current regulation in the battery showed identical dynamic response, as experimentally demonstrated in Chapter 6. The power factor adjustment in the grid side is an important feature for the smart grids allowing voltage support functionalities, which can also be implemented with the proposed control framework. The P-Q controller was also validated in the SGEV laboratory. Finally, the grid currents evidenced a low THD making this converter compliant with the international standards for power quality.

The results presented along the chapters and appendix allowed to answer positively to the three research questions placed in Section 1.3. The methods and controllers, as well as the simulation and experimental results provide scientific support for the conclusions. Following, each research questions is answered with additional details.

RQ 1 *Is it possible to create a new modulation to operate the HFLMC with sufficient low losses and high switching frequency that allows to reduce the volume of the heat sink and passive components, resulting in high power density solution for the PCS?*

A new modulation for the HFLMC was invented as described in Chapter 4. The resulting power conversion system is suitable for application in CES systems. A detailed comparison between the HFLMC and the conventional solution based on VSC-DAB was performed considering a practical implementation. The results are documented in Appendix J and were also published in a conference paper [91]. Despite the modulation frequency being 20 kHz, the transistors switch four or five times for each period of the modulation. Therefore, the effective switching frequency of the transistors is 80 kHz or 100 kHz. It was concluded that the solution based on the HFLMC has the potential to reduce the total volume and weight of the converter by avoiding the DC-link and decreasing the size of the magnetic devices. The efficiency was found to be similar to the VSC-DAB based solution in the voltage range of interest.

RQ 2 *Could this new modulation allow to control simultaneously the active and reactive power in the grid and the current in the batteries, complying with the respective requirements imposed by the grid interconnection and the batteries operation?*

The invented modulation allows the decoupled control of the grid currents in the *dq* reference frame, using the controller proposed in Figure 4.7. At the grid interface, smooth and controlled current waveforms were observed for two critical situations: the converter start-up and the power flow inversion at full load. Above this internal control layer, other controllers were proposed and tested such as: the battery voltage and current controller and the PQ controller. By defining a reference for the , the PQ controller adjusts the set-points for the grid currents controller in order to

properly regulate the Active and Reactive power. The battery current is a function of the Active power and the DC voltage. In turn, the other control approach is capable to accurately regulate the battery voltage and current while allows the adjustment of the power factor in the grid. These controllers were projected in Chapter 4 and well validated through experimental tests documented in Chapter 6. The measurement of the harmonics proved the high quality of the grid currents and compliance with the international standards. Similarly, the current ripple in the battery pack is below 10 %, which stands for a good performance considering most of the application requirements.

RQ 3 *Is it possible to formulate a P-Q controller for the HFLMC to allow the CES unit to be involved in maintaining static voltage stability by proving reactive power, and to keep connected during frequency deviations in order to contribute for the stability of the power system?*

A PQ controller can be implemented above the internal control layer established for the *dq* components of the grid currents. The PQ controller adjusts the set-points for the grid currents controller in order to properly regulate the Active and Reactive power. In this control mode, the battery current is a function of the Active power and the DC voltage. Advanced functionalities can be implemented above this control layer in order to provide services for the grid operation. Specifically, the CES unit can provide reactive power following the curve defined in Figure 1.9. A frequency droop can also be programmed in the firmware in order to contribute for the stability of the power system.

The key features of the power conversion system for the CES unit based on the HFLMC topology and the proposed modulation are:

- Single-stage power conversion
- Bidirectional power flow
- Galvanic isolation
- Buck-boost operation
- Voltage matching by the HFT turns ratio
- Power factor control
- DC voltage and current regulation
- P-Q control
- Zero Voltage Switching
- Absence of DC-link capacitors
- Compact solution with high power density

7.2 Outlook for Future Work

The work conducted in this thesis intended to research power conversion systems for CES applications. The main focus was to propose and experimentally validate a new modulation for the HFLMC topology.

Beyond the contributions provided by this thesis, additional developments could be pursued in order to increase the TRL of the power electronics converter. In this way, it could be interesting to pursue the following ideas:

- The power transformer to be employed in the high-frequency link was designed in Appendix E. Due to lack of time, it was not possible to build this transformer in time to be used in the experimental tests. Thus, the tests were done only with the link-inductor. Despite transformer don't be crucial to validate the modulation and the functionalities, the construction of the transformer should be concluded in order to perform additional tests with it.

- The EMI filter was designed for pre-compliance with the CISPR 11 Class B standard. The insertion losses characterization according the CISPR 17 standard was done. However, the effectiveness of the filter was not tested following the procedure described in CISPR 16 because the required conditions were not available at the INESC TEC laboratory. It could be interesting to perform a formal test in other facilities to check the compliance with the referred international standards.

- As described in Chapter 6, the experimental tests were done with $V_{g,l-l}$ up to 130 V and Vdc=200 V. The converter exchanged almost 2 kW of power both in charger and inverter mode. Despite these test conditions being enough to validate the modulation and the control algorithms, additional tests at the rated specifications listed in Table 1.4 should be done.

- The battery voltage and current controllers were tested with a battery pack of 2.3 kWh capacity and 192V nominal voltage. This pack is composed by 16 cells of UL12-12 connected in series. Additional tests must be done using lithium-ion technology and a battery pack with higher voltage. It will be necessary to implement the communication algorithm with the BMS of the battery pack.

- The benefits obtained by the introduction of this BESS in a low-voltage network under the CES concept should be assessed. The test scenario with RES and EVs can be tested in the SGEV laboratory of INESC TEC using the installed infrastructure. LVRT capability could also be evaluated following the tests defined by the IEEE 2030.3-2016 standard.

- Regarding the modulation, small variations in its formulation can be topic for further research in order to increase the conversion efficiency. For example, variable

frequency modulation should be evaluated for light load operation. Other switching pattern can also be subject of study to reduce switching losses and promote ZVS and/or ZCS.

- Flux reset in the high-frequency transformer must be ensured in every modulation period. Additional research should be done to eventually implement modifications in the modulation to avoid DC offset of the magnetizing flux.

- As can be seen in Appendix I, the prototype is resting on the testbench. In order to facilitate the transport and provide robustness to the converter, an enclosure must be designed and built.

- For commercial purposes and industrialization of this PCS, other alternatives in terms of components must be evaluated in order to reduce the total cost of the system. Liquid cooling could also be considered in order to further reduce the size of the converter.

- A new prototype can be projected to integrate all the improvements discussed above with the objective to increase the TRL for the 6 or 7 level. This new design should now focus in the power density increment to demonstrate the advantages of this solution. The respective comparison with other commercial PCS should be done in order to obtain a benchmark.

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Appendix A

Supplement to Chapter 4

The proposed modulation for the HFLMC was presented in Section 4.2. However, the derivation of the average currents in (4.16) and the duty-cycles in (4.17) was not presented. Following, a detailed analysis of the i_L current at the different instants of the modulation is developed. This current is essential for the deduction of the average currents at the input of the MC. Then, the duty cycles are determined in order to modulate the grid currents according the reference space vector.

In the following analysis, the average currents at the input of the MC will be determined for sector 1, without loss of generality. In this sector, SSVs I_1, I_2, I_4, I_5, and I_7 are applied to the transformer by the MC in order to modulate the reference current vector $\bar{i}_i^*$. The values for the current i_L at the different switching instants inside the modulation period are as follows:

$$
\begin{aligned}
I_{L1} &= i_L(t_1) = I_0 + \frac{V_1 + nV_o}{L}\frac{\delta}{2}\frac{d_1}{2}T_s \\
I_{L2} &= i_L(t_2) = I_0 + \frac{V_1}{L}\frac{d_1}{2}T_s - \frac{nV_o}{L}(1-\delta)\frac{d_1}{2}T_s \\
I_{L3} &= i_L(t_3) = I_0 + \frac{V_1}{L}(2-\delta)\frac{d_1}{4}T_s - \frac{nV_o}{L}(2-\delta)\frac{d_1}{4}T_s \\
I_{L4} &= i_L(t_4) = I_0 \\
I_{L5} &= i_L(t_5) = I_0 + \frac{V_2 + nV_o}{L}\frac{\delta}{2}\frac{d_2}{2}T_s \\
I_{L6} &= i_L(t_6) = I_0 + \frac{V_2}{L}\frac{d_2}{2}T_s - \frac{nV_o}{L}(1-\delta)\frac{d_2}{2}T_s \\
I_{L7} &= i_L(t_7) = I_0 + \frac{V_2}{L}(2-\delta)\frac{d_2}{4}T_s - \frac{nV_o}{L}(2-\delta)\frac{d_2}{4}T_s \\
I_{L8} &= i_L(t_8) = I_0
\end{aligned}
\tag{A.1}
$$

where the different instants of the modulation are:

$$\begin{aligned}
t_0 &= 0 \\
t_1 &= t_0 + \Delta T_1 = \frac{\delta}{2}\frac{d_1}{2}T_s \\
t_2 &= \frac{d_1}{2}T_s \\
t_3 &= (\frac{\delta}{2}+1)\frac{d_1}{2}T_s \\
t_4 &= d_1 T_s \\
t_5 &= t_4 + \Delta T_2 = d_1 T_s + \frac{\delta}{2}\frac{d_2}{2}T_s \\
t_6 &= (d_1 + \frac{d_2}{2})T_s \\
t_7 &= d_1 T_s + (\frac{\delta}{2}+1)\frac{d_2}{2}T_s \\
t_8 &= (d_1+d_2)T_s.
\end{aligned} \tag{A.2}$$

Then, current i_L can be defined by a piecewise function as follows:

$$i_L(t) = \begin{cases}
\frac{I_{L1}-I_0}{t_1}t + I_0, & 0 \le t \le t_1 \\
\frac{I_{L2}-I_{L1}}{t_2-t_1}t + \frac{I_{L1}t_2 - I_{L2}t_1}{t_2-t_1}, & t_1 \le t \le t_2 \\
\frac{I_{L3}-I_{L2}}{t_3-t_2}t + \frac{I_{L2}t_3 - I_{L3}t_2}{t_3-t_2}, & t_2 \le t \le t_3 \\
\frac{I_{L4}-I_{L3}}{t_4-t_3}t + \frac{I_{L3}t_4 - I_{L4}t_3}{t_4-t_3}, & t_3 \le t \le t_4 \\
\frac{I_{L5}-I_{L4}}{t_5-t_4}t + \frac{I_{L4}t_5 - I_{L5}t_4}{t_5-t_4}, & t_4 \le t \le t_5 \\
\frac{I_{L6}-I_{L5}}{t_6-t_5}t + \frac{I_{L5}t_6 - I_{L6}t_5}{t_6-t_5}, & t_5 \le t \le t_6 \\
\frac{I_{L7}-I_{L6}}{t_7-t_6}t + \frac{I_{L6}t_7 - I_{L7}t_6}{t_7-t_6}, & t_6 \le t \le t_7 \\
\frac{I_{L8}-I_{L7}}{t_8-t_7}t + \frac{I_{L7}t_8 - I_{L8}t_7}{t_8-t_7}, & t_7 \le t \le t_8 \\
I_0, & t_8 \le t \le T_s.
\end{cases} \tag{A.3}$$

As represented in Figure A.1, the virtual currents can be defined as a function of the phase currents. When the SSVs associated with duty-cycle d_1 or d_2 are active, a virtual current flows between the associated phases. For example, in sector 1, when SSVs I_1 or I_4 are applied to the transformer, a virtual current $i_{ab}(t)$ is produced due to V_{ab}. The average value of i_{ab}(t) over a modulation period can be determined through i_L since this

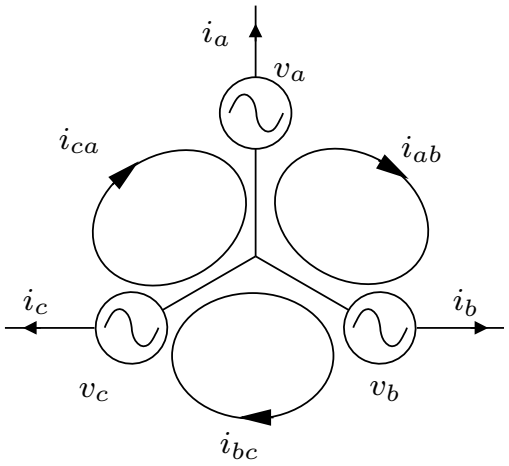


Figure A.1: Relation between virtual currents and phase currents.

current is reflected in the MC input as a function of the applied SSVs:

$$\begin{aligned}\langle i_{ab}\rangle_{Ts} = \frac{1}{T_s}\left[\int_0^{t_2} i_L(t)dt + \int_{t_2}^{t_4} -i_L(t)dt\right] = \frac{1}{T_s}\left[\int_0^{t_1}\left(\frac{I_{L1}-I_0}{t_1}t + I_0\right)dt\right.\\ + \int_{t_1}^{t_2}\left(\frac{I_{L2}-I_{L1}}{t_2-t_1}t + \frac{I_{L1}t_2 - I_{L2}t_1}{t_2-t_1}\right)dt - \int_{t_2}^{t_3}\left(\frac{I_{L3}-I_{L2}}{t_3-t_2}t + \frac{I_{L2}t_3 - I_{L3}t_2}{t_3-t_2}\right)dt\\ \left. - \int_{t_3}^{t_4}\left(\frac{I_{L4}-I_{L3}}{t_4-t_3}t + \frac{I_{L3}t_4 - I_{L4}t_3}{t_4-t_3}\right)dt\right] = \frac{V_o}{4Lf_s}n\delta\left(1-\frac{|\delta|}{2}\right)d_1^2, -1 \le \delta \le 1.\end{aligned} \tag{A.4}$$

By defining $\phi = \delta\frac{\pi}{2}$ the previous result can be rewritten as follows:

$$\langle i_{ab}\rangle_{Ts} = \frac{V_o}{\omega_s L}n\phi\left(1-\frac{|\phi|}{\pi}\right)d_1^2, -\frac{\pi}{2} \le \phi \le \frac{\pi}{2}. \tag{A.5}$$

Using the same approach, the virtual current $i_{ac}(t)$ is determined as:

$$\langle i_{ac}\rangle_{Ts} = \frac{1}{T_s}\left[\int_{t_4}^{t_6} i_L(t)dt + \int_{t_6}^{t_8} -i_L(t)dt\right] = \frac{V_o}{\omega_s L}n\phi\left(1-\frac{|\phi|}{\pi}\right)d_2^2, -\frac{\pi}{2} \le \phi \le \frac{\pi}{2}. \tag{A.6}$$

Regarding $i_{bc}(t)$, this current is zero because none SSV between phase b and c is applied in the sector 1. The phase currents can be calculated considering the well known relation with the virtual currents:

$$\begin{aligned} i_a(t) &= i_{ab}(t) - i_{ca}(t)\\ i_b(t) &= i_{bc}(t) - i_{ab}(t)\\ i_c(t) &= i_{ca}(t) - i_{bc}(t).\end{aligned} \tag{A.7}$$

Then, the average phase currents in sector 1 during a modulation period are:

$$\begin{aligned}\langle i_a\rangle_{Ts} &= \frac{V_o}{\omega_s L} n\phi \left(1 - \frac{|\phi|}{\pi}\right)\left(d_1^2 + d_2^2\right)\\ \langle i_b\rangle_{Ts} &= -\frac{V_o}{\omega_s L} n\phi \left(1 - \frac{|\phi|}{\pi}\right) d_1^2\\ \langle i_c\rangle_{Ts} &= -\frac{V_o}{\omega_s L} n\phi \left(1 - \frac{|\phi|}{\pi}\right) d_2^2.\end{aligned} \tag{A.8}$$

By applying the space vector transformation to the currents in (A.8) it results:

$$\begin{aligned}\bar{i}_i &= \frac{2}{3}\left(\langle i_a\rangle_{Ts} + \langle i_b\rangle_{Ts} e^{j\frac{2\pi}{3}} + \langle i_c\rangle_{Ts} e^{-j\frac{2\pi}{3}}\right)\\ &= \frac{2}{3}\left(b_i\left(d_1^2 + d_2^2\right) + b_i\left(-d_1^2\right)e^{j\frac{2\pi}{3}} + b_i\left(-d_2^2\right)e^{-j\frac{2\pi}{3}}\right)\\ &= \frac{2}{3} b_i \left(d_1^2\left(\frac{3}{2} - j\frac{\sqrt{3}}{2}\right) + d_2^2\left(\frac{3}{2} + j\frac{\sqrt{3}}{2}\right)\right).\end{aligned} \tag{A.9}$$

where $b_i = \frac{V_o}{\omega_s L} n\phi \left(1 - \frac{|\phi|}{\pi}\right)$. In order to properly modulate the grid currents, it is necessary that (A.9) be equal to (4.5):

$$\begin{aligned}I_i \cos(\beta_i) &= \frac{2}{3} b_i \left(\frac{3}{2} d_1^2 + \frac{3}{2} d_2^2\right)\\ I_i \sin(\beta_i) &= \frac{2}{3} b_i \left(-\frac{\sqrt{3}}{2} d_1^2 + \frac{\sqrt{3}}{2} d_2^2\right).\end{aligned} \tag{A.10}$$

By solving both equations in order to d_1 and d_2 results:

$$\begin{aligned}d_1^2 &= \frac{I_i}{b_i} \sin\left(\frac{\pi}{6} - \beta_i\right)\\ d_2^2 &= \frac{I_i}{b_i} \sin\left(\frac{\pi}{6} + \beta_i\right).\end{aligned} \tag{A.11}$$

The relation between the amplitude I_i and the constant b_i can be understood as a current modulation index. By defining $m = \sqrt{I_i/b_i}$ and substituting $\beta_i = \theta_i - \frac{\pi}{6}$ in (A.11), duty cycles d_1, d_2, and d_0 result as in (4.17):

$$\begin{aligned}d_1 &= m\sqrt{\sin\left(\frac{\pi}{3} - \theta_i\right)}\\ d_2 &= m\sqrt{\sin\left(\theta_i\right)}\\ d_0 &= 1 - d_1 - d_2.\end{aligned} \tag{A.12}$$

Appendix B

Switching states of the Variable-step VBC

The variable-step VBC strategy described in Section 3.4.2 was applied in this research work. Considering the safe states previously detailed in Table 3.12, the switching states for each normal and critical interval can be defined in each sector for S_{aX}, S_{bX}, and S_{cX} as listed in Table B.1, Table B.2, Table B.3, Table B.4.

Table B.1: Main switching states in normal intervals based on relative magnitude of the input voltages [229].

Normal intervals	Relative voltage	Main state	S_{aX1}	S_{aX2}	S_{bX1}	S_{bX2}	S_{cX1}	S_{cX2}
I	$V_{ga} > V_{gb} > V_{gc}$	a^I	1	1	1	0	1	0
		b^I	0	1	1	1	1	0
		c^I	0	1	0	1	1	1
II	$V_{gb} > V_{ga} > V_{gc}$	a^{II}	1	1	0	1	1	0
		b^{II}	1	0	1	1	1	0
		c^{II}	0	1	0	1	1	1
III	$V_{gb} > V_{gc} > V_{ga}$	a^{III}	1	1	0	1	0	1
		b^{III}	1	0	1	1	1	0
		c^{III}	1	0	0	1	1	1
IV	$V_{gc} > V_{gb} > V_{ga}$	a^{IV}	1	1	0	1	0	1
		b^{IV}	1	0	1	1	0	1
		c^{IV}	1	0	1	0	1	1
V	$V_{gc} > V_{ga} > V_{gb}$	a^V	1	1	1	0	0	1
		b^V	0	1	1	1	0	1
		c^V	1	0	1	0	1	1
VI	$V_{ga} > V_{gc} > V_{gb}$	a^{VI}	1	1	1	0	1	0
		b^{VI}	0	1	1	1	0	1
		c^{VI}	0	1	1	0	1	1

Table B.2: Commutation switching states in normal intervals based on relative magnitude of the input voltages [229].

Normal intervals	Relative voltage	Main state	S_{aX1}	S_{aX2}	S_{bX1}	S_{bX2}	S_{cX1}	S_{cX2}
I	$V_{ga} > V_{gb} > V_{gc}$	ab^{I}	0	1	1	0	1	0
		bc^{I}	0	1	0	1	1	0
		ca^{I}	0	1	0	0	1	0
II	$V_{gb} > V_{ga} > V_{gc}$	ab^{II}	1	0	0	1	1	0
		bc^{II}	0	0	0	1	1	0
		ca^{II}	0	1	0	1	1	0
III	$V_{gb} > V_{gc} > V_{ga}$	ab^{III}	1	0	0	1	0	0
		bc^{III}	1	0	0	1	1	0
		ca^{III}	1	0	0	1	0	1
IV	$V_{gc} > V_{gb} > V_{ga}$	ab^{IV}	1	0	0	1	0	1
		bc^{IV}	1	0	1	0	0	1
		ca^{IV}	1	0	0	0	0	1
V	$V_{gc} > V_{ga} > V_{gb}$	ab^{V}	0	1	1	0	0	1
		bc^{V}	0	0	1	0	0	1
		ca^{V}	1	0	1	0	0	1
VI	$V_{ga} > V_{gc} > V_{gb}$	ab^{VI}	0	1	1	0	0	0
		bc^{VI}	0	1	1	0	0	1
		ca^{VI}	0	1	1	0	1	0

Table B.3: Main switching states in critical intervals based on relative magnitude of the input voltages [229].

Critical intervals	Relative voltage	Main state	S_{aX1}	S_{aX2}	S_{bX1}	S_{bX2}	S_{cX1}	S_{cX2}
I-II (H)	$V_{ga} \approx V_{gb} > V_{gc}$	a^{I-II}	1	1	0	0	1	0
		b^{I-II}	0	0	1	1	1	0
		c^{I-II}	0	1	0	1	1	1
II-III (L)	$V_{gb} > V_{ga} \approx V_{gc}$	a^{II-III}	1	1	0	1	0	0
		b^{II-III}	1	0	1	1	1	0
		c^{II-III}	0	0	0	1	1	1
III-IV (H)	$V_{gb} \approx V_{gc} > V_{ga}$	a^{III-IV}	1	1	0	1	0	1
		b^{III-IV}	1	0	1	1	0	0
		c^{III-IV}	1	0	0	0	1	1
IV-V (L)	$V_{gc} > V_{gb} \approx V_{ga}$	a^{IV-V}	1	1	0	0	0	1
		b^{IV-V}	0	0	1	1	0	1
		c^{IV-V}	1	0	1	0	1	1
V-VI (H)	$V_{gc} \approx V_{ga} > V_{gb}$	a^{V-VI}	1	1	1	0	0	0
		b^{V-VI}	0	1	1	1	0	1
		c^{V-VI}	0	0	1	0	1	1
VI-I (L)	$V_{ga} > V_{gc} \approx V_{gb}$	a^{VI-I}	1	1	1	0	1	0
		b^{VI-I}	0	1	1	1	0	0
		c^{VI-I}	0	1	0	0	1	1

Table B.4: Commutation switching states in critical intervals based on relative magnitude of the input voltages [229].

Critical intervals	Relative voltage	Main state	S_{aX1}	S_{aX2}	S_{bX1}	S_{bX2}	S_{cX1}	S_{cX2}
I-II (H)	$V_{ga} \approx V_{gb} > V_{gc}$	ab^{I-II}	0	1	0	1	1	0
		bc^{I-II}	0	0	0	1	1	0
		ca^{I-II}	0	1	0	0	1	0
II-III (L)	$V_{gb} > V_{ga} \approx V_{gc}$	ab^{II-III}	1	0	0	1	0	0
		bc^{II-III}	0	0	0	1	1	0
		ca^{II-III}	1	0	0	1	1	0
III-IV (H)	$V_{gb} \approx V_{gc} > V_{ga}$	ab^{III-IV}	1	0	0	1	0	0
		bc^{III-IV}	1	0	0	1	0	1
		ca^{III-IV}	1	0	0	0	0	1
IV-V (L)	$V_{gc} > V_{gb} \approx V_{ga}$	ab^{IV-V}	1	0	1	0	0	1
		bc^{IV-V}	0	0	1	0	0	1
		ca^{IV-V}	1	0	0	0	0	1
V-VI (H)	$V_{gc} \approx V_{ga} > V_{gb}$	ab^{V-VI}	0	1	1	0	0	0
		bc^{V-VI}	0	0	1	0	0	1
		ca^{V-VI}	0	1	1	0	0	1
VI-I (L)	$V_{ga} > V_{gc} \approx V_{gb}$	ab^{VI-I}	0	1	1	0	0	0
		bc^{VI-I}	0	1	1	0	1	0
		ca^{VI-I}	0	1	0	0	1	0

Appendix C

Variable-step VBC strategy: source code

The source code developed during this work for the variable-step voltage-base commutation strategy is reproduced bellow. This VHDL code was tested and validated in the MachXO2 FPGA LCMXO2-7000HE-4TG144C from Lattice.

```
1  --##############################################################################
2  -- AUTHOR:      Diogo Varajao
3  -- CONTACT:     diogo.varajao@ieee.com
4  -- LOCAL:       INESC TEC, Porto, PORTUGAL
5  -- CREATED:     March 2017
6  -- VERSION:     2.0
7  --##############################################################################
8
9  LIBRARY ieee;
10 USE ieee.std_logic_1164.all;
11 USE ieee.numeric_std.all;
12
13 entity MC_4step_VBC is
14   Port(
15     clk_tc       : in std_logic;   -- clock for state transition
16     enable       : in std_logic;
17     sectorVi     : in std_logic_vector(2 downto 0);
18     sectorC      : in std_logic;
19     SaX          : in std_logic;
20     SbX          : in std_logic;
21     ScX          : in std_logic;
22     SaX2         : out std_logic;
23     SaX1         : out std_logic;
24     SbX2         : out std_logic;
25     SbX1         : out std_logic;
26     ScX2         : out std_logic;
27     ScX1         : out std_logic
28     );
29 end MC_4step_VBC;
30
31 architecture moore of MC_4step_VBC is
32
33    type state_type is (stop, A1, B1, C1, AB1, BC1, CA1, A12, B12, C12, A12,
34                  B12, C12, AB12, BC12, CA12, A2, B2, C2, AB2, BC2, CA2, A23,
35                  B23, C23, AB23, BC23, CA23, A3, B3, C3, AB3, BC3, CA3, A34,
```

```
36                  B34, C34, AB34, BC34, CA34, A4, B4, C4, AB4, BC4, CA4, A45,
37                  B45, C45, AB45, BC45, CA45, A5, B5, C5, AB5, BC5, CA5, A56,
38                  B56, C56, AB56, BC56, CA56, A6, B6, C6, AB6, BC6, CA6, A61,
39                  B61, C61, AB61, BC61, CA61);
40
41  signal state_reg, state_next  : state_type := stop;
42
43  signal Sabc    : std_logic_vector(2 downto 0); -- switching signals
44  signal Sabc_pre : std_logic_vector(2 downto 0);
45
46  signal sectorHL    : INTEGER RANGE 0 TO 61 := 0; -- sector with critical intervals
47  signal sectorHL_pre : INTEGER RANGE 0 TO 61 := 0;
48
49  signal startup : std_logic := '1';
50
51 begin
52
53  -- STATE UPDATE AND TIMING WITH ASYNCH ACTIVE LOW RESET
54  process(clk_tc, enable, SaX, SbX, ScX, sectorVi(2 downto 0), sectorHL, state_next)
55  begin
56    if(enable = '0') then
57      state_reg <= stop;
58      sectorHL <= 0;
59      sectorHL_pre <= 0;
60      startup <= '1';
61    elsif(rising_edge(clk_tc)) then
62
63      -- sample of modulation signals
64      if(     (SaX = '0') and (SbX = '0') and (ScX = '1') ) then
65        Sabc <= "001";
66      elsif( (SaX = '0') and (SbX = '1') and (ScX = '0') ) then
67        Sabc <= "010";
68      elsif( (SaX = '1') and (SbX = '0') and (ScX = '0') ) then
69        Sabc <= "100";
70      else
71        Sabc <= Sabc_pre;
72      end if;
73
74      Sabc_pre <= Sabc;
75
76      -- detect sector during start-up (start the operation at the peak of Va)
77      if( startup = '1' ) then
78        if( (sectorVi(2) = '0') and (sectorVi(1) = '0') and (sectorVi(0) = '1')
79                                and (sectorC = '0') ) then
80          sectorHL <= 1;
81          sectorHL_pre <= 1;
82          startup <= '0';
83        else
84          sectorHL <= 0;
85          sectorHL_pre <= 0;
86          startup <= '1';
87        end if;
88
89        state_reg <= stop;
90
91      else
92
```

```
93          if(     (sectorVi(2) = '0') and (sectorVi(1) = '0') and (sectorVi(0) = '1')
94                                      and (sectorC = '1') ) then
95            sectorHL <= 12;
96          elsif( (sectorVi(2) = '0') and (sectorVi(1) = '1') and (sectorVi(0) = '0')
97                                      and (sectorC = '0') ) then
98            sectorHL <= 2;
99          elsif( (sectorVi(2) = '0') and (sectorVi(1) = '1') and (sectorVi(0) = '0')
100                                     and (sectorC = '1') ) then
101           sectorHL <= 23;
102         elsif( (sectorVi(2) = '0') and (sectorVi(1) = '1') and (sectorVi(0) = '1')
103                                     and (sectorC = '0') ) then
104           sectorHL <= 3;
105         elsif( (sectorVi(2) = '0') and (sectorVi(1) = '1') and (sectorVi(0) = '1')
106                                     and (sectorC = '1') ) then
107           sectorHL <= 34;
108         elsif( (sectorVi(2) = '1') and (sectorVi(1) = '0') and (sectorVi(0) = '0')
109                                     and (sectorC = '0') ) then
110           sectorHL <= 4;
111         elsif( (sectorVi(2) = '1') and (sectorVi(1) = '0') and (sectorVi(0) = '0')
112                                     and (sectorC = '1') ) then
113           sectorHL <= 45;
114         elsif( (sectorVi(2) = '1') and (sectorVi(1) = '0') and (sectorVi(0) = '1')
115                                     and (sectorC = '0') ) then
116           sectorHL <= 5;
117         elsif( (sectorVi(2) = '1') and (sectorVi(1) = '0') and (sectorVi(0) = '1')
118                                     and (sectorC = '1') ) then
119           sectorHL <= 56;
120         elsif( (sectorVi(2) = '1') and (sectorVi(1) = '1') and (sectorVi(0) = '0')
121                                     and (sectorC = '0') ) then
122           sectorHL <= 6;
123         elsif( (sectorVi(2) = '1') and (sectorVi(1) = '1') and (sectorVi(0) = '0')
124                                     and (sectorC = '1') ) then
125           sectorHL <= 61;
126         elsif( (sectorVi(2) = '0') and (sectorVi(1) = '0') and (sectorVi(0) = '1')
127                                     and (sectorC = '0') ) then
128           sectorHL <= 1;
129         else
130           sectorHL <= sectorHL_pre;
131         end if;
132
133         sectorHL_pre <= sectorHL;
134
135         state_reg <= state_next;
136
137       end if;
138
139     end if;
140   end process;
141
142
143   -- CONTROL LOGIC STATE MACHINE
144   process(state_reg, Sabc, sectorHL)
145   begin
146
147     -- default conditions
148     state_next <= state_reg;
149
```

```
150     case state_reg is
151
152       -- stop state
153       when stop =>
154         if(    Sabc = "001" and (sectorHL = 1) ) then
155           state_next <= C1;
156         elsif( Sabc = "010" and (sectorHL = 2) ) then
157           state_next <= B2;
158         elsif( Sabc = "100" and (sectorHL = 3) ) then
159           state_next <= A3;
160         elsif( Sabc = "001" and (sectorHL = 4) ) then
161           state_next <= C4;
162         elsif( Sabc = "010" and (sectorHL = 5) ) then
163           state_next <= B5;
164         elsif( Sabc = "100" and (sectorHL = 6) ) then
165           state_next <= A6;
166         else
167           state_next <= stop;
168         end if;
169
170       --#### SECTOR I (1) H-type interval ####
171
172       -- SaX ON
173       when A1 =>
174         if(   sectorHL = 12 ) then
175           state_next <= A12;
176         elsif( Sabc = "010" ) then
177           state_next <= AB1;
178         elsif( Sabc = "001" ) then
179           state_next <= CA1;
180         else
181           state_next <= A1;
182         end if;
183
184       -- SbX ON
185       when B1 =>
186         if(   sectorHL = 12 ) then
187           state_next <= B12;
188         elsif( Sabc = "100" ) then
189           state_next <= AB1;
190         elsif( Sabc = "001" ) then
191           state_next <= BC1;
192         else
193           state_next <= B1;
194         end if;
195
196       -- ScX ON
197       when C1 =>
198         if(    sectorHL = 12 ) then
199           state_next <= C12;
200         elsif( Sabc = "100" ) then
201           state_next <= CA1;
202         elsif( Sabc = "010" ) then
203           state_next <= BC1;
204         else
205           state_next <= C1;
206         end if;
```

```
207
208         --  transition AB1
209         when AB1 =>
210           if(     Sabc = "100" ) then
211             state_next <= A1;
212           elsif( Sabc = "010" ) then
213             state_next <= B1;
214           elsif( Sabc = "001" ) then
215             state_next <= B1;
216           else
217             state_next <= AB1;
218           end if;
219
220         --  transition BC1
221         when BC1 =>
222           if(     Sabc = "010" ) then
223             state_next <= B1;
224           elsif( Sabc = "001" ) then
225             state_next <= C1;
226           elsif( Sabc = "100" ) then
227             state_next <= B1;
228           else
229             state_next <= BC1;
230           end if;
231
232         --  transition CA1
233         when CA1 =>
234           if(     Sabc = "100" ) then
235             state_next <= A1;
236           elsif( Sabc = "001" ) then
237             state_next <= C1;
238           elsif( Sabc = "010" ) then
239             state_next <= C1;
240           else
241             state_next <= CA1;
242           end if;
243
244         --#### SECTOR I-II (12) H-type interval ####
245
246         --  SaX ON
247         when A12 =>
248           if(     sectorHL = 2 ) then
249             state_next <= A2;
250           elsif( Sabc = "010" ) then
251             state_next <= CA12;
252           elsif( Sabc = "001" ) then
253             state_next <= CA12;
254           else
255             state_next <= A12;
256           end if;
257
258         --  SbX ON
259         when B12 =>
260           if(     sectorHL = 2 ) then
261             state_next <= B2;
262           elsif( Sabc = "100" ) then
263             state_next <= BC12;
```

```
264         elsif( Sabc = "001" ) then
265           state_next <= BC12;
266         else
267           state_next <= B12;
268         end if;
269
270       -- ScX ON
271       when C12 =>
272         if(     sectorHL = 2 ) then
273           state_next <= C2;
274         elsif( Sabc = "100" ) then
275           state_next <= CA12;
276         elsif( Sabc = "010" ) then
277           state_next <= BC12;
278         else
279           state_next <= C12;
280         end if;
281
282       -- transition AB12
283       when AB12 =>
284         if(     Sabc = "100" ) then
285           state_next <= CA12;
286         elsif( Sabc = "010" ) then
287           state_next <= BC12;
288         elsif( Sabc = "001" ) then
289           state_next <= BC12;
290         else
291           state_next <= AB12;
292         end if;
293
294       -- transition BC12
295       when BC12 =>
296         if(     Sabc = "100" ) then
297           state_next <= AB12;
298         elsif( Sabc = "010" ) then
299           state_next <= B12;
300         elsif( Sabc = "001" ) then
301           state_next <= C12;
302         else
303           state_next <= BC12;
304         end if;
305
306       -- transition CA12
307       when CA12 =>
308         if(     Sabc = "100" ) then
309           state_next <= A12;
310         elsif( Sabc = "010" ) then
311           state_next <= AB12;
312         elsif( Sabc = "001" ) then
313           state_next <= C12;
314         else
315           state_next <= CA12;
316         end if;
317
318       -- #### SECTOR II (2) L-type interval ####
319
320       -- SaX ON
```

```
321         when A2 =>
322           if(    sectorHL = 23 ) then
323             state_next <= A23;
324           elsif( Sabc = "010" ) then
325             state_next <= AB2;
326           elsif( Sabc = "001" ) then
327             state_next <= CA2;
328           else
329             state_next <= A2;
330           end if;
331
332         -- SbX ON
333         when B2 =>
334           if(    sectorHL = 23 ) then
335             state_next <= B23;
336           elsif( Sabc = "100" ) then
337             state_next <= AB2;
338           elsif( Sabc = "001" ) then
339             state_next <= BC2;
340           else
341             state_next <= B2;
342           end if;
343
344         -- ScX ON
345         when C2 =>
346           if(     sectorHL = 23 ) then
347             state_next <= C23;
348           elsif( Sabc = "100" ) then
349             state_next <= CA2;
350           elsif( Sabc = "010" ) then
351             state_next <= BC2;
352           else
353             state_next <= C2;
354           end if;
355
356         -- transition AB2
357         when AB2 =>
358           if(     Sabc = "100" ) then
359             state_next <= A2;
360           elsif( Sabc = "010" ) then
361             state_next <= B2;
362           elsif( Sabc = "001" ) then
363             state_next <= A2;
364           else
365             state_next <= AB2;
366           end if;
367
368         -- transition BC2
369         when BC2 =>
370           if(     Sabc = "010" ) then
371             state_next <= B2;
372           elsif( Sabc = "001" ) then
373             state_next <= C2;
374           elsif( Sabc = "100" ) then
375             state_next <= B2;
376           else
377             state_next <= BC2;
```

```
378         end if;
379
380       -- transition CA2
381       when CA2 =>
382         if(     Sabc = "100" ) then
383           state_next <= A2;
384         elsif( Sabc = "001" ) then
385           state_next <= C2;
386         elsif( Sabc = "010" ) then
387           state_next <= A2;
388         else
389           state_next <= CA2;
390         end if;
391
392       --#### SECTOR II-III (23) L-type interval ####
393
394       -- SaX ON
395       when A23 =>
396         if(     sectorHL = 3 ) then
397           state_next <= A3;
398         elsif( Sabc = "010" ) then
399           state_next <= AB23;
400         elsif( Sabc = "001" ) then
401           state_next <= AB23;
402         else
403           state_next <= A23;
404         end if;
405
406       -- SbX ON
407       when B23 =>
408         if(     sectorHL = 3 ) then
409           state_next <= B3;
410         elsif( Sabc = "100" ) then
411           state_next <= AB23;
412         elsif( Sabc = "001" ) then
413           state_next <= BC23;
414         else
415           state_next <= B23;
416         end if;
417
418       -- ScX ON
419       when C23 =>
420         if(     sectorHL = 3 ) then
421           state_next <= C3;
422         elsif( Sabc = "100" ) then
423           state_next <= BC23;
424         elsif( Sabc = "010" ) then
425           state_next <= BC23;
426         else
427           state_next <= C23;
428         end if;
429
430       -- transition AB23
431       when AB23 =>
432         if(     Sabc = "100" ) then
433           state_next <= A23;
434         elsif( Sabc = "010" ) then
```

```
435             state_next <= B23;
436           elsif( Sabc = "001" ) then
437             state_next <= CA23;
438           else
439             state_next <= AB23;
440           end if;
441
442         -- transition BC23
443         when BC23 =>
444           if(     Sabc = "100" ) then
445             state_next <= CA23;
446           elsif( Sabc = "010" ) then
447             state_next <= B23;
448           elsif( Sabc = "001" ) then
449             state_next <= C23;
450           else
451             state_next <= BC23;
452           end if;
453
454         -- transition CA23
455         when CA23 =>
456           if(     Sabc = "100" ) then
457             state_next <= AB23;
458           elsif( Sabc = "001" ) then
459             state_next <= BC23;
460           elsif( Sabc = "010" ) then
461             state_next <= AB23;
462           else
463             state_next <= CA23;
464           end if;
465
466         --#### SECTOR III (3) H-type interval ####
467
468         -- SaX ON
469         when A3 =>
470           if(    sectorHL = 34 ) then
471             state_next <= A34;
472           elsif( Sabc = "010" ) then
473             state_next <= AB3;
474           elsif( Sabc = "001" ) then
475             state_next <= CA3;
476           else
477             state_next <= A3;
478           end if;
479
480         -- SbX ON
481         when B3 =>
482           if(    sectorHL = 34 ) then
483             state_next <= B34;
484           elsif( Sabc = "100" ) then
485             state_next <= AB3;
486           elsif( Sabc = "001" ) then
487             state_next <= BC3;
488           else
489             state_next <= B3;
490           end if;
491
```

```
492         --  ScX ON
493         when C3 =>
494           if(     sectorHL = 34 ) then
495             state_next <= C34;
496           elsif( Sabc = "100" ) then
497             state_next <= CA3;
498           elsif( Sabc = "010" ) then
499             state_next <= BC3;
500           else
501             state_next <= C3;
502           end if;
503
504         --  transition AB3
505         when AB3 =>
506           if(     Sabc = "100" ) then
507             state_next <= A3;
508           elsif( Sabc = "010" ) then
509             state_next <= B3;
510           elsif( Sabc = "001" ) then
511             state_next <= A3;
512           else
513             state_next <= AB3;
514           end if;
515
516         --  transition BC3
517         when BC3 =>
518           if(     Sabc = "010" ) then
519             state_next <= B3;
520           elsif( Sabc = "001" ) then
521             state_next <= C3;
522           elsif( Sabc = "100" ) then
523             state_next <= C3;
524           else
525             state_next <= BC3;
526           end if;
527
528         --  transition CA3
529         when CA3 =>
530           if(     Sabc = "100" ) then
531             state_next <= A3;
532           elsif( Sabc = "001" ) then
533             state_next <= C3;
534           elsif( Sabc = "010" ) then
535             state_next <= C3;
536           else
537             state_next <= CA3;
538           end if;
539
540         --#### SECTOR III-IV (34) H-type interval ####
541
542         --  SaX ON
543         when A34 =>
544           if(     sectorHL = 4 ) then
545             state_next <= A4;
546           elsif( Sabc = "010" ) then
547             state_next <= AB34;
548           elsif( Sabc = "001" ) then
```

```
549             state_next <= CA34;
550           else
551             state_next <= A34;
552           end if;
553
554         -- SbX ON
555         when B34 =>
556           if(     sectorHL = 4 ) then
557             state_next <= B4;
558           elsif( Sabc = "100" ) then
559             state_next <= AB34;
560           elsif( Sabc = "001" ) then
561             state_next <= AB34;
562           else
563             state_next <= B34;
564           end if;
565
566         -- ScX ON
567         when C34 =>
568           if(     sectorHL = 4 ) then
569             state_next <= C4;
570           elsif( Sabc = "100" ) then
571             state_next <= CA34;
572           elsif( Sabc = "010" ) then
573             state_next <= CA34;
574           else
575             state_next <= C34;
576           end if;
577
578         -- transition AB34
579         when AB34 =>
580           if(     Sabc = "100" ) then
581             state_next <= A34;
582           elsif( Sabc = "010" ) then
583             state_next <= B34;
584           elsif( Sabc = "001" ) then
585             state_next <= BC34;
586           else
587             state_next <= AB34;
588           end if;
589
590         -- transition BC34
591         when BC34 =>
592           if(     Sabc = "010" ) then
593             state_next <= AB34;
594           elsif( Sabc = "001" ) then
595             state_next <= CA34;
596           elsif( Sabc = "100" ) then
597             state_next <= CA34;
598           else
599             state_next <= BC34;
600           end if;
601
602         -- transition CA34
603         when CA34 =>
604           if(     Sabc = "100" ) then
605             state_next <= A34;
```

```
606           elsif( Sabc = "010" ) then
607             state_next <= BC34;
608           elsif( Sabc = "001" ) then
609             state_next <= C34;
610           else
611             state_next <= CA34;
612           end if;
613
614         --#### SECTOR IV (4) L-type interval ####
615
616         --  SaX ON
617         when A4 =>
618           if(   sectorHL = 45 ) then
619             state_next <= A45;
620           elsif( Sabc = "010" ) then
621             state_next <= AB4;
622           elsif( Sabc = "001" ) then
623             state_next <= CA4;
624           else
625             state_next <= A4;
626           end if;
627
628         --  SbX ON
629         when B4 =>
630           if(   sectorHL = 45 ) then
631             state_next <= B45;
632           elsif( Sabc = "100" ) then
633             state_next <= AB4;
634           elsif( Sabc = "001" ) then
635             state_next <= BC4;
636           else
637             state_next <= B4;
638           end if;
639
640         --  ScX ON
641         when C4 =>
642           if(    sectorHL = 45 ) then
643             state_next <= C45;
644           elsif( Sabc = "100" ) then
645             state_next <= CA4;
646           elsif( Sabc = "010" ) then
647             state_next <= BC4;
648           else
649             state_next <= C4;
650           end if;
651
652         --  transition AB4
653         when AB4 =>
654           if(    Sabc = "100" ) then
655             state_next <= A4;
656           elsif( Sabc = "010" ) then
657             state_next <= B4;
658           elsif( Sabc = "001" ) then
659             state_next <= B4;
660           else
661             state_next <= AB4;
662           end if;
```

```
663
664         --  transition BC4
665         when BC4 =>
666           if(     Sabc = "010" ) then
667             state_next <= B4;
668           elsif( Sabc = "001" ) then
669             state_next <= C4;
670           elsif( Sabc = "100" ) then
671             state_next <= B4;
672           else
673             state_next <= BC4;
674           end if;
675
676         --  transition CA4
677         when CA4 =>
678           if(     Sabc = "100" ) then
679             state_next <= A4;
680           elsif( Sabc = "001" ) then
681             state_next <= C4;
682           elsif( Sabc = "010" ) then
683             state_next <= C4;
684           else
685             state_next <= CA4;
686           end if;
687
688         --#### SECTOR IV-V (45) L-type interval ####
689
690         --  SaX ON
691         when A45 =>
692           if(     sectorHL = 5 ) then
693             state_next <= A5;
694           elsif( Sabc = "010" ) then
695             state_next <= CA45;
696           elsif( Sabc = "001" ) then
697             state_next <= CA45;
698           else
699             state_next <= A45;
700           end if;
701
702         --  SbX ON
703         when B45 =>
704           if(     sectorHL = 5 ) then
705             state_next <= B5;
706           elsif( Sabc = "100" ) then
707             state_next <= BC45;
708           elsif( Sabc = "001" ) then
709             state_next <= BC45;
710           else
711             state_next <= B45;
712           end if;
713
714         --  ScX ON
715         when C45 =>
716           if(     sectorHL = 5 ) then
717             state_next <= C5;
718           elsif( Sabc = "100" ) then
719             state_next <= CA45;
```

```
720         elsif( Sabc = "010" ) then
721           state_next <= BC45;
722         else
723           state_next <= C45;
724         end if;
725
726       -- transition AB45
727       when AB45 =>
728         if(     Sabc = "100" ) then
729           state_next <= CA45;
730         elsif( Sabc = "010" ) then
731           state_next <= BC45;
732         elsif( Sabc = "001" ) then
733           state_next <= BC45;
734         else
735           state_next <= AB45;
736         end if;
737
738       -- transition BC45
739       when BC45 =>
740         if(     Sabc = "100" ) then
741           state_next <= AB45;
742         elsif( Sabc = "010" ) then
743           state_next <= B45;
744         elsif( Sabc = "001" ) then
745           state_next <= C45;
746         else
747           state_next <= BC45;
748         end if;
749
750       -- transition CA45
751       when CA45 =>
752         if(     Sabc = "100" ) then
753           state_next <= A45;
754         elsif( Sabc = "010" ) then
755           state_next <= AB45;
756         elsif( Sabc = "001" ) then
757           state_next <= C45;
758         else
759           state_next <= CA45;
760         end if;
761
762       --#### SECTOR V (5) H-type interval ####
763
764       -- SaX ON
765       when A5 =>
766         if(    sectorHL = 56 ) then
767           state_next <= A56;
768         elsif( Sabc = "010" ) then
769           state_next <= AB5;
770         elsif( Sabc = "001" ) then
771           state_next <= CA5;
772         else
773           state_next <= A5;
774         end if;
775
776       -- SbX ON
```

```
777         when B5 =>
778           if(    sectorHL = 56 ) then
779             state_next <= B56;
780           elsif( Sabc = "100" ) then
781             state_next <= AB5;
782           elsif( Sabc = "001" ) then
783             state_next <= BC5;
784           else
785             state_next <= B5;
786           end if;
787
788         -- ScX ON
789         when C5 =>
790           if(     sectorHL = 56 ) then
791             state_next <= C56;
792           elsif( Sabc = "100" ) then
793             state_next <= CA5;
794           elsif( Sabc = "010" ) then
795             state_next <= BC5;
796           else
797             state_next <= C5;
798           end if;
799
800         -- transition AB5
801         when AB5 =>
802           if(     Sabc = "100" ) then
803             state_next <= A5;
804           elsif( Sabc = "010" ) then
805             state_next <= B5;
806           elsif( Sabc = "001" ) then
807             state_next <= A5;
808           else
809             state_next <= AB5;
810           end if;
811
812         -- transition BC5
813         when BC5 =>
814           if(     Sabc = "010" ) then
815             state_next <= B5;
816           elsif( Sabc = "001" ) then
817             state_next <= C5;
818           elsif( Sabc = "100" ) then
819             state_next <= B5;
820           else
821             state_next <= BC5;
822           end if;
823
824         -- transition CA5
825         when CA5 =>
826           if(     Sabc = "100" ) then
827             state_next <= A5;
828           elsif( Sabc = "001" ) then
829             state_next <= C5;
830           elsif( Sabc = "010" ) then
831             state_next <= A5;
832           else
833             state_next <= CA5;
```

```
834         end if;
835
836       --#### SECTOR V-VI (56) H-type interval ####
837
838       --  SaX ON
839       when A56 =>
840         if(     sectorHL = 6 ) then
841           state_next <= A6;
842         elsif( Sabc = "010" ) then
843           state_next <= AB56;
844         elsif( Sabc = "001" ) then
845           state_next <= AB56;
846         else
847           state_next <= A56;
848         end if;
849
850       --  SbX ON
851       when B56 =>
852         if(     sectorHL = 6 ) then
853           state_next <= B6;
854         elsif( Sabc = "100" ) then
855           state_next <= AB56;
856         elsif( Sabc = "001" ) then
857           state_next <= BC56;
858         else
859           state_next <= B56;
860         end if;
861
862       --  ScX ON
863       when C56 =>
864         if(     sectorHL = 6 ) then
865           state_next <= C6;
866         elsif( Sabc = "100" ) then
867           state_next <= BC56;
868         elsif( Sabc = "010" ) then
869           state_next <= BC56;
870         else
871           state_next <= C56;
872         end if;
873
874       --  transition AB56
875       when AB56 =>
876         if(     Sabc = "100" ) then
877           state_next <= A56;
878         elsif( Sabc = "010" ) then
879           state_next <= B56;
880         elsif( Sabc = "001" ) then
881           state_next <= CA56;
882         else
883           state_next <= AB56;
884         end if;
885
886       --  transition BC56
887       when BC56 =>
888         if(     Sabc = "100" ) then
889           state_next <= CA56;
890         elsif( Sabc = "010" ) then
```

```
891             state_next <= B56;
892           elsif( Sabc = "001" ) then
893             state_next <= C56;
894           else
895             state_next <= BC56;
896           end if;
897
898         -- transition CA56
899         when CA56 =>
900           if(     Sabc = "100" ) then
901             state_next <= AB56;
902           elsif( Sabc = "001" ) then
903             state_next <= BC56;
904           elsif( Sabc = "010" ) then
905             state_next <= AB56;
906           else
907             state_next <= CA56;
908           end if;
909
910         --#### SECTOR VI (6) L-type interval ####
911
912         -- SaX ON
913         when A6 =>
914           if(    sectorHL = 61 ) then
915             state_next <= A61;
916           elsif( Sabc = "010" ) then
917             state_next <= AB6;
918           elsif( Sabc = "001" ) then
919             state_next <= CA6;
920           else
921             state_next <= A6;
922           end if;
923
924         -- SbX ON
925         when B6 =>
926           if(    sectorHL = 61 ) then
927             state_next <= B61;
928           elsif( Sabc = "100" ) then
929             state_next <= AB6;
930           elsif( Sabc = "001" ) then
931             state_next <= BC6;
932           else
933             state_next <= B6;
934           end if;
935
936         -- ScX ON
937         when C6 =>
938           if(     sectorHL = 61 ) then
939             state_next <= C61;
940           elsif( Sabc = "100" ) then
941             state_next <= CA6;
942           elsif( Sabc = "010" ) then
943             state_next <= BC6;
944           else
945             state_next <= C6;
946           end if;
947
```

```
948         --  transition AB6
949         when AB6 =>
950           if(     Sabc = "100" ) then
951             state_next <= A6;
952           elsif( Sabc = "010" ) then
953             state_next <= B6;
954           elsif( Sabc = "001" ) then
955             state_next <= A6;
956           else
957             state_next <= AB6;
958           end if;
959
960         --  transition BC6
961         when BC6 =>
962           if(     Sabc = "010" ) then
963             state_next <= B6;
964           elsif( Sabc = "001" ) then
965             state_next <= C6;
966           elsif( Sabc = "100" ) then
967             state_next <= C6;
968           else
969             state_next <= BC6;
970           end if;
971
972         --  transition CA6
973         when CA6 =>
974           if(     Sabc = "100" ) then
975             state_next <= A6;
976           elsif( Sabc = "001" ) then
977             state_next <= C6;
978           elsif( Sabc = "010" ) then
979             state_next <= C6;
980           else
981             state_next <= CA6;
982           end if;
983
984         --#### SECTOR VI-I (61) L-type interval ####
985
986         --  SaX ON
987         when A61 =>
988           if(     sectorHL = 1 ) then
989             state_next <= A1;
990           elsif( Sabc = "010" ) then
991             state_next <= AB61;
992           elsif( Sabc = "001" ) then
993             state_next <= CA61;
994           else
995             state_next <= A61;
996           end if;
997
998         --  SbX ON
999         when B61 =>
1000          if(     sectorHL = 1 ) then
1001            state_next <= B1;
1002          elsif( Sabc = "100" ) then
1003            state_next <= AB61;
1004          elsif( Sabc = "001" ) then
```

```
1005            state_next <= AB61;
1006          else
1007            state_next <= B61;
1008          end if;
1009
1010        -- ScX ON
1011        when C61 =>
1012          if(     sectorHL = 1 ) then
1013            state_next <= C1;
1014          elsif( Sabc = "100" ) then
1015            state_next <= CA61;
1016          elsif( Sabc = "010" ) then
1017            state_next <= CA61;
1018          else
1019            state_next <= C61;
1020          end if;
1021
1022        -- transition AB61
1023        when AB61 =>
1024          if(     Sabc = "100" ) then
1025            state_next <= A61;
1026          elsif( Sabc = "010" ) then
1027            state_next <= B61;
1028          elsif( Sabc = "001" ) then
1029            state_next <= BC61;
1030          else
1031            state_next <= AB61;
1032          end if;
1033
1034        -- transition BC61
1035        when BC61 =>
1036          if(     Sabc = "010" ) then
1037            state_next <= AB61;
1038          elsif( Sabc = "001" ) then
1039            state_next <= CA61;
1040          elsif( Sabc = "100" ) then
1041            state_next <= CA61;
1042          else
1043            state_next <= BC61;
1044          end if;
1045
1046        -- transition CA61
1047        when CA61 =>
1048          if(     Sabc = "100" ) then
1049            state_next <= A61;
1050          elsif( Sabc = "010" ) then
1051            state_next <= BC61;
1052          elsif( Sabc = "001" ) then
1053            state_next <= C61;
1054          else
1055            state_next <= CA61;
1056          end if;
1057
1058      end case;
1059
1060    end process;
1061
```

```
1062  -- Update the outputs ( SaX1 <=> SaAf | SaX2 <=> SaAr )
1063  process(state_reg)
1064  begin
1065
1066    case state_reg is
1067
1068      --  stop state
1069      when stop =>
1070        SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '0';
1071
1072      --#### Main Switching States of SECTOR I (1) H-type interval ####
1073      when A1 =>
1074        SaX1 <= '1'; SaX2 <= '1'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '1'; ScX2 <= '0';
1075      when B1 =>
1076        SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '1'; SbX2 <= '1'; ScX1 <= '1'; ScX2 <= '0';
1077      when C1 =>
1078        SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '1'; ScX2 <= '1';
1079
1080      --#### Commutation Switching States of SECTOR I (1) H-type interval ####
1081      when AB1 =>
1082        SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '1'; ScX2 <= '0';
1083      when BC1 =>
1084        SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '1'; ScX2 <= '0';
1085      when CA1 =>
1086        SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '1'; ScX2 <= '0';
1087
1088
1089      --#### Main Switching States of SECTOR I-II (12) H-type interval ####
1090      when A12 =>
1091        SaX1 <= '1'; SaX2 <= '1'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '1'; ScX2 <= '0';
1092      when B12 =>
1093        SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '1'; SbX2 <= '1'; ScX1 <= '1'; ScX2 <= '0';
1094      when C12 =>
1095        SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '1'; ScX2 <= '1';
1096
1097      --#### Commutation Switching States of SECTOR I-II (12) H-type interval ####
1098      when AB12 =>
1099        SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '1'; ScX2 <= '0';
1100      when BC12 =>
1101        SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '1'; ScX2 <= '0';
1102      when CA12 =>
1103        SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '1'; ScX2 <= '0';
1104
1105
1106      --#### Main Switching States of SECTOR II (2) L-type interval ####
1107      when A2 =>
1108        SaX1 <= '1'; SaX2 <= '1'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '1'; ScX2 <= '0';
1109      when B2 =>
1110        SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '1'; SbX2 <= '1'; ScX1 <= '1'; ScX2 <= '0';
1111      when C2 =>
1112        SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '1'; ScX2 <= '1';
1113
1114      --#### Commutation Switching States of SECTOR II (2) L-type interval ####
1115      when AB2 =>
1116        SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '1'; ScX2 <= '0';
1117      when BC2 =>
1118        SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '1'; ScX2 <= '0';
```

```
1119        when CA2 =>
1120          SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '1'; ScX2 <= '0';
1121
1122
1123        --#### Main Switching States of SECTOR II-III (23) L-type interval ####
1124        when A23 =>
1125          SaX1 <= '1'; SaX2 <= '1'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '0'; ScX2 <= '0';
1126        when B23 =>
1127          SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '1'; SbX2 <= '1'; ScX1 <= '1'; ScX2 <= '0';
1128        when C23 =>
1129          SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '1'; ScX2 <= '1';
1130
1131        --#### Commutation Switching States of SECTOR II-III (23) L-type interval ####
1132        when AB23 =>
1133          SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '0'; ScX2 <= '0';
1134        when BC23 =>
1135          SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '1'; ScX2 <= '0';
1136        when CA23 =>
1137          SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '1'; ScX2 <= '0';
1138
1139
1140        --#### Main Switching States of SECTOR III (3) H-type interval ####
1141        when A3 =>
1142          SaX1 <= '1'; SaX2 <= '1'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '0'; ScX2 <= '1';
1143        when B3 =>
1144          SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '1'; SbX2 <= '1'; ScX1 <= '1'; ScX2 <= '0';
1145        when C3 =>
1146          SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '1'; ScX2 <= '1';
1147
1148        --#### Commutation Switching States of SECTOR III (3) H-type interval ####
1149        when AB3 =>
1150          SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '0'; ScX2 <= '0';
1151        when BC3 =>
1152          SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '1'; ScX2 <= '0';
1153        when CA3 =>
1154          SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '0'; ScX2 <= '1';
1155
1156
1157        --#### Main Switching States of SECTOR III-IV (34) H-type interval ####
1158        when A34 =>
1159          SaX1 <= '1'; SaX2 <= '1'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '0'; ScX2 <= '1';
1160        when B34 =>
1161          SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '1'; SbX2 <= '1'; ScX1 <= '0'; ScX2 <= '0';
1162        when C34 =>
1163          SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '1'; ScX2 <= '1';
1164
1165        --#### Commutation Switching States of SECTOR III-IV (34) H-type interval ####
1166        when AB34 =>
1167          SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '0'; ScX2 <= '0';
1168        when BC34 =>
1169          SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '0'; ScX2 <= '1';
1170        when CA34 =>
1171          SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '1';
1172
1173
1174        --#### Main Switching States of SECTOR IV (4) L-type interval ####
1175        when A4 =>
```

```
1176          SaX1 <= '1'; SaX2 <= '1'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '0'; ScX2 <= '1';
1177        when B4 =>
1178          SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '1'; SbX2 <= '1'; ScX1 <= '0'; ScX2 <= '1';
1179        when C4 =>
1180          SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '1'; ScX2 <= '1';
1181
1182        --#### Commutation Switching States of SECTOR IV (4) L-type interval ####
1183        when AB4 =>
1184          SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '0'; ScX2 <= '1';
1185        when BC4 =>
1186          SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '1';
1187        when CA4 =>
1188          SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '1';
1189
1190
1191        --#### Main Switching States of SECTOR IV-V (45) L-type interval ####
1192        when A45 =>
1193          SaX1 <= '1'; SaX2 <= '1'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '1';
1194        when B45 =>
1195          SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '1'; SbX2 <= '1'; ScX1 <= '0'; ScX2 <= '1';
1196        when C45 =>
1197          SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '1'; ScX2 <= '1';
1198
1199        --#### Commutation Switching States of SECTOR IV-V (45) L-type interval ####
1200        when AB45 =>
1201          SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '1';
1202        when BC45 =>
1203          SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '1';
1204        when CA45 =>
1205          SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '1';
1206
1207
1208        --#### Main Switching States of SECTOR V (5) H-type interval ####
1209        when A5 =>
1210          SaX1 <= '1'; SaX2 <= '1'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '1';
1211        when B5 =>
1212          SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '1'; SbX2 <= '1'; ScX1 <= '0'; ScX2 <= '1';
1213        when C5 =>
1214          SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '1'; ScX2 <= '1';
1215
1216        --#### Commutation Switching States of SECTOR V (5) H-type interval ####
1217        when AB5 =>
1218          SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '1';
1219        when BC5 =>
1220          SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '1';
1221        when CA5 =>
1222          SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '1';
1223
1224
1225        --#### Main Switching States of SECTOR V-VI (56) H-type interval ####
1226        when A56 =>
1227          SaX1 <= '1'; SaX2 <= '1'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '0';
1228        when B56 =>
1229          SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '1'; SbX2 <= '1'; ScX1 <= '0'; ScX2 <= '1';
1230        when C56 =>
1231          SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '1'; ScX2 <= '1';
1232
```

```
1233        --#### Commutation Switching States of SECTOR V-VI (56) H-type interval ####
1234        when AB56 =>
1235          SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '0';
1236        when BC56 =>
1237          SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '1';
1238        when CA56 =>
1239          SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '1';
1240
1241
1242        --#### Main Switching States of SECTOR VI (6) L-type interval ####
1243        when A6 =>
1244          SaX1 <= '1'; SaX2 <= '1'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '1'; ScX2 <= '0';
1245        when B6 =>
1246          SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '1'; SbX2 <= '1'; ScX1 <= '0'; ScX2 <= '1';
1247        when C6 =>
1248          SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '1'; ScX2 <= '1';
1249
1250        --#### Commutation Switching States of SECTOR VI (6) L-type interval ####
1251        when AB6 =>
1252          SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '0';
1253        when BC6 =>
1254          SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '1';
1255        when CA6 =>
1256          SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '1'; ScX2 <= '0';
1257
1258
1259        --#### Main Switching States of SECTOR VI-I (61) L-type interval ####
1260        when A61 =>
1261          SaX1 <= '1'; SaX2 <= '1'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '1'; ScX2 <= '0';
1262        when B61 =>
1263          SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '1'; SbX2 <= '1'; ScX1 <= '0'; ScX2 <= '0';
1264        when C61 =>
1265          SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '1'; ScX2 <= '1';
1266
1267        --#### Commutation Switching States of SECTOR VI-I (61) L-type interval ####
1268        when AB61 =>
1269          SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '0';
1270        when BC61 =>
1271          SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '1'; ScX2 <= '0';
1272        when CA61 =>
1273          SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '1'; ScX2 <= '0';
1274
1275      end case;
1276
1277    end process;
1278
1279 end moore;
```

Appendix D

Four-step CBC strategy: source code

The source code developed during this work for the four-step current-base commutation strategy is reproduced bellow. This VHDL code was tested and validated in the MachXO2 FPGA LCMXO2-7000HE-4TG144C from Lattice.

```
1  --##############################################################################
2  -- AUTHOR:      Diogo Varajao
3  -- CONTACT:     diogo.varajao@ieee.com
4  -- LOCAL:       INESC TEC, Porto, PORTUGAL
5  -- CREATED:     June 2016
6  -- VERSION:     1.6
7  --##############################################################################
8
9  LIBRARY ieee;
10 USE ieee.std_logic_1164.all;
11 USE ieee.numeric_std.all;
12
13 entity MC_4step is
14   Port(
15     clk_tc     : in std_logic; -- clock for state transition
16     nreset     : in std_logic; -- active low reset
17     CS         : in std_logic; -- current direction (CS=1 -> i>0)
18     SaX        : in std_logic;
19     SbX        : in std_logic;
20     ScX        : in std_logic;
21     SaX2       : out std_logic;
22     SaX1       : out std_logic;
23     SbX2       : out std_logic;
24     SbX1       : out std_logic;
25     ScX2       : out std_logic;
26     ScX1       : out std_logic
27     );
28 end MC_4step;
29
30 architecture moore of MC_4step is
31
32    type state_type is (stop, A1, B2, C3, AB4, AB10, AB6, AB5, AB11, AB7, BA4,
33                        BA10, BA6, BA5, BA11, BA7, AC4, AC14, AC8, AC5, AC15, AC9,
34                        CA8, CA14, CA4, CA9, CA15, CA5, BC6, BC12, BC8, BC7, BC13,
35                        BC9, CB8, CB12, CB6, CB9, CB13, CB7);
```

```
36
37   signal state_reg, state_next  : state_type;
38
39   signal Sabc : std_logic_vector(2 downto 0);   -- switching signals (sampled)
40   signal CSd : std_logic;                       -- current direction (sampled)
41
42 begin
43
44   -- STATE UPDATE AND TIMING WITH ASYNCH ACTIVE LOW RESET
45   process(clk_tc, nreset)
46   begin
47     if(nreset = '0') then
48       state_reg <= stop;
49     elsif(rising_edge(clk_tc)) then
50       state_reg <= state_next;
51       Sabc <= SaX & SbX & ScX;
52       CSd <= CS;
53     end if;
54   end process;
55
56   -- CONTROL LOGIC STATE MACHINE
57   process(state_reg, Sabc, CSd)
58   begin
59
60     -- default conditions
61     state_next <= state_reg;
62
63     case state_reg is
64
65       --  stop state
66       when stop =>
67         if( Sabc = "100" ) then
68           state_next <= A1;
69         elsif( Sabc = "010" ) then
70           state_next <= B2;
71         elsif( Sabc = "001" ) then
72           state_next <= C3;
73         else
74           state_next <= state_reg;
75         end if;
76
77       --  SaX ON
78       when A1 =>
79         if( (Sabc = "010") and (CSd = '1') ) then
80           state_next <= AB4;
81         elsif( (Sabc = "010") and (CSd = '0') ) then
82           state_next <= AB5;
83         elsif( (Sabc = "001") and (CSd = '1') ) then
84           state_next <= AC4;
85         elsif( (Sabc = "001") and (CSd = '0') ) then
86           state_next <= AC5;
87         else
88           state_next <= state_reg;
89         end if;
90
91       --  SbX ON
92       when B2 =>
```

```
93          if( (Sabc = "100") and (CSd = '1') ) then
94            state_next <= BA6;
95          elsif( (Sabc = "100") and (CSd = '0') ) then
96            state_next <= BA7;
97          elsif( (Sabc = "001") and (CSd = '1') ) then
98            state_next <= BC6;
99          elsif( (Sabc = "001") and (CSd = '0') ) then
100           state_next <= BC7;
101         else
102           state_next <= state_reg;
103         end if;
104
105       -- ScX ON
106       when C3 =>
107         if( (Sabc = "100") and (CSd = '1') ) then
108           state_next <= CA8;
109         elsif( (Sabc = "100") and (CSd = '0') ) then
110           state_next <= CA9;
111         elsif( (Sabc = "010") and (CSd = '1') ) then
112           state_next <= CB8;
113         elsif( (Sabc = "010") and (CSd = '0') ) then
114           state_next <= CB9;
115         else
116           state_next <= state_reg;
117         end if;
118
119       -- transition from SaX to SbX with CS=1
120       when AB4 =>
121         state_next <= AB10;
122
123       when AB10 =>
124         state_next <= AB6;
125
126       when AB6 =>
127         state_next <= B2;
128
129       -- transition from SaX to SbX with CS=0
130       when AB5 =>
131         state_next <= AB11;
132
133       when AB11 =>
134         state_next <= AB7;
135
136       when AB7 =>
137         state_next <= B2;
138
139       -- transition from SbX to SaX with CS=1
140       when BA6 =>
141         state_next <= BA10;
142
143       when BA10 =>
144         state_next <= BA4;
145
146       when BA4 =>
147         state_next <= A1;
148
149       -- transition from SbX to SaX with CS=0
```

```
150         when BA7 =>
151           state_next <= BA11;
152
153         when BA11 =>
154           state_next <= BA5;
155
156         when BA5 =>
157           state_next <= A1;
158
159         -- transition from SaX to ScX with CS=1
160         when AC4 =>
161           state_next <= AC14;
162
163         when AC14 =>
164           state_next <= AC8;
165
166         when AC8 =>
167           state_next <= C3;
168
169         -- transition from SaX to ScX with CS=0
170         when AC5 =>
171           state_next <= AC15;
172
173         when AC15 =>
174           state_next <= AC9;
175
176         when AC9 =>
177           state_next <= C3;
178
179         -- transition from ScX to SaX with CS=1
180         when CA8 =>
181           state_next <= CA14;
182
183         when CA14 =>
184           state_next <= CA4;
185
186         when CA4 =>
187           state_next <= A1;
188
189         -- transition from ScX to SaX with CS=0
190         when CA9 =>
191           state_next <= CA15;
192
193         when CA15 =>
194           state_next <= CA5;
195
196         when CA5 =>
197           state_next <= A1;
198
199         -- transition from SbX to ScX with CS=1
200         when BC6 =>
201           state_next <= BC12;
202
203         when BC12 =>
204           state_next <= BC8;
205
206         when BC8 =>
```

```
207         state_next <= C3;
208
209       -- transition from SbX to ScX with CS=0
210       when BC7 =>
211         state_next <= BC13;
212
213       when BC13 =>
214         state_next <= BC9;
215
216       when BC9 =>
217         state_next <= C3;
218
219       -- transition from ScX to SbX with CS=1
220       when CB8 =>
221         state_next <= CB12;
222
223       when CB12 =>
224         state_next <= CB6;
225
226       when CB6 =>
227         state_next <= B2;
228
229       -- transition from ScX to SbX with CS=0
230       when CB9 =>
231         state_next <= CB13;
232
233       when CB13 =>
234         state_next <= CB7;
235
236       when CB7 =>
237         state_next <= B2;
238
239     end case;
240
241   end process;
242
243   -- Update the outputs
244   process(state_reg)
245   begin
246
247     case state_reg is
248
249       -- stop state
250       when stop =>
251         SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '0';
252
253       -- SaX ON
254       when A1 =>
255         SaX1 <= '1'; SaX2 <= '1'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '0';
256
257       -- SbX ON
258       when B2 =>
259         SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '1'; SbX2 <= '1'; ScX1 <= '0'; ScX2 <= '0';
260
261       -- ScX ON
262       when C3 =>
263         SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '1'; ScX2 <= '1';
```

```
264
265         -- transition from SaX to SbX with CS=1
266         when AB4 =>
267           SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '0';
268         when AB10 =>
269           SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '0';
270         when AB6 =>
271           SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '0';
272
273         -- transition from SaX to SbX with CS=0
274         when AB5 =>
275           SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '0';
276         when AB11 =>
277           SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '0'; ScX2 <= '0';
278         when AB7 =>
279           SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '0'; ScX2 <= '0';
280
281         -- transition from SbX to SaX with CS=1
282         when BA6 =>
283           SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '0';
284         when BA10 =>
285           SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '0';
286         when BA4 =>
287           SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '0';
288
289         -- transition from SbX to SaX with CS=0
290         when BA7 =>
291           SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '0'; ScX2 <= '0';
292         when BA11 =>
293           SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '0'; ScX2 <= '0';
294         when BA5 =>
295           SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '0';
296
297         -- transition from SaX to ScX with CS=1
298         when AC4 =>
299           SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '0';
300         when AC14 =>
301           SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '1'; ScX2 <= '0';
302         when AC8 =>
303           SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '1'; ScX2 <= '0';
304
305         -- transition from SaX to ScX with CS=0
306         when AC5 =>
307           SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '0';
308         when AC15 =>
309           SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '1';
310         when AC9 =>
311           SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '1';
312
313         -- transition from ScX to SaX with CS=1
314         when CA8 =>
315           SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '1'; ScX2 <= '0';
316         when CA14 =>
317           SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '1'; ScX2 <= '0';
318         when CA4 =>
319           SaX1 <= '1'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '0';
320
```

```
321         -- transition from ScX to SaX with CS=0
322         when CA9 =>
323           SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '1';
324         when CA15 =>
325           SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '1';
326         when CA5 =>
327           SaX1 <= '0'; SaX2 <= '1'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '0';
328
329         -- transition from SbX to ScX with CS=1
330         when BC6 =>
331           SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '0';
332         when BC12 =>
333           SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '1'; ScX1 <= '0';
334         when BC8 =>
335           SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '1'; ScX2 <= '0';
336
337         -- transition from SbX to ScX with CS=0
338         when BC7 =>
339           SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '0'; ScX2 <= '0';
340         when BC13 =>
341           SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '0'; ScX2 <= '1';
342         when BC9 =>
343           SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '1';
344
345         -- transition from ScX to SbX with CS=1
346         when CB8 =>
347           SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '1'; ScX2 <= '0';
348         when CB12 =>
349           SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '1'; ScX2 <= '0';
350         when CB6 =>
351           SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '1'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '0';
352
353         -- transition from ScX to SbX with CS=0
354         when CB9 =>
355           SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '0'; ScX1 <= '0'; ScX2 <= '1';
356         when CB13 =>
357           SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '0'; ScX2 <= '1';
358         when CB7 =>
359           SaX1 <= '0'; SaX2 <= '0'; SbX1 <= '0'; SbX2 <= '1'; ScX1 <= '0'; ScX2 <= '0';
360
361       end case;
362
363     end process;
364
365 end moore;
```

Appendix E

Power Transformer and Link-inductor

The magnetic devices represent a significant volume and weight of the power electronics converters. By increasing the switching frequency of the converter it is possible to use inductors with less inductance and also reduce the peak flux linkage applied to the transformers. As a consequence, these magnetic devices can be made more compact. However, the change in the frequency spectrum of the current that circulates in the power transformer and the link inductor requires new design methods to achieve a minimum volume and maximum efficiency in all operating range. Several approaches for the design of a HF power transformer were proposed in [284–297]. It was found that there is not a systematic approach for the design of HF power transformers.

In this appendix, a design methodology to systematize the design process of the HF-link elements using analytic and software tools is presented. The models for characterization of the core and winding losses have been reviewed. Considerations about the practical implementation and construction of the magnetic devices are also provided. The software receives the inputs from the mathematical analysis and runs an optimization to find the best design. A 10 kW / 20 kHz transformer plus a link inductor are designed using this strategy achieving a combined efficiency of 99.32 %.

E.1 Modeling of the high-frequency link

As previously described in Chapter 3, the MC applies voltage v_p to the primary winding of the transformer and the FB impresses v_s in the HFT's secondary winding. The HFL operation requires an AC voltage with balanced positive and negative volt-seconds at the transformer terminals. Voltages applied to the transformer and the resulting current during one period of modulation, T_s, is depicted in Figure 4.4(a). The voltage difference between v_p and v_s is applied to the transformer which stores energy in its leakage inductances. Therefore, the equivalent inductance L (see equation E.1), serves as the main energy transfer element. Design a transformer with a specific leakage inductance is a very complex task. The typical design and construction methods used in power magnetics are

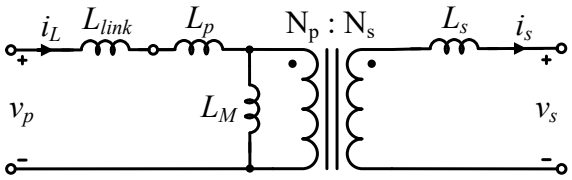


Figure E.1: Equivalent model of the high-frequency transformer.

oriented to minimize the leakage inductance instead of design a transformer with a specific leakage inductance. An alternative approach is to design the transformer with minimum leakage inductance and add an external inductor to meet the requirements for energy conversion [298]. Figure E.1 represents an equivalent model of the high-frequency link where the inductor is in series with the transformer. Note that in this work all coupling capacitances are neglected. L_p and L_s are respectively the primary and secondary side leakage inductances of the transformer. The magnetizing inductance is characterized by L_M referred to the primary side. L_{link} is the external series inductor added to the transformer for the HF-link operation. The equivalent inductance can be related with L_p, L_s, and L_{link} by:

$$L = L_{link} + L_p + \left(\frac{N_p}{N_s}\right)^2 L_s \tag{E.1}$$

where N_p and N_s are the number of turns of the primary and secondary winding, respectively.

E.2 Core loss modeling

The three main physical loss sources in a magnetic core are the hysteresis losses, eddy-current losses, and residual losses. The *B-H* characteristic of a core material, also known as the magnetization curve, represent the relation between the flux density and the magnetic field. The energy loss due to hysteresis in the *B-H* loop is directly proportional to the area inside the magnetization curve and the excitation frequency, f_c [299]. The alternating flux in the core drives electrical eddy currents to flow causing losses in the resistance of the core material. These eddy currents typically increase at least as f_c^2 and are particularly significant in HF applications [299]. Moreover, during a phase of constant flux (where the applied voltage across the magnetic component is zero) losses still occur in the core material. According to [291], these residual losses are due to relaxation processes that occur in the core.

The first empirical method to calculate core loss density, P_c, was proposed by Steinmetz [300]. Core manufacturers provide data of losses per volume that can be used to empirically extract the parameters for the Steinmetz equation. Although, these parameters are only valid for a limited frequency and flux density range [297]. Moreover, the Steinmetz equation is only valid for sinusoidal flux waveforms which is not normally found

in power electronics applications [295]. Several models have been developed in order to overcome this limitation and determine losses for a variety of waveforms. The generalized Steinmetz equation (GSE), the improved GSE (iGSE), and the improved iGSE (i^2GSE) [291] are examples of these new models. However, the impact of a DC premagnetization (HDC) is not considered in these models. In order to overcome this drawback, core loss measurements could be stored in a core material database for further use in loss calculation [301]. This database, designated by loss map, stores the loss information for different operating points according the peak-to-peak flux density, f_c, temperature, and the DC bias [302].

The GeckoMAGNETICS [269] software uses a hybrid loss modeling approach by employing the loss map and the i^2GSE model. Some loss map operating points are used to extract the Steinmetz parameters for a wide frequency and flux density range. Then, the core losses are calculated using the (i^2GSE) model that includes the relaxation effects. First, the flux density waveform is separated into its fundamental flux waveform and into piecewise linear flux waveform segments. Then, the loss energy is computed for all segments and combined to represent the total core loss. In this work, the core losses are determined using the design tool provided by the software.

E.3 Winding loss modeling

Alternating currents induce eddy currents inside the conductor and cause an irregular current distribution. This results in ohmic losses in the winding that can be separated into skin effect losses and proximity effect losses [294]. The skin effect forces the current to flow close to the conductor surface resulting in an increase of the effective resistance. The distance from the outer boundary to where the current density falls to $1/e$ of the maximum is called the skin depth δ_w and is calculated as:

$$\delta_w = \frac{1}{\sqrt{\pi \cdot \sigma \cdot f_w \cdot \mu}} \tag{E.2}$$

where f_w is the frequency of the sinusoidal current, μ and σ are the magnetic permeability and the electrical conductivity of the conductor material, respectively. For copper conductors, the relative magnetic permeability μ_r can be assumed equal to one. The proximity effect losses are due to eddy currents induced by external magnetic field H_e. For example, the air gap fringing field or the magnetic field from other conductors lead to the proximity effect. In the case of litz-wire, it is also necessary to consider the internal magnetic field H_i induced by each strand in its neighbouring strands [303].

In power electronic applications, usually the voltages and currents are not sinusoidal waveforms. One way to handle non-sinusoidal waveforms is by using Fourier analysis. The

effective frequency for a non-sinusoidal current waveform can be calculated as [285]:

$$f_{\text{eff}} = \frac{1}{2\pi}\sqrt{\frac{\sum_{j=0}^{\infty} I_j^2\omega_j^2}{\sum_{j=0}^{\infty} I_j^2}} \tag{E.3}$$

where I_j is the rms amplitude of the Fourier component at frequency ω_j. The skin depth at f_{eff} is a more realistic estimation for the magnetic design process. The effect of eddy currents can be taken in account by the ac copper loss factor, F_{ac}, calculated by [294]:

$$F_{ac} = \frac{R_{ac}}{R_{dc}} = 1 + \frac{(\pi \cdot N_0 \cdot N)^2 d_0^6}{192 \cdot \delta_w^4 \cdot c_{b2}} \tag{E.4}$$

where N is the number of turns, N_0 is the number of strands, d_0 is the diameter of the copper in each strand, and c_{b2} is breadth of the window area of the core. This factor relates dc resistance to an ac resistance which accounts for all winding losses. The dc resistance can be determined by the following:

$$R_{dc} = \frac{MLT \cdot N}{\pi \cdot \sigma \cdot r_0^2 \cdot N_0} \tag{E.5}$$

where MLT is the mean length per turn of the winding, and r_0 is the strand radius. Considering F_{ac} and R_{dc}, the winding losses can be estimated for a given sinusoidal current with rms amplitude $I_{L,nom}$ by:

$$P_w = R_{dc} \cdot F_{ac} \cdot I_{L,nom}^2. \tag{E.6}$$

E.4 Design of Power Transformer

E.4.1 Specifications

The power transfer between the matrix converter and the full-bridge can be controlled by the amplitude and phase-shift of v_p and v_p. For this analysis, it is considered that the amplitude of these voltages is constant during one period of modulation. In practice, this can be approximately achieved if the switching frequency is sufficiently higher compared to the grid frequency, f_i. V_1 and V_2 defined in Figure 4.4 are the amplitude of the switching space vectors applied by the MC. In turn, V_o is the amplitude of the output dc voltage applied by the FB. The resulting power flow from the MC to the FB over one switching period is given by:

$$P_{HFT} = \frac{3}{4}\frac{V_p V_s}{\omega_s L} n\phi\left(1 - \frac{|\phi|}{\pi}\right) \tag{E.7}$$

where ω_s is the switching frequency in radians per second, n is the transformer turns ratio, and ϕ is the phase-shift between v_p and v_s. The operation parameters for the converter and the specifications for the magnetic components that will be considered in the design process are listed in Table E.1. For this application, a 1:1 turns ratio is considered due

Table E.1: Converter parameters and magnetics target specifications.

Parameter	Value	Parameter	Value	Parameter	Value
$V_{g,ll}$	400 V	$V_{dc,nom}$	380 V	L	44 μH
f_i	50 Hz	$I_{dc,max}$	31 A	$I_{L,nom}$	45 A
P_{nom}	10 kW	f_s	20 kHz	$I_{L,pk}$	110 A
$I_{g,max}$	16 A	n	1	T_{max}	100°C

to the nominal dc voltage level. The equivalent inductance must be calculated in order to allow full power transfer to the battery pack in the worst operating conditions. Since the grid voltage can be in the ±10% range, the minimum value is selected for V_p. The dc side of the converter is supposed to support voltages in the range 320-490 V to properly charge and discharge the battery pack. Considering (E.7), the maximum value for L is calculated as 44 μH.

E.4.2 Core material and geometry

The magnetic materials typically used in power applications are classified in ferromagnetics (iron alloys) and ferrimagnetics (ferrites). The iron alloys exhibit high saturation flux density, B_{sat}, while having a low electric resistivity when compared with ferrites. Laminated cores, powder iron cores, amorphous alloys, and nanocrystalline materials are examples of iron alloys categories. The FT-3M and the 2705M are examples of ferromagnetic materials available in the market.

Ferrite cores are ceramic materials having small saturation flux density, typically in the 0.25 to 0.5 T range [299]. However, the ferrites have a high electric resistivity allowing a much smaller eddy current losses. Manganese-zinc (Mn-Zn) cores are commonly used as inductors and transformers in 10 kHz to 1 MHz frequency range. The 3F3 and the N87 are examples of ferrites available in the market. Regarding the core geometry, U and E cores are commonly used in power applications due to their capacity for being stacked, multiplying the magnetic cross section and preserving the winding cross section.

In this design the N87 material was selected, which is a low-medium frequency ferrite appropriated for the excitation frequency employed in this application. The design of a magnetic device (inductor or transformer) must ensure that the core material does not saturate, which means that the flux density must be lower than B_{sat}. Core losses produce heat which increases the operating temperature and typically reduces the B_{sat} limit. Therefore, it is necessary to do a tradeoff between saturation flux density and core loss [299]. From Faraday's law, the peak-to-peak flux density is:

$$\Delta B = \frac{\lambda_1}{2 \cdot N_p \cdot A_c} \tag{E.8}$$

where λ_1 is the flux linkage, and A_c is the effective magnetic cross section of the core. As can be concluded by this equation, a high operating flux density leads to a reduced size of the core, since A_c can be smaller. In other way, if the excitation frequency f_c is increased the flux linkage is reduced, resulting in a lower operating flux density. For the N87 ferrite material, the saturation occurs for $B_{sat} = 390$ mT at 100°C [304]. The peak flux linkage applied to the transformer primary winding is $\lambda_1 = 0.0102$ V.s. The transformer must have a minimum L_M in order to limit the peak magnetizing current. Using (E.9), $L_{M,min}$ was defined as 3 mH to ensure a peak magnetizing current lower than 5 % of $I_{L,nom}$.

$$L_{M,min} = \frac{\lambda_1}{2 \cdot I_{M,max}}. \tag{E.9}$$

E.4.3 Winding type

The more common winding types for magnetic devices are the solid round wire, rectangular wire, foil winding, and the litz-wire. Solid round wires are the most economical solutions, but its scope of application is limited to relatively low frequencies or low current windings. However, they have high skin effect and proximity effect losses that penalize efficiency. In turn, the rectangular wire allows a better fill factor, and the skin effect and proximity effect losses are decreased when compared with the solid round wire [297]. Foil winding is a particular case of a rectangular wire with a very thin layer. By making the foil thickness smaller when compared to the skin depth is possible to reduce even more the skin effect and proximity effect losses. For a high-current application, connecting multiple layers of foil in parallel is required.

A litz-wire is made of multiple individually insulated strands twisted or woven together [285]. Eddy current effects in a winding can be significantly reduced by employing litz-wire. By choosing a strand diameter inferior to the skin depth is possible to improve the performance regarding skin effect and proximity effect losses [299]. Due to the insulation and packing materials, the window area occupied by copper in a litz-wire winding will be less than the area occupied in a solid round wire of the same diameter, resulting in a higher DC resistance. Moreover, the insulation and packing materials also difficult heat dissipation contributing simultaneously for DC resistance increase.

Taking into account the employed excitation frequency and with the intent of reducing the eddy current losses, litz-wire was chosen for this application. The spectrum of i_L is represented in Figure E.2 for operation with the parameters of Table E.1. As can be seen, the main component of the current appears at the switching frequency, $f_s = 20$ kHz. Since both v_p and v_s have a double frequency pattern, a significant component is also generated at $2 \cdot f_s$. Other harmonics arise at side-bands of the base frequency and its multiples due to the phase-shift operation. From (E.3) and considering the harmonics up to 125 kHz, the effective frequency is calculated as 32.0 kHz. For an effective frequency between 20 kHz and 50 kHz, a wire gauge of 36 AWG is recommended by a litz-wire manufacture [305].

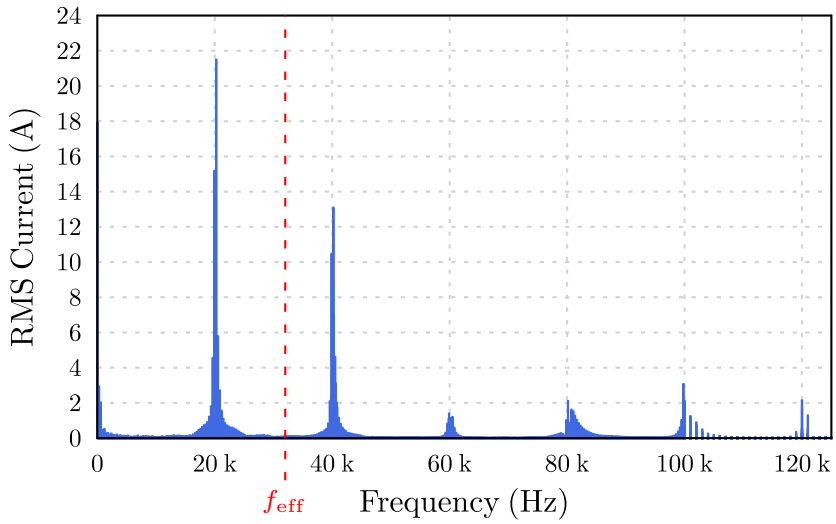


Figure E.2: Frequency spectrum of the current in the transformer primary winding.

Another work [295] establishes a more restrictive relation using the skin depth to strand radius ratio: $\delta_w/15 < r_0 < \delta_w/30$. As a compromise between both criteria it was decided to select the 41 AWG wire gauge, resulting in $\delta_{w,32kHz}/r0 \approx 10.3$. The fill factor, β_w, is a ratio between the winding cross section and the core window area, A_w, as defined in (E.10). Litz-wire has a reduced fill factor, due to serving and strand packing issues, when compared with other winding types. Values between 0.3 and 0.4 are commonly accepted for the fill factor of litz-wire windings [306]. Since the turns ratio of the HFT is unitary, an equal window distribution between primary and secondary is considered in order to reduce the cost.

$$\beta_w = \frac{N \cdot \pi \cdot r_0^2 \cdot N_0}{A_w} \tag{E.10}$$

The winding arrangement is another degree of freedom which influences winding losses. If maximum efficiency is desired, primary and secondary windings must be fully interleaved [295]. Moreover, a substantial reduction in leakage inductance is obtained by interleaving the primary and secondary windings which is a critical design factor for the HFLMC. The leakage inductance referred to the primary side for magnetically symmetric arrangement of windings can be estimated by the following [307]:

$$L_{leak} = \frac{\mu_0 \cdot MLT \cdot N^2}{p_w^2 \cdot h_w} \left(\frac{\sum d_w}{3} + \sum c_w \right) \tag{E.11}$$

where μ_0 is the absolute permeability, d_w the external diameter of the litz-wire bundle, c_w the insulation space between the windings, h_w the bobbin height, and p_w is the number of insulating interspaces between the litz-wire bundles. The flux increase due to the leakage inductance is determined by (E.12). After this calculation it must be verified if the total

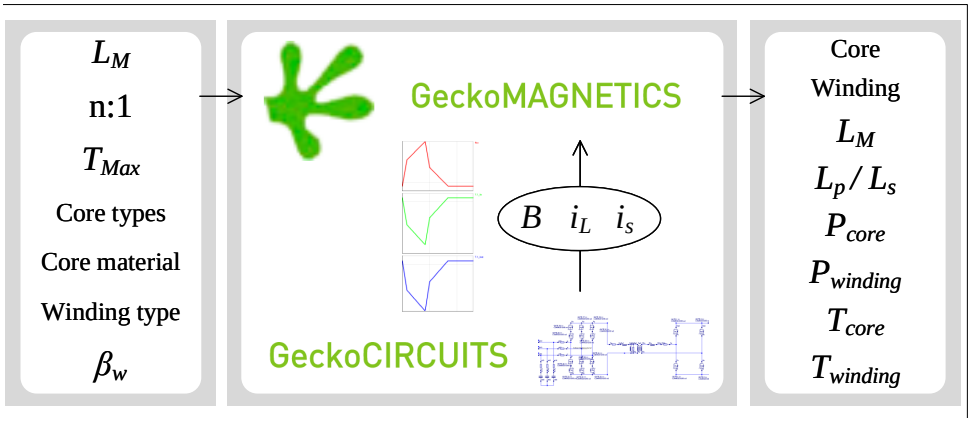


Figure E.3: Transformer design methodology.

flux density does not exceed the saturation limit.

$$\Delta B_{leak} = \frac{L_{leak} \cdot I_{L,pk}}{N_p \cdot A_c}. \tag{E.12}$$

E.4.4 Design results and verification

Recurring to its wide core and windings database, the software evaluates the possible combinations and presents the result in the conventional power-loss versus volume (P-V) plot. The designer must implement the complete electric circuit and respective command system in GeckoCIRCUITS [269] software. Subsequently, GeckoMAGNETICS receive B, i_L, and i_s from simulation in order to compute the core and winding losses for each design combination. Figure E.3 shows a flowchart with the design process employing the software bundle. The input parameters for the software are: $3 \leq L_M \leq 10$ mH, $n = 1$, $T_{max} = 100$°C, double-E cores, N87 material, litz-wire, and $0.2 \leq \beta_w \leq 0.4$. After evaluation of the possible design combinations, the software present the results in a P-V plot. The design that presented the best compromise between losses and volume is detailed in Table E.2. Regarding the magnetic circuit, 5 stacks of EE80 cores were mounted in a custom bobbin, made of Polyphenylsulfone (PPSU) supporting temperatures up to 180°C. The stacks are spaced by 2 mm to improve heat extraction from the windings. The specified peak flux density is calculated by (E.8) as 238 mT. From (E.12), the flux increase due to L_{leak} is 32.7 mT. As can be concluded, the total flux density does not exceed the 273 mT limit previously specified. A litz-wire with 1440 strands is selected which has a 5.70 mm^2 cross section. The RUPALIT Safety V155 with 3 layer mylar insulation [308] from Rudolf Pack GmbH is chosen for this application. Each winding is composed by two litz-wire bundles connected in parallel corresponding to an effective cross section $A_{cu} = 11.40$ mm^2. For the converter specifications of Table E.1, the resulting current density at nominal operation is $J_w = 3.99$ A/mm^2. The practical fill factor is calculated from (E.10) as $\beta_w = 0.28$. The mean length turn for the stacked cores is $MLT = 0.372$ m. Considering the effective

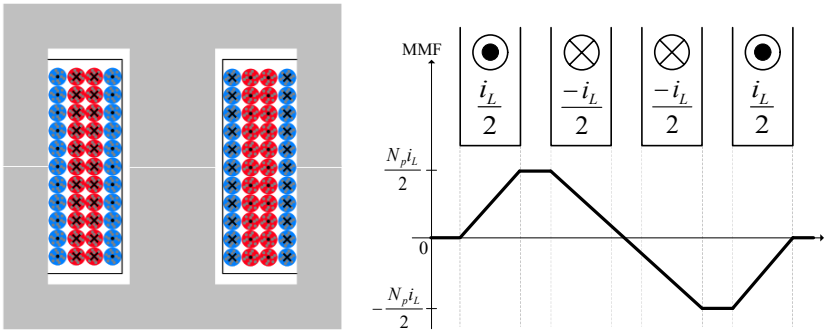
Table E.2: Design values for the power transformer.

Variable	**Design value**
Core	5 × EE80/38/20
Core material	N87
Effective magnetic cross section	1950 mm^2
Specified peak flux density	238 mT
Air gap (l_g)	0 mm
Distance between stacks	2 mm
Number of Turns (N_p : N_s)	11 : 11
Litz-wire ($N_0 \times d_0$)	1440 × 71 μm
Winding arrangement	2 litz-wire bundles in parallel
Interleaving of the windings	2/1 vertical interleaved
Magnetizing inductance (L_M)	3.55 mH
Leakage inductances (L_p / L_s)	3.19 μH / 3.19 μH
DC Resistance (R_{dc})	6.9 mΩ
Dimensions	80.0 × 77.0 × 143.5 mm
Boxed Volume	0.884 dm^3

cross section and the number of turns, the dc resistance of each winding at 100°C is $R_{dc} = 6.9$ mΩ. By (E.4) the ac copper loss factor at f_{eff} is $F_{ac} = 1.035$. Taking in account these results, from (E.6) the estimated winding losses of each winding is $P_{w,\text{hft}} = 14.9$ W which is very close to the 15.1 W calculated by the software. This difference is related to some minor aspects that are neglected by the F_{ac} factor.

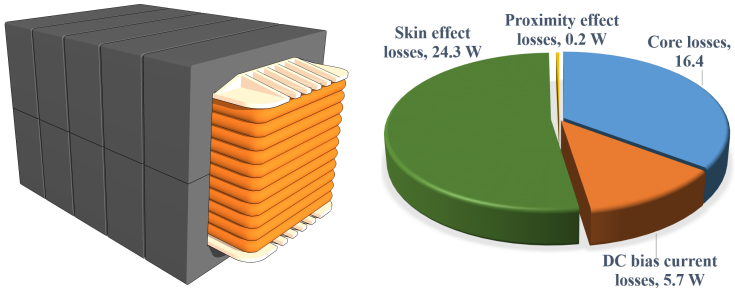
Figure E.4(a) shows the winding arrangement where it is clear the interleaving of the secondary winding inside the primary winding. The proximity effect losses are proportional to the square of the magnetic flux (MMF) in the winding. Figure E.4(b) depicts the MMF for this transformer. Since the interleaving strategy reduces the MMF peak by half, the proximity effect losses are reduced by a factor of four. Simultaneously, from (E.11) can be concluded that the leakage inductance has one-fourth of the value of the simple winding arrangement.

A 3D CAD model of the transformer is represented in Figure E.5(a). This is a compact design and achieves a power density of 11.3 kW/dm^3. The power loss distribution between core and windings is depicted in Figure E.5(b). Winding losses are divided into proximity effect losses, skin effect losses and dc bias current. The total losses of this design are 46.6 W corresponding to an efficiency of 99.53 %. A photo of the constructed transformer is depicted in Figure E.5(c).



(a) (b)

Figure E.4: (a) Cut of the transformer with the winding arrangement. (b) MMF distribution versus position of the interleaved windings inside the core window.



(a) (b)

Figure E.5: Power Transformer. (a) 3D CAD model. (b) Core and winding losses distribution.

E.5 Design of Link Inductor

The additional inductance required for the HF-link operation must be provided by the link inductor. The projected transformer has a total leakage inductance of 6.4 μH. Thus, from (E.1) the link inductor must be designed to have at least 37.6 μH at $i_{L,pk}$. Since the inductance varies with the current and the temperature, the link inductor is designed with a nominal value of $L_{nom} = 40\,\mu$H. Since this inductor will conduct the same current as the transformer and will have equal excitation frequency, the 41 AWG litz-wire is selected for the conductor. For practical reasons, the design is restricted to the same number of strands. Regarding the core, double-E and ELP cores are preferred in order to provide a compact inductor. The flowchart for inductor design methodology is very similar to the one in Figure E.3. The input parameters for the software are: $L_{nom} = 40\,\mu$H, $L_{link} \geq 0.90 \cdot L_{nom}$ at $i_{L,pk}$, $T_{max} = 100°$C, double-E and ELP cores, N87 material, and 1440 $\times$ 71 μm litz-wire. The P-V plot provided by the software after the optimization is depicted in Figure E.6. As can be seen, the space of results is large considering the volume and power losses range. The selected design is marked in this plot and the respective design values are listed in Table E.3.

Regarding the magnetic circuit, 2 stacks of EE70 cores can be mounted in the available commercial bobbin. The stacks are spaced by 1 mm to improve heat extraction from the

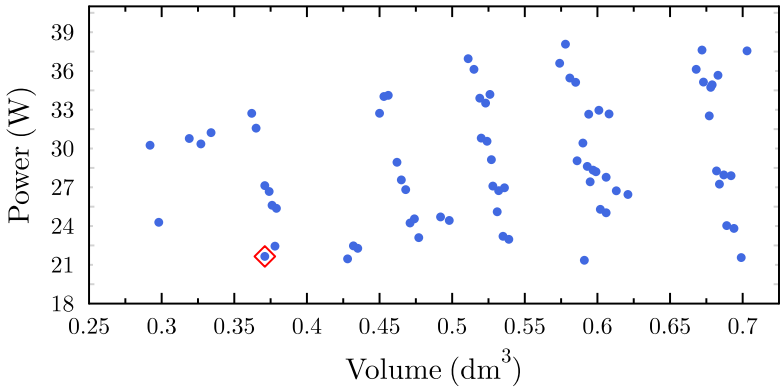
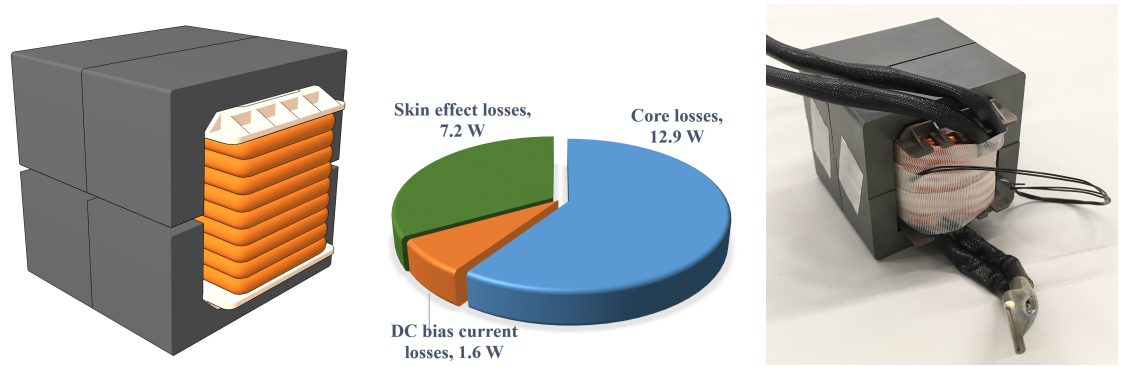


Figure E.6: P-V plot of the link inductor design.

Table E.3: Design values for the link inductor.

Variable	**Design value**
Core	2 × EE70/33/32
Core material	N87
Effective magnetic cross section	1366 mm^2
Specified peak flux density	360 mT
Air gap (l_g)	5.6 mm
Distance between stacks	1 mm
Number of Turns (N)	9
Litz-wire ($N_0 \times d_0$)	1440 × 71 μm
Winding arrangement	2 litz-wire bundles in parallel
Inductance (L_{link})	40.2 μH
DC Resistance (R_{dc})	3.9 mΩ
Dimensions	70.5 × 68.8 × 82.0 mm
Boxed Volume	0.398 dm^3

windings. An air gap of 5.6 mm is necessary to increase the reluctance and prevent core saturation. The obtained inductance at peak current is $L_{link,pk} = 38.1\,\mu$H. The peak flux density is calculated as $\hat{B}_{max} = 360$ mT which has a smaller margin for the limit of the N87 ferrite material. However, the selected design is accepted since the core temperature is 73°C. The winding is composed by two litz-wire bundles connected in parallel, resulting in a current density at nominal operation of $J_w = 3.99$ A/mm^2. The practical fill factor is calculated from (E.10) as $\beta_w = 0.22$. The mean length turn for the stacked cores is $MLT = 0.251$ m. Considering the effective cross section and the number of turns, the dc resistance of each winding at 100°C is $R_{dc} = 3.84$ mΩ. By (E.4) the ac copper loss factor



(a) (b) (c)

Figure E.7: Link Inductor. (a) 3D CAD model. (b) Core and winding losses distribution. (c) Photo of the constructed link inductor.

at f_{eff} is $F_{ac} = 1.041$. Taking into account these results, from (E.6) the winding losses are estimated as $P_{w,\text{link}} = 8.3$ W which is also very close to the 8.8 W calculated by the software.

A 3D CAD model of the link inductor is represented in Figure E.7(a). This design achieves a power density of 25.1 kW/dm^3. The power loss distribution between core and winding is depicted in Figure E.7(b). Winding losses are divided into skin effect losses and dc bias current. The proximity effect losses are negligible. The total losses of this design are 21.6 W corresponding to an efficiency of 99.78 %. A photo of the constructed link-inductor is depicted in Figure E.7(c).

E.6 Conclusion

An approach to design the transformer and the link inductor for the HFLMC has been presented in this appendix. The models for the core and winding losses characterization have been reviewed and selected to guide the design. Core geometry and materials are compared as also the different conductor types. The most appropriate options for this specific application are discussed and selected. The best result from the optimization process is selected and validated using the previously presented models. This design process was a challenging task since the beginning when having in mind the non-conventional waveform of the applied voltage. The worst-case scenario is taken always into account resulting in robust magnetic components. The high currents circulating in the windings require the use of high gauge wires which in this case is litz to avoid excessive losses. The EE80 core is a good option to accomodate this large windings since it has a large winding area/magnetic area ratio. This ratio is much lower in the EE70 cores, which benefits the inductance factor, being much more adequate for inductors. A 10 kW / 20 kHz transformer plus a link inductor are designed using this strategy. The final results of the set designed are impressive, achieving a combined efficiency at full load of 99.32 %.

Appendix F

DC Filter

The current flowing to the battery pack should have very low ripple in order to do not perturb the BMS operation, avoid internal heating of the cells, and extend battery life [309–311]. Current at the DC side of the FB has significant ripple due to the high-frequency link operation. Therefore, a DC filter should be connected between the FB and the battery pack in order to attenuate the unwanted ripple components present in i_o.

F.1 Spectrum of the converter output current

The output current can be obtained by simulating the converter operation without any DC filter at nominal conditions: $P_{nom} = 10$ kW, line-to-neutral grid voltage $V_{g,ln} = 230$ V, grid frequency $f_g = 50$ Hz and output voltage $V_{dc} = 380$ V. A simulation model of the HFLMC was implemented in GeckoCIRCUITS as described in Section 4.4. Fig. F.1 shows the spectrum of the FB output current, $I_o(j\omega)$, obtained from simulation. As expected, the main component of the output current is DC. However, other components appear at the switching frequency, $f_s = 20$ kHz, and at frequencies multiple of f_s.

F.2 Required attenuation

The required attenuation for the DC filter can be estimated by comparing the highest harmonic with the DC component of the output current. In this case, the highest harmonic appears at the switching frequency with a magnitude of 19.9 A, while the DC component reaches 26.2 A. Considering an admissible ripple of 2 % for the highest component, the maximum harmonic current would be 0.398 A. Thus, an attenuation of 36.4 dB should be provided by the DC filter.

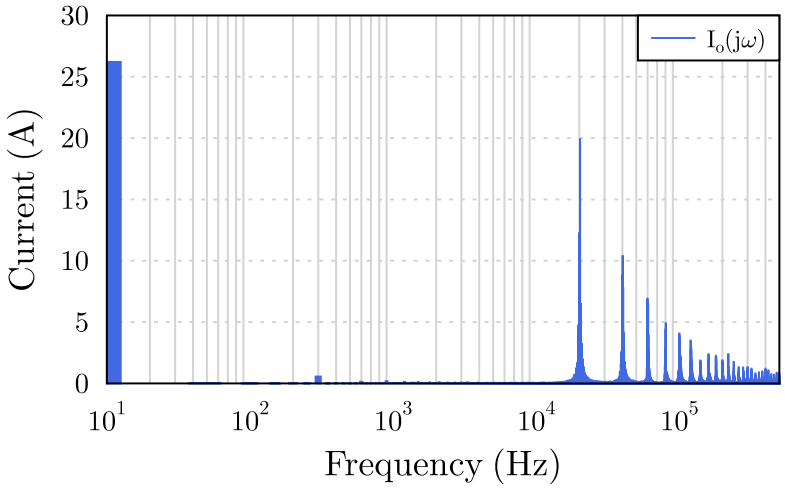


Figure F.1: Frequency spectrum of the converter output current $I_o(j\omega)$ (RMS values).

F.3 Topology and Components

In theory, there are a large number of filter topologies that can be employed for DC filtering [312, 313]. Although, a low number of topologies are used due to cost and complexity reasons. The third-order CLC circuit, also known as PI filter, is a very common topology employed as the FB output filter to do the interface with a battery pack. The equivalent circuit of the DC filter is represented in Figure F.2. R_o represents the DC resistance of the high current inductor.

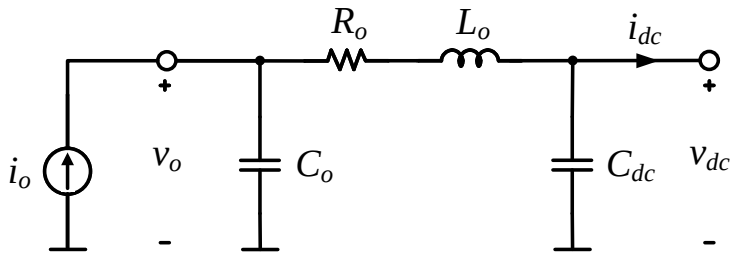


Figure F.2: Equivalent circuit of the DC filter.

In order to obtain a high impedance mismatch, C_{dc} capacitor at the battery side is significantly lower compared with C_o. Thus, this filter can be approximated by a second-order LC circuit in order to simplify the design process. Transfer function $H_{crl}(s)$ which relates $I_{dc}(s)$ with $I_o(s)$ is defined in (F.1). The magnitude of $H_{crl}(s)$ characterizes the attenuation capability of this single-stage LC filter.

$$H_{crl}(s) = \frac{1}{s^2 L_o C_o + s R_o Co + 1} \tag{F.1}$$

The resonance frequency of this filter can be determined using the following relation:

$$f_0 = \frac{1}{2\pi\sqrt{L_o C_o}}. \tag{F.2}$$

The full-bridge is a voltage-fed topology and behaves as a current source at its DC side. Capacitor C_o is placed at the DC side of the FB in order to limit the voltage ripple and ensure a correct system operation. From the simulations, the RMS current provided by this capacitor reaches 31.9 A in the worst operating conditions. Therefore, the capacitance needs to be higher than 83.9 μF to ensure a maximum 5 % voltage ripple. Due to the discrete availability of capacitance values and also for practical implementation reasons, capacitor C_o is selected to 90 μF.

The DC filter should provide 36.4 dB attenuation, which by the following:

$$f_0 = \frac{20kHz}{\sqrt{10^{\frac{Att_{DC}}{20}}}} \tag{F.3}$$

results in $f_0 = 2466$ Hz. Considering C_o and (F.2), L_o is calculated as 46.3 μH.

Table F.1 lists all the components for the DC filter. C_o is implemented with three 30 μF MKP capacitors mounted in parallel with a total 42 Arms current capability. Regarding L_o, there are not much commercial inductors available in the market with this current rating. As a compromise, one 60 μH inductor with 28 A rated current capability was selected. The inductance at 31 A (see Table 1.4) is still above 46.3 μH, allowing compliance with the filter specification. For operation at partial load, the resulting attenuation will be higher which is beneficial to reduce the current ripple. The DC resistance of the high current inductor, R_o, is then 8.5 mΩ. For the C_{dc} at the battery connection, one 1.5 μF MKP capacitor was employed.

Table F.1: Components for the DC filter.

Component	Specification
C_o	KEMET, MKP C4AEHBW5300A3JJ, 30 μF ($\pm$ 5%), 600 V_{dc}, 14 Arms, 3.6 mΩ, 255 Apk, 30 nH ESL ($\times$3)
L_o	Vishay, IHV28BZ60, 60 μH ($\pm$ 10%), 28 A, 8.5 mΩ, 1.9 MHz SRF
C_{dc}	EPCOS, MKP B32674D8155K, 1.5 μF ($\pm$ 10%), 875 V_{dc}, 7.5 A, 14.7 mΩ, 23 nH ESL

F.4 Evaluation of the DC filter

By substituting the values of the different components in transfer function H_{clr}, the gain can be depicted as in Figure F.3. As required, a 36 dB attenuation is provided at 20 kHz.

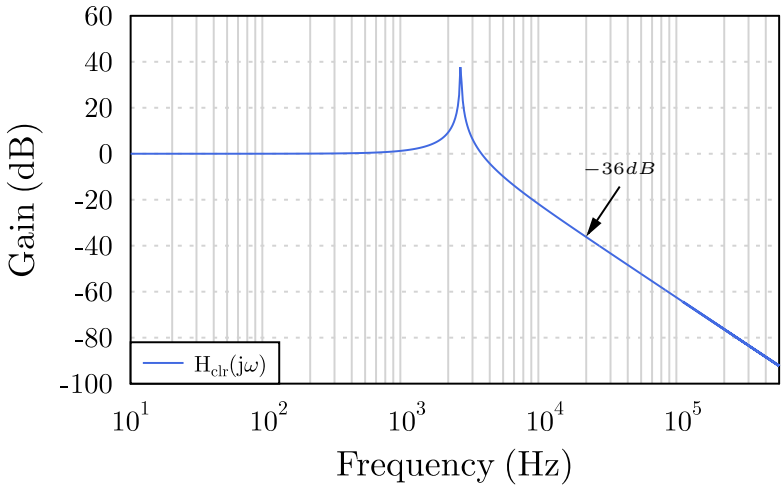


Figure F.3: Frequency response of the DC filter: magnitude of H_o.

The frequency spectrum of the battery current $I_{dc}(j\omega)$ after the application of DC filter is depicted in Figure F.4. As can be seen, the components above the switching frequency are significantly attenuated when compared with Figure F.1.

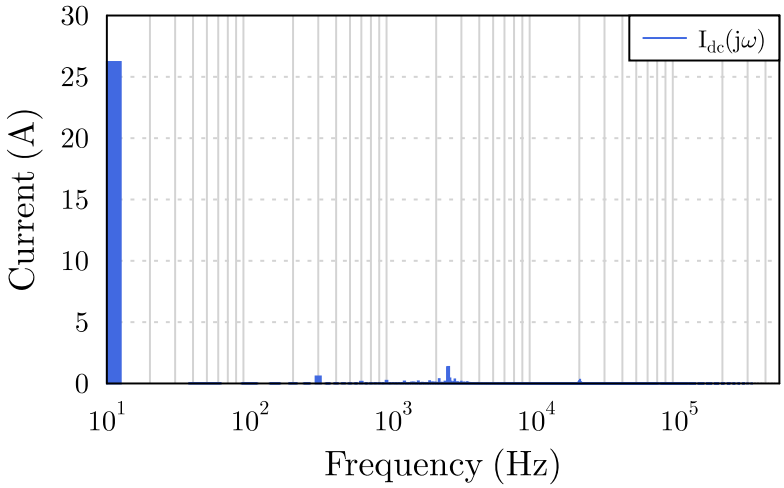


Figure F.4: Frequency spectrum of the battery current $I_{dc}(j\omega)$ (RMS values) with the DC output filter.

Effectiveness of this filter can also be verified comparing the frequency spectrum of $I_o(j\omega)$ with $I_{dc}(j\omega)$ in dBμA, as represented in Figure F.5. It is clear that a 36 dB attenuation at 20 kHz is obtained after employing the DC filter. Moreover, a decreasing tendency of the harmonics in $I_{dc}(j\omega)$ can be noticed.

Finally, a new simulation was performed with the DC filter implemented in the power circuit (see Figure G.1). From the results in Figure F.6, it is clear that the DC filter can

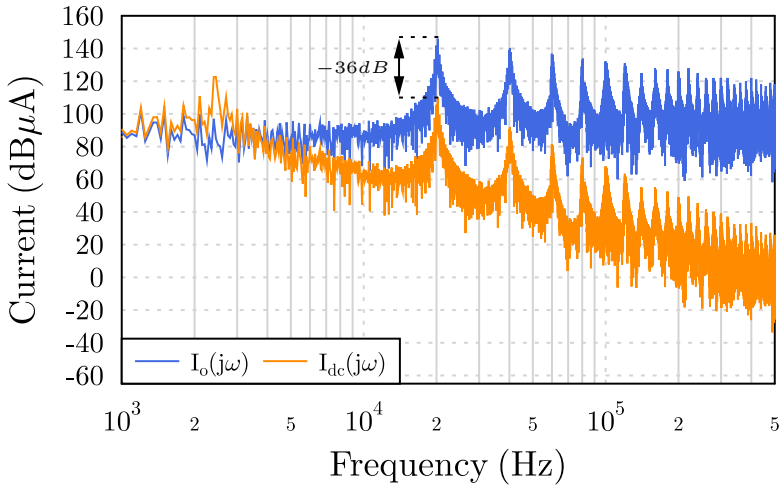


Figure F.5: Frequency spectrum of the converter output current $I_o(j\omega)$ and the battery current $I_{dc}(j\omega)$ in dBμA after employing the DC filter.

effectively reduce the ripple components of i_o. Consequently, i_{dc} is a DC current with constant magnitude and low ripple.

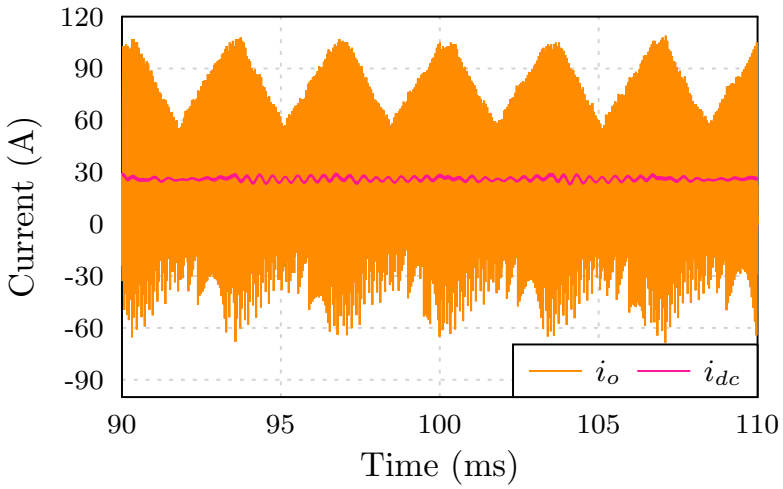


Figure F.6: Comparison between the converter output current i_o and the resulting battery current i_{dc} after employing the DC filter.

Appendix G

Simulation Model

A simulation model of the HFLMC is implemented in GeckoCIRCUITS [199] software to verify and validate the proposed modulation and the controllers. Figure G.1 show the implementation details of the power circuit and the control algorithms in this software.

The SiC MOSFET of type C2M0025120D [258] with a typically on-resistance of 25 mΩ was selected for the MC and the FB. Switching and conduction losses are modeled using information provided by the manufacturer, as represented in Figure G.2.

A thermal circuit was also build up taking in account the SiC MOSFET parameters and the selected heatsink, as represented in Figure G.3. The first-order thermal model is incorporated in the simulation considering an ambient temperature of 40°C. The heatsink is designed for a maximum junction temperature of 155°C at nominal operating conditions.

The losses can also be measured in every component which allows to produce a chart with the loss distribution in each block of the converter: EMI filter, MC, HFT, FB, and DC filter.

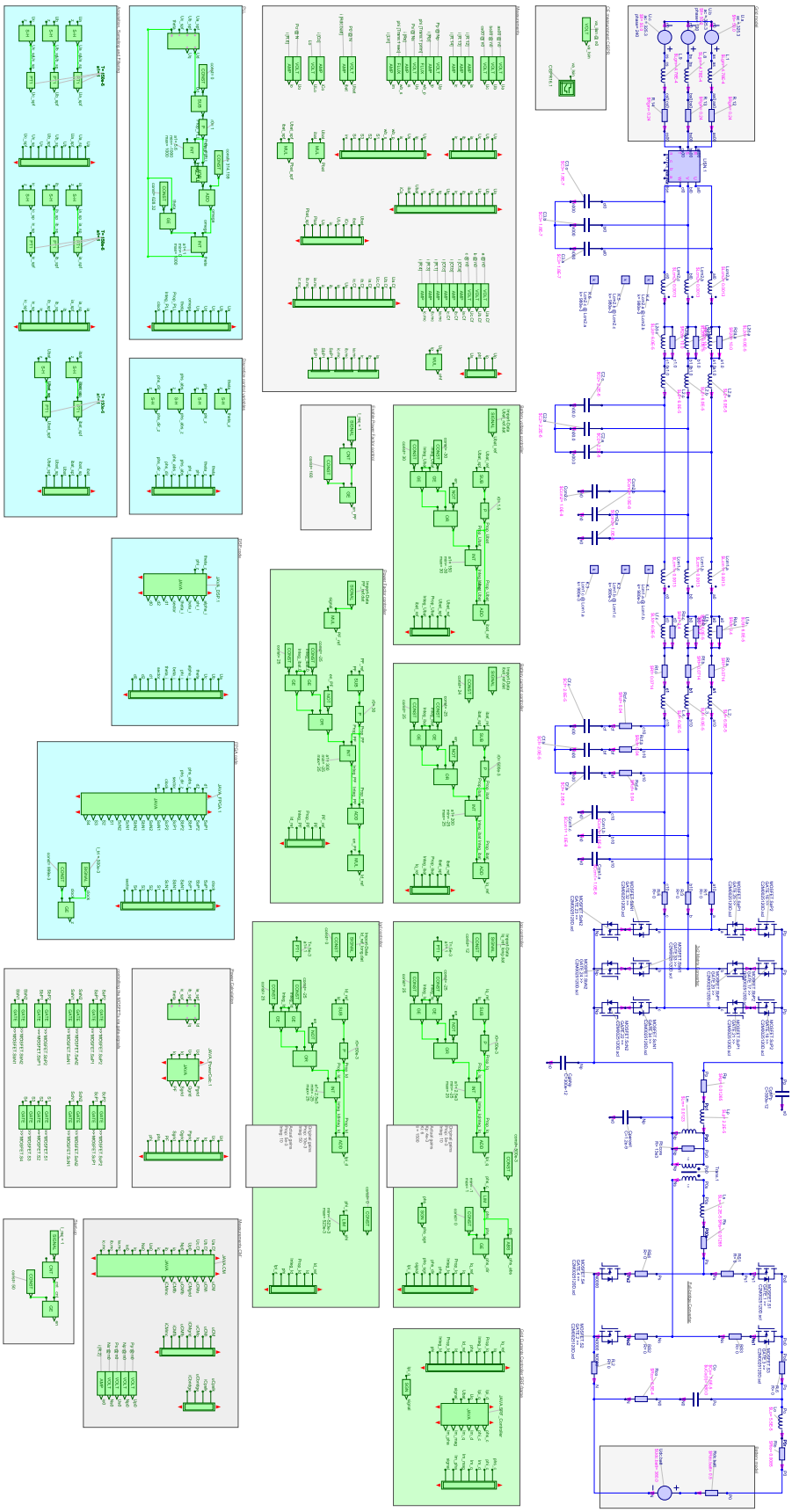
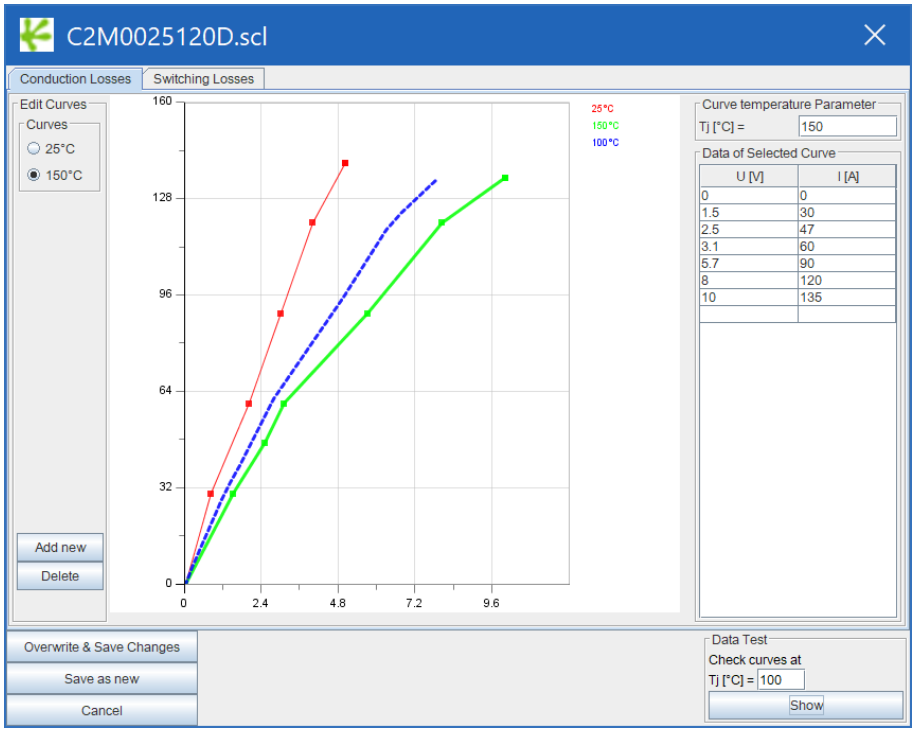
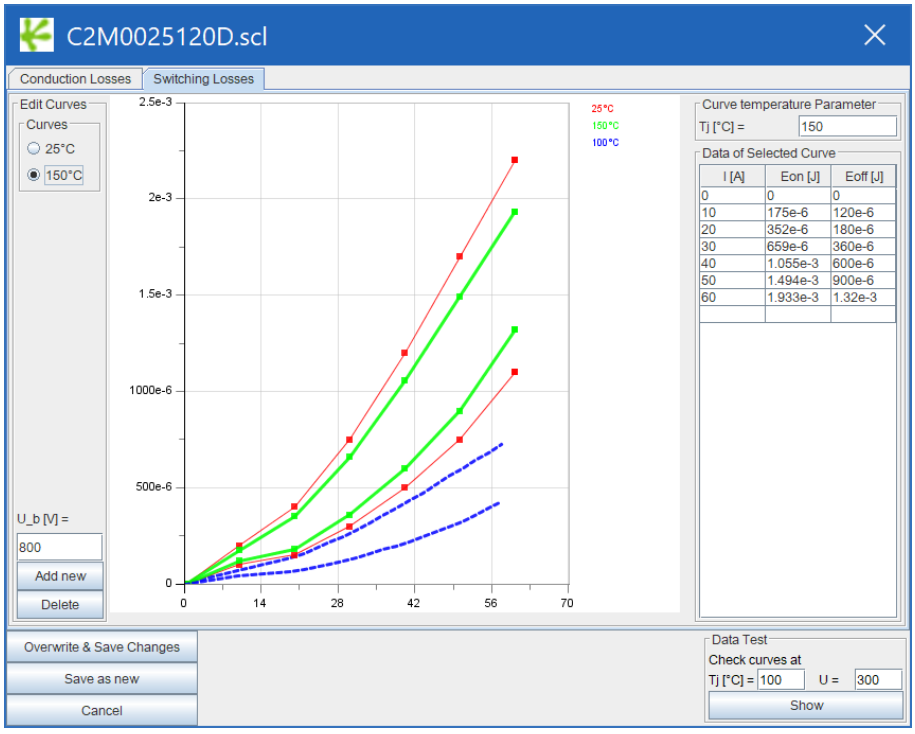


Figure G.1: Simulation model of the power circuit and control algorithms implemented in GeckoCIRCUITS software.



(a)



(b)

Figure G.2: Simulation model of the C2M0080120D SiC MOSFET implemented in GeckoCIRCUITS software. (a) Conduction losses model. (b) Switching losses model.

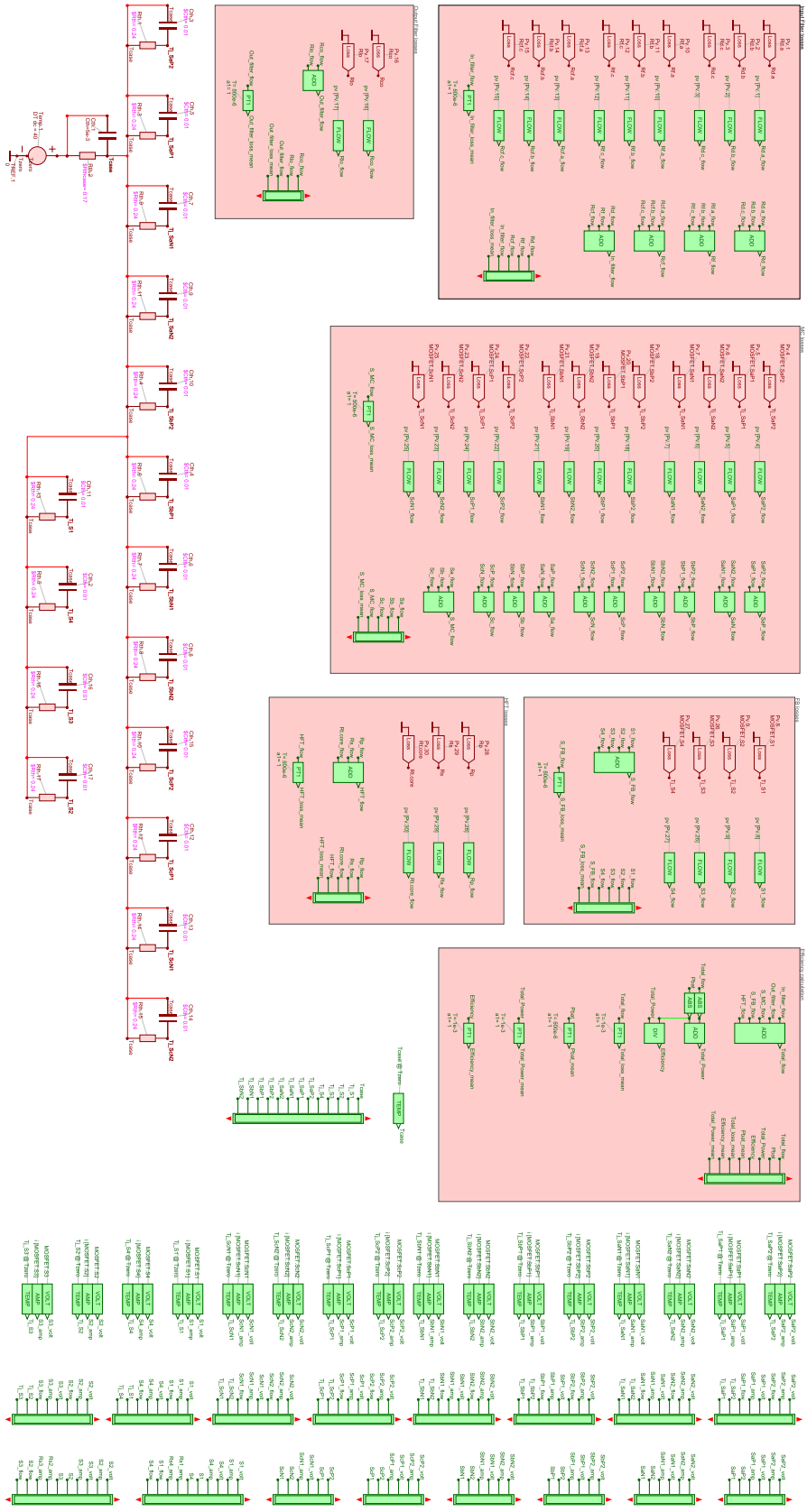


Figure G.3: Simulation model of the thermal circuit and losses measurement implemented in GeckoCIRCUITS software.

Appendix H

PCB Design: schematic, layout, and image

Four PCBs were designed to implement the different parts of the functional prototype described in Section 6.2.

The first step was to create a schematic with all the components, including the circuits for voltages and currents measurement, gate driver for the MC and FB, analogue circuits for signal conditioning, and the interfaces with DSP and FPGA. The PCB schematics are represented in Figure H.1 - Figure H.4, and Figure H.8. Schematic capture was performed using the NI Multisim [314] software from National Instruments.

The layout of the PCBs is composed by 2 layers, as illustrated in Figure H.5 and Figure H.9. In order to ensure the required current carrying capacity, a copper trace width of 95 μm was selected for the PCBs production. NI Ultiboard [315] software from National Instruments was used for the layout design.

Finally, the PCB images submitted for production are represented in Figure H.6, Figure H.7, Figure H.10, and Figure H.11.

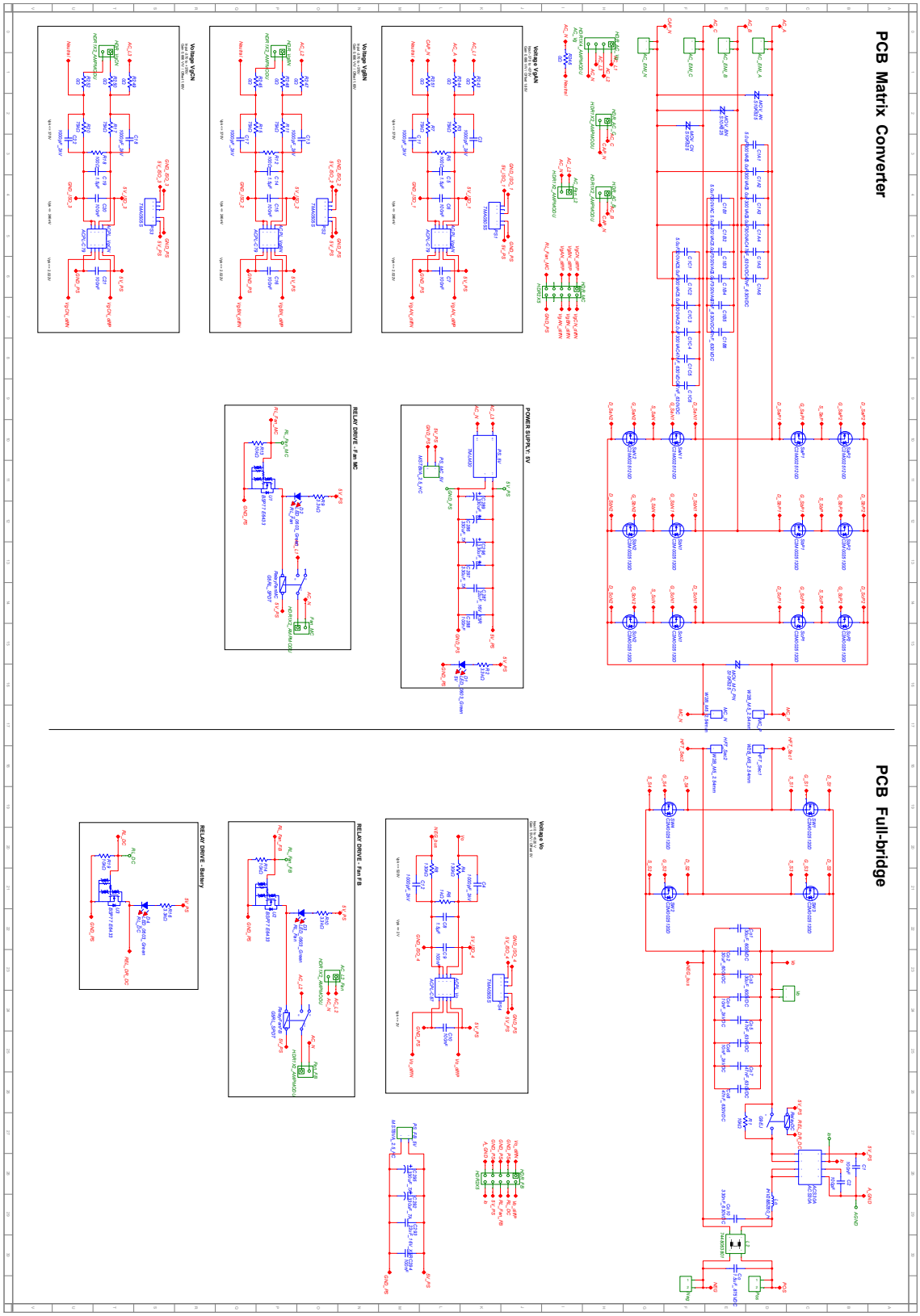


Figure H.1: PCB schematic of the power circuit, and the circuits for voltages and currents measurement.

Figure H.2: PCB schematic of the gate drivers for matrix converter.

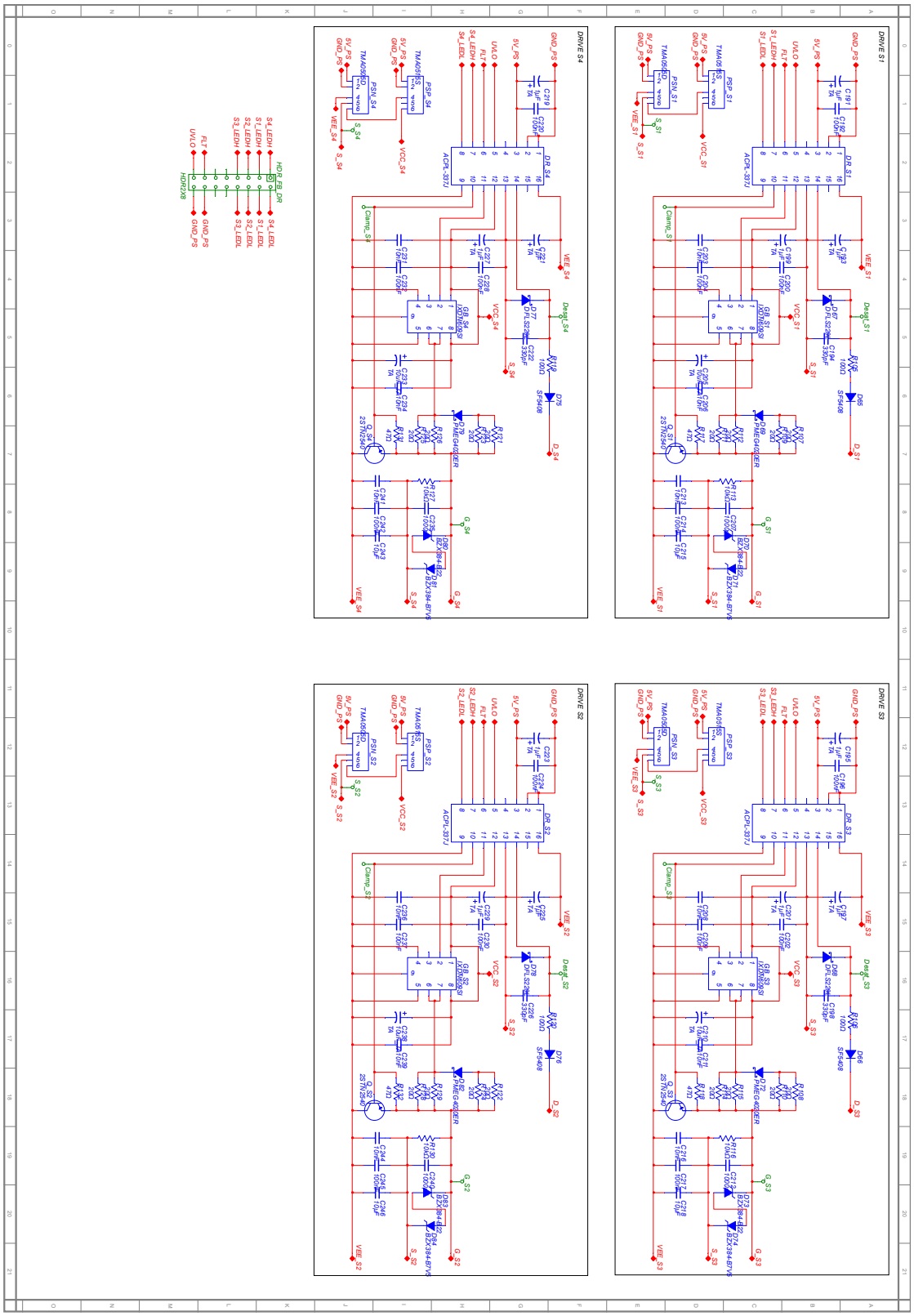


Figure H.3: PCB schematic of the gate drivers for full-bridge.

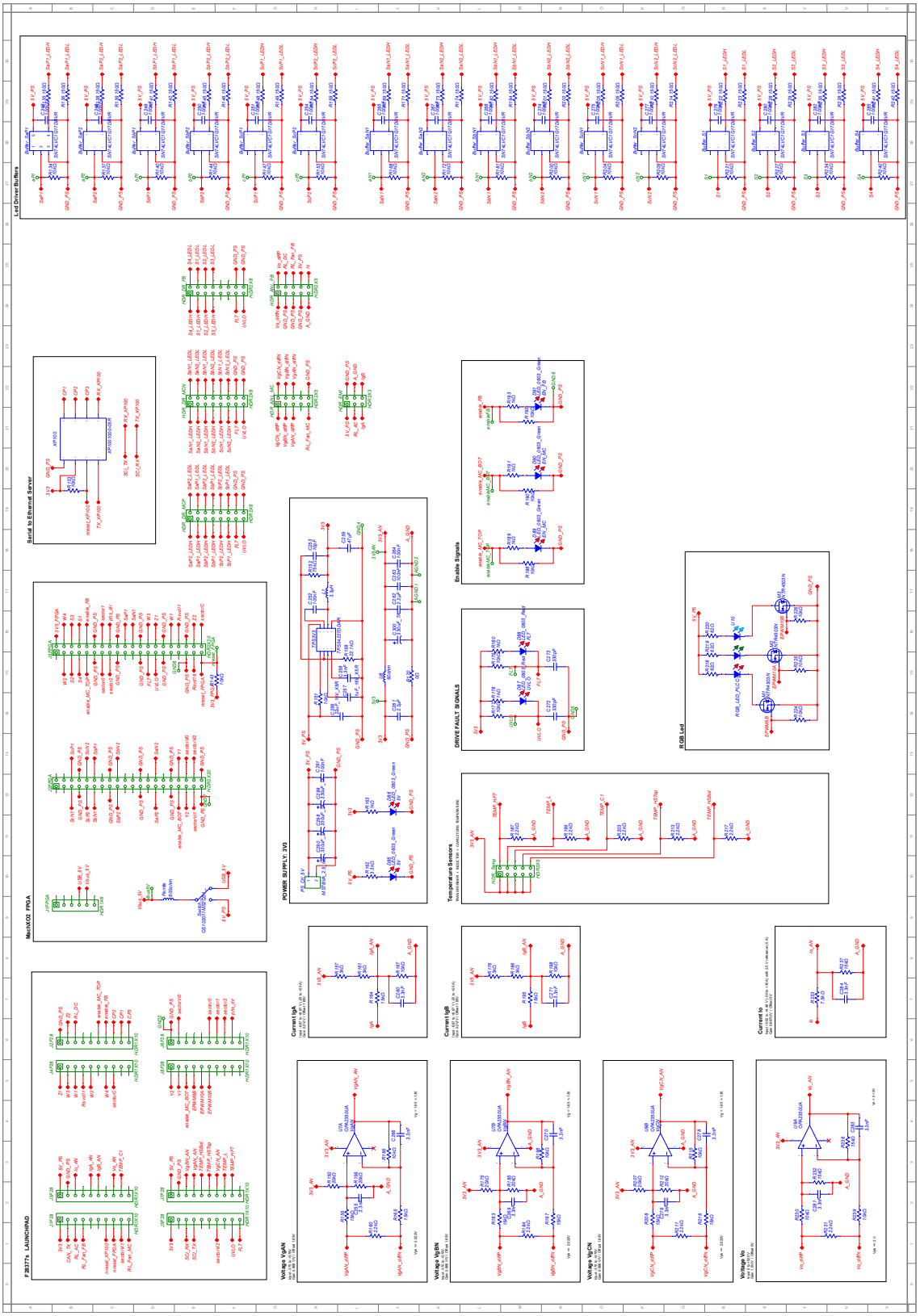


Figure H.4: PCB schematic of the analogue circuits for signal conditioning, and the interfaces with DSP and FPGA.

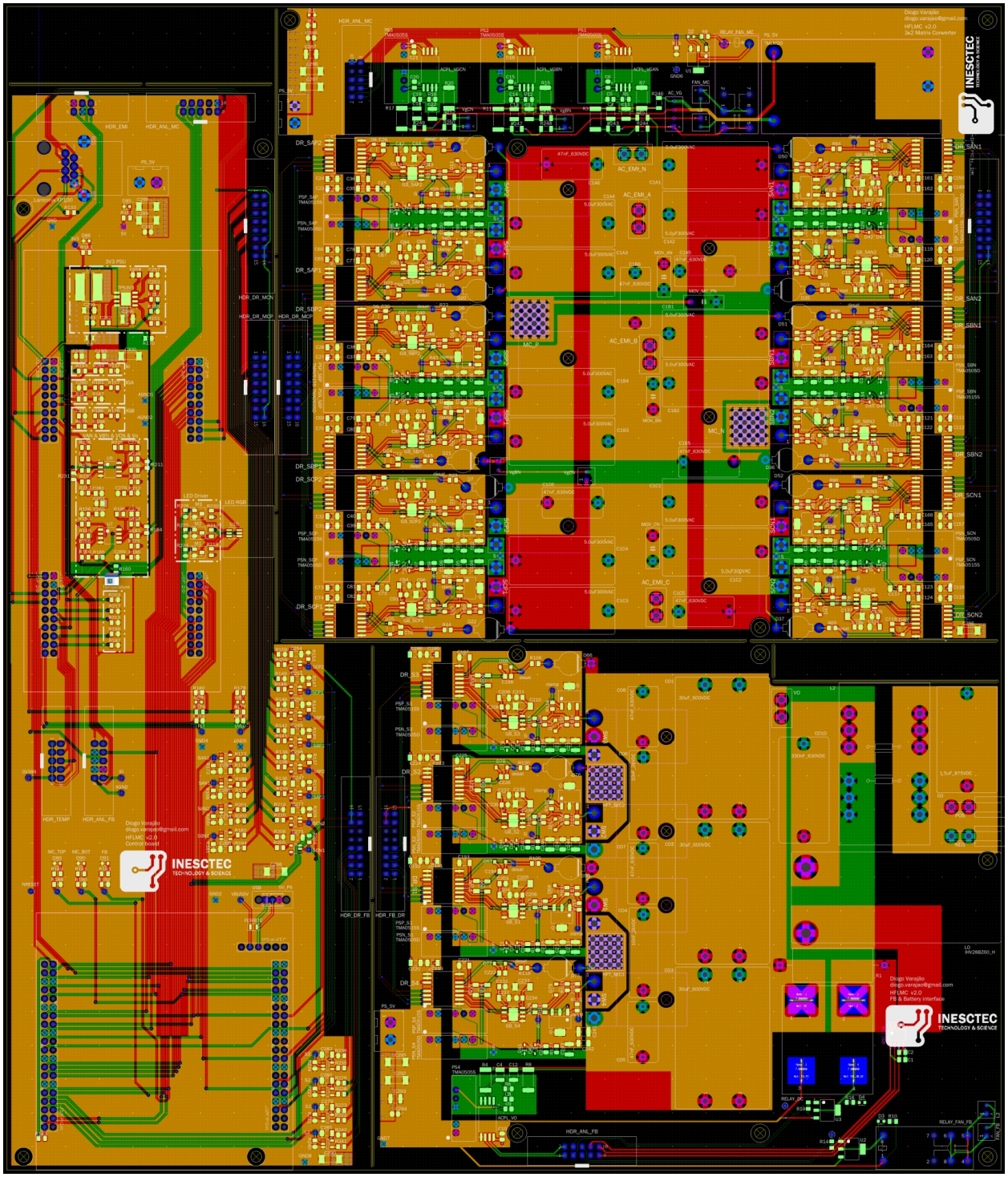


Figure H.5: PCB layout: 2 layers, 295 x 345 mm.

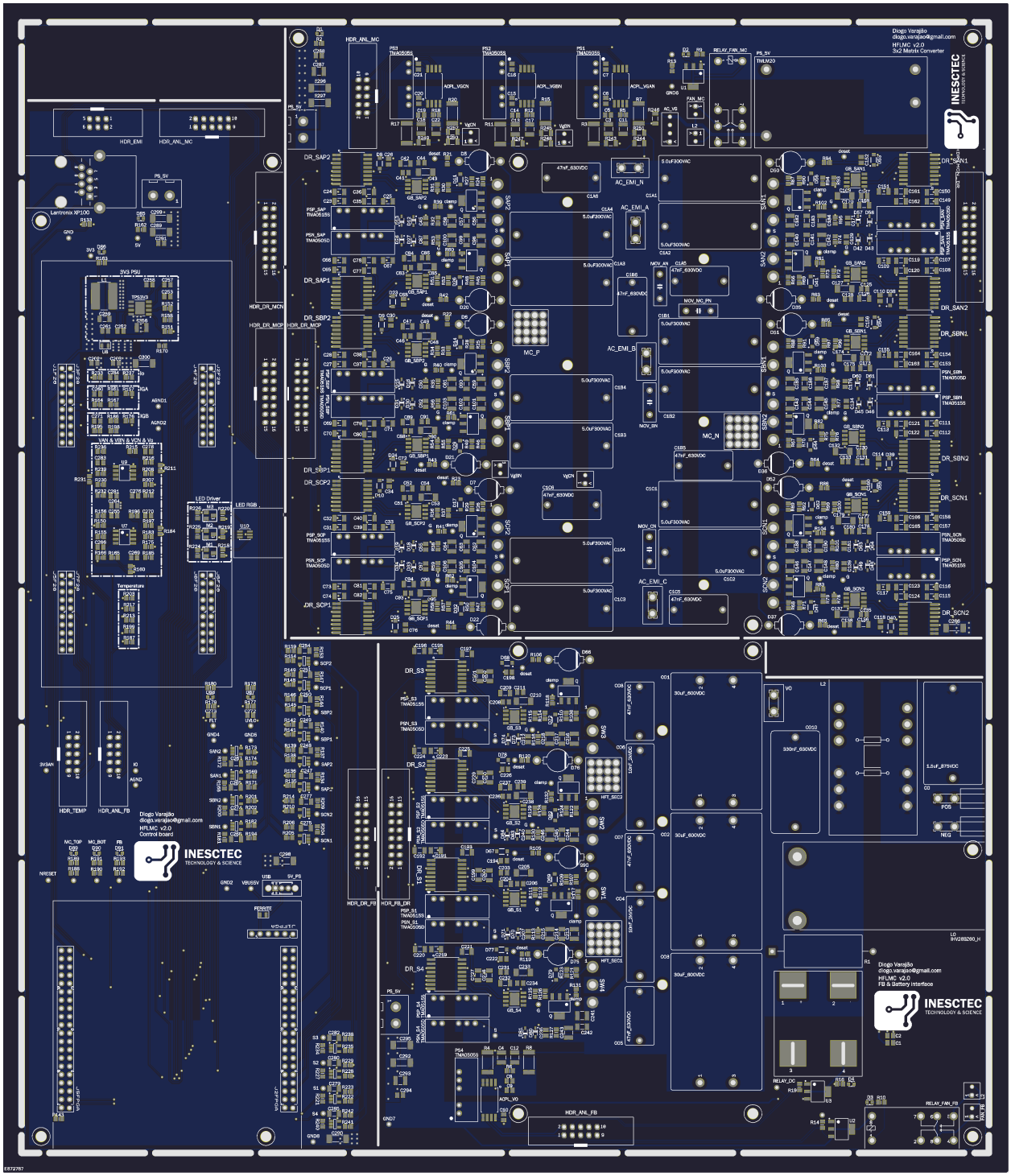


Figure H.6: PCB image submitted for production: top side, 95 μm copper.

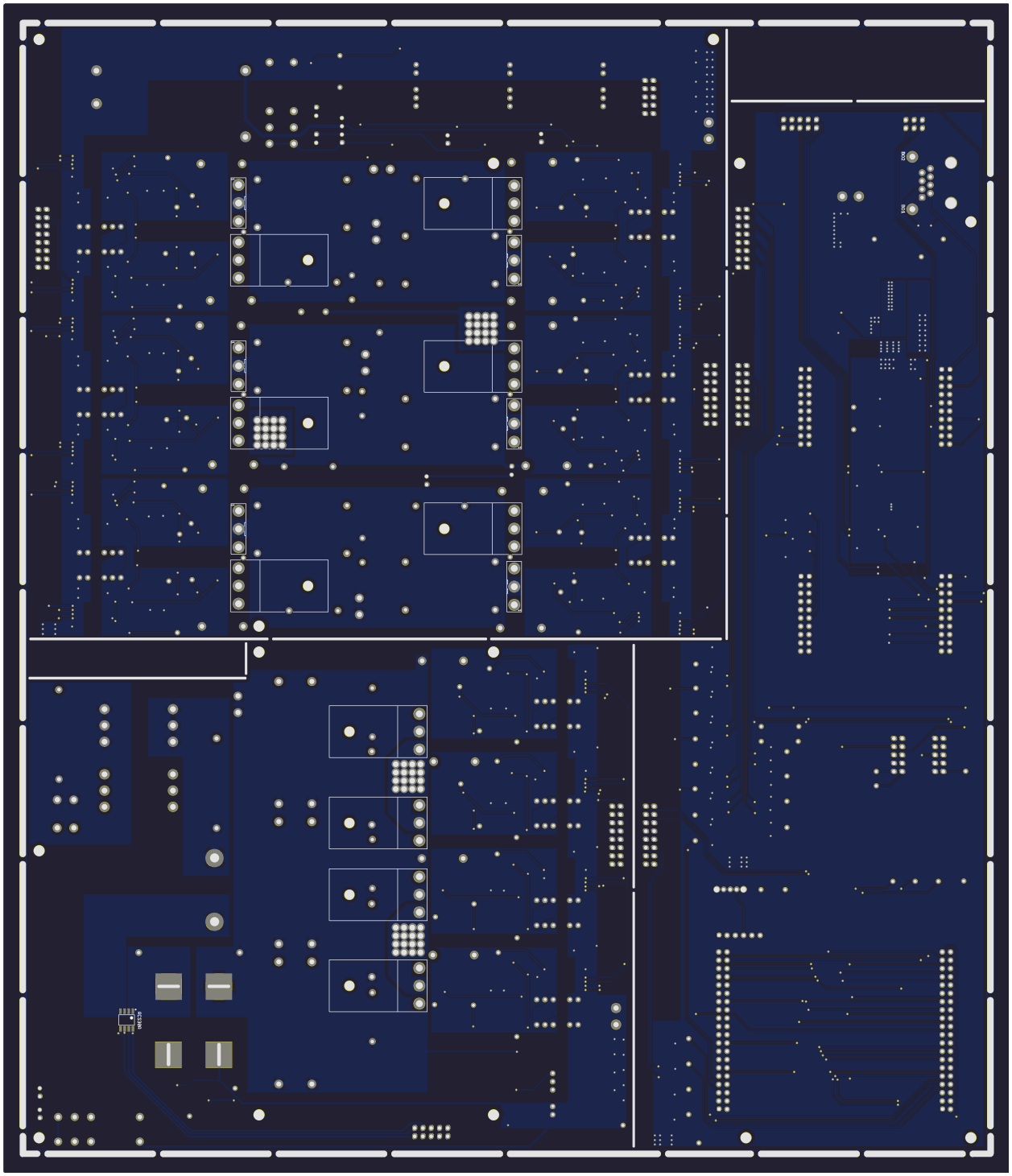


Figure H.7: PCB image submitted for production: bottom side, 95 μm copper.

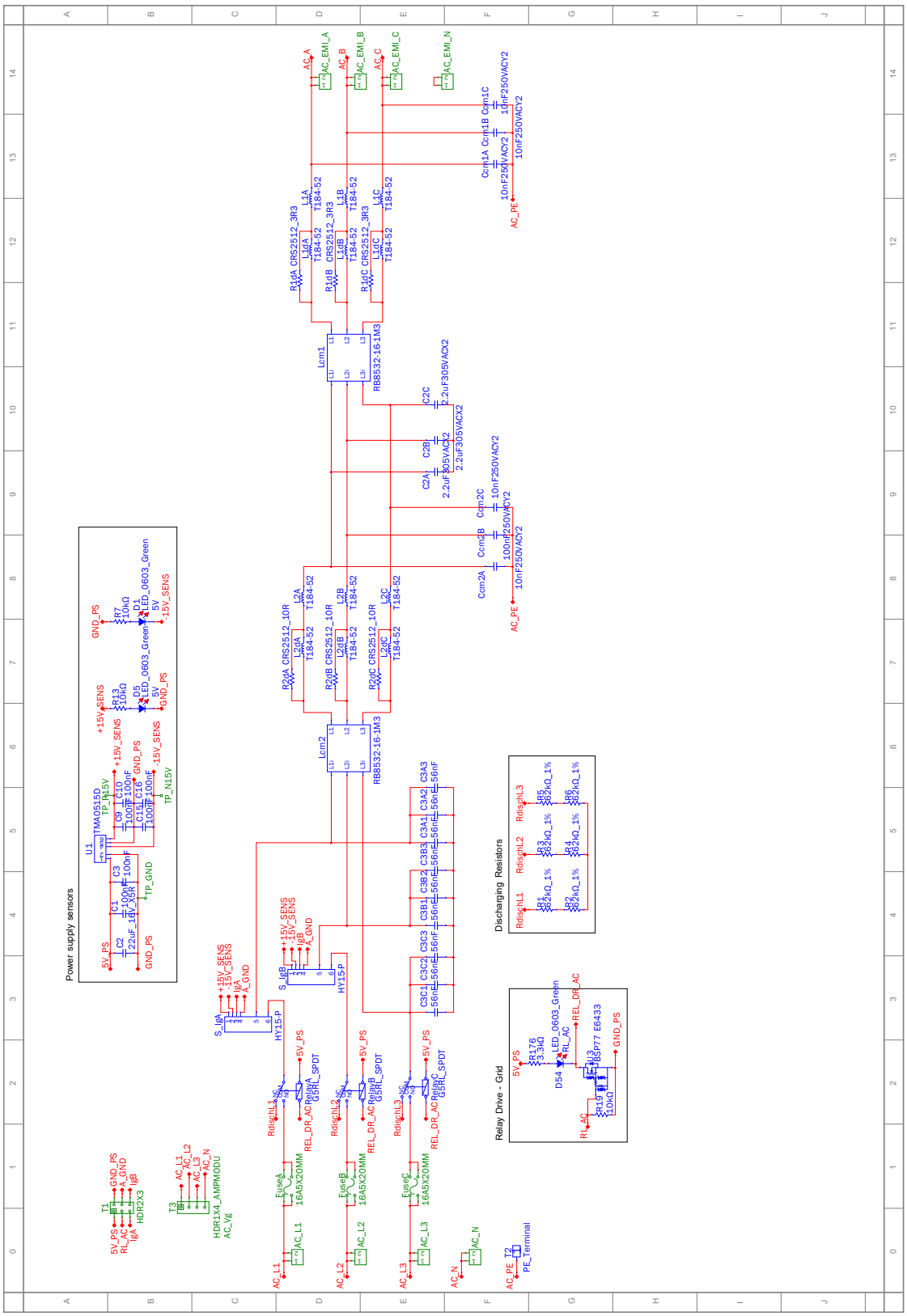


Figure H.8: PCB schematic of the EMI Filter.

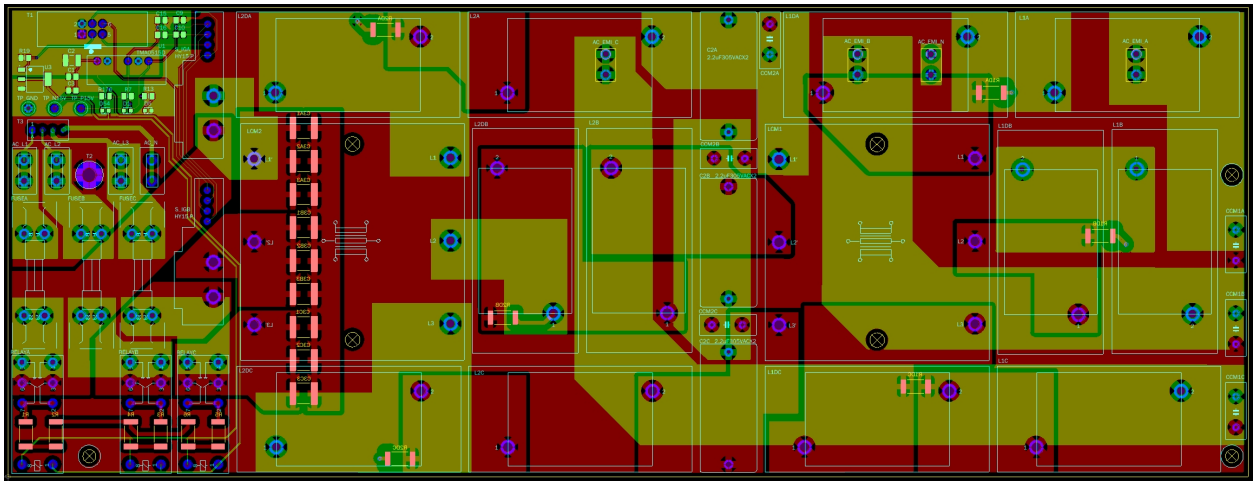


Figure H.9: PCB layout of the EMI Filter: 2 layers, 305 x 115 mm.

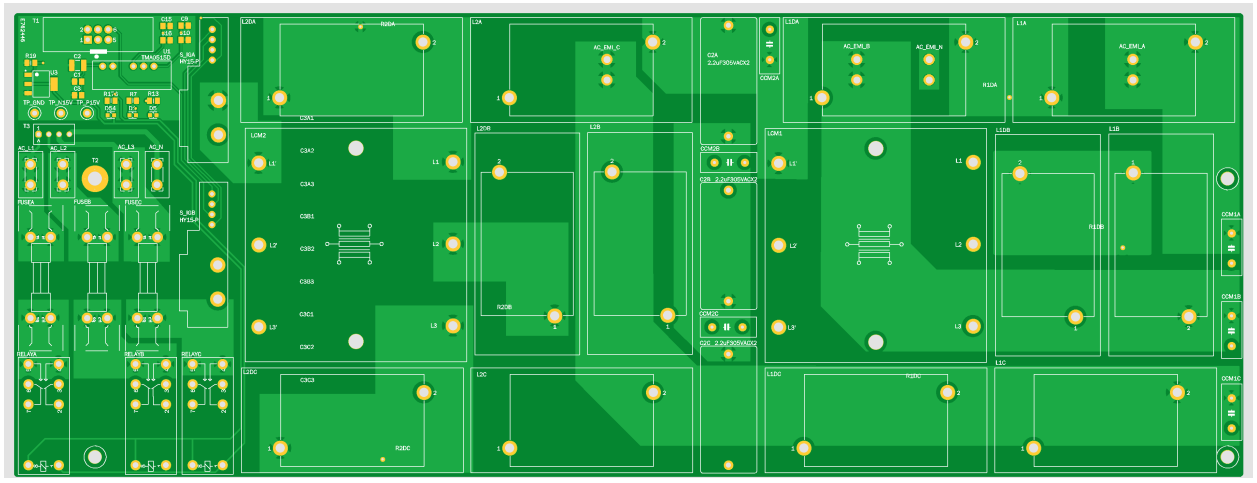


Figure H.10: PCB image of the EMI Filter submitted for production: top side, 95 μm copper.

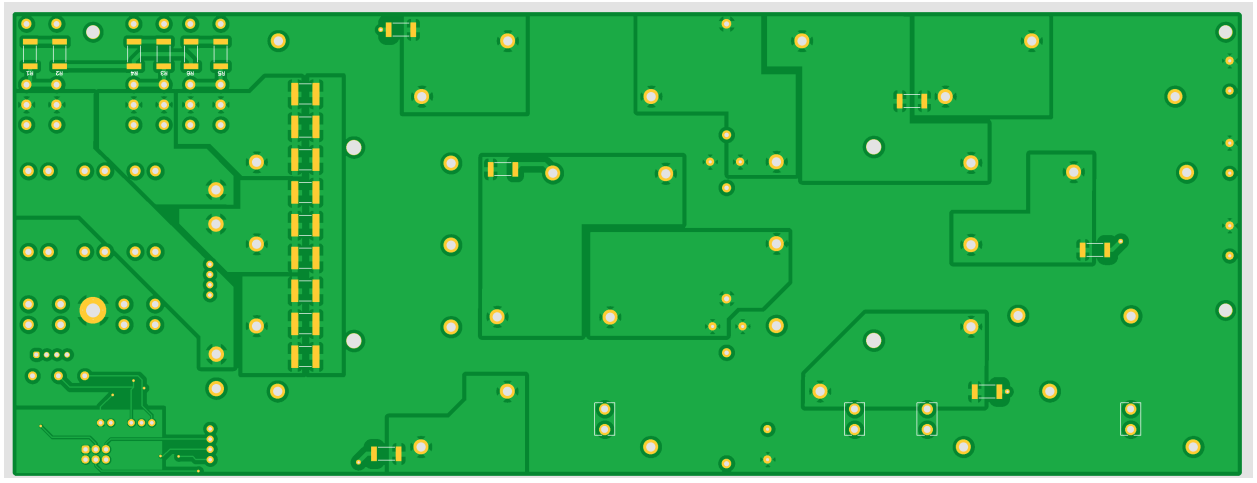


Figure H.11: PCB image of the EMI Filter submitted for production: bottom side, 95 μm copper.

Appendix I

Testbench at the SGEV Laboratory

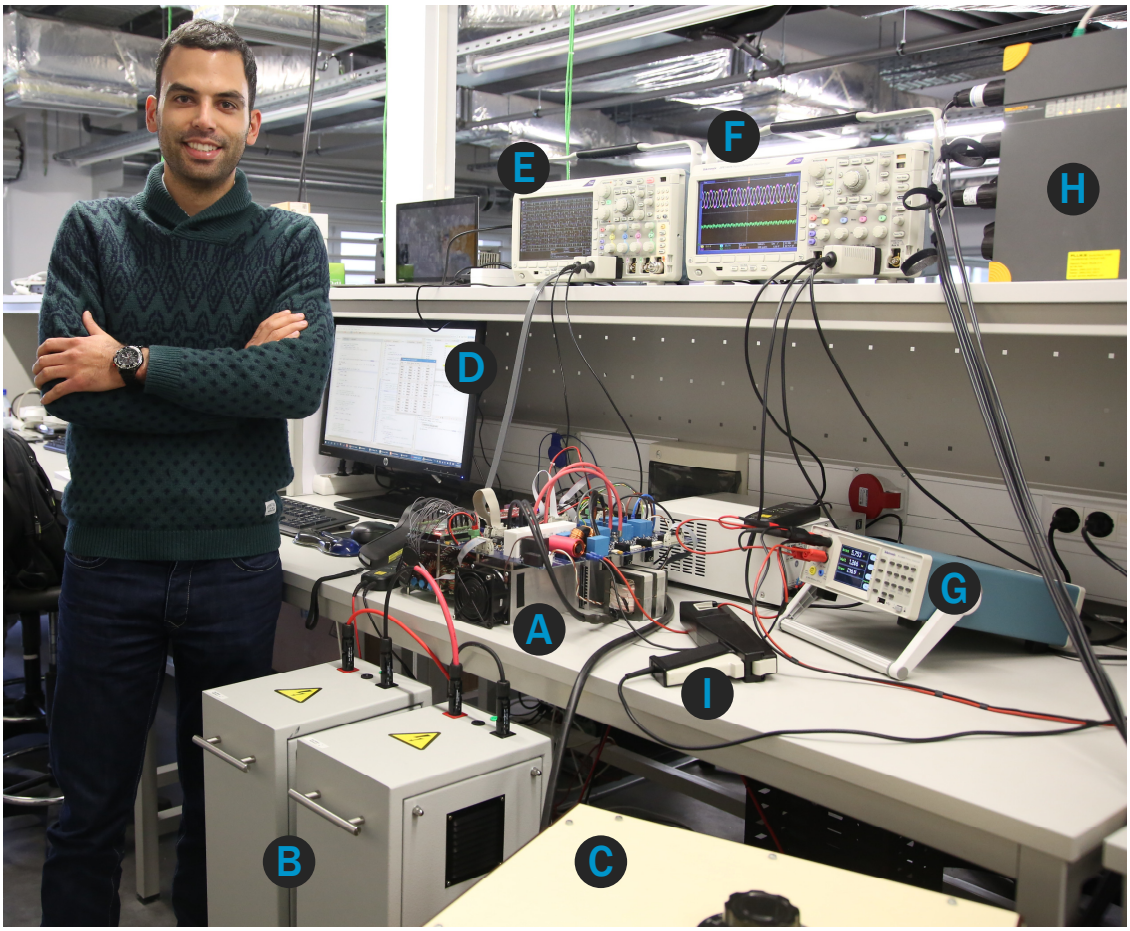


Figure I.1: Photo of the testbench at the Smart Grids and Electric Vehicles (SGEV) laboratory of INESC TEC. Legend:

Ⓐ High-frequency Link Matrix Converter; Ⓑ Battery pack of 2.3kWh and 192V;
Ⓒ Autotransformer; Ⓓ Graphical User Interface; Ⓔ Tektronix MDO3024 Oscilloscope;
Ⓕ Tektronix DPO3034 Oscilloscope; Ⓖ Tektronix PA1000 Power Analyzer;
Ⓗ Fluke 1760 Power Quality Recorder; Ⓘ Tektronix TCP0150 Current Probe.

The Centre for Power and Energy Systems (CPES) develops research activities in the following areas: Decision Making, Optimisation and Computational Intelligence, Forecasting, Static and Dynamic analysis of Energy Grids, Reliability, and Power Electronics. The SGEV laboratory allows the CPES to put into practice the concepts, algorithms and scientific knowledge generated by the Power & Energy Systems cluster of INESC TEC. The SGEV laboratory infrastructure is composed by the following equipments:

- 400 V busbars that can be configured with up to six semi-buses;
- 25 kWh FLA battery bank coupled to 3x SMA Sunny Island 5048 inverters;
- 6 kWp PV panels connected to 3x SMA Sunny Boy 3000HF inverters;
- 3 kW micro wind turbine emulator connected to a SMA Windy Boy 3000;
- 54 kW resistive load bank;
- LV cables emulators (100 A / 0.3 Ω and 50 A / 0.5 Ω);
- Triphase PM15A30F30 power module;
- OPAL-RT OP5600 real-time simulator.

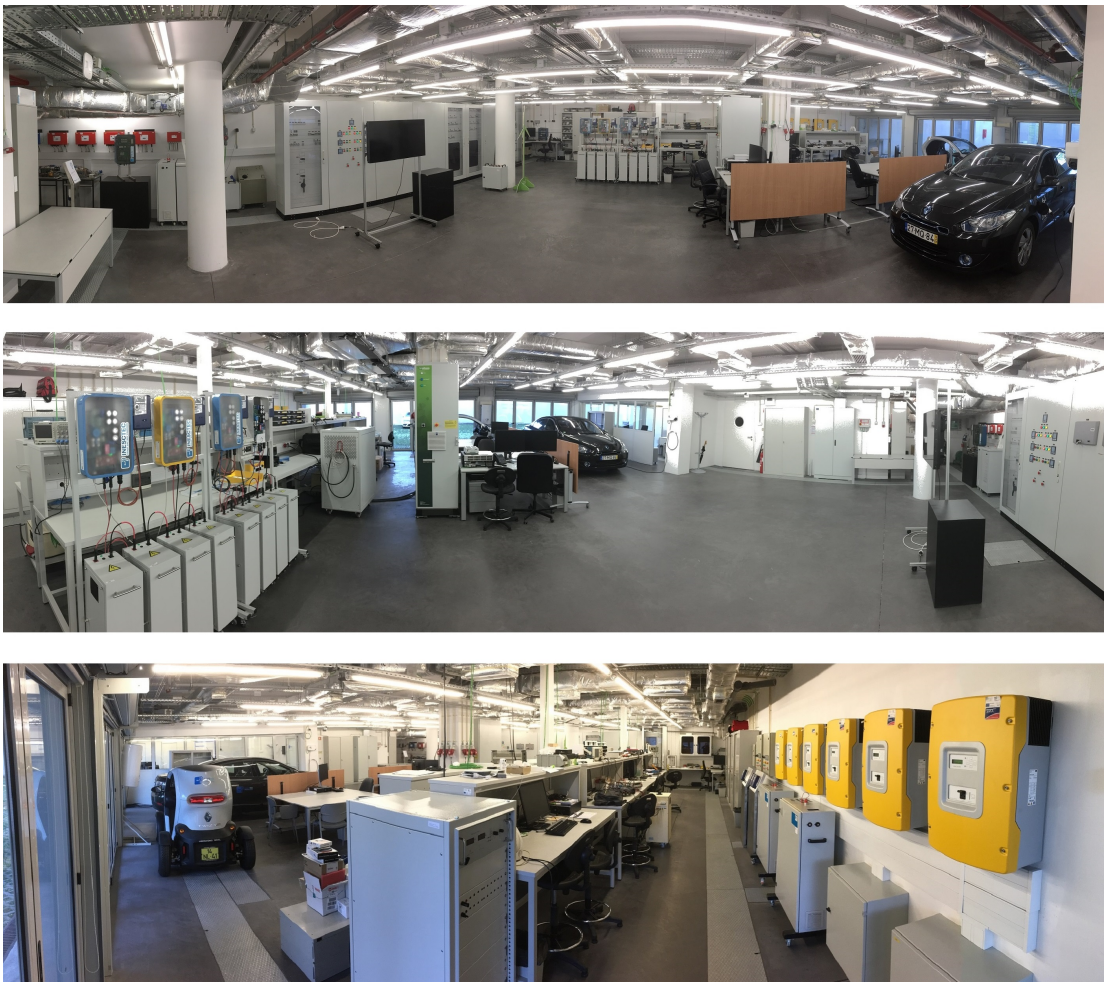


Figure I.2: Overview of the SGEV laboratory of INESC TEC.

Appendix J

HFLMC vs VSC-DAB

As previously described in section 1.2, the power conversion system is a key part of the CES. In this section is made an extensive comparison between the HFLMC and the traditional solution based on a Voltage Source Converter and a Dual Active-Bridge (VSC-DAB). Simulation results are presented to assess the power quality provided by the front-end and the battery side converters, as well as performance evaluation, efficiency analysis and discussion of most relevant design components.

H.1 Prototypes description

Two prototypes were designed to fulfill the specifications and requirements of Table 1.4. A 10 kW PCS to connect the three-phase 230 / 400 V_{rms}, 50 Hz mains to a battery pack with voltage range of 320 V to 490 V is considered.

It was decided to investigate the application of SiC MOSFETs for the switching devices. More specifically, the 1.2 kV MOSFETS of type C2M0025120D [258] with a typically on-resistance of 25 mΩ at a junction temperature of 25 °C were chosen. The components for the VSC-DAB and for the HFLMC prototypes are listed in Table J.1 and Table J.2, respectively.

The input filters for both converters were designed in order to provide the same harmonic attenuation at nominal operating conditions. The LCL filter for the VSC-DAB topology was designed following the procedure described in [316]. The resonant frequency was fixed at 6 kHz with $L_f = L_B = 250$ μH, $C_f = 5.6$ muF and a damping resistance $R_d = 1$ Ω. The LC filter for the HFLMC topology was designed following the procedure described in [90]. The resonant frequency was fixed at 2 kHz with $L_f = 320$ μH, $C_f = 20$ μF and a damping resistance $R_d = 8$ Ω.

The turns ration n of the transformer and the leakage inductance are designed in order to allow the maximum output power flow in the worst operation conditions. In this way, was selected the pair n = 2 / L = 250 μH for the VSC-DAB, and n = 2 / L = 84 μH for the HFLMC.

Table J.1: Components of the VSC-DAB.

MOSFETs SaP,... ScN; S5,... S8	1 × C2M0025120D, 1.2 kV, 90 A, 25 mΩ
MOSFETs S1, S2, S3, S4	2 × C2M0025120D, 1.2 kV, 90 A, 25 mΩ
Transformer	1 × PM114/93 N87; 36 primary turns, 18 secondary turns; Litz wire, 30 strands, 0.400 mm
Inductor L_f, L_B	1 × PM50/39 N87; 41 turns; Litz wire, 30 strands, 0.400 mm
Inductor L_o	1 × SER2918H, 10 μH, 2.60 mΩ
Capacitors C_f	1 × B32926C3565K, 5.6 μF, 305 V
Capacitor C_{dc}	2 × 2 × B43501A0567M000, 560 μF, 420 V
Capacitors C_o	4 × B32678G6256K, 25 μF, 630 V
Heat Sink (passive cooling)	2 × FISCHER ELEKTRONIK - SK 92/75 SA 1.60 °C/W
Total volume of components: 3.1 L (2.5 L excluding heatsink)	
Total weight of components: 5.9 Kg (5.1 Kg excluding heatsink)	

Table J.2: Components of the HFLMC.

MOSFETs SaP1,... ScN2;	1 × C2M0025120D, 1.2 kV, 90 A, 25 mΩ
MOSFETs S1, S2, S3, S4	2 × C2M0025120D, 1.2 kV, 90 A, 25 mΩ
Transformer	1 × PM87 N87; 32 primary turns, 16 secondary turns; Litz wire, 30 strands, 0.400 mm
Inductor L_f	1 × PM50/39 N87; 52 turns; Litz wire, 30 strands, 0.400 mm
Inductor L_o	6 × SER2918H, 10 μH, 2.60 mΩ
Capacitors C_f	2 × B32926C3106K, 10 μF, 305 V
Capacitors C_o	4 × B32678G6256K, 25 μF, 630 V
Heat Sink (passive cooling)	2 × FISCHER ELEKTRONIK - SK 56/75 SA 0.45 °C/W
Total volume of components: 3.4 L (1.6 L excluding heatsink)	
Total weight of components: 5.7 Kg (3.2 Kg excluding heatsink)	

Concerning the connection with the battery pack, an output LC filter was designed to reduce the current ripple, and providing the same attenuation at nominal operating conditions for both converters. For the VSC-DAB $L_o = 10$ μH and $C_o = 100$ μF were chosen, and for the HFLMC $L_o = 60$ μH and $C_o = 100$ μF. An aluminium electrolytic capacitor

of C_{dc} = 560 μF was selected for the DC-link of the VSC-DAB. SiC MOSFETs can be operated at higher temperatures, providing simultaneously low conduction and switching losses compared with IGBTs. So, passive cooling method was designed to provide a proper converter operation considering an ambient temperature of 40 °C. As a criterion to project the heatsink, was decided to have the same maximum junction temperature (100 °C) in both converters for nominal operating conditions.

H.2 Simulation results

The two converters are simulated using GeckoCIRCUITS [199] coupled with MLS. The simulation models and parameters are described above. The grid was modelled with a three-phase AC voltage source in series with a line impedance of 50 μH and 50 mΩ. In other hand, the battery is modelled by a DC voltage source in series with a resistance of 0.5 Ω as an approximation for the battery internal impedance [71]. For these comparative tests, was decided to control the converter to follow a reference of power at the battery pack. A proportional-integral (PI) controller was designed for this task. The operation of both converts at nominal conditions is shown in Figure J.1 and Figure J.2. A transition in the power reference from $P_{batt}{}^{*}$ = 0 to $P_{batt}{}^{*}$ = 10 kW and then to $P_{batt}{}^{*}$ = - 10 kW was performed to evaluate the dynamic operation of the converters. As can be seen in Figure J.1(a) and Figure J.2(a), the power in the battery is properly controlled, and the power in the grid has a slightly difference due to power losses in the conversion process. Figure J.1(c) and Figure J.2(c) show the voltage and current in the battery pack. A change in the battery voltage naturally occurs due to the internal impedance of the battery. As supposed, only a small ripple appears in the battery current. The measured ripple in battery for both converters over the output power range is represented in Figure J.3, and complies with the requirements listed in Table 1.4. The resultant current in the grid has improved dynamic and power quality even during inversion of the power flow, as shown in Figure J.1(b) and Figure J.2(b). The measured THD in grid current over the output power range is depicted in Figure J.4. As specified in the requirements of Table 1.4, the THD is kept below 5 % for input current above 40 % of $I_{AC,P,nom}$. Regarding the high frequency link operation, it is noticeable a difference in the primary voltages applied to the transformer (Figure J.1(d) and Figure J.2(d)). This clearly shows the single-stage operation of the HFLMC where a low-frequency envelope appears due to the absence of a DC-link between the grid and the transformer.

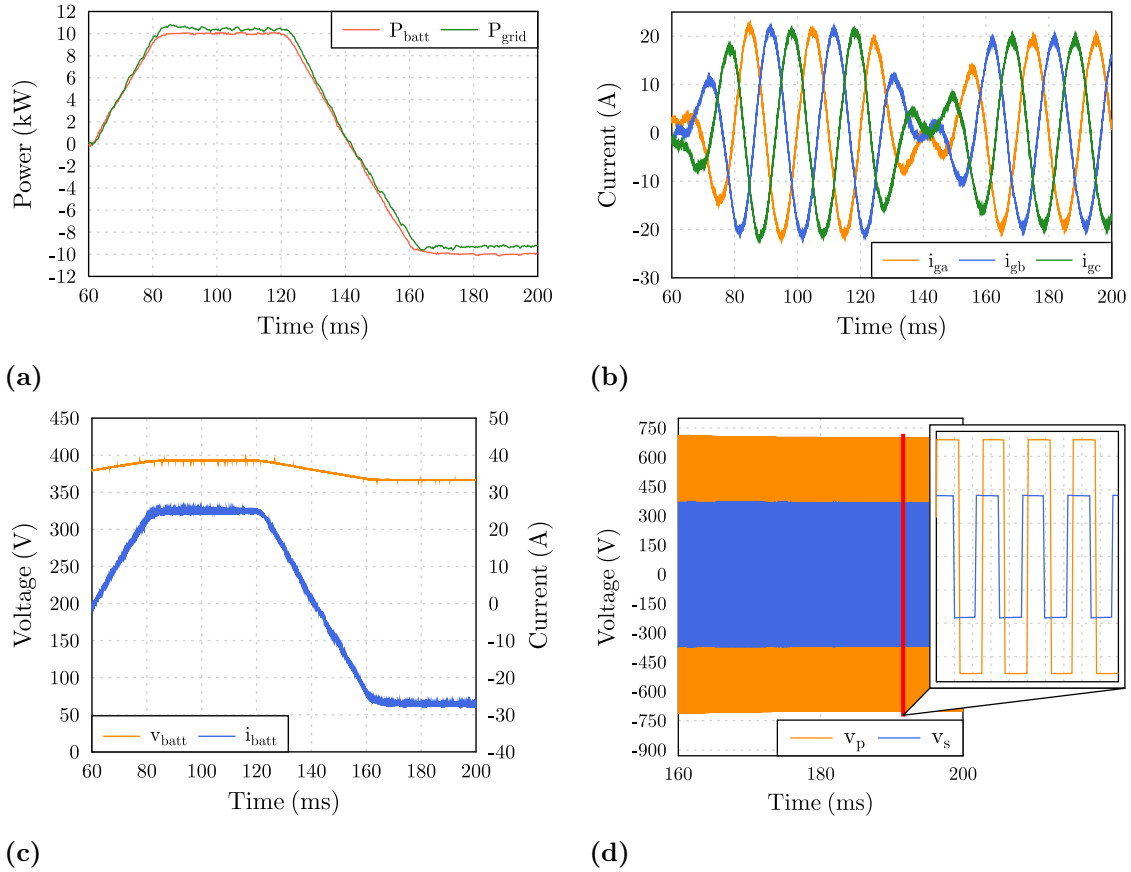


Figure J.1: Simulation results for the VSC-DAB operation for a transition from $P_{batt}{}^{*} = 0$ to $P_{batt}{}^{*} = 10$ kW and then to $P_{batt}{}^{*} = -10$ kW. (a) Simulated power in the battery pack and in the grid, and (b) voltage and current in the battery pack, and (c) AC phase currents i_{ga}, i_{gb}, i_{gc}, and (d) voltages v_p, v_s across the transformer windings.

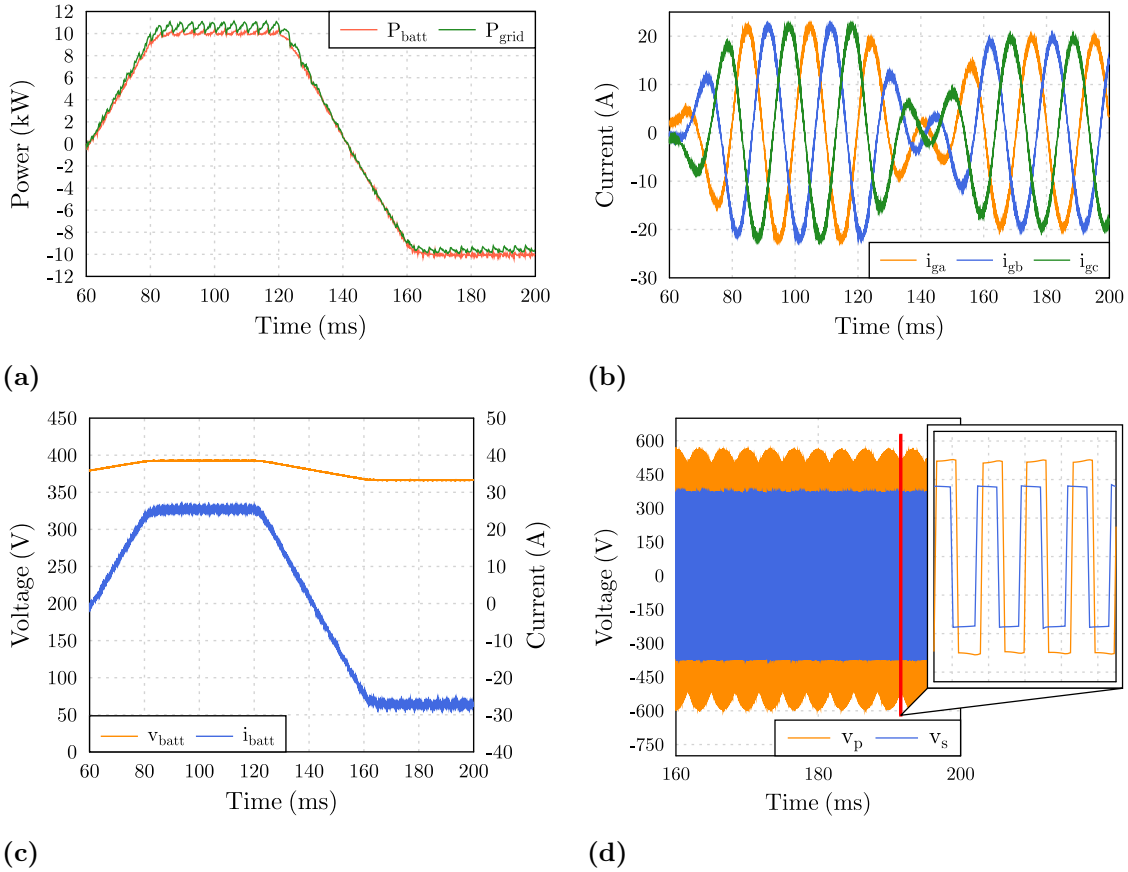


Figure J.2: Simulation results for the HFLMC operation for a transition from $P_{batt}{}^{*} = 0$ to $P_{batt}{}^{*}$ = 10 kW and then to $P_{batt}{}^{*}$ = - 10 kW. (a) Simulated power in the battery pack and in the grid, and (b) voltage and current in the battery pack, and (c) AC phase currents i_{ga}, i_{gb}, i_{gc}, and (d) voltages v_p, v_s across the transformer windings.

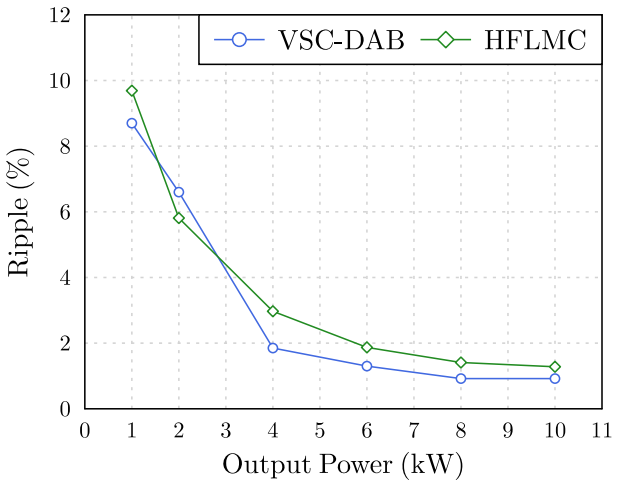


Figure J.3: Measured current ripple in the battery pack for the VSC-DAB and for the HFLMC over the output power range for battery voltage of 380 V.

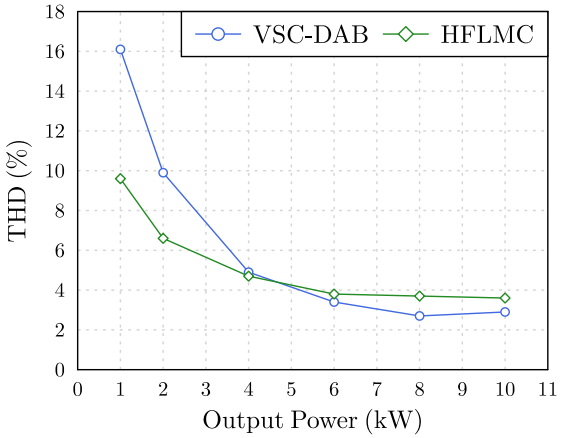


Figure J.4: Measured THD in grid current for the VSC-DAB and for the HFLMC over the output power range for battery voltage of 380 V.

The measured efficiency over the output power range for battery voltages of 320 V and 380 V is plotted in Figure J.5. It can be seen, that the efficiency for the VSC-DAB converter is almost the same for these two output voltages, and reaches a peak of 97.1 % for 8 kW and a battery voltage of 320 V. For the HFLMC, a peak efficiency of 97.4 % is reached at an output power of 6 kW and a battery voltage of 320 V. The HFLMC efficiency curve for 380 V is below the other curves, but presents good efficiency near the nominal output power. A load-independent loss component of 20 W, representing auxiliary circuits, gate drives, sensors and EMI filters was also considered. Figure J.6 shows the calculated distribution of the power losses for the HFLMC at nominal operating conditions. It is clear that the SiC MOSFETs account for 62 % of the power losses in the converter. For this reason, a thermal heatsink to ambient resistance of $R_{th,s-a} = 0.22$ °C/W was selected.

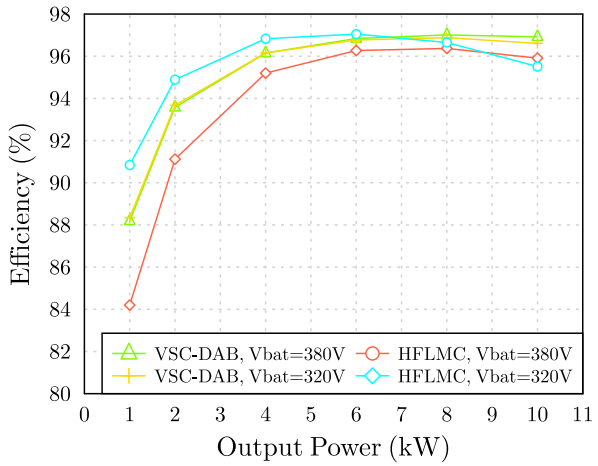


Figure J.5: Measured efficiency in simulation for the VSC-DAB and for the HFLMC over the output power range for battery voltages of 320 V and 380 V.

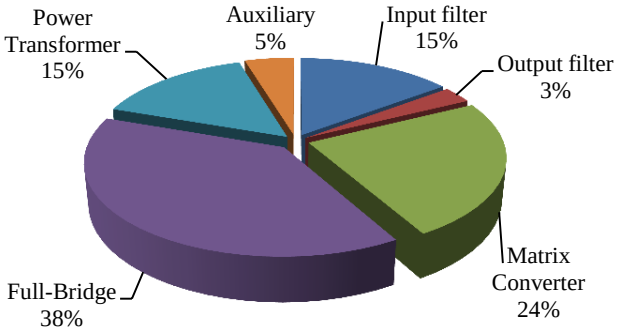


Figure J.6: Calculated distribution of the power losses for the HFLMC at an output power of 10 kW and a battery voltage of 380 V.

H.3 Conclusions

A comparative analysis of both topologies operating in closed loop allows to see that the two topologies can track a set point with very small error, in steady-state or during transitions. At the grid interface, smooth and controlled current waveforms can be observed for two critical situations – the converter start-up and an inversion in the power flow with full load. Regarding the power quality at the battery pack, it can be found that with 1 kW load the current ripple is already below 10 %, which stands for a good performance considering most of the application requirements. For higher loads, ripple drops down to around 1 %, which indicates that if necessary the output filter can be reduced to improve the converter efficiency, reducing cost, weight and size. In this case, for light loads, a variable frequency modulation can be a solution to investigate in order to keep the ripple under a specified limit. Analysing the harmonic distortion at the grid connection, the values achieved are by far within the most commonly applied standards, with the HFLMC being particularly good in the 10 to 50 % load range, when compared with the VSC-DAB solution. For heavier loads both are very close in terms of THD with values below 4 %.

Comparing both topologies in terms of complexity and component count, they are quite similar. It can be noticed that the matrix converter-based topology is by far smaller and lighter, but significantly higher power losses lead to the need for a large heatsink which seriously penalizes this topology. A pie chart with the distribution of the losses allows to see that almost two thirds (2/3) of the losses are in the power switches for the HFLMC. They are mainly conduction losses, which have a quadratic relationship with the current value. This phenomenon can be observed in the efficiency plots, where curves for different battery pack voltages are presented. For the tests with a 380 V battery pack, the shape of the curve is very similar for both topologies. In other hand, for 320 V tests the efficiency of the HFLMC starts to decrease for load levels above 50 % due to high currents flowing through the power switches. A practical solution for this problem should be the use of

multiple switches in parallel. A trade-off must be found between the cost increase in the additional switches and the consequent reduction in costs related to heat dissipation.

From these results should be pointed out that the matrix converter has a higher potential for this application, but the efficiency must be improved to result in a compact device. In the next developments, soft-switching will be explored in order to reduce the losses in the power switches. Furthermore, the application of different switching patterns in the modulation to reduce the number of commutations will be also topic for future research. Moreover, the power loss models will be further improved and also the magnetic components will be optimized to obtain a complete design for physical implementation.

Curriculum Vitae

Personal Details

Name	Diogo André Cerqueira Pinto Bezerra Varajão
Date of Birth	21th December 1988
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Education

1995 – 1999	Primary School, Escola Primária da Correlhã
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2001 – 2004	Middle School, E. B. 2, 3 da Correlhã
2004 – 2007	Secondary School, Escola Secundária de Ponte de Lima

University

2007 – 2010	B.Sc. in Electrical and Computer Engineering, Faculty of Engineering of the University of Porto (FEUP)
2010 – 2012	M.Sc. in Electrical and Computer Engineering – Power Electronics, FEUP
2013 – 2018	Ph.D. in Electrical and Computer Engineering, FEUP

Work

2013 – 2014	Invited Assistant Professor, FEUP
2011 – 2017	Research Fellow, INESC TEC
2017 – 2018	Head of Research and Development (R&D), AddVolt S.A.

Awards

2011 – 2012	Scientific Initiation Scholarship, INESC TEC
2012	Best Presentation at IECON'12 Conference, IEEE
2013	ABB Award 2013, ABB Portugal
2013 – 2017	Ph.D. Research Scholarship, FCT – Portuguese Science and Technology Foundation
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