FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO

Isolated and Bidirectional DC-DC Converter for Electric Vehicles

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Abstract

Nowadays, the demand for electric vehicles has grown at a rapid pace, and to meet this need and due to the environmental constraints, the power electronics fields has continuously looked for innovative solutions to make conversion systems lighter and compact. DC-DC bidirectional converter topology is an excellent example of an interface between two DC bus and is typically found in electrical vehicle storage systems.

With the premises mentioned early, a DC-DC converter is required for this dissertation project to controls the power transfer in both directions with the best efficiency and the lowest volume. In this way, emerging semiconductor technologies will be analyzed as well as the feasibility of bringing these components into the conversion system. In the first part, a converter topology in the power electronics field is presented with the purpose of studying, selecting and implementing a DC-DC converter with high power density for application in electric vehicles. State of the art presents the research and comparison between different DC-DC converter topologies and with focus on the isolated dual-active-bridge (DAB) and respective modulation techniques that allow to enhance efficiency and make the converter more compact and lighter, highlighting the inherent advantages and limitations of each one.

The DAB topology is analytically studied and modeled by a detailed model that includes the major power losses. Closed-loop control is design for the DAB converter supported by a detailed model transfer function. Market research of semiconductors using silicon carbide technology is shown. The efficiency of the DAB converter at different switching frequencies, from 40 kHz to 80 kHz is presented. A gate driver circuit was designed to drive a half bridge structure, and the board circuit schematic is presented.

Keywords – Dual-active-bridge, bidirectional and isolated DC-DC converter, high-frequency transformer, thermal model for semiconductor, Silicon Carbide MOSFET.

Resumo

Atualmente, a procura por veículos elétricos tem crescido a um ritmo acelerado, e de forma a responder a essa necessidade e devido às restrições ambientais, a área da eletrónica de potência tem procurado continuamente soluções inovadoras para tornar os sistemas de conversão mais leves e compactos. Os conversores bidirecionais DC-DC são um bom exemplo de topologia que serve de interface bidirecional entre dois barramentos, e é tipicamente encontrada em sistemas de armazenamento de veículos elétricos.

Com as premissas mencionadas atrás, para o trabalho desta dissertação é requerido um conversor DC-DC que controle a transferência de energia nos dois sentidos com a melhor eficiência e no menor volume. Desta forma, semicondutores com tecnologia emergente serão analisados, assim como a viabilidade de trazer estes componentes para o sistema de conversão. O documento apresenta numa primeira parte o estudo de topologias de conversores DC-DC existentes na área da eletrónica de potência com o objetivo de estudar, selecionar e implementar um conversor DC-DC com elevada densidade de potência para aplicação em veículos elétricos. O estado da arte apresenta a pesquisa e comparação entre topologias de conversores bidirecionais DC-DC dando especial atenção foco ao conversor isolado de dupla ponte (DAB) com componentes ativos e as respetivas técnicas de modulação, onde são analisadas com vista a melhorar a eficiência de conversão, realçando as vantagens e limitações inerentes das mesmas.

A topologia DAB é estudada analiticamente e modelada através de um modelo detalhado que inclui as perdas de potência gerais. Um controlo em malha fechada é desenvolvido para o conversor DAB com o auxílio da função de transferência do modelo detalhado. O estudo de mercado de semicondutores com a tecnologia carboneto de silício é apresentado. A eficiência do conversor DAB obtida para diferentes frequências de comutação, de 40 kHz a 80 kHz é apresentada. Um circuito de driver foi projetado para comandar uma estrutura de meia ponte, e o esquema do circuito é apresentado.

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Abbreviation and symbols

Lists of abbreviations

AC	Alternating Current
AWG	Standardized American Winding Gauge
DAB	Dual-Active-Bridge
DC	Direct Current
DPS	Dual Phase-Shift modulation
SPS	Single Phase-Shift
Eoff/Eon	Switching turn-off or turn on losses respective
EMI	Electromagnetic interference
EV	Electric Vehicle
FFT	Fast Fourier Transformer
GaN	Gallium Nitride
HF	High Frequency
IBDC	Isolated Bidirectional DC Converter
IEC	International Electrotechnical Commission
Llk	Leakage Inductance
PCB	Printed Circuit Board
PFC	Power Factor Correction
PSM	Phase-Shift modulation
Rth.TIM	Thermal Interface Material Resistance
Rth.ch	Heatsink Thermal Resistance
Rth.jc	Junction to Case Thermal Resistance
Si	Silicon element
SiC	Silicon Carbide element
SPS	Single Phase-Shift (same as PSM)
TRM	Triangular modulation

TZM	Trapezoidal modulation
Ths	Heatsink temperature
Tj	Junction Temperature
UPS	Uninterrupted Power Supply
ZCS	Zero-Current-Switching
ZVS	Zero-Voltage-Switching

Lists of symbols

A	Ampere
A_c	Cross-sectional area of the magnetic core
Aw	Conductor Cross-sectional Area
B	flux density
B_{max}	Maximun Flux Density
B_{sat}	Saturation Flux Density
δ	Phase-shift in radians
D_1	Phase-shift of diagonal switches normalized
D_2	Phase-shift between two output voltage of H-bridge at transformer side
f_{SW}	Switching frequency
Hz	Hertz
H_c	Coercive force
J	Current Density
ℓ_c	Magnetics path length core
L_m	Magnetizing inductance
N	Turn ratio
n_{pri}	Number of turns in the primary side
P_{cu}	Copper or winding losses
P_c, P_{fe}	Core losses
$\mathcal{R}$	Electromotive force
V	Volt
V_{Batt}	Voltage across the battery
V_{DC}	DC-link voltage
$\mu 0$	free air permeability
μr	relative permeability
ρ_W	Electrical Resistivity
w	Angular frequency (rad/s)

Chapter 1

Introduction

In this chapter, the motivation and main goals of this dissertation theme are presented. The chapter begins with a presentation of the proposed dissertation, followed by a description of objectives to be achieved and finally the structure of the document.

1.1. Motivation

Nowadays the demand for electric vehicles is growing and has been a challenge for the power electronics field that needs to be continuously looking for innovative solutions in order to make more compact and robust converters with the best efficiency.

Since the beginning of this century, the transportation systems are continually changing and innovating. Especially in cities, the electrification of transports is a priority issue due to high pollution levels and noise. This topic has been discussed, and there are some companies that seek innovation in this sector, as Mercedes-Bens which intends to have an electric version of each car model until 2022 [1]. Countries are concerned in reducing emissions, and it is consensual the adoption of electrical vehicles: e.g., France has the plan to ban the sale of cars with internal combustion engines – conventional engines – until 2040 [2]. Norway is more ambitious and pretends in 2025 sell only electric vehicles.

AddVolt is a Portuguese company who developed a solution targeted to reduce fuel consumption, noise and pollutant emissions in heavy duty vehicles. This technology allows recovering energy during braking or deceleration by installing an electrical generator in the truck. The generated energy is stored in a battery pack and then used to power a secondary electrical system

that is responsible for the refrigeration of "goods". This solution is mainly focused on the refrigerated transportation sector, where the traditional diesel motor is used to power the refrigeration system. A reduction of CO_2 and noise levels are expected along with reduced maintenance.

Increasingly, the population's awareness and political pressures have led to the adoption of renewable energies and this has changed for example the way we move, with the adoption of electric vehicles. Power electronics play an important role, in particular with DC-DC bidirectional power converters in various applications ranging, as the electric vehicle chargers. The interface between the electrical generator, the battery pack, and the secondary electrical system is implemented by power electronics converters. Bidirectional AC-DC and DC-DC conversion stages are required to control the power flow in both direction and to make that, with high efficiency, an advantage technique modulation is approached.

Therefore, the study of this dissertation has the objective of improving the prototype of bidirectional DC-DC converter already used in the company, making it more compact and lighter.

1.2. Power converter system

The power electronics converters are essential components for the electrical system of the truck. The purpose of energy converters is to convert electrical energy from one form to another in an appropriate manner, AC-DC, DC-DC, or just by changing the voltage or frequency level, which ultimately can result in a combination of these.

1.2.1. The power density

When a power converter is required to increase the power rate, the intrinsic components, mainly the passive filters, they are usually large due to the high current which must be archived. The power losses increase when a converter is working in high current. The high switching frequencies bring other issues regarding the electromagnetic interference (EMI), and the EMI filters will be larger to face this situation. With the reason presented before, it is difficult to increase the power rate per volume of equipment. The converter power density is a metric of power per mass/volume, and it is limited by the component sizes. Therefore, it is a challenge for design engineers to find solutions which allow to improve and make the converter with high power density and the best efficiency.

1.2.2. Standards and regulation

The respective standard regulations applicable to the mode of operation of the isolated DC-DC converter are summarized:

- IEC 61800-3:2017: EMC requirements and specific test methods;
- IEC 61800-5-1:2007: Safety requirements - Electrical, thermal and energy.

These standards are applicable to this type of system and they are the same as those applied to the adjustable speed power drive systems.

1.2.3. Requirements and specifications

The specifications and main requirements for the bidirectional and isolated DC-DC converter are listed in Table 1.

Table 1 – Specifications and main requirements.

Secondary voltage, battery side (OPT1)	200-450 V
Secondary voltage, battery side (OPT2)	120-175 V
Primary voltage, DC-link side (OPT1)	700 V
Primary voltage, DC-link side (OPT2)	400 V
Maximum output power	22.1 kW
Galvanic isolation	Yes
Bidirectional power flow	Yes
Power density	$\geq$ 2.0 kW/l
Overvoltage and overcurrent protection	Yes
Cooling	Air cooling

This converter is intended to be used with three-phase and single-phase inverters. Therefore, and in order to obtain a versatile conversion system, two different operating ranges for the battery and inverter sides are considered depending if the system is working in a three-phase (OPT1) or single-phase (OPT2) configuration. The battery pack for three-phase configuration ranges from 200 to 450 V. In turn, the voltage should be controlled in the 120 to 175V range for single-phase systems. A galvanic isolation between two DC bus is a mandatory requirement. The DC-link voltage in three-phase configuration is settled at 700 V, while for single-phase configurations 400V are used.

1.3. Research goals and contributions

The power electronics have been growing for the past few decades due to industrial demand, so making systems more compact, more efficient and more robust has become determinant for the industry. Many counties are concerned with the environmental pollution, and it has become a central trigger for engineers to find new technologies, in order to enable the use of clean and sustainable energies in a more efficient way. Gallium Nitride (GaN) and Silicon Carbide (SiC) materials are the example of recent tecnologies which can enable this. During many years, the Silicon (Si)-based semiconductors were largely used as the leading solution for power application due to its well known mature technology and their low cost. However Si-based semiconductors have limited switching frequency operation which is not suitable for high power applications where high power density is required. A brief overview of that material will be presented in the next chapter, emphasizing their characteristics and advantages.

The main objective is to design and implement an isolated high-power density bidirectional dc-dc converter, improving the existing prototype in the company. An overview of bidirectional dc-dc converter topologies is presented in state of the art as well as the main modulation techniques. The mathematical model of the converter is also an essential design requirement for performing closed-loop simulations which allows a better approximation of the system to be implemented. The simulations are performed in a graphical environment via GeckoCIRCUITS® that will enable to support and validate the theoretical study.

Considering this, it is presented below a list of the specific primary goals of the dissertation:

- Revision of the state of the art of bidirectional and isolated dc-dc converters (IBDC);
- A detail analysis of dual-active-bridge (DAB) topology.
- The study and comparison of the most used modulation methods for the DAB
  - Phase shift modulation
  - Dual phase-shift modulation
  - Trapezoidal modulation
  - Frequency modulation
- Simulation in GeckoCIRCUITS® software of DAB topology operating with the selected modulation,
- Design and implementation of the bidirectional and isolated dc-dc converter responsible for the interface between the battery pack and the DC link coupled at the inverter side.
- It is expected to have experimental result in open-loop and closed-loop operating modes.

1.4. Structure of the Document

The first chapter presents the main objectives of the dissertation. Emphasis is given to power converters and their importance in electronic systems is explained. The converter requirements are also presented.

The second chapter focusses in the literature review of isolated and bidirectional dc-dc converter topologies. A review of the common and advanced modulation techniques used in DAB converters is done. Advantages and disadvantages are highlighted.

The chapter 3 demonstrates the mathematical model of the converter and the entire modeling process is documented, followed by component design, control design, and simulation in open-loop and the closed-loop mode of operation. A thermal model for power semiconductors is presented in order to estimate the temperature and losses in the active components.

Chapter 4 covers the research of available power semiconductors with SiC technology. Main considerations for driving circuit, the isolation between the low and high side of the driver is presented. A design of a circuit to a half bridge with SiC MOSFETs are presented and explained the main stage of the implementation. At the end of the chapter, a DAB solution is presented, and include active and passive components chosen.

The final chapter 5 make an overview of the project and suggestion for future works.

Chapter 2

State of the Art

This chapter presents the revision of different topologies of power converters for isolated bidirectional DC converter and manly comparison between those topologies with the soft switching operation.

2.1. Review of isolated and bidirectional DC-DC converters

In the present section, the isolated and bidirectional DC-DC topologies that result from research and study based on literature support are presented. The advantages and disadvantage of those topologies are also discussed.

A review of IBDC topologies are presented in [3] and the classification is based on the number of switches that are used in the circuit. As shown in Table 2, there are a considerable number of topologies of IBDC with a different configuration. The typically single DAB has eight switches and compares to the four-switches topology like dual-half-bridge. In turn, the DAB has the double of power capacity and the current stress is half of each transistor. This is a great feature in using DAB tropology for high power application. The ripple frequency for push-pull, half-bridge and full-bridge converters is two times high than the switching frequency.

Table 2 Classification of IBDC Topology based on the number of switched [3].

Classification	Dual-switches	Three-switch	Four-switch	Five-switch	Six-switch	Eight-switch
Typical models	dual-flyback, dual-Cuk, Zeta-Sepic	forward-flyback	dual-push-pull, push-pull-forward, push-pull-flyback, dual-half-bridge	full-bridge-forward	half-full-bridge	dual-active-bridge

2.1.1. Dual-Active-Bridge (DAB)

Most recent years, the technological advancements in power devices and magnetic materials (mainly good results obtained in use silicon carbide – SiC – and gallium-nitride – GaN – material on power device) have made DAB-IBDC viable for eliminating bulky and heavy LF transformers from power conversion systems [3].

The topology shows in Figure 2.1 is known as single dual-active-bridge. The DAB was firstly introduced in 1991 [4] for high-power applications. The present circuit has two full bridge with H configuration and a voltage V_{DC} and V_{Batt} are applied to the first and second output side of respective H-bridge. The two bridges are coupled with a high-frequency transformer and this is an important component in the circuit since provides a galvanic isolation between the battery pack and the inverter. Moreover, a high-frequency operation allows to reduce the size of the transformer, so it's less bulky and heavy compared to the low-frequency transformer, also known as line-frequency transformer. The leakage inductance is a characteristic of the transformer for store and transfer energy.

The transfer of energy is obtained by changing the angle of phase between primary and secondary voltages applied to the transformer or varying the duty-cycle to obtain the desired power flow. More detail for the operation mode of DAB with soft-switching will be presented in section 2.3. along with other modulation techniques.

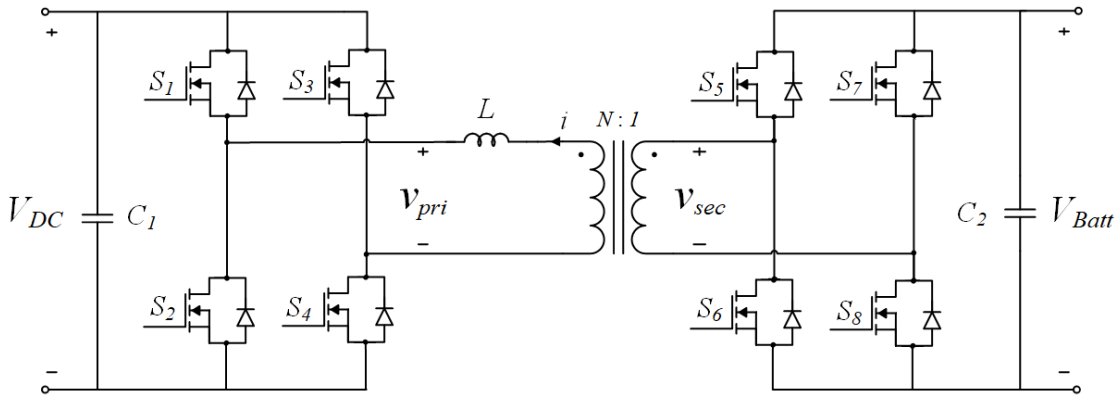


Figure 2.1 - Bidirectional and isolated dual-active bridge dc-dc converter.

2.1.2. Three-phase dual-active-bridge

Certain applications require high power capacity, and in this way, multiphase converters are used. The simple three-phase DAB configuration is shown in

Figure 2.2. The first topology of a bidirectional DC-DC converter operating as three-phase dual-active-bridge was implemented in 1991 [4] and the AC three-phase transformer has a YY structure and the leakage inductance L_{lk} in each phase represented in the

Figure 2.2 was used as the energy transfer element.

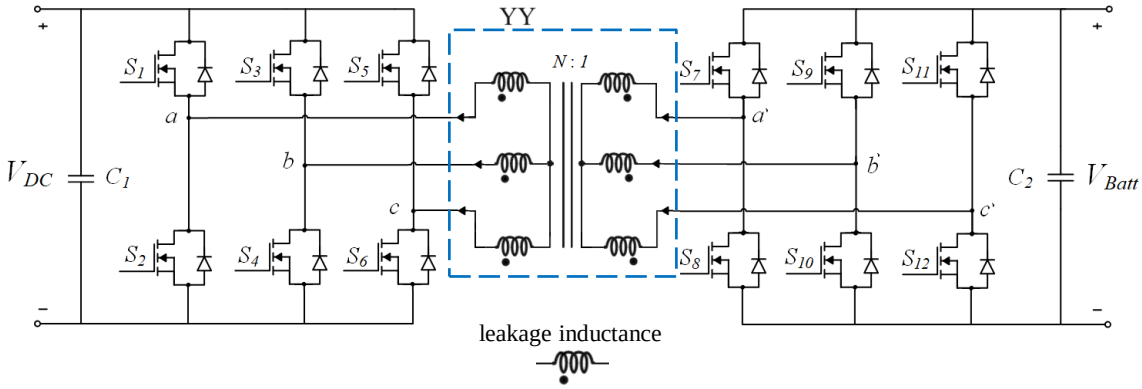


Figure 2.2 - Three-phase DAB-isolated bidirectional DC-DC converter, topology adapted from [4].

This circuit allows the energy transit in both directions, like the single DAB, between two inverting three-phase bridges through the phase-shift modulation. The switching signals for the transistors have a 50% duty cycle. An overview of the comparison between single-phase and three-phase DAB-IBD is shown in Table 3 for an application of a power transmission at 50 kW, with a V_{Batt} = 200 V and output voltage of V_{DC} = 2000 V. The values for the main variables resulted from the equations and curves presented in [4].

Table 3 - Comparison of single-phase and three-phase DAB-IBDC [3].

Converter	Number of switches	Peak current A	Peak voltage V	Transformer kVA	Cap RMS current/ A
Single-phase	8	297.6	2000	56.3	12.9
Three-phase	12	293.5	2000	55.7	4.8

With the analysis of Table 3, the transistors of the 3-phase converter topology have a slight reduction of current stress when compared with the single-phase topology, in column three of the table. Thus, for the same nominal voltage, the current per phase is smaller in the three-phase topology for each switch. Another feature is the ripple frequency in the DC-link current, secondary side, it is three times the switching frequency instead of the double frequency on single DAB topologies. The total number of active devices – twelve transistors – is a disadvantage in the bidirectional three-phase converter, so more power and devices are required that increase the size and price for this circuit topology. Another disadvantage is the complex structure that not make possible building a three-phase symmetrical transformer with identical leakage inductances in each phase [3].

2.1.3. Series resonant DAB

In Figure 2.3**,** the series resonant *LC*-type topology is shown. The circuit consists of a resonant tank formed by an inductor and an additional capacitor, which is the main difference compared to the single DAB converter configuration. Both the magnetic elements present in the system, inductor and capacitor, as well as the high-frequency transformer, are responsible for the energy transfer through the front-to-front converter.

Like the traditional dual-active-bridge approached described in subsection 2.1.1 it is possible to operate the *LC*-type with higher frequency and efficiency due to their advantages of operation [3]. A single-phase-shift modulation method is proposed in [5] to control the resonant series DAB converter. The active power is controlled by the only one adjustable degree of freedom– the phase-shift between the secondary and primary voltage of the high-frequency transformer. The transistors on the two H-bridges are driven with 50% duty cycle under the traditional phase-shift. For wide changes in load or supply voltage, all switches of both bridges of converter may work in zero-voltage-switching (ZVS) or zero-current-switching (ZCS) [5] renewable generation systems. The ZVS could be implemented for primary side switches and ZCS for secondary side switches [3], when the power flow is done from the primary bridge (rectifier bridge) into the secondary bridge (rectifier).

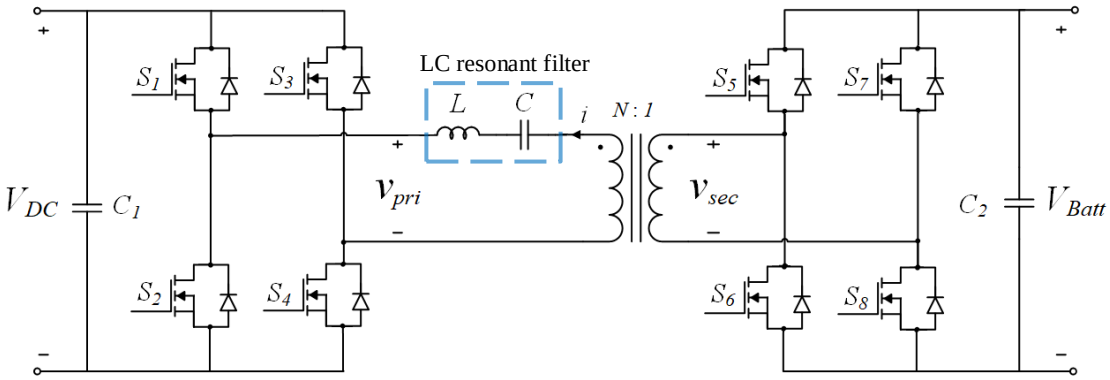


Figure 2.3 – Series resonant DAB isolated and bidirectional dc-dc converter [5].

The two IBDC topology analyzed in section 2.1.1 e 2.1.2 have intrinsic electromagnetic interference (EMI) created by rectangular waveforms of voltages which crossed through winding on both sides of the HF transformer. The EMI levels impose limits on the sizing of magnetic components, and a simple increase of switching frequency of devices to compensate that limitation is not seen as a viable solution since the switching losses increase.

The topology in Figure 2.3 has the disadvantage of being constituted by additional resonant elements compared to the traditional DAB topology, which results in increased cost and size.

2.1.4. CLLC-DAB

The dual-active-bridge with CLLC resonant tank has “high power density, high efficiency, buck/boost capability, and controllable bidirectional power transfer” [6]. These advantages make the converter a candidate for the implementation of bidirectional charging systems in hybrid and electric vehicles. An example of bidirectional resonant converter for battery charger application is presented in [7].

The DAB with a series-parallel CLLC tank resonant was proposed in [8] and a detail principal operation is also presented. The power transit in both directions is guaranteed by a variable frequency modulation. Looking to the Figure 2.4, in forward mode, the switches of the second bridge (been an inverter for this operation mode) are driven by 50% of the duty cycle in order to generate AC power, and the switches of the first bridge (rectifier) are turned OFF and the transferred power is rectified by the antiparallel diodes of the power switches [3]. The circuit structure is illustrated in Figure 2.4.

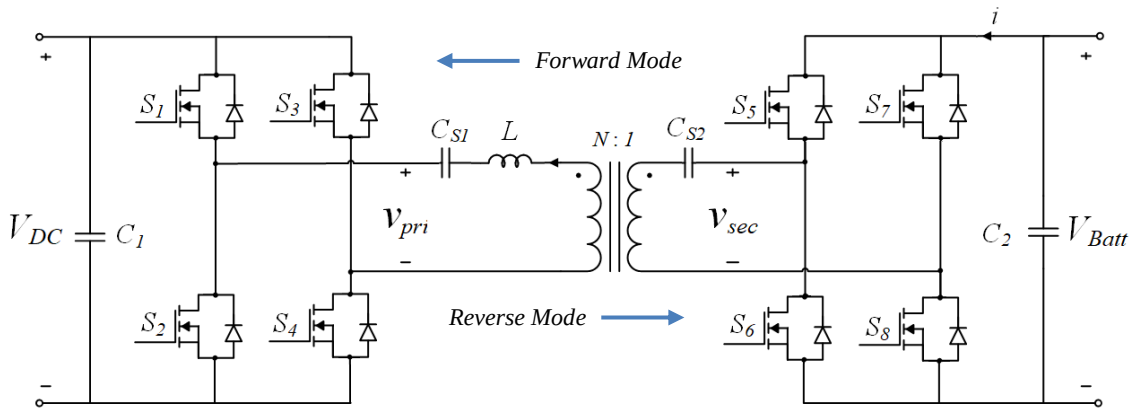


Figure 2.4 - Bidirectional and isolated full-bridge CLLC, adapted from [8].

The converter represented in Figure 2.4 is an asymmetric resonant bidirectional converter. The resonant network is represented by C_{s1} and inductance L in primary side and C_{s2} in the secondary side of the transformer. A soft-switching is implemented to eliminate the switching losses and reducing the electromagnetic interference [8]. When the converter operate in forward mode, the soft-switching is done in two ways by the zero-voltage-switching (ZVS) operation for the inverting stage (second bridge), and by the zero-current-switching (ZCS) operation of the rectifier side, at the first bridge [8]. The ZVS can be implemented in the MOSFETS semiconductors if the frequency of operation of the drive is performed below the resonant frequency. This imposed condition limits the sizing of the elements of the resonant tank. The detailed analysis of the mode of operation with soft-switching technique is presented in the literature [3, 6, 8].

2.1.5. Comparison of different topologies operated with soft-switching

In all section 2.1. the mainly isolated and bidirectional topologies DC-DC along with the analysis of structure and operation with a soft-switching mode for each one was presented.

By the analysis of Table 4 is verified that for different topologies studied in previous sections, different control strategies are required. The soft-switching region of the CLLC topology is wider compared to the other DAB circuits particularly at light load conditions [6]. For the resonant topologies, series resonant and CLLC-DAB asymmetric, the control computing times increase due to the complexity of the converter that is a result of increasing system order [9]. The frequency modulation implemented in CLLC resonant converters increase the control complexity and this topology requires more resonant elements that increase the size and the cost of all converter [3]. In relation to the three-phase DAB, from the view of the filter, the frequency ripple of input/output voltage and current are three times higher than the switching frequency [10] and this is an advantage in terms of the size of the filter since the filter value is smaller due to the imposed high-frequency.

Table 4 Comparison of various topologies operated with soft-switching. Conclusion based on [4]

Converter	**Resonant network element**	**Power control**	**Drive**	**Soft-switching characterization**	**Soft-switching range**	**Frequency output**	**Bidirectional transition speed**	**Complexity of implementation**
Dual-active Bridge	No	Phase-shift modulation	All switches are driven by 50% of duty-cycle	ZVS for few switches	Narrow	Double	Fast	low
Three-phase DAB	No	Phase-shift modulation	All switches are driven by 50% of duty-cycle	ZVS for primary switches, ZCS for secondary switches	Narrow	Triple	Fast	average
Series resonant DAB	Series resonant tank	Phase-shift modulation	All switches are driven by 50% of duty-cycle	ZVS for inverter switches, ZCS for rectifier switches	Narrow	Double	Fast	average
CLLC-DAB symmetric resonant	Series resonant tank	Frequency modulation	50% of duty-cycle for inverter switches, turn off for rectifier switches	ZVS for inverter switches, soft commutation for rectifier switches	Wide	Double	Slow	high

2.2. Dual active bridge topology

In the present section, the configuration of the DAB converter and the basic principal operation will be discussed.

This topology for bidirectional isolated DC-DC converter was presented in 1991 [4] for high-power-density power converters. In the right side of the circuit, a battery pack is connected to the dc-dc converter. As discussed in topic 2.1.1 the main circuit consists of a two single-phase voltage source inverter connected by a high-frequency transformer that provides galvanic isolation. The link-inductor allows controlling the power flow in both directions between the battery and the DC-link that interfaces the inverter. Another feature of this topology is that the converter can also be operated in boost and buck mode. L represents the link-inductor and the V_{DC} is the voltage at the inverter, from the left side, that should be kept constant at the rated value. Figure 2.5 represents a simple DC-DC converter configuration, which is expected to be implemented with the elaboration of this dissertation.

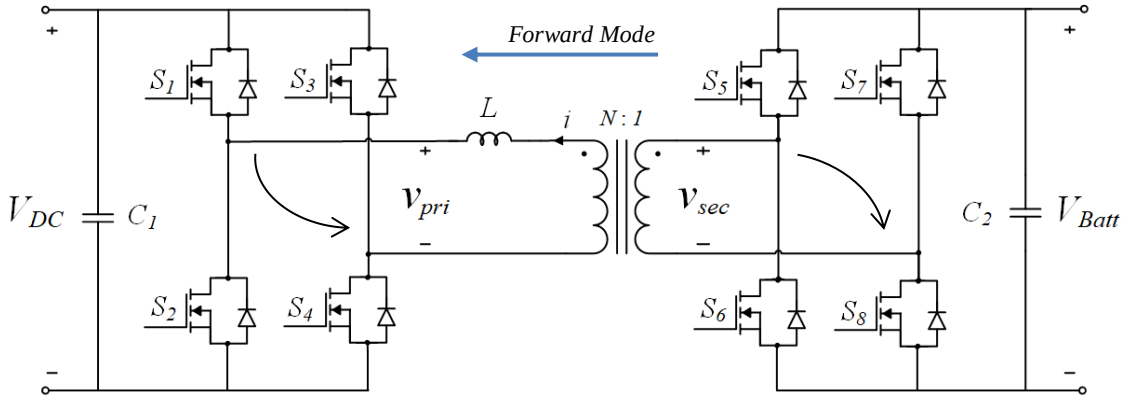


Figure 2.5 - Single-phase dual active bridge topology for IBDC converter.

Two modes of operation with a soft-switching modulation can be defined:

- Forward-mode: when the battery pack is discharging
- Reverse mode: when the battery pack is charging

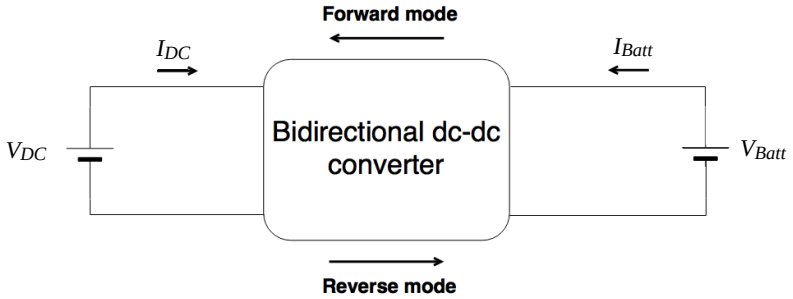


Figure 2.6 - Forward mode $I_{Batt} > 0$ and $I_{DC} < 0$. Reverse mode $I_{Batt} < 0$ and $I_{DC} > 0$.

Due to the considerable number of semiconductors in this topology, it is required implementation of strategies to reduce the commutation losses, namely the zero-voltage-switching (ZVS) and zero-current-switching (ZCS) technique. The ZVS allow to eliminate losses during turn ON transition, however the switching losses during turn OFF still be occurred on semiconductor switched [11], while ZCS is used to eliminate the losses when the switch turns OFF and reduce the losses when the switch turns ON.

The dual active bridge has advantages of "high power density, zero-voltage switching (ZVS), bidirectional power transfer capability, a modular and symmetric structure, and simple control requirements." [12].

The next section provides an overview of the main known modulation techniques. A detailed analysis for each of the control techniques will be presented.

2.3. Modulations for the DAB

For the topologies previously presented, the implementation of a control method is a requirement to control the amount of energy circulating in both directions and that bidirectional flow of energy is achieved through modulation techniques. This section will introduce and analyze some of the most used modulation methods on dual active bridge topologies.

2.3.1. Phase-shift modulation

The traditional and standard method for command the dual-active-bridge consists in control all transistors of both bridges through the single phase-shift. The diagonal transistors pairs are simultaneously switched with 50% of duty-cycle and the other complemented transistors in the same bridge with also 50% duty-cycle ratio but with 180 degrees of phase-shift. Providing a quasi-square waveform of high-frequency across the terminal of the external inductor *L* and the secondary transformer side. To control the power flow between two bridge/inverters, in other words, the direction and magnitude of current in the external inductor *L* is controlled by regulating the phase-shift ratio – D normalized - of two square waveforms, v_{pri} e v_{sec}, generated by the respective bridges. The power flow is described by the following mathematical equation (2.1), first introduced in 1992 [13], and the losses are neglected:

$$P_{PSM} = \frac{NV_{Batt}V_{DC}}{8F_S L} D(2 - |D|) \tag{2.1}$$

When D = 1, corresponding to the phase-shift maximum between the square voltage v_{pri} and v_{sec} possible in DAB under PSM to transfer power.

In equation (2.1) the V_{DC} and V_{Batt} represent the amplitude of the primary and secondary voltage applied to both output sides of H-bridges respectively, wherein the DC-link bus is primary voltage and the battery side is the secondary voltage. The F_S is the frequency that transistors on inverters/bridge are commuted, the N is the transformer turns ratio and at last L could be the leakage inductance of the transformer, if the transformer is designed to have a desired leakage inductance to meet the requirements by applying the traditional phase-shift, or an external inductor. Considering the L an external inductor coupled to the primary of the transformer, this element is the most important parameter in power circuit for energy transfer, therefore its dimensioning is crucial to make converter operate in the desired power range. The L could also be represented by the sum of the external impedance and the intrinsic transformer leakage inductance. More later in Chapter 3 the converter design will be discussed.

The single DAB is operated in a two-level waveform with the control technique presented in this topic. The resulted of single phase-shift is shown in Figure 2.7, adapted from [14], were the main ideal waveforms are presented.

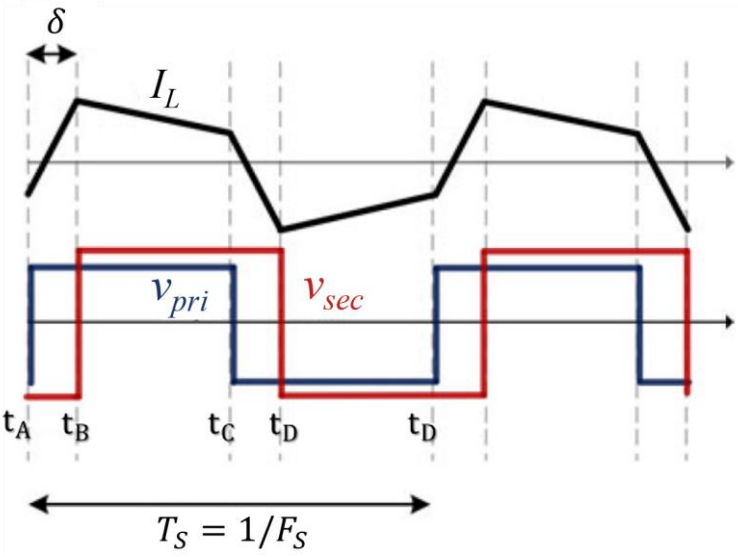


Figure 2.7 - Idealized operating waveforms of the DAB converter (i_L, v_{pri} and v_{pri}), and v_{pri} lead v_{sec}.

Where is observed in Figure 2.7 the voltage v_{pri} lead the voltage v_{sec} and the power flow from the DC-link side (V_{DC}) to the battery side (V_{Batt}). When the v_{pri} is positive and the v_{sec} negative, between t_A and t_B, the i_L is increasing. During the next time segment $t_B \leq t \leq t_C$ the current i_{lk} starts decreasing once the v_{sec} is higher than v_{pri}.

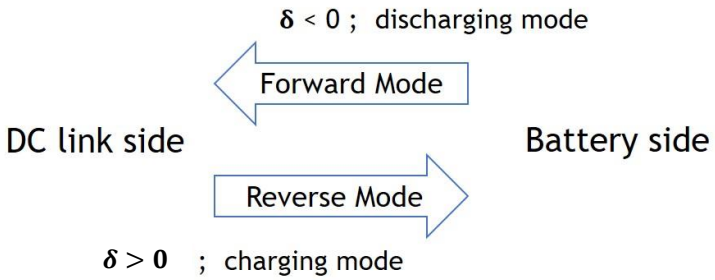


Figure 2.8 - Simplest diagram of power flow on DAB-IBDC converter with phase-shift modulation. Arrows indicate the direction of energy flow in the converter.

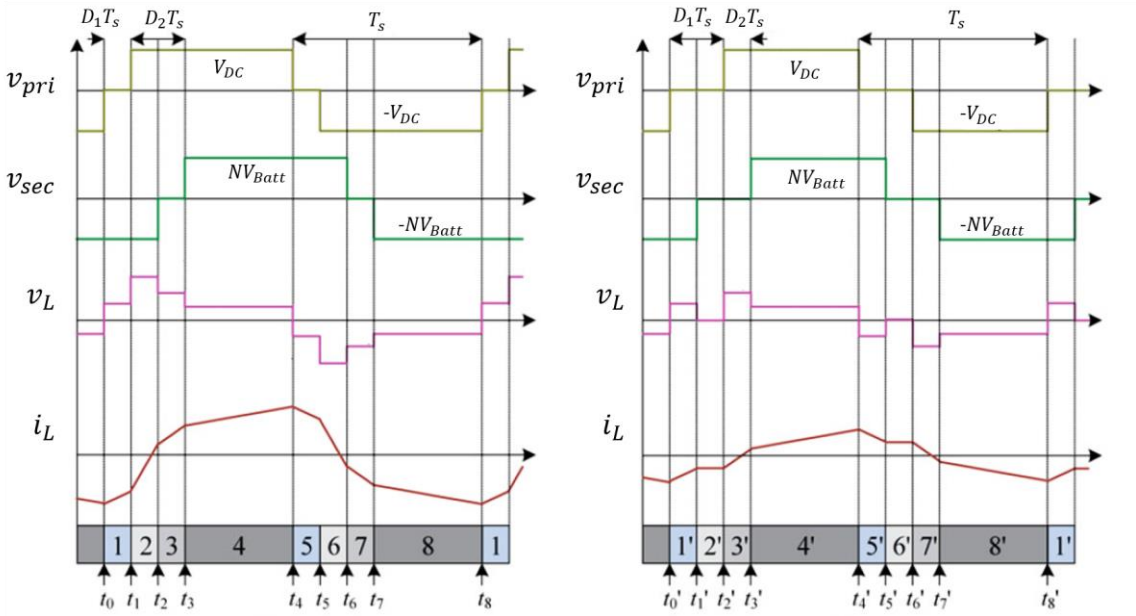
With the support of diagram from Figure 2.8, for the battery be in charging mode the phase-shift must be higher than zero, assume a positive value. In this scenario, the voltage v_{pri} lead behind v_{sec}. The battery is in discharging mode when phase-shift between primary voltage and secondary voltage of HF transformer is negative. Therefore, v_{pri} has a lag in relation to the v_{sec}. Summarily the power flow in dc-dc converter from the bridge with square voltage in the lead to the bridge with a square voltage in lag, in such way, the bidirectionality is achieved due to the phase-shift concept. The soft-switching is a technique commonly used in the DC-DC converter to make high efficiency resulting from the reduction of switching losses.

With this phase-shift modulation, the power flow through the leakage inductance depends on its value. There is a significant circulating power when the voltage amplitude of two sides of the transformer is not matched, then both the RMS and peak current increase. Moreover, the converter cannot operate under ZVS in the whole power range in this situation. Therefore, the power loss becomes much higher, and its efficiency is significantly reduced. [3].

2.3.2. Dual-phase-shift modulation

With the dual-phase-shift (DPS) technique there are two ways to control the power flow. The direction and magnitude of current are controlled by adjusting the phase-shift between transformer primary and secondary square voltage and also the phase-shift between the gate signals of the diagonal switches of each bridge. This control concept of dual phase-shift was presented in [15] with a two degree of freedom to control the system, one by adjusting the outer-phase-shift (D_2) between v_{pri} and v_{sec} that is the same parameter adjusted in traditional single phase-shift, and the other by shifting gate signals of diagonal semiconductors, e.g., introducing a phase-shift (D_1) between S1 and S4 gate signal in first H-bridge represented in Figure 2.5, also designed inner-phase-shift. The algorithm proposed for DPS can decrease peak current, reducing the losses and increasing the system efficiency. Also eliminates reactive power that circulates in the power transformer, increase power capability, and minimize the output capacitance [15].

Differently from the traditional two-level voltages at the secondary and primary output of the transformer, with the DPS control algorithm, the voltage emerges on three voltage levels, as we can be seen in Figure 2.9 (v_{pri} and v_{sec}), from [16]. The approximated sinusoidal waveform of the current in the external inductor placed in the transformer primary side is one of the advantages of implementing the DPS with the consequent reduction of electromagnetic interference (EMI).



(a) (b)

Figure 2.9 - (a) Ideal waveform of IBDC under DPS in the condition of $0 \leq D_1 \leq D_2 \leq 1$. (b) Ideal waveforms of IBDC under DPS control in the condition of $0 \leq D_2 \leq D_1 \leq 1$ [16].

The output power analysis in the DAB converter with dual phase-shift modulation is expressed by the following equations [16, 17]:

$$0 \leq D_1 \leq D_2 \leq 1 \qquad P_{DPS} = \frac{NV_{Batt}V_{DC}}{4F_SL} \times (2D_2 - 2D_2^2 - D_1^2) \tag{2.2}$$

$$0 \leq D_2 \leq D_1 \leq 1 \qquad P_{DPS} = \frac{NV_{Batt}V_{DC}}{4F_SL} \times (2D_2 - 2D_2D_1 - D_2^2) \tag{2.3}$$

Some considerations:

- The primary or secondary square voltage, v_{pri} or v_{sec} respectively, not have necessarily the same duty-cycle – e.g. constant 50% for one bridge and different ratio for the other bridge. The voltage waveform shown in Figure 2.9 with three-level is responsible for the significantly reduction of reactive power;
- All semiconductor switches are driven with 50% of duty cycle;
- The signal for the diagonal switches in both bridges has a phase-shift of D_1;

- For the traditional phase-shift control only one degree of freedom is adjusted - the phase shift between the primary and secondary voltage of both side of the transformer, v_{pri} and v_{sec} respectively;
- For the same output power there is an infinite combination of two-phase shift, D_1, and D_2;
- From (2.2) and (2.3), the maximum output power in DPS cannot be concluded that is higher than SPS [17];
- "The DPS control can offer wider power transmission range than the SPS control does that will also enhance regulating flexibility" [16];
- "With the same current stress, the DPS control can transfer more power than the SPS control does" [16].

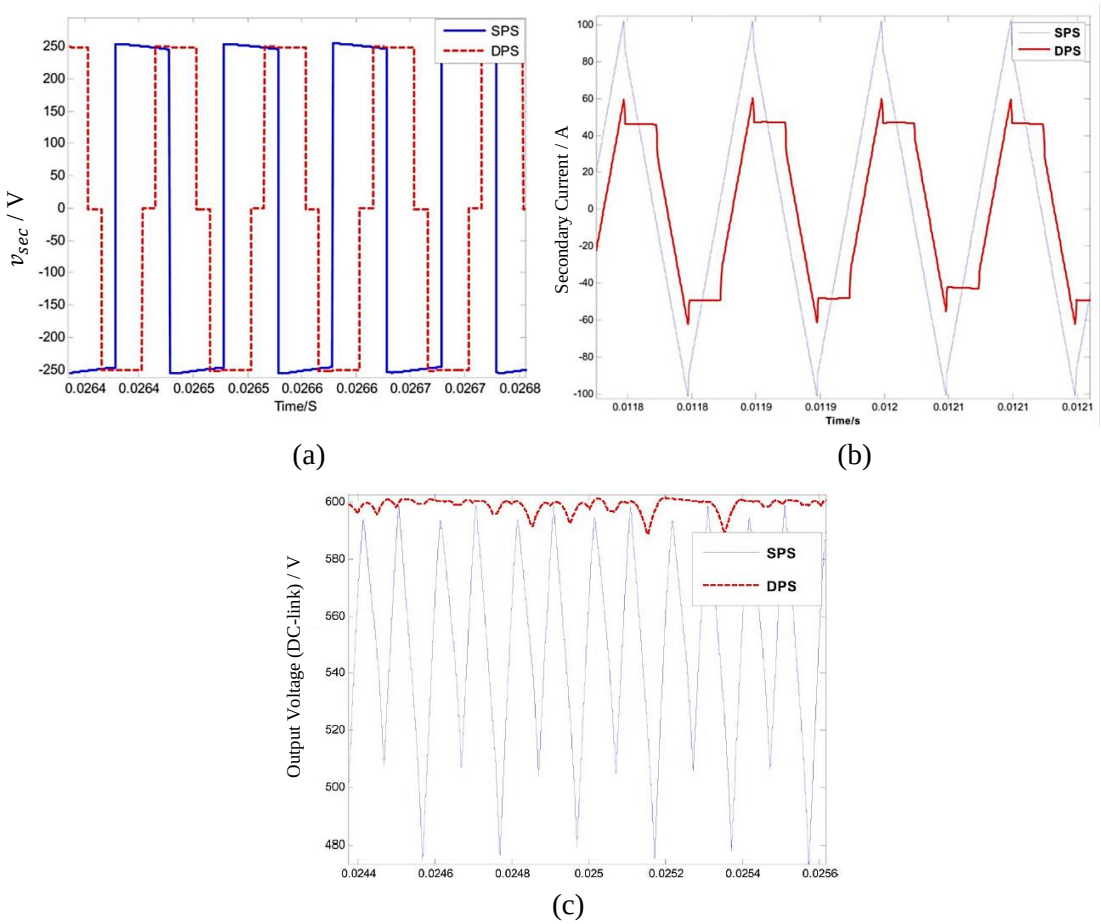


Figure 2.10 – Comparison of control algorithms SPS and DPS. (a) Transformer secondary voltage under SPS and DPS. (b) Primary current resulted by implements SPS and DPS under same output power. (c) Voltage ripple for two control algorithms (same PI parameter, C = 200μF) [15].

Figure 2.10 shows the simulation results of two different control algorithms (SPS and DPS) made by author [15], where the voltage waveform of the transformer secondary side are present

in Figure 2.10 (a). And in the Figure 2.10 (b) is shown the transformer current in the primary side for the two types of control modulation and following the converter topology of Figure 2.1. This result is obtained under the same output power. The output voltage ripple (DC-link side) in DAB converter for two control algorithms is shown in Figure 2.10 (c). With the same parameter of PI controller and the same output power, the author in observed that the peak current of DPS control is much smaller compared to the SPS control. The smaller voltage ripple observed in Figure 2.10 (c) results from the reduced inherent reactive power of using the DPS modulation in the DAB converter.

The authors in [15] also present a detailed analysis of soft-switching of the DPS control only for the operating mode $D_1 \leq D_2 \leq (1 - D_1)$, and it is verified that all the turn-off commutations occur with hard-switching, while zero-current-switching (ZCS) is implemented for all the turn-on actions.

2.3.3. Trapezoidal and triangular modulation

Due to the disadvantage of traditional SPS modulation, another advanced modulation was investigated to improve the efficiency of conversions, such as the triangular and trapezoidal modulation, TRM and TZM respectively.

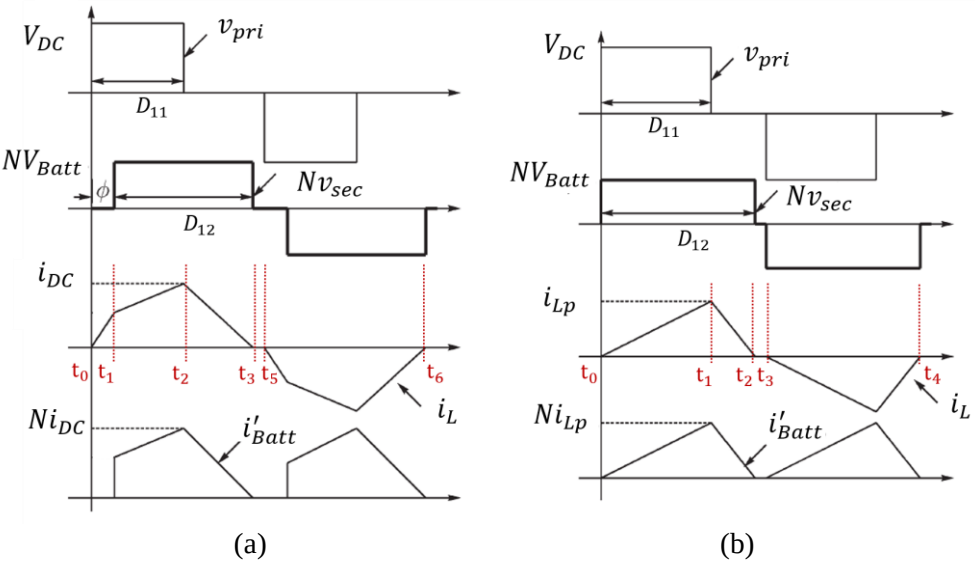
a) Trapezoidal modulation

Different from the conventional PSM, in TZM the duty cycle of the transformer output voltage waveforms, primary and secondary side, (converter topology of Figure 2.5), they are not driven by the same duty cycle. Where it can be seen in Figure 2.11, adapted from [18], the D11 and D12 can be less under 0.5 and also different from each other [18]. The D_{11} and D_{12} on equation (2.4) are the duty rate in p.u., where 1 p.u. represents 360º and when the D_{11} and D_{12} are equal 0.5 p.u., the DAB is modulated under SPS modulation, and the transformer voltage has a square waveform with 50% of the duty cycle and the transferred power is controlled by phase-shift ϕ. In TZM the output power is described by the equation (2.4), adapted from [18]. To convert the phase shift in p.u. into to radians, can be easily made by multiplying it by 2π.

$$P_{TZM} = \frac{V_{DC}}{LF_S}\left(D_{11}^2 V_{DC} - (D_{12} - \phi)^2 N V_{Batt}\right)$$
$$D_{12} = \frac{V_{DC}}{N V_{Batt}} D_{11} \tag{2.4}$$

The waveform of i_L in Figure 2.11 (a) can be observed in four different sequences of time. The transformer current encrease from zero between $t_0 < t < t_1$, in the next time segment $t_1 <$

$t < t_2$ the V_{DC} and NV_{Batt} is applied to the transformer. The indutor current decrease to zero between the segment $t_2 < t < t_3$, and reach the zero in t_4. At instant of time t_0, t_4, t_5 and t_6 the indutor current reaches the zero and ZCS is possible [19], therefore the ZCS occur in four transistor and ZVS for the others four, so the trapazoidal modulation has high efficiency inherent by the soft-switching implementation in some transistors, and also allow high power transfer.



(a) (b)

Figure 2.11 - Ideal waveforms of the two different modulations and the power transit between first H-bridge into second H-bridge. (a) Trapezoidal modulation. (b) Triangular modulation.

b) Triangular modulation

The TRM is investigated in [19] and the transformer voltage v_{pri} and v_{sec} is generate in three level, similar to the DPS presented in section 2.3.2, however the duty rate isn't necessary the same for the signal on two bridge, and this modulation method doesn't consider a phase-shift angle between the two-transformer voltages. The TRM can viewed is a special case of TZM with zero phase-shit, $\phi = 0$. The key waveforms of TRM is shown in Figure 2.12 (adapted from [20]), where V_{DC} and V_{Batt} are the DC-link and battery voltage respectively. The equation (2.5) describe the power transfer under TRM [18] for the operation mode presented in Figure 2.12 (a). The duty cycle D_{11} and D_{12} are in p.u. system and the maximum value in radian correspond to $\pi/2$, when the transformer output voltage has a square waveform with 50% of duty cycle.

$$P_{TRM} = \frac{V_{DC}}{F_S L}\left(D_{11}^2 V_{DC} - (D_{11})^2 N V_{Batt}\right)$$

$$D_{12} = \frac{V_{DC}}{N V_{Batt}} D_{11} \tag{2.5}$$

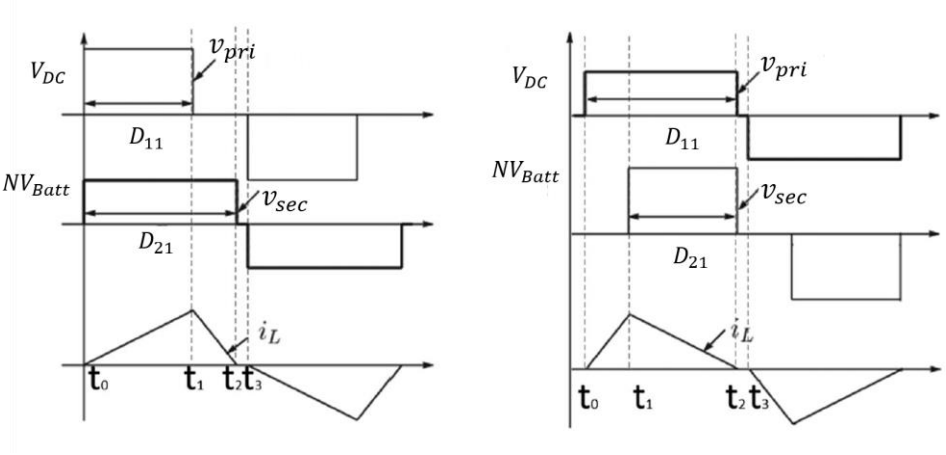


Figure 2.12 - Key waveforms of triangular modulation. (a) TRM when $V_{Batt} > NV_{DC}$. (b) TRM when $V_{DC} < NV_{Batt}$.

For the DAB converter in Figure 2.5, the voltage ratio is defined by NV_{Batt}/V_{DC} and this approach must be considered in implementing the TRM. Even when the input and output voltages are significantly different, $V_{DC} \ll NV_{Batt}$ the TRM method can be implemented [21], however in the case of the $V_{DC} = NV_{Batt}$, the power transfer is not possible.

The waveforms presented in Figure 2.12 (a) are performed by the active device in high voltage side (V_{DC}), while the power transit in low voltage side is ensured by the antiparallel diode, thus there no signal for the low side transistors. In this operation mode $V_{DC} > NV_{Batt}$, the power flows from the high to the low side voltage windings of the transformer.

Different of the phase-shift modulation, change the duty cycle of transistor signals under triangular modulation allow to reduce the reactive transformer power and also reduce the switching losses [21]. The ZCS is possible in this modulation for the high voltage side, in case of the converter operate under the condition shown in Figure 2.12 (a), and it contributes to reducing the switching losses and the EMI. Only two turn-offs occur per period of switching, and they're performed by the same two switches [19]. The complexity of the modulation and the control algorithm is a disadvantage of the triangular and trapezoidal implementation.

The author of [18] was presented a comparison of maximum power transfer capability under traditional, triangular and trapezoidal modulation with a certain parameter, a phase-shift of $\phi = 0.125\ p.u.$ and a duty ratio $D_{11}^{max} = 0.21\ p.u.$ With those settings the PSM has higher maximum power capability compare to the other two modulation, following the relation $P_{max}^{PSM} > P_{max}^{TZM} > P_{max}^{TRM}$.

2.3.4. Frequency Variation

As seen in previous section about others technique modulation, the switching frequency on single PSM is kept constant, and the pairs of transistors are driven with the same duty cycle.

Before the explanation of the variable frequency modulation (VFM), there is some consideration be tanking on DAB: both switching frequency and leakage inductance define the maximum power rating of the converter. The next table shows the following results of changing the switching frequency in a design project; some conclusion was withdrawn from [14]:

Table 5 – Results of changing the F_S from its design value.

Switching frequency	
Decreasing F_S	• increases the power transfer capability; • reduce the magnetization current of the magnetic cores • not executable by the risk of magnetic components saturation;
Increasing F_S	• limits the power transfer capability; • increases of the switching losses and conduction losses

The VFM does not only control the transfer power as it interferes in the design of magnet component. Taken this in mind, the F_S need be varied according to the operating conditions, not only control the transfer power in agreement with project requirements but to reduce the peak currents present in the transformer at lighter loads [22].

Note: $\delta = 2\pi \times \phi$ in radian

$$\phi = \text{sign}(I_{ref})\left(\frac{1}{4} \pm \frac{1}{4}\sqrt{1 - \text{sign}(I_{ref})\frac{8F_S L I_{ref} h_{pri}^{-1}}{NV_{Batt}}}\right) \tag{2.6}$$

The phase-shift signal depending on the reference current signal ($\text{sign}(I_{ref})$). The h_{pri} is a variable that describe the structure of primary H-bridge of Figure 2.5, in this case a full-bridge is represented, and its value is 1. For half-bridge structure the $h_{pri} = 0.5$. The leakage inductance is represented by L. The reference current (I_{ref}) is the primary-side input current. The relation between switching frequency F_S and the reference current is show in follow equation, after change the percentage of switching period (T_s) to radian, $\phi = \delta/2\pi$:

$$F_s = \frac{V_{SEC}}{2\pi I_{ref} L_{Ik}} \delta \left(1 - \frac{|\delta|}{\pi}\right) \tag{2.7}$$

Assuming the ideal operation, the algorithm is established by the equations (2.6) and (2.7).

2.3.5. Comparison of modulations

The DAB topology is very requested for bidirectional power flow applications. Even the easy implementation of a soft-switching feature on this topology to reduce switching losses of active devices and the core losses in HF transformer, the power circulating flow in DAB converter under the traditional SPS adding a larger current stress and larger converter loss affecting the efficiency of the system.

The authors of [16] say that with the same D_2 used in SPS - the outer phase-shift - the DPS control, with $D_1 \neq 0$ - phase shift of signal for the diagonal switch in both bridge - can offer wider power transmission range than the SPS control. Even the IBDC under DPS modulation have the same global maximum power than the SPS modulation, the same global maximum power can be obtained with the two-algorithm control implementation.

The theoretical and simulation results presented in some articles show that there is a reduction by implement DAB in power circulating flow. Thus low loss and high efficiency are obtained.

Even the simple DSP control proposed in [23] demonstrated good theoretical and simulation results in power circulating flow, low loss, and high efficiency also obtained. The only consists of one outer-phase-shift angle and one inner-phase-shift angle" for one the bridge, therefore, the only output voltage on one side of transformer emerge on three voltages level.

As can be seen, the DPS control offers a larger power output capability when compared to the SPS control [15]. The DAB converter modulated under DPS present improvements compared to the traditional phase-shift control. The peak current and steady-state current decreasing, and there is an improvement in the system efficiency and minimization of the output capacitance [15]. In addition, the DAB converter only can operate in a limited power range with the ZVS implementation.

The trapezoidal modulation it's seen interesting algorithm when the input and output voltage of the converter system is equal, while for the triangular modulation it's a good choice when input and output voltage are different each other. The limited power transfer intrinsic on the TRM is a result of the inefficient use of the switching period. The following Table 6 summaries the main feature relative to the modulation studied.

Table 6 – Main difference between the algorithm studied.

Modulation	Voltage range operation	reactive power circulation	Soft-switching	Efficiency	EMI	Power transfer	Algorithm implementation
PSM	Entered range	Significant	Reduced soft-switching region under light-load operation. Limited power range under ZVS	Average	Base	High	simple
DPS	Larger range operation	Reduced and even eliminated	Entire operation range	High	Redu. *	Wider range than the PSM	average
TRM	When $V_{DC}>N\cdot V_{Batt}$ or $V_{DC}<N\cdot V_{Batt}$	Reduced	ZCS for the lower side	High	Redu. *	Limited (low)	complex
TZM	Entered range	Reduced	ZCS occur in the 4 switches and ZVS in the others	High	Redu. *	High	complex
VFM	Entered range	Allow reduction when it complements other modulation	Allow ZVS and ZCS depending on the current level	Hight. Allow improving	Redu. *	High	complex

*“Redu.” mean reduction: The EMI reduction is a consequence of ZVS or ZCS capability

2.4. Semiconductor overview

A semiconductor material is a technology used in electronics to isolate or behaver as a conductor, depending on the operation characteristic (turn-on or turn-off). A semiconductor device can be switch between being an isolator and being a conductor, and there are different ways of switching a semiconductor device. The semiconductor particularity has the benefit from the high temperature during the operation mode. They tend, but not all, to conduct better in consequence of the temperature increase. The conduction performance is affected in metals when the temperature rises. The resistivity increases, and the conductor will drive worst.

As should be expected, different power device has different operation range. Regarding this, the follow Figure 2.13 from [24], present the different application context of the main semiconductors available and the position of the gallium nitride (GaN) and silicon carbide (SiC) power devices on the market today.

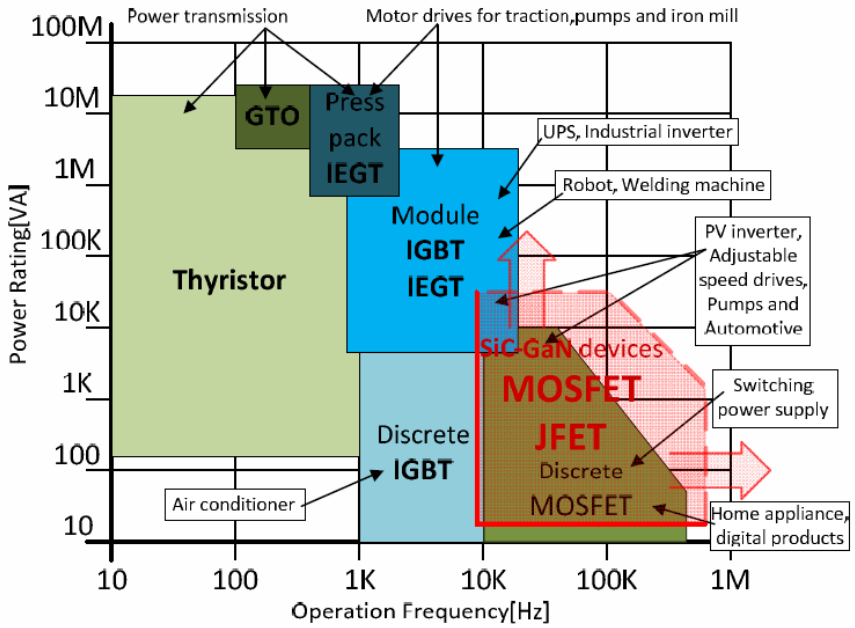


Figure 2.13 - Main application of the power device and the integration of the GaN and SiC semiconductor on the market [24].

From the previous graphic can be concluded that the emerging technology (GaN and SiC) fill the operation region above 10kHz and they have been adapted for medium voltage regime (MV, 2 kV – 35 kV): solar inverter, home application, EV charging converters, an uninterrupted power supply (UPS).

As well known, the power electronics revolution like the innovation on computing hardware, the smartphones, data center and more recently the electric vehicle, they used and continuously

use the silicon technology in their circuits. In fact, the silicon (Si) is an abundant element in the Earth's crust and the base for most electronics today.

2.4.1. IGBT and MOSFET

The main advantages properties are briefly described in this subsection. The Si-based IGBT and MOSFET have different properties and will be seen next.

During decades Si-based device was main chosen for power electronics system, especially the insulated-gate bipolar transistors (IGBT). It is a preference device used in high power application limited to 6.5 kV. Their limitations in term of switching operation up to some tens of kHz, and the junction temperature above 175ºC. This limitation has challenged engineers in recent years to select other superior material for transistors. The power metal-oxide-field-effect transistor (MOSFET) is more suitable for low power and low voltage range where a high switching operation is required. Looking to the Si-based power switches, the IGBT shows superior to the MOSFET since the IGBT has high voltage and current capability, although the frequency operation is the main restriction.

The commercially available wide-bandgap (WBG) semiconductor and the improvements on power device in the last decade, it is proving from the experimental prototypes and research that the emerging wide-bandgap material has potential to replace the typically Si material used in power device. The recent work made by Shan Yin and colleagues, they demonstrated with a prototype of voltage source inverter at 50-kW [25], a high-density converter that can operate at 100kHz with an efficiency of 97.9% using SiC power model in their converter. These results are excellent progress in power electronics field, and it is inevitable the penetration of WBG semiconductors for the voltage range from 650 V to 1700 V.

2.4.2. The emerging technology of wide-bandgap material

Table 7 shows the physical properties of the main wide-bandgap material in comparison to the popular Si material. The bandgap energy represents the energy required to “free” an electron and make it moves inside the semiconductor. So, the transistor made of SiC or GaN required more energy to excite an electron from the valence band to the conduction band. Note that the energy comes from an external source, and a semiconductor has this characteristic when an external power supply is applied it pass from isolation state into a conduction state.

The material with high breakdown field meaning that it is possible to block higher voltage, and it translates for the semiconductor in the capability of holding more voltage. Therefore, the application limits of the Si-based MOSFET with the capability of blocking only a few hundred

voltages can now be extended up to 1.7 kV (commercially available) with the use of silicon carbide material. This new technology of semiconductors is open new opportunities in the industry to make used of MOSFET and SiC material to improve the system in medium and high voltage field.

Table 7 - Properties of wide-bandgap material compared to the silicon material [26].

Material	Chemical symbol	Bandgap Energy (eV)	Electron Mobility ($cm^2/V.s$)	Break-down field (V/cm)	Thermal conductivity (W/cm.K)
Silicon	Si	1.12	1400	0.23×10^6	1.5
Silicon Carbide	4H-SiC	3.26	950	2.2×10^6	3.7
Gallium Nitride	GaN	3.39	1500	3.3×10^6	1.3 to 3
Diamond	C	5.47	1800	5.6×10^6	20

From Table 7, the Si material has a lower thermal conductivity than the emerging WBG material. A poor thermal conductivity will slow the heat flow transfer. Although the heatsink can deal with this problem, allows to extract heat from the devices and maintaining the operation control. But find other semiconductor solutions that offer better reliability and efficiency characteristics is always preferred. Without a doubt, the SiC material is an excellent candidate for a hostile environment, where the temperature is an issue, and it offers a higher thermal resistance (three times higher than Si).

Despite the great characteristic of the WBG semiconductor, the SiC, and GaN, the engineers have to face and taken into account the new challenge with circuit driver for fast switching device and the worries with electromagnetic interference at the high switching frequency. This will be discussed in Chapter 4.

2.4.3. The application of SiC in power electronics

The recent report provided by Yole Développment, August 2017 [27], shows that the SiC technology has been sold and adapted gradually in regime from 600 V to 1.7 kV, in medium voltage regime for solar inverter, automotive electrical equipment and an uninterrupted power source (UPS). As seen in Figure 2.14 the applications like photovoltaic inverter, power factor controller (PFC), power supply, and the UPS, they are driving the SiC market today and is expected to grow in next years with a focus on the market related with automotive equipment, motor driver and renewable systems.

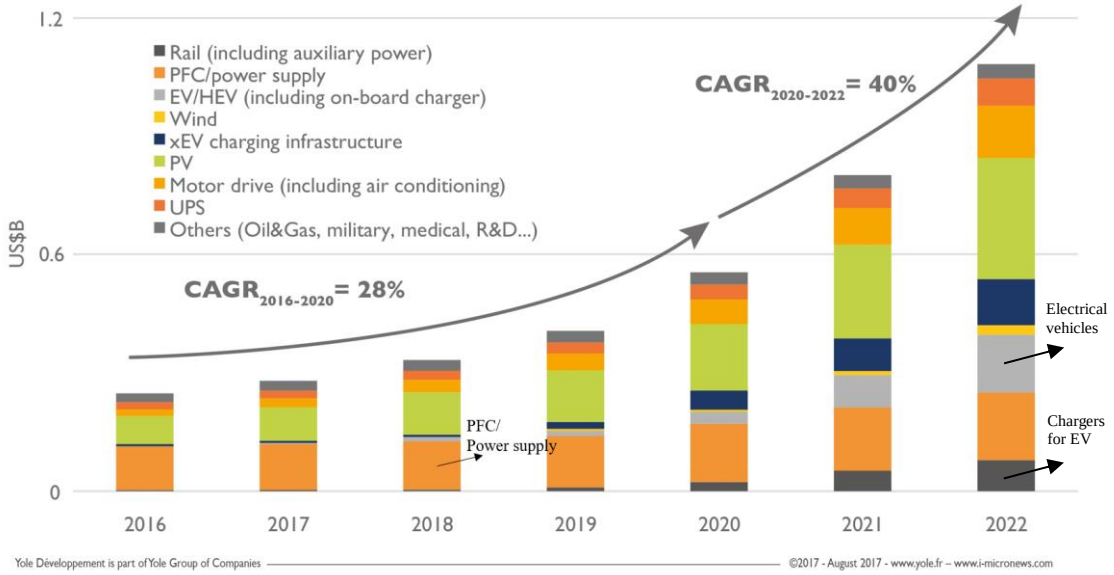


Figure 2.14 - The SiC device in the market for the next years slip by application [27].

Note: CAGR – Compound Annual Growth Rate.

2.5. Magnetics for DC-DC converter

This section is going to present a brief revision about magnetic components, which is ones of the important parameter to be in consideration since for this project it is expected to have electrical isolation between the power supply and the rest of the system (DC-link), so galvanic isolation is needed. Therefore, not only the design of the converter is considered in project engineering, the design and model of the magnets should be taken into account.

The magnetic components could be seen from two different points of view. One is the electrical parts, and the other is the magnetic parts. The following sections are going to describe the two approaches, electrical and magnetic fields, also describe the losses in magnetic component and finally the properties of magnetic materials. The revision is supported by the bibliography [28].

2.5.1. Electrical and magnetic domain

There is a relationship between both domains. Firstly, in the electrical domain, the two variable knowns are the voltage across two points (positive and negative reference) of the wire and the current through the wire. On the other side, the magnetic domain also has the same equivalent variable, the potential variable between two points (x1 and x2) is called by the magnetomotive force (MMF) and it is described by equation (2.8) as the integral of the magnetic field H along path x1 and x2.

If the magnetic field is uniform, the following equation is reduced to expression $\mathcal{F} = H\ell$.

$$\mathcal{F} = \int_{X1}^{X2} H \cdot d\ell \tag{2.8}$$

The flow variable in the magnetic domain is represented by the rate of change of the flux, $d\phi/dt$.

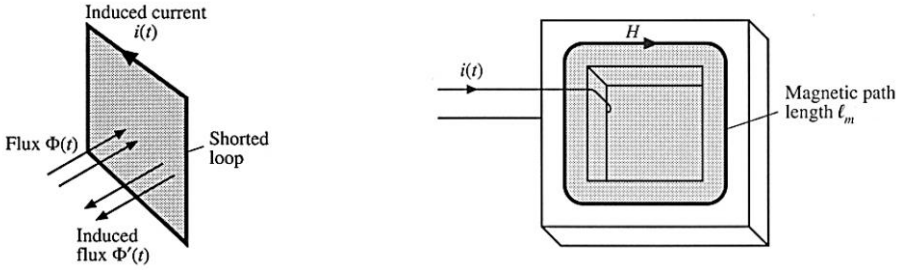
Considering the numbers of turns (N) across the core, according to the Faraday's laws, the potential difference across the wire (inductor) from the electrical domain is related to the flux by the equation (2.9). It means that flux induces a voltage $v(t)$ across given wire and is known as an induced electromotive force (emf).

$$v(t) = \frac{d\phi}{dt} \tag{2.9}$$

From Ampere' laws, the current in a wire is related to the magnetomotive force by the following equation, where the total current in a wire is equal to the integral of the H field lines in a close path.

$$i = mmf = \oint H \cdot d\ell \tag{2.10}$$

Like the current induced by the flux $\phi(t)$ in a closed loop wire - Figure 2.15 (a) from [29], the external magnetic field (H) passing through the center of the core (across the ℓ_m path) induces a current $i(t)$. Then, if the magnetic field intensity is uniform with the magnitude of $H(t)$, the total current $i(t)$ is equal to $H(t)\ell_m$.



(a) (b)

Figure 2.15 - (a) Simple schematic that illustrates the current $i(t)$ induced by the flux $\phi(t)$ in a short loop wire. (b) close magnetic core.

The total flux is equal to the integral of flux density B over the surface S:

$$\phi(t) = \int_S B \cdot dA \tag{2.11}$$

The B and H field can be related by the follow expression, where μ is the core permeability expressed in H/m, as a product of free space μ_0 and of the relative permeability μ_r.

$$B = \mu_0 \mu_r H \tag{2. 12}$$

The diagram of (2.13) resumes the relation between the different magnetic and electrical quantities.

$$i \xrightarrow{\times N} \mathcal{F} \xrightarrow{\times 1/\ell} H \xrightarrow{\times \mu_0 \mu_r} B \tag{2.13}$$

For the uniform flux density of magnitude B passing through a surface with an area of A_c, the (2.11) is reduced into:

$$\phi = BA_c \tag{2.14}$$

In a magnetic core, the A_c represents the cross section of the material where the magnetic field lines will pass through this section.

From the expressions from (2.13), since $B = \mu H$, $H = \mathcal{F}/\ell_m$ and the $B = \phi/A_c$ from (2.14) , the magnetomotive ($\mathcal{F}$) can be express by:

$$\mathcal{F} = \mathcal{R}\phi \tag{2.15}$$

The equation (2.15) is equivalent to the Ohm's law for the magnetic circuits. The magnetic reluctance is calculated for the uniform magnetic field by:

$$\mathcal{R} = \frac{\ell_m}{\mu A_C} \tag{2.16}$$

Moreover, the unit is the inverse of Henry, H^{-1}. The inverse of magnetic reluctance turns in another term, it's known as the permeance:

$$\mathcal{P} = 1/\mathcal{R} \tag{2.17}$$

It is quickly observed that the permeance unit is Henry, the same unit for inductance. However, they are different concepts. Like the magnetic reluctance that corresponds to the resistance in electric circuits, the permeance is equivalent to the capacitance.

The next step will deduce the inductance parameter. Therefore, starts with the relation of flux equal to the permeance per MMF:

$$\phi = \mathcal{R}^{-1}\mathcal{F} = \frac{Ni}{\mathcal{R}} \tag{2.18}$$

Multiply both side of the equation (2.18) by N, and differentiating terns dependent of the time and simplify the MMF into Ni, results in:

$$N\frac{d\phi(t)}{dt} = \mathcal{R}^{-1}N\frac{di(t)}{dt} \tag{2.19}$$

From the Ampere's law, the flux $\phi(t)$ induce a voltage in each turn of the wiring when it passes through. Then, the total voltage induced is:

$$v(t) = N\frac{d\phi(t)}{dt} \tag{2.20}$$

The first term of the equation (2.19) is replaced by the (2.20), and the inverse of magnetic reluctance into N turns is equal to the inductance:

$$v(t) = L\frac{di(t)}{dt} \tag{2.21}$$

When the current in the device (e.g., in a winding) where $|I| < I_{sat}$, it behaves as an inductor and their value is described by:

$$L = \frac{\mu_0\mu_r A_C N^2}{\ell_m} = \mathcal{R}^{-1}N^2 = A_L N^2 \tag{2.22}$$

At the point when the core saturates, it means that the $|I| > I_{sat}$, the flux density $B(t) = B_{sat}$ and consequently, by the Faraday's law, the voltage across the winding is equal zero and the magnetic device behaviour approaches a short circuit.

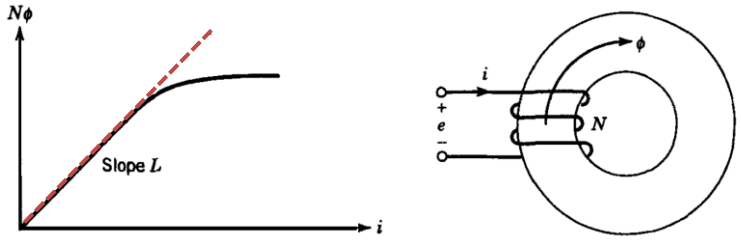
The inductance design corresponds to the electrical design approach, and their value is obtained from expression (2.22), and where the factor A_L is founded on the magnetic core datasheet, and the unit is typically nH/turns.

Considering a winding around a simple magnetic circuit as shown in Figure 2.16, adapted from [30] , the self-inductance *L* is associated with the flux that links the magnetic core:

$$L = \frac{N\phi}{i} \tag{2.23}$$

$$L = \frac{N}{i}\frac{Ni}{\mathcal{R}} = \frac{N^2}{\mathcal{R}} \tag{2.24}$$

As seen in Figure 2.16 (a), the $N\phi$ varies with i and can be linearized by the diagonal lines. It is common in coils with ferromagnetic cores. The line slope represents the linearized inductance *L*. Replace the ϕ in the previous equation (2.22) for the equation (2.18), the coil inductance is given by (2.24), and it is independent of the current.

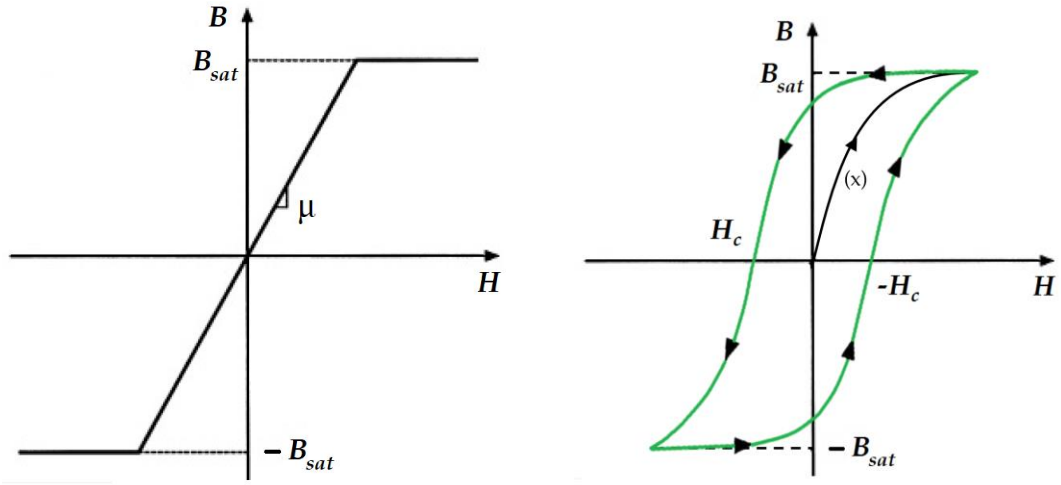


(a) (b)

Figure 2.16 – Self-inductance represented by *L'*.

2.5.2. Hysteresis curve

Well known in the literature, the Figure 2.17 adapted from [29] shows the relation of the flux density B verse flux intensity H. The B can be seen as the internal magnetic field of the material and the H as an external field applied.



(a) (b)

Figure 2.17 - (a) Curve *B-H* characteristic of the magnetic core material by neglecting the hysteresis. (b) The typical *B-H* magnetization curve

If the hysteresis is neglected, Figure 2.17 (a), the characteristic of the magnetic core material tends to be a straight line at a certain region, since after a specific stage that characteristic is limited by the material properties and the flux will saturate.

Interesting properties of the magnetic core is the "memory". Considering a magnetic core wholly demagnetized and slowly increase the flux density by increasing the external magnetic field intensity, the curve (x) is followed. After this point forward, and since the material will not demagnetize again, for example, curie temperature will not be met, the successive increases and decreases of the external *H*, the flux density *B* will follow the hysteresis curve represented in Figure 2.17 (b). The saturation is a problem in the magnetic device because of the risk of the short circuit. So that the operational *B-H* loop, for example in a conventional transformer, will be less large than hysteresis shown in Figure 2.17 (b) and below the saturation flux value (B_{sat}, $-B_{sat}$).

2.5.3. Magnetic Materials

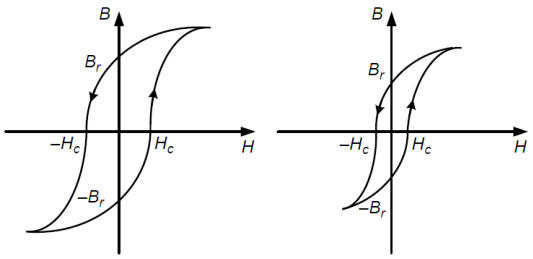
In the power electronics fields, the magnetic materials are separated into two domains: soft magnetic materials and hard magnetic materials. The characteristics and properties that distinguish the two types of materials can be made by observing the hysteresis loop, Figure 2.18.

It is not the intention of this section extend the studied of magnetic material and the detailed behavior in a present of a field. Some materials have a low relative permeability - $\mu_r < 1$ - and they have a susceptibility to produce a negative magnetization in the presence of a field. They are knowns as diamagnetic materials. The paramagnetic materials have a weak susceptibility in the

presence of a field, and the internal magnetic produced follow them in the same direction of the field applied. This material also has a low permeability, but it is superior to one - $\mu_r > 1$. Both diamagnetic and paramagnetic materials lost the magnetization easily when a field is no longer applied. In contrast, the ferromagnetic materials are quite different, they have a high relative permeability, they can be easily magnetized even in a weak magnetic and when the applied field is removed the ferromagnetic remains to preserve the magnetization.

Soft Magnetic Materials

The hysteresis cycle can be used to classify material property between soft and hard magnetic materials. The hard compared to soft materials has a wide hysteresis cycle as observed in Figure 2.18, a high coercive force and a difficult in realigned with the field. Note for the coercive force, a measure of a capability of the ferromagnetic material to hold an external field without lose the magnetization. The properties of hard magnetic materials are desirable in permanent magnets, commonly seen in electrical motors and generators to generate magnetic fields.



(a) (b)

Figure 2.18 - Hysteresis cycle for: (a) hard magnetics materials and (b) soft magnetics materials[28].

Hereupon, the continuous study will be done for the material more used for rectifier filters, in high frequency and isolated transformer since the low coercive force allows the easy magnetization and demagnetization again. The classification for soft materials follow with a short description of their main features:

Ferrites

Concerning composition, ferrites are ceramic magnetic materials obtained by a combination of iron oxide (Fe_2O_3) with other oxides powder metals, that after the mix are pressed and synthesize at high temperature. The synthetic materials Mn-Zn and Ni-Zn are the most common ferrites used in power electronics application. In general, ferrites have a low saturation field *B* (0.2 – 0.5 T) and it can enforce restrictions of their use in the high current application. Other disadvantage in ferrites is the low Curie temperature, around 200 ºC, that impose design limitation and more

attention by the engineers to control the temperature in application with ferrite cores. There are different shapes of ferrites available for transformers core and inductors.

Laminated iron alloys

To archive reduced eddy current (also known Foucault current) a laminated process proved some significant benefits of their use in AC applications. The addition of other metals into the iron alloys results in two popular categories: silicon-iron and nickel-iron.

The Si added to the iron reduce the magnetic saturation, then Si-Fe alloys only need a small external field to reach the saturation. But the silicon increases the resistive significantly and contributes to reducing the Curie temperature.

The ferro-nickel alloys are expansive materials and they are composed of 80% of nickel and the remain 20% of iron. These alloys are founded in telecommunication field (e.g., current transformer, audio transformer and magnetics amplifiers). They have high values of permeability and contribute to have in such application reduced eddy currents.

Powder iron

They are founded in a common toroidal or ring shape, and in the core, they are formed by a mix of iron and powder iron with an isolated material. The main feature of this soft materials is the high magnetic saturation peak compared to the ferrites. They are known to have low relative permeability (15 to 500), low core electrical resistivity and lower eddy current.

Nanocrystalline materials

In more recent years with the technic improvements and technologies, new types of soft materials appear, with nanocrystals in their composition. Regarding the properties, the nanocrystalline materials present a high coercive force, a high relative permeability around 20 000 and a maximum magnetic saturation moderate. The nanocrystalline are suitable for high frequency application.

Table 8 – Soft magnetic materials and their properties [28].

Materials	Ferrites	Nanocrystalline	Amorphous	Si iron	Ni-Fe (permalloy)	Powdered iron
Model	Epcos N87	Viroperm 500 F	Metglas 2605	Unisil 23M3	Magnetics Permalloy 80	Micro-metals 75 μ
Permeability, μ_i	2200	15 000	10 000–150 000	5000–10 000	20 000–50 000	75
B_{peak}, T	0.49	1.2	1.56	2.0	0.82	0.6–1.3
ρ, $\mu\Omega$m	10×10^6	1.15	1.3	0.48	0.57	10^6
Curie temp. T_c, °C	210	600	399	745	460	665
P_{fe} mW/cm^3	288 at 0.2 T 50 kHz	312 at 0.2 T 100 kHz	294 at 0.2 T 25 kHz	5.66 at 1.5 T 50 Hz	12.6 at 0.2 T 5 kHz	1032 at 0.2 T 10 kHz
K_c	16.9	2.3	0.053	3.388	0.448	1798
α	1.25	1.32	1.81	1.70	1.56	1.02
β	2.35	2.1	1.74	1.90	1.89	1.89

Table 8 presents the properties overview of the soft magnetic material studied and compared in the present section. The constant K_c, α and β are available in the magnetic cores datasheet.

From the table, it can be seen that the powder iron cores and iron alloys with nickel (Ni-Fe) are not appropriate to HF application. Typically, the nanocrystalline has a high magnetizing saturation than ferrite models, as observed in the previous table. Considering the *L* filter of the DAB been an external inductor placed to the transformer, and regarding the high switching frequency expected, the inductor *L* must handle with high current ripple. The follows tables show more recent available magnetic materials with focus in a ferrite and nanocrystalline materials. The physical and magnetic properties are showed.

Table 9 – Physical parameters of Sof Magnetics Materials [31].

	Density (kg/m^3)	Thermal conductivity (W/(m K))	Electrical resistivity (Ωm)
Polycrystalline Fe	7867	79.6	10.5×10^{-8}
NO Fe–(1.0 wt%)Si	7800	40	25×10^{-8}
NO Fe–(3.5 wt%)Si	7600	20	50×10^{-8}
GO Fe–(3 wt%)Si	7650	20	45×10^{-8}
Bonded-sintered Fe powders	7100–7700	10–30	50×10^{-6}–1000×10^{-6}
Permalloy/Mumetall ($Fe_{15}Ni_{80}Mo_5$)	8700	19	70×10^{-8}
Permendur ($Fe_{49}Co_{49}V_2$)	8200	32	40×10^{-8}
$Fe_{50}Ni_{50}$	8120	13	48×10^{-8}
$Fe_{52}Ni_{48}$			
Sintered ferrites (Mn–Zn and Ni–Zn)	4800–5300	4–7	10^{-2}–10^5
Amorphous alloys (Fe- and Co-based)	7200–7900	9	$120–140\times10^{-8}$
Nanocrystalline alloys (FINEMET)	7200	5	118×10^{-8}

Table 10 – Magnetic parameters of soft magnetic materials[31].

	Composition (wt% cryst. alloys, at% amorphous alloys)	Max. relative permeability (μ_{max})	Coercive field H_c (A/m)	Saturation polarization J_s (T)	Curie temperature T_c (°C)	Saturation magnetostriction $\lambda_s=(\Delta l/l)_{J_s}$
Polycrystalline Fe	Fe_{100}	$3–50\times10^3$	10–100	2.16	770	5×10^{-6}
NO Fe–Si	$Fe_{96\text{-}99}$-$Si_{1–4}$	$3–10\times10^3$	30–80	1.96–2.12	735–765	10×10^{-6}
GO Fe–Si	Fe_{97}-Si_3	$15–80\times10^3$	4–15	2.02	750	$1–3\times10^{-6}$
Fe–(6.5 wt%)Si	$Fe_{93.5}Si_{6.5}$	$5–30\times10^3$	10–40	1.80	690	5×10^{-7}
Sintered/bonded powders	$Fe_{99.5}P_{0.5}$	10^2–10^3	100–500	1.65–1.95	770	—
Permalloy/Mumetall	$Fe_{15}Ni_{80}Mo_5$/ $Fe_{14}Ni_{77}Mo_4Cu_5$	5×10^5	0.3–2	0.75–0.80	420	1×10^{-6}
Permendur	$Fe_{49}Co_{49}V_2$	2×10^3	30–100	2.35	930	$60\cdot10^{-6}$
Fe50–Ni50	$Fe_{52}Ni_{48}$	10^5	4	1.60	450	25×10^{-6}
Sintered ferrites	$(Mn,Zn)O\cdot Fe_2O_3$	10^3–10^4	5–20	0.4–0.55	130–280	-2×10^{-6}
	$(Ni,Zn)O\cdot Fe_2O_3$	10^2–10^3	20–200	0.2–0.35	110–400	-20×10^{-6}
Sendust	$Fe_{85}Si_{9.5}Al_{5.5}$	50×10^3	5–10	1.70	670	1×10^{-6}
Amorphous alloys (Fe-based)	$Fe_{78}B_{13}Si_9$	10^5	2–5	1.56	415	37×10^{-6}
Amorphous alloys (Co-based)	$Co_{67}Fe_4B_{14.5}Si_{14.5}$	5×10^5	0.5–1	0.62	320	5×10^{-7}
Nanocrystalline alloys (FINEMET)	$Fe_{73.5}Cu_1Nb_3Si_{13.5}B_9$	5×10^5	0.5–1	1.24	600	2×10^{-6}
Nanocrystalline alloys (NANOPERM)	$Fe_{86}Cu_1Zr_7B_6$	5×10^4	3	1.52	600	1×10^{-7}

2.5.4. Losses

In magnetics, there are two types of losses that occur during the conduction operation: the copper losses and the core losses, P_{cu} and P_{fe} respectively.

Starting with the copper losses: If the current across the wiring is variable, the RMS value becomes higher, and the wiring will heat. The power loss in the winding is given by:

$$P_{cu} = R_{AC} I_{rms}^2 \tag{2.25}$$

To represent the total core losses with a presence of sinusoidal excitation, taken in consideration that the losses in a winding are proportional to the square current load, the equation Steinmetz is used [28]:

$$P_{fe} = K_c f^{\alpha} B_{max}^{\beta} \tag{2.26}$$

In the above equation, the constant α, β and K_c could be founded in the datasheet of the magnetic core. The same information is shown in the Table 8.

2.6. Conclusions

This chapter essentially sought to frame the dissertation topic in a current context, with an introduction to the existing topologies of isolated DC-DC converters with the focus on DAB configuration topologies. Several concepts were approached in the technical scope to support the work to be developed during the dissertation project. As an example, the modulation technique, an important thematic in this type of projects in order to improve the performance of power electronic systems.

Base on power topologies studied and the advantages and limitation respectively, the choice of a DC-DC converter with galvanic isolation should meet the requirements and goals imposed by the project proposed. The soft-switching operation is essential for converter applications where high efficiency and light-weight design is required. From the topologies presented the single DAB converter meets the essential characteristics to be implemented in the project, besides presenting a compact structure and a reduced number of active components and magnetic elements, unlike other topologies analyzed (e.g., *CLLC*-type has extra resonant components). The modulation technique is an important approach and should reach a consensus to design. The next chapter will discuss the converter modulation as the mathematical model to the converter and also the dimensioning of the components.

Choosing a magnetic core to be part of the transformer core must agree on the requirements. It is expected an HF transformer. The ferrite core and nanocrystalline can be used for high-

frequency application and the second has an advantage of a high magnetic flux saturation. For a general application that it is required low permeability, the powder core is the best choice compared to the ferrites.

Chapter 3

Converter design

The present chapter intends to describe the study of dual active bridge converter topology with more detail. This topology was chosen because of the reasons presented in section 2.1.5.

As discussed early, the primary target of this dissertation is to design a high-density power DC-DC converter with galvanic isolation and best efficiency. This converter offers an integration of the energy supply system into a low voltage, in this case, a DC power system (e.g., an inverter DC-AC or a DC-DC converter).

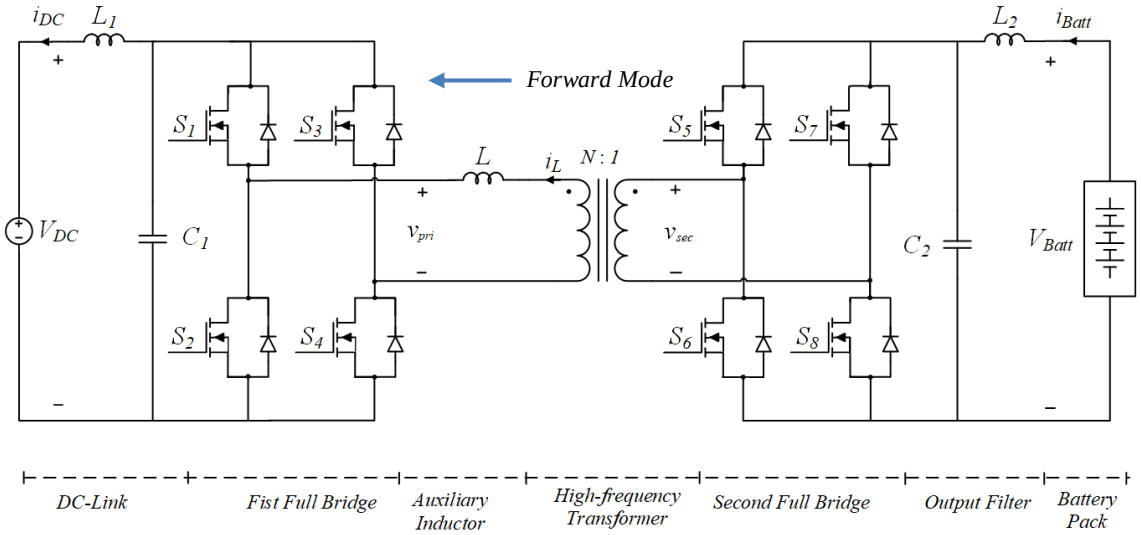


Figure 3.1 - The main structure of the DAB converter for this project.

The voltage across the capacitor C_1 and C_2 are denominated by V'_{DC} and V'_{Batt} respectively.

3.1. Traditional modulation

As seen in the section the 2.3.1, the power flow in DAB under conventional modulation (PSM) is, losses neglected, described by the equation: auxiliary

$$P_{SPM} = \frac{NV_{batt}V_{DC}}{8F_sL} D(2 - |D|) \tag{3.1}$$

Where the phase-shift is now normalized into a range between {-1; 1}. The conversion of the phase-shift to radian is easily made by multiplying *D* by 0.5π ($\delta_{rad} = 0.5\pi \times D$).

The maximum power possible on DAB in both directions of the power flow, also considering the battery without charging restriction regarding current limitation in this mode, occurs when D= ± 1, which in radians is equivalent to δ = ± π/2:

$$|P_{\max}| = \frac{NV_{Batt}V_{DC}}{8F_sL} \tag{3.2}$$

From the equation (3.2), the external inductor *L* can be found considering a given power that it preferred to transfer, and its value will be calculated in section 3.4.1. The M express the relation between the voltage across the transformer windings:

$$M = \frac{NV_{Batt}}{V_{DC}} \tag{3.3}$$

The transfer power on DAB, as a function of phase-shift angle, is illustrated in Figure 3.5, under the traditional modulation. A different curve is obtained for different voltage rate of the power source (e.g., battery pack), look at Table 3.1. A fixed voltage of 700V to the DC-link stage is considered. In Figure 3.5, the power transfer is normalized to be independent of the inductance value and the switching cycle. This is possible due to the same ratio maintained between the frequency and the inductance of the transformer at inverse rate relation.

To be more explicit about how the different curve is obtained, Table 3.1 expresses that association. From the requirement stated in the first chapter for the option one (OPT1), in the worst-case scenario it is expected a battery pack voltage around 200 V. In a full charge scenario, a 450 V is expected. There is a different voltage range from the power source to the DC-link stage, at the end of the second bridge. Thus, an optimum transformer turn ratio needs to be determined not only to limit the shifting value but also to reduce the reactive power flow. So, when the phase-shift is zero, only active power is transferred in the converter. The increase of the phase-shift translates into a rise in current flow due to the dynamic change of the battery voltage during the charge and discharge. The determination of N must minimize the amount of the current flow in nominal operation when the $N \times V_{batt}$ is close to the V_{DC}. Due to the characteristic and limitation

of the battery, the Figure 3.2 shows the restriction imposed in terms of power transfer capability as function of the battery voltage level. As seen in the Figure 3.2, below the voltage level of 250 V, the charging and discharging current was limited to $22100/250 = 88{,}5$ A. The Figure 3.3 resumes the current limits in entire range of the battery voltage.

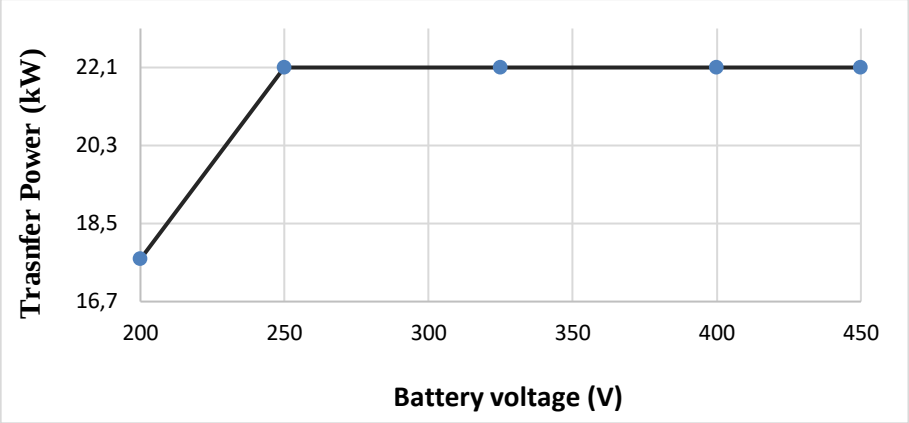


Figure 3.2 – Power transfer as a function of battery voltage level.

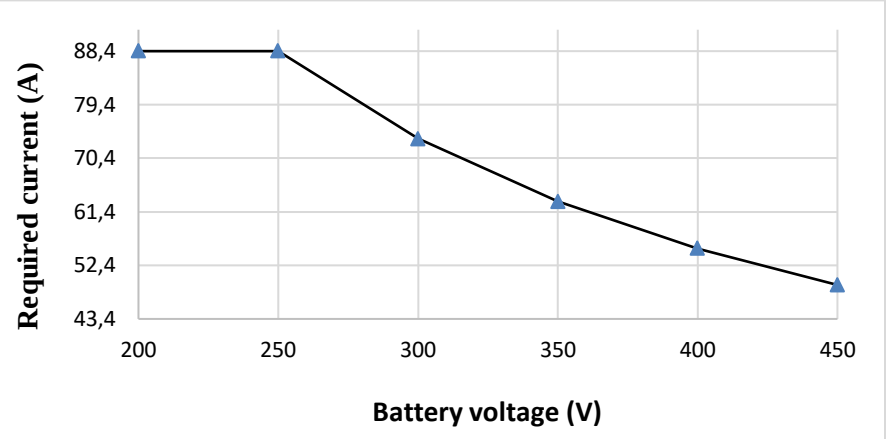


Figure 3.3 – Required current as a function of battery voltage level.

Notes:

- In a real application, the battery has operation limits: which range from 200V to 450V; Different battery chemistries present different current limitations.

- The transformation ratio must be carefully analyzed during the DAB design. The value of *N* limits in part the phase-shift range. If the N is not appropriately sized for the system, it may happen that for a given voltage level in the battery, it is not possible for the DC-DC converter to provide the desired nominal power, even impose the maximum phase-shift (90º degrees) between voltages at the output of both H-bridges.

The main waveforms that results in the simulation of DAB under phase-shift modulation are shown in Figure 3.4, where the primary and secondary voltage applied to the external inductor L and the transformer secondary side, respectively. The secondary voltage translated into the transformer primary side is represented by Nv_{sec}.

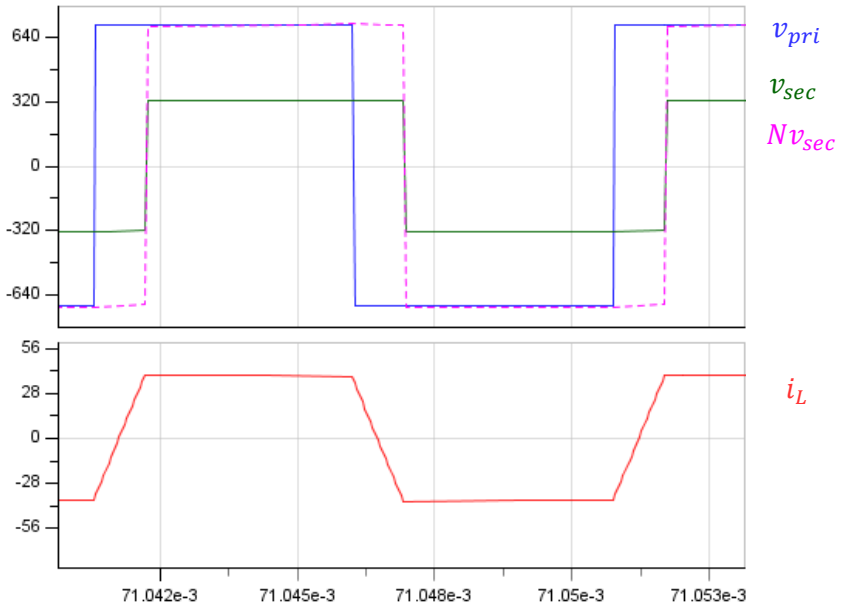


Figure 3.4 - Waveforms v_{pri}, v_{sec}, and Nv_{sec} obtained from circuit simulator under PSM.

3.1.1. Procedures to choose the right transformer turn rate N

Given the voltage range {200, 450}, to minimize the reactive power circulation, the intermediate value of 325 V was selected as the nominal value for the turn ratio project.

$$N \cong V_{DC}/V'_{Batt} = 700/325 \cong 2.15$$

The Table 3.1 is obtained for different operation points, where the turn ratio is stablish to a fixed value. When *N* is determined, the leakage inductance value is calculated for the frequency range using equation (3.1), that is intended to be analyzed in the next sections. The transformer leakage inductance is calculated for the scenario where the battery is at the lower voltage level (200 V) at rated power (22.1 kW). Note the turn ratio N:1 referred from primary to the secondary.

Table 3.1 – Voltage ratio with N=2.15.

V_{DC} (V)	V_{Batt} (V)	M= NV_{Batt}/V_{DC}
700	200	0,61
700	250	0,77
700	325	1,00
700	400	1,23
700	450	1,38

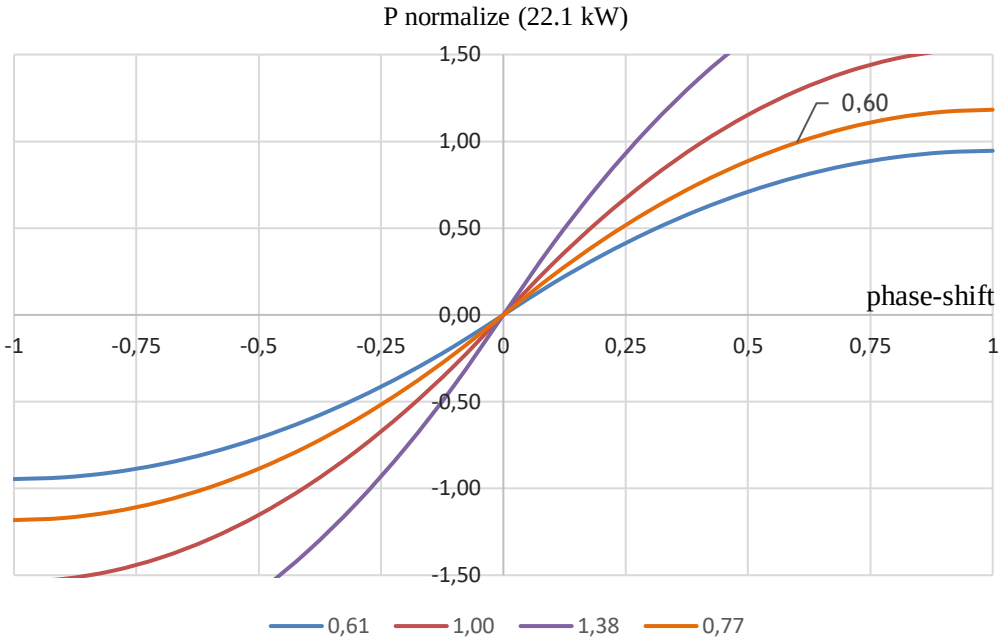


Figure 3.5 - Relationship between transfer power and phase-shift angle.

Considering Figure 3.5, the active power has a quasi linear increase until D = ± 0.5. After a phase-shift angle of a ± π/4 radians (D = ±0.5 normalized) the active power does not change much, both in forward or reverse mode. Therefore, it is required to limit the phase-shift angle, not only due to the reason the power transit starts to change lesser after D = 0.5, but also to reduce the reactive power circulation. At this point, the current flow increases more, mainly when the relation between NV_{Batt} and V_{DC} is different of one. A working point where the power supply system (battery) operates in low voltage, under the nominal power value.

Soft-switching range

The PSM technique has only one degree of freedom, which means that there is only one variable to control the power flow. In this case, it is impossible to control the reactive power separately. This is a disadvantage seen in the state of de art chapter about PSM. To define the

region for soft-switching inherent in the DAB converter, the expression (3.4) and (3.5), adapted from [32] defines the limits of the phase-shift towards reducing the switching losses.

Condition 1 $$D > \frac{NV_{Batt} - V_{DC}}{NV_{Batt}} \quad \text{if } NV_{Batt} > V_{DC} \tag{3.4}$$

Condition 2 $$D > \frac{V_{DC} - NV_{Batt}}{V_{DC}} \quad \text{if } NV_{Batt} < V_{DC} \tag{3.5}$$

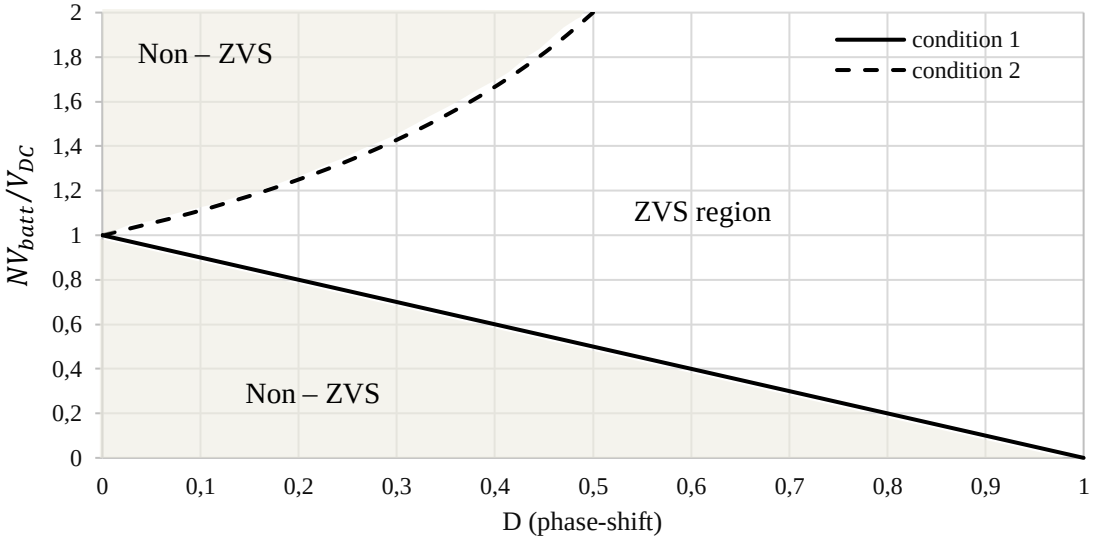


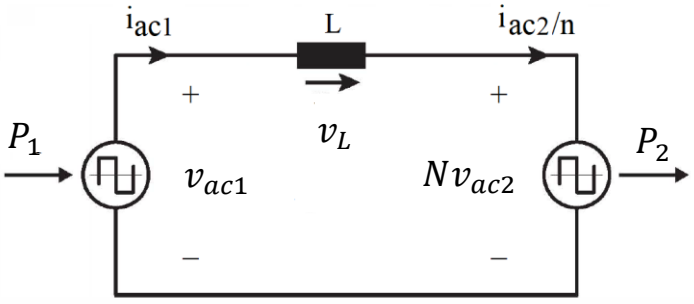
Figure 3.6 – Definition of the soft-switching region.

3.2. Analysis of the DAB topology neglecting the losses

The converter could be analytically characterized by the model shown in Figure 3.7 below, (adapter from [33]). The bidirectional DAB converter is reduced merely to the configuration with square voltage supply v_{ac1} at the output of the first bridge, connected with an inductor L into to the second square voltage supply v_{ac2}. This general model does not consider the losses on the active components, and on the resistive elements inherent of the winding connections, and the parasites capacitances are suppressed either. The high frequency transformer is ideally reduced into an inductor. The operation analysis of the DAB and the way that the power flux direction is obtained, it was also described in the previous chapter and can be consulted in section 2.3.1. The present section intends to show the mathematical expression of the command signal for the active devices. With an appropriate combination of switching signals, at the inductor terminals is generated, respectively in each side, a square voltage wave, with two levels, $\pm v_{ac1}$ and $\pm v_{ac2}$. The zero state it is possible, depending on the switching state of T1-T4 and T5-T8. The expression (3.6) resume the all possible combinations.

$$vac_1(t) = \begin{cases} +v_{ac1} & combination\ of: \ T1,T4\ turn\ on, \quad T2,T3\ turn\ off \\ 0 & combination\ of: \ T1,T3\ turn\ on, \quad T2,T4\ turn\ off \\ 0 & combination\ of: \ T2,T4\ turn\ on, \quad T1,T3\ turn\ off \\ -v_{ac1} & combination\ of: \ T2,T3\ turn\ on, \quad T1,T4\ turn\ off \end{cases} \tag{3.6}$$

$$vac_2(t) = \begin{cases} +v_{ac2} & combination\ of: \ T5,T8\ turn\ on, \quad T6,T7\ turn\ off \\ 0 & combination\ of: \ T5,T7\ turn\ on, \quad T6,T8\ turn\ off \\ 0 & combination\ of: \ T6,T8\ turn\ on, \quad T5,T7\ turn\ off \\ -v_{ac2} & combination\ of: \ T6,T7\ turn\ on, \quad T5,T8\ turn\ off \end{cases}$$



$i_{ac1} = i_L$

$i_{ac2}/N = i_L$

$P_1 = P_2$

Figure 3.7 – A general model without losses consideration.

The voltage applied to both side of the inductance L, resulted from the combination of the switching transistors, will create a voltage v_L across the inductor terminals.

$$v_L(t) = v_{ac1}(t) - Nv_{ac2}(t) \tag{3.7}$$

The $v_L(t)$ will generate a current $i_L(t)$, and it is expressed by:

$$i_L(t) = i_L(t_0) + \frac{1}{L}\int_{t0}^{t1} v_L\, dt, \qquad t_0 < t_1 \tag{3.8}$$

Where the $i_L(t_0)$ is the initial current on the inductor. The P_1 and P_2 represent the average power during each cycle period (T_S=1/F_S). Since it is not considered the power losses during the conversion:

$$P_1 = P_2 = P_{avr} = \frac{1}{T_S}\int_{t_0}^{t_{0+T_S}} p(t)\, dt \tag{3.9}$$

As described before in modulations section (2.3.), the forward and reverse power flow of the DAB have some intrinsic parameters to generate the waveform v_{ac1} and v_{ac2} appropriately. They are the switching frequency of the device, the phase-shift angle between v_{ac1} and v_{ac2} and the duty cycle of each square waveforms v_{ac1} and v_{ac2} .

3.3. Modeling of the DAB converter

In literature, there are many modeling approaches to characterize the DAB converter. The reason for creating a model for a converter topology is to allow developing a closed-loop control system. A general model does not consider the input/output filters and the winding resistance of the transformer and the connections, they are neglected to simplify the analysis. An accurate generalized model of the DAB DC-DC converter is derived in [34] without considering the core losses, and only the winding resistance is included in the model, though this model is not accurate enough and the author report that it is unsuccessful to predict the steady-state operating point at high frequency.

Whereas another complex model is deduced and some of that includes essential considerations to approximate the model closer to the real operation of the converter with the more accurate analysis in term of losses and efficiency. In [35], K. Zhang proposes a reduced-order average model (AVM) for the DAB analysis, and it is a complete model since it includes the conduction losses, meaning that the on-conduction resistances of the transistors are added. Furthermore, the transformer core losses and the input/output filters are also included in the model.

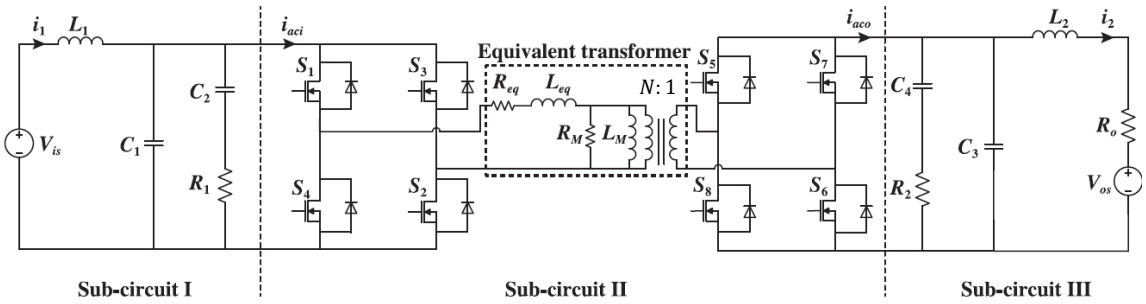


Figure 3.8 - Circuit DAB with the main parameters represented [35].

The model will give a comprehensive analysis in a steady state operation of the converter through equations. Moreover, to implement the hardware, the modeling and simulation of the converter are required to size the components and to design the controller.

In the next, the steady state equation of the DAB will be derived, and the analysis of the small perturbation added to the reduced model will be approached. For dynamic of the converter, the simple modulation technique (SPM - section 2.3.1) is used, like model's author refer, it is a way to reduce the complexity in deriving the small-signal AVM [35].

3.3.1. The equation of DAB in steady state

Foremost, let's begin dividing the DAB circuit of Figure 3.8, from [35] into three parts, where the V_{os} represents the battery and R_0 it's series resistance of the battery. The state equation for the topology of Figure 3.8 follows:

$$L_1 \frac{di_1}{dt} = v_{is} - v_{c1} \tag{3.10}$$

$$L_2 \frac{di_2}{dt} = v_{c3} - v_{os} - i_2 R_0 \tag{3.11}$$

$$C_2 \frac{dv_{c2}}{dt} = \frac{v_{c1} - v_{c2}}{R_1} \tag{3.12}$$

$$C_4 \frac{dv_{c4}}{dt} = \frac{v_{c3} - v_{c4}}{R_2} \tag{3.13}$$

$$C_1 \frac{dv_{c1}}{dt} = i_1 - i_{aci} - \frac{v_{c1} - v_{c2}}{R_1} \tag{3.14}$$

$$C_3 \frac{dv_{c3}}{dt} = i_{aco} - i_2 - \frac{v_{c3} - vc4}{R_2} \tag{3.15}$$

Note that the t term refers to the time within a period T_s (it is a half of the switching period). The input filter parameters are described by LC structure (C_3 and L_2) and the series RC (C_4 and R_2) and they are used to reduce either current and voltage ripple. The same configuration filter is used in the output side, the C_1 and L_1, and C_2 and R_2 respectively. The v_{c1}, v_{c2}, v_{c3} and v_{c4} are voltages across the respective capacitor. The equivalent resistance R_{eq} includes the sum of the two equivalent on-conduction resistances (R_{ON}) of the transistors and diodes connected to the transformer terminals during the turn-on of the diagonal transistors. Moreover, the transformer magnetizing resistance R_M, the winding resistance on the primary R_{l1} and the equivalent resistance form secondary to referred into primary side R_{l2}.

$$R_{eq} = R_M + 2R_{ON} + R_{l1} + \frac{R_{l2} + 2R_{ON}}{\left(\frac{1}{N}\right)^2} \tag{3.16}$$

The current in the DC bus of each DC-DC converter, i_{aci} and i_{aco} respectively, have the waveforms showed in Figure 3.9. Note that the linear waveforms showed, ceases to be when the existence R_{eq} is no more neglected and the rise and fall current curve passes to be lightly exponential. For now, the R_M and the magnetize inductance L_M are ignored and to complete the reduced model, the average current needs to be derived:

$$i_{aci} = \begin{cases} i_\alpha = \dfrac{v_{c1} + v'_{c3}}{R_{eq}} + \left(-I_{t1} - \dfrac{v_{c1} + v'_{c3}}{R_{eq}}\right) e^{-\frac{R_{eq}}{L_{eq}}(t - dT'_s)}, & 0 \le t < dT'_s \\ i_\beta = \dfrac{v_{c1} + v'_{c3}}{R_{eq}} + \left(I_{t2} - \dfrac{v_{c1} + v'_{c3}}{R_{eq}}\right) e^{-\frac{R_{eq}}{L_{eq}}(t - dT'_s)}, & dT'_s \le t < T'_s \end{cases} \tag{3.17}$$

The voltage v'_{c3} is the voltage v_{c3} referred to the primary transformer side, with the correct transformation $v'_{c3} = N v_{c3}$. The current peak value on the Figure 3.9, from [35], are I_{t1} and I_{t2}. The average current within half switching period $T'_s = 0.5 \times T_s$:

$$I_{aci} = \frac{1}{T_s'}\left(\int_0^{dT_s'} i_\alpha \, dt + \int_{dT_s'}^{T_s'} i_\beta \, dt\right) \tag{3.18}$$

Since the two waveforms current i_{aci} and i_{aco} are symmetrical about the horizontal axis, the output average current in the transformer follow:

$$\frac{I_{aco}}{N} = \frac{1}{T_s'}\left(\int_0^{dT_s'} -i_\alpha \, dt + \int_{dT_s'}^{T_s'} i_\beta \, dt\right) \tag{3.19}$$

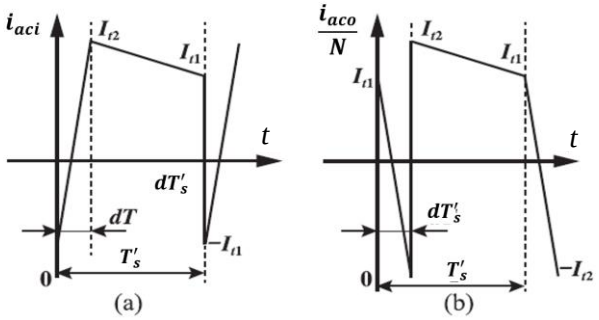


Figure 3.9 - Input and output current in DAB. (a) Input current i_{aci} in first H-bridge and (b) output current i_{aco} in the second H-bridge represented in a half switching period.

In order to simplify the previous equations, it is replaced by the i_α and i_β from (3.17) into (3.18) and (3.19):

$$\begin{aligned} T_s' I_{aci} &= \frac{v_{c1} + v_{c3}'}{R_{eq}} dT_s' + \frac{v_{c1} - v_{c3}'}{R_{eq}} (1-d) T_s' \\ &+ \frac{L_{eq}}{R_{eq}}\left(I_{t1} + \frac{v_{c1} + v'_{c3}}{R_{eq}}\right)\left(e^{-\frac{R_{eq}}{L_{eq}}(dT_s')} - 1\right) \\ &+ \frac{L_{eq}}{R_{eq}}\left(\frac{v_{c1} + v'_{c3}}{R_{eq}} - I_{t2}\right)\left[e^{-\frac{R_{eq}}{L_{eq}}(T_s' - dT_s')} - 1\right] \end{aligned} \tag{3.20}$$

$$\begin{aligned} T_s' \frac{I_{aco}}{N} &= -\frac{v_{c1} + v_{c3}'}{R_{eq}} dT_s' + \frac{v_{c1} - v_{c3}'}{R_{eq}} (1-d) T_s' \\ &- \frac{L_{eq}}{R_{eq}}\left(I_{t1} + \frac{v_{c1} + v'_{c3}}{R_{eq}}\right)\left(e^{-\frac{R_{eq}}{L_{eq}}(dT_s')} - 1\right) \\ &+ \frac{L_{eq}}{R_{eq}}\left(\frac{v_{c1} - v'_{c3}}{R_{eq}} - I_{t2}\right)\left[e^{-\frac{R_{eq}}{L_{eq}}(T_s' - dT_s')} - 1\right] \end{aligned} \tag{3.21}$$

Until now, the equation for the reduced-order AVM are analyzed and it is represented by the equation (3.10)-(3.17), (3.20) and (3.21). Note that, once again, the core losses and the magnetizing inductance are neglected. Some information was suppressed from the derivation of the reduced model, so, for more comprehensive analysis, it is recommended for the reader to review the respective reference. The author also presents the derivation for AVM with the effect of the transformer losses. This approach is not considered in the actual section.

3.3.2. Small-signal derivation

It is time to consider the small perturbation in the control signal. A small variation will be introduced into the large-signal variables from previous equations and the small-signal model will be derived. Following the input and output variables with the additional small ac variations.

$$v_{is} = V_{is} + \hat{v}_{is} \tag{3.22}$$

$$v_{os} = V_{os} + \hat{v}_{os} \tag{3.23}$$

$$d = D + \hat{d} \tag{3.24}$$

$$i_1 = I_1 + \hat{\imath}_1 \tag{3.25}$$

$$i_2 = I_2 + \hat{\imath}_2 \tag{3.26}$$

$$v_{c1} = V_{c1} + \hat{v}_{c1} \tag{3.27}$$

$$v_{c2} = V_{c2} + \hat{v}_{c2} \tag{3.28}$$

$$v_{c3} = V_{c3} + \hat{v}_{c3} \tag{3.29}$$

$$v_{c4} = V_{c4} + \hat{v}_{c4} \tag{3.30}$$

Replace the equation from (3.22) - (3.30) in the reduced-order equation (known as large-signals) the small-signal model can be also obtained.

In order to not extend all deduction for the modeling of the converter founded in [35], the model linearization and consequently the details to derive the small-signal model for DAB can be founded in the reference. Applying the Laplace transform with an appropriate frequency-domain analysis, a control-to-output transfer function is obtained. After some reorganization, the output and input transfer function follow in the expression (3.31) and (3.32).

The quantities y, n, p, q, r and z founded in below transfer function, they are constant values and depending on the converter parameter (e.g., equivalent resistance, inductance, transfer rate and input and output DC voltage applied to the transformer terminals). The expression for that quantities could be founded in the reference [35], and they were omitted in this section.

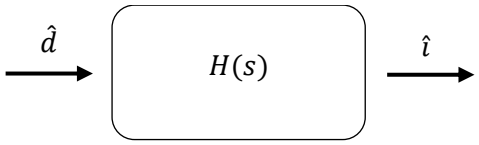


Figure 3.10 - Diagram of the system transfer function depending on the phase angle as input.

The current control system is expressed in function of the phase-shift input:

$$G_{out}(s) = \left.\frac{\hat{\imath}_2(s)}{\hat{d}(s)}\right|_{\hat{v}_{is}(s)=0,\hat{v}_{os}(s)=0}$$

$$G_{out}(s) = \frac{x - \dfrac{py}{q + C_1 s - \dfrac{1}{R_1(C_2R_1s + 1)} + \dfrac{1}{R_1} + \dfrac{1}{L_1 s}}}{\left(\dfrac{1}{N}\left(C_3 s + \dfrac{1}{R_0 + L_2 s} - \dfrac{1}{R_2(C_4R_2s + 1)} - Nz + \dfrac{1}{R_2}\right) + \dfrac{ry}{q + C_1 s - \dfrac{1}{R_1(C_2R_1s + 1)} + \dfrac{1}{R_1} + \dfrac{1}{L_1 s}}\right)(R_0 + L_2 s)} \quad (3.31)$$

Following the same process, the control-to-input transfer function is derived by:

$$G_{out}(s) = \left.\frac{\hat{\imath}_2(s)}{\hat{d}(s)}\right|_{\hat{v}_{is}(s)=0,\widehat{v}_{os}(s)=0} \quad (3.32)$$

However, only the output will be considered for this project. It is expected in the next section, to develop a closed-loop control for the output side, where a current control will be appropriately defined to control the battery DC side.

3.4. Components sizing

The converter design has critical components that must be selected carefully to prevent it from oscillating, voltage stress or even to decrease the complexity of the control loop. The major elements of the converter are the inductors as a part inherent of the transformer and the typical LC.

3.4.1. AC link inductance

Some parameters are defined form the requirements, as the V_{DC} fixed at 700V, the voltage V_{Batt}, the transformer rate N was determined in section 3.1. because of reason mentioned. The only parameter remaining to be known is the filter inductance to allow a transfer power of 22.1 kW at a specific frequency. It is an integral part of the DC-DC converter. Due to the SiC MOSFET

capability for high-frequency switching, the high switching of the transistor will be analyzed. Regarding the prototypes available in the literature with SiC technology inherent, excellent results were obtained in power conversion at a frequency switching of 60 kHz and 100 kHz. The experimental prototypes are found in [36] and [25], respectively.

Some simulations will be done at a frequency range between 40 kHz at 1120 kHz and open-loop simulation. Analyzes will be approached in terms of efficiency, total losses in the switching device, and Joule losses in the resistive elements are included. The key waveform from DAB simulation will also shown.

Taken the equation (3.1), replacing the P_{SPM} for the maximum nominal power 22.1 kW, the filter inductance is determined for the worst case where the voltage level on pack battery is limited to 250 V. The required phase-shift to obtain the desirable maximum transfer power, solving the equation (3.1) in order to D (normalized):

$$D = signal(x) \times \left(1 - \sqrt{1 - \frac{8P_{SPM}F_S L}{NV_{Batt} \times V_{DC}}}\right) \mid \begin{cases} x = +1, forward\ operation \\ x = -1, \ reverse\ operation \end{cases} \tag{3.33}$$

The maximum phase-shift is D = 0.602 (54.7 º), maintaining the same ratio as seen in Table 3.2. The phase-shift value was defined in order to find a balance between the reactive power and the value of the external inductance. For larger lags between the V_{Batt} and V_{DC}, the greater the reactive current flow.

Table 3.2 – Filter inductance in order to the switching frequency.

Switching frequency	Filter inductance
40 kHz	45 µH
60 kHz	30 µH
80 kHz	22.5 µH
100 kHz	18 µH
120 kHz	15 µH

In chapter 4 will be listed the available semiconductor in the market with the emerging technology, that complies with this requirement and could be suitable to the project DC-DC converter.

Before that, follows the dimensioning the input/output filters as also the transformer in the next two sections.

3.4.2. Input and output filters

The role of the input/output filters included in the converter design, is to suppress the current and voltage ripple. The *LC* configuration is well known in electronics, and they have a different purpose. The simple structure for the DAB converter shown in Figure 3.11Figure 3.12, includes the leakage inductance connected to an ideal transformer; non-ideal MOSFET for the H-bridge; and an ideal DC voltage source, one for the equivalent DC-link and other for the battery system side. The small resistance *R4* was added to measure the current into/from the battery side, depending on the energy flow direction. The resistance *R1* have the same purpose but for the DC-link side.

During the transient response, it was verified that a significant amount of time was required for the DAB converter to reach the steady state (in order of some ten microseconds). So, a capacitor was added in series with the external inductor *L*, in the primary side of the inductor, to suppresses the DC component of the transformer current and allows to focus on the steady-state regime observation, not affecting the overall system operation.

Different from the time domain analysis, a Fast Fourier Transformer (FFT) can be used to analyze the signals into the frequency domain. From the FFT spectrum of Figure 3.13, it is shown the fixed frequency in the range and their magnitude value. If the converter operates with a rate of F_S, in the transformer output point of view, the pulsation frequency in output is double for the DAB topology.

It can be observed in the FFT spectrum a dominated signal at a frequency of around 80 kHz, but the MOSFET operates at half of that. Such away, the battery current across the resistor *R4* is not a purely DC signal, as observed. There is some AC component in the signal at a high frequency. A low pass filter is needed in order to remove the ripple from the converter into the battery. The high-frequency components introduce instability and desirable ripple into to the DC supply or DC system, depending on where the bridge is connected.

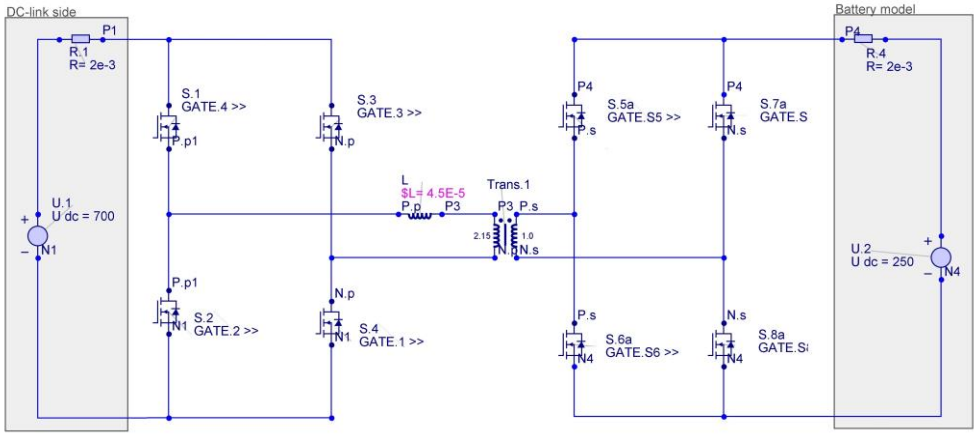


Figure 3.11 – Simple DAB converter structure in environment simulation GeckoCIRCUITS.

The spectral harmonic in Figure 3.13 come from the simulation performed in GeckoCIRCUITS® with the topology in Figure 3.11. No output filters were considered, and the power transit is derived from the DC power supply U.1 into the U.2. All command signals have 50% of the duty cycle, and the voltage v_{sec} is shifted by 56º degrees relative to the voltage Vpri, in order to get the power transit at 22.1 kW in the DC-bus. Both DC bus supplyies are considered ideal. Later, the modulation technique developed in the simulator software will be explained in section 3.7. For the design of the low pass filter to be placed at the outlet of H-bridges, the combination of an inductor with a capacitor will be used. The combination of both *L* and *C* will create a resonant effect on the circuit (Figure 3.12). In point of view at the converter output, this filter is a current filter placed in the output to deal with the high magnitude harmonics.

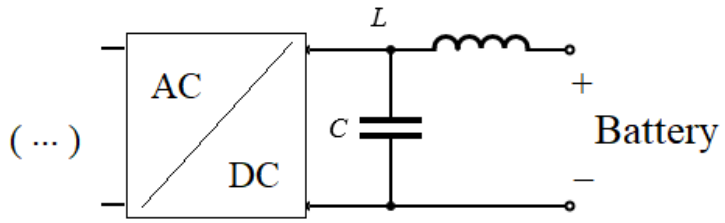


Figure 3.12 – Typical *LC* structure filter.

The filter design procedure will be described later in the document. Since the desired output is DC, a capacitor across the output terminals of the circuit is needed, and it will receive the high-frequency ripple current and reduce the voltage oscillation. This is due to the high-frequency modulation of the converter (e.g., PWM). The DC capacitor must be adequately dimensioning to support a range of DC voltage between 200 V to 450 V, and 700 V for the DC-link. The current in a capacitor is given by the expression $i_c = C\frac{dv}{dt}$, and the capacitance value is derived by:

$$C = \frac{i_{C\ ripple}}{\Delta V \times F_s} \tag{3.34}$$

The ΔV define the voltage variation (ripple) across the capacitor. For the design procedure, the ripple value was chosen to be 5% of the DC bus nominal voltage. The ripple voltage is inversely proportional to the capacitance value:

$$\Delta V_{bus} = V_{DC} \times (\%\ of\ V_{ripple}) \tag{3.35}$$

The ΔV is a design requirement, the frequency and the voltage bus depending on the system operation, and the $i_{C\ ripple}$ is still to be found. To find the ripple that the capacitor will support in worst case scenario, a short exercise is made in a simulation environment. Analysing the predominant components in the FFT spectrum allows to determine the best cut-off frequency for the low-pass filter to reduce the magnitude of the undesired AC components.

A DAB simulation in the forward operation (Figure 2.8) is made at rated power 22.1 kW. Figure 3.13 is observed each different AC components in the FFT spectrum, for the input and output current ripple of the DC-DC converter. The use of non-ideal MOSFETs in the current simulation was mentioned earlier, but in relation to the losses model used into power switch components will be explained in section 3.7.

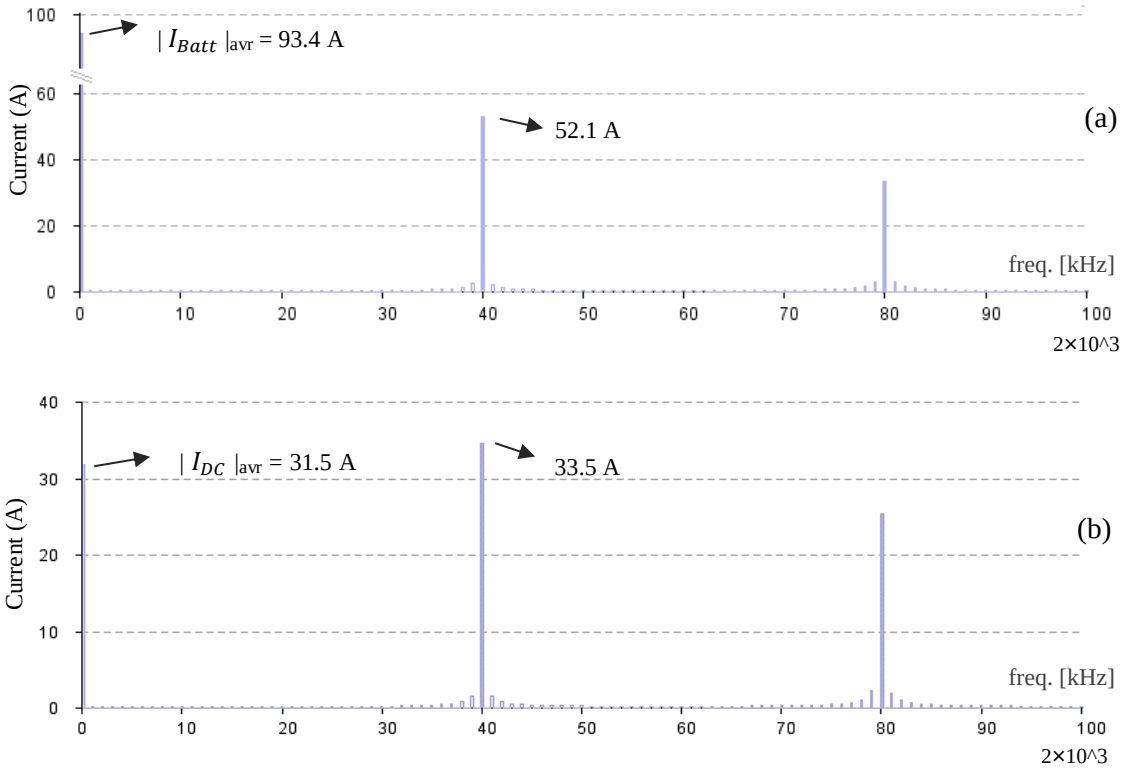


Figure 3.13 – The battery current (a) and DC-link current (b) expressed in FFT domain

Observing the Figure 3.13, the DC value for battery current side is 93.4 A and -31.5 A to the DC-link side. By the observation of the FFT spectrum, the magnitude of the AC signals around 80 kHz and 120 kHz is significant. This approach shows the importance of using a filter to remove high-frequency harmonics or attenuate their magnitude value. It is important to clarify, that the DAB topology injects HF ripple into the battery if no DC bus interface exists. The capacitor deals well with high frequency because it allows HF signal to pass through it. However, an inductor needs to be added to reduce the magnitude.

Filter dimensioning:

Exercise: Find the capacitance value to deal with the ripple current at HF and a voltage oscillation given by ΔV.

Battery side:

I_{ripple} (80 kHz) = 52.1 A (value from the simulation)

ΔV_{Batt} = 12.5 V (5% of 250V)

$$C2 = \frac{52.1}{(12.5 \times 80\ 000)} \cong 52\ uF \tag{3.36}$$

DC-link side:

I_{ripple} (80 kHz) = 33.5 A (value from the simulation)

ΔV_{DC} = 28 V (4% of 700V)

$$C1 = \frac{33.5}{(28 \times 80\ 000)} \cong 15.0\ uF \tag{3.37}$$

Resonant filter:

The goal is to size a low-pass filter to attenuate the HF AC signals. Once the capacitor value has already been calculated, inductor *L* will be derived from the following equation.

$$f_{cut-off} = 1/(2\pi \times \sqrt{LC}) \tag{3.38}$$

Where $f_{cut-off}$ represents the resonant frequency for the *LC* topology filter configuration (Figure 3.12). The capacitor value is adjusted to a standard value. Therefore:

- *C1* = 33 µF (film capacitor)
- $f_{cut-off}$ desired below 15 kHz to reduce significantly the magnitude of HF of AC signals. With a L1 = 10uH, the $f_{cut-off}$ is equal to 8.76 kHz
- *C2* = 68 µF (film capacitor)
- *L2* = 10 µH
- $f_{cut-off} = 6.1\ kHz$ (resonant frequency)

a) Simulate the input and output filter

In a MATLAB environment, the Bode plot is drawn for the transfer function of the low-pass filter. The magnitude of the RLC filter is derived as function of the output across the capacitor:

$$H = \frac{\frac{1}{LC}}{s^2 + \frac{R}{L}s + \frac{1}{LC}} \tag{3.39}$$

The magnitude as function of the frequency is shown in Figure 3.14, for which *C1* and *L1* are taken from the dimensioning made before. A resistive component is added in series to the inductor. It is known that resistive element in circuit translate into losses, thus their value must be lower to increase the efficiency of the converter.

Figure 3.16 shows the results of DAB input current in the frequency domain with the LC input filter and *R* = 3mΩ in series. The resistance will attenuate the magnitude at the resonant frequency. Apply RLC circuit to the DAB converter, in terms of current magnitude at 80 kHz is

expected a reduction of -38.3 dB and -44.7 dB, for the input and output current on DAB, respectively. Figure 3.16 shows a significant decline of the HF current components in DAB compared to the results in Figure 3.13. The addition of RLC filter protects the overall system connected to the DC bus from voltage spike and HF current pulsation. The Bode and phase representation for the output filter was omitted from the document due to the similarity results with the input filter.

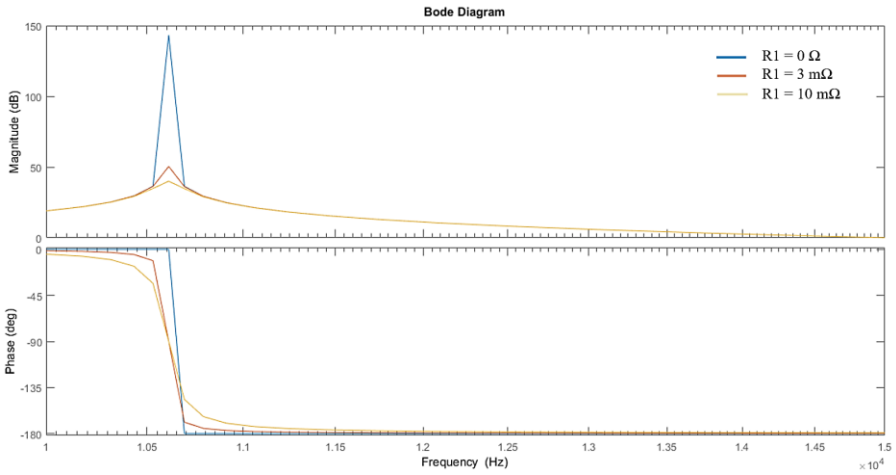


Figure 3.14 – Frequency response of the input *LC* filter, magnitude (dB) vs frequency (Hz) as a function of the series resistance.

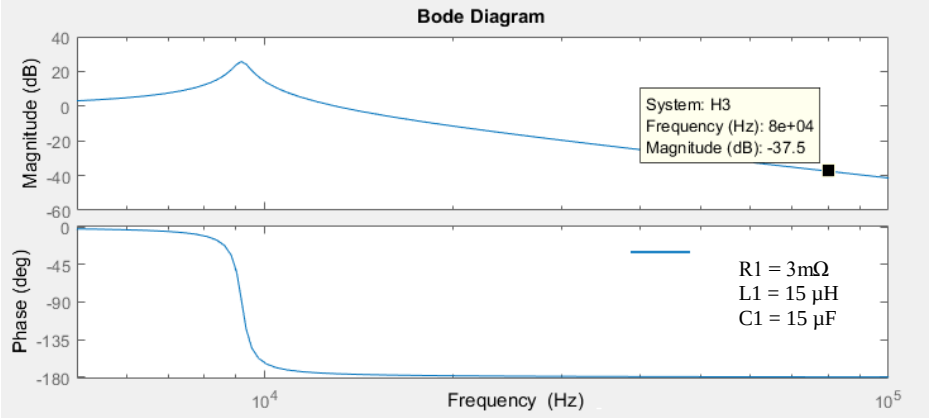


Figure 3.15 – Frequency response of input filter *RLC*.

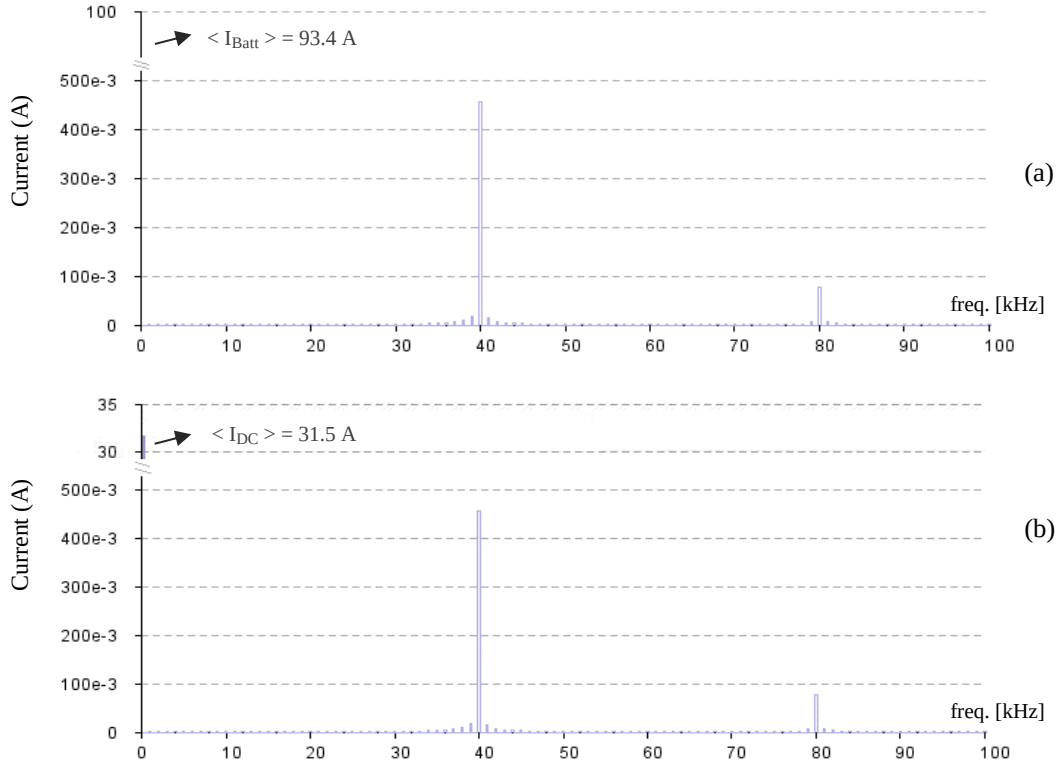


Figure 3.16 – Battery current (a) and DC link current (b) expressed in FFT domain, with *RLC* filters.

3.5. Project of the HF Transformer

Since the beginning, an HF transformer is expected to be dimensioned and included in the DC-DC converter topology. The transformer turn rate N was discussed and determined in section 3.1. This present section will describe the entire procedure to design a transformer.

The value of N has a direct impact on the phase-shift. For example, for a given amount of N, a smaller phase-shift between the AC-square voltage applied to the primary and secondary transformer may be required, to deliver the same power. Figure 3.5 clearly shows this importance. It is known that the voltage in the battery ranges from 200 up to 450 V, but only above 250 V is it allowed to drive the converter at nominal power 22.1 kW. The author of this dissertation was encouraged in to find emerging solutions to improve the power density of conversion. Once the increasing of the operation frequency allows meeting this requirement, and the SiC MOSFET shows to be an excellent candidate to allow frequency above 40 kHz. Later, the feasibility of increasing the switching frequency up to 100 kHz will be explored. The external inductance value required to provide the rated power at the lowest level of battery voltage was calculated and is presented in Table 3.2. in the range of frequencies to be studied.

The transformer is designed in function of the phase-shift, the voltages, the turn rate N and the leakage inductance. Another essential part of the project need be analyzed: the choice of the core and its sizing. The sizing of the core must meet the requirements set in previous sections: the P_N, the F_S, and the transformation ratio. It should be considered during the design, the minimization of the transformer prototype dimensions, the cost, and their intrinsic electric and magnetic losses.

After list all design input required for the HF transformer, the next step is to choose the core material.

- The transformer ratio selected is N:1, where N is 2.15 (Table 3.1);
- HF transformer able to achieve a P = 22.1 kW;
- Considering the external filter L added in series to the transformer to make possible the transit of power in the dc-dc converter, the leakage inductance of the transformer existed and is a part of the transformer. Thus, their value will be a consequence of the imperfect magnetic links between windings.

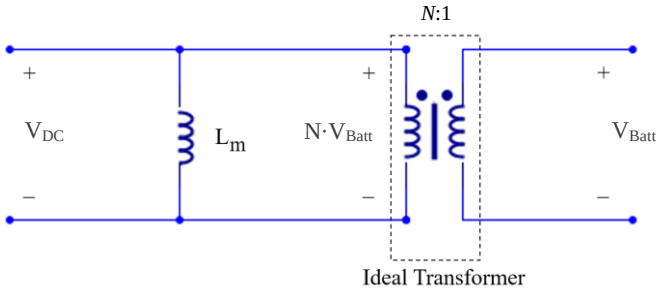


Figure 3.17 – The transformer model used in the simulation with a magnetizing inductance.

3.5.1. Design procedure

A. *External inductor*

The coupling inductor to be placed on the primary side of the transformer was dimensioned early to different scenarios of switching frequency Table 3.2. Their value was chosen to guarantee the maximum transfer power at the low voltage battery level at nominal power (250 V). This inductor will be coiled in the air. Alternatively, the transformer could be designed to have that desired inductance by controlling the leakage inductance, L_{lk}. For this project, the inductance will be considered as an external component.

B. *Transformer*

The magnetic cores used as an example to present the transformer procedure is a toroidal core made by the nanocrystalline material. Compared to the general cores shapes (e.g., with shape E), the toroidal core has smaller core losses than conventional magnetic cores, mainly due to the

curved shape. The dimension of the nanocrystalline core is present in Table 3.3 and the core shape is shown in Figure 3.18.

Table 3.3 – Two nanocrystalline toroidal core with different size and own characteristics.

	Finished dimension (mm)			Ae	ℓ_m	Weight	AL value (μH/N²)	Pc*1 (W Max)
	A Max.	B Max.	C Min.	(mm2) TYP.	(mm) TYP.	(g) TYP.	10kHz +/-30%	20kHz 0.1T
(a)	104.7	25.7	75.3	135.8	286.2	336	13.7	0.14
(b)	145.0	36.0	95.3	419.4	382.8	1,335	31.7	0.56

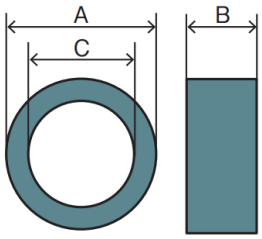


Figure 3.18 – Shape of the nanocrystalline core selected.

Where Ae is the cross-sectional area, and ℓ_m is the mean magnetic path length, also known by MLT (mean length turn). In the appendix is found the core features taken from the manufacture's datasheet. At 40 kHz and 100 kHz with the magnetic field intensity B_m equal to 0.1 T, the core loss per Kg in this toroidal core is expected to be 1 W and 5 W, respectively. The Table 3.4 summarise the core losses and the relative permeability at different frequencies operation of the transformer.

Table 3.4 – Nanocrystalline core losses at the different operating frequency for flux density of 100 mT.

Frequency operation kHz	Bm T	Relative permeability	Core Losses W/Kg
40	0.1	1700	1
80	0.1	1570	3
100	0.1	1500	5

The present sub-section will be divided into the electrical project of the transformer, and finally, the saturation state of the magnetic core is verified when a given external field is applied. Summarily the procedure to optimize the transformer matches these points:

I. Defining a n_{pri} and n_{sec} in terms of winding turns regarding transformation rate N;

II. Calculate the magnetizing inductance by using the equation (2.22);

III. Verify the magnetizing ripple (3.41);

IV. Determining and selecting the winding resistance

V. Window area utilization

VI. Losses analysis at rated condition (P_c – core loss and P_{cu}: copper loss)

Whenever the efficiency of the transformer is not achieved, a new interaction is followed by assuming these two conditions:

a. If the $P_c > P_{cu}$, then increase the cross-sectional area of the core

b. If the $P_{cu} > P_c$, then increase the winding area

*Note: this procedure is adapted from [37] to optimize the size and efficiency of the transformer. The optimization regarding to the leakage inductance is not considered.

VII. Determine the transformer efficiency

B.1 ***Magnetizing inductance***

Beginning with to determine analytically the inductance expected in magnetic core using the equation (2.22). This inductance will be referred to the primary side of the transformer (reference side). The turn ratio is 2.15 and represents the relation between the winding turn in the primary to the secondary side of the transformer. The calculation of this inductance will be a described as a relation with the number of winding turns and the properties of the magnetic core, A_L.

B.2 ***Winding n_{pri} and n_{sec} design***

The first part of the expression (2.22) is used when the magnetic circuit is uniform. Using the second part of the equation $A_L n_i^2$, the magnetizing inductance is derived. Take the turns of wire in primary side, the L_m is estimated by:

$$L_{m.pri} = A_L n_{pri}^2 \tag{3.40}$$

The A_L parameters is founded in core's datasheet, like it is founded in Table 3.3, and the n_{pri} is the number of turns in the primary side.

After determining the turn winding for both sides of the transformer, it is mandatory to calculate the peak magnetic field *B* to verify if the saturation of the core is reached.

The equation (2.21) can be formulated to represent the input voltage of the HF transformer:

$$v_{pri} = L_m \frac{di_{Lm}}{dt} \tag{3.41}$$

The L_m is the magnetizing inductance, and the magnetizing current i_{Lm} across the inductor is expressed by:

$$i_{Lm} = i_{pri} - \frac{i_{sec}}{N} \tag{3.42}$$

B.3 ***Wire sizing and expected copper loss***

Following the procedure to determine the winding resistance and the respective copper losses. The resulting resistance of the winding turn around the transformer core is derived from the expression [28]:

$$R_{wi} = \rho_w \frac{N_i \ell_m}{A_{wi}} \tag{3.43}$$

Where the ρ_W is the electrical resistivity of the conductor, A_{wi} the cross-sectional area of the conductor and the ℓ_m the length of a turn around the core. Considering copper conductor, their electrical resistivity is around 1.68×10^{-8} Ω·m.

The term A_{wi} is now represented by A_{cu} referring to the copper wire. A_{cu} can be associated to the current density in a wire, deduced by:

$$J = \frac{I_{rms}}{A_{cu}} \tag{3.44}$$

A winding with a specific number of turns, the current density is:

$$J = \frac{I_{rms.pri}}{n_{pri} A_{cu}} \tag{3.45}$$

From the equation (3.56) the A_{cu} can be derived. In motor and power transformer application, the density current is normally chosen by the designer engineers to be less than 5.5 A/mm^2. This current density is not restricted at that value, and always will depending of the temperature in the wire. But for an application with a reasonable temperature, 5 A/mm^2 is a conservative value.

B.4 ***Transformer Saturation***

It is essential to verify if the internal field of the core reaches the saturation flux density B_{sat}. After the wire designs, the choices of the number of turns and the selection of the magnetic core, the follows equation must be verified the core saturation, from the magnetic flux applied to the magnetic core:

$$\sum H = \frac{N \times I}{\ell m} \tag{3.46}$$

Moreover, the maximum flux density, B_{max}, is determined by:

$$B_{max} = \Delta B = \frac{V}{4 A_c N F_s} \tag{3.47}$$

Where the A_c is the effective core cross-sectional area.

B.5 ***Transformer efficiency***

The estimation of the transformer efficiency is derived by:

$$\eta_{\%} = \frac{P_{out}}{P_{out} + P_{cu} + P_c} \tag{3.48}$$

3.5.2. Transformer design

The number of turns will be calculated using the nanocrystalline core presented in Table 3.3 (b) using the procedure enumerated before, and assuming the transformer operating at 80 kHz.

1. Defining the winding turns n_{pri} and n_{sec} and the respective Lm:

The expected magnetizing inductance in the primary side is presented in Table 3.5 for different turns rate n_{pri}: n_{sec}.

Table 3.5 – Different configuration of n_{pri}: n_{sec} and the respective primary magnetizing inductance, considering the transformer operation at 80 kHz.

n_{pri} turns	n_{sec} turns	Ratio N : 1	Lm mH
60	28	2.14 : 1	115.00
43	20	2.15 : 1	58.61
28	13	2.15 : 1	24.80
17	8	2.13 : 1	9.38
13	6	2.17 : 1	5.28

2. Sizing wire resistance

Once the transformer is designed for an HF application, it is expected that the current flow is distributed more near the conductor surface. This phenomenon is known by skin effect. The Litz-wire is an excellent solution to reduce this effect because this conductor type is formed by strands with less diameter.

Before calculating the wire resistance, a cross-sectional area must be determined regarding the density current establish before to 5 A/mm^2. The current flowing through the secondary side is higher than the primary side, which the conductor sizing must be regarded as the nominal operating conditions of the secondary bus. The nominal secondary current is $I_{Batt} = 88.4\ A$ (P = 22.1 kW and V_{Batt} = 250 V):

$$A_{cu.2} = \frac{I_{Batt}}{J} = 17.7\ mm^2 \tag{3.49}$$

The $A_{cu.2}$ obtained from the design project is 13.6 mm² and the physical value standard is 13.3 mm². Regarding this, the primary and secondary winding resistance is given in Table 3.6 for different winding turns n_{pri}: n_{sec}.

Table 3.6 – Winding parameters for different scenarios of turn ratio.

np tuns	ns turns	$A_{cu.2}$ mm²	AWG†	A'_{cu} mm²	R_{pri} mΩ	R_{sec} mΩ	Ku
60	28	17.7	4	21.2	47.1	10.2	0.22
43	20	17.7	4	21.2	33.6	7.3	0.16
28	13	17.7	4	21.2	21.9	4.7	0.10
17	8	17.7	4	21.2	13.5	2.9	0.06
13	6	17.7	4	21.2	10.1	2.2	0.05

Note table above:

$A_{cu.2}$ is project cross-sectional area project from (3.49) for the secondary winding | AWG† is the standardised American Wire Gauge | A'_{cu} is the physical value standard

Looking to the Table 3.6, the equivalent resistance value for the primary and secondary winding are satisfactory with the A'_{cu} selected. The calculation to determine the secondary winding resistance is given by:

$$R_{sec} = 1.68 \times 10^{-8}\Omega \cdot m \times \frac{8 \cdot 0.3828\ m}{17.7\ mm^2} = 2.9\ m\Omega \tag{3.50}$$

As mentioned before, it is considered a copper winding, which electric resistivity is $1.68 \times 10^{-8}\Omega$·m. The primary winding resistance is easily determined by $R_{pri} = R_{sec} \times N^2 = 13.5\ m\Omega$.

The *Ku* constant is a factor that referees to the windows area utilization:

$$Ku = \frac{NA_{cu}}{Wa} \tag{3.51}$$

3. *Saturation core verification*

The maximum flux density peak must be calculated to verify the core saturation using the equation (3.46). The current constant presented in the equation represent magnetizing current ripple. Taking the *Lm* from the Table 3.5 and knowing the mean core length ℓm = 382.8 mm, the current ripple is easily derived through the equation (3.41). Some adjustment must be made, and observing the typical shape of the magnetizing current in Figure 3.22, im ripple occurred in a one quarter of cycle of the switching period

$$i_{Lm} = \frac{V_{pri} \times \frac{0.5}{F_s}}{L_m} \tag{3.52}$$

Table 3.7 – Estimation of the magnetic field applied to the toroidal nanocrystalline core and expected magnetizing current ripple with the converter operating at 80 kHz, for two different winding turns.

n_{pri} tuns	n_{sec} turns	i_{Lm} ripple Peak-to-peak A	*Ripple %* from nominal i_{pri}	*H* A/m	Bpeak mT
43	20	0.07	0.24 %	4.2	0.14 << B_{SAT}
13	6	0.83	2.63 %	14.1	0.37 << B_{SAT}

*Note: B_{sat} magnetic peak saturation (1.2 mT)

The resulting magnetic field applied H with the condition enumerates in Table 3.7, and observing the core saturation B-H curve in appendix A.2, it could be concluded that the using nanocrystalline core (Table 3.3 (b)), it still far below from saturation with winding turns 13:6 chosen for an application at 80 kHz. Until a field intensity of H = 30 A/m , it still to be a reasonable value for the transformer operating. However, the higher is the flux density Bm, higher the core losses. The transformer operation is critical after an applied H = 40 A/m since the core is starting to saturate.

4. *Losses*

In other to validate the uses of this core for HF transformer, it is imperative to calculate the copper and core losses. Due to the nonexistence of the constants in the manufacturer's datasheet, was assumed the typical value for the core selected. Therefore, α =1.32, β = 2.1 and K_c = 2.3, from Table 8, assuming the transformer operation at 80 kHz with winding configuration of 17:8, the H =10.4 A/m and the flux density (Bm) is about 0.28 T. And the core losses are estimated to 159 W. Note that the Steinmetz equation (2.26) gives the losses in watt per volume (W/m^3). The core volume determined is about 337.68 cm^3.

Table 3.8 shows an overview of primary and secondary copper losses. It is assumed that the converter operates at nominal, with the V_{DC} fixed, and a constant primary effective current. For the second bridge, the power rate is maintained at nominal and the three battery voltage scenarios are presented in the table below.

Table 3.8 – Copper losses expected for both side of the transformer in a different configuration of turn ratio.

n_{pri} tuns	n_{sec} turns	R_{pri} mΩ	R_{sec} mΩ	V_{Batt} V	$P_{cu.1}$ W	$P_{cu.2}$ W	Ku
17	8	13.5	2.9	400	13.4	8.9	0.06
17	8	13.5	2.9	325	13.4	13.4	0.06
17	8	13.5	2.9	250	13.4	22.7.	0.06

*Note: $P_{cu.1}$ is primary copper losses, and $P_{cu.2}$ is the copper losses in the secondary side.

Transformer configuration with winding turn ratio 17:8 seems to be suitable for the transformer design, besides that the transformer can operate in safety without occurring the saturation risk. The copper losses are reduced on the primary side, and the same for the secondary side with the set turn rate mentioned. With this configuration, the expected core losses at 40 kHz and 80 kHz is 253 W and 159 W respectively.

3.5.3. Discussion

The procedure presented in this section follows the winding optimization technique, looking for the best copper winding structure, selecting the optimum conductor A_{cu} to be placed around the core and to meet the maximum flux required. The cross-sectional area increasing will be limited by the window utilization factor of the transformer. In toroidal cores, the Ku is typically around 0.15 to 0.25. For the primary and secondary winding project, this value was fulfilled, as be seen in Table 3.8. The optimization procedure to dimensioning the electric part of the transformer and thus find the most appropriate core was achieved in this section. At last, following in the Table 3.9 the parameters and specifications derived from the transformer project presented before.

Table 3.9 – Transformer design with a nanocrystalline core

Parameter		Value
Core material		Nanocrystalline
Dimension		Toroidal shape: 145 : 36 : 95.3
Weigh		1.335 Kg
Primary winding resistance	R_{pri}	13.5 mΩ
Primary winding resistance	R_{sec}	2.9 mΩ
Winding turns	$n_{pri}:n_{sec}$	17:8
Expected magnetic flux at 80 kHz		0.28 T
Core losses (80 kHz and 0.35 T)		159 W

3.6. Controller design

Developing a closed-loop control is critical to validate and test the purpose DC-DC converter. The block control that will be suggested is divided into two sub-blocks: one to create the PWM signals for the power switch in order control the transfer power between the two bridges and other block to control the voltage and current in the battery side of the converter DC-DC,

structure of the last block control are shown in Figure 3.19. The signals modulation will be described in section 3.7.4. In the present dissertation, only a voltage and current control will be designed and described for the battery bus. It is assumed that voltage across the DC-link bus is controlled by the second system connected the DAB converter, a power inverter. The closed-loop control will be used to control the voltage across the battery during the dynamic and continuous operation.

The equation (3.31) is rearranged to a numerator/denominator fraction, and some elements of the transfer function are not considered for the topology that was analyzed. The output transfer function is resumed into:

$$G_{out} = \frac{\hat{\imath}_{batt}(s)}{\hat{d}(s)}\bigg|_{\hat{v}_{is}(s)=0,\,\hat{v}_{os}(s)=0} = \left(\frac{1}{R_0 + L_2 s}\right) \cdot \frac{x - yp/G_{A1}(s)}{nG_{A2}(s) + yr/G_{A1}(s)} \tag{3.53}$$

$$G_{A1}(s) = \frac{1}{R1} + \frac{1}{L_s s} + q \quad \Big| \quad G_{A2}(s) = C_3 s + \frac{1}{R_0 + L_2 s} - \frac{z}{n} \quad \Big| \quad R_{eq} = 2R_s + \frac{2R_s}{n^2}, \; n = 1/N$$

Note that z, q, p, r, and y depend on the *D*' (phase-shift), and on the voltage supply V_{Batt} and V_{DC} directly. Adjustment is made for the $D = 0.5 \times D'$. Replacing the constant of the transfer function by the parameters sized in previous sections and assuming the F_S at 40 kHz, a V_{DC} = 700 V, and a V_{Batt} = 325 V, the Bode representation is shown in Figure 3.19. This plot shows the frequency response of the DAB converter in term of output and input, which the phase-shift is the input. Looking in Bode at low frequency, the gain is around 46 dB. Close to the angular frequency of 38.3×10^3 rad/s (~6 kHz), the amplitude peak response is about 85 dB and -180 degrees. At the input/output point of view, this means that the output (output current) is higher than input about 216 times (85-38.3 dB) and the output signal is lag 180 degrees behind the input at the same frequency (~6 kHz). This represents a significant delay of the system in responding quickly, and it is not the intended result for the system. Therefore, a controller must be introduced to compensate the delay. The second order peak amplitude in Figure 3.19 is due to the resonance introduced by the *LC* filter. Observing the Figure 3.21 (b) is concluded that the system has an unstable step unit response during the transient regime. Simplify the expression of G_{out} such that the numerator and denominator have the format expressed in (3.54), it is observed that the system is of the quarter order. With the aim in developing a closed-loop current control for the output current in battery bus and knowing the system order of the transfer plant function (3.53), a PI controller can be used to monitor and regulate the desired current. Later, a second PI controller will be added to regulate the current in the battery side, and this controller will be external to the

first PI controller mentioned early. The structured of the control loop is shown in Figure 3.19. Later in section 3.8. this controller will be designed and simulated.

$$H_{OUT} = \frac{a_n^2 s + (\dots) + a_1 s + k1}{b_n^4 s + (\dots) + b_1 s + k2} \tag{3.54}$$

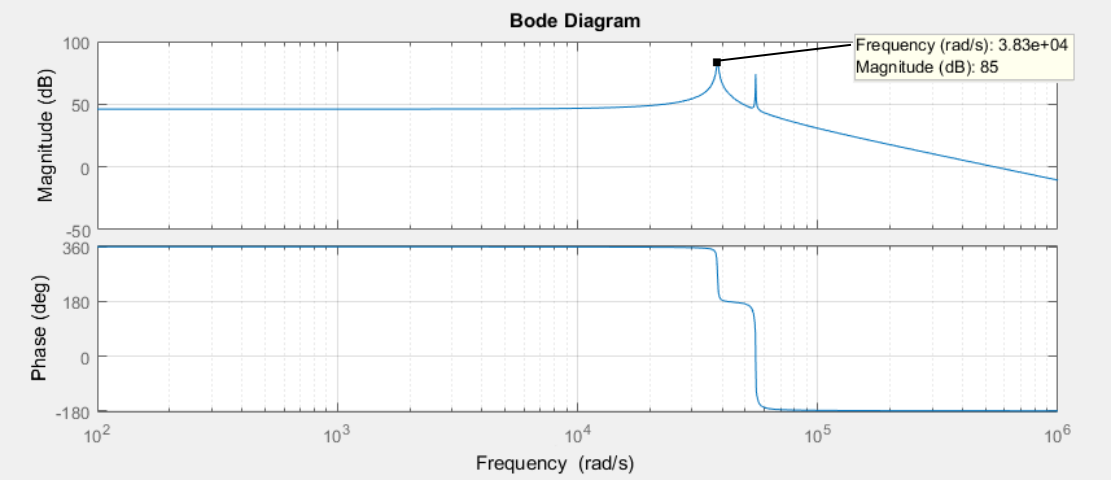


Figure 3.19 – Bode plot representation of the output transfer function with D=0.5, input/output filters and other non-idealities.

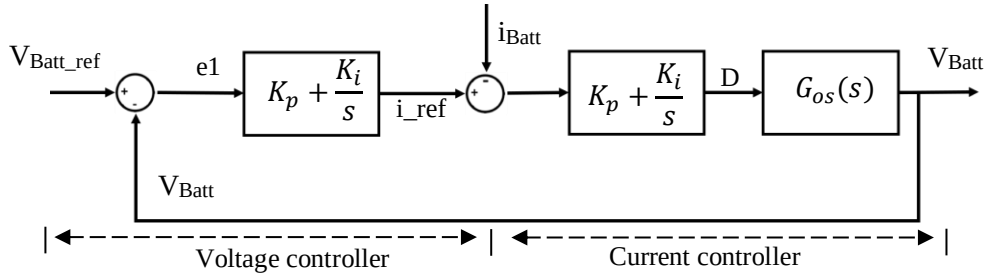


Figure 3.20 – Purposed closed-loop controller for DAB converter.

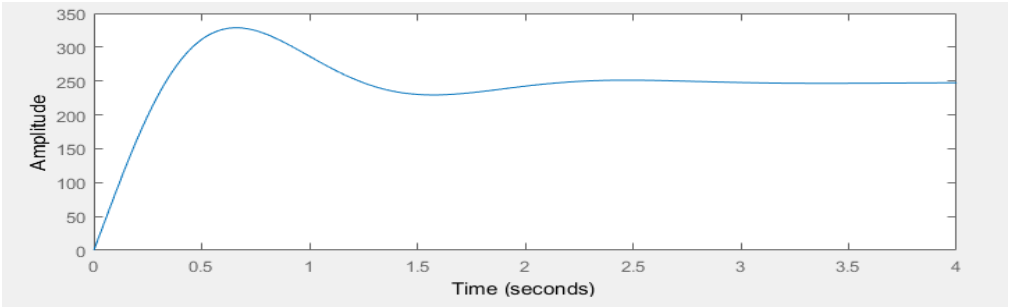


Figure 3.21 – The unit step response of the system in open-loop at 40 kHz.

3.7. Simulation in open loop

In this section, the simulation of the detailed DAB converter model will be described and explained. It will be included in the same simulation a thermal model to increase the accuracy of the simulation. The aim in estimating the major losses in the power devices is done to better understand the influence of losses and consequently the temperature in the converter efficiency. Furthermore, it helps to choose the appropriate power device and even more critical, the heatsink. The high temperature in the power device junction can reduce their lifetime or in the worst case destroy it.

The DC-DC converter to study, the DAB case under phase-shift modulation, will be implemented in the circuit simulator GeckoCIRCUITS®. The converter circuit includes an ideal input and output supply sources, *LC* filters are coupled to both output H-bridge, and the resistive connections are neglected. The MOSFET components are used in the model, and they are not ideal. Due to the straightforward implementation in the referred simulator, the losses properties of the power device from the datasheet are added into the MOSFET component models. The HF transformer is assumed ideal for the simulation environment, and a magnetizing inductance is included in the transformer model. A first simulation is made to understand the current rate expected in each bridge to select a suitable semiconductor.

The thermal model allows extracting only the macro losses from the converter, since the other non-ideal components are still considered as ideal, as for example, the assumption of the ideal transformer. Furthermore, in addition to the semiconductor losses estimation from the simulation environment, the losses in some selected magnetic cores will also be analyzed and predicted by an analytic deduction.

Table 3.10 – Parameters of the Input and output filters and respective requirements.

frequency	C_{DC}	V_{DC} % of ripple	$L1$	$f_{RES.1}$	C_{Batt}	V_{Batt} % of ripple	L2	$f_{RES.2}$
40 kHz	33 µF	4 % - 28 V	10 µH	8.8 kHz	100 µF	5 % - 12.5 V	10 µH	5.0 kHz
80 kHz	15 µF	4 % - 28 V	10 µH	13.0 kHz	68 µH	5 % - 12.5 V	10 µH	6.1 kHz

Table note: $f_{RES.1}$ – resonant frequency of the *LC* primary filter.

3.7.1. Magnetizing inductance

The magnetizing inductance is usually neglected in simulation since the high value translates in a low interference regarding the low AC ripple in the transformer. The magnetizing current in

PWM converter with magnetic cores (e.g., flyback topology) has a triangular shape typically. The L_m is introduced into the simulation model to add non-idealities.

The L_m can be derived by the equation (2.21). Consider the equivalent model in Figure 3.17, where the magnetic inductance is referred to the primary side, and the voltage across the L_m is the primary voltage. Assuming the DAB converter simulated at switching frequency of 40kHz, the Lm value can be approximately obtained by:

$$L_m = \frac{V_{pri}\frac{0.5}{F_s}}{diL} \tag{3.55}$$

Where the diL is the peak-to-peak current ripple and a half of switching period is considered. It is chosen half period because, analysing the L_m current waveform represented in Figure 3.22, when a positive voltage is applied across the terminals of the transformer primary side, the magnetizing current increases from the minimum to maximum, until the moment when the voltage turns to negative. The 50% of duty cycle is inherent of the traditional modulation. Then it is considered a half switching period. The results in Figure 3.22 where obtained from the DAB simulation with the transformer model represented in Figure 3.17, in a steady state regime.

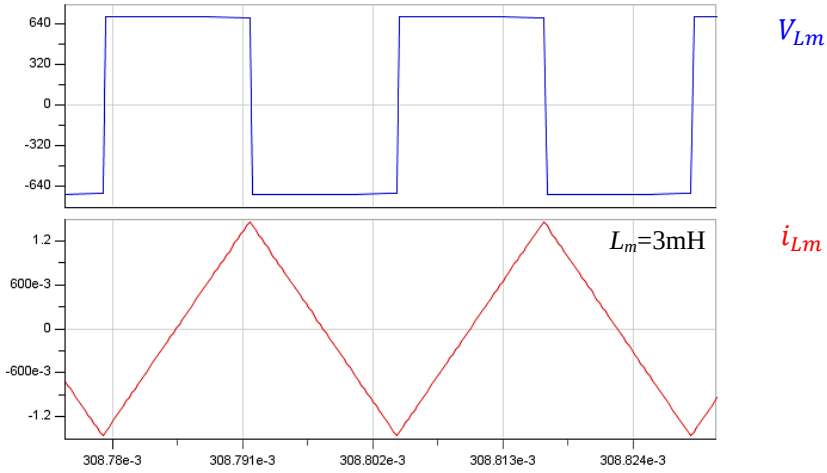


Figure 3.22 – Waveform of the magnetizing current on *Lm* from the simulation.

A 3 mH of magnetizing inductance is assumed to be a part of the ideal transformer. The primary voltage of 700 V is applied, and by the equation (3.41), the peak-to-peak current of 3 A is expected in the magnetizing inductance, at a 40 kHz operation. So, the magnetizing current ripple (peak current) is 1.5 A, which is less than 5% of the nominal current from the converter requirements. In a perspective of the transformer core, the magnetizing current is responsible for creating the internal flux.

$$\%\ of\ ripple = \frac{1.5\ A}{nominal\ current} = \frac{1.5\ A}{\frac{22100}{700}} \times 100 = 4.7\ \% \tag{3.56}$$

3.7.2. Parameters of the simulation model

Taking all the considerations derived from the requirements to design the DC-DC converter; the key parameters are summarized in Table 3.11.

The results from the simulation help studying the converter in the following important aspects:

- Power losses analysis and the current stress that semiconductors must handle in the DAB topology.
- Choose the proper active device.
- Predicting the temperature and helping to select the suitable heatsink in terms of size and capability to extract heat.

Table 3.11 – Circuit specification of the detailed DAB DC-DC converter simulated in GeckoCIRCUITS® environments

Power MOSFETs	*Note
Transformer turn ratio	2.15:1 (dc-link side: batt side)
Link-inductor	45 µH
Magnetization Inductance (L_m)	3 mH
Input inductor L1	10 µH
DC Capacitor (DC-link side)	33 µF
Output inductor L2	10 µH
DC Capacitor (Battery side)	100 µF
Output power	22.1 kW
Galvanic isolation	Ideal transformer
Switching frequency	40 kHz

*Note: The simulation will be made with modules MOSFETs (CAS120MM12BM2) and with a discrete MOSFETs (C2M0025120D).

3.7.3. Thermal model derivation

The circuit simulator GeckoCIRCUITS® has a simple and intuitive interface that allows to create a thermal model for the semiconductor. Based on the conduction and switching losses information was given by the datasheet's module or discrete MOSFETs, it is easy to set those parameters into the circuit simulator (Figure 3.27 and Figure 3.28). The dashed curve in Figure

3.27 was a result of interpolation with the 25 ºC and 150 ºC curve. This feature gives an idea of the potential of the GeckoCIRCUITS® to make interpolation during the simulation based on different temperature. Later the temperature dependence with the power losses measured will be explained. Let's first explain the thermal model used to estimate the junction and heat-sink temperature. The dynamic behaviors could be seen from the two approaches as seen in Figure 3.23: an *RC* network model (also known Foster model) or a Cauer model. Both are used to represent the transient and steady-state thermal behaviors.

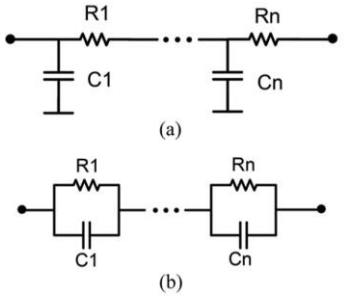


Figure 3.23 – Equivalent thermal network. (a) Cauer model and (b) Foster model respectively [38].

The Foster network is the most common model used because some datasheets provide the *RC* parameters. The Cauer network is more equivalent to the physical structure of the device, and it is the best approximation for the thermal behaviors [38]. However, this model is more difficult to derive and use. Although the Foster model has no physical meaning, it is easy to extract the temperature behaviors in each node of the network model (e.g., from the junction or heat sink node).

For the circuit simulation, the thermal model showed in the Figure 3.25 will be used. The model consists in thermal resistance in series like the configuration model given in the Figure 3.24.

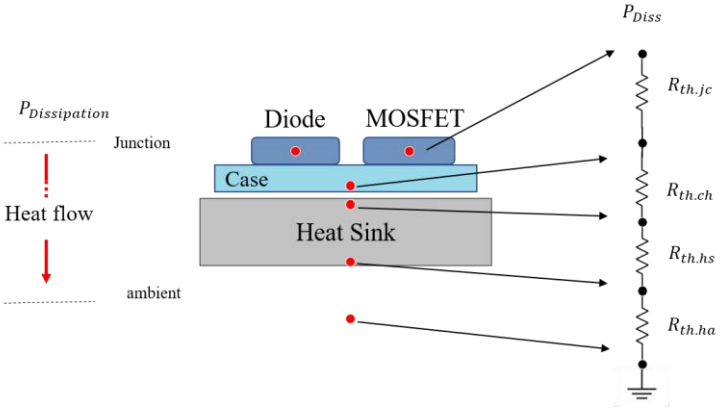


Figure 3.24 – Equivalent thermal model resistance in a network configuration.

A note to the thermal interface (TIM) resistance chosen to be an interface between the case package of the device and the heatsink, represented by $R_{th.tim}$. Regarding the capacitors in parallel with thermal resistance in Figure 3.25, their value is chosen to filter the power losses ripple and to get the average losses. The capacitance value does not influence the temperature measured in each node, in a steady state operating point. The dashed line around the losses block, Figure 3.25, it is used to get the transient semiconductor losses during the simulation. This block can separate the switching and conduction losses. The *RC* thermal parameters are found in the appendix for two MOSFET solutions, as will be discussed later. The heatsink was selected to has enough space to include four MOSFET module structures with a width of 62 mm each. The same heatsink parameters are used for discrete MOSFET solutions. The thermal resistance of the heatsink was determined considering a forced air cooling at 5 m/s.

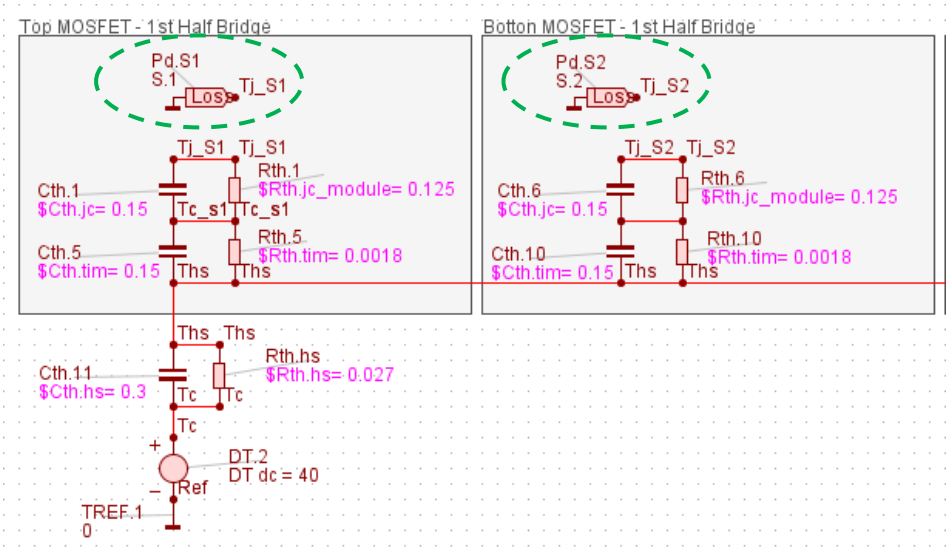


Figure 3.25 – Part of the thermal model to the MOSFET and the heatsink designed in GeckoCIRCUITS® environments.

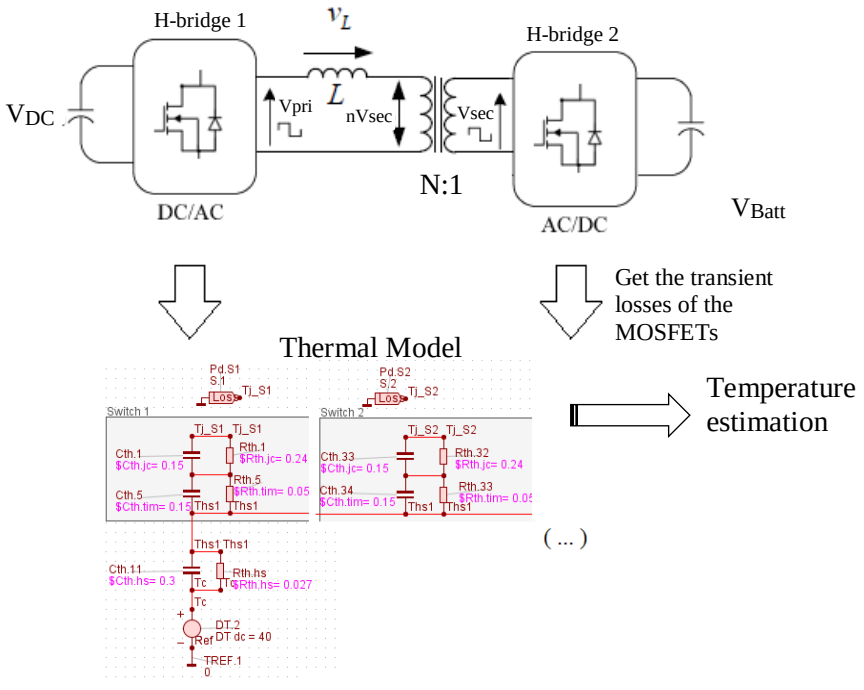


Figure 3.26 – Functional diagram of the implemented thermal model.

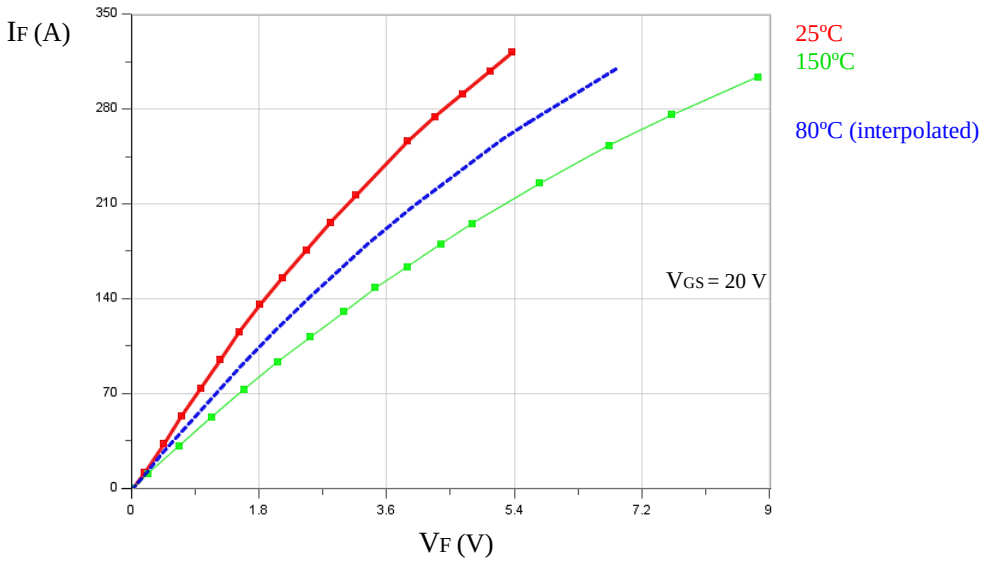


Figure 3.27 – Curve of the conduction losses characteristic from the datasheet's module CAS120M12BM2 set in the circuit simulator.

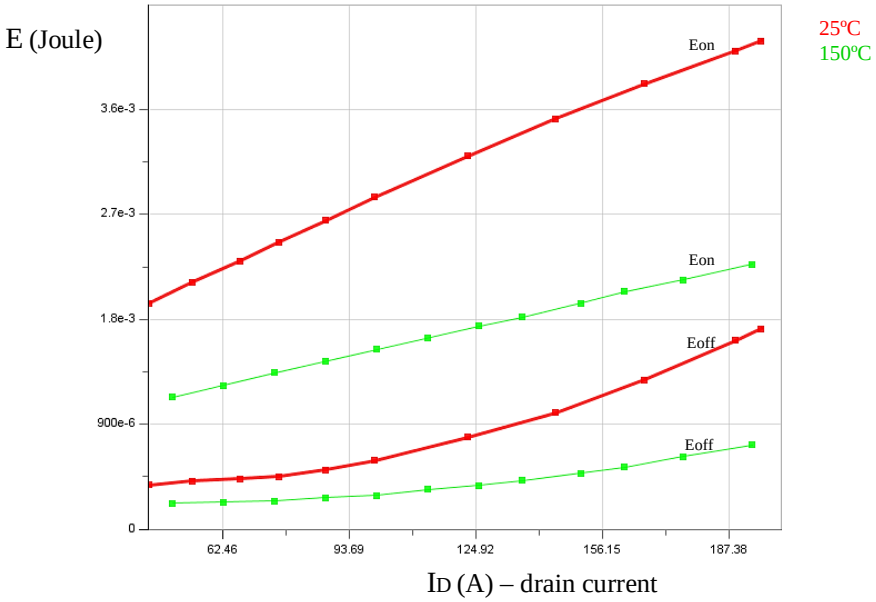


Figure 3.28 – Curve of the switching losses characteristic at 25ºC and 150ºC from the datasheet's module CAS120M12BM2, separated by turn-on and turn-off losses.

Before presenting the simulation results regarding the semiconductor power losses and efficiency at different switching frequencies, it will be explained the block that represents the modulation control created to generate the PWM signals for all MOSFETs.

3.7.4. Modulation circuit - PSM

The traditional modulation is easily implemented in the circuit simulator. The modulation model observed in Figure 3.29, contains two square signals generated by configurable block RECT. Both rectangular signals have 50% of duty cycle with a period of $1/F_s$, where F_s is the switching frequency. The second square PWM signal, at the bottom of the image, is shifted from the first PWM signal, in the top, by a phase-shift given in degrees (phase.2). It is assumed that between the PWM signal and its complementary signal (e.g., gs1s4 and gs2s3 signal respectively) there is no interception. It means that in the same leg, the MOSFET in the top never turn-on at the same time of the MOSFET in the bottom. In a practical implementation, the turn-on of both MOSFET in the same leg translates in a short circuit of the leg and consequentially of the power supply source. This type of events must be avoided. A practical solution consists in introducing a dead time between the PWM signal to the MOSFET in the top and the complementary PWM signal in the bottom MOSFET. All PWM signals for the two bridges are represented in the Figure 3.30.

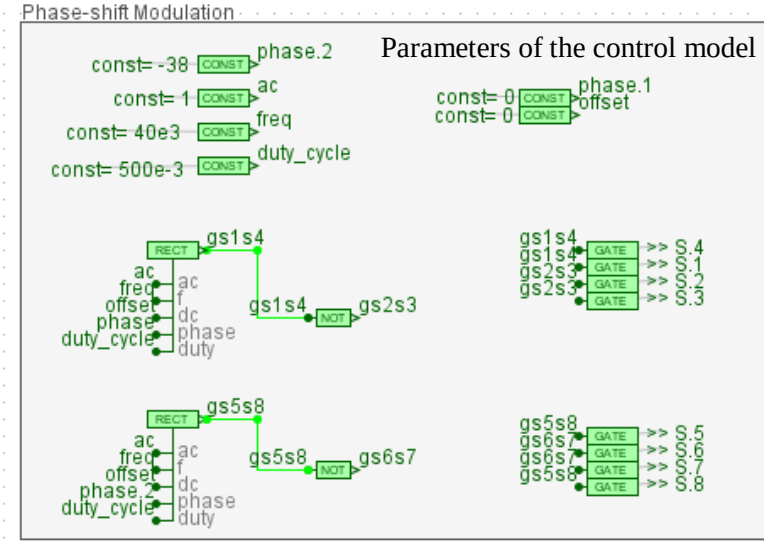


Figure 3.29 – The control model to implement the traditional phase-shift modulation

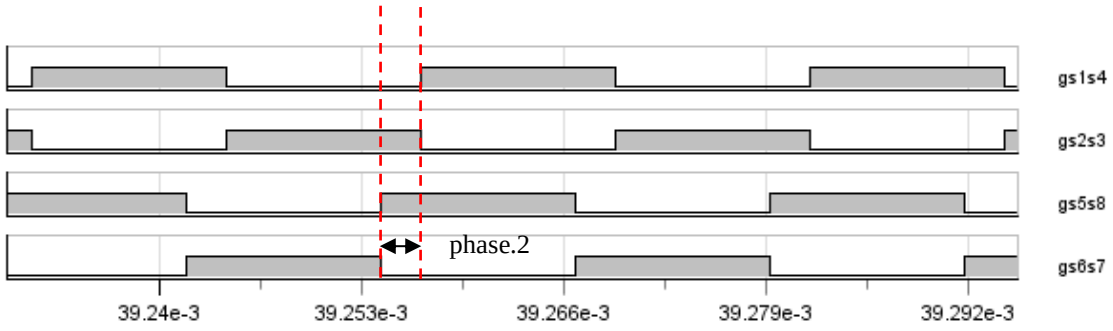


Figure 3.30 – PWM signals under single phase-shift modulation.

3.7.5. Results of the simulation

Considering the control diagram presented before and taking into account the thermal model derivation explained to estimate the temperature in different nodes, the inclusion of switching and conduction losses model into the components MOSFET and assuming the ideal transformer and the supply source. The next results are obtained from the circuit simulator.

The time step has an impact on the accuracy of the results. First simulations made, have allowed analyzing the transient phenomenon, and help to find the optimum time step. This parameter was chosen carefully, a value of 45 ns was defined for all simulation. In the environments simulation when the MOSFET of the converter operates at 100 kHz, the number of samples per period is equal to 222. It is a good number of points per simulation cycle.

a) Simulation of the DAB in steady-state regime:
   - Forward operation of the DAB: V_{DC} = 700 V and for the worst case scenario in the battery V_{Batt} = 250V. The results from the simulations are presented and which it is shows the key waveforms of the primary and secondary voltage at the transformer terminal and the transformer current in the external filter L (Figure 3.31).
   - Reverse operation mode at close the nominal power (charging battery): V_{DC} = 700 V and V_{Batt} = 325 V (Figure 3.32).

b) Evaluate the DAB efficiency at different frequencies for low voltage on the battery. All simulations are performed at nominal power 22.1 kW, with V_{Batt} = 250 V and the DAB circuit operates in discharging mode.
   - 40 kHz – 120 kHz with module MOSFET CAS120M12BM2
   - 40 kHz – 120 kHz with discrete MOSFET and a parallel power devices configuration of 2xDC 3xBatt. The first H-bridge has two parallel MOSFET in each switch position, and three parallel MOSFET has implemented for the second H-bridge.

c) Reactive power circulation analysis with a zero phase-shift.

Forward operation – discharging mode:

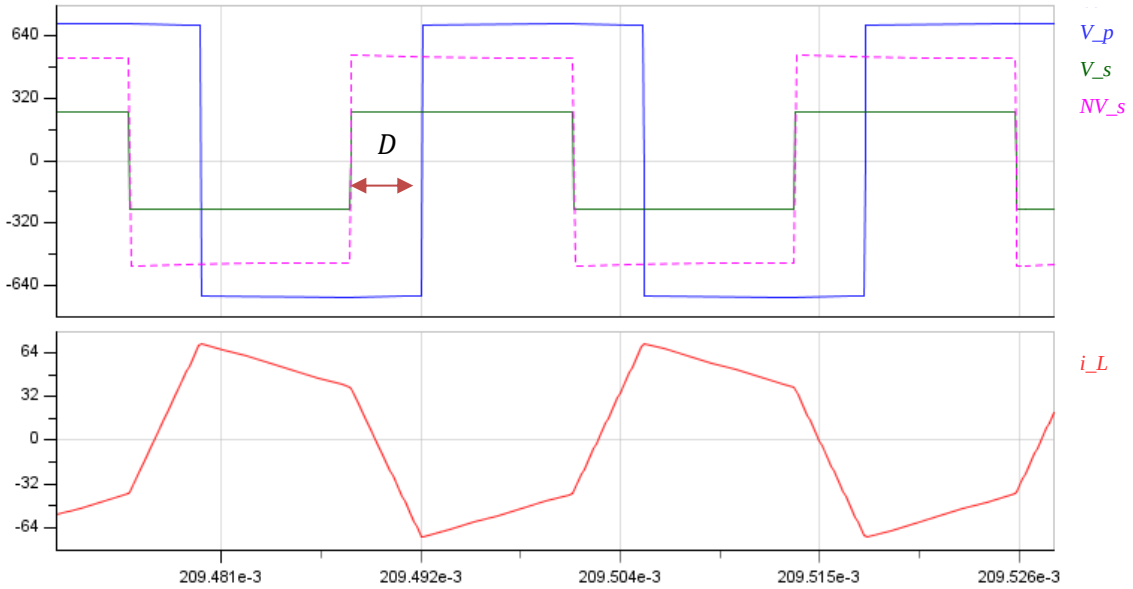


Figure 3.31 – Simulation of the DAB under PSM at 40 kHz, in nominal power and $D = 0.607$ meaning 54.7º of phase-shift: steady-state regime.

Reverse operation – charging mode:

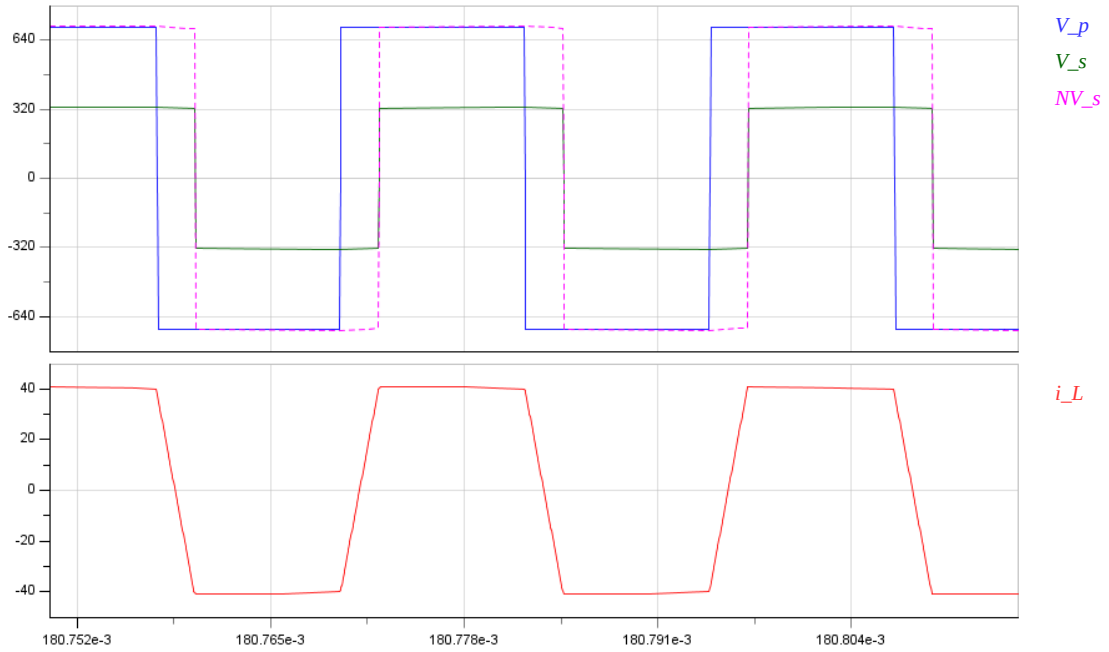


Figure 3.32 - Simulation of the DAB under PSM at 40 kHz, in nominal power and $D = 0.607$: steady-state regime.

Efficiency performance at different frequencies:

It was considered an ideal transformer, then only the semiconductor losses are represented.

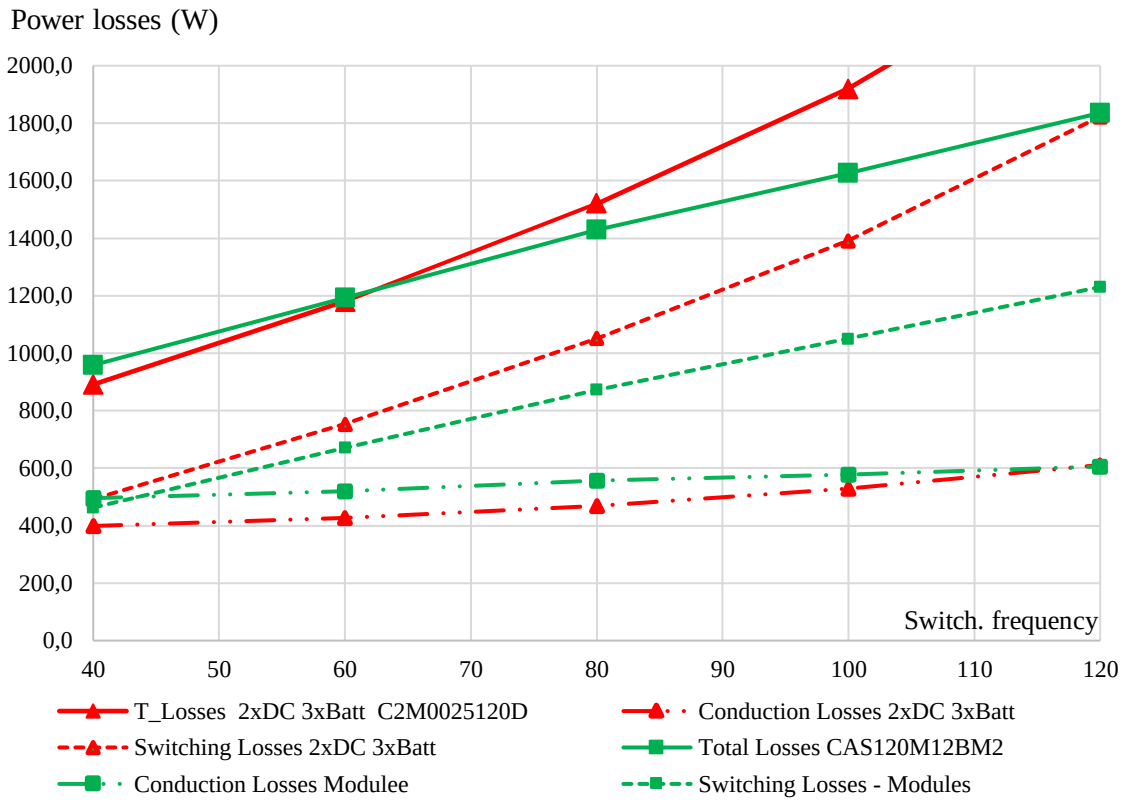


Figure 3.33 – Power losses on semiconductors measured from the simulation some different switching frequencies at nominal transferred power with 250 V on the battery (discharging operation) for two different power switch solutions.

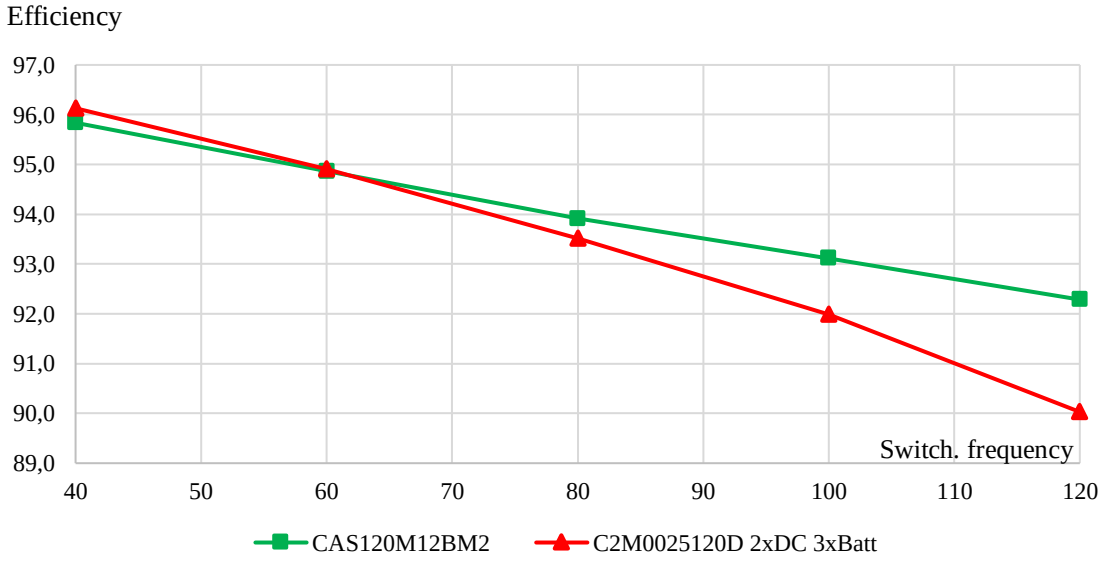


Figure 3.34 – Efficiency comparison between the module and discrete MOSFETs for DAB circuit performed at nominal transferred power, in a discharging mode with 250 V on the battery.

Table 3.12 and Table 3.13 present the temperature withdrawals from the thermal model implemented. The simulation was performed with DAB at nominal power in a discharging operation, with two different MOSFET solutions, and they are presented in the respective table. It is simulated in case that V_{Batt} = 250 V, and V_{DC} = 700 V. The ambient temperature for the thermal model was assumed at 40 ºC.

Table 3.12 – Average temperature estimated in Celsius from the thermal model with discrete MOSFET.

F_S	*Tj_Batt (avr)*	*Tj_DC (avr)*	*T_hs*	*Tcase_S5*	*Tcase_S1*
40 kHz	78	86	64	70	72
60 kHz	89	104	72	78	84
80 kHz	102	124	81	89	98
100 kHz	117	148	92	102	113
120 kHz	137	177	106	118	133

(C2M0025120D 2xDC 3xBatt)
Tj_DC – average junction temperature on active devices in DC-side
Tc_S5 – average case temperature on device S5

After simulation of the DAB converter with the thermal model initial purpose, if it is verified high temperature, the new procedure follows in to find other power semiconductor or select a heatsink with lower thermal resistance.

Table 3.13 - Average temperature estimated from the thermal model with MOSFET module.

F_S*	*Tj_Batt (avr)*	*Tj_DC (avr)*	*T_hs*	*Tcase_S5*	*Tcase_S1*
40 kHz	83	79	65	66	66
60 kHz	91	89	72	70	71
80 kHz	100	101	78	78	79
100 kHz	109	111	84	84	84
120 kHz	117	121	90	89	90

*switching frequency used on CAS120M12BM2 model, in a circuit simulator.

Reactive power circulation:

| *Operating condition:* V_{DC} = 700V, V_{Batt} = 250 V, F_S = 80 kHz and zero phase-shift.

Observing the DAB equation which describes the power transfer (3.1) with zero phase-shift, the active power transit is zero and there only existing reactive power circulation. The reactive current

circulation in DAB is more significant when the converter is operating an unbalance primary and secondary rate voltage, Figure 3.35.

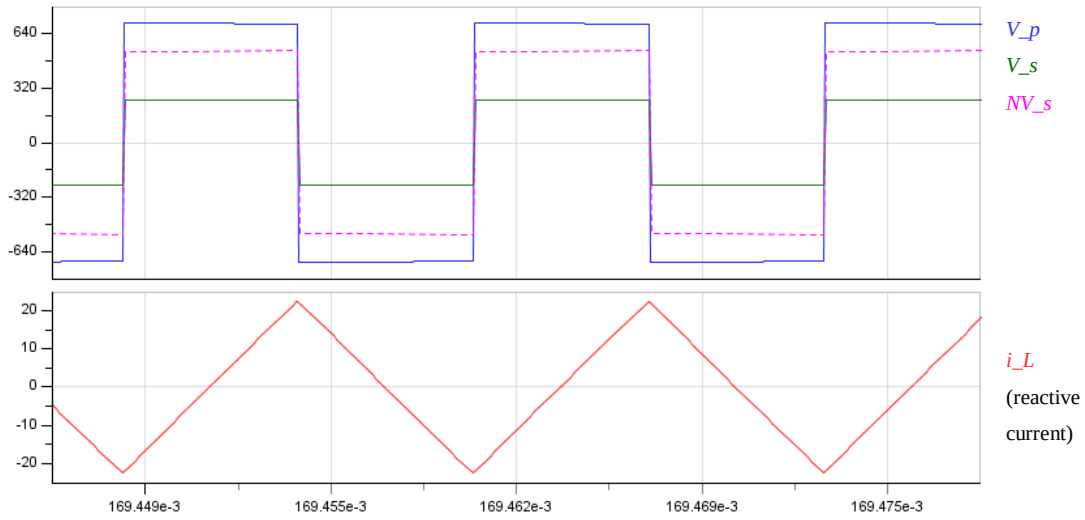


Figure 3.35 – The shape of the voltage applied to the transformer terminals and the transformer current drawn with zero phase-shift.

Auxiliary Snubber Capacitors

With the purpose of reducing the switching losses, on the first H-bridge, an auxiliary snubber capacitor is connected in parallel to each MOSFET. The dead time for minimizing the snubber losses is given by the equation [39]:

$$T_{dead} = \frac{\pi\sqrt{LC}}{2} \tag{3.57}$$

Where *C* in the equation (3.57) is the capacitance equivalent by the sum of the snubber capacitance *Cs* and the parasitic drain-to-source capacitance of the specific MOSFET. And the L is the external parasitic inductance.

Set the dead time to 9 ns, and *L* = 45nH, then the *C* = 7.3 nF. For the simulation , the *Cs* was defined as 5 nF.

Table 3.14 – Results from a simulation of the DAB converter at rated power, 40 kHz and V_{Batt} = 250 V.

	Total losses DC side	Total losses Batt. side	Cond. losses – DC side	Switch. Losses – DC side	Cond. Losses Batt. side	Switch. Losses Batt. side
Without *Cs*	1148	772	129	1019	400	373
With *Cs*	818	7541	116	701	385	370

The introduction of the snubber capacitance across the MOSFET allows to significantly reduce the total switching losses for the power device in the first H-bridge, as can be observed in Table 3.14. The reduction of the losses has as a consequence result in the temperature reduction, Table 3.15. For this simulation the snubber capacitor was implemented only in the first H-bridge, this to understand the impact on power losses. Due to the benefit of using a snubber capacitor in parallel with MOSFET, it is consensual to its use in all converter's semiconductors.

Table 3.15 -Average temperature obtained from the thermal model.

	Tj_dc	*Tj_Batt*	*T_hs*	*T_case_S1*	*T_case_S5*
Without *Cs*	147,6	117	92	113	102
With *Cs*	122	107	82	98	98

3.7.6. Discussion

Based on the simulation results, the thermal model is a useful tool to investigate the reliability of the power switches in HF application. As seen in the Figure 3.31 at 80 kHz, the DAB converter with discrete power switches has higher losses (conduction + switching losses) than the converter model with the power module. However, the thermal model behavior shows a different scenario. Observing Table 3.12 and Table 3.13, the converter with discrete MOSFETs at 80 kHz shows that the power devices of first H-bridge, have approximated 20º C more in the body junction than the devices in second H-bridge. A 100 kHz, the high temperature on the device in first H-bridge makes the operation impractical at this switching frequency level. Although, the temperature in the heatsink and the other power switches placed on the second bridge (battery side) present a reasonable temperature, even at 100 kHz. The reason for high junction temperature verified in discrete power switches of the first bridge is due to the hard switching events occur in this bridge during the discharging mode. This explains the significant increase in the switching losses, while the conduction losses have a slight increase, as can be observed in Figure 3.31. On the other hand, the temperature could be reduced by selecting another heatsink, or even using different heatsinks to place the power devices of each H-bridge separated. However, this procedure only deals with the temperature, but the losses inherent in the hard switching will still happen under the traditional modulation. A possible solution is using a snubber capacitance in parallel with the MOSFET to enable ZVS and to reduce the switching losses and overvoltage, during the turn-on and turn-off of the semiconductor.

3.8. Simulation in closed-loop

Beginning with the current control closed-loop to monitor and regulate the battery current in the DAB simulation. Take the output transfer function (3.53) and assuming all parameters sized, another parameter will be considered: a damping resistance is now introduced in series with the capacitor *C2* and *C3*, as shown on the DAB circuit of Figure 3.8. Damping resistors are included because they are part of the capacitor itself. The *R1* and *R2* must have a resistance value much lower than the filter reactance placed on outside of the converter. Ten times smaller is a conservative value for the damping resistor because it must be ensuring the role of the DC bus capacitor in to suppress the current ripple from the converter. Table 3.16 gives the reactance value of the inductor filter at different frequencies. Assuming the operation converter at a switching frequency 40 kHz, in the outlet of the converter the current pulsation is given at 80 kHz. Taking the information from the below table, *R1* and *R2* are design to 38 mΩ. All parameters are summarized in the appendix (Note 1).

Table 3.16 – Reactance of the inductor sized early.

	frequency kHz	Reactance Ω
L1 = 10 µH	80	5.0
L1 = 10 µH	120	7.5
L1 = 10 µH	160	10.1

The infinite margin shows in the Bode diagram of the Figure 3.37 meaning that the system is stable in all range of the frequency operation. The PI controller has the format shown in (3.34), and the constant parameters were tuned in MATLAB® software to achieve the best performance in time for the controller.

$$\mathrm{PI}(s) = K_p + \frac{K_i}{s} \tag{3.58}$$

Looking at Figure 3.36, the response of the second-order model to a unit step, incorporating the current controller PI, has a satisfactory response and can be now setting in the model circuit. In the appendix can be found the closed-loop block implemented in the simulator software, Figure A.1. Note that for the results showed in the Figure 3.38 only the current controller block was used. The parameters for the PI controller are presented in table

Table 3.17 – PI controller parameters

Kp	8e-3
ki	4.7e3

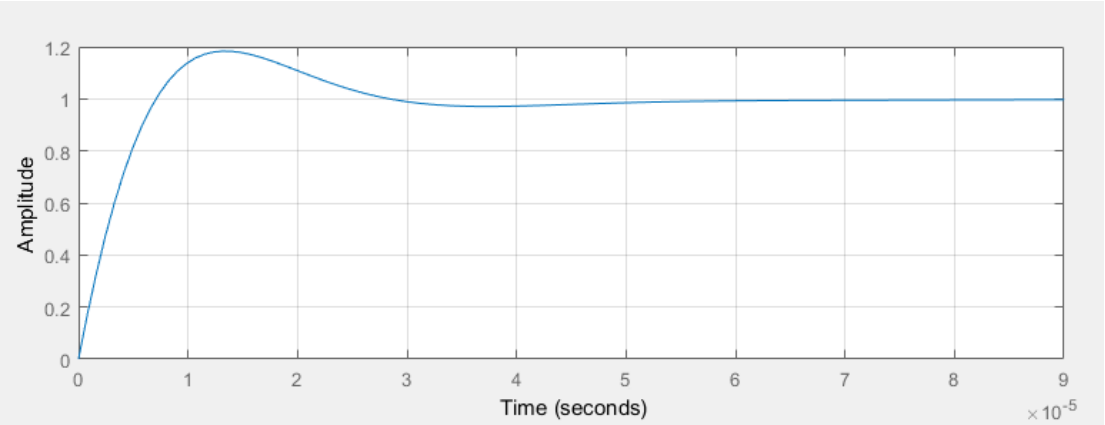


Figure 3.36 –Step unit response of the second-order system with a PI controller in closed-loop.

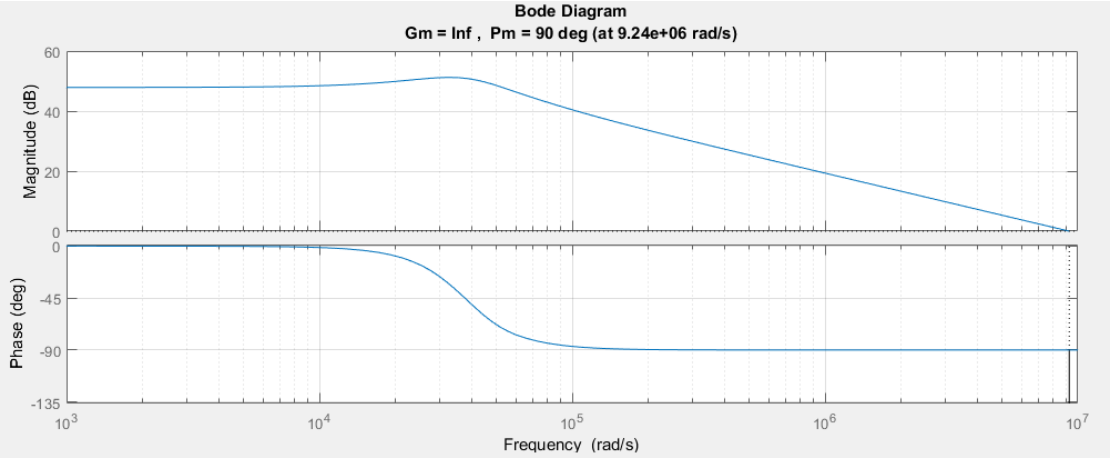


Figure 3.37 – Bode diagram of the output transfer function with D = 0.4, and includes input/output filter, damping resistors, and other non-idealities.

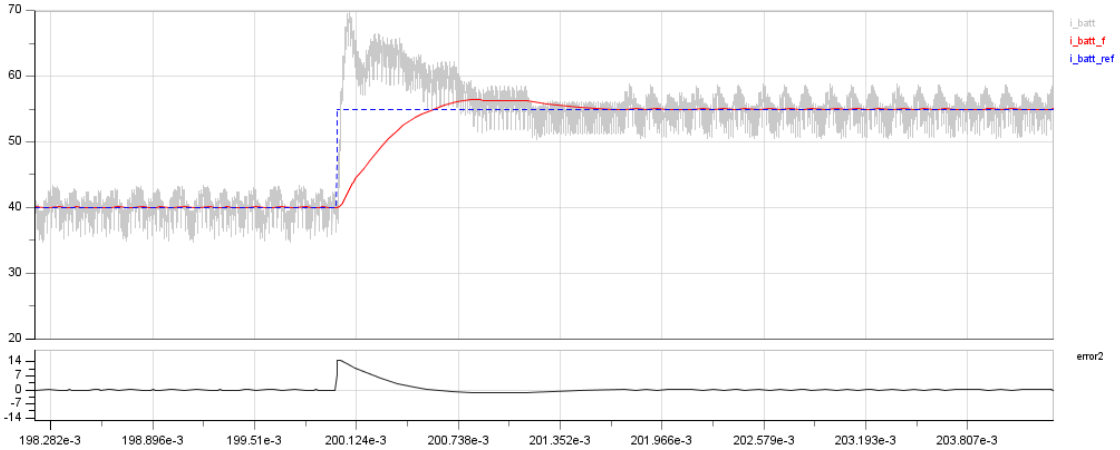


Figure 3.38 – Dynamic response of the DAB converter to a change of the discharging current imposed to battery following a reference, at 40 kHz and a battery voltage of 250V.

Note: where the parameters of figure: i_{Batt} is the current measured in the simulation; i_{Batt_f} is the average current obtained with a low pass filter, and the dashed line represents the current reference. The phase-shift error from the PI-controller is shown on the Figure 3.38 bottom.

3.9. Conclusions

In this chapter was studied the structure of the isolated and bidirectional DAB converter topology. The main waveforms in the steady-state regime were shown and obtained and performed in simulator environments. Another aspect of the converter was taken, namely the dimensioning of the passive components and the passive filters are analyzed. A small-signal model was presented with the support of literature. This model is based on the major losses in the converter, which the conduction losses on the power semiconductors, also include the input/output filters dimensioned. The transformer power losses were not considered in the model either in the simulation. At last, an open-loop simulation is made to obtain the efficiency performance of DAB converter considering in the circuit model different approached of power MOSFETs, discrete and module structure. The effect of using snubber capacitor in parallel with MOSFET on DAB converter is also analyzed. Simulation in closed-loop with PI-controller for output battery current regulation was designed

Chapter 4

Converter - project proposal

After the study and simulation of the DC-DC converter, the next step would be the implementation of all system formed by the converter prototype. Due to the important considerations on the SiC-based semiconductors implementation in the overall system, and the motivation to study further the aspect to driver this type of power switches, present chapter will focus in the design of the circuit drive to generate the command signals. Moreover, the conditioning will be considered and implemented between the controller and the circuit driver. The isolation of high power level and the logical level will be analyzed and chosen as a requirement. The market search will be made related to the power switches module and discrete available and more appropriate for the project.

4.1. Power switches

Follow in the table the main characterization of SiC MOSFET from the well-known manufacturer, Wolfspeed, ROHM Semiconductor and Semikron. Table 4.1 summarizes the main parameters of each power device searched, such the nominal blocking voltage V_{DS}, the continuous operation current at a reference temperature (ref. 25ºC), the power dissipation, the price, and among other characteristics are presented. The result of the search regarding the commercial SiC MOSFET, it shows that those devices are mainly produced for 1.2 kV and 1.7 kV. The specification and power switches prices were updated by the present date of the dissertation.

Table 4.1 – Key parameters of SiC MOSFET from different manufacturers.

	CAS120M12BM2 [1]	APTMC120AM16CD3AG [2]	APTMC120AM08CD3AG [3]	BSM120D12P2C005 [4]	BSM180D12P2C101 [5]	10-PC094PB017ME02-L620F36Y [6]	FF11MR12W1M1_B11 [7]
Type	Half-bridge	Half-bridge	Half-bridge	Half-bridge	Half-drive	Full bridge	Half-bridge
NTC	No	No	No	No	No	Yes	Yes
Package (width)	62mm	62mm	62mm	45.6mm	45.6 mm	22.5 mm	33.8mm
Package housing							
V_{DS}	1.2 kV	1.2 kV	1.2 kV	1.2 kV	1.2 kV	0.9 kV	1.2 kV
I_D (Tc=80ºC)	150 A	98 A	190 A	134 A (Tc=60ºC)	204 A (Tc=60ºC)	55 A	100 A (40 ºC)
$R_{DS(on)}$ 25º C	13mΩ	16mΩ	8 mΩ	18 mΩ	11 mΩ	23 mΩ	11 mΩ
V_{GS},*max*	-10/25 V	-10/25 V	-10/25 V	-6/22 V	-6/26	-8/19 V	-10/20
Ciss	6.30 nF *´	4.75 nF **	9.50 nF **	14 nF *^	23 nF *^	1.98 nF *^^	7.95 nF *~
Coss	0.88 nF *´	0.4 nF **	0.8 pF **	~ 0.9 nF *^	~0.9 nF*^	0.18 nF *^^	0.47 nF *~
Tmax	150 ºC	150 ºC	150 ºC	150 ºC	150 ºC	175 ºC	125 ºC
Rth,JC	0.125 ºC/W	0.19 ºC/W	0.10 ºC/W	0.16 ºC/W	0.11 ºC/W	0,94 ºC/W	0,55 ºC/W
P_D (dissipation) (Tc = 20 ºC)	925 W	625 W	1100 W	780 W	1130 W	101 W	-
Module size	106x62x30 mm	108x62x31 mm	108x62x31 mm	122x45.6x17 mm	122x45.6x17 mm	66x32.5x12,9mm [a]	62.8x33.8x12mm
Weight	290 g	350 g	350 g	280 g	-	-	24 g
Price (1 un.)	280,36 €	444,8 €	908.6 €	320,7 €	352,41 €	346.8 €	130.5 €
Price (10 un.)	-	444,8 €	908.6 €	312,2 €	339,361 €	337.5 €	124.2 €
Price (100 un.)	-	444,8 €	908.6 €	305,2 €	339,361 €	337.5 €	117.0 €

	QJD1210010 [8]	QJD1210SA1 [9]	APTMC120AM20CT1AG [10]
Type	Hall-bridge	Hall-bridge	Half-bridge
NTC	No	No	No
Package (width)	56.1 mm	56.1 mm	40.8mm
Package housing			
V_{DS}	1.2 kV	1.2 kV	1.2 kV
I_D	100 A (150 ºC)	100 A (78ºC)	108 A (80 ºC)
$R_{DS(on)}$	15 mΩ (25 ºC)	17 mΩ (25 ºC)	17 mΩ (25 ºC)
V_{GS},max	-5/25 V	+/-20 V	-10/25 V
Ciss	10.2 nF *~	8.2 nF	5.96 nF
Coss	1 nF *~	2.9 nF	0.44 nF
Tmax	150 ºC	150 ºC	150 ºC
Rth,JC	0.138 ºC/W	0.24 ºC/W	0.12 ºC/W
P_D (dissipation)	1080 W	-	600 W (Tc=25 ºC)
Module size	109.8x56.1x18mm	109.8x56.1x18mm	51.6x40.8x11.5mm
Weight	270 g	270 g	
Price (1 un.)	available for ordering	available for ordering	330,42 €
Price (10 un.)	“	“	-
Price (100 un.)	“	“	368,8 €

Note:

[1]CREE/Wolfspeed, [2,3,10]Microsemi, [4,5]ROHM, [6]Vincotech, [7]Infineon, [8,9]POWEREX

NTC – negative temperature coefficient. It is a typically thermistor, which is dependent on temperature, and the resistance value change inversely to the temperature.

Conditions:
* Recommended operation value by manufacturer
** V_{GS} =0V, V_{DS} =1KV, f= 1MHz |
*´ V_{DS} = 1kV f=200 kHz |
*^ V_{GS} = 0 V and V_{DS} =10V, f = 1MHz
*~ V_{GS} =0V, V_{DS} =800V, f= 1MHz
*^^ V_{DS} = 600 V and V_{GS} = 0 V

The first analysis of MOSFET modules shown in Table 4.1, and considered the price and specification ratio, the CAS120M12BM2 from CREE manufacturer is an excellent option for the application project. It has a small drain-source On resistance compared to the other power modules. The small input capacitance Ciss also is an advantage due to the lower power losses consequence.

However, the table shows other solution like the APTMC120AM20CT1AG from Microsemi that in term of characteristics could be a good choice if the price wasn't considered. The main difference that compromises the selection is the package configuration and the layout. This MOSFET market analysis reveals that currently, at the time of this research[1], the manufacturer offers power modules with different size and pins configuration. In industry application, the 62 mm power modules are preferred than others due to the easy implementation of the power circuit and the command circuit.

The next Table 4.2, presents the discrete MOSFET available and more suitable for the DAB converter.

Table 4.2 – Discrete MOSFETs available and its specifications.

	C2M0025120D[a]		UJ3C120040K3S[b]		C3M0030090K[a]		SCT3030KLGC11[d]	
Type	TO-247-3		TO-247-3		TO-247-4L		TO-247-3	
Package housing								
V_{DS}	1.2 kV		1.2 kV		1.2 kV		1.2 kV	
I_D	67 A (90 ºC)		50 A (90ºC)		44 A (90ºC)		51 A (100ºC)	
$R_{DS(on)}$	25 mΩ (25 ºC)		35 mΩ (25 ºC)		30 mΩ (25 ºC)		30 mΩ (25 ºC)	
V_{GS},*op*	-5/25 V		-		-4/+15 V		0/+18 V	
V_{GS},*max*	-10/25 V		-25/+20 V		-8/+19 V		-4/+22 V	
Ciss	2788 pF ††		1500 pF †		1864 pF		2222 pF	
Coss	220 pF ††		210 pF †		131 pF		180 pF	
Tmax	150 ºC		150 ºC		150 ºC		150 ºC	
Rth,JC	0.24 ºC/W		0.27 ºC/W		0.84 ºC/W		0.34 ºC/W	
P_D (dissipation)	463 W		429 W		149 W		339 W	
Units per module equivalent	DC side	batt. side	DC side	batt. side	DC side	batt. side	DC side	batt. side
	2 per arm	4 per arm	2 per arm	4 per arm	2 per arm	6 per arm	2 per arm	6 per arm
	111,62 €	223,24 €	-	-			72,52€	217,56€
Price (1 un.)	57,24 €		Not available		24,93 €		36,26 €	
Price (10 un.)	57,24 €		"		24,93 €		33,83 €	
Price (100 un.)	55,81 €		"		24,31 €		33,77 €	

[1]May 2018

4.2. Gate Driver SiC MOSFETS

This section will perform a brief introduction to the main topics to drive the SiC-based device properly. In the 21st century, more and more efforts have been put into improving Silicon Carbide devices, which is causing the market to grow in many fields. In the last chapter, the perks of SiC power devices were discussed. The available power devices in the market more adequate to the converter project were presented in the before section.

SiC-devices have gained attention and has been a priority chosen for the project and design engineers in the power electronics application due to the significant benefits presented in section 2.4.2**.** It is AddVolt's interest to bring more attractive semiconductors regarding efficiency and robustness into their system. And it is the purpose of this dissertation to study the viability of SiC MOSFET implementation.

Including these devices in the system represents a new challenge. The present section focuses on the main characteristics and techniques for the circuit driver implementation. Summarily, the selection of the gate driver IC must follow the requirements:

- Include logic functions (Miller Clamp, short circuit detection, under voltage lock-out);
- isolation is mandatory, between the command signals (primary side) and the high-power level (secondary side);
- Input/output supply in agreements to the imposed requirements (input: 8 to 32 V; output: -5 V, 0 V, +20 V). The bipolar power supply is required to perform the clamping of MOSFET, especially in the SiC-based semiconductor;
- Negative DC bias.

4.2.1. Gate driver circuit for SiC MOSFET

The SiC MOSFET requires more attention than Si MOSFET or IGBTs.

i. In the market, there are a few manufacturers that offer a SiC device for high power application. Actually, Cree is the company who has a wide offer of the transistor with the recent technology, the silicon carbide.

ii. For SiC MOSFET, the gate drivers should be capable of providing a negative voltage, and high gate-to-source voltage in order to minimize switching times and energy losses.

It was made a search in the market for the available and more interesting circuit driver suitable to drive SiC devices. The characteristics and parameters of each gate driver and some features are enumerated in Table 4.3.

Usually, optically isolated devices have fast response compared to devices with galvanic isolation. However, observing the Table 4.3, ADuM4135 gate driver has a faster response time than the other solutions with optically isolation. Since the propagation delay of the signal from the input to the output is relatively low, around 55 ns, which makes this device attractive for applications with SiC MOSFETs. The only barrier in using ACPL-32JT is the frequency restriction at a maximum of 80 kHz and the low peak output current around 2.5 A against to 4 A of the ADuM4135.

The input power supply for the gate drivers was another challenge founded. Only the ACPL-32JT device, shown in this section and a few more devices available in the market, allows a large input PWM signals at 15V. Being able to be supplied with a large input voltage. The input power supply was initially a requirement to satisfy the existent interface in the AddVolt system (8 – 15 V). This interface is known as the control board which includes the microcontroller.

Table 4.3 – Gate driver available and intrinsic parameters and functions.

Gate Driver	Isolation capability	CMR Typ. (**kV/µs**)	Input supply range V_{DD1} **(V)**	Output supply range **(V)** V_{DD2} | V_{SS2}		Propagation delay Typ. **(ns)**	Integrate logic function
ADuM4135[a]	Galvanic	100	2.3 - 6	12-30	-15 to 0	55	A, B, C
ACPL-352J[b]	Optocoupler	50	4.5 - 5.5	15-30	-15 to 0	90-100	A, B, C
ACPL-32JT[b]	Optocoupler	30	8 – 18	15-25	-8 to 0	120-160	A, B, C, D

V_{DD1} – input supply voltage on the primary side
V_{DD2} – output supply voltage on the secondary side
V_{SS2} – negative supply for the secondary side
Manufacturer: [a]Analogic Device | [b]Avaga

Note:

- All gate drivers are proper for IBGT and also SiC MOSFET
- CMR – common mode rejection
- logic function: A -Miller clamp detection, B – Undervoltage lockout (ULLO), C – Desaturation detection; D – regulated voltage

Due to the limited devices available to respond to the needs, it was decided to study and use the standard alternatives for the smart integrated gate driver. In this case, it was decided to use the standard input range, typically between 3.3 and 6 V. ADuM4135 is the best solution, since it has robust isolation. In technical meaning, this smart IC has higher common-mode transient immunity (CMTI). Furthermore, a high-power board control for module SiC is available in the market that integrates the ADuM4135 gate driver [40]. Some features of this product include isolation of 100 kV/µs, guaranteed by the isolated gate driver, and a practical application with switching frequency until 200 kHz.

4.2.2. The ADuM4135 – smart driver

Figure 4.1 shows a functional diagram of the ADuM4135 driver. As mentioned before, the driver has internal isolation between the low side to the high side.

- Low-side – input signal
- High-side – output gate driver

It is known that SiC technology allows extending the operation to a high level of switching. But what parameters will limit the increase of switching frequency?

Driver circuits may be an obstacle, as there may be no gate driver models available that allow increasing switching frequency due to the inability to provide enough power to drive the MOSFET in HF. In another hand, the drive's response time may not be fast enough to allow high switching frequency.

Another essential aspect that directly influences semiconductor switching is the turn-on and turn-on losses. The application note AN4671 founded in [41], it was used to understand these barriers, and it will be used to support the driver circuit design for the application with the aim of reducing the losses.

The schematic of the board circuit with the gate IC for driving a half-bridge configuration with SiC MOSFETs, and all components and the isolated interface between power source and control system was design and it is available in appendix. The next section will describe the procedure to design the driver circuit. The circuit will be designed to obtain the best performance of the smart driver and to fulfill the high-frequency switching requirements.

Note: The grounds on Low-side and High-side are isolated from each other.

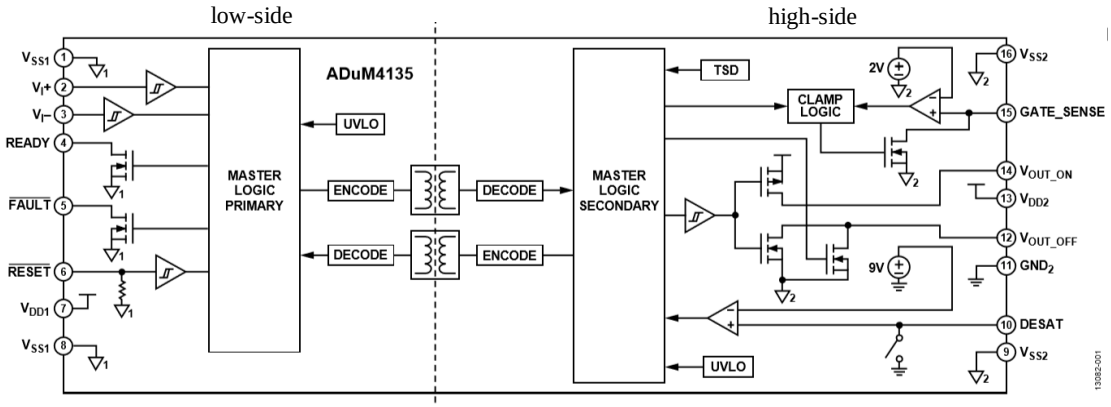


Figure 4.1 – Block Diagram of the gate driver with the representative internal function.

4.2.3. Low-side of the gate driver

The ADuM4135 has a set of inputs and outputs. The V_1^+ and V_1^- pins are the input drive signals which are then provided by the microcontroller, after a proper signal conditioning. The existence of more than one input PWM signal is to increase the number of input state possibilities. Table 4.4 shows voltage level of the gate being driven, the V_{GATE} on the secondary side, depending on the combination of the two input drive signals. Nevertheless, only one input pin V_1^+ will be used for driving the MOSFET. The expression (4.1) resumes the way that output V_{GATE} is configurated. The pin V_1^- must be connected to the primary ground.

$$V_{GATE} = \begin{cases} high \quad ,when\ V^+ is\ high \\ low \quad ,when\ V^+ is\ low \end{cases} \tag{4.1}$$

The READY pin is an open-drain logic output. A high level on this pin indicates that IC is operational as gate driver.

Table 4.4 – Truth table, from the gate driver datasheet.

V_{I+} Input	V_{I-} Input	$\overline{\text{RESET}}$ Pin	READY Pin	$\overline{\text{FAULT}}$ Pin	V_{DD1} State	V_{DD2} State	V_{GATE}[2]
L	L	H	H	H	Powered	Powered	L
L	H	H	H	H	Powered	Powered	L
H	L	H	H	H	Powered	Powered	H
H	H	H	H	H	Powered	Powered	L
X	X	H	L	Unknown	Powered	Powered	L
X	X	H	Unknown	L	Powered	Powered	L
L	L	H	L	Unknown	Unpowered	Powered	L
X	X	L[3]	Unknown	H[3]	Powered	Powered	L
X	X	X	L	Unknown	Powered	Unpowered	Unknown

X – pin state can be Low or High, don't care about the pin sate.
V_{GATE}[2] – the voltage applied to the gate of the MOSFET (low or high level)

The IC must be supplied with the requirements established. Thus, a DC voltage supply at 5 V will be available to feed the primary side. For now, it is not discussed how the 5 V will be contained from the 15 V coming from the control board. In the section 4.2.6 will be explored the choice of the isolated DC-DC interface and the signal conditioning for PWM signals which are provided by the control board with a 15 V logic.

Pin description – low side:

- The input low voltage V_{DD1} is connected to the primary supply (e.g., 5V). A ceramic capacitor (100 nF) is added between V_{DD1} and the primary ground. The ceramic capacitors have low inductance and an excellent HF response.
- The two pins VSS1 are linked to the ground on the primary side, as well as the negative input drive V_1^-.
- The output $\overline{\text{FAULT}}$ pin is used for the microcontroller to detect a presence of desaturation events. When the pin is low, it means that a desaturation fault occurred. This pin is connected to a pull-up resistance to allow the reading.
- The output READY pin is used to read the state of the gate driver operation. This pin must be connected to a power supply through a pull-up resistance to ready their signals. The device is ready to operate when a high state is read in this pin. A low state on this pin can represent an occurrence of other fault events.
- The positive input drive V_1^+ receive the PWM signal from the control board. However, signal conditioning must be considered, since the IC is only prepared to receive 5V logic, and the control board provides 15V logic. The PWM signal conditioning will be discussed later in the document.

Considering the DC-DC converter architecture proposed, it is necessary to evaluate the number of inputs and outputs from the control board (microcontroller) needed to operate with each MOSFET. In this dissertation, only the circuit driver for a half bridge configuration will be represented. The same circuit configuration is then replicated for the rest of the half bridges of the converter. However, it is essential to analyzing the application as a whole – the dual-active bridge. Considering his, then:

- Following the description mentioned, for each H-bridge it is necessary four signals used as inputs in the control board to read the status of all $\overline{\text{FAULT}}$ pins. Moreover, four signals used as an output to clear the denaturation failures in each IC and four more signals to read the READY pin status. In a total of 12 signals into the microcontroller only for the one H-bridge.

- The total 24 signals, between output $\overline{\text{RESET}}$, input READY, and the input $\overline{\text{FAULT}}$ for the microcontroller point of view, are not practically archivable due to the microcontroller limitations.
- The microcontroller inside the control board available in the company only allows reading one signal fault.

Considering all the restrictions mentioned, it was decided to connect $\overline{\text{RESET}}$ pin to the $\overline{\text{FAULT}}$ pin through a resistance, in orther to simplify the control circuit and to reduce the number of signals into microcontroller. When a fault occurs, the low state on the $\overline{\text{FAULT}}$ pin brings the pin to ground and the fault is cleaned.

The power side has more considerations than low side. The next section will give more attention to the sizing of the gate resistance. The influence of gate resistance with the switching losses and its direct relation in the voltage (V_{GS}) rise and fall time will be discussed. The desaturation function will be studied and designed to detect excessive current through the MOSFET.

4.2.4. High-side of the gate driver

a) Desaturation events:

This function is used to detect short-circuit events in the power device, during the conduction operation. The excessive current makes the MOSFET to come out of the saturation region. Consequently, the device is damaged or even destroyed. Internally, the gate driver has a voltage threshold at 9V. If the voltage applied to the desaturation pin exceeds the threshold voltage, the ADuM4135 goes into a failure state, the $\overline{\text{FAULT}}$ pin is driven to a low state, and this function is only available during the turn-on of the power device. When the desaturation detection is triggered, the ADuM4135 turns off the power device.

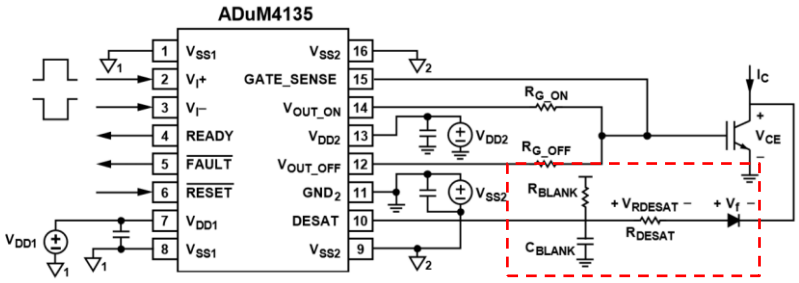


Figure 4.2 – Example of circuit driver application.

The protection to overcurrent must be dimensioned to ensure fast response and preserve the lifetime of the SiC MOSFET. Based on the schematic in Figure 4.2 from the fabricant's datasheet, illustrates the implementation of the desaturation protection for the MOSFET.

Inside the DESAT node, there is an internal CMOS configuration (Figure 4.1) and to ensure the overvoltage protection at the input, a Schottky diodes rectifiers are typically added. The ADuM4135 has an internal blanking time to avoid false switching while the MOSFET first turns on. The time between first desaturation events and the failure report (as a consequence of drive low the pin $\overline{\text{FAULT}}$) is almost 2 us, t_{REPORT} in Figure 4.4. The pull-up resistance is implemented to have an external power source to charge the blanking capacitor, in addition to the internal current provided by the gate driver (typ. 500 uA).

The R_{Blank} was chosen to extract an extra current from the secondary power supply source. Their value is higher to drive a low current. The C_{Blank} is dimensioning to have a blanking time approximately 2 µs, a suggestion given by the manufacture's driver IC.

Sizing of the blanking capacitor for an application:

The short circuit protection will be based on the circuit showed in Figure 4.3. The half bridge should have a nominal current of 32 A for the application. This is related to the nominal current expected in the first H-bridge of the DAB, connected to the DC-link bus. In a normal operation, the voltage at desaturation pin is near V_f = 4.2 V. Considering the voltage drop of 2×1.65 V across the two fast diodes connected to the MOSFET's drain, and a drain-source voltage V_{DS} = 0.9 V at 25 ºC during the nominal operation MOSFET. For the short circuit it is assumed a drain current of 40 A, representing about 20% above of the nominal current in the primary side of the transformer (32 A nominal). The V_{DS} is now 1.2 V at I_D = 40 A and the V_f reaches 4.5 V. The On-state resistance of the MOSFET at 25 ºC is $R_{ON\ (25^oC)} = 25$ mΩ, and this value will be considered to the driver design. The voltage drops across the blanking resistance is neglected, to determine the C_{Blank}.

When an anomaly occurs, the voltage at DESAT pin starts increasing. The C_{Blank} follows this change, and due to the potential voltage difference, it begins to charge with the energy provided by the ADuM4135 and from the pull-up resistance R_{Blank}.

$$V_C = V_{final} + \left(V_{initial} - V_{final}\right)e^{-\frac{t}{RC}} \tag{4.2}$$

The internal desaturation threshold is 9 V, thus the $V_{final} = 9V$. In normal operation of the MOSFET, it is seen that the V_{DESAT} = 4.5 V, therefore the initial voltage across the blank capacitor is 4.2V. By the suggestion of manufacturers' gate driver, the recommended blanking time for MOSFET/IGBTs is 2us, Figure 4.4. The constant *RC* must be equal to a 1/5 of the t_{blank} and then it is known that capacitor will reach 63% of the maximum voltage (9 V) in a one constant time (τ = *RC*). By solving equation (4.2) in order of *C* with $V_C = 4.5 + 0.63 \times (9 - 4.5)$ V at the end of one time constant τ, and R_{Blank} = 10 kΩ, the blank capacitor is determined by:

$$C_{Blank} = \frac{-t}{R \times \ln\left(\frac{V_C - V_{final}}{V_{initial} - V_{final}}\right)} = 40pF \tag{4.3}$$

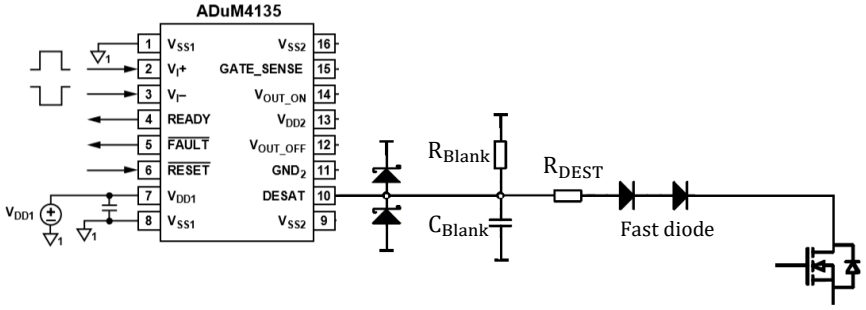


Figure 4.3 – Desaturation circuit. Desaturation circuit is adapted to the project application.

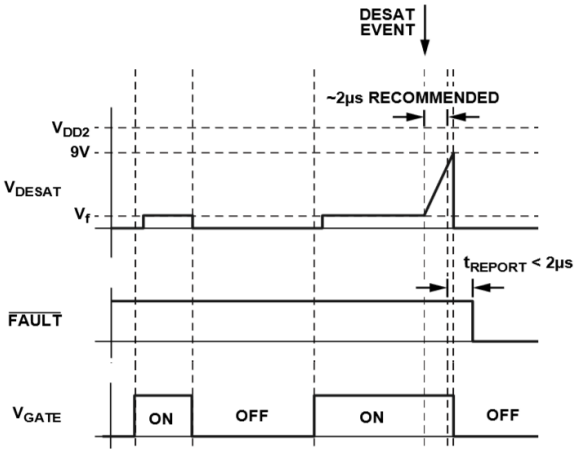


Figure 4.4 – Example of a desaturation events timing diagram, from datasheet's gate driver.

Since the desaturation circuit was almost designed, with C_{Blank} = 40 pF and R_{Blank} = 10 kΩ, and the R_{DEST} was for now considered small enough to be neglected (assuming the current in desat. circuit in order of mA and the R_{DESAT} value of some hundred ohms).

When a desaturation event is triggered, this is, the V_{DS} across MOSFET plus the voltage drop in the two fast diodes rises above the 9 V. At this point, the IC driver will turn-off the MOSFET in few microseconds, less than 2 us, preventing the MOSFET of excess current flow. The expected a short circuit current for this example that will activate the protection of MOSFET to come out of saturation is derived from this expression:

$$R_{ON(60^0C)} \times I_{short} + 2V_{diode} = 9\,V \tag{4.4}$$

Where the I_{short} is the minimum short circuit current. From the Figure 4.5 related to the MOSFET operating zone, it is possible to verify that the power device supports a pulse current of 200 A within 1 to 10 ms approximately at a voltage V_{DS} = 10V across the MOSFET.

Alternatively, the blanking capacitance can be reduced to increase the response time, and the resistance R_{DESAT} added in series with the two diodes will introduce a voltage drop that can be a benefit to limit the drain current in the MOSFET. With an R_{DESAT} = 1 kΩ, when 9V was applied to the DESAT pin, the short current expected to activate the protection of MOSFET is given by:

$$\begin{aligned} V_{DESAT} + R_{ON(25\,^0C)} \times I_{short} + 2V_{diode} &= 9\ V \\ V_{DESAT} = R_{DESAT} \times (I_{Blank} + I_{IC}) = 1\,000 \times (500uA + 1.1mA) &= 1.1\ V \\ I_{short} = \frac{9 - 2 \times 1.65 - 1.1}{0.028} &= 164\ A \end{aligned} \tag{4.5}$$

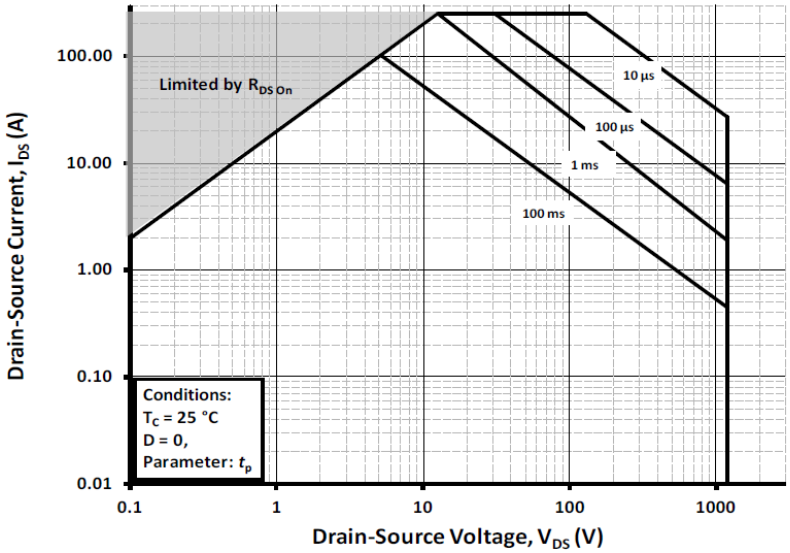


Figure 4.5 - Safe operation from datasheet's C2M0025120D.

The diode's function is to conduct during the turn-on of the transistor and allow to sense and monitor the saturation MOSFET's drain voltage. During the turn-off, the diode blocks the high voltage applied to the device and protect the driver IC. A fast diode must be used to allow a fast response, minimizing the C_{Blank} charge and avoiding the gate driver to detect false desaturation.

Table 4.5 - Components presents in the desaturation circuit.

$\boldsymbol{R_{BLANK}}$	10 kΩ
$\boldsymbol{C_{BLANK}}$	39 pF
$\boldsymbol{R_{DESAT}}$	1 kΩ
Schottky diode	Reverse voltage 100V
Fast diode	Reverse voltage 1200 V
$\boldsymbol{R_{ON\ (60^0C)}}$ *	28mΩ

* $\boldsymbol{R_{ON\ (60^0C)}}$ – On-drain MOSFET resistance

Calculate the required turn-on and turn-off gate resistance

The sizing of the gate resistance must have into account the switching losses. The gate driver ADuM4135 allows using two different current paths to control the turn-on and turn-off of the MOSFET. It provides two separate output nodes: the Vout_ON and Vout_OFF. With this benefit, it is possible to control the rise and fall time separately avoiding the use of a reverse diode to drive the gate low during the turn-off. The procedure to select the proper resistance must comply with some requirements:

- It is desired to have a turn-off faster than the turn-on;
- Select a low external gate resistance was possible to decrease Eon and Eoff.

The current gate driver allows a maximum peak current of 4 A. Observing the first equation (4.6), the external gate resistance value could be selected to control the maximum peak gate current ($I_{G.peak}$) for the MOSFET. Some technical application notes about to choose suitable IC driver refer that the output peak current of the IC driver ($I_{OUT.peak}$) must be equal or preferentially higher than the required $I_{G.peak}$. Selecting the peak current of 4 A, the max. $I_{OUT.peak}$ of the driver IC, and knowing the voltage applied to the gate-to-source of MOSFET of 20V (20V / -5V), and the internal resistance of the ADuM4135, the $R_{G(OFF)}$ is determined by the expression (4.6) [42]:

$$R_{G(OFF)} = ((VDD2 - VSS2) - I_{peak} \times R_{IC.intern\_N})/I_{G.peak}$$
$$R_{G(OFF)} = ((20\ V - (-5\ V)) - 4\ A \times 0.6\Omega)/4\ A = 5.7\ \Omega \quad (4.6)$$

Note that internal resistance $R_{IC\_intern\_N}$ is referred to NMOS gate resistance internal to the driver IC, and it is active during the turn-off events. The $R_{G(OFF)}$ derived must be adapted to an existing standard value and to guarantee the required $I_{G.peak}$ below to the maximum $I_{OUT.peak}$ of the IC driver. Considering the intrinsic internal gate resistance of the MOSFET[2], the $R_{G(int)}$ of 1.1 Ω, $R_{G(OFF)}$ is selected to be 5.1 Ω and the required $I_{G.peak}$ is equal to 3.9 A.

Looking at Figure 4.6 from MOSFET's datasheet, the required time to turn-on and turn-off can be determined. To ensure a slower turn-on than turn-off, $R_{G(ON)}$ needs to be slightly higher than $R_{G(OFF)}$. Table 4.6 present a summary of the calculated values for the two-gate resistances and the respective switching times response. The table also provides a relation of different external R_G values and respective rise-time and fall-time. It observed from the Table 6 which the large gate resistance $R_{G(ON)}$ increases the turn-on time. Another consequence is the increase of Eon and decrease of the maximum $I_{G.peak}$ required. As an example, for $R_{G(ON)}$ = 9.1 Ω, using the equation (4.3) and knowing the V_{GS} = 20 V, the $R_{IC.intern\_N}$ = 0.6 Ω and the $R_{G(int)}$ =1.1 Ω, the peak current gate during turn-on is equal to 2.3 A.

[2] MOSFET with SiC technology, V_{DS} = 1200 V, I_D = 67 A @ 90 ºC, and $R_{DS(on)}$ = 25 mΩ at 25 ºC

Table 4.6 - Gate resistance and switching times.

	Value	Fall time	td(off)	Total turn-off
$R_{G(OFF)}$	5.1 Ω	35 ns	36 ns	71 ns

	Value	Rise time	td(on)	Total turn-on
$R_{G(ON)}$	9.1 Ω	53 ns	21 ns	74 ns
$R_{G(ON)}$	10 Ω	56 ns	22 ns	78 ns

td(off) - Turn-Off Delay Time
td(on) - Turn-On Delay Time

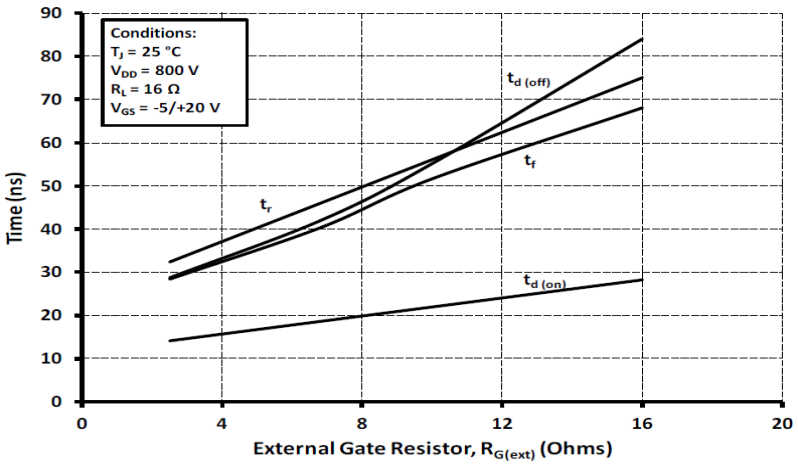


Figure 4.6 – Timing delay vs $R_{G(ext)}$.

4.2.5. Power to driving a MOSFET

The IC driver must provide power to drive a MOSFET. The power required to operate a MOSFET at a specific frequency is also a requirement to consider in the design. The isolated DC-DC source and the gate driver may not be enough to ensure the operation at a given frequency. Furthermore, the power need increases with the switching frequency. Therefore, the power dissipation must be considered to ensure that all control system (driver + isolated supply source) met the operation specification.

The expression (4.1) is suggested by the manufacturer's device to calculate the estimated power to drive a single MOSFET. It is considered the input capacitance of the device by a factor of 5 to arrive at a conservative estimate about the capacitance seen when a load is being driven. In practice, the power dissipation is less than the value calculated in expression (4.1).

$$P_{DISS} = 5 \times C_{ISS} \times (V_{DD2} - V_{SS2})^2 F_s \tag{4.1}$$

Table 4.7 – Power dissipation as a function of the switching frequency.

Switching frequency	V_{GS}	Negative supply	Ciss (from MOSFET datasheet)	Power dissipation expected
60 kHz	20 V	- 5 V	2788 pF	0.7 W
80 kHz	20 V	- 5 V	2788pF	0.87 W

The V_{GS} in Table 4.7 represents the positive gate-source voltage applied to the gate MOSFET. As it was discussed in section 3.4.1, the increase of the switching frequency in power electronics brings the benefit of the reduction of passive components. It was shown that the inductor filter is reduced to half when the F_S rise from 40 kHz to 80kHz, with the use of SiC technology. However, the higher switching frequency may push the devices to its limits and results in the increase of the energy consumption on the driver circuit side.

4.2.6. Isolated DC-DC power supply and signal conditioning

Beside the previous consideration about appropriate voltage to drive MOSFET, the power source need high isolation to separate the low side from high side. A voltage regulator is also required to supply the ADuM4135 of 5V on the primary side, since the control board of AddVolt's system as mentioned before, has a power supply of 15 V available. The R-78E-1 switching regulator from Table 4.8 was chosen to be included in gate driver circuit designed. Conditioning of logical input PWM from the microcontroller into the driver IC will be made by a level shift, which translates one logical signal to another logical signal. The simple schematic of Figure 4.7 represents the integration of all part of the gate driver circuit for one single MOSFET including the PWM conditioning and isolation between low and high-power side.

Table 4.8 – Isolated DC-DC converter supply.

Gate Driver	RKZ-152005D	R15P22005D	R-78E-1
Manufacture	RECOM Power	RECOM Power	RECOM Power
Input Voltage	15 V	15 V	7-28 V
Output Voltage	20 V / -5 V	20 V / -5 V	5 V
Isolation voltage(1)	3 kVDC	6 kVDC	-
Power	2W	2 W	-
Type of isolation	Galvanic	Galvanic	No isolation
Capacitance load(2) (max)	100/1500 µF	47/680 µF	220 µF
Efficiency (%)	86	84	91
Price(3)	5,14 €	6,06 €	2,67 €

(1) Isolation during 1 second | (2) verified at nominal input voltage and full load | (3) June 2018

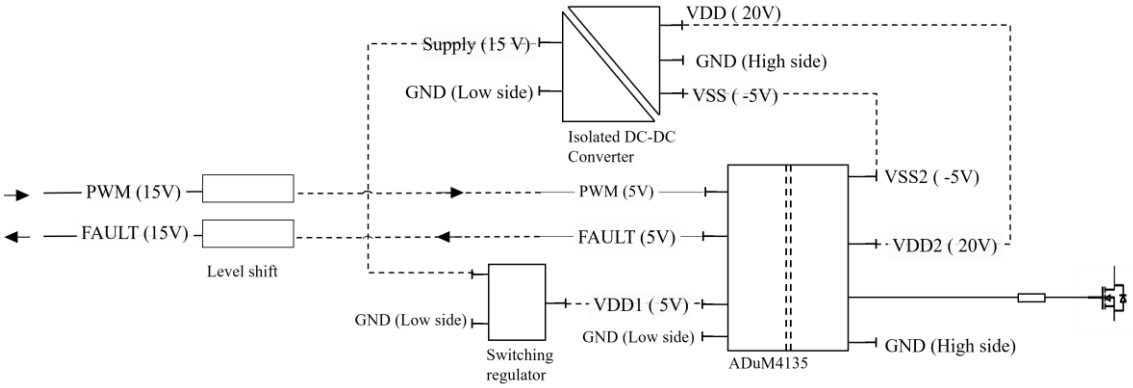


Figure 4.7 –Diagram of circuit gate driver designed for one single MOSFET.

4.3. DC capacitor and Bus-bar

The importance of the DC capacitor placed on the outlet of the converter to face with voltage and current ripple was seen early in section 3.4.2, where an *LC* filter was designed to the DAB converter input/output. The inductance *L* represents a parasite impedance resulted in the connections between the H-bridge and DC bus. The *LC* configuration introduces a resonant effect causing a current oscillation at the DC bus. In the controller design section 3.7. , it was verified that the effect of the second-order parasite inductance made difficult the design of the simple PI-controller. A damping resistance was added to the passive element to reduce the resonant impact and enable a dynamically stable PI controller to be obtained.

Features of the DC capacitor:

- Facing and reducing the voltage ripple;
- It is a bypassed for current ripple. It is crucial choices a capacitor with a small resistance component. The parasite resistance of the capacitors will affect AC ripple path. Significant value can impose a barrier to the current ripple.
- Receive a large harmonic spectrum.

Many converter applications use this component to face the HF ripple current. There are different types of dc bus capacitor and their use depending on the application. The electrolytic and film capacitors are two common passive components in power circuits selected for DC bus. The aluminum electrolytic capacitor is a good candidate to suppress voltage ripple and a high energy storage capability. These features are regarding the high capacitance per volume ratio [43]. Looking to the Figure 4.8, the capacitor could be represented by the equivalent model shown. The ESR meaning equivalent series resistance. The electrolytic capacitor has high ESR

compared to the film capacitor. The ESR value depending on the amplitude and the frequency of the voltage across the capacitor. With the introduction of wide-bandgap semiconductors in power system, the high switching frequency is allowed, and this can restrict the use of electrolytic capacitors. Film capacitor has low ESR value and consequentially low power losses and better to face AC ripple.

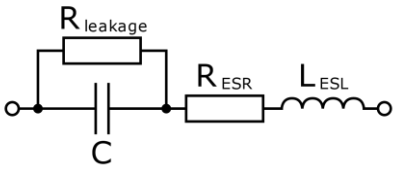


Figure 4.8 – Capacitor with detail parameters.

The bus capacitor must be handling with the HF ripple and using the equation (3.34) a minimum capacitance is founded. To determine their value, an HF ripple voltage must be defined as a design requirement. And the HF ripple current term ($I_{ripp\_2\times Fs}$) in the equation (4.8) is regarded to the amplitude of the carrier frequency which occur in the output of the H-bridge at double of the switching frequency. Considering the DC-DC converter at nominal operation with a $F_s =$ 80 kHz, the capacitor needed for both side of the first and second H-bridge (C_{DC} and C_{Batt} respectively) is calculated by:

$$C = \frac{I_{ripp.2\times Fs}}{\Delta V \times 2F_s} = \quad \begin{cases} C_{DC} = 50\ uF \\ C_{Batt} = 80\ uF \end{cases} \tag{4.2}$$

Where the voltage ripple ΔV is required to be 5V.

4.4. Proposal

Based on what has been presented, the isolated DC-DC converter shows good results with the use of wide band-gap semiconductors. The use of discrete MOSFETs with the parallel configuration reveals issues at the high switching frequency, mainly due to the substantial increase of switching losses above 80 kHz compared to the module structure. Although the cost per MOSFET module unit with half bridge structure, their application in the DAB converter stays to have advantages over the use of discrete MOSFETs. At the moment of this dissertation was written, the total cost of using half-bridge MOSFET modules is approximately equal than the total discrete MOSFET with the two-parallel discrete MOSFETs configuration in the DC-link and 3 parallel discrete MOSFETs for the battery side.

Following the parameters and specification of the isolated and bidirectional DC-DC converter in Table 4.9 and Table 4.10.

Table 4.9 – Filtering parameters and specification for each H-bridge.

First H-bridge connected to a DC-link		Second H-bridge connected to a Batt. pack	
Parameters	Value	Parameters	Value
L_2	10 uH	L_2	10 uH
C_1	50 uF*	C_2	80 uF*

*Film capacitor

Table 4.10 - Parameters and specification of the proposal isolated DC-DC DAB converter.

	Parameters	Value
Maximum power rating	P_o	22.1 kW
DC link voltage	V_{DC}	700 V
Battery voltage	V_{Batt}	200-450 Vdc
Switching frequency	F_S	80 kHz
External L filter	L	22.5 µF
Half-bridge Module		SiC technology
Transformer core material		Nano-crystalline
Transformer voltage ratio	N: 1	2.13 : 1
Winding turn	$n_{pri}: n_{sec}$	17:8
Maximum flux density	B_{peak}	0.28 T

*****Power module with 13mΩ drain-source on resistance at 25 ºC

L – auxiliary inductor of the primary side of the transformer

The conversion efficiency of the DC-DC converter studied can be determined for 80 kHz with nominal battery voltage $V_{Batt.N}$= 325 V (nominal), considering not only the macro losses in the MOSFETs estimated with the thermal model implemented in the GeckoCIRCUITS® simulator but also adding the core and copper losses for the proposal core transformer designed in section 3.5. And both copper and core losses are calculated analytically. From the simulation, the total losses of power MOSFETs – with SiC technology and module structure – in the two H-bridges at 80 kHz is estimated by 1170 W assuming the discharging mode with the battery voltage of 325 V. These losses are results of the discharging mode of the battery under the nominal power in the DC-link. Almost 74 % of the total MOSFET losses in the two bridges are a consequence of the semiconductor turn-on and turn-off, known by switching losses. Taking the core and copper losses calculated in section 3.5. for 80 kHz of switching operation, and with the winding configuration of 17:8 – P_{cu} = (13.5 + 22.7) W and $P_{c(80\ kHz)}$= 159 W, the DC-DC converter efficiency studied is estimated to 94.2 % assuming the nominal discharging operation.

Chapter 5

Conclusions and Future Work

At the final chapter is presented the main conclusions as results from the dissertation project developed. Following the proposals future works.

5.1. Conclusions

The power electronics field is vast, and for this dissertation, the motivation to study topologies of isolated DC-DC converters was established with the major aim in increasing the power density with the best efficiency. The author of this dissertation was encouraged in proposing a compact and light prototype to be inserted as an interface between the DC-link bus and a battery pack for low and medium voltage. After studying the converter topologies, the isolated bidirectional DC-DC converter was selected due to the high-power capacity and reduced active components compared to other topologies studied.

The analysis of the DAB-IBDC converter structure was made with a detailed model, which considers the major losses, as the conduction losses on the semiconductor and the power transformer. The model also includes the input/output filters. When the power module MOSFETs are used, the efficiency conversion during the battery discharging mode at the nominal operation (P_N and $V_{Batt.N}$) is 95.0 %, which was calculated considering only the power losses in the active components estimated with the thermal model implemented at a switching frequency of 80 kHz. In simulation environments, the model circuit designed was performed in open-loop and closed-loop. A thermal model was designed to investigate the reliability of the power semiconductors in high-frequency operation, one for discrete structure and other for half-bridge module structure. A comparative of the major power losses were presented for two different power MOSFETs solutions. The efficiency of the DAB converter at different high operation frequencies, from 40 kHz

to 80 kHz, was shown. The results from the simulation made it possible to choose the appropriate switching frequency by using the emerging power semiconductor.

This dissertation presents a market overview of silicon carbide MOSFET. The operation characteristic of this semiconductor and also the techniques for the driver circuit implementation are analyzed. A gate circuit driver was designed to drive a half-bridge structure, and the board circuit schematic is presented.

5.2. Future work

Since some objectives were not reached in this dissertation due to temporal constraints that did not make possible to approach some interesting subjects. Following the possible improvement and suggestion to the DAB converter topologies.

A. ***The transformer design improvements:***

In this dissertation, the procedure for designing the transformer followed a winding optimization technique, looking for the best copper winding structure, selecting the optimum cross-sectional area of the copper. It was verified that the window area utilization of the transformer was not used well, based on the *Ku* factor. A good transformer design can be made in order to choose a better magnetic core dimension to use better the windows area. Other approaches to design an optimum transformer is considering the leakage inductance during the design procedure to obtain the desired inductance to allow the power flow in the DAB converter and additional adjusting the external inductor placed in series with the transformer in the primary side.

B. ***Advanced modulation technique implementation***:

The DAB topology is very requested for bidirectional power flow applications due to the easy implementation of a soft-switching feature with this topology to reduce the power switching. However, with the traditional phase-shift, the soft-switching is limited especially when the voltage on both sides of the transformer is not balanced. And another disadvantage under the traditional SPS is the reactive current circulating in DAB converter, adding a more substantial current stress and more considerable converter loss affecting the efficiency of the system. This problem was verified in the simulation when the only one degree of freedom is used to control the power transited on DAB converter, using the traditional modulation. Therefore, the implementation and validation of other advanced modulation techniques are open to being considered for the DC-DC converter chosen in other to increase the converter efficiency.

C. Optimize a better closed-loop control:

Since a simple closed-loop was implemented in this work to monitor and control the current flow on the battery side, it proposes to improve the voltage and current controller for the battery side.

Could be interesting in implement a control structure that allows changing the modulation to obtain better efficiency, for example, has different modulation for different battery voltage level.

Appendix

A.1 *Thermal model parame*ters

This appendix presents the parameters used in the thermal model created for two MOSFET solutions.

Table A.1 – Parameters of the thermal model for the power modules (CAS120M12BM2)

Thermal parameters for the MOSFET body	
The junction temperature (T_j)	Measuring in each S_i switch
Thermal capacitance, junction to case ($C_{th.jc}$)	0.15 ^{0}C/W
Thermal resistance, junction to case ($R_{th.jc}$)	0.125 ^{0}C/W
Thermal interface parameters	
Thermal interface material, resistance $R_{th.tim}$	0.009 ^{0}C.inch^2/W
Thermal interface material, capacitance,$C_{th.tim}$	0.15 ^{0}C/W
Thermal parameters for the heatsink	
Thermal resistance, $R_{th.hs}$	0.027 ^{0}C/W
Thermal capacitance, $C_{th.hs}$	0.3 ^{0}C/W

Note A1 The $R_{th.tim}$ need be dived by the surface area (inch^2) of the pad: 0.009/4.92=0.0018 ºC/W

The thermal resistance of the heatsink was calculated considering two variables, the length of the heatsink and the fan accoupled to force the extraction of the heat. air flux was defined to be 5 m/s and the heatsink has a width of 300 mm, enough space to include four MOSFET module structures, and they have a width of 62 mm.

Table A.2 – Parameters of the thermal model for the discrete MOSFET (C2M0025120D)

Thermal parameters for the MOSFET body	
Thermal resistance, junction to case ($R_{th.jc}$)	0.24 ^{0}C.inch^2/W
Thermal capacitance, junction to case ($C_{th.jc}$)	0.15 ^{0}C/W
Thermal interface parameters	
Thermal interface material, resistance $R_{th.tim}$	0.107 ^{0}C.inch^2/W
Thermal interface material, capacitance,$C_{th.tim}$	0.15 ^{0}C/W
Thermal parameters for the heatsink	
Thermal resistance, $R_{th.hs}$	0.027 ^{0}C/W
Thermal capacitance, $C_{th.hs}$	0.3 ^{0}C/W

Note A2 The $R_{th.tim}$ in table is dived by the surface area (inch^2) of the pad: 0.107/0.71 = 0.150 ºC/W
It is used the same heatsink to discrete. Keeping the same dimension and air force fan.

A.2 *Closed-loop diagram and parameters*

Note 1:

Parameters of the DAB converter used to the simulation in closed-loop, section 3.8.

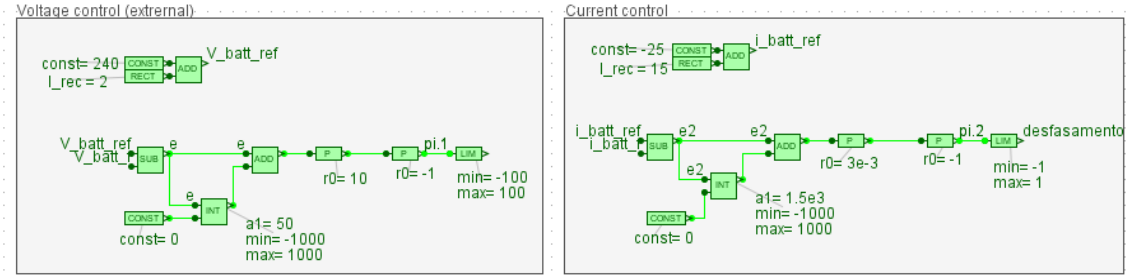
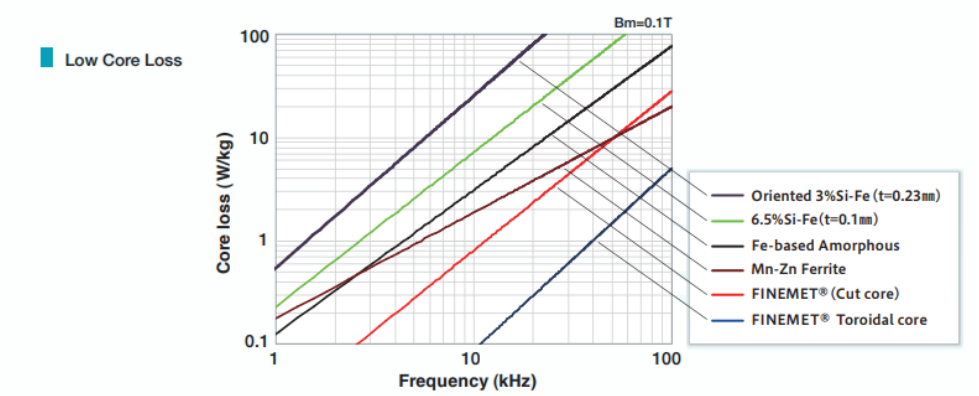


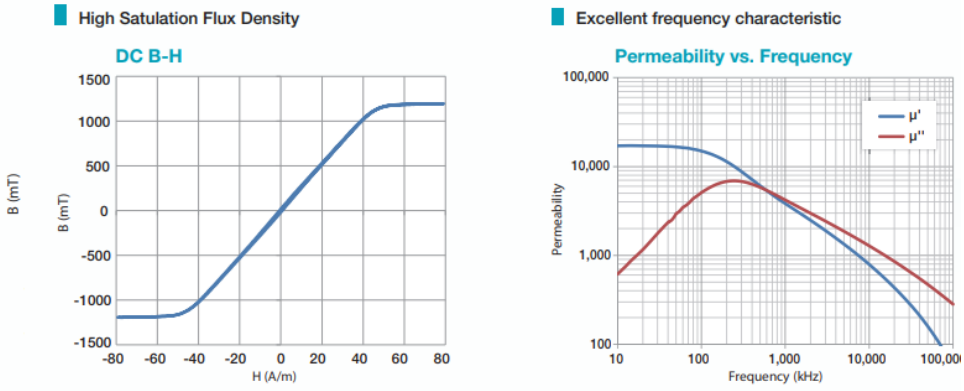
Figure A.1 – Closed-loop controller implemented in GeckoCIRCUITS®.

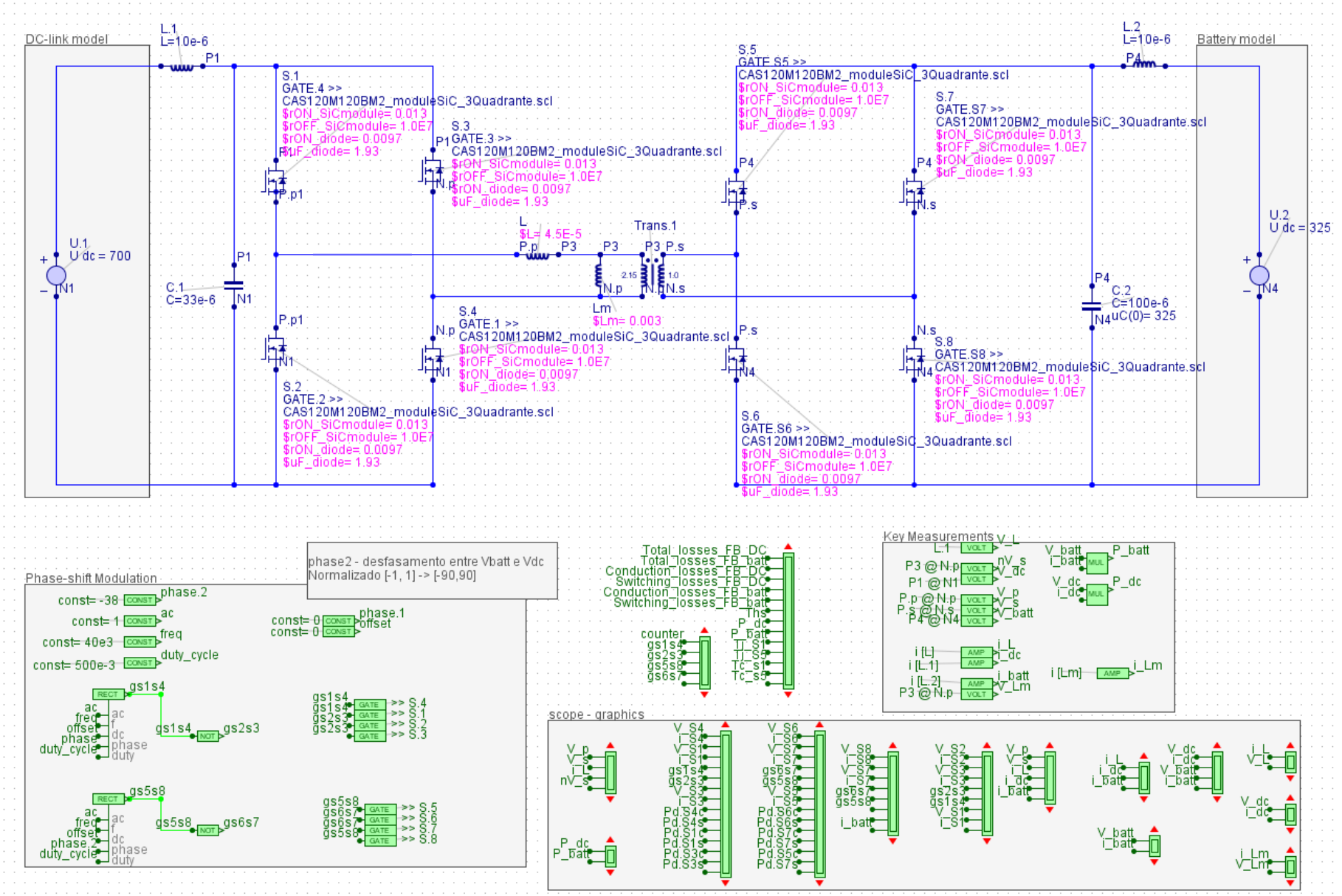
A.2 *Nanocrystalline material's Datasheet*

A feature of the toroidal core made by the nanocrystalline material.



Core losses with a flux density Bm equal 100 mT




DC-link model
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L=10e-6
P1
S.1
GATE.4 >>
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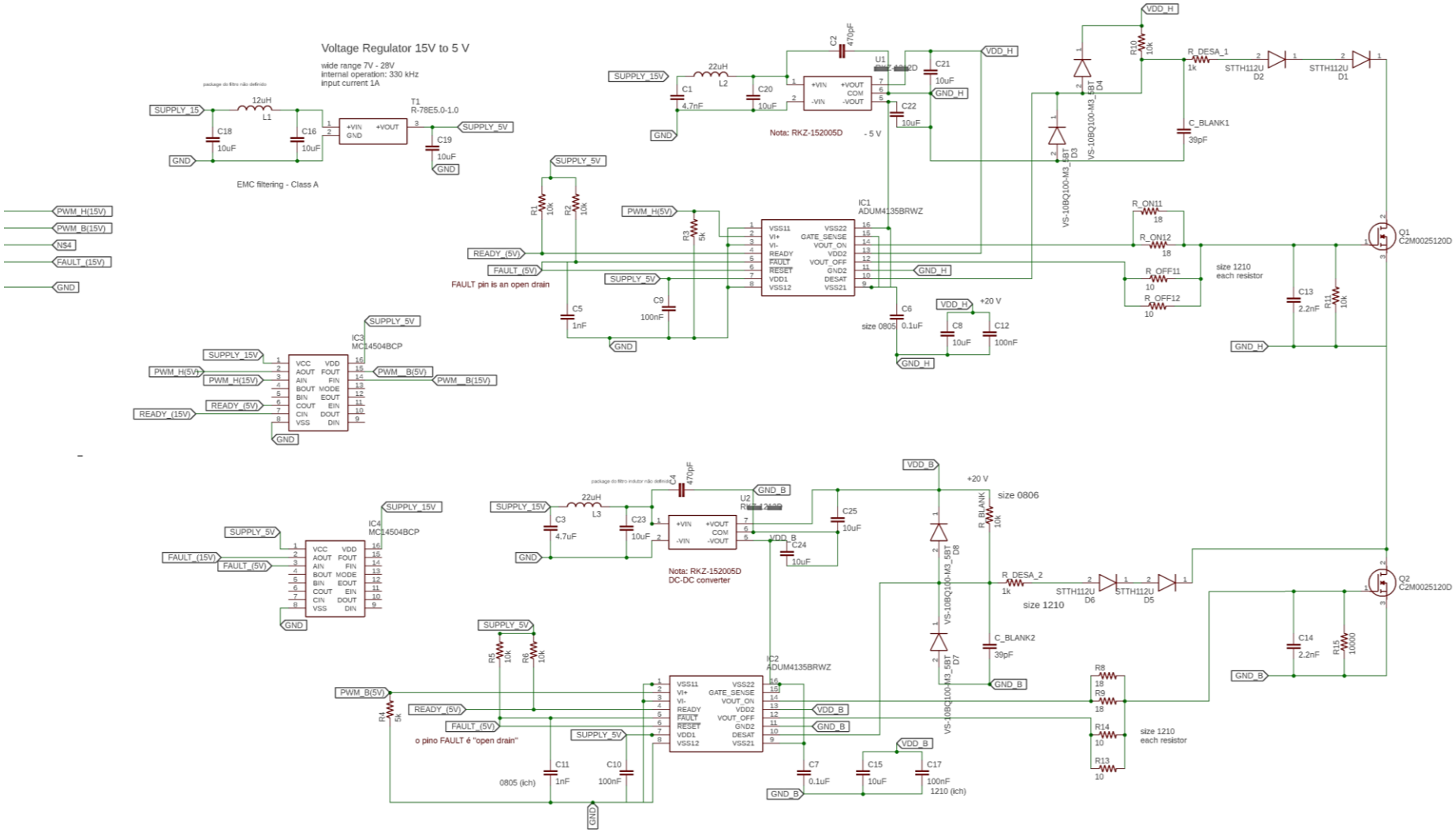
$rOFF_SiCmodule= 1.0E7
$rON_diode= 0.0097
$uF_diode= 1.93
S.3
GATE.3 >>
S.5
GATE.S5 >>
S.7
GATE.S7 >>
L.2
L=10e-6
P4
Battery model
U.1
U dc = 700
N1
C.1
C=33e-6
L
$L= 4.5E-5
Trans.1
2.15
1.0
N.p
N.s
Lm
$Lm= 0.003
S.4
GATE.1 >>
S.2
GATE.2 >>
S.6
GATE.S6 >>
S.8
GATE.S8 >>
C.2
C=100e-6
uC(0)= 325
U.2
U dc = 325
N4
Phase-shift Modulation
phase2 - desfasamento entre Vbatt e Vdc
Normalizado [-1, 1] -> [-90,90]
const= -38
phase.2
const= 1
ac
const= 40e3
freq
const= 500e-3
duty_cycle
const= 0
phase.1
offset
gs1s4
gs2s3
gs5s8
gs6s7
NOT
RECT
GATE
counter
Total_losses_FB_DC
Total_losses_FB_batt
Conduction_losses_FB_DC
Switching_losses_FB_DC
Conduction_losses_FB_batt
Switching_losses_FB_batt
Ths
P_dc
P_batt
Key Measurements
V_L
V_batt
i_batt
P_batt
V_dc
i_dc
P_dc
V_p
V_s
i_L
i_batt
i_Lm
VOLT
AMP
MUL
scope - graphics
nV_s
Pd.S4
Pd.S1
Pd.S3
Pd.S6
Pd.S7
Pd.S5
Pd.S2
Pd.S8


Voltage Regulator 15V to 5 V
wide range 7V - 28V
internal operation: 330 kHz
input current 1A
EMC filtering - Class A
Nota: RKZ-152005D
- 5 V
FAULT pin is an open drain
size 1210
each resistor
size 0805
size 0806
+20 V
Nota: RKZ-152005D
DC-DC converter
o pino FAULT é "open drain"
0805 (ich)
1210 (ich)
PWM_H(15V)
PWM_B(15V)
NS4
FAULT_(15V)
GND
SUPPLY_15
SUPPLY_5V
SUPPLY_15V
GND_H
GND_B
VDD_H
VDD_B
READY_(5V)
FAULT_(5V)
PWM_H(5V)
PWM_B(5V)
IC1
ADUM4135BRWZ
IC2
ADUM4135BRWZ
IC3
MC14504BCP
IC4
MC14504BCP
Q1
C2M0025120D
Q2
C2M0025120D
STTH112U
VS-10BQ100-M3_5BT

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