FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO

Low-pass CMOS Sigma-Delta Converter

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Abstract

The continuing need to provide better health for the population requires the development of new and better medical devices. Portable devices for the analysis of biological signals, such as the electrocardiogram or electroencephalogram, are nowadays an important area of development. These devices help health professionals to come up with fast diagnoses on the field and can be used by citizens who require constant vigilance.

Developing these devices brings new challenges to the scientific community, namely at power consumption and data quality of the analog/digital interface. In order to design a good portable medical device, it is necessary an analog/digital converter suitable for low frequencies, with low power consumption and high resolution.

The goal of this work is the design of an converter, based on a Sigma-Delta architecture, that meets the necessary medical requirements.

The converter was implemented in a 130 nm CMOS technology to work in a bandwidth of 1 kHz. The selected sampling frequency is 1 MHz and the source voltage is 1.2 V. The integrators of this Sigma-Delta converter use switched-capacitor and correlated-double-sampling techniques and employ an unusual amplifier typology, in order to reach a high gain without resourcing to *cascode* techniques. The quantizer has a resolution of 1.5 bit and is realized with two dynamic comparators, so the power consumption is minimized.

The results, obtained from a simulated circuit, were a SNR of 87.5 dB and a 1.158 mW power consumption.

Keywords: ADC, Amplifier, CMOS, Comparator, Converter, Low-pass, Low-power, Low-voltage, Sigma-Delta, Switched-capacitor.

Resumo

A contínua necessidade em promover uma melhor saúde à população obriga ao desenvolvimento de novos e melhores dispositivos médicos. Atualmente, os dispositivos portáteis para análise de sinais biológicos, tais como o eletrocardiograma ou o electroencefalograma, são uma importante área de desenvolvimento. Estes ajudam profissionais de saúde a fazer rápidos diagnósticos no terreno e cidadãos com necessidades de vigilância permanente.

A constante evolução destes aparelhos portáteis traz novos desafios para a comunidade cientifica, nomeadamente no gasto energético e na qualidade dos dados obtidos da interface analógico/digital. Para se conceber um bom dispositivo médico portátil é necessário que o seu conversor analógico/digital funcione com frequências muito baixas, que tenha baixo consumo energético e elevada resolução.

O objetivo deste trabalho é descrever o desenho de um conversor, baseado numa arquitetura Sigma-Delta, que vá de encontro aos requisitos acima mencionados.

O conversor foi implementado numa tecnologia 130 nm CMOS para funcinar numa largura de banda de 1 kHz. A frequência de amostragem usada é 1 MHz, e a tensão de alimentação 1,2 V. Os integradores deste conversor Sigma-Delta usam técnicas de capacidades-comutadas e *correlated-double-sampling* e foram realizados com uma invulgar tipologia de amplificador, de forma a obter-se um ganho elevado sem recurso a técnicas *cascode*. O quantizador possui uma resolução de 1,5 bit e é realizado com dois comparadores dinâmicos, de modo a minimizar o consumo energético.

Os resultados, obtidos através de um circuito simulado, foram um SNR de 87,5 dB e um consumo energético de 1,158 mW.

Palavras-chave: ADC, Amplificador, CMOS, Comparador, Conversor, Passa-baixo, Baixa-potência, Baixa-Tensão, Sigma-Delta, Capacidades-comutadas.

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Diogo Dinis da Fonseca

"Para mí la muerte, ahora mismo,
es la diferencia entre haber estado
y ya no estar"

José Saramago

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Listings

Abbreviations

A/D	Analog to Digital
AAP	Axon Action Potential
ADC	Analog-to-Digital Converter
AZ	Autozero
BW	Bandwidth
CDS	Correlated Double Sampling
CMFB	Common-mode Feedback
CMOS	Complementary Metal-oxide-semiconductor
CMRR	Common-mode Rejection Ratio
CT	Continuous-time
D/A	Digital to Analog
DAC	Digital-to-Analog Converter
DEM	Dynamic Element Matching
DNL	Differential Non-linearity Error
DT	Discrete-time
DWA	Data-Weighted Averaging
ECG	Electrocardiogram
EEG	Electroencephalogram
EMG	Electromyogram
ENOB	Effective Number of Bits
EOG	Electro-oculogram
ERBW	Effective Resolution Bandwidth
FFT	Fast Fourier Transform
FoM	Figure of Merit
INL	Integral Non-linearity Error
LSB	Least Significant Bit
MSB	Most Significant Bit
NMOS	N-type MOSFET
NOB	Number of Bits
N_{TF}	Noise Transfer Function
OSR	Oversampling Ratio
PCM	Pulse Code Modulation
PDF	Probability Density Function
PM	Phase-margin
PMOS	P-type MOSFET
RMS	Root Mean Square
S&H	Sample & Hold
SAR	Successive Approximation

SC	Switched Capacitor
SDM	Sigma-Delta Modulator
SFDR	Spurious-free Dynamic Range
SNDR	Signal-to-noise-and-distortion Ratio
SNR	Signal-to-noise Ratio
S_{TF}	Signal Transfer Function
Switch-cap	Switched Capacitor
THD	Total Harmonic Distortion

Symbols

$\Sigma\Delta$	Sigma-Delta
Δ	step Size
ε_Q	Quantization Error

Chapter 1

Introduction

This chapter introduces the actual context of this dissertation and also the objectives to be achieved in the end.

1.1 Context

The digital domain is made for humans by humans. This domain, although it may represent the real world in mathematical terms, is not directly coupled with the phenomena it represents. The heart beating, the current flow, sounds, temperature, time, living beings are all analog. The entire world run in continuous time events with effective continuous amplitude variation. Conversely, a digital system only handles sequence of numbers with finite resolution, thus, in essence, it is a discrete-time and -amplitude system. In order to be able to interpret the information conveyed by the real world, a translator capable of converting the continuous-time and -amplitude signals into discrete ones is needed. This translator is called an analog-to-digital converter (ADC). An ADC thus discretizes the amplitude of signals, but within a window of conversion time, which always implies a finite time resolution. In the same way as an ADC, it is necessary to translate information into the digital domain, a digital-to-analog converter (DAC) is also necessary to allow the digital system to interact or actuate on the physical world. For example, when a person takes a photo with a D-SLR camera, he or she can perceive the landscape, but the camera needs to convert the image to a digital format and process it. Later the owner will want to see the image, and the camera, computer or printer will need to convert the image from digital to analog domain, because the human cannot draw a meaning of what is behind the numbers that represents the image.

At this stage the reader already understands the importance of an ADC in modern technology, as most consumer electronics, if not all, hold inside a digital processing or controlling unit. Every cellphone, sensing or controlling system needs one or more converters. So, it is important for engineers and scientists to study converters and find new methods to keep improving them, either in resolution, speed and/or power efficiency.

Some years ago, with the increasing need for better conversion resolutions, the Sigma-Delta ($\Sigma\Delta$) converter was invented. A simple but powerful and efficient converter that disrupted the

low-frequency measurements. This ADC architecture can convert low-frequency signals with very high amplitude resolution, but surprisingly, based on a converter of just a few quantization bits.

1.2 Motivation

Like most of the integrated circuits, the converters are mainly designed with complementary metal-oxide-semiconductor (CMOS) technologies. Although at a lower pace than in the past, these technologies are still evolving to smaller feature sizes and getting more power efficient year after year. With the decreasing of CMOS size, the logic way is to have more device density per unit area, achieving higher complexity per chip die. Analog circuits are different from digital. To achieve good characteristics, analog circuits normally need more space, more isolation and careful layout design. However, the technology trend has been mainly ruled by digital system demands and complexity, posing a pressure for an increase density of devices per unit area, making the design of analog circuits even more challenging. For instance, the reduction of the size of CMOS devices is followed by a decrease of supply voltages, which is good for power saving, but limits the signal to noise ratio, and transistor intrinsic gains are also becoming smaller, making the design of amplifiers and comparators more difficult. Observing these difficulties, new techniques and methods need to be followed in order to deal with the limitations imposed by lower feature size technologies, taking advantage of faster and more compact circuitry. Because almost all devices are nowadays mobile and battery dependent, the challenge for this dissertation is to perform a conversion with good linearity, such that the signal can be recovered back with a sufficiently high number of effective bits using modern technologies and focusing on low-power consumption and efficiency. There are several ways to accomplish an efficient conversion, but one of the best, with given evidences, is the Sigma-Delta modulator (SDM). It is based on a very low resolution conversion and can accomplish very high effective resolutions, of 16 or more bits, by shaping the quantization noise through filtering of the quantization error signal in the Sigma-Delta loop.

1.3 Goals

In this decade, battery operated devices are very important, so it is necessary to build $\Sigma\Delta$ converters that are very power efficient. This dissertation has as objectives the design of a low-pass, low-power Sigma-Delta converter to operate in bio-potential frequency band range, with focus on battery based devices.

The work comply a set of important steps:

- Design of loop filters;
- Design of comparator;
- Design of DAC.

1.4 Document Structure

This document is divided in six chapters. The first is this one and introduces the project. Chapter 2 presents a background with the most relevant aspects of continuous to discrete conversion. The development and some background of $\Sigma\Delta$ are referred in chapter 3, this also includes a collection of State-of-the-art Sigma-Delta ADCs. Chapter 4 presents the proposal, architecture selection and the simulations. Chapter 5 describes the implementation of this work at circuit-level and the circuit simulation results. At last, chapter 6 summaries the work done.

Chapter 2

Analog-to-Digital Converters

This chapter presents the basics for understanding analog-to-digital converters. It will cover fundantal definition and performance aspects, with a brief reference to Nyquist-rate converters. At the end, the $\Sigma\Delta$ converter is introduced and will be discussed in more detail in Chapter 3.

2.1 Digital-to-Analog Converters

A digital-to-analog converter, shown in Fig. 2.1, is a device that translates a digital input into an analog output (e.g. voltage value between two references).

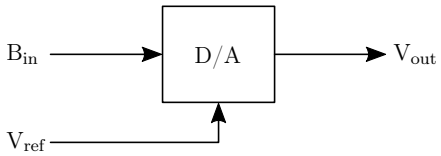


Figure 2.1: Block diagram representing a DAC

Thus, a digital-to-analog (D/A) block produces an analog output (e.g. voltage) from a digital B_{in} word. As expected, there are a few number of possible analog values, specified by the total number of possible binary combinations, or digital words, 2^N, where N is the number of bits. The output signal is relative, so it needs a pair of reference values, V_{ref}^{+} and V_{ref}^{-} that set up the boundaries for the converter output. Knowing the reference voltages and the B_{in} word,the following relationship is obtained

$$V_{out} = V_{FS} B_{in} = V_{FS} \left(b_N 2^{-N} + \cdots + b_2 2^{-2} + b_1 2^{-1} \right) \tag{2.1}$$

where

$$V_{FS} = V_{ref}^{+} - V_{ref}^{-} \tag{2.2}$$

Fig. 2.2 shows the transfer characteristic of an ideal DAC. As referred, a number of well defined values determine the possible analog output values, consequence of a finite number of bits (NOB) – eight level in the used example, including the zero value.

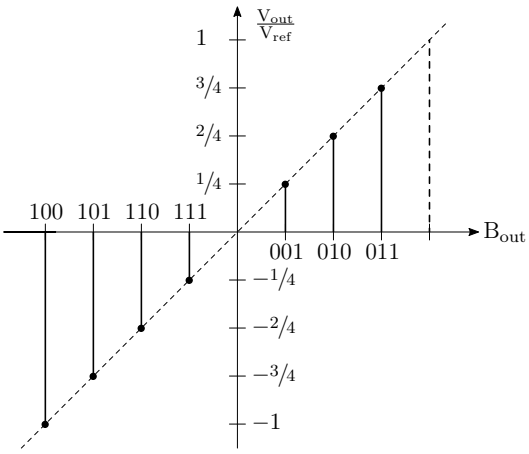


Figure 2.2: Transfer characteristic of a DAC

2.2 Analog-to-Digital Converters

An analog-to-digital converter is a block (Fig. 2.3) that translates an analog input (e.g. voltage) into a digital output word, B_{out}. Because the input signal is relative, it is also necessary a pair of reference values, V_{ref}^{+} and V_{ref}^{-}, that establish the limits where an input is convertible.

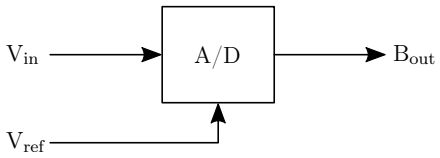


Figure 2.3: Block diagram representing an ADC

The analog-to-digital (A/D) block is necessary because a digital device cannot use continuous signals. Converters only retain a "portion" of the original signal, resulting in a signal that is discrete in amplitude and time. The minimum range of analog amplitudes that are translatable to a single digital value is given by the V_{LSB}, which is defined by:

$$V_{LSB} = \frac{V_{ref}^{+} - V_{ref}^{-}}{2^N} = \frac{V_{FS}}{2^N} = 1\text{LSB} \times V_{FS} \tag{2.3}$$

The least significant bit (LSB) has the same meaning of the V_{LSB}, but without the reference (i.e. it is a number without physical units).

Normally, a converter produces a specific B_{out} from a set of valid input values that contain the value that is perfectly represented and its neighbors in a $\pm\,{}^1\!/_2\,V_{LSB}$ range. This behavior can be modeled by equation

$$V_{FS}\left(b_N 2^{-N} + \cdots + b_2 2^{-2} + b_1 2^{-1}\right) = V_{in} \pm V_x \tag{2.4}$$

where b_N represents the most significant bit (MSB), b_1 the least significant bit and V_x is specified by

$$-\frac{1}{2}V_{LSB} \leq V_x < \frac{1}{2}V_{LSB} \tag{2.5}$$

This behavior creates a signal ambiguity, witch is known as *quantization error*.

An important limitation of converters are their boundaries. The relation presented in equation (2.4) is only valid if the input signal remains inside the range:

$$\left[V_{ref}^{-} - \frac{V_{FS}}{2^{N+1}}; V_{ref}^{+} - \frac{V_{FS}}{2^{N+1}}\right] \tag{2.6}$$

For every input signal that is outside of the range defined in (2.6), represented by letters *a* and *b* in Fig. 2.4, is not correctly quantized and is said to be *overloaded*, the magnitude of quantization error will be bigger than $^1/_2V_{LSB}$ and the quantized value will be at one of the extremes of the range (2.6).

Definition (2.4) only contemplates unsigned codes (i.e. operates only with negative or positive analog signals, exclusively), but normally it is necessary to define a transfer equation that can code negative and positive signals. Doing a brief reference to signed codes, the next definition presents an A/D converter using the most popular signed digital representation (i.e. 2's Complement)

$$V_{FS}\left(b_N 2^{-N} - b_{N-1}2^{-(N-1)} + \cdots + b_2 2^{-2} + b_1 2^{-1}\right) = V_{in} \pm V_x \tag{2.7}$$

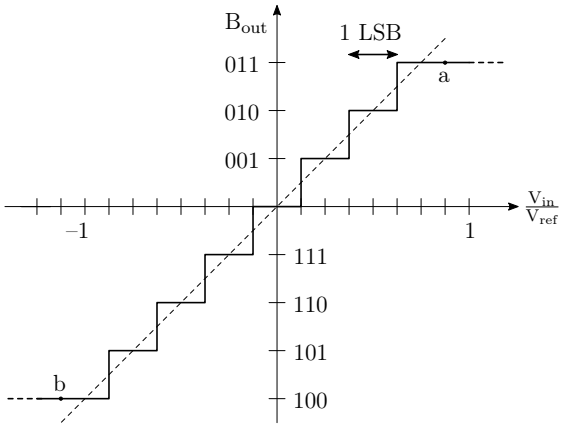


Figure 2.4: Transfer characteristic of an ADC

2.3 Quantization Noise

From section 2.2 it is possible to comprehend that every converter has quantization errors, even the ideal A/D converters. This error depends on the input signal and on the width of quantization intervals – smaller intervals give less quantization errors. Since they are permanent and important to characterize the ADC, they are modeled by an additive noise source, in order to use them in A/D studies.

The quantization noise (V_Q) can be modeled by subtracting the original signal from the quantized one. This approach is represented in Fig. 2.5. Another way to see the same problem is thinking about the quantized signal as being the original analog input plus an addictive noise. However, this is an approximation, in reality there is always a correlation between the error and the input signal, which may be small enough to consider the quantization error as an uncorrelated noise source.

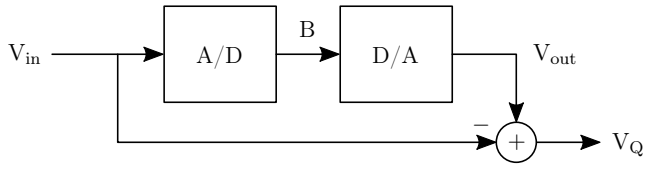


Figure 2.5: Circuit to obtain noise behavior, assuming an ideal DAC

The error, obtained from a ramp input signal with the circuit represented by Fig. 2.5, is shown in Fig. 2.6. Notice that at the extremes of the function the boundaries surpass the range $\pm 1/2 V_{LSB}$, this is a consequence of an *overloaded* signal.

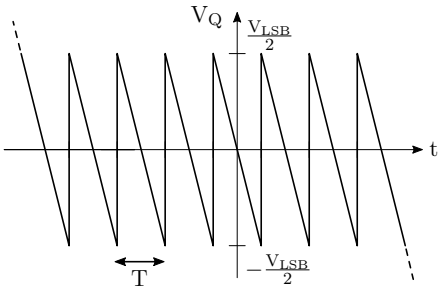


Figure 2.6: Error obtained from an ADC with a ramp input signal

If possible, the quantization error is modeled as white noise. For that, it is normal to assume that the input signal is varying rapidly between (2.6) limits. With that assumption, the quantization noise signal can be accepted as being a random variable uniformly distributed between $\pm 1/2 V_{LSB}$, whose probability density function (PDF) is represented as in Fig. 2.7.

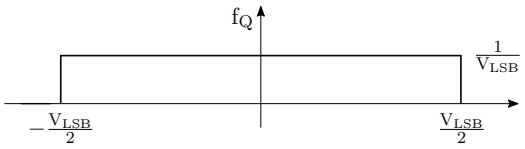


Figure 2.7: Probability density functions of quantization noise of a A/D converter

With the PDF of the quantization noise it is possible to calculate the root mean square (RMS) value, or noise power, of the quantization error:

$$V_{Q(RMS)} = \left[\int_{-\infty}^{\infty} x^2 f_Q(x)\,dx\right]^{1/2} = \left[\frac{1}{V_{LSB}}\left(\int_{-V_{LSB}/2}^{V_{LSB}/2} x^2 dx\right)\right]^{1/2} = \frac{V_{LSB}}{\sqrt{12}} \tag{2.8}$$

The result of equation (2.8), where f_Q is the amplitude of the PDF of quantization noise, is a good approximation for real noise produced from an ADC, principally if the signal satisfy the assumptions for white noise. This value is also a good approach with a fast sampling rate or a large number of bits. From equations (2.8) and (2.6) it is possible to verify that by adding a bit to the converter, the noise power decreases by a factor of 4.

2.4 Specifications and Performance Indicators

2.4.1 Static Specifications

- **Resolution** of a converter defines the number of levels that correspond to distinct digital words. An N-bit resolution converter has 2^N different digital words, so it can convert 2^N analog levels.

- **Analog resolution (V_{LSB})** is an analog increment corresponding to a 1 LSB code change and can be obtained with the converter resolution and the V_{FS} value using the equation (2.3).

- **Input Range** is defined by the converter boundaries, a signal can not be larger than this value, otherwise overloading will occur. The input range of a converter is given by definition (2.6).

- **Offset Error** is a shift in all quantization steps of the converter transfer characteristic curve (dotted line in Fig. 2.8a) in relation to the ideal curve (dashed line). It is described by a deviation of $V_{0...01}$ (i.e. transition from level 0 to level 1) from $1/2$ LSB and is defined by:

$$E_{off(A/D)} = \frac{V_{0...01}}{V_{LSB}} - \frac{1}{2}LSB \tag{2.9}$$

- **Gain Error** is the deviation in slope, of the straight line interpolating the transfer characteristic and the ideal one (represented by a solid line in Fig. 2.8a). A simple way to calculate

the gain error is subtracting the offset error and evaluate the difference between the actual and the ideal curve at full-scale value, $V_{1\ldots1}$ (i.e. transition to last level).

$$E_{gain(A/D)} = \left(\frac{V_{1\ldots1}}{V_{LSB}} - \frac{V_{0\ldots01}}{V_{LSB}}\right) - \left(2^N - 2\right) \tag{2.10}$$

- **Differential non-linearity error (DNL)** is a deviation in the step size (Δ) of a real converter from the ideal width, as shown in Fig. 2.8b. A code k is obtained if the input signal is between $V_{k-1,k}$ and $V_{k,k+1}$ (i.e. k step), so $\Delta_{real}(k) = V_{k,k+1} - V_{k-1,k}$. The DNL of a code is formally obtained with

$$DNL(k) = \frac{\Delta_{real}(k) - \Delta_{ideal}}{\Delta_{ideal}} (LSB) \tag{2.11}$$

  The maximum DNL, which is usually simply referred to as DNL, is the maximum of $|DNL(k)|$ for all k.

- **Integral non-linearity error (INL)** is a measure of the deviation of the transfer characteristic from the endpoint-fit line, represented in Fig. 2.8b. There are other ways to define INL (e.g. deviation from best-fit-straight line), but this one corrects the two limits of the curve.

  Like DNL, the maximum INL, or simply INL is the maximum of $|INL(k)|$ for all k. This characteristic is directly related to DNL, at any value k, the $INL(k)$ value is the running sum of DNLs corrected by the gain error.

$$INL(k) = (1+G)\sum_{i=1}^{k} DNL(i) \tag{2.12}$$

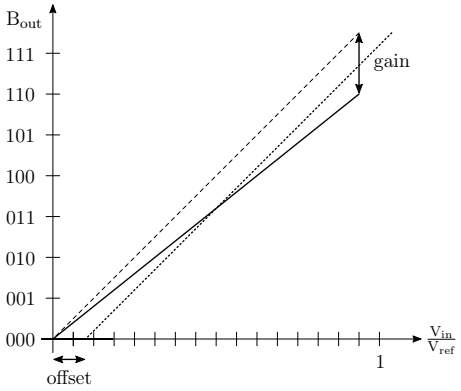
  where G is the gain error.

- **Monotonicity** characteristic indicates that an increasing input signal produces only increasing output values and decreasing input signals produce decreasing output values. A representation of a problem of non-monotonicity is shown in Fig. 2.8c, where a negative slope exists in a real transfer characteristic.

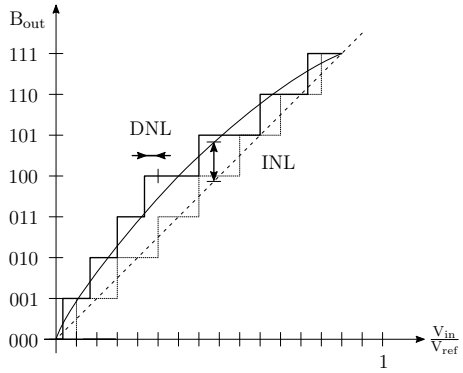
- **Missing codes** is when a digital code is skipped at the ADC output, that is represented by Fig. 2.8c. The quantization interval of a missing code is zero because it is impossible to reach the code. This problem appears in DNL specification as being $DNL_{missing\ code} = -1$, and the maximum DNL of the converter is 1 LSB or larger.

- **Hysteresis** is a dependence of the output signal on the input tendency, it occurs when a transition between two values of transfer characteristic is different depending if the input signal is increasing or decreasing. This characteristic may be desirable in a comparator block of a converter to diminish the transition noise (i.e. consecutive transitions when the

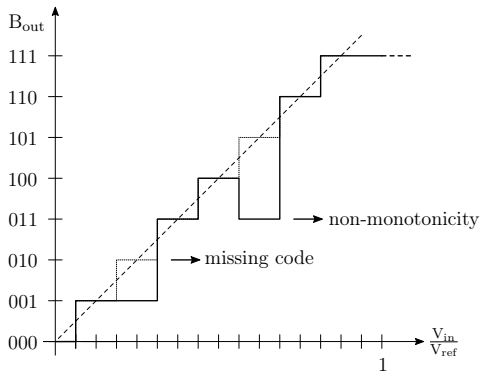
signal value is not well defined), and when occurs, the assumed value is the maximum of such differences, as represented in Fig. 2.8d.



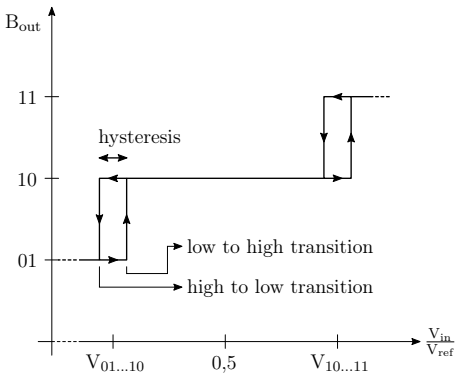
(a) Gain and Offset errors of a ADC



(b) DNL and INL in a A/D converter



(c) Representation of non-monotonicity of a ADC and a missing code



(d) Hysteresis occurring in two transitions of a converter

Figure 2.8: Non-linearities of an A/D converter

2.4.2 Dynamic Specifications

- **Signal-to-noise ratio (SNR)** is the ratio between the power of the signal and the sum of noise produced by the circuit with quantization noise. The noise considered in SNR is only the one found in the Nyquist interval. The obtained value depends on the validity of the used model for quantization noise and on the selected signal used for calculations. Normally a sinusoidal input signal is used for reference.

$$\mathrm{SNR} = \frac{\mathrm{P_{signal}}}{\mathrm{P_{noise}}} \tag{2.13}$$

Although the last formula is correct, it is common to use it with dB units

$$\mathrm{SNR} = 10\log\left(\frac{\mathrm{P_{signal}}}{\mathrm{P_{noise}}}\right) = 20\log\left(\frac{\mathrm{V_{signal(RMS)}}}{\mathrm{V_{noise(RMS)}}}\right) \tag{2.14}$$

For the SNR calculation, it is necessary to have a well defined input wave. The first one is a sawtooth signal, which is a good way to simulate a random signal uniformly distributed, because *"randomly chosen samples from sawtooth waveform in the deterministic case would also have a uniformly distributed probability density function"* [1], so they have the same amount of power. The calculation for the power of this signal is similar to (2.8) but the boundaries of the integral are the limits of the quantizer.

$$\mathrm{P_{sawtooth}} = \frac{\mathrm{V_{FS}}}{\sqrt{12}} \tag{2.15}$$

The second is a sinusoidal wave. Considering the maximum peak-to-peak range equal to the converter boundaries, the sinusoidal power becomes

$$\mathrm{P_{sine}} = \frac{\mathrm{V_{FS}}}{2\sqrt{2}} \tag{2.16}$$

evaluating formula (2.14) for a sawtooth and sinusoidal input signals, respectively:

$$\mathrm{SNR_{sawtooth|dB}} = 6.02\mathrm{N\ dB} \tag{2.17}$$

$$\mathrm{SNR_{sine|dB}} = 6.02\mathrm{N} + 1.76\ \mathrm{dB} \tag{2.18}$$

The SNR with a sinusoidal wave is larger because this one holds more energy than a ramp wave with the same amplitude.

- **Signal-to-noise-and-distortion ratio (SNDR),** also known by SINAD, is similar to the SNR, but contemplates also non-linearity distortion terms. The SNDR ratio is between the RMS value of the input signal and the root sum square of the previous noise with harmonic components. SNDR depends on signal amplitude, but also on its frequency.

- **Dynamic Range** of a converter is, in general terms, the ratio between minimum and maximum signal amplitudes that can be processed correctly, where the minimum amplitude is the one whose SNR value is 0 (i.e. noise with the same magnitude as the signal).

- **Effective number of bits (ENOB)** is the maximum number of bits that a converter can obtain. It is measured with the knowledge of SNR or SNDR.

$$\mathrm{ENOB} = \frac{\mathrm{SNR_{dB}} - 1.76\,\mathrm{dB}}{6.02}\mathrm{bit} \tag{2.19}$$

The previous formula assumes a sinusoidal input signal. This specification can also be named as N_{ef}. In a Nyquist-rate converter this measure is normally smaller than the expected resolution. With oversampling converters the opposite occurs.

- **Total-harmonic-distortion (THD)** is the ratio between the signal power and the total power of the harmonic components. Normally, harmonics are accounted until the tenth [2, p. 610].

- **Spurious-free dynamic range (SFDR)** is the ratio of the input signal RMS value and the RMS value of the highest spurious component in the Nyquist-band. This specification provides information similar to THD but using the worst tone. With large input signals, this tone is one of the harmonics of the signal, but if the signal amplitude is small, the distortion caused by the signal is negligible and tones not related with signal become dominant. Therefore, the highest spurious may not be related to the signal.

- **Effective resolution bandwidth (ERBW)** is the analog input frequency at which the SNDR drops by 3 dB from the low frequency value. The ERBW gives the real maximum bandwidth (BW) that the converter can handle.

- **Equivalent input referred noise** is the electronic noise generated by the circuit of the ADC. This can be seen by putting a *dc* input and verifying that the output is not fixed on a single value, but varies around that value, this variance can be modeled by a white gaussian noise [2].

2.4.3 Performance Indicators

There are several parameters that characterize converters, making it difficult to find a common figure for global assessment. There is, however, a common accepted figure-of-merit (FoM) that compares the power consumption with bandwidth and number of bits. This is a reasonably fair measure for comparison since those parameters are interdependent.

The basic FoM formula is

$$\text{FoM} = \frac{P_{\text{total}}}{2^{\text{ENOB}} \times 2\text{BW}} \,(\text{pJ/conv-step}) \tag{2.20}$$

but the ENOB can be replaced by NOB or BW by ERBW.

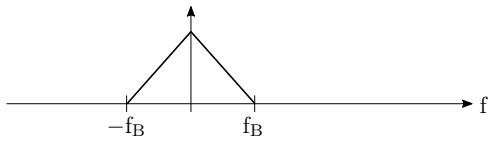
There are more figures-of-merit, each with its own advantages, but they will not be used in this document [3].

2.5 Sampling

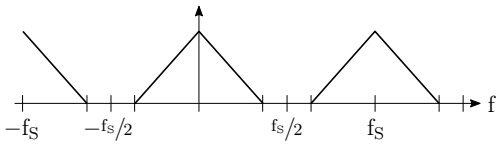
To convert a value from analog to digital, the value has to stay stationary for a specified amount of time in order to give time for the converter to translate it correctly. However, an analog signal changes constantly. To accomplish that, it is necessary to use a block called Sample & Hold

(S&H). It takes a snapshot of the signal and keeps it stationary for the necessary time. In mathematical terms, the S&H block discretizes the input signal that in frequency domain is given by a superposition of infinite replicas of the input.

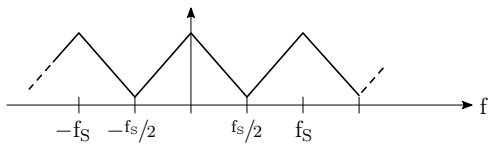
There are some special needs for sampling a signal, in particular with the sampling frequency. As can be seen in the Fig. 2.9, if the sampling frequency is smaller than $2 \times f_B$, where f_B is the bandwidth of the input signal, the spectrum is aliased by its replicas and the information in the signal is corrupted. In order to avoid aliasing problems, the sampling rate has to be larger than $2 \times f_B$ and a low-pass filter has to be implemented at the input of S&H to suppress the noise components that are bigger than f_B.



(a) Continouos-time signal spectrum



(b) Sampled spectrum with $f_s/2 > f_B$



(c) Sampled spectrum with $f_s/2 < f_B$

Figure 2.9: Spectrum of a signal before and after the sampling with different sampling frequencies

The Sample & Hold can also be parameterized using performance specifications.

- **Conversion time** is the minimum time taken for the converter to perform a conversion of one value, including the acquisition time of S&H block.
- **Sampling rate** is the inverse of conversion time, it gives the notion of maximum speed for sampling clock.
- **Settling Time** is the required time for the converter settle on a specific amount of the final value.
- **Aperture Jitter** that can also be named Sampling Time Uncertainty is the time difference between taken samples. The interval among two samples is never equal and this parameter characterizes that error.

2.6 Nyquist Architectures

Nyquist converters generates only an output per input value and their sampling frequency is from 1.5 to 10 times the Nyquist rate. Nyquist architectures remain a very important subject, they are used in high-speed converters and also inside ΣΔ converters that use a quantizer of more than one bit.

There are several types of Nyquist-rate architectures, the most important ones will be briefly presented here.

- **Full-flash** are used in high-speed conversion ratio, because it uses a single clock cycle per conversion. This converter, represented by Fig. 2.10, uses 2^N comparators, having a high input capacitive load and using a large amount of power, besides, it is complicated to obtain high bit resolutions.

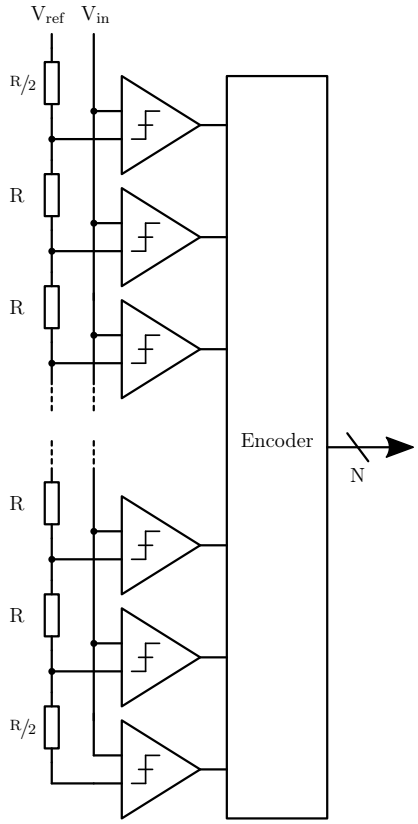


Figure 2.10: Full-flash Converter

- **Sub-ranging flash** uses two chained flash converters – the first for MSBs and the second for LSBs. It needs two or three clock pulses, but uses much less comparators, decreasing the power consumption and input capacitance. A problem associated with these converters is the need for double reference voltages. If a converter of this type is well planned, it

can be faster and have a higher number of bits than a full-flash, because of the lower input capacitive load.

- **Two-steps flash** is similar to the previous converter. The biggest difference is that this uses an amplifier between the two flash converters, thus, it does not need double reference voltages.

  The Fig. 2.11 represents both, Sub-ranging and Two-steps converters. To be a Sub-ranging converter, the gain k is one. If the converter is a two-steps, the gain k needs to be such that the voltage references all equal to both ADCs.

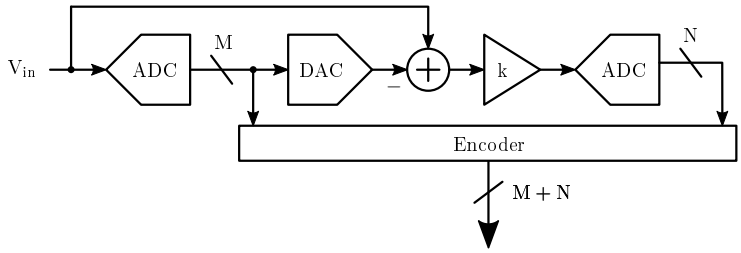


Figure 2.11: Sub-ranging and Two-step Converters

- **Folding** is similar to sub-ranging converter, but do not need a DAC between comparators, having a more linear characteristic. The idea behind this converter is to have several differential-pairs with opposite slops and offsets, folding the characteristic into sub-ranges, in a way that only a differential-pair is active for a given input value, and uses a final flash converter to obtain the digital value. This converter has two big problems, the impossibility to realize a perfect folding and the delays between the differential-pairs, which limits the accuracy.

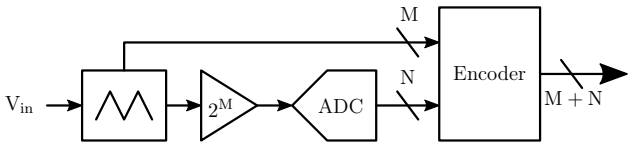


Figure 2.12: Folding Converter

The first block in Fig. 2.12 represents the differential-pairs that will convert the M-MSB. The next blocks are similar to the two previous converters.

- **Time interleave** is a technique to get a similar conversion ratio with less demanding specifications, by using an analog demultiplexer, n converters and a digital multiplexer (Fig. 2.13). In that way, several converters can work in parallel.

- **Successive approximation (SAR)** is a converter that uses the concept of successive approximations. It uses multiple clock periods and uses the knowledge of previous determined

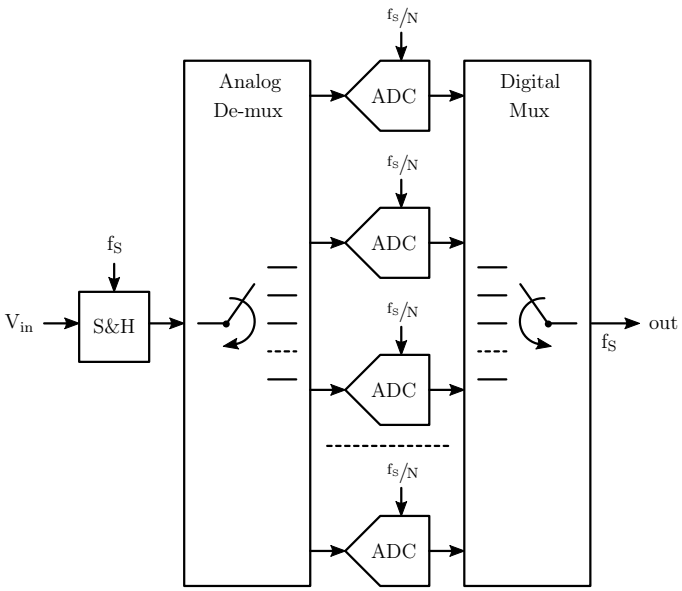


Figure 2.13: Time-interleaved Converter

bits to obtain the next, as represented by Fig. 2.14. This converter can reach high bit resolutions, but, because the use of a clock cycle per bit, it tends to be slow. Although the conjunction of time interleaving techniques with high-speed digital circuits available in recent sub-micron technologies, it is possible, in fact, to have high-speed SAR converters.

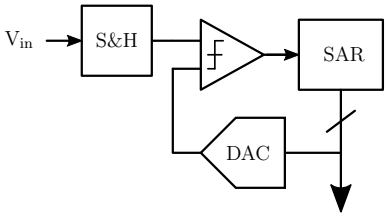


Figure 2.14: SAR Converter

- **Pipelined** is a converter that has its path divided into k stages, with memory registers between them. The Fig. 2.15 represents this converter with k stages and an encoder that needs to be more complex than the others, because the various stages of one sampling conversion end at different clock cycles. Since it has distinct pipelined stages, it is possible to have simultaneous conversions, resulting in a throughput of k times a single stage converter with the same speed. It is possible to design a pipelined converter based on different architectures, such as the two-step or a SAR converter. For example, a two-step converter can be divided into two stages, one for the MSBs and another for the LSBs. When the LSBs of a given sample are being converted the first stage is already converting the MSBs of the next sample. According to the pipeline idea, this converter can be divided into more stages, simplifying the stages until a single bit comparator per stage.

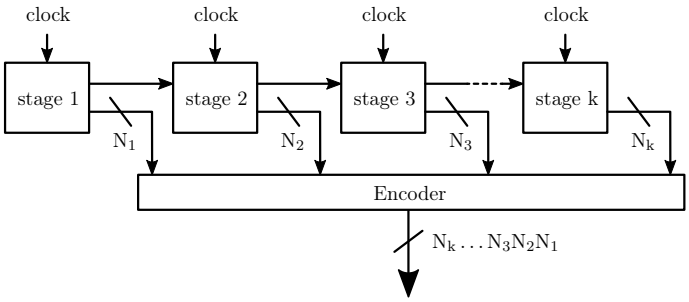


Figure 2.15: Pipelined Converter

2.7 Oversampling

A Nyquist rate converter requires a very accurate low-pass filter, with tight characteristics and has a high in-band noise. Using a sampling rate that is more than 10 times the $2 \times f_B$, where $2 \times f_B$ is the minimum sampling rate to avoid aliasing, it is possible to relax the requirements for the low-pass filter. Nevertheless, such procedure typically demands more complicated digital post processing, however, this does not pose a major problem for modern CMOS technologies.

An important specification of oversampling is the oversampling ratio (OSR), that is defined by

$$\mathrm{OSR} = \frac{f_s}{2f_B} \tag{2.21}$$

where f_s is the sampling rate and f_B is the signal bandwidth. The OSR value oscillates typically from 10 to 512 [1]. But, nowadays, with newer technologies, it is possible to reach larger values.

The oversampling technique reduces the in-band noise compared to a lower sampling frequency. In reality, the total noise power remains the same but spread in a larger band, (i.e. the bandwidth given by the oversampling rate), as Fig. 2.16 shows, and, when a low-pass filter is applied at f_B frequency, the final noise power is lower than in a Nyquist-rate converter with the same signal-band. But the obtained benefit with this technique is bellow the needs for a good quality high-resolution converter. In fact, to improve the converter resolution by only 1 bit, the OSR has to increase by a factor of four. For example, to increase 2 bits, an OSR $= 16$ is needed, but a 6 bit increment needs an OSR of 4096. Using an audio example, a widely considered sampling rate is 44.1 kHz (in fact, it is almost the lowest possible sampling rate, because the Human hearing frequency range is from 20 Hz to 20 kHz), with a common 1 bit converter, without using a noise shaping approach, an OSR of 2^{30} is needed to obtain a CD-quality 16 bit resolution. However, this OSR for this base sampling rate gives an sampling rate of approximately 47.35 THz, which is an unattainable value. So, this technique is used together with others (e.g. noise shaping) to get a desirable result.

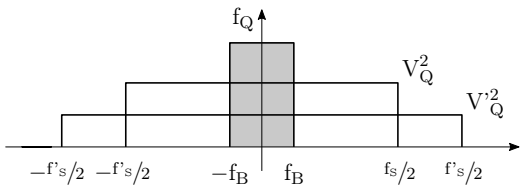
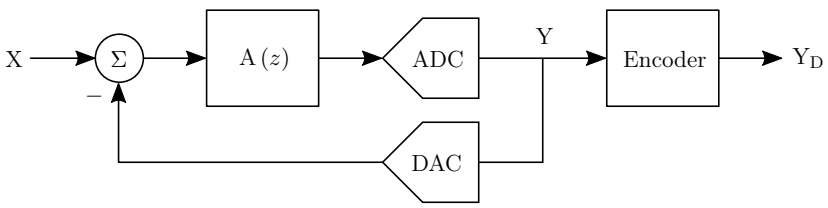


Figure 2.16: Noise spreading with oversampling

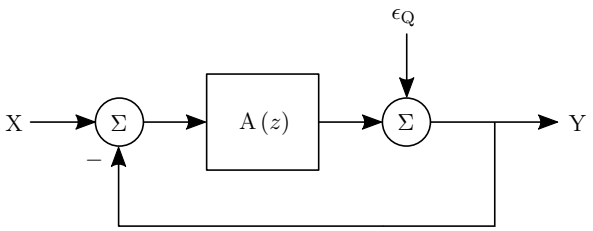
2.8 Sigma-Delta Converter

A Sigma-Delta converter is a converter that uses oversampling, noise shaping and other techniques to improve the ENOB. This section makes a brief introduction to this architecture, but given its importance for the current work, a more detailed analysis will be developed in the following chapter.

Two typical representations of Sigma-Delta converters are represented in Fig. 2.17. The first one is a complete block digram that contains a block to subtract the output signal from the input wave, a filter $A(z)$, an ADC to convert the value from analog to digital, this can just be a comparator (i.e. 1-bit ADC) or have multiple levels, a feedback DAC to translate the ADC output from digital to analog, which allows analog feedback, and an encoder to transform a low-resolution high-speed signal into a high-resolution low-speed one. The second representation is an abstraction that only shows the filter, a white noise model of the ADC and the feedback path.



(a) Complete diagram of a Sigma-Delta



(b) Simplified Sigma-Delta scheme with a noise model for ADC

Figure 2.17: Diagrams of a Sigma-Delta

Since oversampling technique is not enough, another technique, called noise shaping, is applied. In this one, the assumed white noise spectrum is changed to a shaped spectrum where the noise is pushed to higher frequencies, which will be cut with low-pass filtering. In this way the noise referent to quantization present in the signal band is reduced with two different methods. The next equation demonstrates that the signal and the noise are affected by different transfer functions

$$\begin{aligned} & \mathrm{Y} = [\mathrm{X} - \mathrm{Y}]\,\mathrm{A}(z) + \varepsilon_{\mathrm{Q}} \\ \Longleftrightarrow\ & \mathrm{Y} = \frac{\mathrm{X} \times \mathrm{A}(z)}{1 + \mathrm{A}(z)} + \frac{\varepsilon_{\mathrm{Q}}}{1 + \mathrm{A}(z)} \end{aligned} \tag{2.22}$$

where $\mathrm{A}(z)$ is the transfer function of the filter used for noise shaping, Y the output signal, X the input signal and ε_{Q} the quantization error. If $\mathrm{A}(z)$ were infinite, the quantization noise would be zero and $\mathrm{Y} = \mathrm{X}$.

Using this approach, it is possible to improve the SNR of the converter by a factor related to the OSR parameter. Without a noise shaping approach the SNR formula becomes

$$\mathrm{SNR}_{\Sigma\Delta|\mathrm{dB}} = 6.02\mathrm{N} + 1.76 + 10\log_{10}(\mathrm{OSR}) \tag{2.23}$$

and using a first-order filter for noise shaping the SNR formula is

$$\mathrm{SNR}_{\Sigma\Delta,1|\mathrm{dB}} = 6.02\mathrm{N} + 1.76 - 5.17 + 30\log_{10}(\mathrm{OSR}) \tag{2.24}$$

For these calculations a sinusoidal input wave, with power obtained in (2.16), was used. When the noise shaping is used exists a cost (e.g. 5.17 dB for first-order filter), but the gain obtained in SNR is bigger than without this method. For the first case, the SNR improves 3 dB/octave. Using a first-order filter the gain is of 9 dB/octave, which gives an equivalent gain of 1.5 bit/octave.

Its now understandable why Sigma-Deltas are widely used nowadays. If a very-high-resolution converter is needed, the $\Sigma\Delta$ is almost the unique option. This converter will be explained with more detail in the next chapter.

Chapter 3

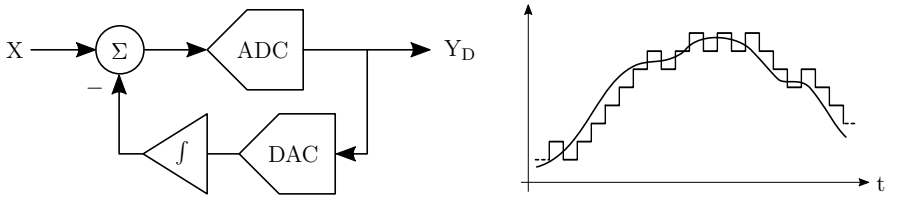
Sigma-Delta Converter

This chapter discusses the Sigma-Delta converter and its fundamental specifications. It will cover the principal approaches of $\Sigma\Delta$ converters and the advantages of different loop filter orders. At the end of Chapter, the State-of-Art of Sigma-delta ADCs will be discussed.

3.1 Sigma-Delta Basics

3.1.1 Delta and Sigma-Delta Modulator

Oversampling original usage was not for stretching of the noise along a wider bandwidth, but to try to increase the effectiveness of a pulse code modulation (PCM) transmission. The idea of oversampling was to use a high rate to transmit the Δ (i.e. difference) between consecutive samples, in place of the absolute value of each sample, used in PCM. The method presented is called Δ Modulator for 1 bit quantization and differential-PCM for multi-bit quantization. The block diagram and a input-output representation are shown by Fig. 3.1.



(a) Digram block of a Delta modulator

(b) Input and output signals of a Delta Modulator

Figure 3.1: Delta Modulator

It is possible to observe in Fig. 3.1 that the output signal is a high frequency signal, it is ideally only constituted by the changes between samples. So, the DC component is not relevant as the modulator has a high-pass response. A problem of this approach is the requirements for the DAC that has to permit a high frequency input tracking.

The creation of the (SDM) results from an alteration of the Δ-Modulator. Changing the position of the integrator block, it will operates on the error difference instead of operating on the signal estimation. Thus, the response of this system goes from high-pass to low-pass. Fig. 3.2 represents the block diagram for a Sigma-Delta Modulator, revealing the reason behind the name of the converter, the result of ΣΔ is the integration (Σ) of the difference (Δ) along samples (perhaps a more coherent reference would be ΔΣ, as the Δ appears first).

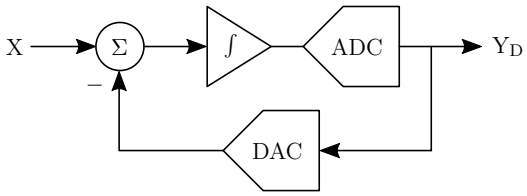


Figure 3.2: Sigma-Delta Modulator

3.1.2 Noise shaping

As shown in previous chapter, the oversampling alone cannot increase much the converter resolution without the use of prohibitive sampling frequencies. Nonetheless, it is used to lower the anti-aliasing specifications and, since the anti-aliasing filter is analog, facilitates the converter design.

To obtain a good bit resolution, another technique is used – Noise shaping. In a converter, the noise spectrum is considered uniform along all bandwidth (i.e. white noise), as shown in Fig. 3.3 in darker gray. The idea of Noise-shaping is to transform the white noise into a shaped noise with more power at the higher frequencies, that will be cut by the digital filter. Thus, the noise spectrum is lowered in the signal band and it is possible to obtain a better SNR only by using a noise shaping filter before the ADC block. As it is possible to note in lighter gray in Fig. 3.3, outside of the signal-band the noise increases, but will be filtered. The behavior of this filter was already referred in Section 2.8, demonstrating that it will act like a low-pass filter for input signals and high-pass filter for the quantization noise induced by the ADC block, shaping out the unwanted noise, moving it from the signal band to higher frequencies.

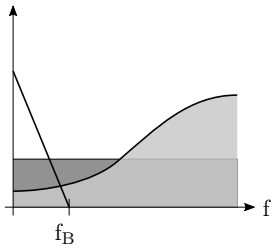


Figure 3.3: Noise shaping technique representation

The two transfer functions obtained from Noise Shaping are often called noise transfer function (N_{TF}) and signal transfer function (S_{TF})

$$\begin{aligned} Y &= \frac{X \times A(z)}{1 + A(z)} + \frac{\varepsilon_Q}{1 + A(z)} \\ &= X \times S_{TF}(z) + \varepsilon_Q \times N_{TF}(z) \end{aligned} \tag{3.1}$$

3.2 Sigma-Delta Converter

Fig. 3.2 represents the first block as an integrator, but this block can be represented by a generic transfer function, as shown in Fig. 3.4. The Sigma-Delta Converter is formed by a filter $A(z)$ and a quantizer, followed by a feedback feeding path.

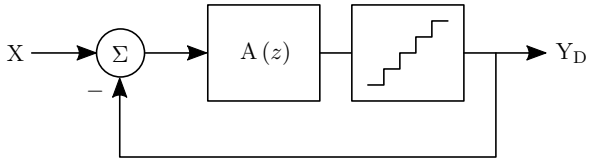


Figure 3.4: Diagram block of a Sigma-Delta Modulator

The input is integrated by the loop filter $A(z)$ and the quantizer produces the digital output. Depending on the type of converter, an extra block may be needed in the feedback loop (e.g. in the SDM to be created in this scope, the block required will be a DAC). The feedback signal obtained from the output will be subtracted from the input to create the error difference signal, which will be the next input of the loop (i.e. integration of differences). This behavior is shown in Fig. 3.5.

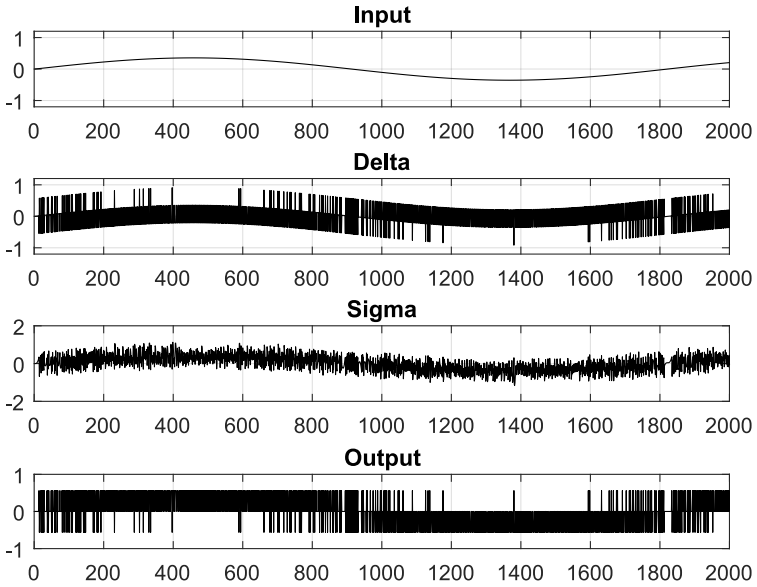


Figure 3.5: Signals of a Sigma-Delta Modulator

In section 2.7, quantization error (ε_Q) was presented like being a noise of the quantizer used in the $\Sigma\Delta$ loop, in reality, this ε_Q is composed by the quantization noise, explained in section 2.3, plus other noises sources inside the loop.

3.2.1 1 Bit Converter

To have a good converter, a high resolution is important, but the more levels the converter has, the harder is to have good characteristics, specifically, INL and DNL, lowering the SNDR.

Using the $\Sigma\Delta$ approach, a single bit quantizer is a possibility. This quantizer has a unique quality, it is inherently linear, because of having only two output values, the transfer characteristic curve is always a straight line with perfect DNL and INL characteristics. Another advantage is the simplicity to design a DAC that converts only two values. Off course that a single bit quantizer will not produce the highest resolution converter, but it is the basis for a SDM build and keeping with low resolution quantizers will result in good DNL and INL performance, simplifying also the design of the feedback DAC.

3.2.2 First-Order Noise shaping Filter

As said before, S_{TF} is a low-pass filter and N_{TF} is a high-pass filter. But for that the $A(z)$ block needs to have special characteristics.

Remember that N_{TF} should have a zero at DC for being a high-pass filter and

$$S_{TF}(z) = \frac{A(z)}{1+A(z)} \tag{3.2}$$

$$N_{TF}(z) = \frac{1}{1+A(z)} \tag{3.3}$$

For that the $A(z)$ can be a simple discrete integrator, like

$$A(z) = \frac{1}{z-1} \tag{3.4}$$

Since this is a simple integrator, the scheme is the one represented by Fig. 3.6 and the transfer function is

$$Y(z) = X(z) \times z^{-1} + \varepsilon_Q(z) \times \left(1 - z^{-1}\right) \tag{3.5}$$

the signal at output is a delayed version of the input plus a high-passed noise.

Calculating the noise power in the band-of-interest, the approximated result is

$$P_{noise} \cong \frac{\Delta^2 \pi^2}{36} OSR^{-3} \tag{3.6}$$

and the obtained SNR is

$$SNR_{\Sigma\Delta,1|dB} = 6.02N + 1.76 - 5.17 + 30\log_{10}(OSR) \tag{3.7}$$

The use of a first-order shaping filter gives a 9 dB improvement per octave over a converter without noise shaping filter, which corresponds to a gain of 1.5 dB/octave.

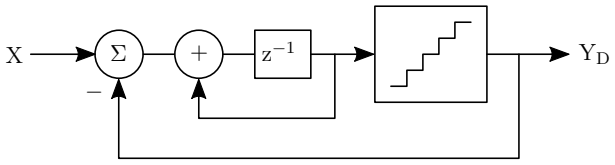


Figure 3.6: First-order Sigma-Delta Modulator

3.2.3 Second-Order Noise shaping Filter

A second-order noise shaping implies that the N_{TF} is a second-order high-pass function

$$N_{TF}(z) = \left(1 - z^{-1}\right)^2 \tag{3.8}$$

and a desirable S_{TF} is $S_{TF}(z) = z^{-1}$ to have only a unitary delay.

The schematic in Fig. 3.7 represents the given S_{TF} and N_{TF}.

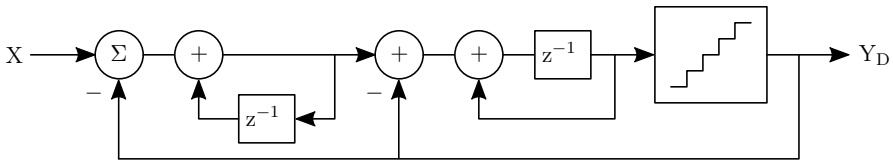


Figure 3.7: Second-order Sigma-Delta Modulator

The resulting quantization noise power over band-of-interest is

$$P_{noise} \cong \frac{\Delta^2 \pi^4}{60} OSR^{-5} \tag{3.9}$$

and the SNR for the second-order modulator is now

$$SNR_{\Sigma\Delta,2|dB} = 6.02N + 1.76 - 12.9 + 50\log_{10}(OSR) \tag{3.10}$$

For this time, the improvement is about 15 dB/octave over a converter without noise shaping filter, which is equivalent to a gain of 2.5 bit/octave.

3.2.4 Noise Transfer Function Curves

A noise shape structure does not reduce the noise, in reality, with one more block in the chain the total noise power increases. This effect can be seen in Fig. 3.8. However, since the curve of PDF changes with the increase of the noise shaping order, the noise power will decrease in the band-of-interest.

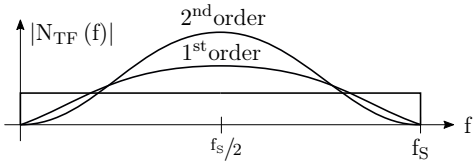


Figure 3.8: Representation of probability density function of a converter without Noise shaping and with first and second order noise shaping

3.2.5 Higher Order Noise shaping Filter

As seen in the previous section, increasing the order of noise shaping structure will increase the SNR or unlock the possibility to use a less demanding sampling rate to reach the same SNR value, since less noise power stays inside of the band-of-interest.

An Lth order noise shaping can achieve an SNR of

$$\mathrm{SNR}(L) = 6.02\mathrm{N} + 1.76 - 10\log_{10}\left(\frac{\pi^{2L}}{2L+1}\right) + (20L+10)\log_{10}\mathrm{OSR} \tag{3.11}$$

An Lth order can improve the SNR by $6L+3\mathrm{dB/octave}$, that is equivalent to $L+0.5\mathrm{bit/octave}$.

The graphic represented in Fig.3.9 shows the evolution of SNR with the increase of OSR using several order of noise shaping filters.

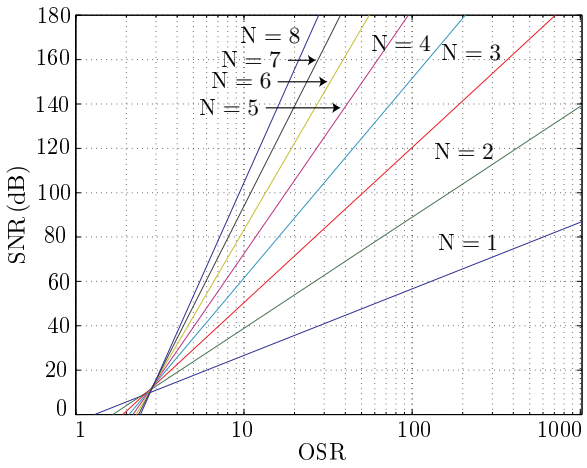


Figure 3.9: SNR versus OSR using different order noise shaping functions [2]

3.2.6 Multi-bit Converter

As explained in 3.2.1, 1 bit converters are very linear and have simpler DACs in feedback because of having only two levels, but they have some disadvantages. In order to obtain a high ENOB, it is necessary to use a higher sampling rate, which brings its own problems, related to power consumption and clock jitter. It also complicates the design of amplifiers because their bandwidth needs to be larger than the clock frequency, and need a higher order noise filter, which increases

the instability of the system, since the feedback error is larger and idle tones are more perceptible. These are diminished in multi-bit SDM.

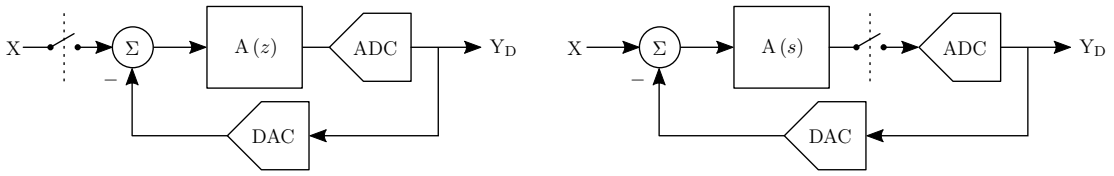
With a multi-bit quantizer, the ENOB can be larger without an increase of the modulator order or the OSR. This approach also has some drawbacks, such the difficulty of designing linear ADCs and DACs with more that 1 bit, but since these components are inside a ΣΔ loop, a 3 or 4 bit converter can reach 16 or more ENOB.

To accomplish the multi-bit quantizer, any of the Nyquist-rate converters presented in section 2.6 can be used, but it will need to obey the constraints imposed by the specifications.

3.2.7 Discrete-time and Continuous-time Sigma-Delta Modulator

In a continuous-time (CT) architecture, the sampler is inside the loop (i.e. the sampling is made after the filter), so its non-idealities are attenuated by the feedback. A discrete-time (DT) converter has the sampler outside the loop and its non-idealities will degrade the converter performance. When a converter is built, an important difference is that in a CT-ΣΔ the filter is realized in *s-domain* and in a DT-ΣΔ is in *z-domain*. The structural differences are represented by Fig 3.10.

In a DT converter, the data is sampled before entering the loop filter, so the input signal will be formed by steps and a filter with a larger slew-rate will be necessary than in CT converter. A common approach of DT-ΣΔ is with switched-capacitor (switch-cap) circuits, where the coefficients are set by a ratio of capacitors, so deviations in absolute values of capacitors are not relevant. It is possible, with clever layout, to make the ratio of capacitors very precise. Unfortunately, in a CT converter, this is not possible and coefficients have bigger deviations from expected, generating larger non-idealities.



(a) Block diagram of discrete-time Sigma-Delta converter (b) Block diagram of continuous-time Sigma-Delta converter

Figure 3.10: Block diagrams of Sigma-Delta converters

3.2.8 State-of-Art of Sigma-Delta ADCs

Despite recent advances, the ΣΔ architecture is not new in the literature. In these last years the trend is to adapt this converters to band-pass situations, suitable for communications and to create structures that have a high number of bits, with low power consumption to use in portable audio devices and bio-medical devices powered by battery.

Since the band-pass scheme is out of the scope of this dissertation, this section will only contemplate the low-pass structures.

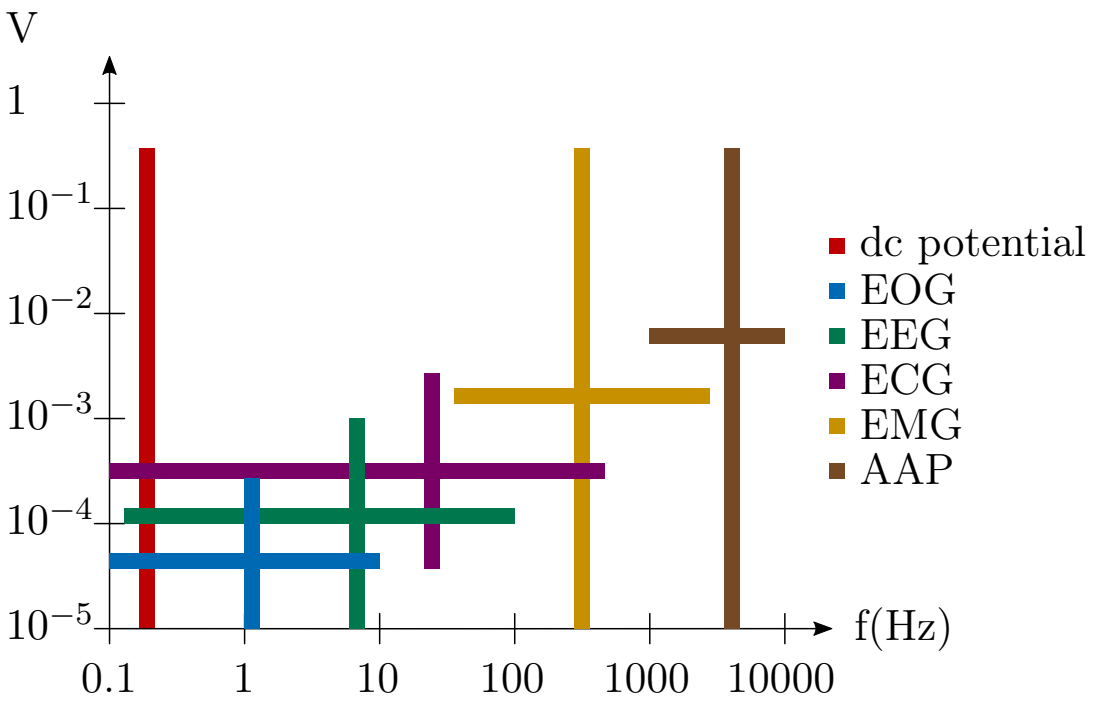


Figure 3.11: Voltage and frequency range of the most relevant bio-potential signals [5]

There are three tables below. Table 3.1 contains the more common low-pass converters, discrete-time with switched-capacitor elements and switched-opamp (SO) technique. Table 3.2 have the continuous-time converters for the same bandwidth. Table 3.3 contains some different converters that deserve to be mentioned.

Distinct criterion was used to search for more relevant converters. Since the objectives for this dissertation are to obtain a low-pass (i.e. bandwidth since a few Hz to audio-band) and low-power $\Sigma\Delta$, these were the most important criteria. Then, the ENOB of all converters was calculated with (2.19), using SNDR instead of SNR, when it was provided. To be able to compare all converts, the FoM described in (2.20) was used. Considering that FoM is the performance indicator parameter, the converters are sorted in its ascending order, since lower is better.

The converter to be done in this dissertation is not a continuous-time converter, but some of these have interesting values (e.g. FoM of converter of report [4]) and they may have some interesting blocks to study.

As can be seen in Fig. 3.11, most of biological signals have a small bandwidth, so, if the purpose of the converter is for one of these signals, a good design option is to design a sub-1 kHz bandwidth converter, obtaining a better SNR with same power consumption. This approach can be confirmed in next paragraphs.

The authors in [6] and [7] made low-pass converters with a BW of only 250 Hz. These converters are not interesting for an audio implementation, but have very-low-power consumption, ideal for portable devices to realize medical tests, like electro-oculogram (EOG), electroencephalogram (EEG) and electrocardiogram (ECG). They show an ENOB of 7.2 and 7.8, respectively, and low

FoM. In [7], the authors use amplifiers with a folded-cascode design to increase the gain, but did not reuse it in the converter of their other paper [6], obtaining a converter that works with 0.6 V and has a better FoM. They use a feed-forward architecture to achieve an efficient operation at low supply voltages.

Other reports, such as in [8] and [9], refer low bandwidth applications. The first has some interesting results. The authors made three different implementations, one with a normal active second-order SC noise shaping filter, another with an active filter in the first stage and a passive in the second stage and the last with only passive filters. Passive filters are more subjected to non-idealities and SNDR is lower than with active filters, but the power consumption is also lower and the drawback of SNDR may not be more important than the power saving gain. Using a power supply of 0.7 V on the full-passive converter, it is possible to obtain the less power consumer of all DT converters here reviewed. The authors in [9] designed a reconfigurable converter that can work with three different bandwidths, 256 Hz, 2.048 kHz and 16 kHz, for different medical applications and audio-band, respectively. It has, unlike most others, a low power 4 bit SAR quantizer, achieving a high resolution of 16 bit with an 8.6 µW power consumption for the lowest band.

Some authors refer more general converters, which can be used in a wide range of bio-potential signals. These converters have a bandwidth of about 10 kHz, being useful not only for EOGs, EEGs, ECGs, but also for other medical tests, such as electromyograms (EMG) and axon action potential (AAP), which needs a larger BW [9]. The report referenced in [10] have a full-clocked switched-opamp, saving power, with that feature it has the best FoM of the analyzed SC converters. The article also refers to an audio-band version with a 17-level flash ADC instead of a comparator, getting 15 bit of resolution with only 58 µW of power consumption. The authors of [11] aim to consume less power than a conventional converter using a charge-pump integrator, but power consumption is 10 times bigger that converter of paper [10]. The authors of [12] create a converter that works with a supply of only 0.25 V, which is relevant for using in medical implants, so it is important to study the used techniques to achieve such interesting values. Authors in [13] and [14] use a single-phase clocking technique, which avoids the clock phase generator non-idealities, but both do not achieve a great result with this technique. Authors of paper [15] enhance the performance of a Sigma-Delta converter by modifying the differential pair of the operational transconductance amplifier (OTA), since the OTA is the most power-consuming block of a $\Sigma\Delta$ converter. The paper referenced in [16] combines switched-capacitor with switched-opamp to take advantage of both techniques, but the result is not better than other converters. The converter of paper [17] has feed-forward in output of both integrators in order to decrease their maximum swing output, the adder of second feed-forward path is a passive analog adder, saving power. This converter has a 4 bit SAR ADC, that is very power efficient and uses a low area. The converter in [18] has only a 8 kHz BW, but works well for almost all bio-potential signals, it only uses MOSFET components, so all capacitors are MOSCAP (i.e. capacitors designed with MOSFETs), occupying less area, but more susceptible to process variations.

The last group of discrete-time converters are those that are made for audio-band signals. Since

Table 3.1: Discrete-time Converters

Ref.	f_S (MHz)	BW (kHz)	SNDR (dB)	Supply (V)	Power (µW)	Filter order	FoM (pJ)	Technology node (nm)
[10]	0.64	10	85	1	13	4	0.045	180
[19]	2.5	20	81.7	0.5	35.2	4	0.089	130
[20]	1.92	20	81	0.6	34	5	0.093	130
[21]	4	20	81	0.7	36	3	0.098	180
[17]	1	10	80	1	22.4	2	0.137	65
[9][a]	0.065	0.265	99	1	8.6	2	0.231	180
[9][b]	1.05	16	75	1	39	2	0.265	180
[8][c]	0.5	0.5	65	0.7	0.43	2	0.296	65
[11]	2.5	10	87.8	1.2	148	2	0.369	130
[22]	20	20	73.1	0.9	60	4	0.406	130
[8][d]	0.25	0.5	76	0.9	2.1	2	0.407	65
[12]	1.4	10	61	0.25	7.5	3	0.409	130
[8][e]	0.25	0.5	70	0.9	1.27	2	0.491	65
[8][c]	0.5	0.5	67	0.9	0.92	2	0.503	65
[13]	5	10	80.1	0.9	200	2	1.210	180
[15]	1.28	10	68.6	0.9	60	2	1.364	180
[14]	5.12	10	84	0.9	400	2	1.544	180
[18]	1.024	8	67	0.7	80	2	2.733	180
[16]	2.56	10	70.49	1.8	161	2	2.944	180
[6]	0.01	0.25	45	0.6	0.54	3	7.434	180
[7]	0.01	0.25	48.19	0.8	0.816	3	7.542	180

[a] Very-low-band approach of converter of paper [9].
[b] Audio-band approach of converter of paper [9].
[c] Implementation of converter of report [8] with passive filters.
[d] Implementation of converter of report [8] with active filters.
[e] Implementation of converter of report [8] with a passive and a active filters.

bio-potential signals have a smaller band, these converters are well suitable for those signals, but normally consume more power. The reports referenced in [19], [20] and [21] are exceptions to this assumption, because they consume only 35.2 µW , 34 µW and 36 µW, respectively, which is less than some converters with a lower bandwidth. The first uses input-feed-forward topology and a double-sampled $\Sigma\Delta$, the second obtain a good performance by suppressing a sub-threshold-leakage current in SC meshes, and the third increases the power efficiency by replacing the OTA with an inverted-based SC. The last DT converter [22] is a quite normal $\Sigma\Delta$ converter, working in this context such a reference to compare all the others converters.

The authors of report [23] made the unique CT converter suitable to very-low bandwidth reviewed in this document. This converter suits well for ECG and EEG applications. It includes the preamplifier necessary to amplify these signals that are very low-voltage. The proposal is to exchange from a traditional block diagram of a front-end circuit to one simpler with less components (i.e. less noise) and a CT sigma-delta modulator.

Table 3.2: Continuous-Time Converters

Ref.	f_S (MHz)	BW (kHz)	SNDR (dB)	Supply (V)	Power (μW)	Filter order	FoM (pJ)	Technology node (nm)
[4]	2	10	58	0.4	0.41	2	0.032	130
[24]	3.072	24	90.8	1.8	121	3	0.066	180
[25]	2.56	20	79.1	0.6	28.6	4	0.097	130
[26]	3.2	25	74	0.5	370	3	1.807	180
[27]	12	20	76.5	1.1	1200	2	5.492	45
[23]	0.256	0.2	57.9	1	1.614	3	6.289	180
[28]	12	20	74	1.2	2200	2	13.428	65

[a] Used the SNR value once the SNDR is not available in report. For the SNR value an A-weighted input was used, since this converter is specifically for audio applications.

An interesting article, because of its low-power consumption and low-voltage, having a great FoM, is that referenced in [4]. It uses an opamp-less topology and a passive-loop filter to save power and MOSCAPs to save area. It also has a bandwidth of 10 Hz, a good value for almost all bio-potential needs.

All other CT converters are suitable for audio-band signals. The converter of article [24] has a good performance, getting an SNDR larger than 90 dB with a 24 Hz BW with a relative low-power consumption. This is an important mark, because this dissertation tries to design a DT converter with an SNDR approaching this value. For a good SNDR, the authors of the converter use a 4 bit flash ADC and an active-RC loop-filter. The converter in [25] has a worst SNDR than previous, but the authors obtained a much lower power consumption and a sub-1 V supply. Authors of [26] aims to use a true low-voltage design, without internal voltage boosts or low-threshold devices. In order to obtain a correct operation with low-voltage, they use some approaches such as body-input gate-clocked comparator and a return-to-open feedback DAC. The only converter done with the 45 nm technology node is the one referenced at [27], this article demonstrate the augment of flicker noise with the decrease of technology is restrictive, thus, it is possible to observe in table 3.2 that this is not the best converter, besides the use of a modern technology. In the other hand, the power supply and area may be smaller and it is possible to compensate some problems with a more robust digital component. The last CT converter, in [28], has a specific goal, it is to be connected directly to a microphone without a preamplifier or an anti-aliasing filter. It is relevant because the use of a more recent technology node, the authors had to deal with the problems previously mentioned.

In table 3.3, some others converters are mentioned. Authors of converters [29] and [30] design converters with a 90 nm technology, using the same approach. The converters can operate with a supply of 0.2 V using a frequency-to-digital $\Sigma\Delta$, *"where the input signal is frequency modulated in a voltage-controller oscillator (VCO)"* [30], in fact this converter uses one more block, the VCO, but can operate at very low voltages. The converter referenced in [29] has a lower SNDR, but it is a very-low-power converter with an audio-bandwidth, in fact it is the converter that consumes less power per bandwidth. The other converter consumes more power but it has a much better

SNDR, and an ENOB of almost 10 bit, which is a remarkable characteristic for a very-low-voltage converter. Authors of [31] obtained a good SNDR with a low sampling rate by using a signal adaptive control architecture, where the feedback to the second stage of noise shaping filter can go trough different blocks selected by a switch, but distortion factors increase comparative to a more traditional converter.

The last analyzed converter [32] is an adaptive Sigma-delta ADC. It can exchange between two sampling rates, depending on the input signal slope. It also had a SAR ADC in the quantizer block in order to achieve an ENOB of 7.3 bit. With a low bandwidth, together with the sampling-rate change approach, the converter can achieve high power savings, consuming only 151 nW. Unfortunately, the information available in this article is not sufficient to do a fair comparison with others.

Table 3.3: Others Converters

Ref.	f_S (MHz)	BW (kHz)	SNDR (dB)	Supply (V)	Power (µW)	Filter order	FoM (pJ)	Technology node (nm)
[29]	3.4	20	44.2	0.2	0.44	1	0.083	90
[30]	12	20	60.3	0.2	7.5	1	0.222	90
[32]	0.02	–	45.3	1	0.151	–	0.487[a]	180
[31]	0.5	3.4	63	1.2	38	2	4.841	350

[a] FoM not calculated due to lack of bandwidth information, used the paper FoM.

Chapter 4

Low-pass Converter for Bio-potential Signals

This chapter presents an outline of the work developed in this dissertation. It describes the objectives and architecture definition. At the end, simulations are made to gauge the effectiveness of the architecture.

4.1 Proposal

This dissertation proposes the design of a low-pass, low-power and high-resolution ΣΔ converter. As a preliminary work, the selected application target was the conversion of bio-potential signals, because of their importance in present times, and which, in many cases, demand high bit resolutions.

The proposed converter is inspired mainly by an interesting 2^{nd}-order converter described in [17], where the authors obtained a high SNDR of 80 dB, consuming only 22.4 µW, with a relatively low OSR and a bandwidth of 10 kHz. Another important reference is the 3^{rd}-order converter reported in [33], where a 1.5 bit quantizer is used to improve the SNR. Since high-resolution converters are important for better medical analysis, preferably with resolutions above 16 bits, the needed SNDR value has to be at least 98 dB. This is a value difficult to reach with such low-power converters, as in those reported architectures. It is also the case for the architecture that is developed in this work. However, the goal is to keep low-complexity and low-power.

As referred, this work targets mainly the conversion of ECG or other bio-potential signals with the same bandwidth requirements. Thus, the respective bandwidths can be lowered to 1 kHz or less, as it can be verified in Fig. 3.11. Using a larger OSR of 1024, it is possible to obtain a theoretical resolution of 24 bit from a 2^{nd}-order converter with a 1 bit quantizer, which has the advantage of having a transfer characteristic inherently linear. The process chosen to develop the circuits is a double-well, 130nm CMOS technology.

4.2 Second-order Low-Pass Sigma-Delta

Finding the best ΣΔ architecture is a difficult task, and involves a set of trade-offs, mainly complexity and power consumption. After a few analysis, and keeping the focus on minimum power consumption to favor portability, the following guidelines and specifications were defined:

- Second-order Sigma-Delta Converter;
  - The choice of a 2^{nd}-order noise shaping filter relates to two main reasons. It is more effective than a first-order loop filter, meaning better SNR, and has no stability problems, as higher-order loop filters have. When a higher-order loop filter is used, some changes are imperative to stabilize the system, such as a larger attenuation on the integrators, which will decrease the effective SNR. Furthermore, higher order ΣΔ converters naturally implies the use of more amplifiers, meaning more power consumption.
- Bandwidth of 1 kHz;
  - This bandwidth covers the ECG bandwidth without restriction. The use of larger bandwidths would enable the conversion of more signals than the specified, however, such will imply amplifiers with higher slew-rates and bandwidths, for the same OSR in relation to the Nyquist frequency, resulting in more power consumption.
- OSR = 512;
  - The converter uses a high OSR to improve the SNR, but, since the signal bandwidth is small, the final sampling frequency is only 1 MHz. The SNR could be further improved with a higher OSR, but that implies amplifiers with larger gain-bandwidth products. In fact, a good performance is granted if the gain-bandwidth product is near to five times the sampling rate [2], but as the bandwidth requirements increase, more difficult it is to get, and, once again, implies more power consumption.
- 1.5 bit Quantizer;
  - A higher bit quantizer improves significantly the SNR over 1 bit quantizers. Unfortunately, nonlinearity eventually overcomes the SNR gain, which is especially limited by the DAC due to mismatches. A 1.5 bit is a good compromise in this respect.
- Feed-forward topology;
  - This is a method to decrease the output swing of integrators, by introducing a path between the input of the modulator and the output of each integrator, which negligible changes the signal and does not introduce substantial non-idealities.

The block diagram of the 2^{nd}-order converter is represented in Fig. 4.1. Both integrator gains A and B are unitary, which the reason will become apparent later in the document.

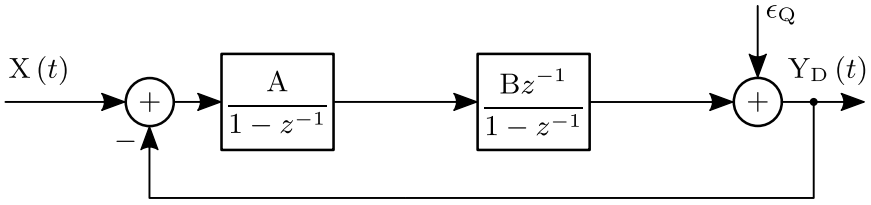


Figure 4.1: Block diagram of the 2nd-order Sigma-Delta Modulator

4.3 Stability and Integrators Output Swing

A second-order ΣΔ has no big stability issues, since a feedback path is used to dump the second integrator of the loop filter [2], as shown by Fig. 4.2. With this technique, the second integrator becomes an approximated integrator that includes the quantizer in the dumping loop. There are other ways to do the dumping, but this one gives an optimal transfer function, since the signal component is only affected by a delay, as equation (4.1) shows. This dumping path resolves the stability problems, but voltage peaks may occur at the amplifiers output, especially when the input signal is almost equal to the reference voltage. It is then necessary to limit the input signal, the loop-gain or use other auxiliary techniques, such as feed-forward.

$$\mathrm{Y}(z) = \mathrm{X}(z) \times z^{-1} + \varepsilon_{\mathrm{Q}}(z) \times \left(1 - z^{-1}\right)^2 \tag{4.1}$$

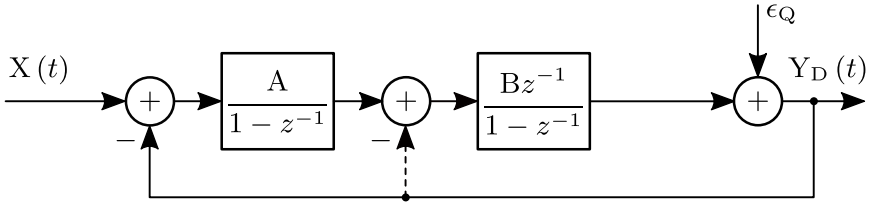


Figure 4.2: 2nd-order ΣΔ Modulator with a dumping path represented by a dashed line

In certain cases, even if the loop-filter is stable, the output swing of the integrators can be larger than the supply voltage (Fig. 4.3), which is not tolerable in a real system. This is due to large quantizing noise when low-resolution quantizers are used. When the amplitude of the integrators input is higher than the reference, there are several options to solve it, such as those named previously. An attenuation in integrators seems a good option, because the loop-filter will be stable between the imposed boundaries, and allows the use of a larger input signal. However, this approach has some designing problems. Since the converter is to be designed using discrete-time switched-capacitor techniques, there are no resistors and the absolute value of capacitors is not important for the transfer function. Only the capacitor ratio is important, which can be made very precise (it cannot be forgotten, though, that the absolute value of capacitors is important for other measures, such as the settling time). Knowing that accurate ratios are required and that in fabrication processes it is easier to obtain a good ratio if the capacitors have equal values, the

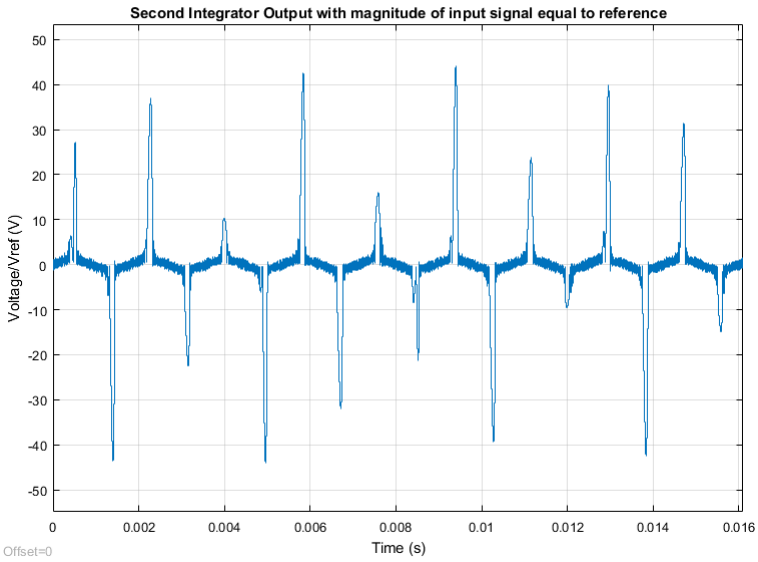


Figure 4.3: Second integrator with a too large output swing

integrators attenuation is a method to be avoided, because it needs capacitors with different values. Solutions, such as lower input signal, or lower reference for the DAC are more acceptable options – in fact, the majority of bio-potential signals have a lower amplitude (Fig. 3.11), so low input requirements will not be difficult to satisfy.

Reducing the maximum magnitude of input signals and reference voltage to lower values limits the converter operation and its effective SNR, so it is important to find an equilibrium between these and other alternatives. One way to resolve the issue is through a feed-forward path (Fig. 4.4) that will cancel the signal component at output of amplifiers, lowering their swing – this is applied in this work.

After drawing the block diagram with feedback, feed-forward and second integrator dumping (Fig. 4.1), the transfer function is given by:

$$\mathrm{Y}(z) = \mathrm{X}(z) + \varepsilon_{\mathrm{Q}}(z)\left(1 - z^{-1}\right)^2 \tag{4.2}$$

It is possible to observe the absence of a delay in the input signal, thanks to the double feed-forward scheme. In the next chapter, the delay will be added again because of the converter design, which does not harm the final performance.

4.4 Design Decisions and Simulation Results

The Sigma-Delta Converter was simulated with the Simulink Toolbox of MathWorks, together with Matlab. To launch the Simulink model, represented by Fig. 4.5, a Matlab script (A.2) has bean written based on several models of Maloberti's book [2]. This simulation was important

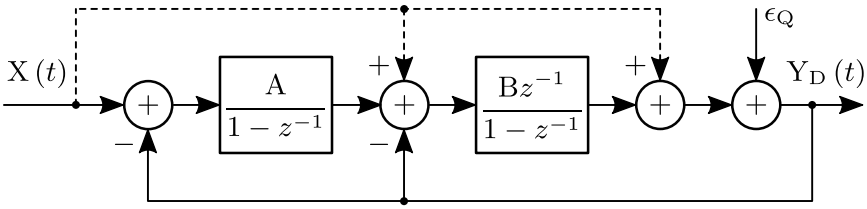


Figure 4.4: 2nd-order ΣΔ Modulator with a feed-froward path represented by a dashed line

to benchmark the performance of the Sigma-Delta with ideal components and without any non-linearities. Latter, some limitations were integrated in components to simulate some non-idealities, such amplifier finite gain and finite slew-rate.

Before reaching the final design, represented in Fig. 4.5, several simulations, with first- second- and third-order converter and MASH topologies, were made. A table with calculated and simulated values is present in appendix C to demonstrate the theoretical values and to give support to the taken decisions.

MASH Converters can have a better SNR than the others, but, because of the use of more amplifiers and a more complex digital logic, the power consumption is always higher, which goes against one of the motivations to this dissertation – low-power consumption.

First-order converters are simpler, but, since the noise shaping is only of first-order, it is complicated to achieve a high SNR.

Third-order converters have an ideal SNR larger than second order implementations, but, because of the stability problems, the integrators need to be attenuated and the final SNR is significantly lower than the ideal. Since this topology needs one more amplifier than a second-order ΣΔ Modulator, the small benefits of resolution gain does not compensate the higher power consumption.

With the 2nd-order converter selected, some limitations were used to obtain more a realistic SNR and amplifiers voltage output. After the introduction of these limitations, the goal was to

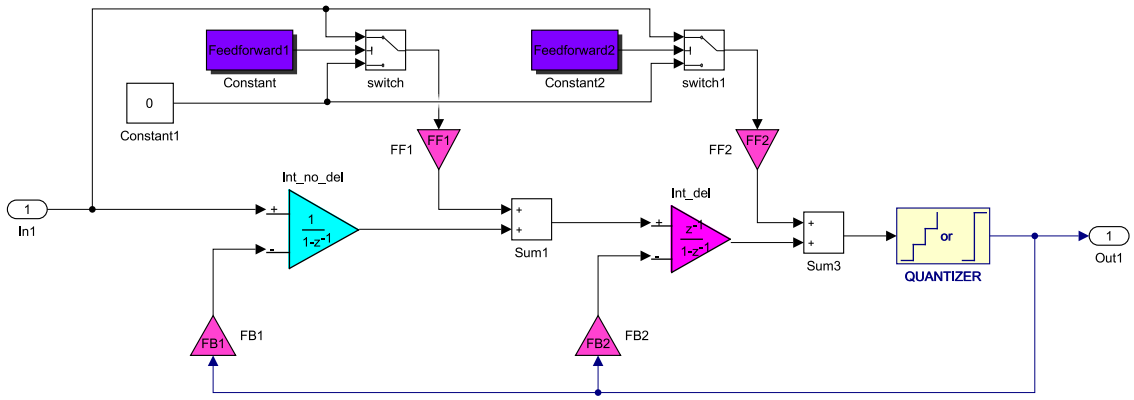


Figure 4.5: Simulink model diagram of the 2nd-order Converter

increase the theoretical SNR without increasing the power consumption and ensure that the amplifiers output are lower than the maximum swing of their output stage.

One important design decision to make over about the different blocks, such as the ADC or a DAC, is the number of bits. A ΣΔ Modulator is not a Nyquist ADC, but it needs one to convert analog signals into digital domain and a DAC to do the opposite, to close the loop. As seen in previous chapters, Nyquist ADCs and DACs suffer from effects such as INL and DNL, and the more bits it has, the greater these limitations are. In a ΣΔ Converter, these issues are more important in the DAC, because it is in the feedback path and its defects will not be filtered by the noise filter, so it is important to select a very linear DAC, and to do a careful design of this block. Since 1 bit ADC and DAC are inherently linear (i.e. do not have INL or DNL), they are a good option to design a high-resolution ΣΔ, like the converters reported in [8]. But if the sampling rate and filter-loop order are limited to decrease the power consumption, it is difficult to obtain a very-high-resolution circuit. When 2 bit ADC and DAC are used, the SNR increases, but the system will be more sensitive to mismatches, mainly at the DAC, which will impose non-linearities. To solve these issues, techniques such as Dynamic Element Matching (DEM) [34], where Data-weighted Averaging (DWA) [35] is one possible algorithm, can be used. This method transforms DAC errors into uncorrelated noise (e.g. white noise or shaped noise), in order to decrease its influence on the output signal. This technique is digital and will add more power consumption and complexity to the final system, but improves the SNR of the converter and it is good to have in quantizers with two or more bits. At last, an alternative to 1 or 2 bit resolution quantizers is a quantizer with a resolution of 1.5 bit (Fig. 4.6). With such quantizer, it is possible to obtain a high resolution even without a DEM block, or if needed, it is much simpler, since the complexity of these techniques increase with the number of quantizing levels.

In order get the theoretical SNR of more than 120 dB (i.e. a resolution of 20 bit) with a 1.5 bit quantizer and a second-order noise shaping filter, an OSR of 512 is needed. A larger OSR would give a better SNR, but at the same time, it consumes more power and needs amplifiers with larger gain-bandwidth products [2], which in turn needs a faster clock frequency, which is more difficult to design.

In real systems, the slew-rate and amplifier intrinsic gain are two important factors that constrains the SNR. To understand the effect and what are the best values, a sweep was done to obtain the SNR for a range of gain and slew-rate values. In Fig. 4.7 is observable that a gain higher than 70 dB will not increase the SNR, so this is the selected gain to reach when designing the amplifiers. Latter on, since the Sigma-Delta system will have more non-idealities, like thermal-noise from switches, the effective SNR will be lower. This means that the requirements on the amplifier can be reduced. Fig. 4.8 demonstrates that a slew-rate of 5 V/µs for the first amplifier and of 6 V/µs for the second are sufficient to obtain the best SNR possible.

Since the output of the integrators is larger than desired (see Fig. 4.9a), the feed-forward technique was employed to decrease it. This technique was used without limiting the input signal and the reference (Fig. 4.9b), but simulations show that the output voltage swing of the second integrator is higher than the supply voltage, so the reference voltage and maximum input signal

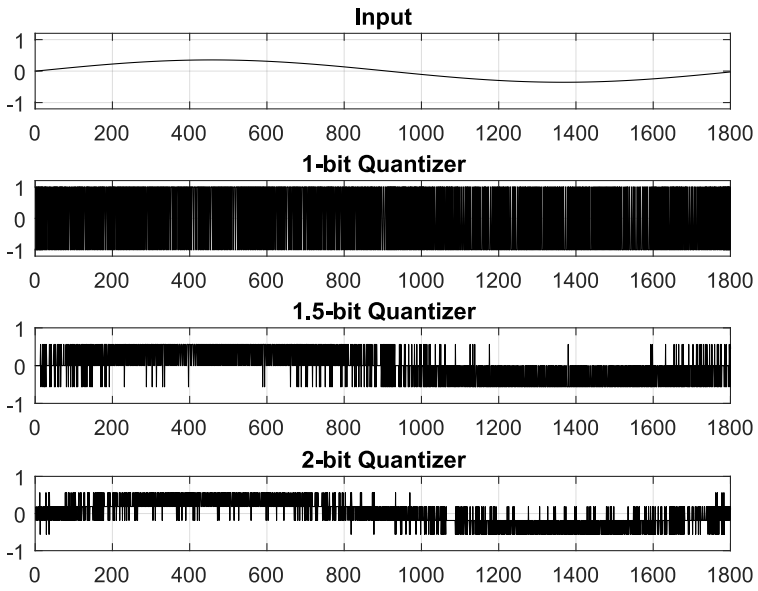


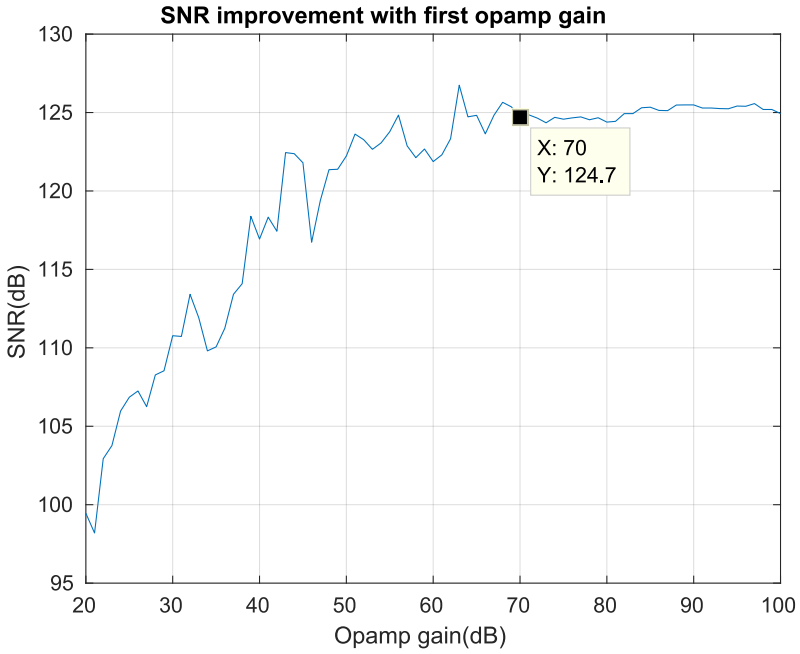
Figure 4.6: Output of a ΣΔ Modulator with quantizers of 1 bit, 1.5 bit and 2 bit

were lowered to obtain the desirable result (Fig. 4.9c).

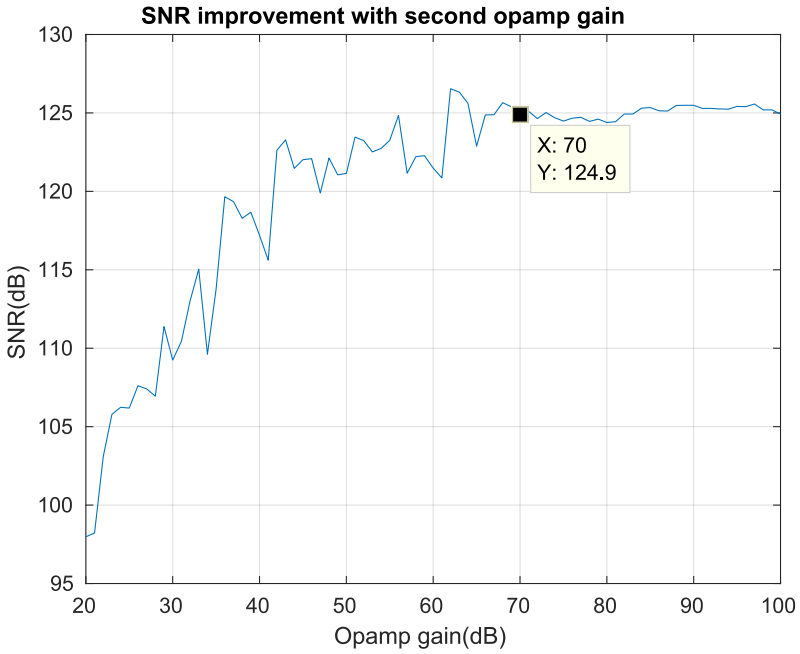
Using a reference signal with 5 dB below the maximum acceptable output swing of the amplifiers and an input signal of 4 dB below the reference voltage is enough to guarantee the stability and a voltage swing under the maximum permitted.

With all selections made, the most important indicator of a Sigma-Delta, the SNR, can be obtained. To do that, the selected input signal frequency was set to 562.5 Hz, that is near to middle frequency of the chosen bandwidth, and, at the same time, is a co-prime number of the sampling frequency. This avoids the concentration of noise on harmonics (a typical case when the noise pattern repeats itself), and be more "white". This is more critical for Nyquist rate converters, where there is no "dynamics", but still a good practice in ΣΔ FFT analysis. The final result is a SNR of 126.9 dB and can be confirmed in Fig. 4.10.

The power density spectrum of the converter output signal is represented by Fig. 4.11. It is possible to observe that the PSD of the output signal has a tone near to 1.688 kHz, that is the third harmonic of input signal, but it is outside of the band-of-interest, so it will be removed by the decimator filter. Fig. 4.9c represents the voltage occurrences at the integrators output. Since the feed-forward technique is used, the more probable values are near to zero and the absolute maximum is below the maximum specified for the integrators output.

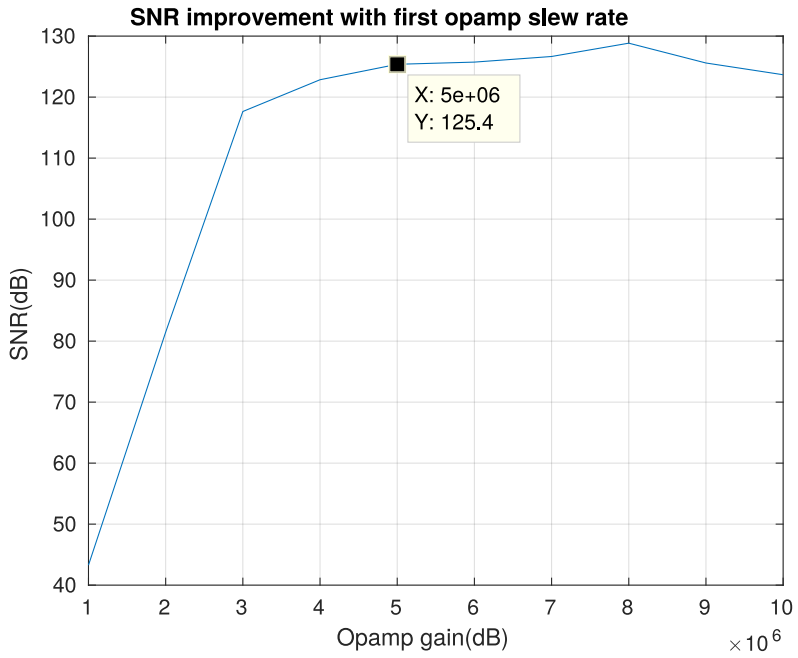


(a) First amplifier

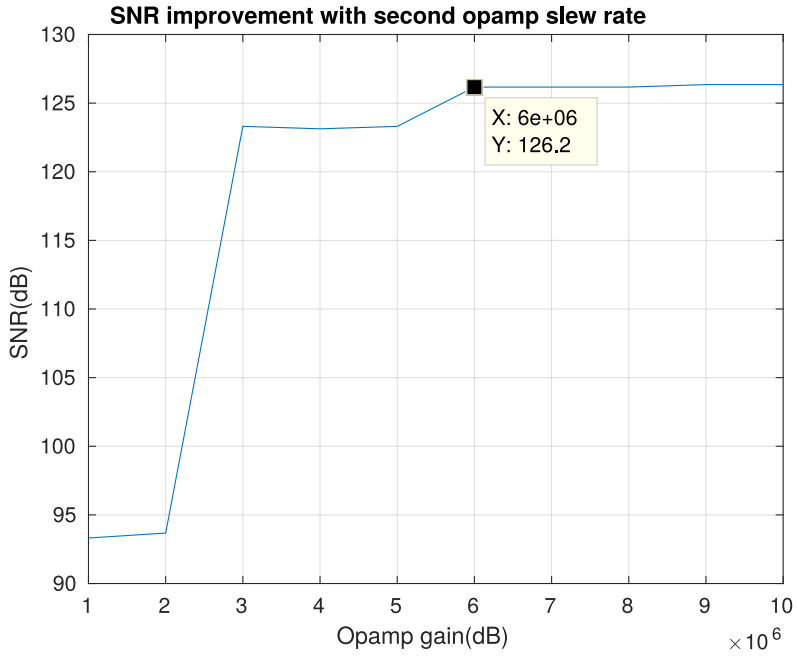


(b) Second amplifier

Figure 4.7: Converter SNR enhancement with amplifiers gain

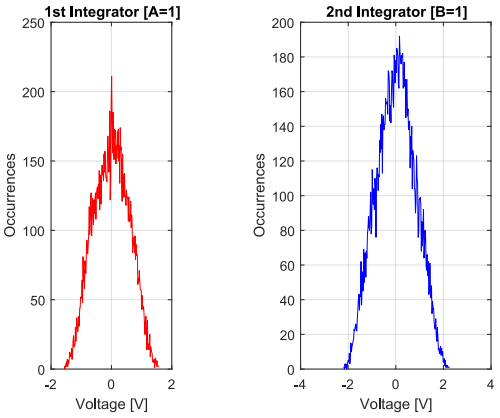


(a) First amplifier

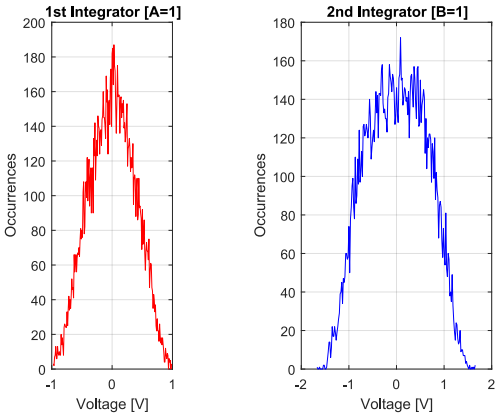


(b) Second amplifier

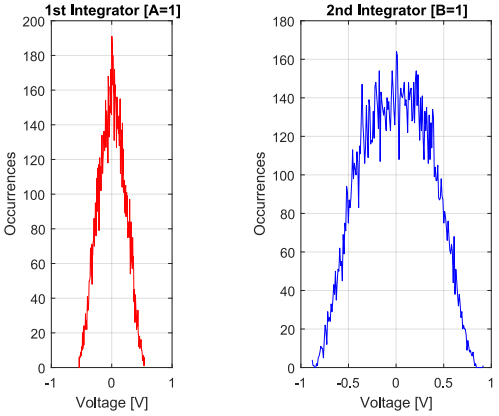
Figure 4.8: Converter SNR enhancement with amplifiers slew-rate



(a) Without feed-forward neighter reduced reference



(b) With feed-forward



(c) With feed-forward and reduced voltage reference

Figure 4.9: Output voltage of amplifiers

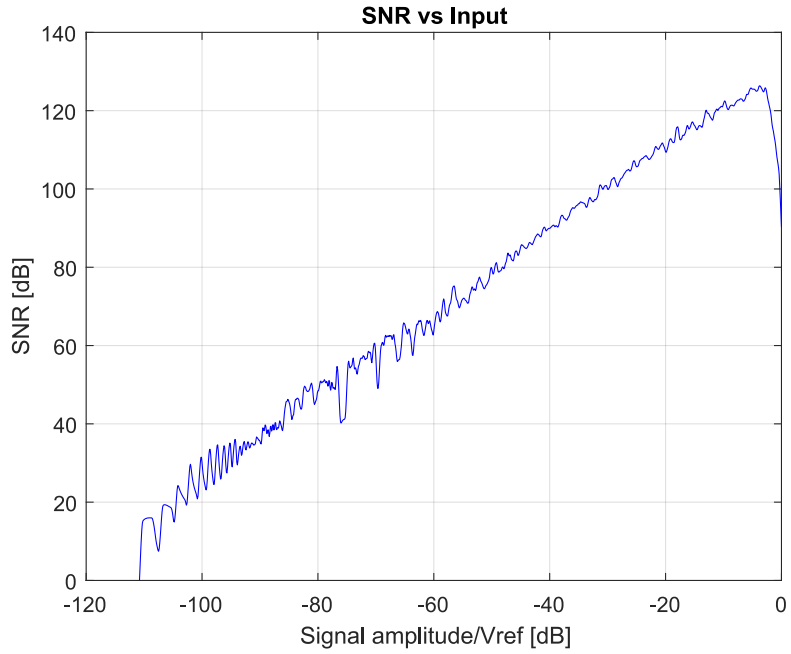


Figure 4.10: Simulation of SNR versus Input Amplitude

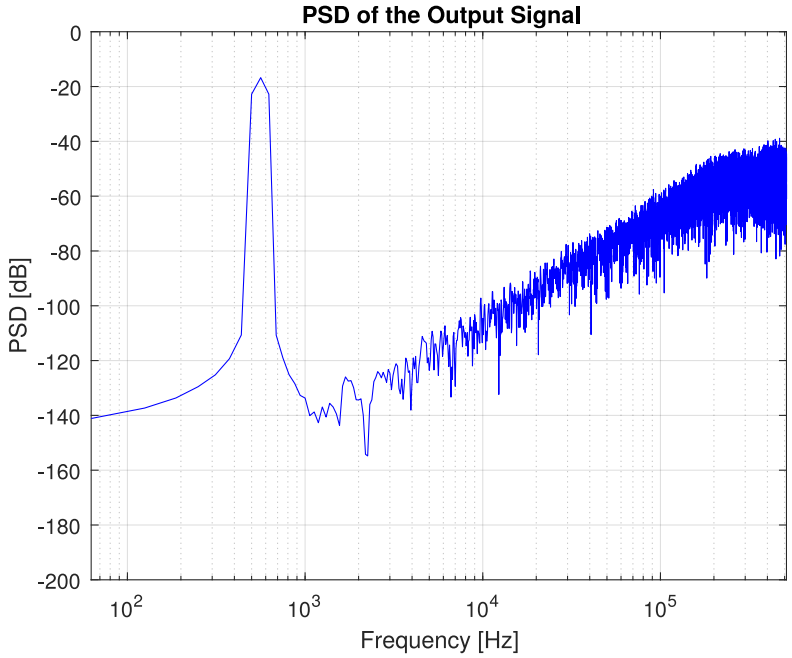


Figure 4.11: Matlab simulation of power density spectrum of Output Signal

Chapter 5

Circuit Implementation

This chapter describes the circuit level implementation of the proposed converter. This part of the dissertation was conducted with the help of Cadence IC-Design Tools.

5.1 Sampling Circuit

A discrete circuit requires sampled input signals. Normally, the sampling of inputs is done with a standalone S&H, but when a switched-capacitor (switch-cap) circuit is used, the S&H is not needed because sampling is inherent in switch-cap circuits.

Using the simple switch-cap circuit represented in Fig. 5.1, it is possible to verify that the continuous input voltage is applied to the sampling capacitor only when the switches S_1 and S_3 are *on*. With these switches *off*, the sampling voltage is hold and can be transferred to the next circuit through switch S_4, with S_2 closed to give the needed reference.

The switches are implemented with MOSFETs operating in *triode region*. When a MOSFET is used for this purpose, there are several non-ideal aspects to take into account, being the clock feed-through one of the most relevant and that will be explained further down.

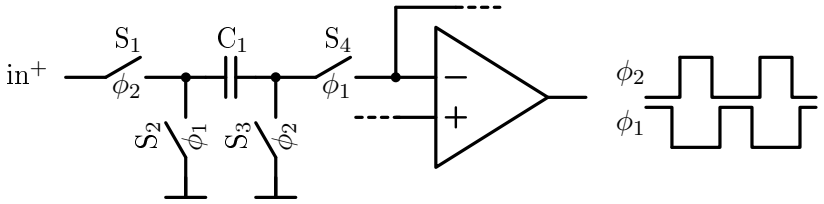


Figure 5.1: Sample and Hold Circuit

Other important factors to be considered are the leakage current and the parasitic capacitance of the transistors. The circuit shown in Fig. 5.1 is designed to be parasitic-insensitive [1]. To resolve the leakage problem, clock phases ϕ_1 and ϕ_2 have to be non-overlapping, as shown in the figure, preventing these leakage currents to discharge the capacitor, resulting in a charge transfer error.

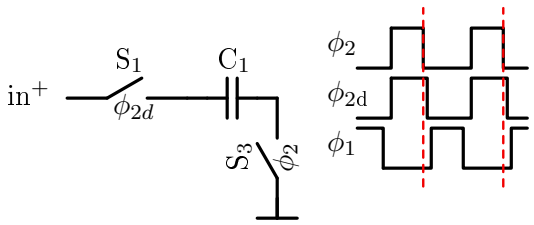


Figure 5.2: Bottom plate sampling implementation

5.1.1 Clock Feed-through Compensation

Clock feed-through is an important effect that occurs in a MOSFET when it switches from *on* to *off*. This effect results when part of the channel charge goes to the sampling capacitance. Since this charge injection is not negligible and non-linearly dependent of input the signal, it will modify, in a non-linear way, the signal stored in the sampling capacitor, decreasing the effective SNR [1].

There are several techniques to compensate the clock feed-through effect, one of them is the bottom-plate sampling [2] (Fig. 5.2). This technique ensures a constant charge injection on every clock cycle (i.e. makes it a predictable effect), giving rise to an equally constant offset. Taking Fig. 5.2 for reference, the idea is to avoid the influence of charge coming from S_1 channel on C_1, because it is input dependent. This is accomplished by making sure that S_3 opens primarily to S_1, by adding a small delay to S_1 clock. When S_1 eventually opens, there will be no path to change the charge of C_1. In practice, some change will happen due to parasitics on the right side of C_1 plate, but the total charge will remain unchanged and will be integrated later, during the next clock phase. All that it remains is the charge injection from S_3, that is signal independent, and always very similar.

Because this converter is differential, an equal offset in both paths will not affect the signal at all, but as there are limitations of matching in fabrication processes, the offsets will not be equal and the reduction of this effect will not be total.

5.2 Switches

Like mentioned before, the switches are implemented as MOSFETs, more specifically, an N-type MOSFET (NMOS), because they have less *on*-resistance than P-type MOSFET (PMOS).

5.2.1 Switch Noise

An important limitation of converters is the noise, in fact almost all limitations can be modeled like noise. One main source of noise are the transistors used as switches which operation can be characterized by a *on*- and a *off*-resistance. When they are *off*, in the *cutoff region*, the equivalent resistance is very high, so it does not affect substantially the circuit, but when they are *on*, in the *triode region*, the *on*-resistance will produce noise that will alter the system response. This noise is named *thermal noise*, which occurs due to thermal excitation of charge carriers inside a conductor.

This type of noise is non-correlated, meaning that the autocorrelation function is a Dirac delta (the noise is only similar to itself), and holds a power density spectrum constant with frequency, thus coined as *white noise*. This is important to be kept true, as much as possible, for the current noise shaping to work.

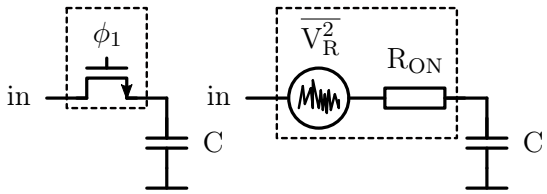


Figure 5.3: Model of switch thermal noise

5.3 Integrator

A $\Sigma\Delta$ Modulator needs integrators to perform the noise shaping filtering function. Fig. 5.4 shows the second-order switch-cap filter used in this design. It is possible to observe that the circuit is differential, but only one branch is showed, just to simplify the visual analysis. A differential design enables a better rejection of the common-mode and the use of an unipolar supply with a V_{CM} centered signal, because the information does not depend on a reference ground, with the added benefit of being able to double the maximum output swing.

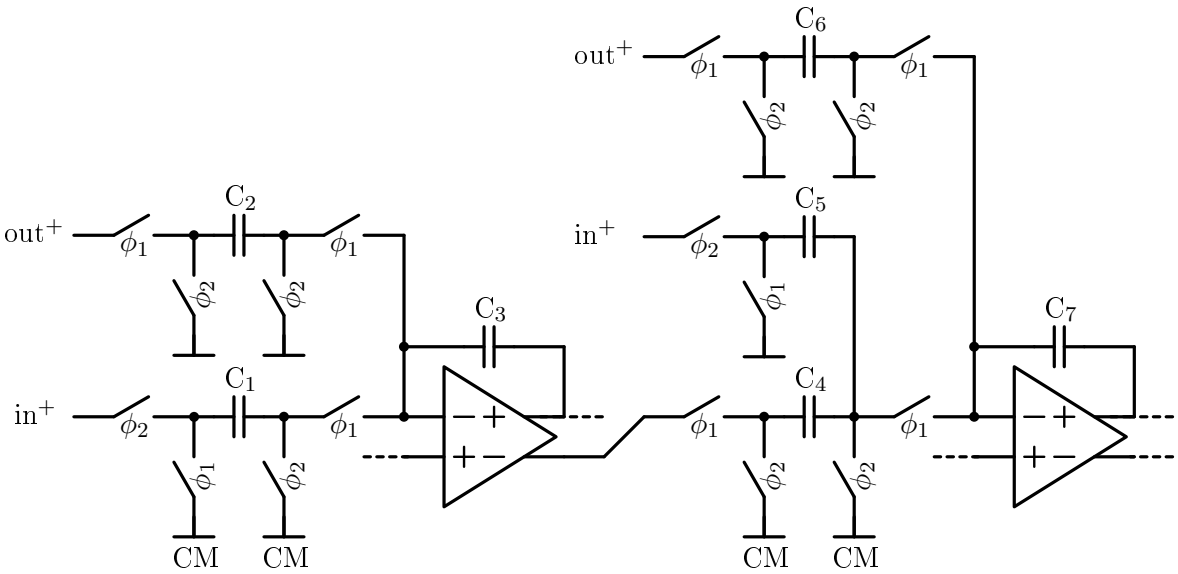


Figure 5.4: Schematic of integrators of converter

Analyzing Fig. 5.4, during phase ϕ_1 of the clock, sampling capacitors, C_1 and C_4 transfer their stored charges to the amplifier feedback capacitors, C_3 and C_7. At the same time, the first integrator output and feedback signal (out^+) are sampled by capacitors C_4 and C_6, respectively, to be added at the second integrator input. The feedback signal is also sampled in ϕ_1 by capacitor C_2.

In the next phase, ϕ_2, the input signal (in^+) is sampled using capacitor C_1 and the feed-forward signal (in^-) is sampled by C_5. An important annotation of this figure is that the first integrator outputs are swapped for design convenience (inverts the signal).

Doing a brief analysis to compare Fig. 5.4 with Fig. 4.1, at the first integrator input, the feedback signal is subtracted from the delayed input signal. Since this delay occurs before the modulator, it will not affect the transfer function. With the three capacitors equal, the integrator gain is unitary, as proposed in Chapter 4. At the second integrator input, inverted images of feedback signal and the modulator input signal (i.e. feed-forward signal) are added to the first integrator output, as described in Fig. 4.1. All the capacitors have the same value in order to achieve an unitary gain at this stage. The last sum, which is the second integrator output with the feed-forward signal, is made outside this block, at the comparators input.

Analyzing the circuits in Fig. 5.5, from a point of view of charge conservation and for each integrator, one gets for the first

$$Q_{\phi 1} = -\,fb^+\,[n-1/2]\,C_2 - out\,[n-1/2]\,C_3$$

$$Q_{\phi 2} = -\,in^+\,[n-1]\,C_1 - out\,[n-1]\,C_3 \tag{5.1}$$

Since the charge remains the same until ϕ_2, $fb^+\,[n-1/2] = fb^+\,[n]$ and $out\,[n-1/2] = out\,[n]$, so, knowing that the capacitors are equal, the first integrator transfer function is given by

$$\frac{out\,(z)}{in^+\,(z)\,z^{-1} - fb^+\,(z)} = \frac{1}{1-z^{-1}} \tag{5.2}$$

Second Integrator

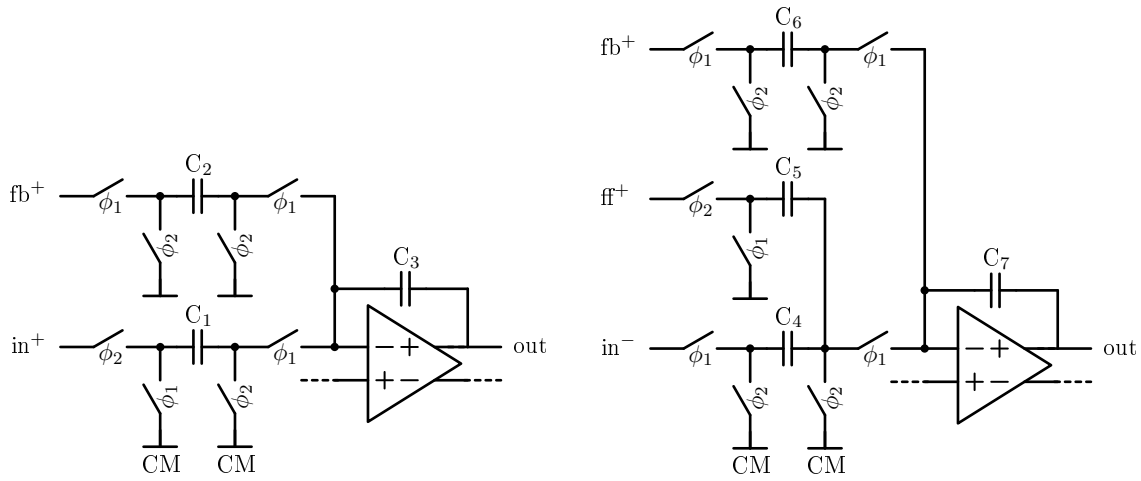
$$Q_{\phi 1} = -\,in^-\,[n-1/2]\,C_4 - fb^+\,[n-1/2]\,C_6 - out\,[n-1/2]\,C_7$$

$$Q_{\phi 2} = -\,ff^+\,[n-1]\,C_5 - out\,[n-1]\,C_7 \tag{5.3}$$

Again, the capacitors are equal; $in^-\,[n-1/2] = in^-\,[n]$, $fb^+\,[n-1/2] = fb^+\,[n]$, $out\,[n-1/2] = out\,[n]$, and $in^-\,[n] = -\,in^+\,[n]$, so the second integrator transfer function is given by:

$$\frac{out\,(z)}{in^+\,(z) + ff^+\,(z)\,z^{-1} - fb^+\,(z)} = \frac{1}{1-z^{-1}} \tag{5.4}$$

The delay, needed to stabilize the converter, which is not present neither in 5.1 neither in 5.4, is given by the quantizer block. Then the transfer functions of both integrators, together with quantizer delay, equalize the transfer function of (4.1) and not the expected (4.2), because of the input delay and the fact that the quantizer delay is after the feed-forward path, which does not detract the converter performance.



(a) First Integrator (b) Second Integrator

Figure 5.5: Schematic of each integrator of the converter

5.4 Amplifier

The design used for the amplifier, shown in Fig. 5.6 is an alternative typology to traditional ones, which can have a large gain without resource to *cascode* techniques, that would decrease the maximum output swing. With this typology, it was possible to obtain a gain up to more than 70 dB with a gain-bandwidth product of 100 MHz, that is more than necessary.

The difference of this design in relation to more traditional ones is the absence of a common-mode negative feedback on first stage, and the use of a cross-coupled pair (positive feedback), most common in comparators, together with the use of extra PMOS M_5 and M_6 that perform g_m cancellation over M_3 and M_4 in differential mode, and lowers the common-mode gain, to the point that the bias becomes stable without a common mode feedback.

The g_m cancellation is accomplished with MOSFETs M_5 and M_6. These two transistors permits the cancellation of the $-1/g_m$ factor from M_3 and M_4, getting an equivalent resistance of (5.5).

Consider the following analysis based on Fig. 5.7a, which is a simplified representation of the first stage, just for one branch of the differential pair.
The equivalent resistances for this stage are obtained as:

$$R_{eq1} = r_{o3,4} \parallel -\frac{1}{g_{m3,4}} \parallel r_{o5,6} \parallel \frac{1}{g_{m5,6}} \approx \frac{r_{o3,4}}{2} \tag{5.5}$$

and

$$R_{eq2} = r_{o1,2} \tag{5.6}$$

The approximation in (5.5) is made knowing that $r_{o3,4} \approx r_{o5,6}$ and that $g_{m3,4} \approx g_{m5,6}$, which results in a resistance with half the value of r_{o3} in parallel with an infinite resistance. Note that $1/g_{m5,6}$

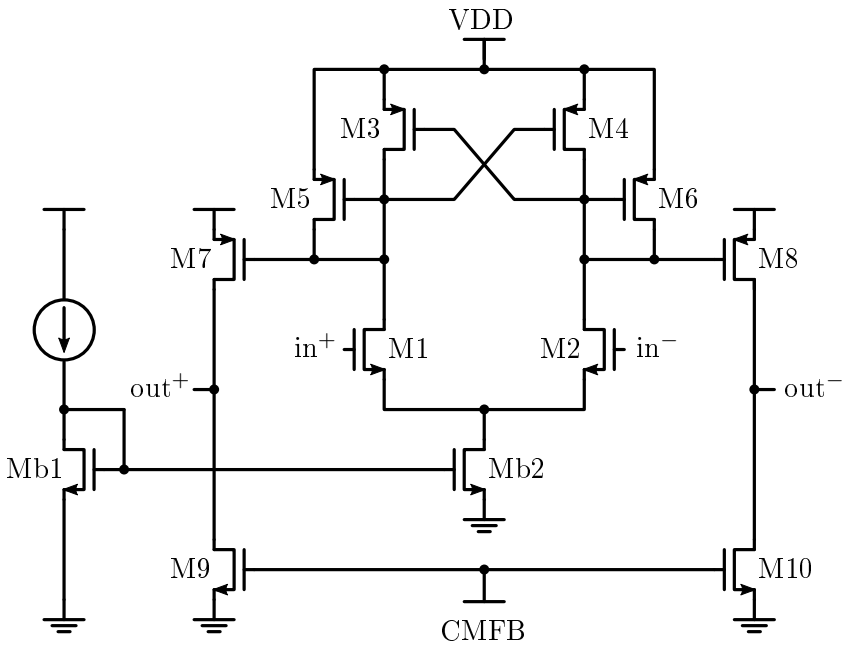


Figure 5.6: Amplifier circuit without CMFB circuit

can be made slightly smaller than $1/g_{m3,4}$ to grant a final positive resistance, although at the cost of decreasing the total equivalent resistance. Nevertheless, current starvation on the load could improve this loss [36]. So, the first stage differential gain is

$$A_{v1} = -g_{m1,2}\left(r_{o1,2} \parallel \frac{r_{o3,4}}{2}\right) \tag{5.7}$$

the second stage gain is

$$A_{v2} = -g_{m7,8}\left(r_{o7,8} \parallel r_{o9,10}\right) \tag{5.8}$$

and the final differential gain

$$A_v = A_{v1} \times A_{v2} = g_{m1,2}g_{m7,8}\left(r_{o1,2} \parallel \frac{r_{o3,4}}{2}\right)\left(r_{o7,8} \parallel r_{o9,10}\right) \tag{5.9}$$

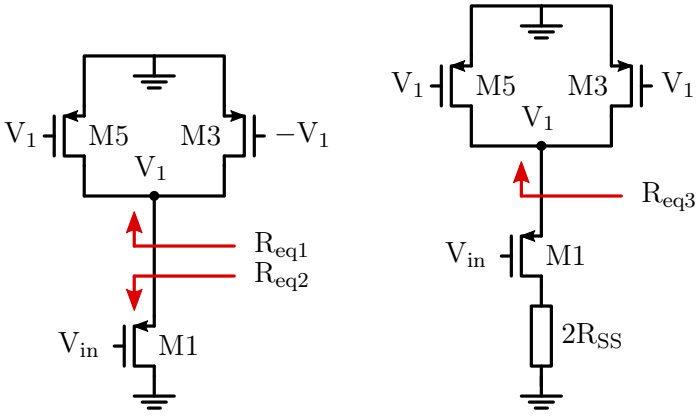
The common-mode gain of the first stage (Fig. 5.7b) can be calculated realizing that the gate voltages of transistors M_3 and M_4 are both the same sign in common mode, so the $1/g_m$ factor is predominant.

$$R_{eq3} = r_{o3,4} \parallel \frac{1}{g_{m3,4}} \parallel r_{o5,6} \parallel \frac{1}{g_{m5,6}} \approx \frac{1}{2}\frac{1}{g_{m3,4}} \tag{5.10}$$

Neglecting $r_{o1,2}$, the first stage common-mode gain is given by

$$A_{CM} = -\frac{R_{eq3}}{\dfrac{1}{g_{m1,2}} + 2R_{SS}} \approx -\frac{R_{eq3}}{2R_{SS}} = -\frac{\dfrac{1}{g_{m3,4}}}{4R_{SS}} \tag{5.11}$$

Since $R_{SS} \gg {}^{1}/_{g_{m3}}$, the common-mode gain will be very low, for a good common-mode rejection ration (CMRR).



(a) High load for differential gain and (b) Low load for common-mode gain cancellation of $-{}^{1}/_{g_m}$ factor

Figure 5.7: Benefits of the amplifier typology – left branch view

A Miller compensation, using a series of capacitor and resistor between output of first and second stage, was used to increase the phase-margin (PM) up to 70° with a load of 2 pF (Fig. 5.8), ensuring that the amplifier has a stable output. The gain-bandwidth product declined to 69 MHz, but remained greater than the necessary for this application.

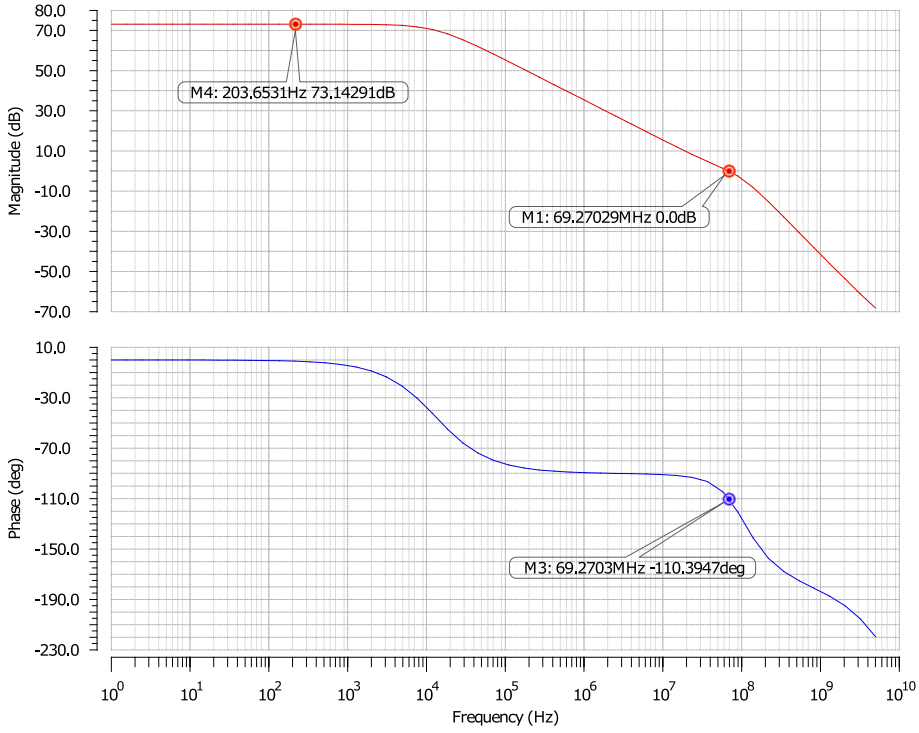


Figure 5.8: Amplifier magnitude and phase (Differential gain)

5.4.1 Common-mode Feedback

A common-mode feedback circuit (CMFB) is crucial in a differential amplifier, since it does not have a ground reference to set the common mode voltage, furthermore, the respective gain needs to be small. This is the case for the output (second) stage of the amplifier. The output circuit itself is set to a rail-to-rail topology, which is fundamental to keep a large output dynamic range. The rail-to-rail output characteristic is shown in Fig. 5.9, where the unipolar input is represented in red and the differential outputs are represented in blue and green. As it can be verified, the outputs are approximately linear up to 1.19 V and down to 11 mV when the input is 1.2 V, which is the supply voltage.

Since this converter is a discrete-time switch-cap, the selected CMFB for the output also employees switch-cap technology. The circuit in Fig. 5.10 was the selected from [37], because it can be used at any phase of clock. The right side of circuit operate on the opposite clock phase of the left side, and, in this way, the bias voltage for transistors M_9 and M_{10} is always ready to impose the correct output common-mode value.

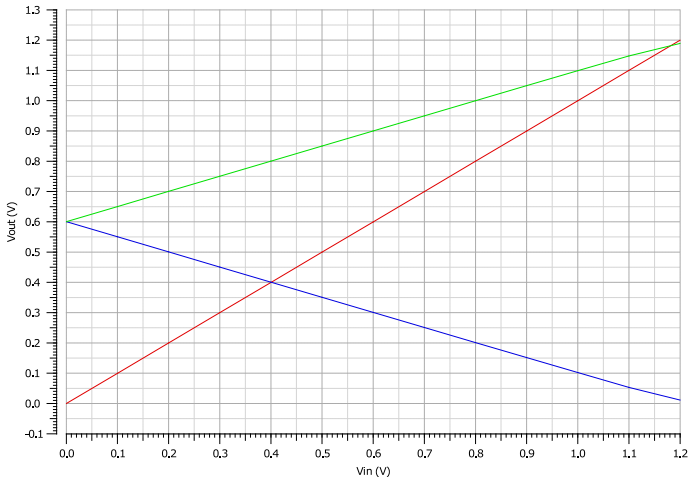


Figure 5.9: Rail-to-rail output swing of second stage of the amplifier

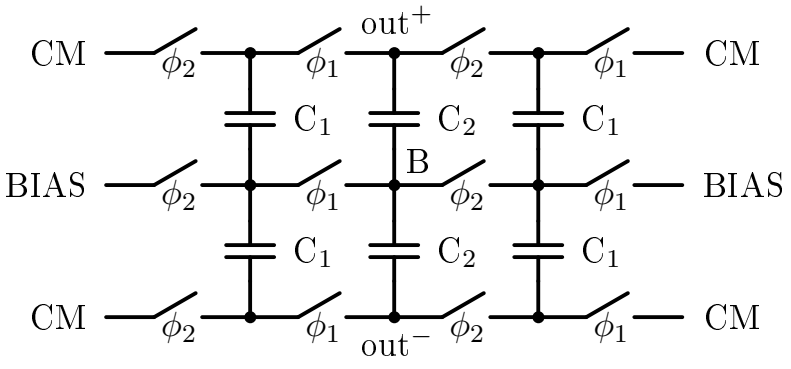


Figure 5.10: Common-mode feedback Circuit

The CM nodes of this block are linked to the common-mode voltage of the main circuit, the out^+ and out^- to the related outputs of the amplifier, the BIAS nodes to a reference voltage that is near to the voltage required to bias transistors M_9 and M_{10} and, finally, the B node is connected to the gates of these transistors. This CMFB circuit senses the difference of potential between the common-mode output value (5.12) and the CM nodes, and manages, through feedback, to decrease this difference by varying the bias voltage of M_9 and M_{10} around the BIAS value.

$$\frac{out^+ + out^-}{2} \tag{5.12}$$

5.5 1.5 bit Quantizer

The selected quantizer has a resolution of 1.5 bit because of the good compromise it offers. The linearity characteristic is little affected in relation to a 1 bit quantizer, and the final SNR is almost as much as that obtained with a quantizer of 2 bit resolution. To implement this quantizer, two reference voltages and two comparators are needed, as shown in Fig. 5.11. The quantizer output is given by Table 5.1.

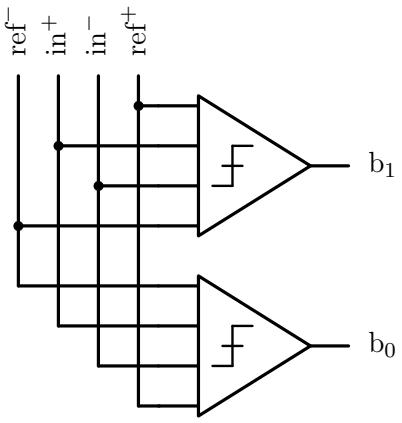


Figure 5.11: Quantizer Circuit

input value	output b_1	output b_0
$< ref^-$	0	0
$[ref^-, ref^-]$	0	1
$> ref^+$	1	1

Table 5.1: Quantizer output

5.5.1 Comparator

The two comparator blocks of the quantizer do the comparison between the input voltage and pre-defined reference voltages, producing digital bits as outputs. Since this implementation is a 1.5 bit quantizer, an encoder to feed the DAC is not necessary. The comparator (Fig. 5.12) is constituted by a switch-cap circuit that calculates the correct input value to be used in the comparator latch, followed by the comparator latch that does the comparison itself, a signal restorer buffer and a D-Latch. The inputs of the switch-cap circuit corresponds to the main branch of the modulator (i.e. the second integrator output), the references and also the second feed-forward branch, which needs to be added here.

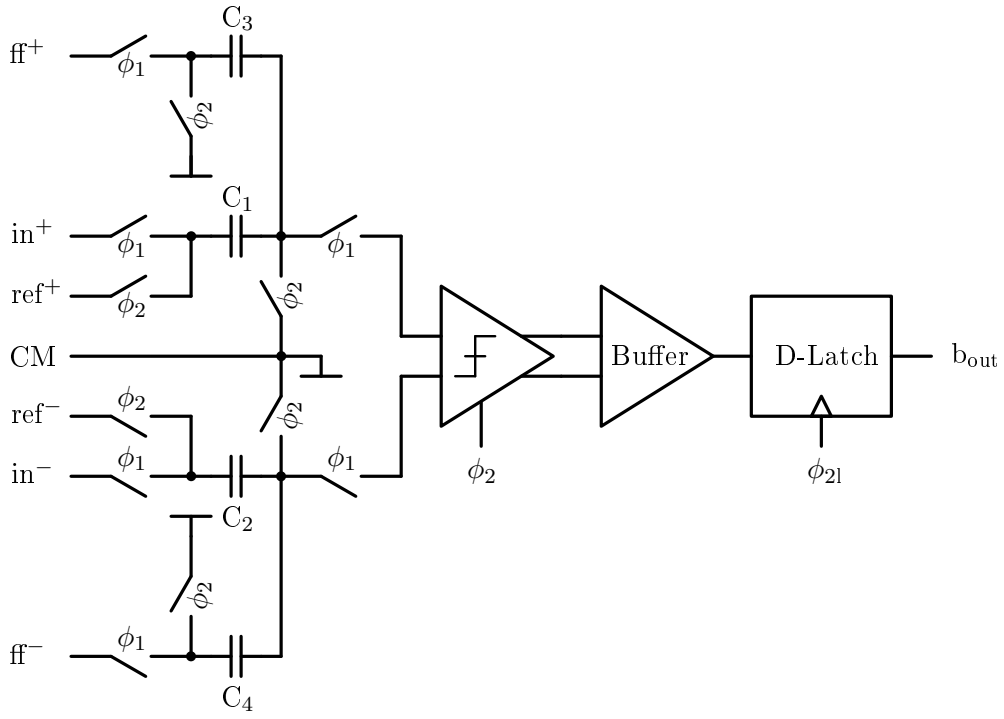


Figure 5.12: All blocks used to do the comparation

Analyzing Fig. 5.12, in phase ϕ_2 capacitors C_1 and C_2 are pre-charged to the reference voltages. In ϕ_1, C_1 and C_2 acquire the difference between input and reference and C_3 and C_4 will add the feed-forward voltages, so the input of comparator latch is given by

$$\text{in}_{\text{latch}} = \text{in} - \text{ref} + \text{ff} \tag{5.13}$$

The latch clock, ϕ_{2l} is shorter than ϕ_2 in order to allow the latch to hold the value before the comparator latch changes to the reset phase, which will be explained below.

Since the comparator latch is dynamic, the output value will be always V_{DD} at $\overline{\phi_2}$ and will give the useful result at ϕ_2. The buffer will balance the comparator latch load, since the D-Latch changes its input impedance with the clock phases. The D-Latch will keep the result for a full clock cycle to be used by the DAC.

As stated earlier, the comparator latch used in this design (Fig. 5.13) is a dynamic latch, commonly referred as StrongARM Latch, and was proposed by Razavi [38]. Since it is dynamic, it has two main phases, *reset* and *tracking*. With the *clk* signal down, both outputs are reset to V_{DD} by M_7 and M_8. During the next phase, with *clk* at high, the two inputs are compared and the outputs, out^+ and out^-, will go to V_{DD} or GND, in opposite phases of each other and in response to the polarity of $\left(\text{in}^+ - \text{in}^-\right)$.

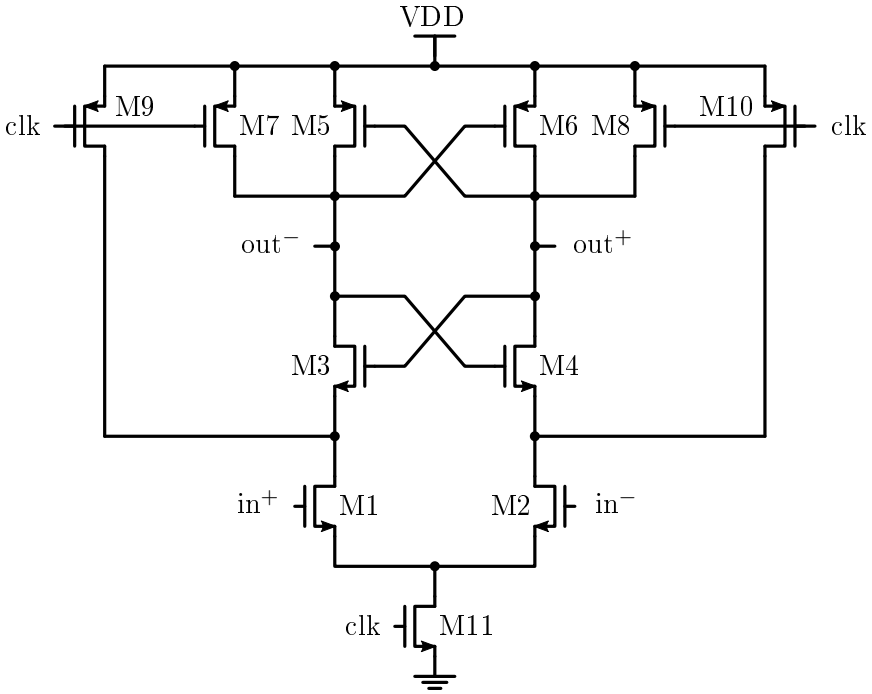


Figure 5.13: Comparator Latch Circuit

5.5.2 Buffer

A buffer is placed in front of the StrongARM latch in order to keep its output-load balanced. The buffer represented in Fig. 5.14 is a self-biasing differential input amplifier [39] and is designed with two main inverters and a third one that enables better voltage levels.

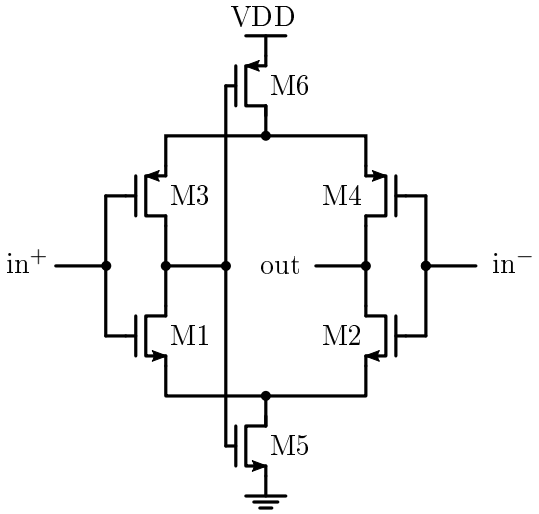


Figure 5.14: Buffer Circuit

5.5.3 D-Latch

The D-latch is a necessary block to keep the value equal until the end of the clock cycle, in order to feed the DAC correctly. The D-latch is static and is represented in Fig. 5.15. It uses two connected inverters, forming a positive feedback loop, so the output value have always the same logical value and it is automatically restored to V_{DD} voltage or GND. The M_2 switch is used to set the positive feedback and M_1 is used to make the latch transparent (i.e. put at output node the input signal, restored). In a brief description, with the *clk* signal up, the latch will follow the input signal, when *clk* signal goes down the latch will hold the previous value until *clk* goes up again.

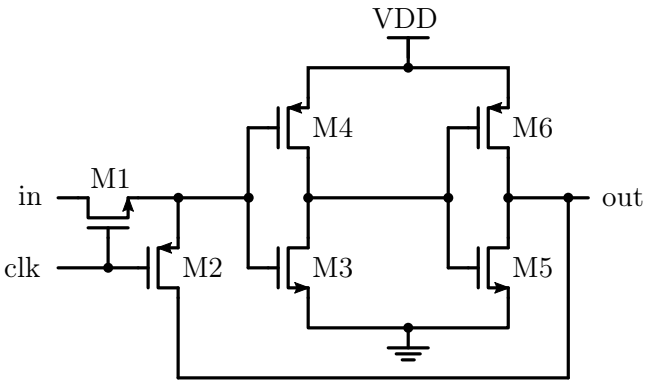


Figure 5.15: D-latch Circuit

5.6 DAC

The DAC used in this design, which closes the feedback loop of the Sigma-Delta Modulator, is a capacitor differential DAC. Since the quantizer has 1.5 bit, with outputs defined by Table 5.1, the DAC has to have two capacitors in order to get the right value at the output. These capacitors have half of the size of the amplifiers feedback capacitors in both integrators. In fact, this DAC reuses the amplifiers of the integrators (see full A/D in Fig. 5.22), so the evaluated value is directly added to the integrator path, with several advantages, such as it consumes less power and removes components (e.g. the amplifier itself and is common-mode feedback circuit) that would cause common-mode problems and lower the effective SNR.

Each capacitor is connected to ref^+ and ref^- through a switch, in order to obtain the correct value for summation. They are also connected to the common-mode voltage to do the evaluation of the analog output at phase ϕ_2. At ϕ_1, capacitors C_1 to C_4 are charged to the right reference, corresponding to the current binary sample. Clock signals ϕ_3 to ϕ_6 were created to control the charging process of these capacitors, according to a binary logic circuit controlled by the ADC bits, as shown in Fig. 5.17 and its output in Table 5.2. It ensures that only the positive or the negative reference are connected to each capacitor, and only in phase ϕ_2.

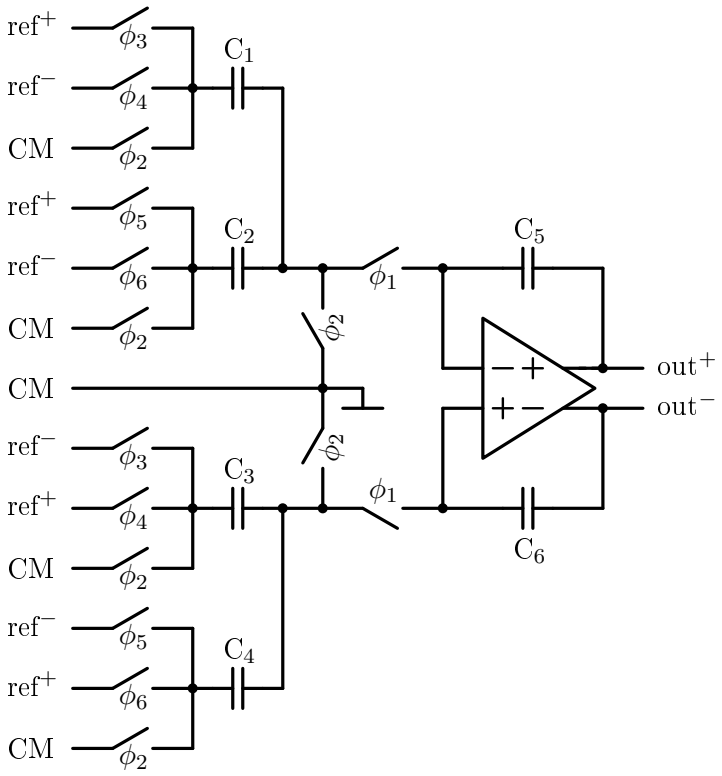


Figure 5.16: DAC Circuit

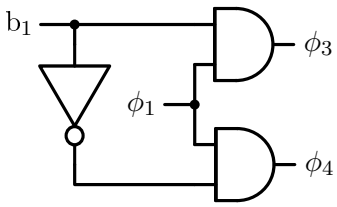


Figure 5.17: Clocks logic for DAC

ϕ_1	b_1	$\overline{b_1}$	ϕ_3	ϕ_4
0	0	1	0	0
0	1	0	0	0
1	0	1	0	1
1	1	0	1	0

Table 5.2: Clocks logic output

5.7 Converter

Fig. 5.21 shows the complete converter schematic. This circuit performs the transfer function defined in equation (4.1), as shown in section 5.3. The converter was designed to be fully-differential with a 1.2 V supply source and a 0.6 V common-mode voltage, in order to maximize the voltage swing.

The input $^1/_f$ noise and offset of the integrators have a large influence in the system. In order to diminish their effect, the technique Correlated double sampling (CDS), which is a type of a more general Autozero (AZ) technique [40], was used with the schematic shown in Fig. 5.18.

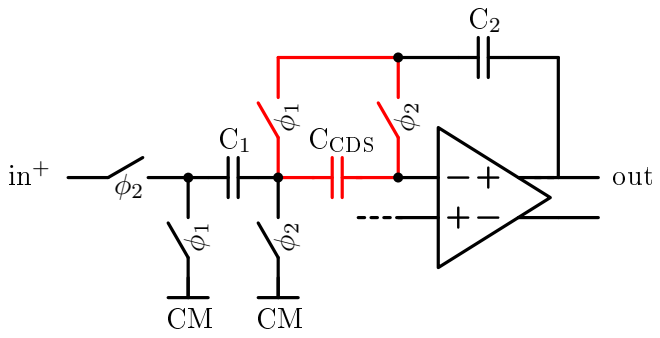


Figure 5.18: Implementation of Correlated Double Sampling

With this technique, the input noise is sampled at ϕ_2 and then subtracted from the instantaneous value of the contaminated signal at ϕ_1, decreasing its influence at the modulator output. Thus, the CDS implementation used in this design aims to minimize errors due to offset voltages and flicker-noise. If the present noise is a *dc* offset, it will be canceled, if it is flicker noise (same as $^1/_f$ noise), it will be high-pass filtered. It adds few components, that is an advantage over others CDS techniques, because every component adds noise. Another advantage of this technique is that it is possible to implement on non-inverting as well as on inverting integrators. This is the case for the first integrador of the $\Sigma\Delta$, which has, simultaneously, and inverting and non-inverting operation.

After the introduction of the CDS technique and of the DACs, the final converter diagram is present by Fig. 5.22. In this figure, numbers 1 and 2 are the DACs for the first and second integrator, respectively. Number 3 is the feed-forward branch for the second integrator input. Number 4 is the feed-forward branch that will be added at ADC input, like explained at Section 5.5.1. The last block, number 5, is the clock logic for the DAC, mentioned in Section 5.6.

5.8 Cadence Simulation Results

The transistor-level circuit was implemented with a 130 nm technology and its design was done with Cadence tools. To obtain the resultant SNR, the input signal frequency, amplitude and voltage reference were matched with previous Matlab simulations. The simulation time has been selected according to number of samples used in Matlab, that are 16484 samples, where the 100 firsts are for the transient time and discarded for the calculation proposes. Latter on, the SNR is obtained with a Matlab script (B.1).

5.8.1 Noise in transient analysis

To have a better simulation of the circuit, noise has to be injected. The Cadence software has an option to inject noise in transient analysis, being able to simulate several noise effects, in particular the thermal noise of the switches (Section 5.2.1). To perform the analysis, the selected Noise Fmax was set to 16 MHz that is large enough to cover the noise folding.

5.8.2 Ideal Components

During Cadence simulations, some elements were considered ideal. These are: reference current bias of the amplifiers, clock sources, signal source and references generator. The clock signals pass through a low-pass filter to approximate better the reality.

5.8.3 Power Consumption

As was pointed out at the beginning of this work, a minimal power consumption is very important for portable systems. All the blocks were tested and their power consumption are shown in Table 5.3.

Table 5.3: Power consumption of all blocks of converter

Block	Power Consumption
First Amplifier	582.4 µW
Second Amplifier	568.5 µW
Quantizer	760.4 nW
Comparators	411.0 nW
Buffers	50.98 nW
Latches	181.0 nW
DAC	5.932 µW
Total[a]	1.158 mW

[a] Total power consumption contemplates all consuming parts, including switch-cap circuits, which are not mentioned isolated in table.

Looking into the table, the most power hungry blocks, as expected, are the amplifiers. Together, they take 99% of the total power, however, it should be possible to reduce. As seen in Fig. 5.8, their gain-bandwidth product is about 70 MHz, that is much larger than the necessary. If these amplifiers were designed to have a 5 MHz gain-bandwidth product, their power consumption can potentially decrease five times, reducing the total power consumption to about 230 µW. This as an optimization procedure that needs to be accomplished.

5.8.4 Performance Results

The PSD of the transistor-level implementation, for an input frequency of 562.5 hertz and 4 dB below the reference, is presented in Fig. (5.19). The measured band is of 1 kHz and the OSR is 512. The obtained SNR for these conditions is 87.5 dB.

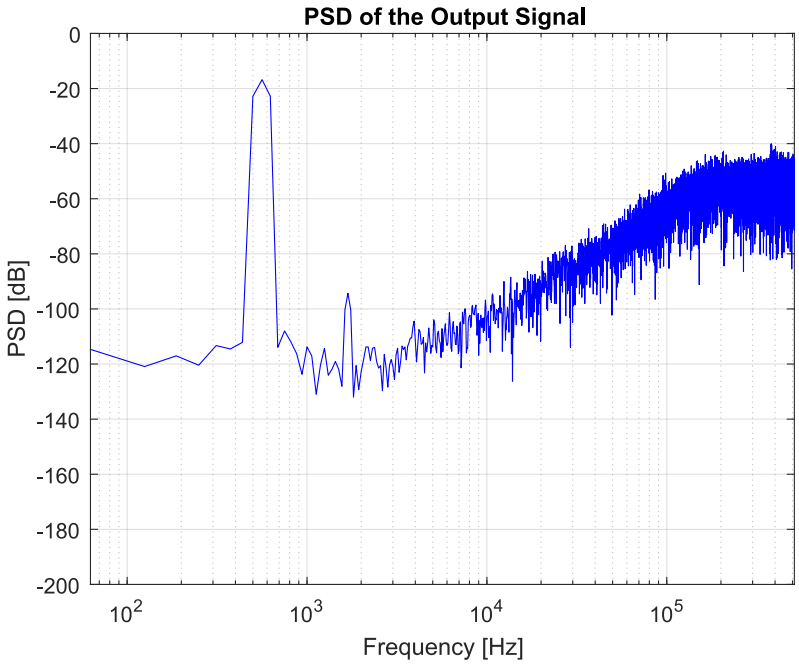


Figure 5.19: Matlab simulation of power density spectrum of Output Signal using Cadence data

As can be observed, there is a tone around the frequency 1.688 kHz (third harmonic of input signal), as in the previous Matlab simulation (Fig. 4.11), but it is not a problem, because it is outside the band-of-interest and it will be filtered by the decimator digital filter.

An important characteristic to study is the measurement of the SNR along several amplitudes of the input signal. This characteristic is represented in Fig. 5.20. As expected, the SNR drops when the input signal is large, mainly because the quantizer error starts getting too high and the noise shaping filter cannot handle it. This figure also indicates the dynamic range of this converter, which is about 87 dB.

A last result, the corners analysis, is very important because it indicates the behavior of the converter with variations of fabrication process. This analysis is performed with four corners, where four different combinations with fast (F) and slow (S) MOSFET transistors are analyzed. The MOSFET can be faster or slower than typical due to several mismatches, such as different height of C_{ox} or different percentages of doping of silicon. This analysis gives the SNR at the four possible limits, defined by the manufacturers. The results of the corners analysis are presented in Table 5.4. As can be noted, the converter is relatively robust to serious mismatches at fabrication process. But the corner with fast NMOS and slow PMOS has a better value than the result with typical MOSFETs, conversely the worst case scenario is with slow/slow, which demonstrates that some components of the converter need to be better designed.

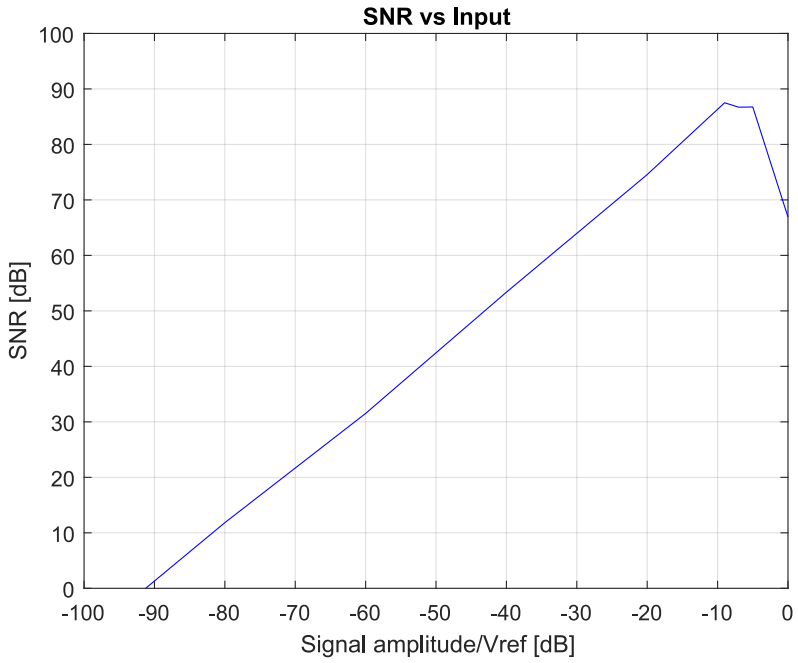


Figure 5.20: Matlab simulation of SNR along several amplitudes of the input signal using Cadence data

Table 5.4: Corners Analysis

		NMOS	
		F	S
PMOS	F	84.9 dB	83.3 dB
	S	88.3 dB	80.6 dB

As expected, the thermal noise of the transistors is a big factor to the limitation of performance. Since the Cadence simulation includes the thermal noise and other limitations, such as real clocks, its results are lower than in Matlab simulations. The overall results are presented and compared with some state-of-art converters in Table 5.5. Although this is not a fair comparison, since the results are not silicon proofed nor from post-layout simulations, it gives an indicator of where the design stands.

The figure-of-merit of this work can be reduced to at least 4 pJ or more with the reduction of amplifiers gain-bandwidth product and other alterations, especially if DEM methods are employed because a better SNR is expected. Also, the capacitor values could be increased and the amplifiers more optimized for noise.

Table 5.5: Summary of the measured results and comparation with some others Converter

		[17]	[33]	[8][a]	[14]	This Work
Sampling frequency	(MHz)	1	6	0.25	5	1
Bandwidth	(kHz)	10	24	0.5	10	1
OSR		50	128	250	256	512
SNDR (SNR)	(dB)	80	89	76	84	87.5
ENOB	(bit)	13	14.5	12.3	13.6	14.2
Supply voltage	(V)	1	0.9	0.9	0.9	1.2
Power consumption	(µW)	22.4	1500	2.1	400	1158
Filter Order		2	3	2	2	2
FoM[b]	(pJ)	0.137	1.356	0.407	1.544	29.87
Technology node	(nm)	65	130	65	180	130

[a] Implementation of converter of report [8] with active filters.
[b] The formula used to calculate the FoM is (2.20).

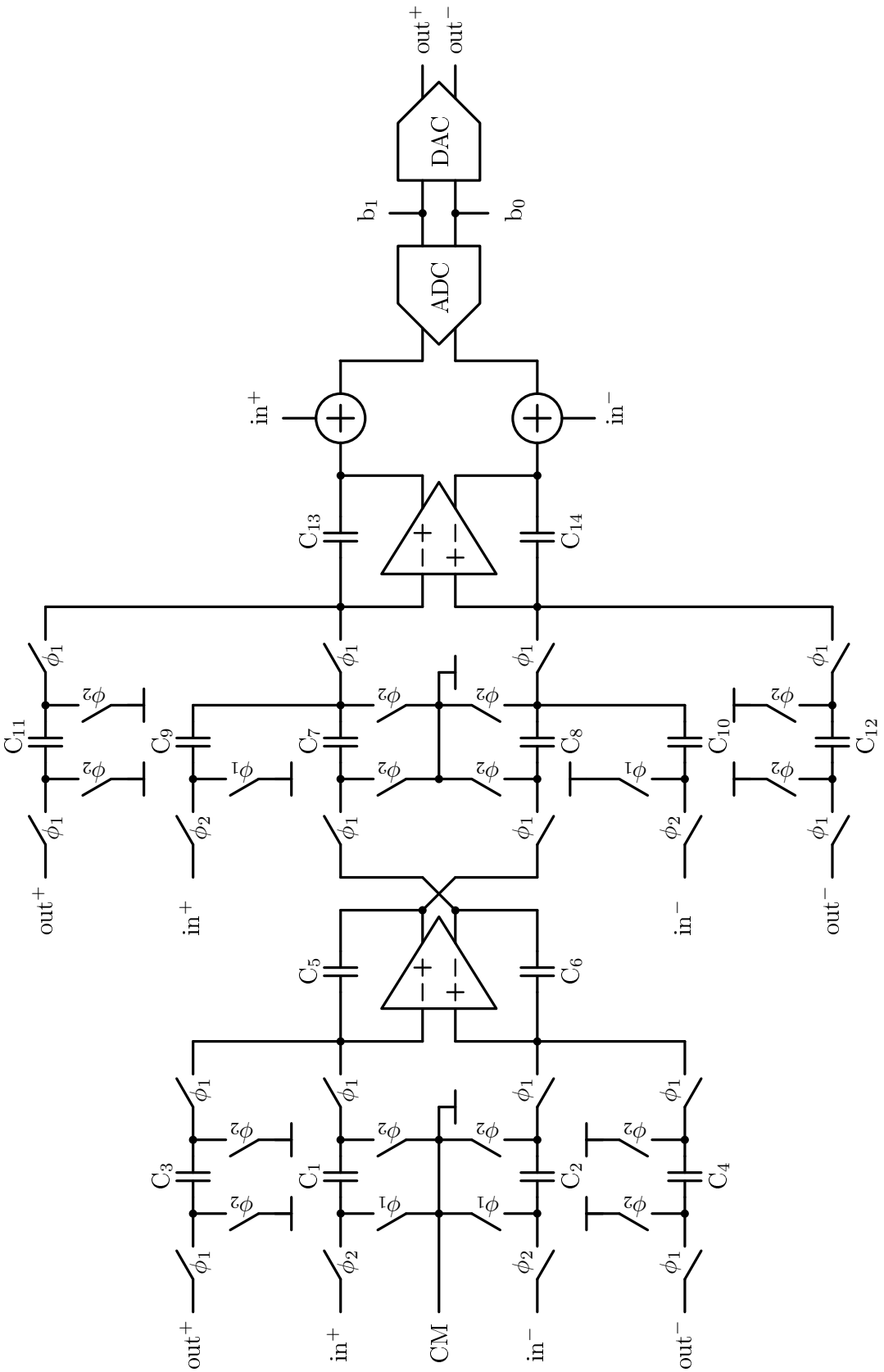


Figure 5.21: Sigma-Delta Converter

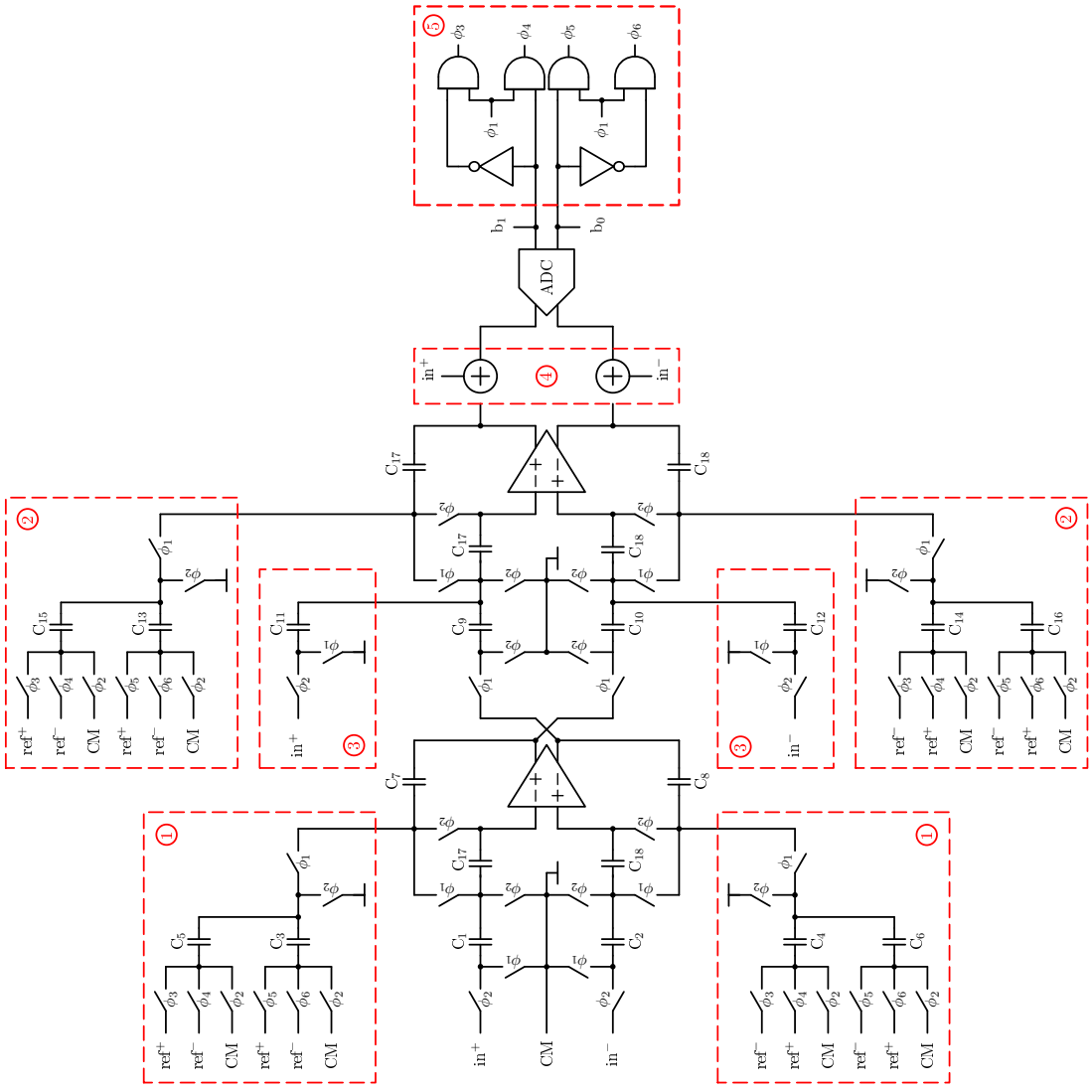


Figure 5.22: Sigma-Delta Converter – with DAC represented

Chapter 6

Conclusion

This chapter summarizes the work accomplished, and indicates possible future directions to improve its performance.

6.1 Summary

Portable medical devices are a relatively new reality that has gained more and more users. Doctors and others health professionals can carry these devices everywhere, because they are small, relatively cheap and battery powered. A health professional with these equipments can help saving lives in a emergency, because, even when not in the service, he or she can do a brief diagnostic, accelerating the process while medical help does not arrive. This is not the only application of this technology. These devices can substitute others that are heavier and consume more power. A sick person may have one or more of these equipments to do constant diagnosis to have a better control of the diseases. But these portable medical devices have some limitations, such reliability of results (i.e. effective resolution of analog-to-digital converter) and power efficiency.

To have a high-resolution converter, the Sigma-Delta Modulator is one of the best solutions, it does not need high-linearity blocks neither a high-resolution quantizer. There has been a high investment in the development of high-resolution, low-power and low-voltage converters, namely, in Sigma-Delta and SAR converters, in an attempt to obtain more reliable and more complete medical devices with an increasing autonomy.

In this dissertation, a 2^{nd}-order Sigma Delta Modulator with a 1.5 bit quantizer and a 1.5 bit DAC, together with a feed-forward scheme, was accomplished. It presents a non-classic two-stage, fully-differential, amplifier typology with a positive feedback scheme on the first stage, avoiding common-mode feedback at this stage. This proposal uses a high sampling rate (i.e. an OSR of 512) in order to obtain a higher SNR. The proposed architecture uses a 1.5 bit quantizer because it can be almost as linear as a 1 bit quantizer, improving the SNR without comprise the system linearity, which would limit the maximum SNR if the quantizer were of two or more bits.

The use of a fully-feed-forward topology (i.e. a feed-forward path to output of both opamps), such as that proposed in [17], allows higher input signals with a maximum supply voltage of 1.2 V, that is the maximum of selected transistors.

This Sigma-Delta Modulator was implemented using a 130 nm technology with a power supply of 1.2 V. The sampling rate is 1 MHz. For the proposed 1 kHz bandwidth, doing a transient analysis with noise, the measured SNR was 87.5 dB for a sinusoidal signal with maximum amplitude of 355 mV and frequency 562.5 Hz. The total consumed power was 1.158 mW.

The power consumption is higher than the wanted. But, knowing that the amplifiers are the most power hungry blocks, it should be possible to reduce the total power consume by do some tweaks to amplifiers. For example, the gain-bandwidth product of the amplifiers is larger than the necessary, so it is possible to reduce it to about 5 MHz, reducing the power consumption of the amplifiers by, potentially, five times. Other alterations can be done to improve the figure-of-merit of this work, such as the use of DEM methods to boost the effective SNR.

6.2 Applications

The main focus of the described converter is for low bandwidth signals, like bio-potential ones. The Table 6.1 shows the most important bio-signals and their approximate bandwidth.

Table 6.1: Bio-potential Signals

Bio-potential Signal	Bandwidth (Hz)
Electro-oculogram	10
Electroencephalogram	100
Electrocardiogram	600[a]
Electromyograms	5 k
Axon Action Potential	10 k
Audible Sound	20 k

[a] Since the majority of the information of heart beats are in the lower frequencies, this bio-potential signal can also be obtained using converter with lower bandwidth, as in [9].

The audible sound is important in the medical community, but it has a much wider use, so the development for audio devices is a bit different. As can be seen in Table 6.1, three of the other five signals can be obtained with the designed converter. In that way, this converter has a wide use possibility.

As said before, the battery-powered medical devices are increasingly a reality. So, it is important to develop this type of converters in order to reach better options. It is important to consume less and less power, as was stated throughout the document. Also, a high-resolution converter is

important to have more reliable results. These type of converters are to be implemented in devices to diagnose people, or animals, so better resolution means better diagnose, that, in its turn, means more saved lives.

6.3 Future Work

Like any scientific work, there are always place for improvements. Its specifications can be improved in order to be ready for industry and be used in a real portable medical device. Bellow, a list with ideas to improve the converter and continue the work are shown:

- The DAC is an important circuit to the resolution of a $\Sigma\Delta$ Modulator, because of its mismatches are not being filtered. In order to improve the DAC, a DEM circuit can be designed.
- The amplifiers of the circuit have an interesting design, but they are designed to have larges differential gain and gain-bandwidth product. They can be redesigned, each one with different specifications, in order be more power efficient.
- In the same way as amplifiers, the comparator StrongARM Latch can be redesign to be more power efficient and to have a better common-mode rejection, without prejudice the effective SNR.
- An alternative discarded was the use of a third order filter because of its small gain in relation to a second order one and the design difficulties thanks to its instability. But, with more time, it would be interesting do a design with it, to compare and select the best option.
- In order to have a a product ready to industry, decimator and clocks modules needs to be done, along with a more complex analysis such as Monte-Carlo Simulation, the layout of the transistor-level design with parasitic extraction and the fabrication and test of chip in a real world context.

Appendix A

Matlab Model

A.1 Simulink Model

The Simulink Model used by Maloberti's book was improved with the use of the non-linearities Saturation, Slew-rate and Opamp Finite Gain [2] in a single Model. This section do a brief description of them.

There are two integrator models, one with a delay on feedback path (i.e. does not delay the signal propagation) and another with de delay on forward path. But apart from that, the models are equal. The Fig. A.1 represents the first one. This block as an ideal closed-loop gain given by *Gain1* and gain error induced by intrinsic finite gain of a real opamp given by *gainerr1* and *phaseerr1*. It also have a definable saturation and a block that simulate the Slew-rate and the GBW limitations of Opamp.

Listing A.1: Function *slew*

```
function out = slew(in,alfa,sr,GBW,Ts)

% Models the op-amp slew rate for a discrete time integrator
% in:   input signal amplitude
% alfa: effect of finite gain (ideal op-amp alfa=1)
% sr:   slew rate in V/s
% GBW:  gain-bandwidth product of the integrator in Hz
% Ts:   sample time
% out:  output signal amplitude

tau=1/(2*pi*GBW);  % Time constant of the integrator
Tmax = Ts/2;
slope=alfa*abs(in)/tau;

if slope > sr                          % Op-amp in slewing
      tsl=abs(in)*alfa/sr-tau;         % Slewing time
      if tsl >= Tmax
            error=abs(in)-sr*Tmax;
```

```
19        else
20              texp=Tmax-tsl;
21              error=abs(in)*(1-alfa)+(alfa*abs(in)-sr*tsl)*exp(-texp/tau);
22        end
23  else                                    % Op-amp in linear region
24        texp=Tmax;
25        error=abs(in)*(1-alfa)+alfa*abs(in)*exp(-texp/tau);
26  end
27
28  out=in-sign(in)*error;
```

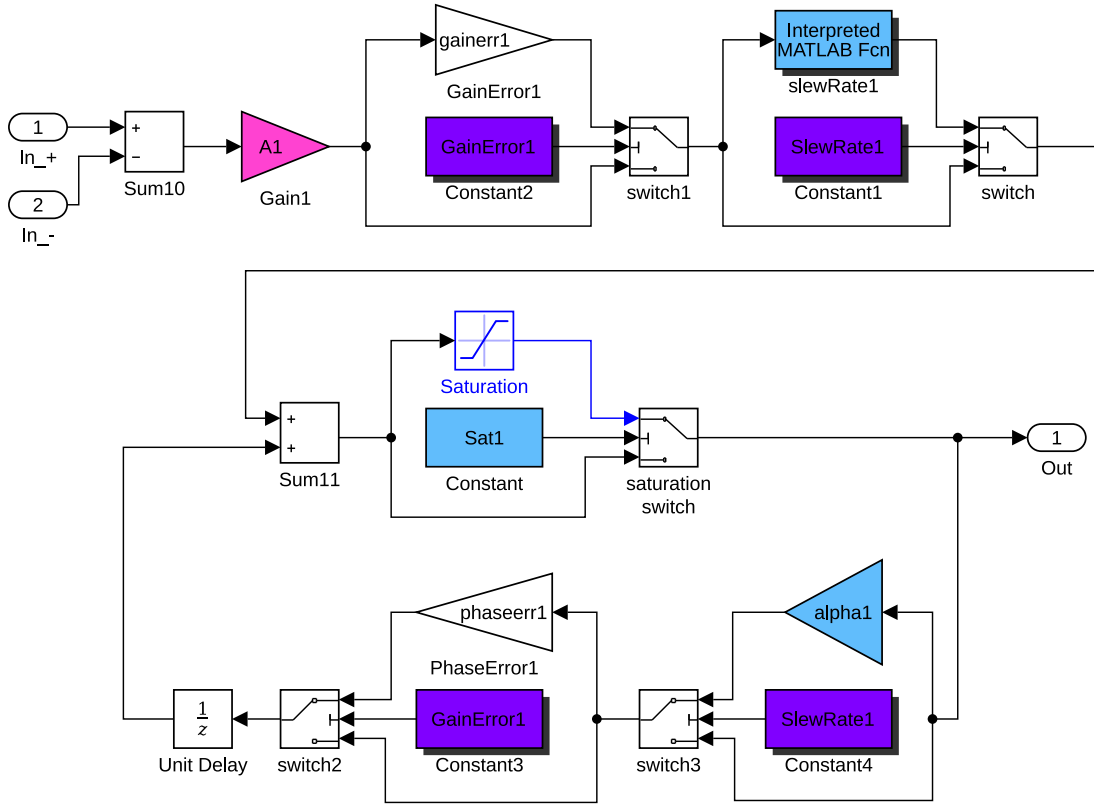


Figure A.1: Matlab model of the Integrator

A.2 Matlab Setup Code

The code snippets showed bellow is the main Matlab scripts used to simulate the system at logical level. Other scripts, such as plot generators or console prints of results are not transcribed in this appendix, but they are based on Maloberti's examples [2].

Listing A.2: Script to obtain the ideal SNR

```
% Sigma-Delta Converters tests
% Adaptation of Examples of chapters 6 and 7 of Maloberti's book
% ************************************************************

% Global Variables
bw=1e3;          % Base-band
R=512;           % Oversampling
Fs=R*2*bw;       % Oversampling frequency
Ts=1/Fs;         % Sampling time
N=1024*16;       % Samples number
nper=9;
Fin=nper*Fs/N;   % Input signal frequency (Fin = nper*Fs/N)
finrad=Fin*2*pi;% Input signal frequency in radians
%************************************************************

% Input Variables
Vref_dB=-5; % References for quantizer
Vref=10^(Vref_dB/20);

Amp_dB=Vref_dB-4;
Ampl=10^(Amp_dB/20);
Ntransient=100;
%************************************************************

% Component's Switches (0->OFF / 1->ON)
% Opamps Saturation Switch
Sat1=1;
Sat2=1;

% Quantizers Saturation Switch
satQuant1=1;

% Feed-Forward Switch
Feedforward1=1;
Feedforward2=1;

% Slew-rate Switch
SlewRate1=1;
```

```
39 SlewRate2=1;
40
41 % Gain Error Switch (page 268)
42 GainError1=1;
43 GainError2=1;
44 %*************************************************************
45
46 % Component's Variables
47 % Feedback Gain
48 FB1=1;
49 FB2=1;
50
51 % Feedfoward Gain
52 FF1=1;
53 FF2=1;
54
55 % Opamps Intrinsic Gain
56 A1_dB=68;
57 A2_dB=68;
58 AI1=10^(A1_dB/20);
59 AI2=10^(A2_dB/20);
60
61 % Capacitances Value
62 C1_1=250e-15;
63 C2_1=250e-15;
64 C1_2=250e-15;
65 C2_2=250e-15;
66
67 % Finite Gain Error
68 gainerr1=AI1/(AI1+1+C1_1/C2_1);
69 gainerr2=AI2/(AI2+1+C1_2/C2_2);
70 phaseerr1=(1+AI1)*C2_1/((1+AI1)*C2_1+C1_1);
71 phaseerr2=(1+AI2)*C2_2/((1+AI2)*C2_2+C1_2);
72
73 % Closed-Loop Gains of Opamps
74 A1=C1_1/C2_1;
75 A2=C1_2/C2_2;
76
77 % Opamps Saturation Level
78 sat1=1;
79 sat2=1;
80
81 % Feedback Gain to Compensate Slew-rate Block
82 alpha1=1-1/AI1;
83 alpha2=1-1/AI2;
```

```
84
85  % Slew-rate
86  sr1=5e6;
87  sr2=6e6;
88
89  % Quantizers Saturation Level
90  QuantSat1=Vref;
91
92  % "1.5 bits" Quantizer
93  Nbits=1.5;
94  Ncomp=2;
95  Nlevels=3;
96
97  % Open Simulink Diagram
98  options=simset('RelTol', 1e-3, 'MaxStep', 1/Fs);
99  sim(architecture, (N+Ntransient)/Fs, options);
100 %*************************************************************
101
102 % Calculate SNR and PSD using the bit-stream
103 f=Fin/Fs;                % Normalized signal frequency
104 fB=N*(bw/Fs);            % Base-band frequency bins
105 yy1=yout(2+Ntransient:1+N+Ntransient)';
106 [snr,ptot]=calcSNR(yy1(1:N),f,fB,N);
107 Rbit=(snr-1.76)/6.02;
108
109 end
```

Listing A.3: Calculation of the SNR

```
1  function [snrdB,ptotdB,psigdB,pnoisedB] = calcSNR(vout,f,fB,N)
2  % SNR calculation in the time domain (P. Malcovati, S. Brigati)
3  % (Maloberti's Book)
4  % vout: Sigma-Delta bit-stream taken at the modulator output
5  % f:    Normalized signal frequency (fs -> 1)
6  % fB:   Base-band frequency bins
7  % w:    windowing vector
8  % N:    samples number
9  % snrdB:     SNR in dB
10 % ptotdB:    Bit-stream power spectral density (vector)
11 % psigdB:    Extracted signal power spectral density (vector)
12 % pnoisedB:  Noise power spectral density (vector)
13
14 w=hann(N)';                                % Hanning Window
15 fB=ceil(fB);
16 signal=(N/sum(w))*sinusx(vout(1:N).*w,f,N); % Extracts sinusoidal signal
17 noise=vout(1:N)-signal;                     % Extracts noise components
```

```
stot=((abs(fft((vout(1:N).*w)'))).^2);       % Bit-stream PSD
ssignal=(abs(fft((signal(1:N).*w)'))).^2;    % Signal PSD
snoise=(abs(fft((noise(1:N).*w)'))).^2;      % Noise PSD
pwsignal=sum(ssignal(1:fB));                 % Signal power
pwnoise=sum(snoise(1:fB));                   % Noise power
snr=pwsignal/pwnoise;                        % SNR
snrdB=dbp(snr);
norm=sum(stot)/sum(vout(1:N).^2)*N;          % PSD normalization
if nargout > 1
        ptot=stot/norm;
        ptotdB=dbp(ptot);
end

if nargout > 2
        psig=ssignal/norm;
        psigdB=dbp(psig);
end

if nargout > 3
        pnoise=snoise/norm;
        pnoisedB=dbp(pnoise);
end
```

Listing A.4: Function *sinusx*

```
function outx = sinusx(in,f,n)
% Extraction of a sinusoidal signal (Maloberti's Book)
sinx=sin(2*pi*f*[1:n]);
cosx=cos(2*pi*f*[1:n]);
in=in(1:n);
a1=2*sinx.*in;
a=sum(a1)/n;
b1=2*cosx.*in;
b=sum(b1)/n;
outx=a.*sinx + b.*cosx;
```

Listing A.5: Function *dbp*

```
function y=dbp(x)
% dbp(x) = 10*log10(x): the dB equivalent of the power x
% (P. Malcovati, S. Brigati) (Maloberti's Book)
y = -Inf*ones(size(x));
nonzero = x~=0;
y(nonzero) = 10*log10(abs(x(nonzero)));
```

Appendix B

SNR Extraction

B.1 SNR Extraction from Cadence Model

The code snippet showed bellow is to extract the SNR value from Cadence simulation using the Matlab functions.

Listing B.1: Script to obtain the real SNR

```
% SNR from Cadence simulation
% ************************************************************
bw=1e3;          % Base-band
R=512;           % Oversampling
Fs=R*2*bw;       % Oversampling frequency
Ts=1/Fs;         % Sampling time
N=1024*16;       % Samples number
nper=9;
Fin=nper*Fs/N;  % Input signal frequency (Fin = nper*Fs/N)
finrad=Fin*2*pi;% Input signal frequency in radians
Ntransient = 100;

f=Fin/Fs;
fB=N*(bw/Fs);

% outY is the value obtained from a CSV file that is generated from
% Cadence Virtuoso Output
out=outY(2+Ntransient:1+N+Ntransient)';
[snr,ptot]=calcSNR(out(1:N),f,fB,N);

end
```

Appendix C

SNR Values for Different Converters

This appendix present calculated and simulated SNR values using different types of Converters, see Table C.1.

The specifications used to obtain these values was:

- Bandwidth = 10 kHz;
- OSR = 64;
- Input Frequency = 4770 Hz;
- No saturations;
- No Feed-forward;
- Infinite amplifier gain and slew-rate.

These specifications are not the used in the final design, but they gave a good feedback about the resolution advantages of different Converter topologies.

Table C.1: SNR Values for Different Converters

Type	Order	Quantizer (bit)	Calculated SNR (dB)	Simlated SNR (dB)	Simulated ENOB
loop-filter	1	1	56.8	59.2	9.3
loop-filter	1	2	62.8	65.0	10.5
loop-filter	1	3	68.8	69.5	11.3
loop-filter	1	4	74.9	75.9	12.3
loop-filter	2	1	85.2	74.3	12.1
loop-filter	2	2	91.2	86.4	14.1
loop-filter	2	3	97.2	95.3	15.5
loop-filter	2	4	103.2	103.2	16.8
MASH-1-1	2	1	85.2	79.5	12.9
MASH-1-1	2	2	91.2	89.4	14.6
MASH-1-1	2	3	97.2	97.1	15.8
MASH-1-1	2	4	103.2	105.1	17.2
MASH-2-1	3	1	111.4	96.1	15.7
MASH-2-1	3	2	117.4	116.6	19.1
MASH-2-1	3	3	123.5	125.3	20.5
MASH-2-1	3	4	129.5	131.3	21.5
MASH-2-2	4	1	117.4	109.3	17.9
MASH-2-2	4	2	123.4	144.3	23.7
MASH-2-2	4	3	129.4	153.5	25.2
MASH-2-2	4	4	135.5	163.0	26.0
MASH-1-1-1	3	1	111.4	108.6	17.7
MASH-1-1-1	3	2	117.4	118.5	19.4
MASH-1-1-1	3	3	123.5	125.5	20.6
MASH-1-1-1	3	4	129.5	131.8	21.6
MASH-2-1-1	4	1	117.4	122.8	20.1
MASH-2-1-1	4	2	123.4	143.8	23.6
MASH-2-1-1	4	3	129.4	151.3	24.8
MASH-2-1-1	4	4	135.5	159.6	26.2
MASH-2-2-1	5	1	138.8	113.4	20.1
MASH-2-2-1	5	2	144.8	166.2	23.6
MASH-2-2-1	5	3	150.8	167.4	24.8
MASH-2-2-1	5	4	156.8	167.7	26.2

MASH Converters naming system is in the form MASH-A-(...)-B, where A to B are the loop-filters and their values are the order of those filters. The calculated values for MASH are approximations using a simple loop-filter Converter with equal order.

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